ELECTRON BEAM LITHOGRAPHY FOR JOSEPHSON JUNCTION FABRICATION

by

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Electron beam lithography for Josephson junction fabrication

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ABSTRACT

This report briefly covers the work done at ERL, UCB, Berkeley, California, U.S.A., during the period from 16th April 1984 to 30th September 1984. The research goal was to develop an electron beam lithography technique on PMMA for the fabrication of Josephson tunnel junctions of sizes one micron and below using lift-off technique. Experiments were conducted for the evaluation of the necessary exposure and development parameters for fabricating 1 μm and 0.5 μm islands on PMMA for lift-off process. The lithography steps are reported as required for 1 μm and 0.5 μm junctions. The report is divided into the following sections. Section 1.0 describes the requirements on the technique to be developed. Section 2.0 describes the various approaches reported in the literature and some techniques investigated by the author during the period of this report. Section 3.0 discusses the experiments and results obtained for different mask levels involved in the Josephson junction device fabrication.

September 30, 1984

ACKNOWLEDGEMENT

(Life is a process of learning. In the process one gets to learn both good and evil. The wise remember only the good)

I wish to extend my sincere thanks to Prof T. Van Duzer for his constant attention during the course of research. My thanks are due to Prof. A. Neureuther for support and scientific discussions. I would like to thank Prof D. J. Angelakos, Dr. Amarjit Singh Dr. G. N. Acharya, and Dr. W. S. Khokle for sponsoring my deputation under this collaborative project between ERL and CEERI. My sincere thanks are due to Dr. Richard Ruby, Herbert Ko and to Albert Chen for introducing me to the various instruments and procedures of the laboratory. I thank P.R. Deshmukh for the data obtained from from his simulation studies and his constant company. I wish to convey my gratitude to all the members of the cryo group for making me feel at home. The thanks are due to Kevin Clark for his early take-over of the LEBES and pleasant company. I take this opportunity to convey my heart felt regards to my parents and sisters whose remote motivation helped me in becoming what I am.

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Section 1.0

1.0 Introduction

The fabrication steps for the sandwiched Josephson tunnel junctions is illustrated in figure 1 (a) and (b). The device consists of four layers. The base and counter electrode layers (B and C) are made of superconductive material (viz Pb) on silicon substrate (A). The tunnel barrier (E) is made by growing a thin oxide layer. The insulator layer (D) is necessary to isolate the base and counter electrodes and is made by evaporating silicon monoxide (SiO).

The base electrode is made using photolithography and lift off procedures. The insulation layer and the counter electrode are made using electron beam lithography and lift off. The Silicon oxide layer should have a central gap (either 1 μm or 0.5 μm square) for barrier growth and counter electrode contact. It is also required that the isolation layer cover the base electrode step (approximately 400nm) so that the counter electrode layer may be electrically isolated from the base electrode.

The requirements on the lithography technique developed are as follows:

1. Resist thickness must be about 1 μm to cover all the previous fabrication topography.
2. Overhangs structures to be developed for good lift off.
3. The pre- and postbake temperatures must be limited to 70oC to avoid softening of base electrode made

of lead.

4. The opening in the SiO layer should be one micron and below.

The lithography process to be developed must take into account the following constraints:

1. Overhang stability:

   To get a small opening (0.5 μm x 0.5μm) in the relatively large SiO layer (10 μm x 10 μm) on a 1 μm PMMA resist requires making self supporting resist structures with large aspect ratio.

   For good stability the ratio of the top and bottom dimensions of the overhang structures must not be greater than 3. (Collins and Halsted 1982)

2. Overhang size control:

   When the structures are made on diazo resists, the top and bottom dimensions of the overhang structure on resist can be independently controlled. This achieved by soaking in chlorobenzene.(Hatzakis et.al. 1980)

   This process is not compatible for the PMMA resist exposed by electrons.

   The ratio of the top and bottom dimensions of the overhang profile is dependent on the electron energy, substrate material and also the resist thickness.

   Unlike the case in the diazo resists it is not possible to control the top dimension independently.

But most of the cases the undercut profiles are obtained easily due to the backscattering of the electrons from the substrate and the base electrode.

3. The registration marks to be used must be high enough for good contrast in the secondary electron imaging.

Section 2.0

2.0 Lithography techniques

The definition of the junction gap is the most critical lithography step involved during the fabrication of a sub micron Josephson junction device using lift off process. When positive resists are used the gap is defined as the island left in the developed resist pattern for SiO deposition. Thus the research work is focussed on the techniques to fabricate a sub micron island.

Direct writing on 1 μm thick PMMA has been done to fabricate upto 1 μm width lift off structures. (Magerlein 1980) There have been attempts to use the photoresists for electron beam writing. A performance comparison of diazo resists (Shaw and Hatzakis 1978) under electron beam and optical exposure shows that the island width control is critical and it is difficult to get the under cut profiles as good as obtained in PMMA. Negative resists followed by reactive ion etching (Lessor et al. 1978) has been used and 2 μm lift off structures have been fabricated.

The strategy planned is to fabricate the tunnel gap by making two mutually perpendicular SiO layers as shown in figure 2. The advantages are:

1. Stability of the island rail formed after development as it is connected to the undeveloped resist area.
2. Easier lift-off because the same SiO thickness needed can be split into two steps.
3. Lower alignment inaccuracy as the length of the rail

is much larger than its width.

Thus the the fabrication of the Josephson device needs three levels of electron beam lithography. The first two insulator areas are exposed leaving the submicron island in the middle. SiO is deposited by evaporation and rest of the resist is lifted off. This layer must cover a step formed by the base electrode on the silicon substrate. The next layer of SiO made also by lift off has an orthogonal gap. The third layer is the counter electrode which covers the tunnel barrier grown on the base electrode in the opening between the two crossed SiO layers.

Section 3.0

3.0 Experimental results

Standardisation of the lithographic steps requires establishing the parameters such as resist thickness, spin coating time, pre-bake time and temperature, exposure dose, developer concentration and development time, evaporation, residue resist removal and lift-off process etc. This section describes the evaluation of these parameters.

3.1 **Resist thickness and spin coating.** The resist thickness obtained on a substrate by spin coating is given as:

$$T = \frac{K C^2}{\sqrt{S}} \qquad (3.1)$$

Where, T is the resist thickness (in Angstroms), C is the concentration of resist solution (in %), S is the spinning speed (in rpm) and K is a constant of proportionality which depends on the intrinsic viscosity of the polymeric material and hence a function of the molecular weight of the polymer (Thompson and Kerwin 1976). Experiments show that the thickness of the resist coated on to a wafer decreases uniformly away from the resist center. To control the thickness of the resist within 5% of the value obtained from above equation it is found that the spin rate is optimal at 6000 rpm. Table 3.1 lists the

thickness obtained for various resists:

Table 3.1

Resist	spin rate (rpm)	Thickness(T in μm)	ΔT (%)	K
PMMA (4%)	6000	0.25	3	12103.07
"	3000	0.35	5	-
PMMA (9%)	6000	1.30	5	12431.80
AZ 1350 J	6000	1.50	6	-
AZ 1350 B	6000	0.50	3	-
"	3000	0.70	4	-

The resist were coated at various spin speeds and baked at 70oC (Lead softens above this temperature). The refractive index was measured using ellipsometric techniques. The refractive index for PMMA baked at 70oC for 2 hours is measured to be 1.48. The film thickness was measured using the Nanospec thickness monitoring instrument. The K values for the PMMA were calculated from equation 3.1.

3.2 Prebaking

It is necessary to bake the resist to remove the residual solvent after spin coating. The product of baking temperature and time controls the glass transition phase of the resist polymer. Above this temperature the resist undergoes glass to rubber transition and releases all the internal stresses developed during spin coating. The upper temperature of pre-bake depends on the stability of the resist. Above this temperature the negative resists cross-link and the positive resists degrade. Table 3.2 lists these temperatures for various electron resists.

Table 3.2

Resist	Tgt (oC)	Tu (oC)	Reference
PMMA	110	200	Harris R.A. (1973)
PBS	95	140	Bowden et al (1975)
P(GMA-CO-EA)	20	-	Feit et al (1980)

Tgt = Glass transition temperature.
Tu = Temperature of unstability.

3.3 Exposure

Test patterns were exposed on a silicon wafer coated with PMMA. These included (figure 3):

1. Some line patterns with varying width and gap.

2. Large areas laid out with varying exposure.

3. Some patterns exposed for the experimental evaluation

of proximity effect.

These patterns were exposed with varying doses ranging from 20- 1000 μC. The average dose values are plotted (figure 4) as a function of the exposure time per spot and the stepping distance.(Raja N.K.L. 1984) After development in 1:10 MIBK:IPA for 20 seconds, it was observed that the patterns exposed in the dose range

$$200\ \mu C < \text{Dose} < 300\ \mu C$$

were perfectly developed and the rest were either under or over developed. The volume enclosed between threshold planes corresponding to doses 200 and 300 uC and the dose surface contains the points P1, P2 and P3 which are most suitable for exposure. The parameters for these points are given in the Table 3.3.

Table 3.3

Point	Exp. Time (in μs)	Step distance(in nm)
P1	1.2	15.26
P2	1.6	15.26
P3	2.0	22.89

3.4 Initial experiments.

Cross-sectional profiles of lines drawn PMMA/Si were studied for determining the side wall slope. Three different exposures (figure 5 - 7) were made in the range computed from the line charge density obtained from the EDF computations (Deshmukh P. R., 1984). The development time was 20 seconds in 1:10 MIBK:IPA.

The Lebes instrument uses the standard Everhart Thornley Secondary electron detector for detecting the signals from the registration marks made on the electron resists. The contrast in the detected signal falls rapidly as the resist thickness increases. Thus it is necessary to find the minimum registration step heights for various resist thicknesses. The minimum necessary heights of the registration marks, made of lead on a Pb/Si substrate and covered with PMMA (figure 8), in order to be detectable during the process of re-registration, are

shown in Table 3.4.

Table 3.4	
Resist thickness (μm)	Registration mark height (nm)
1.2	400
0.25	100

Islands of PMMA were made with a nominal gap of 1.0 μm (figure 9). About 200 nm thick SiO layer was deposited by evaporation and lift-off techniques (figure 10). The top width of the island varies from about 0.6 μm in the middle of the pattern to about 0.9 μm at the corners. This can be attributed to the proximity effects in exposure.

When nominal gap width was chosen to be 0.5 μm, it was found that the control on the exposure and development time is very poor. Figure 11 and 12 show two samples of the pattern exposed and developed in identical conditions. In the latter, the backscattered electron exposure is so high that the island structure of PMMA is lifted-off. This phenomenon is predicted by the theoretical plots of of the energy deposition curves at the top and bottom layers of the resist shown in figure 13 (Deshmukh P. R., 1984).

3.5 Cross-linking

A futile attempt was made fabricate the island for SiO lift-off by cross-linking the region (figure 14). The doses used were above 2000 μC. Although it is possible to cross-link the required region, this method fails because of excessive dose spread to neighbouring regions leading to unwanted development.

3.6 Josephson Device

The general layout of the test chip to be made by the electron beam lithography is shown in figure 15. This contains two devices which differ in the number of the SiO layers used. Figure 16 shows the layout of the device with single SiO layer and the base and counter electrode layers. In figure 17 two SiO layers which are oriented perpendicular to each other are shown.

The results of processing of these steps are shown in figures 18 and 19. The structures made with nominal island width of one micrometer are shown in figure 18 and those with nominal island width of half a micrometer are depicted in figure 19. Figure 20 shows the 1 μm X 1 μm opening in the middle of the crossed SiO layers. The step coverage of second SiO layer can be seen in figure 21.

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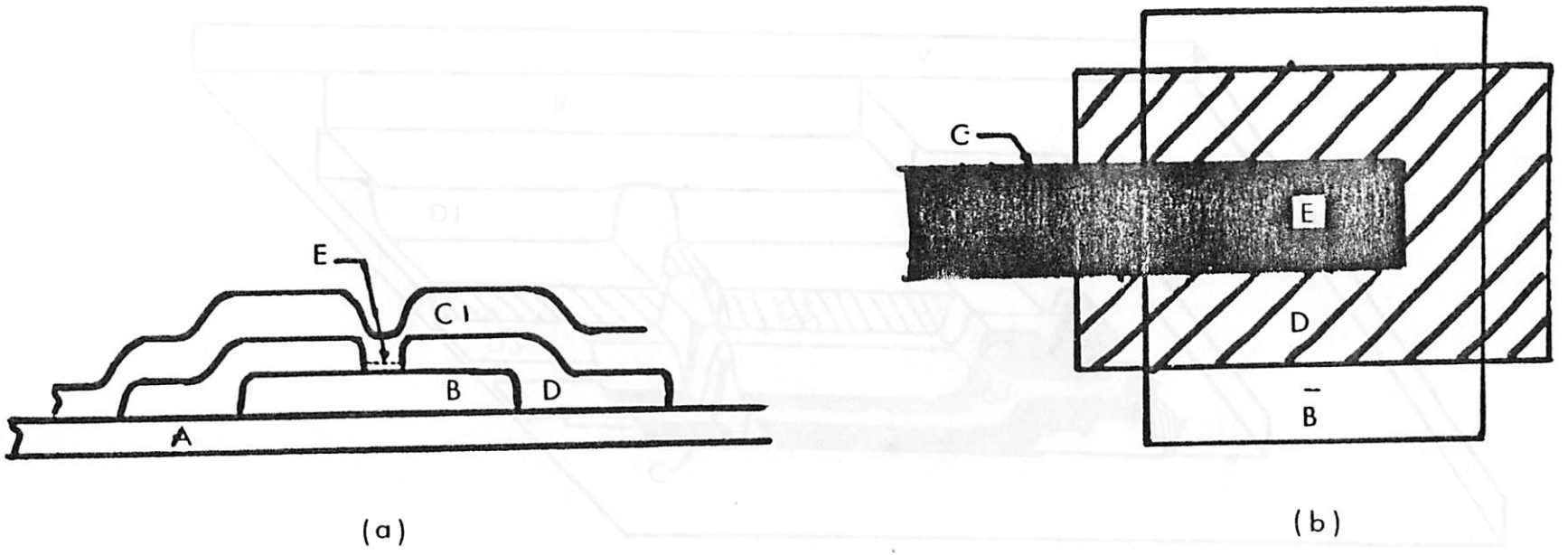


Figure 1. The sandwiched Josephson tunnel barrier junction cross-section (a) and top view (b).
A = Silicon substrate,
B = Base electrode (Lead),
C = Counter electrode (Lead),
D = Insulator (Silicon monoxide) and
E = Tunnel oxide.

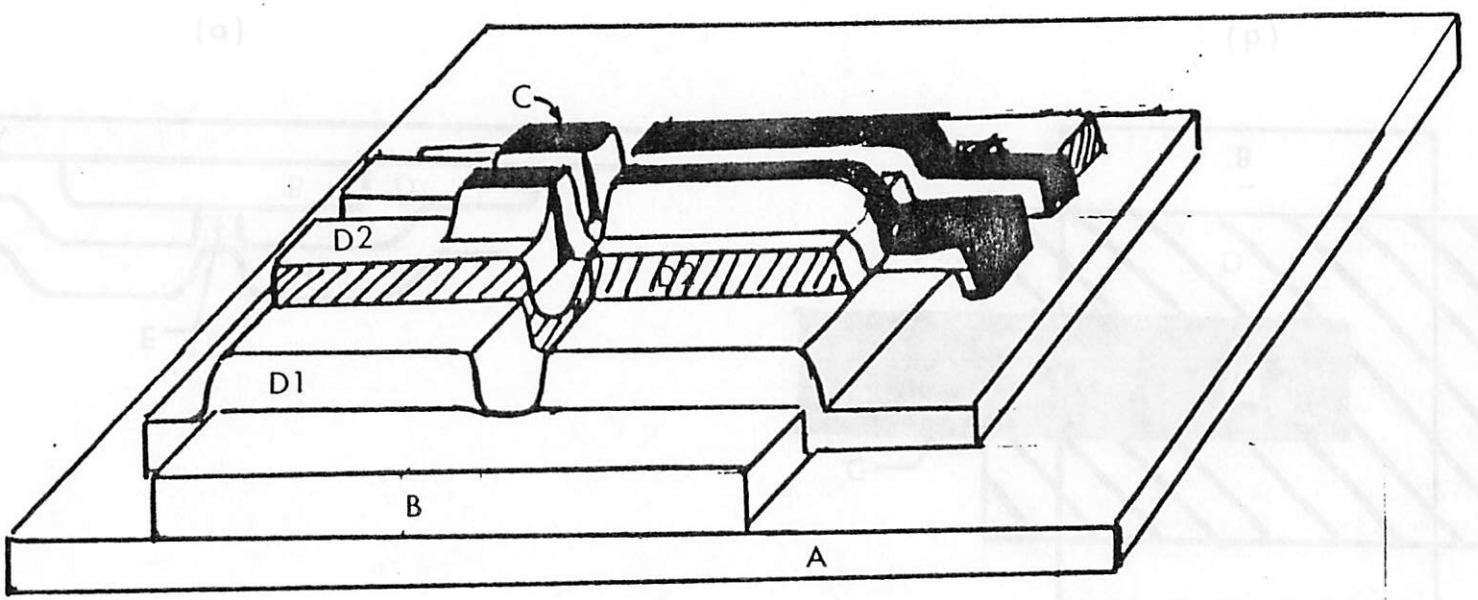


Figure 2. The Crossed insulator layer Josephson junction.
The layers D1 and D2 denote the SiO layers.

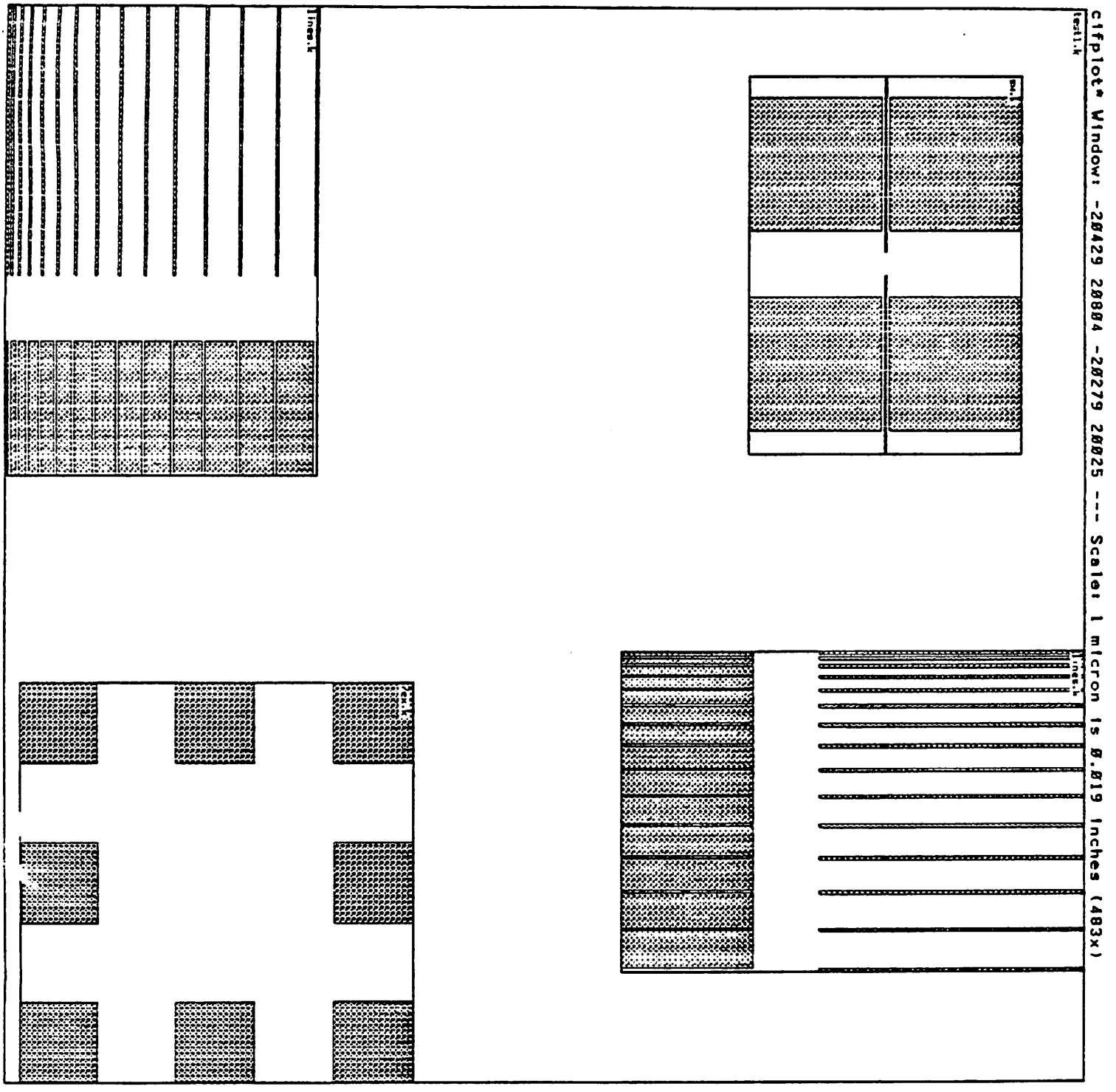


Figure 3. Test patterns used for the evaluation of exposure dose, resolution limit and proximity effect.

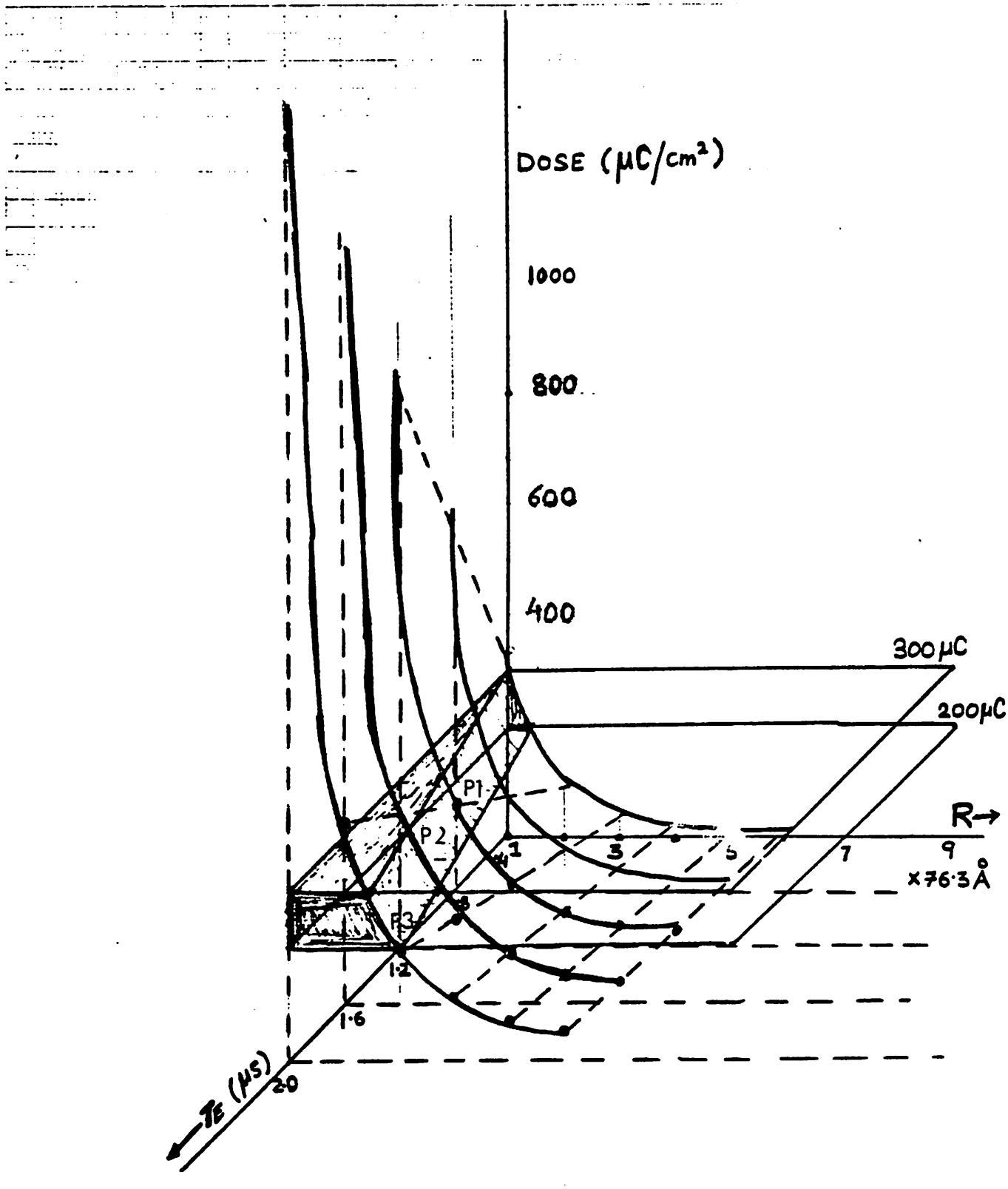


Figure 4. Plot of the dose surface as function of the exposure time and stepping distance. The shaded area is found to be the best exposure region for 0.3 to 1.0 μm PMMA.

Figure 5. Line profile (PMMA on Silicon) at 60o tilt.
Exposure line charge density = 6.55 x 10-9 C/sq.cm.

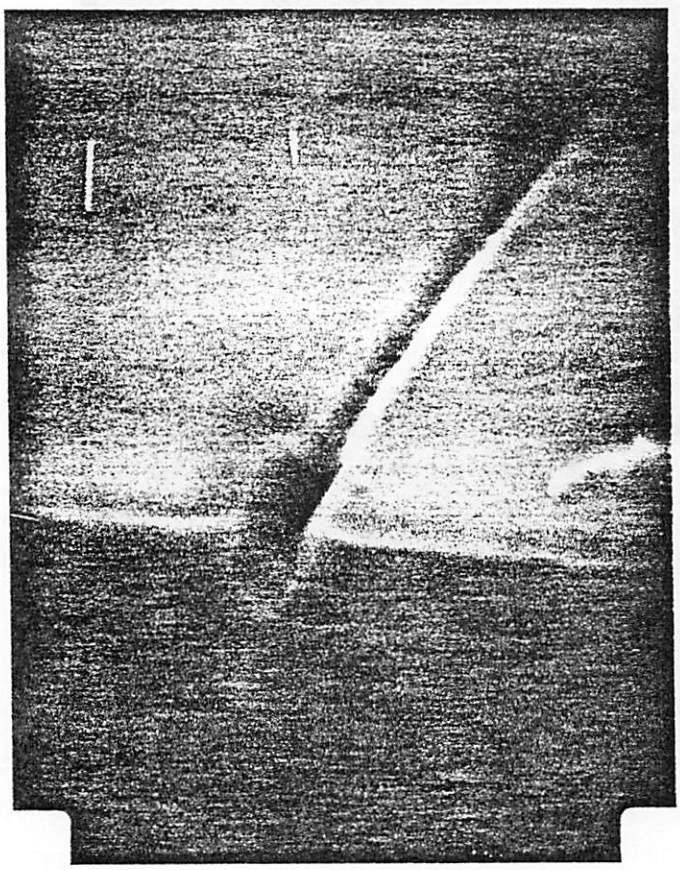


Figure 6. Line profile (PMMA on Silicon) at 60o tilt.
Exposure line charge density = 9.82 x 10-9 C/sq.cm.

Figure 7. Line profile (PMMA on Silicon) at 60o tilt.
Exposure line charge density = 13.10 x 10-9 C/sq.cm.

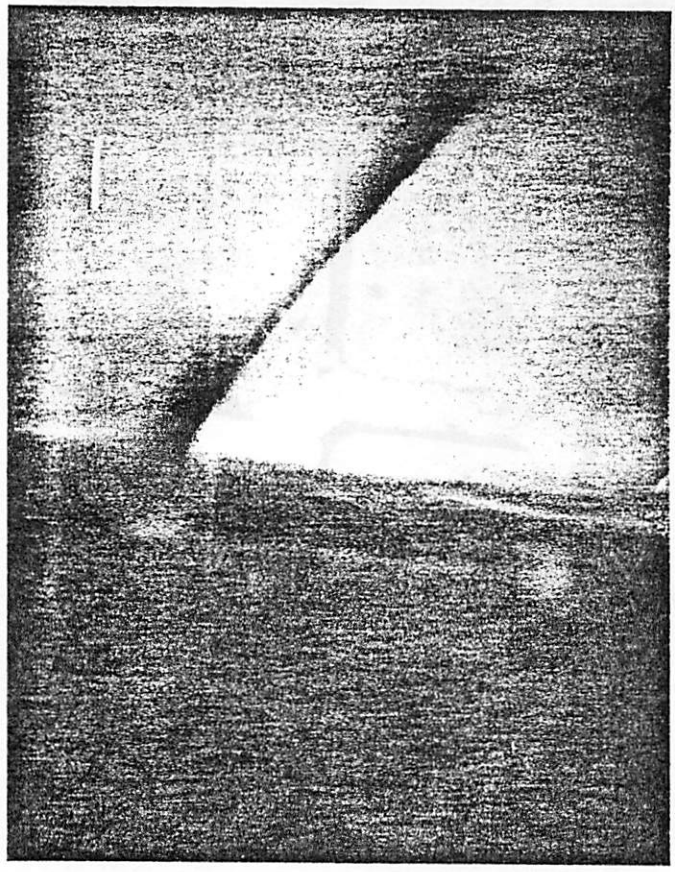
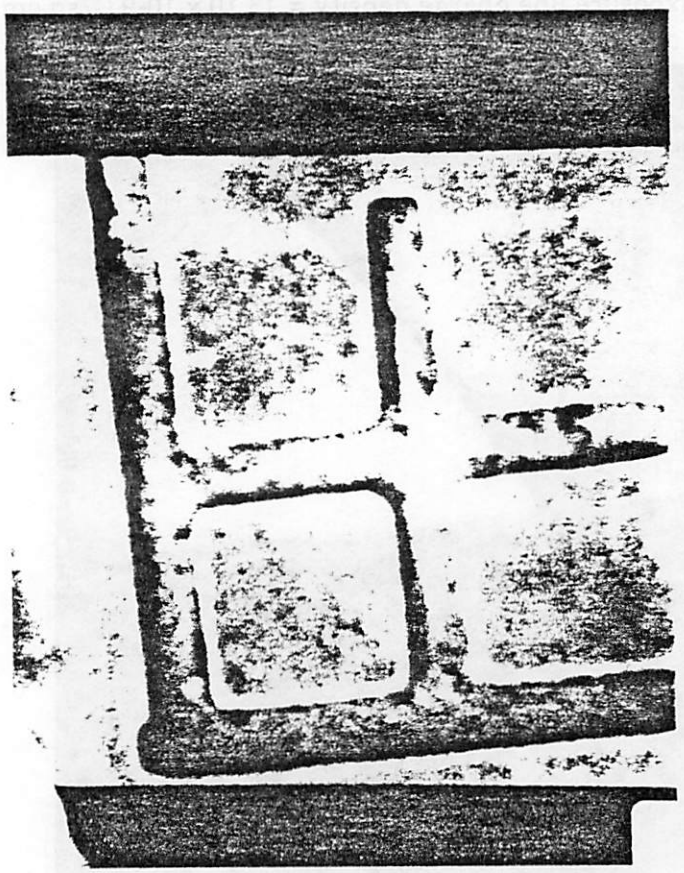


Figure 8. Registration mark made of 400 nm Pb on Silicon Substrate coated with 1.2 μm PMMA.



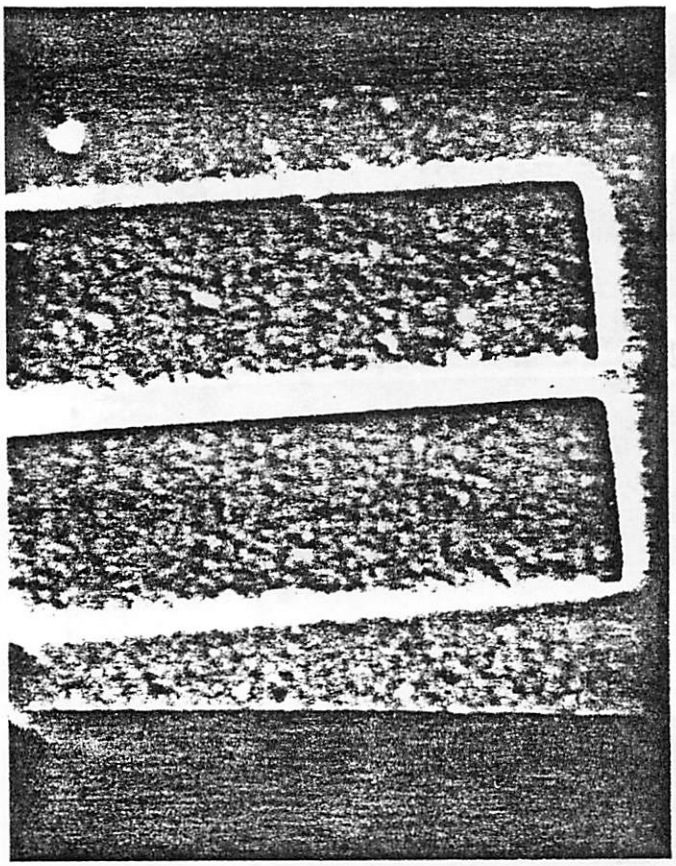


Figure 9. Island of PMMA for lift-off. 1.2 μm PMMA on Pb/Si.
Width of the SiO opening = 5.2 μm
Length of the SiO opening = 9.0 μm

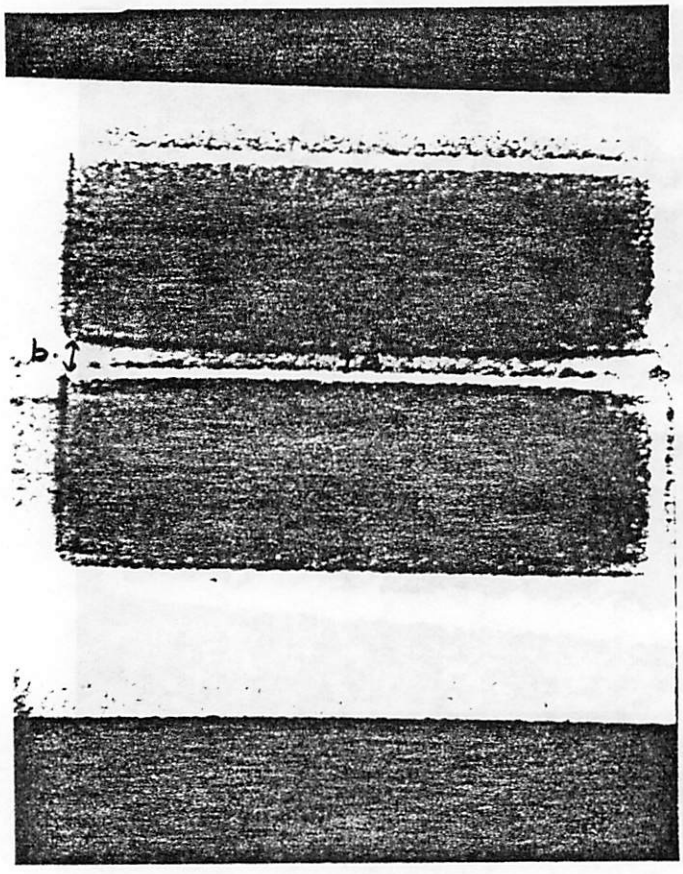


Figure 10. After SiO lift-off.
a = 0.6 μm, b = 0.9 μm

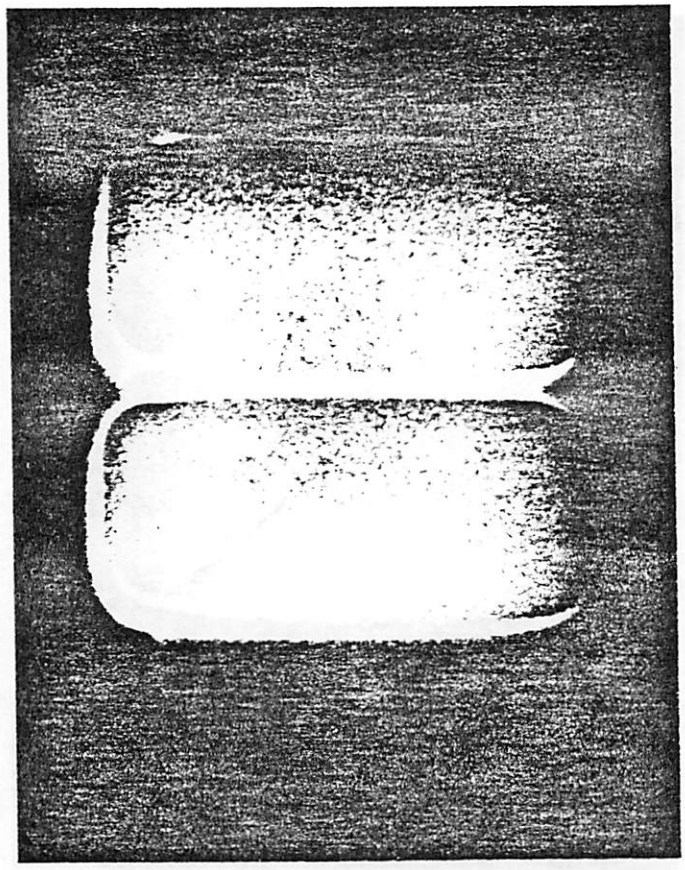


Figure 11. Critical development. 1.2 μm PMMA on Silicon. Development time 20 seconds in 1:10 MIBK:IPA The lower layer of resist in the middle of the island is probably developed and a microbridge is formed.

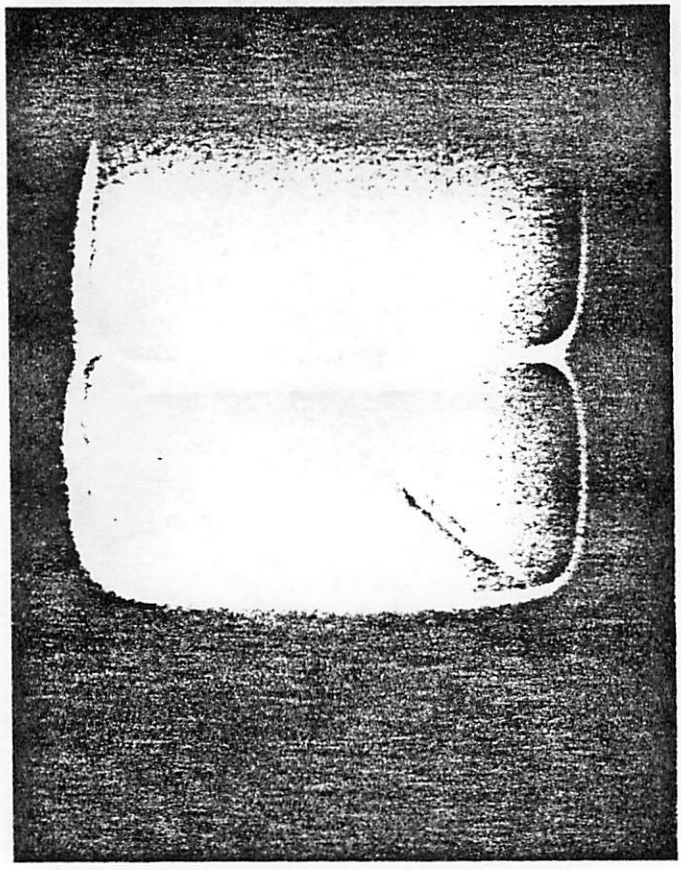


Figure 12. The broken bridge with the collapsed island. The parts of the resist island at the corners are sticking to the substrate due to relatively lower exposure at the corners.

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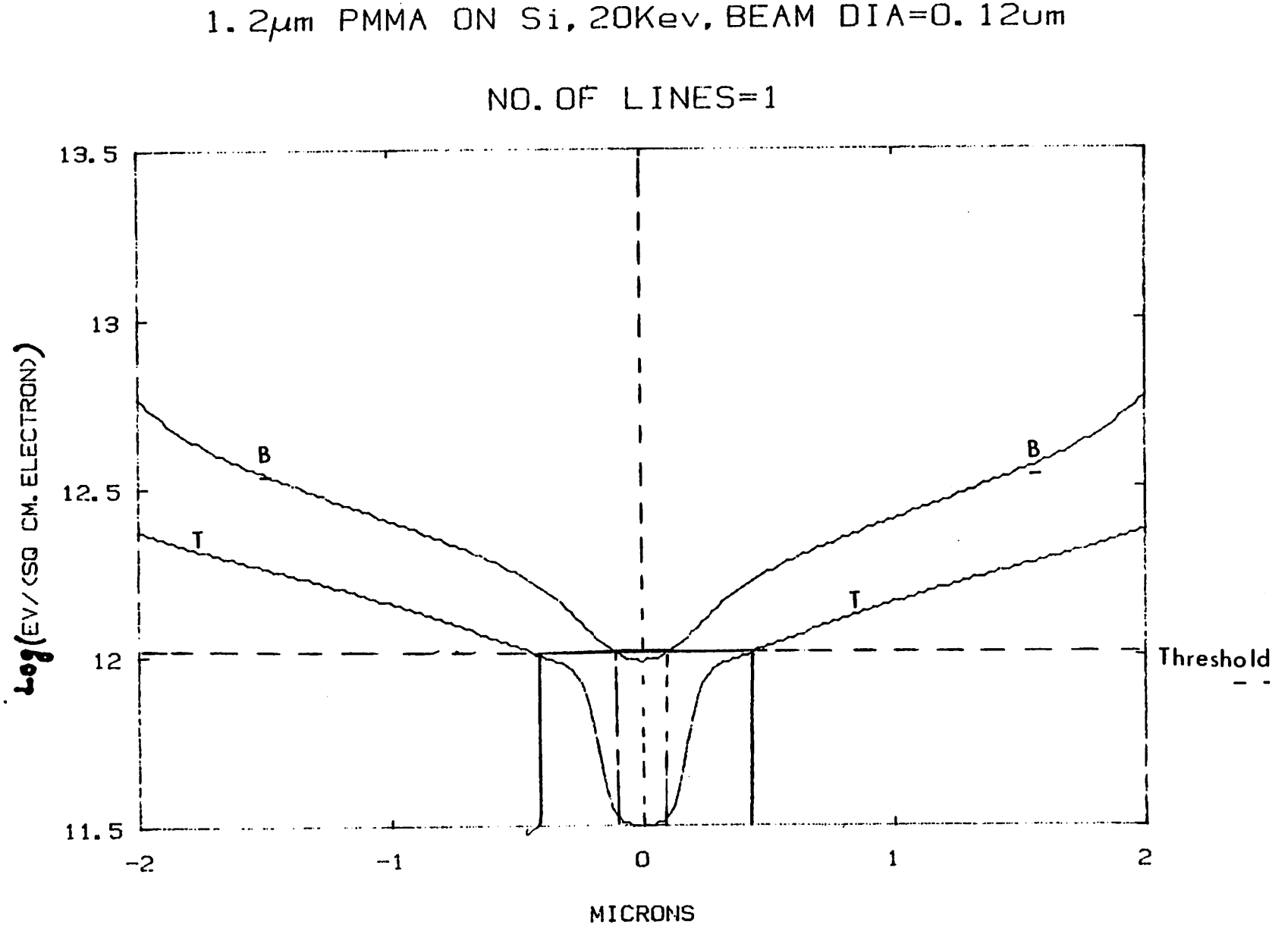


Figure 13. Energy deposition curves in the region of the island.
T = Top layer; B = Bottom layer.
The vertical lines correspond to a top width
of 0.64 μm. The threshold barely passes
through the bottom curve.

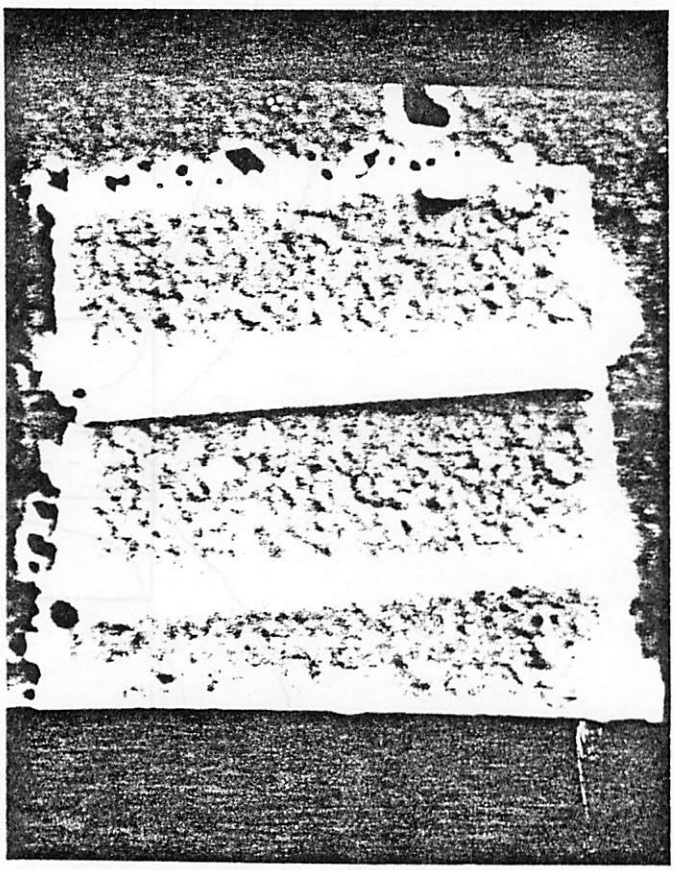


Figure 14. Cross-linked island. PMMA on Silicon.
Dose = 2000 μC per sq. cm.

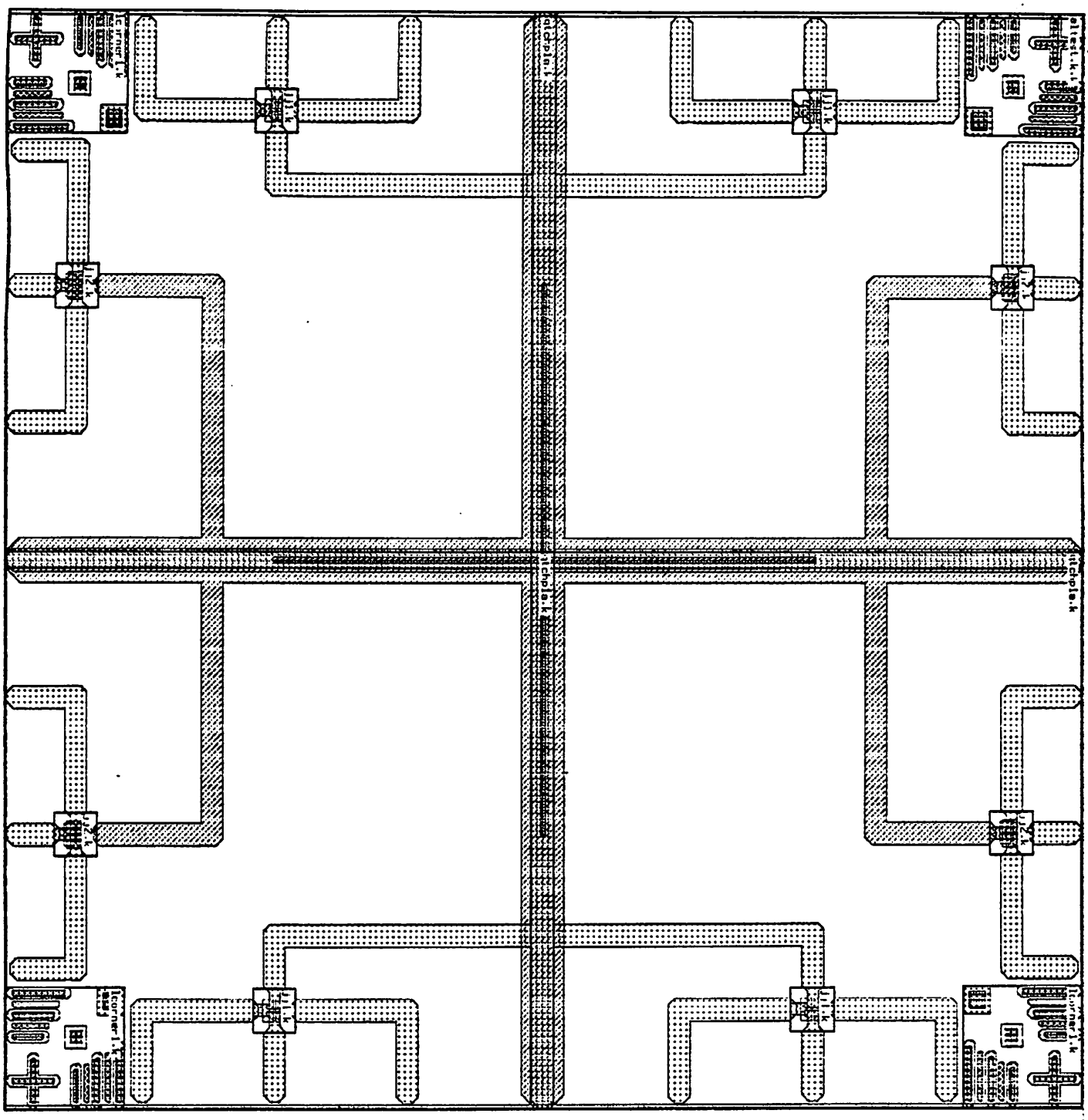


Figure 15. Layout of the Josephson junction device and interconnections.
Field size = 0.5 mm x 0.5 mm.

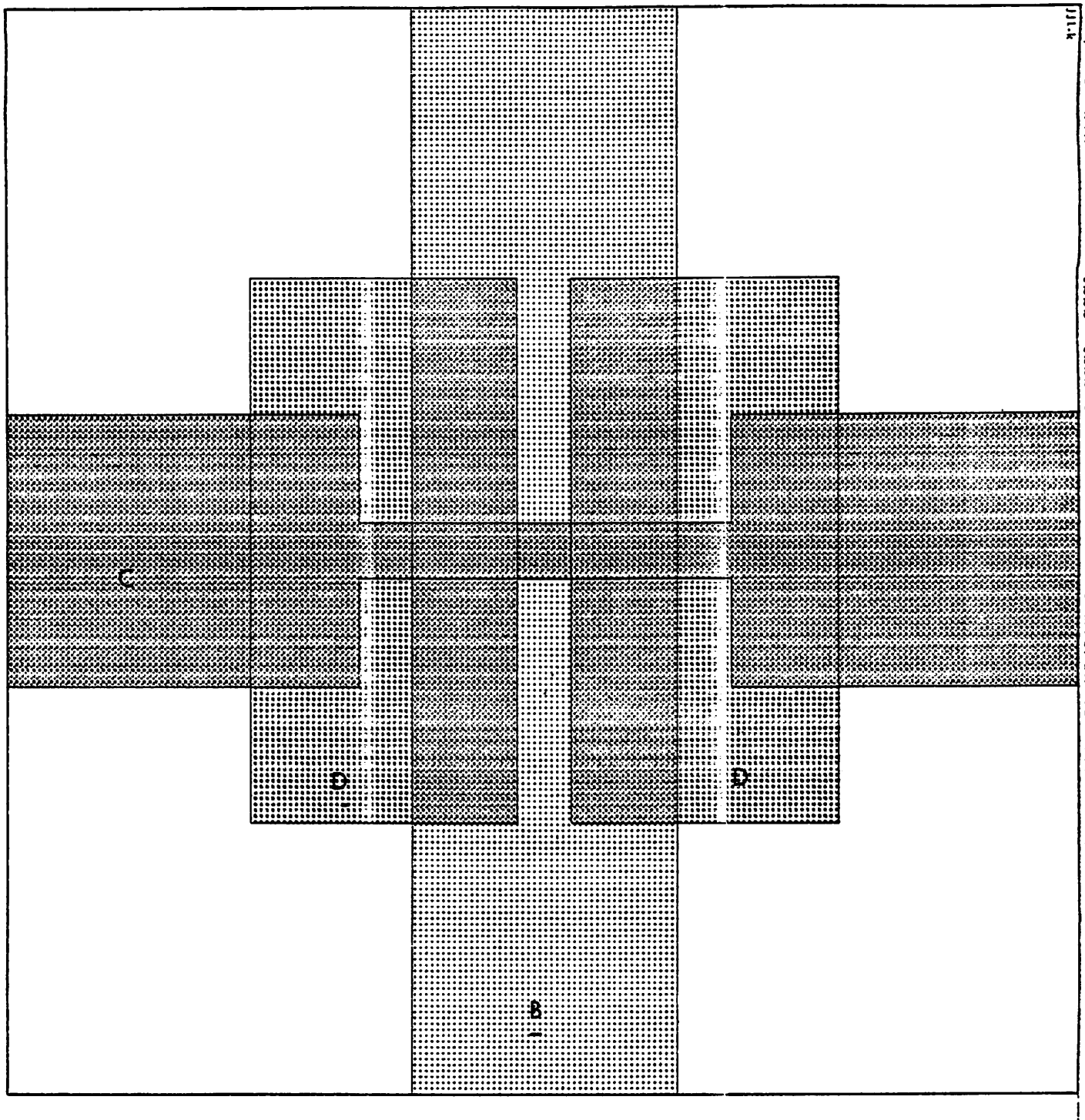


Figure 16. Josephson device layout : Single SiO layer.
B = base electrode, C = counter electrode,
D = SiO insulator layer.

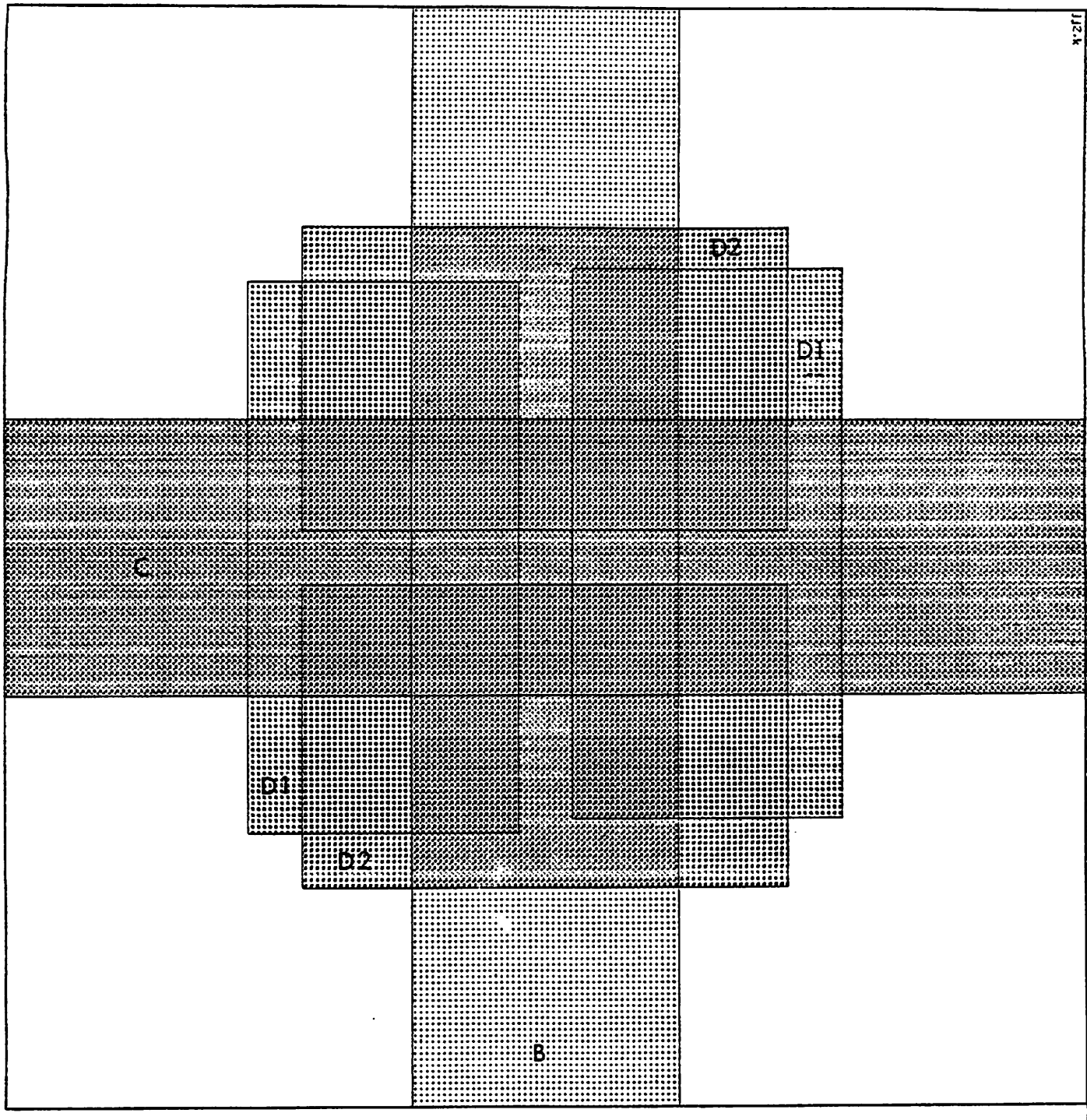


Figure 17. Josephson device layout : Double SiO layer.
B = base electrode, C = counter electrode,
D1 = first SiO insulator layer,
D2 = second SiO insulator layer.

Figure 18. Double SiO layer lithography.
1.0 μm nominal junction size.
width measured = 0.969 μm

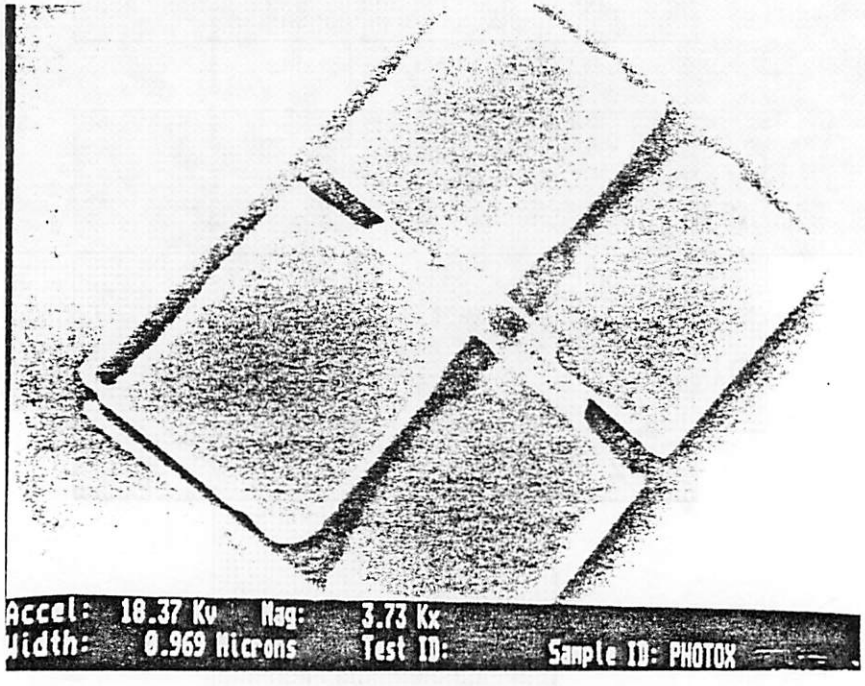


Figure 19. Double SiO layer lithography.
0.5 μm nominal junction size.
width measured = 0.409 μm

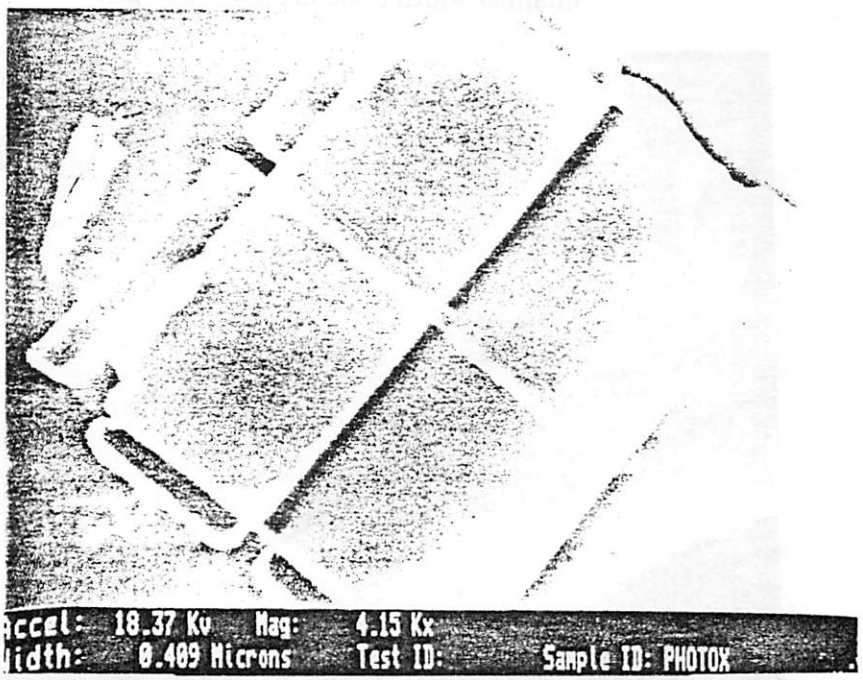
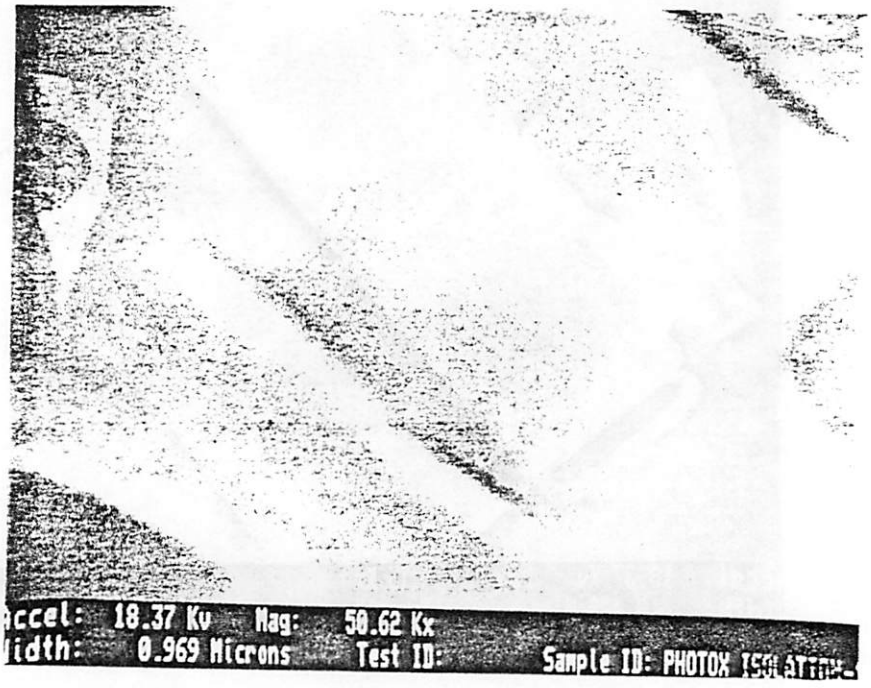


Figure 20. Tunnel barrier opening in the double SiO layer process.
Smallest width measured = 0.969 μm



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