VIOLATION OF PORT CONDITIONS IN THE INTERCONNECTION OF MULTIPORTS

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Violation of Port Conditions in the Interconnection of Multiports

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Abstract

We present simple topological conditions to check whether the port conditions of individual multiports are satisfied when they are interconnected to make up a larger multiport.

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1. Introduction

In certain network synthesis procedures the desired multiport is built up by the interconnectionof a number of smaller multiports (see pp. 191-193 of [1]). It is then of interest to know whether the port conditions of the individual multiports are satisfied inthe final multiport. This problem has been solved in some restricted cases of practical interest by using the Brune-test (see p. 192 of [1]). However the solution is not easy to extend to the general case. In this paper we present a simple general solution for a variation of the original problem. If certain precautions are taken the deviation from the original problem does not appear to be practically significant.

2. Preliminaries

By $S \uplus T$ we mean the union of S and T and further that S, T are disjoint $\underline{f} : S \to \mathbb{F}$ is said to be a vector on S over the field $\mathbb{F}$. We denote by $\underline{f}/T$ the restriction of a vector on S to a subset T of S. Addition and scalar multiplication of two vectors on the same set are defined in the usual way. A collection of vectors on the same set closed under addition and scalar multiplication is called a vector space. If ν is a vector space on S and $T \subseteq S$ then $\nu \cdot T$ is the restriction of all vectors of ν to T; $\nu \times T = \{\underline{g}_T : \underline{g}_T = \underline{f}/T, \ \underline{f} \in \nu \text{ and } f(e) = 0, \ e \in S-T\}$. Let G be a directed graph on S. Then the collectionof cycles (solutions of KCE) of G forms a vector space on S denoted by $\nu_{cy}(G)$. The collection of coboundaries (solutions of KVE) of G forms a vector space on S denoted by $\nu_{cob}(G)$. Let $T \subseteq S$. $G \times T (G \cdot T)$ is the directed graph obtained from G by short (open) circuiting and removing all edges in (S-T).

If $\underline{f}, \underline{g}$ are vectors on S then $\langle \underline{f}, \underline{g} \rangle = \sum_{e \in S} f(e) \cdot g(e)$. We say that $\underline{f}, \underline{g}$

are orthogonal to each other iff $\langle \underline{f}, \underline{g} \rangle = 0$. If ν is a vector space on S the collection of vectors orthogonal to every vector in ν also forms a vector space and is denoted by ν^*. Tellegen's Theorem states that $\nu_{cob}(G) = (\nu_{cy}(G))^*$, for any directed graph G.

3. The Multiport Connection Problem

We illustrate this problem through an example. In Figs. 1(a), 1(b) we have shown the directed graphs $G_{S_1P_1}$, $G_{S_2P_2}$ of two 2-ports. They are connected together in 'series' to yield a 2-port whose directed graph is shown in Fig. 1(d). We would say that the port conditions of the 2-port of Fig. 1(a) are satisfied in the larger 2-port of Fig. 1(e) if the current leaving the former 2-port at a,b respectively is equal to the current entering at a', b' respectively. However in the final multiport of Fig. 1(e) nodes a', b' get fused with other nodes. It is therefore more convenient to phrase the port conditions as current constraints on the internal currents of the multiport. In this case this means that $i_1 = -i_4$ and $i_2 = -i_5$. Equivalently we may state this condition as follows: Let $\underline{i}_{SP_e}$ be a current vector of the multiport on graph G_{SP_e} Then $\underline{i}_{SP_e}/S_1$, $\underline{i}_{SP_e}/S_2$ should be restrictions of cycles of the graphs $G_{S_1P_1}$ and $G_{S_2P_2}$. (In this case $S_1 = \{1,2,3,4,5\}$, $S_2 = \{6,7,8,9,10\}$.) However this test is inconvenient since it requires the solution of the multiport on G_{SP_e}. It is much quicker but almost as informative to examine whether, whenever $\underline{i}_{SP_e}$ is a cycle of G_{SP_e}, $\underline{i}_{SP_e}/S_1$, $\underline{i}_{SP_e}/S_2$ are restrictions of cycles respectively of $G_{S_1P_1}$ and $G_{S_2P_2}$. We formalize these ideas below. The multiport connection problem may be stated as follows: We are given multiports $N_{S_iP_i}$ (i=1,...,n) with directed graphs

$G_{S_iP_i}$ on the sets of edges $S_i \uplus P_i$ (i=1,...,n) where the sets S_i (i=1,...,n), and the sets of ports P_i (i=1,...,n) are disjoint. The multiports are to be connected together according to the directed graph (the 'port connection diagram') G_p on the set of edges $(\uplus P_i) \uplus P_e$. The result is a multiport N_{SP_e} on the directed graph G_{SP_e} on the set of edges $S \uplus P_e$ where $S = \uplus S_i$. We now have two port connection problems

(a) (Topological) is $(\nu_{cy}(G_{SP_e}))$. $S_i \subseteq (\nu_{cy}(G_{S_iP_i}))$. S_i, (i=1,...,n)?

(b) (Practical) Does $\underline{i}_{SP_e}/S_j \in (\nu_{cy}(G_{S_jP_j}))$. S_j, (j=1,...,n), whenever $(\underline{v}_{SP_e}, \underline{i}_{SP_e})$ is a solution of N_{SP_e}?

If (a) holds we say that in the multiport N_{SP_e} the topological conditions of $N_{S_iP_i}$ (i=1,...,n) are met whereas if (b) holds we say the practical port conditions are met. Observe that the topological conditions are stronger than the practical conditions i.e., in order that the port conditions of the individual multiports are satisfied in a practical circuit it is sufficient but not necessary that the topological conditions are satisfied.

Example 1

Let us reexamine the graphs of Fig. 1 following the notation established in the statement of the port connection problem. Figs. 1(a), 1(b) show directed graphs $G_{S_1P_1}$, $G_{S_2P_2}$ of multiports $N_{S_1P_1}$, $N_{S_2P_2}$. Here $S_1 = \{1,2,3,4,5\}$, $S_2 = \{6,7,8,9,10\}$, $P_1 = \{p_1,p_2\}$, $P_2 = \{p_3,p_4\}$. The multiports $N_{S_1P_1}$, $N_{S_2P_2}$ are to be connected according to the directed graph (the 'port connection diagram') G_p in Fig. 1(c). (In this case this is equivalent to connecting the two 2-ports in 'series'). The resulting multiport N_{SP_e} has the directed graph G_{SP_e}. The set of ports P_1, P_2 do not appear in the final multiport N_{SP_e}. They are used only

to indicate the mode of connection.

We need the following well known result [2] from graph theory for solving the (topological) port connection problem. We omit the proof.

Theorem 1

Let G be a directed graph on S. Let $T \subseteq S$. Then

$$\nu_{cy}(G \times T) = (\nu_{cy}(G)) \cdot T.$$

We now state the main result of this paper.

Theorem 2

The topological port conditions of $N_{S_i P_i}$ $(i=1,\ldots,n)$ are met in the multiport N_{SP_e} iff $\nu_{cy}(G_{S_i P_i} \times S_i) \supseteq \nu_{cy}(G_{SP_e} \times S_i)$ $(i=1,\ldots,n)$ or equivalently iff $\nu_{cob}(G_{S_i P_i} \times S_i) \subseteq \nu_{cob}(G_{SP_e} \times S_i)$ $(i=1,\ldots,n)$.

Proof

The condition on cycles follows from Theorem 1 while the condition on coboundaries is obtained by observing that $\nu_1 \subseteq \nu_2$ iff $\nu_1^* \supseteq \nu_2^*$ and that $\nu_{cy}(G) = (\nu_{cob}(G))^*$. Q.E.D.

Test

From Theorem 2 it follows that the topological port conditions of $N_{S_i P_i}$ $(i=1,\ldots,n)$ are met in the multiport N_{SP_e} iff the rows of the incidence matrix of $G_{S_i P_i} \times S_i (i=1,\ldots,n)$ are orthogonal to the rows of a circuit matrix of $G_{SP_e} \times S_i$ $(i=1,\ldots,n)$.

Example 2

Consider the graphs of Fig. 1. Graphs $G_{S_1 P_1} \times S_1$, $G_{S_2 P_2} \times S_2$,

$G_{SP_e} \times S_1$, $G_{SP_e} \times S_2$ are shown in Fig. 2. The cycle $\begin{matrix}1&2&3&4&5\\[1&0&1&0&0]\end{matrix}$ belongs to $\nu_{cy}(G_{SP_e} \times S_1)$ but not to $\nu_{cy}(G_{S_1P_1} \times S_1)$. So port conditions of $N_{S_1P_1}$ are violated. Equivalently the coboundary $\begin{matrix}1&2&3&4&5\\[1&0&0&1&0]\end{matrix}$ belongs to $\nu_{cob}(G_{S_1P_1} \times S_1)$ but not to $\nu_{cob}(G_{SP_e} \times S_1)$. This again indicates that port conditions of $N_{S_1P_1}$ are violated. It may be verified that port conditions of $N_{S_2P_2}$ are also violated.

We now consider the relevance of the topological conditions to practical circuit interconnection. Consider the equations of N_{SP_e}

$$(\underline{A}_S \quad \underline{A}_{P_e}) \begin{matrix}\underline{i}_S \\ \underline{i}_{P_e}\end{matrix} = 0 \tag{1}$$

$$(\underline{B}_S \quad \underline{B}_{P_e}) \begin{matrix}\underline{v}_S \\ \underline{v}_{P_e}\end{matrix} = 0 \tag{2}$$

$$D_S(\underline{i}_S, \underline{v}_S) = 0 \tag{3}$$

where equations (1) and (2) are the KCL and KVL conditions while (3) is just a symbolic representation for the device characteristic equations. The topological conditions would not be necessary for a practical circuit to satisfy the port conditions of the individual multiports iff the current vector $\underline{i}_{SP_e}$ in a solution of N_{SP_e} satisfies $\underline{i}_{SP_e}/S_i \in (\nu_{cy}(G_{S_iP_i}))\cdot S_i$ $(i=1,\ldots,n)$ even though $(\nu_{cy}(G_{S_iP_i}))\cdot S_i \not\subseteq (\nu_{cy}(G_{SP_e}))\cdot S_i$ $(i=1,\ldots,n)$. This is equivalent to saying that the vector $\underline{i}_S$ of equation (1) satisfies an additional linear constraint. In general if N_{SP_e} has a unique solution the probability of the current vector satisfying an arbitrary linear constraint in addition to the

topological constraints may be taken to be low unless the device characteristic contains that linear constraint. The most common such linear constraint is the open circuit condition. This can be avoided by simply deleting the open circuit edge before testing for port condition satisfaction. The other pathological situation corresponds to short circuit edges. A loop of such edges can cause N_{SP_e} to have a non unique solution in a trivial way. We can avoid this by contracting all short circuit edges, except those whose currents control voltages or currents elsewhere, before conducting the test.

Example 3

Consider again the graphs of Fig. 1. Suppose branch 5 were an open circuit and branch 7 were a short circuit. Then $S_1' = \{1,2,3,4\}$, $S_2' = \{6,8,9,10\}$ and $G_{S_1'P_1} = G_{S_1P_1} \cdot S_1'$ $G_{S_2'P_2} = G_{S_2P_2} \times S_2'$. $G_{S'P_e} = G_{SP_e} \cdot (S_1' \cup S_2) \times (S_1' \cup S_2')$. G_P is as before. The test is now performed with $G_{S_1'P_1}$, $G_{S_2'P_2}$ and $G_{S'P_e}$.

Conclusion

We have given a simple test for checking whether the port conditions of individual multiports are violated when they are connected according to a port connection diagram.

Acknowledgement

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References

[1] Guillemin, E. A., Synthesis of Passive Networks, Wiley, New York, 1957.

[2] Tutte, W. T., "Lectures on Matroids," J. Res. Natl. Bur. Stand., Sect. B., Vol. 69B, pp. 1-47 (1965).

Figure Captions

Fig. 1(a). Graph $G_{S_1P_1}$ of the multiport $N_{S_1P_1}$.

Fig. 1(b). Graph $G_{S_2P_2}$ of the multiport $N_{S_2P_2}$.

Fig. 1(c). The "port connection diagram" G_P.

Fig. 1(d). Graph G_{SP_e} of multiport N_{SP_e}.

Fig. 2(a). $G_{S_1P_1} \times S_1$.

Fig. 2(b). $G_{S_2P_2} \times S_2$.

Fig. 2(c). $G_{SP_e} \times S_1$.

Fig. 2(d). $G_{SP_e} \times S_2$.

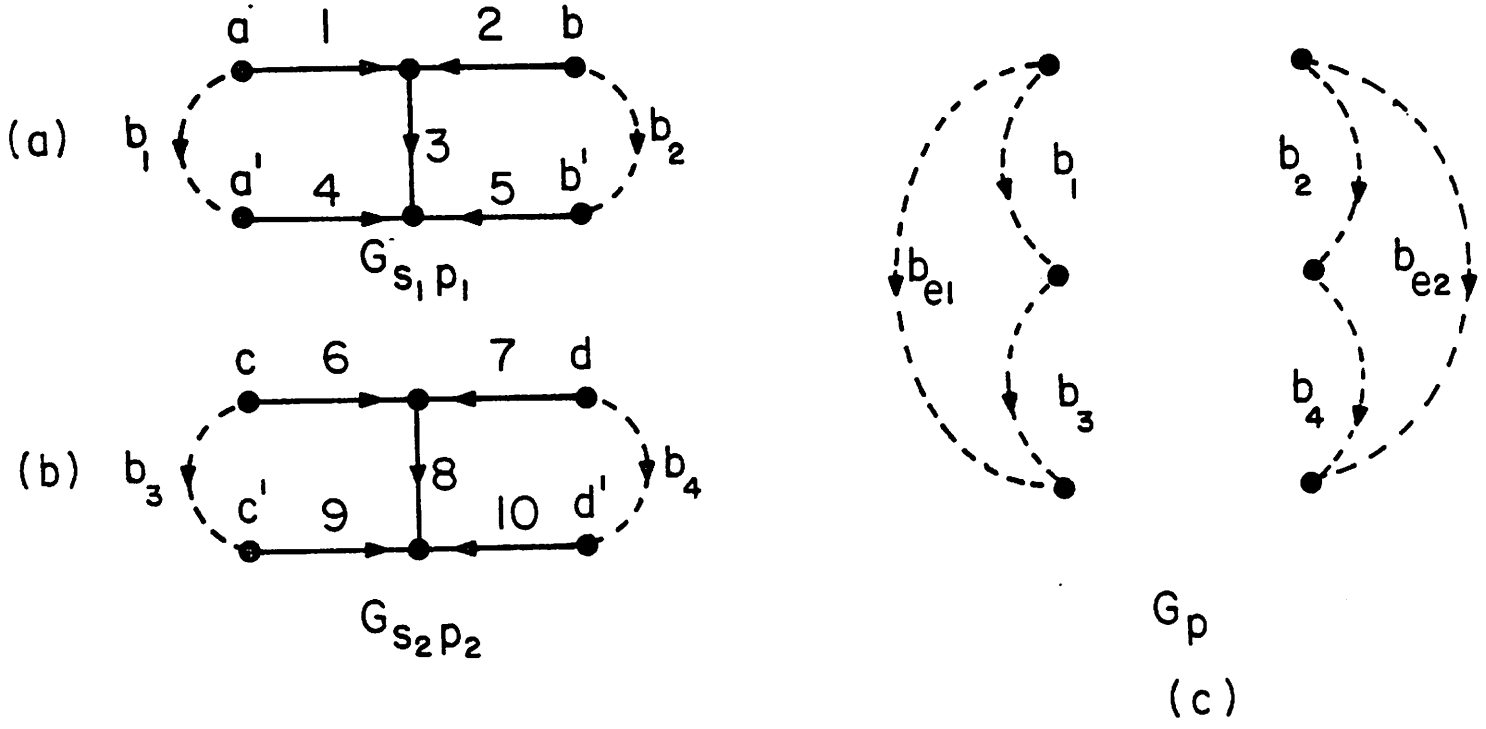
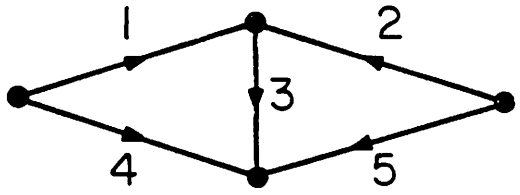
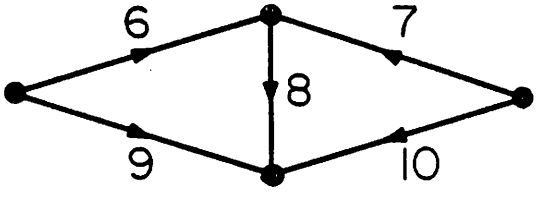

(a)
a
1
2
b
b1
3
b2
a'
4
5
b'
Gs1p1
(b)
c
6
7
d
b3
8
b4
c'
9
10
d'
Gs2p2
be1
b1
b3
b2
be2
b4
Gp
(c)
1
2
3
4
5
be1
be2
6
7
8
9
10
Gspe
(d)

Fig. 1



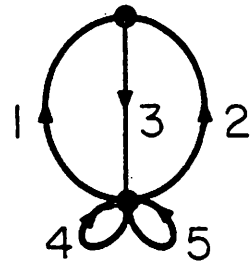
$G_{S_1 P_1} \times S_1$

(a)



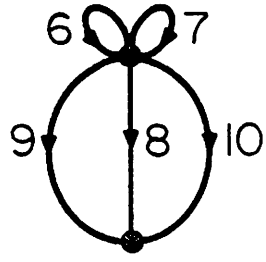
$G_{S_2 P_2} \times S_2$

(b)



$G_{S Pe} \times S_1$

(c)



$G_{S Pe} \times S_2$

(d)

Fig. 2