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((n-1)a) $g_1(\underset{\sim}{v}) + g_2(\underset{\sim}{v}) + \ldots + g_{n-1}(\underset{\sim}{v}) \geq 0$ whenever $v_k \geq 0$

((n-1)b) $g_1(\underset{\sim}{v}) + g_2(\underset{\sim}{v}) + \ldots + g_{n-1}(\underset{\sim}{v}) \leqq 0$ whenever $v_k \leqq 0$

for all $k = 1,2,\ldots,n-1$

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(b) If the input terminal ⓐ and output terminal ⓒ are connected together, and it is assumed that there are no internal connections to either ⓐ or ⓒ ,[17] then the bounding region of Fig. 8(b) shrinks to that shown in Fig. 8(c).

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[17] This somewhat specialized condition will turn out to be relevant to the proof of Property 17. The connection shown is one that would seldom be encountered, in a network used for obtaining TC plots.

QUALITATIVE PROPERTIES OF RESISTIVE NETWORKS CONTAINING MULTI-TERMINAL NONLINEAR ELEMENTS

by

L. O. Chua, Y-F Lam and L. A. Stromsmoe

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

QUALITATIVE PROPERTIES OF RESISTIVE NETWORKS CONTAINING MULTI-TERMINAL NONLINEAR ELEMENTS[†]

L.O. Chua, Y-F Lam, and K.A. Stromsmoe[††]

ABSTRACT

This paper is concerned with the qualitative properties of nonlinear multi-terminal resistors and nonlinear resistive networks--properties which give results that require neither computation nor equation formulation. The basic circuit theoretic concepts of passivity, local passivity, monotonicity, activity and local activity are defined and properties are developed that relate these fundamental concepts. The notion of "no-power gain" and that of "no-voltage gain" or "no current gain" are shown to be in general distinct from one another. The concept of no-gain elements is generalized to include multi-terminal elements. The main result obtained is that an n-terminal element possesses the no-gain property if, and only if, at each operating point, a connected network of n-1 positive linear two-terminal resistors exists which has the same operating point. This generalization serves as a basic tool for the derivation of bounds on the two most useful characterizations for nonlinear resistive networks; namely, the driving point (DP) and the transfer characteristic (TC) plots. The sharpest possible bounding regions are obtained for a large class of nonlinear networks--including networks which use operational amplifiers as one of the main elements.

The concepts of symmetric and complementary symmetric networks are introduced and used to show that various classes of networks have either odd or even symmetric DP and TC plots. Again when operational amplifiers are used as a basic circuit element, it is shown that many operational amplifier circuits exhibit odd symmetric DP and TC plots.

Finally, the concepts of locally no-gain n-ports and locally no-gain networks are introduced and it is shown that these concepts are related to the classical n-port resistor synthesis problem.

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[††]L.O. Chua and Y-F Lam are with the Department of EECS University of California, Berkeley, California and K.A. Stromsmoe is with the Department of Electrical Engineering, University of Alberta, Edmonton, Alberta, Canada.

I. INTRODUCTION

Much research has been directed to the study of resistive nonlinear networks over the last decade. Most of these research activities can be grouped under the category of "existence and uniqueness results" [1], or under the category of "computational techniques" [2]. Very little research has been devoted to deriving results of a more qualitative nature -- i.e. results which do not involve any computation or equation formulation--until the recent work by Willson on the no-gain property for networks containing three-terminal elements [3]. Our objective in this paper is to derive qualitative properties for the two most useful and commonly specified characterizations of resistive nonlinear networks; namely, the associated driving-point and transfer characteristic plots[1] -- henceforth abbreviated simply as DP and TC plots [4]. In particular, we will show in Section IV that the DP and TC plots of various classes of resistive nonlinear networks must necessarily lie within some bounding regions. These bounding regions are the best possible that can be found and they can be determined by inspection of the network topology and the element constitutive relations.

Another important qualitative property that will be derived in this paper is the conditions which guarantee that the DP plot or TC plot of various classes of networks will exhibit some form of symmetry. For example, it is generally known--though never explicitly pointed out--that the DP plot and TC plot of any circuit made up exclusively of operational amplifiers and bilateral two-terminal resistors (characterized by odd-symmetric v-i curves) are always odd symmetric regardless of the network topology [5]. It turns out that this is due to the fact that an operational amplifier satisfies a more subtle form of symmetry called "complementary symmetry" to be presented in Section V. This new concept does not require the network to display any topological symmetry and is therefore applicable to a very large class of practical networks.

For complete generality, we will allow our networks to contain not only two-terminal or three-terminal elements, but also multi-terminal elements such as operational amplifiers and analog multipliers [6], having more than three terminals. Since the key to our derivation of the bounding regions in Section IV is precisely the "no-gain property" of many solid state

[1] We use the term "plot" and not "function" as normally found in linear network literatures because the driving-point and transfer characteristics for nonlinear networks could be multivalued and are therefore not functions.

devices, it is essential to generalize Willson's results in [3] to allow n-terminal elements. This turns out to be a non-trivial task because the formulation and methods of proof given in [3] are not suited for generalization to the multi-terminal cases. Hence, a completely different approach has been developed and is presented in Section III. Even though the results in this section are used only as a tool for deriving the bounding regions in Section IV, they are of a rather basic nature and will no doubt find other applications in future works.

Willson has shown that passivity is only a necessary condition for 3-terminal no-gain elements. This observation is also true for n-terminal elements when $n \geq 3$. It is not surprising that this is the case since the concept of passivity is more germane to a study of power gain, and not voltage gain, or current gain. Indeed, it follows from Tellegen's theorem that to obtain power gain in a network N, it is necessary that at least one element of N be active. Hence passivity is synonymous to "no-power gain"; i.e., the power gain is not greater than unity. It has very little to do with voltage gain or current gain as aptly demonstrated by the ideal transformer which is passive but is capable of either a voltage gain, or a current gain greater than unity. Since all realistic models of real multi-terminal devices must be passive, the more important notion is really that of local activity in so far as obtaining greater-than-unity local power gain is concerned. From a circuit-theoretic point of view, it is important that concepts which are relevant to power gain be clearly separated from those which are relevant to voltage gain or current gain. Hence it is appropriate that we first present a study of power-gain related concepts in Section II. In particular, we will present a careful study of the relationships between passivity and local passivity; as well as between monotonicity and local passivity for multi-terminal elements. The results in this section are relevant for a firm understanding of the results in section III.

Finally, since this paper is addressed exclusively to networks containing only dc independent voltage and current sources as well as multi-terminal resistors [4] defined by

$$f_i(v_1, v_2, \ldots v_n, i_1, i_2, \ldots i_n) = 0, \qquad i = 1,2,\ldots n$$

we will use the word "elements" and "resistors" interchangeably.

II CONCEPTS AND PROPERTIES RELATED TO POWER GAIN

Our objective in this section is to study the relationship between a number

of circuit-theoretic concepts which are relevant to the study of power gain of multi-port nonlinear resistive networks.

Definition 1 Passive and Locally Passive Resistors

An n-port resistor $\mathcal{R}$ is said to be passive if, and only if, the scalar product

$$\langle \underset{\sim}{v}, \underset{\sim}{i} \rangle \triangleq \sum_{j=1}^{n} v_j i_j \geq 0 \tag{1}$$

for all admissible signal pairs $(\underset{\sim}{v}, \underset{\sim}{i})$. It is said to be locally passive if, and only if

$$\langle \delta\underset{\sim}{v}, \delta\underset{\sim}{i} \rangle \geq 0 \tag{2}$$

for all admissible incremental signal pairs $(\delta\underset{\sim}{v}, \delta\underset{\sim}{i})$ about each operating point Q of $\mathcal{R}$. It is said to be strictly passive if the strict inequality sign holds in (1) whenever $\underset{\sim}{v} \neq 0$ and $\underset{\sim}{i} \neq 0$, and strictly locally passive if the strict inequality sign holds in (2) whenever $\delta\underset{\sim}{v} \neq 0$ and $\delta\underset{\sim}{i} \neq 0$. The element $\mathcal{R}$ is said to be active if it is not passive and locally active if it is not locally passive.

Definition 2 Monotone-Increasing Resistors

An n-port resistor $\mathcal{R}$ is said to be monotone increasing if, and only if,

$$\langle \underset{\sim}{v}' - \underset{\sim}{v}'', i' - i'' \rangle \geq 0 \tag{3}$$

for any two admissible signal pairs (v',i') and (v",i"). It is said to be strictly monotone increasing if the strict inequality holds in (3) for any two distinct admissible signal pairs.

For simplicity, we will assume throughout this section that our n-port resistor $\mathcal{R}$ is characterized by a C^1-hybrid representation[2]

$$\begin{aligned} \underset{\sim}{i}_a &= \underset{\sim}{h}_a (\underset{\sim}{v}_a, \underset{\sim}{i}_b) \\ \underset{\sim}{v}_b &= \underset{\sim}{h}_b (\underset{\sim}{v}_a, \underset{\sim}{i}_b) \end{aligned} \tag{4}$$

where $\underset{\sim}{v} \triangleq [\underset{\sim}{v}_a^t \; \underset{\sim}{v}_b^t]^t$ and $\underset{\sim}{i} = [\underset{\sim}{i}_a^t \; \underset{\sim}{i}_b^t]$.

[2]For a more general parametrizable case, see [7].

A simple characterization of monotone-increasing resistors was given in [8] and is reproduced here since it will be needed in the proof of Property 2.

Property 1 Monotone Increasing Criteria

An n-port resistor $\mathcal{R}$ is monotone-increasing if, and only if, its incremental hybrid matrix

$$\underset{\sim}{H}(\underset{\sim}{v}_a,\underset{\sim}{i}_b) \triangleq \begin{bmatrix} \frac{\partial \underset{\sim}{h}_a}{\partial \underset{\sim}{v}_a} & \frac{\partial \underset{\sim}{h}_a}{\partial \underset{\sim}{i}_b} \\ \frac{\partial \underset{\sim}{h}_b}{\partial \underset{\sim}{v}_a} & \frac{\partial \underset{\sim}{h}_b}{\partial \underset{\sim}{i}_b} \end{bmatrix} = \begin{bmatrix} \underset{\sim}{H}_{aa} & \underset{\sim}{H}_{ab} \\ \underset{\sim}{H}_{ba} & \underset{\sim}{H}_{bb} \end{bmatrix} \tag{5}$$

is positive semi-definite[3] for all $(\underset{\sim}{v}_a,\underset{\sim}{i}_b)$. Moreover, if $\underset{\sim}{H}(\underset{\sim}{v}_a,\underset{\sim}{i}_b)$ is positive definite[3] then $\mathcal{R}$ is strictly monotone-increasing.

The next property shows that the circuit theoretic concept of local passivity and the mathematical concept of monotonicity are equivalent to each other.

Property 2. Equivalent Local Passivity Criteria

An n-port resistor $\mathcal{R}$ is locally passive {resp., strictly locally passive} if, and only if, it is monotone increasing {resp., strictly monotone increasing}.

Proof.

$$\begin{aligned} \langle \delta\underset{\sim}{v}, \delta\underset{\sim}{i} \rangle &= \langle \delta\underset{\sim}{v}_a, \delta\underset{\sim}{i}_a \rangle + \langle \delta\underset{\sim}{v}_b, \delta\underset{\sim}{i}_b \rangle \\ &= \langle \delta\underset{\sim}{v}_a, \underset{\sim}{H}_{aa}\delta\underset{\sim}{v}_a + \underset{\sim}{H}_{ab}\delta\underset{\sim}{i}_b \rangle + \langle \underset{\sim}{H}_{ba}\delta\underset{\sim}{v}_a + \underset{\sim}{H}_{bb}\delta\underset{\sim}{i}_b, \delta\underset{\sim}{i}_b \rangle \\ &= [\delta\underset{\sim}{v}_a^t \delta\underset{\sim}{i}_b^t]\ \underset{\sim}{H}(\underset{\sim}{v}_a,\underset{\sim}{i}_b)\ [\delta\underset{\sim}{v}_a^t\ \delta\underset{\sim}{i}_b^t]^t \geq 0 \end{aligned}$$

Hence $\langle \delta\underset{\sim}{v}, \delta\underset{\sim}{i} \rangle$ is non-negative {resp., positive} if, and only if, $\underset{\sim}{H}(\underset{\sim}{v}_a,\underset{\sim}{i}_b)$ is positive semi-definite {resp., positive definite} and the conclusion follows from Property 1. ¤

Property 3 Necessary Condition for Passivity

An n-terminal resistor $\mathcal{R}$ characterized by a continuous hybrid representation

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[3] A not necessarily symmetric n×n matrix $\underset{\sim}{M}$ is said to be positive semi-definite if, and only if, $\underset{\sim}{x}^t\ \underset{\sim}{M}\ \underset{\sim}{x} \geq 0$ for any $\underset{\sim}{x} \in \mathbb{R}^n$. It is said to be positive definite if, and only if, $\underset{\sim}{x}^t\ \underset{\sim}{M}\ \underset{\sim}{x} > 0$ for any $\underset{\sim}{x} \neq \underset{\sim}{0}$. It is easy to prove that $\underset{\sim}{M}$ is positive semi-definite or positive definite if, and only if, its symmetrical part $\underset{\sim}{M} + \underset{\sim}{M}^t$ is positive semi-definite or positive definite, respectively.

of (4) is passive only if its constitutive relation passes through the origin.

Proof. Suppose $(\underset{\sim}{I}_a,\underset{\sim}{E}_b) = (\underset{\sim}{h}_a(\underset{\sim}{0},\underset{\sim}{0}),\underset{\sim}{h}_b(\underset{\sim}{0},\underset{\sim}{0})) \neq (\underset{\sim}{0},\underset{\sim}{0})$. Then at least one component of $(\underset{\sim}{I}_a,\underset{\sim}{E}_b)$ is nonzero. Without loss of generality, let $I_1 \neq 0$.

Assume first $I_1 > 0$. Since $\underset{\sim}{h}_a(\underset{\sim}{0},\underset{\sim}{0})$ is continuous, there exists an open ball B_ε defined by

$$B_\varepsilon \triangleq \{(\underset{\sim}{v}_a,\underset{\sim}{i}_b) \in \mathbb{R}^n: \|\underset{\sim}{v}_a\|^2 + \|\underset{\sim}{i}_b\|^2 < 2\varepsilon > 0\} \tag{6}$$

such that $i_1 = h_1(\underset{\sim}{v}_a,\underset{\sim}{i}_b) > 0$ for all $(\underset{\sim}{v}_a,\underset{\sim}{i}_b)$ in B_ε. Consider a point $(\underset{\sim}{v}'_a,\underset{\sim}{i}'_b) = (-\varepsilon,0,0,\ldots,0)$ in B_ε. Let $\underset{\sim}{i}'_a = \underset{\sim}{h}_a(\underset{\sim}{v}'_a,\underset{\sim}{i}'_b)$ and $\underset{\sim}{v}'_b = \underset{\sim}{h}_b(\underset{\sim}{v}'_a,\underset{\sim}{i}'_b)$. Then

$$\langle \underset{\sim}{v}',\underset{\sim}{i}' \rangle = -\varepsilon h_1(\underset{\sim}{v}'_a,\underset{\sim}{i}'_b) < 0 \tag{7}$$

Similarly if $I_1 < 0$, then there exists an open ball $B_{\hat{\varepsilon}}$ as defined in (6) with ε replaced by $\hat{\varepsilon}$, such that $i_1 = h_1(\underset{\sim}{v}_a,\underset{\sim}{i}_b) < 0$ for all $(\underset{\sim}{v}_a,\underset{\sim}{i}_b)$ in $B_{\hat{\varepsilon}}$. In particular, let us consider the point $(\underset{\sim}{v}''_a,\underset{\sim}{i}''_b) = (\hat{\varepsilon},0,0,\ldots,0)$ in $B_{\hat{\varepsilon}}$. Let $\underset{\sim}{i}''_a = \underset{\sim}{h}_a(\underset{\sim}{v}''_a,\underset{\sim}{i}''_b)$ and $\underset{\sim}{v}''_b = \underset{\sim}{h}_b(\underset{\sim}{v}''_a,\underset{\sim}{i}''_b)$. Then

$$\langle \underset{\sim}{v}'',\underset{\sim}{i}'' \rangle = \hat{\varepsilon}\, h_1(\underset{\sim}{v}_a,\underset{\sim}{i}_b) < 0 \tag{8}$$

Together (7) and (8) imply that if $I_1 \neq 0$, then $\mathcal{R}$ is not passive. Since $\mathcal{R}$ is passive by hypothesis, $I_1 = 0$. By repeating the above procedure for all components of $(\underset{\sim}{I}_a,\underset{\sim}{E}_b)$, we conclude that $(\underset{\sim}{I}_a,\underset{\sim}{E}_b) = (\underset{\sim}{0},\underset{\sim}{0})$. ∎

A locally passive n-terminal resistor need not be passive, and vice-versa. The precise relationship between the two is given by the next property.

Corollary 3.1 Passivity and Local Passivity Relationship

A locally passive n-terminal resistor $\mathcal{R}$ characterized by a C^1-hybrid representation of (4) is passive if, and only if, its constitutive relation passes through its origin.

Proof. A. Sufficiency: It follows from Property 2 that $\mathcal{R}$ is locally passive if, and only if, $\langle \underset{\sim}{v}'-\underset{\sim}{v}'',\underset{\sim}{i}'-\underset{\sim}{i}'' \rangle \geq 0$ for any two admissible pairs $(\underset{\sim}{v}',\underset{\sim}{i}')$ and $(\underset{\sim}{v}'',\underset{\sim}{i}'')$. Now choose $(\underset{\sim}{v}''_a,\underset{\sim}{i}''_b) = (\underset{\sim}{0},\underset{\sim}{0})$. Thus by hypothesis, this implies that $(\underset{\sim}{i}''_a,\underset{\sim}{v}''_b) = (\underset{\sim}{0},\underset{\sim}{0})$ and we have $\langle \underset{\sim}{v}'-\underset{\sim}{v}'',\underset{\sim}{i}'-\underset{\sim}{i}'' \rangle = \langle \underset{\sim}{v}',\underset{\sim}{i}' \rangle \geq 0$ for any admissible pair $(\underset{\sim}{v}',\underset{\sim}{i}')$. Hence $\mathcal{R}$ is passive.

B. Necessity: This follows directly from Property 3. ¤

Corollary 3.2 Strict Passivity and Strict-Local Passivity Relationship

A strictly locally passive n-terminal resistor $\mathcal{R}$ characterized by a C^1-hybrid representation of (4) is strictly passive if, and only if, its constitutive relationship passes through the origin.

In the study of active networks, it is usually desirable to have some simple criteria for ascertaining whether an n-terminal resistor is active, or locally active. The following properties provide convenient sufficient conditions for this purpose.

Property 4 Activity Criteria

Let $\mathcal{R}$ be an n-terminal resistor having a terminal voltage v_k {resp.; terminal current i_k} which does not depend upon its associated terminal current i_k {resp.; terminal voltage v_k}, and is not identically zero; i.e.,

$$v_k = f_k(x_1,x_2,\ldots,x_{k-1},x_{k+1},\ldots,x_n) \triangleq f_k(\underset{\sim}{x}) \tag{9}$$

$$\{\text{resp.; } i_k = g_k(x_1,x_2,\ldots,x_{k-1},x_{k+1},\ldots,x_n) \triangleq g_k(\underset{\sim}{x})\} \tag{10}$$

where x_j denotes either v_j or i_j for each $j \neq k = 1,2,\ldots,n$, and $\underset{\sim}{x} = [x_1,x_2,\ldots,x_{k-1},x_k,x_{k+1},\ldots,x_n]^t$ with $x_k = i_k$ {resp.; $x_k = v_k$}. Let y_j be the complementary variable, i.e., $y_j = v_j$ if $x_j = i_j$ and $y_j = i_j$ if $x_j = v_j$. If y_j does not depend upon i_k {resp.; v_k} for all $j \neq k$, then $\mathcal{R}$ is active.

Proof. We will prove the case corresponding to $f_k(\underset{\sim}{x})$ of (9) only.

Since $f_k(\underset{\sim}{x})$ is not identically zero by hypothesis, there exist $\bar{\underset{\sim}{x}}$ such that $f_k(\bar{\underset{\sim}{x}}) \neq 0$. Choose

$$\begin{aligned} i_k = \bar{i}_k > 0 \text{ if } f_k(\bar{\underset{\sim}{x}}) \triangleq \bar{v}_k < 0 \\ = \bar{i}_k < 0 \text{ if } f_k(\bar{\underset{\sim}{x}}) \triangleq \bar{v}_k > 0 \end{aligned} \tag{11}$$

Then

$$\langle \underset{\sim}{v},\underset{\sim}{i} \rangle = \sum_{\substack{j=1 \\ j\neq k}}^{n} \bar{v}_j\bar{i}_j + \bar{v}_k\bar{i}_k \tag{12}$$

Since $\bar{x}_j$ is an independent variable and $\bar{y}_j$ does not depend on $\bar{i}_k$ by hypothesis, and

since $\bar{v}_k \bar{i}_k < 0$, we can always choose $\bar{i}_k$ sufficiently large such that $\langle \underset{\sim}{v}, \underset{\sim}{i} \rangle < 0$. Hence $\mathcal{R}$ is active. ∎

Property 5. Local Activity Criteria

An n-terminal resistor $\mathcal{R}$ is locally active if there exists an operating-point Q having an incremental voltage δv_k {resp.; an incremental current δi_k} about Q, which does not depend upon its associated incremental current δi_k {resp.; incremental voltage δv_k}, and is not identically zero; i.e.,

$$\delta v_k = f_k(\delta x_1, \delta x_2, \cdots, \delta x_{k-1}, \delta x_{k+1}, \cdots, \delta x_n) \triangleq f_k(\delta \underset{\sim}{x}) \tag{13}$$

$$\{\text{resp.; } \delta i_k = g_k(\delta x_1, \delta x_2, \cdots, \delta x_{k-1}, \delta x_{k+1}, \cdots, \delta x_n) \triangleq g_k(\delta \underset{\sim}{x})\} \tag{14}$$

where δx_j denotes either δv_j or δi_j $\delta \underset{\sim}{x} = [\delta x_1, \delta x_2, \cdots, \delta x_{k-1}, \delta x_k, \delta x_{k+1}, \cdots, \delta x_n]^t$ with $\delta x_k = \delta i_k$ {resp.; $\delta x_k = \delta v_k$}, and if the complementary variable δy_j of δx_j does not depend upon δi_k {resp.; δv_k} for all $j \neq k = 1,2,\cdots,n$, then $\mathcal{R}$ is locally active.

Proof. The proof of Property 5 is similar to that of Property 4 and is therefore omitted. ∎

Observe that in order for these properties to hold, both $f_k(\cdot)$ {resp.; $g_k(\cdot)$} and the remaining dependent variables y_j must not depend upon i_k or δi_k {resp., v_k or δv_k}. For example, an ideal grounded two-port transformer characterized by $v_2 = nv_1$ and $i_1 = -ni_2$ satisfies the first condition (v_2 is independent of i_2) but not the second condition (i_1 depends on i_2). Indeed, this element is non-energic and is therfore passive. It follows immediately from Property 4 that the ideal linear operational amplifier (characterized by $i_1 = 0$, $i_2 = 0$, and $v_3 = A(v_2 - v_1)$) and the ideal analog multiplier (characterized by $i_1 = 0$, $i_2 = 0$, and $v_3 = kv_1v_2$) are both active 4-terminal elements. Similarly, all controlled sources are active. It also follows from Property 5 that any 3-terminal element having an incremental circuit model characterized by a transfer conductance function $i_2 = f(v_1)$ and $i_1 = 0$, or by a transfer resistance function $v_2 = f(i_1)$ and $v_1 = 0$, must be locally active. It is interesting to observe that this property is shared by the ideal incremental circuit models of most 3-terminal devices--including vacuum tubes, transistors, and FET's--capable of local power gain.

III CONCEPTS AND PROPERTIES RELATED TO VOLTAGE AND CURRENT GAIN

In this section we consider various aspects of no-gain circuits [3,9,10]. Necessary and sufficient conditions are given to establish the relationship between a multi-terminal resistor and a no-gain element. The implications of these conditions on the representation of a multi-terminal resistor are examined. In particular, the constraints imposed upon "locally no-gain elements" are derived. These constraints turn out to be extremely strong, thereby implying the rather surprising observation that most multi-terminal elements ($n \geq 3$) should be capable of incremental voltage or current gain.

Finally to investigate the no-gain property of circuits containing elements such as ideal diodes whose constitutive relations fall right on the passivity boundary, we introduce the concept of "weakly no-gain elements" and derive their properties.

A. No-Gain Elements

Definition 3 $\mathcal{S}$-loop and $\mathcal{O}$-cutset

An $\mathcal{S}$-loop {resp.; $\mathcal{O}$-cutset} is a loop {resp.; cutset} consisting of short {resp.; open} circuit elements only. An aligned loop {resp.; cutset} is a loop {resp.; cutset} for which the reference directions of all elements composing it have the same orientation.

To provide an important tool for the derivation of the main theorem in this section, "criteria for no-gain n-terminal resistors[4]", we need to generalize the results of Wolaver in [10] to include both short circuit and open circuit elements. This generalization requires the use of the following two special cases of Minty's color arc Theorem [11]:

Lemma 1

(a) Let $\mathcal{B}$ be the set of all branches in a network containing only two-terminal elements, and let b be an element of $\mathcal{B}$. Let $\mathcal{L}$ and $\mathcal{C}$ be any two subsets of $\mathcal{B}$ such that $\mathcal{B} = b \cup \mathcal{L} \cup \mathcal{C}$ and $\mathcal{L} \cap \mathcal{C}$ is an empty set. Then b forms a loop exclusively with elements in $\mathcal{L}$ or a cutset exclusively with elements in $\mathcal{C}$, but not both.

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[4] For brevity, a multi-terminal element is simply called an n-terminal element, where "n" is used in the generic sense, and $n \geq 2$.

(b) In a network with the associated reference directions[5] assigned to the elements each branch lies in either an aligned loop or an aligned cutset, but not both.

Property 6 No Gain Property for Networks Containing Two-Terminal Elements

Given a network containing independent voltage and current sources, positive linear two-terminal resistors,[6] short circuit elements which do not form $\mathcal{S}$-loops and open circuit elements which do not form $\mathcal{O}$-cutsets,[7] then

1) the current magnitude through any element[8] is not greater than the sum of the current magnitudes through all independent voltage and current sources.

2) the voltage magnitude across any element[8] is not greater than the sum of the voltage magnitudes across all independent voltage and current sources.

Proof. We will prove the current magnitude case only. The voltage magnitude case can be proven in a dual manner.

The current magnitude through any independent source or open circuit element satisfies the conclusion trivially. Hence, we only have to consider the current magnitude through any short circuit element or any positive linear resistor.

To consider the current magnitude through any positive resistor R, we can coalesce any two nodes connected by a short circuit element, and delete all open circuit elements. The resulting circuit contains only independent sources and positive linear two-terminal resistors. Hence, the result of Wolaver's Theorem [10] applies--the current magnitude through any positive linear resistor is not greater than the sum of the current magnitudes through the sources.

It remains to consider the current magnitude through a short circuit element s. Without loss of generality, let us delete all open circuit elements. Since the network contains no $\mathcal{S}$-loops, it follows from the color arc Lemma 1(a) that

[5]The reference current of each branch enters the positive terminal of the referenced voltage of the same branch.

[6]A two-terminal positive linear resistor has a resistance R restricted by $0 < R < \infty$.

[7]Clearly, if there is an $\mathcal{S}$-loop in a circuit N, then a circulating current of arbitrary magnitude can be sustained by the short circuit elements forming this $\mathcal{S}$-loop. In a dual manner, if there is an $\mathcal{O}$-cutset, then the voltages across the open circuit elements forming this $\mathcal{O}$-cutset can be raised by an arbitrary level, without affecting the branch voltages of other circuit elements inside N. Hence, any network containing an $\mathcal{S}$-loop or $\mathcal{O}$-cutset can not exhibit the no-gain property.

[8]This includes open and short circuit elements.

the short circuit element s must form a cutset exclusively with positive linear resistors and independent sources. (Choose b=s, $\mathcal{L}$=set of all short circuit elements, and $\mathcal{C}$=remaining elements.) Hence, as far as the current through s is concerned, there is no loss of information to coalesce any two nodes connected by a short circuit with the exception of s. The resulting circuit contains positive linear resistors, independent sources and the short circuit element s. We now use this simplified circuit to investigate the current i_s through the short circuit element s.

If s forms a cutset exclusively with independent sources, then i_s is given by an alegbraic sum of currents through the independent sources in the cutset. In this case, the conclusion follows trivially.

Suppose the short circuit element s does not form a cutset exclusively with independent sources. In this case, we let the associated reference directions of all positive linear resistors and independent sources be chosen such that all voltages across them are positive. It is clear that no matter which reference direction is assigned to s, there can be no aligned loop that contains s. (Otherwise there will be a loop containing positive-voltage branches and a zero-voltage branch thereby violating KVL.) It follows from Lemma 1(b) that there is a cutset $\mathcal{C}_s$ containing s such that the reference directions of all elements in $\mathcal{C}_s$, except s, have the same orientation. The associated reference direction of s can be selected to coincide with those associated with the other elements in $\mathcal{C}_s$. Hence, $\mathcal{C}_s$ is then an aligned cut set. Let A be the set of all positive linear resistors in $\mathcal{C}_s$ and let B be the set of all independent sources in $\mathcal{C}_s$. It then follows from KCL that,

$$i_s + \sum_{k\in A} i_k + \sum_{j\in B} i_j = 0 \tag{15}$$

Since all positive linear resistors have positive voltages, $i_k \geq 0$ for all $k \in A$. Hence, (15) implies that

$$|i_s| \leq - \sum_{j\in B} i_j \leq \sum_{j\in B} |i_j| \tag{16}$$

The term on the right of (16) is no greater than the sum of the current magnitudes of all independent sources, the conclusion of Property 6 follows.

This completes the proof of Property 6. ∎

Definition 4 No-Gain Networks

A resistive network is said to possess the no-gain property if each solution at any time is such that, (a) the magnitude of the voltage between any pair of nodes in the network is less than or equal to the sum of the magnitudes of the voltages appearing across the independent voltage and current sources, and (b) the magnitude of the current flowing into each terminal of every element is less than or equal to the sum of the magnitudes of the currents flowing through the independent voltage and current sources.

Definition 5 No-Gain Resistor

An n-terminal ($n \geq 2$) resistor $\mathcal{R}$ is said to be a no-gain resistor if each connected network containing $\mathcal{R}$, positive linear two-terminal resistors, short and open circuit elements which do not form $\mathcal{S}$-loops and $\mathcal{O}$-cutsets respectively, and nonzero independent voltage and current sources, possesses the no-gain property.[9]

Reference Directions

Unless specified otherwise, an n-terminal element has the reference directions shown in Fig. 1, where all voltages are assumed to be node-to-datum voltages and all terminal currents are assumed to enter the n-terminal element.

Theorem 1 The No-Gain Resistor Criteria

An n-terminal resistor $\mathcal{R}$ is a no-gain resistor if, and only if, at each dc operating point Q of $\mathcal{R}$, there exists a connected n-terminal network N_Q containing n-1 linear positive two-terminal resistors which has the same operating point.

Proof

A. Sufficiency: Let $\mathcal{R}$ be imbedded in any connected network N containing only positive linear two-terminal resistors, short and open circuit elements which do not form $\mathcal{S}$-loops and $\mathcal{O}$-cutsets respectively, and nonzero independent voltage and current sources. Let $\hat{Q}$ be an operating point of the network and let Q be the

[9] Observe that the definition of a no-gain n-terminal resistor here differs from that given in [3]. One could argue that Willson had actually used the present definition in his proof of Theorem 2, when he connected terminals 2 and 3 together in Fig. 13(a) in [3] for the case where $v_2 = 0$. This is because a short circuit element must be physically connected across terminals 2 and 3 in order to maintain the desired potential difference for v_2. Moreover, the identity of v_2 would be lost if nodes 2 and 3 were coalesed into one node.

corresponding operating point of $\mathcal{R}$. By hypothesis, there exists an n-terminal network N_Q containing n-1 two-terminal positive linear resistors, which, when imbedded in N will result in the same operating point $\hat{Q}$. Since the resulting network (i.e. with N_Q replacing $\mathcal{R}$) satisfies all conditions of Property 6, it follows that the voltage between any two nodes and the current through any two-terminal element possesses the no-gain property. Hence, we only need to prove that the current through any terminal of N_Q also possesses the no-gain property. Without loss of generality, let us choose any terminal ⓐ of N_Q and suppose that there are $M \leq n-1$ positive linear two-terminal resistors <u>inside</u> N_Q connected to node ⓐ. Partition these resistors into three sets S_1, S_2, and S_3, where $S_1 \triangleq \{R_1, R_2, \ldots, R_J\}$ denotes the set of resistors having actual current flowing away from node ⓐ, or $i_{R_k} < 0$ for $k = 1, 2, \ldots, J$; $S_2 \triangleq \{R_{J+1}, R_{J+2}, \ldots, R_L\}$ denotes the set of resistors having actual current flowing into node ⓐ, or $i_{R_k} > 0$ for $k = J+1, J+2, \ldots, L$; and $S_3 \triangleq \{R_{L+1}, R_{L+2}, \ldots, R_M\}$ denotes the set of resistors having zero current. The partitioning scheme is shown in Fig. 2. The terminal current i_α is given by,

$$-i_\alpha = (i_{R_1} + i_{R_2} + \cdots + i_{R_J}) + (i_{R_{J+1}} + i_{R_{J+2}} + \cdots + i_{R_L}) \tag{17}$$

where $i_{R_k} < 0$ for $k = 1, 2, \ldots, J$ and $i_{R_k} > 0$ for $k = J+1, J+2, \ldots, L$.

Using the method indicated by Willson [3], we can take any two resistors in S_1 {resp.; S_2}, say R_a and R_b, and replace them by an equivalent subnetwork containing three <u>positive</u> linear resistors, as shown in Fig. 3, without effecting the operating point. Observe that the current flowing through the third linear resistor R_c is given by $i_{R_c} = i_{R_a} + i_{R_b}$. Clearly i_{R_c} possesses the no-gain property since the resulting network satisfies the conditions of Property 6. This procedure can obviously be repeated until all currents flowing through all resistors in S_1 {resp.; S_2} is equal to a single current actually flowing <u>away from</u> {resp.; <u>toward</u>} node ⓐ through a single two-terminal positive linear resistor, as shown in Fig. 4, where

$$i_A = \sum_{k=1}^{J} i_{R_k} < 0 \text{ and } i_B = \sum_{k=J+1}^{L} i_{R_k} > 0 \tag{18}$$

If we replace the subnetwork of Fig. 2 by the equivalent subnetwork of Fig. 4 in

the overall imbedded network N, the resulting network still satisfies all hypotheses of Property 6. Hence i_A and i_B possess the no-gain property. Since i_A and i_B have opposite signs,

$$|i_\alpha| = |i_A + i_B| \leq \max \{|i_A|, |i_B|\} \tag{19}$$

Hence i_α also possesses the no-gain property.

B. Necessity: Consider any imbedding network N as in the sufficiency proof, and let Q be an operating point of the no-gain resistor $\mathcal{R}$ in the network. Without loss of generality, let us choose the terminal of $\mathcal{R}$ having the lowest potential as the datum node, and relabel the remaining n-1 nodes of $\mathcal{R}$ so that the operating point voltages of $\mathcal{R}$ satisfy the inequality[10]

$$V_{(1)} \geq V_{(2)} \geq \cdots \geq V_{(k)} \geq \cdots \geq V_{(n-1)} \geq 0 \tag{20}$$

Let $I_{(1)}, I_{(2)}, \ldots, I_{(n-1)}$ be the corresponding operating point currents with the usual reference direction--current entering the no-gain n-terminal resistor $\mathcal{R}$. Using this notation, let us now pause to consider two lemmas, whose proofs are given in the Appendix:

Lemma 2

(a) If

$$V_{(1)} > V_{(2)} > \cdots > V_{(k)} > \cdots > V_{(n-1)} > V_{(n)} \tag{21}$$

then the operating point currents of the no-gain resistor $\mathcal{R}$ must satisfy the following system of strict inequalities

$$I_{(1)} > 0 \tag{22a}$$

$$I_{(1)} + I_{(2)} > 0 \tag{22b}$$

$$\vdots$$

$$I_{(1)} + I_{(2)} + \cdots + I_{(k)} > 0 \tag{22c}$$

[10] Note that $V_{(1)}$ {resp.; $V_{(2)}, V_{(3)} \ldots$ } is the voltage between the highest {resp.; second highest, third highest, ...} and the lowest operating-point potential nodes of the no-gain n-terminal resistor $\mathcal{R}$. Observe that the datum node may be different for different operating points.

$$\vdots$$

$$I_{(1)} + I_{(2)} + \cdots + I_{(k)} + \cdots + I_{(n-1)} > 0 \tag{22d}$$

(b) If

$$V_{(1)} > V_{(2)} > \cdots > V_{(k-1)} = V_{(k)} > V_{(k+1)} > \cdots > V_{(n-1)} \tag{23}$$

then the operating-point terminal currents of the no-gain resistor $\mathcal{R}$ must satisfy the following system of inequalities

$$I_{(1)} > 0 \tag{24a}$$

$$I_{(1)} + I_{(2)} > 0 \tag{24b}$$

$$\vdots$$

$$I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} > 0 \tag{24c}$$

$$I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k-1)} + I_{(k)} > 0 \tag{24d}$$

$$I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k-1)} \geq 0 \tag{24e}$$

$$I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k)} \geq 0 \tag{24f}$$

$$I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k-1)} + I_{(k)} + I_{(k+1)} > 0 \tag{24g}$$

$$\vdots$$

$$I_{(1)} + I_{(2)} + \cdots + I_{(k)} + \cdots + I_{(n-1)} > 0 \tag{24h}$$

Lemma 3

Given any set of n-1 node-to-datum voltages satisfying (21) {resp.; (23)}, and any set of terminal currents satisfying (22) {resp.; (24)}, there exists a connected n-terminal network containing n-1 linear positive two-terminal resistors having the same operating point voltages and currents.

With these two lemmas, we will now proceed to complete the necessity proof of Theorem 1 by first assuming that the operating-point voltages satisfy either the strict inequality of (21) or the mixed inequality of (23). By Lemma 2, the operating-point currents must satisfy the strict inequality of (22) in the former case and the mixed inequality of (24) in the latter case. It

follows from Lemma 3 that there exists a connected n-terminal network containing n-1 linear positive two-terminal resistors having the same operating-point voltages and currents as the no-gain resistor $\mathcal{R}$.

Using exactly the same procedures as in the proofs of Lemmas 2 and 3, it is easy to show that in the cases where there are more than two terminals of $\mathcal{R}$ having identical potential at a particular operating-point such as

$$V_{(1)} > \cdots > V_{(\alpha)} = V_{(\alpha+1)} = \cdots = V_{(\beta)} > V_{(\beta+1)} > \cdots$$

$$> V_{(\gamma)} = V_{(\gamma+1)} = \cdots = V_{(\delta)} > \cdots V_{(n-1)} \tag{25}$$

The corresponding operating-point terminal currents of $\mathcal{R}$ must satisfy the following system of mixed inequalities

$$\left.\begin{array}{l}
I_{(1)} > 0 \\
\vdots \\
I_{(1)} + \cdots + I_{(\alpha-1)} > 0 \\
I_{(1)} + \cdots + I_{(\alpha-1)} + I_{(\alpha)} + \cdots + I_{(\beta)} > 0 \\
I_{(1)} + \cdots + I_{(\alpha-1)} + I_{(p)} \gtrless 0 \quad \text{for } p = \alpha, \alpha+1, \cdots, \beta \\
\vdots \\
I_{(1)} + \cdots + I_{(\alpha)} + \cdots + I_{(\gamma-1)} > 0 \\
I_{(1)} + \cdots + I_{(\alpha)} + \cdots + I_{(\gamma-1)} + I_{(\gamma)} + \cdots + I_{(\delta)} > 0 \\
\vdots \\
I_{(1)} + \cdots + I_{(\alpha)} + \cdots + I_{(\gamma-1)} + I_{(p)} \gtrless 0 \quad \text{for } p = \gamma, \gamma+1, \cdots, \delta \\
\vdots \\
I_{(1)} + \cdots + I_{(\alpha)} + \cdots + I_{(\delta)} + \cdots + I_{(n-1)} > 0
\end{array}\right\} \tag{26}$$

In turn the two systems of mixed inequalities in (25) and (26) guarantee that a connected n-terminal network, containing n-1 positive linear two-terminal resistors having the same operating-point voltages and currents as the no-gain resistor $\mathcal{R}$, can be constructed. Hence the necessity part of the theorem is proved. This completes the proof of Theorem 1. ¤

Corollary to Theorem 1 Interconnection of No-Gain Resistors (Closure Property)

Let $\mathcal{R}$ be a connected n-terminal network obtained by a valid

interconnection[11] of m multi-terminal resistors R_1, R_2, ..., R_m, where R_i is an n_i-terminal resistor and $n_i \geq 2$ for $i = 1, 2, \ldots, m$. If R_1, R_2, ..., R_m are no-gain resistors, then $\mathcal{R}$ is a no-gain n-terminal element.

Proof: Let $\mathcal{R}$ be imbedded in an arbitrary network N containing positive linear two-terminal resistors, independent voltage and current sources, short and open circuit elements which do not form $\mathcal{S}$-loops or $\mathcal{O}$-cutsets, respectively. Let Q be an operating point of the resulting circuit. This gives rise to an operating point Q_i for each resistor R_i inside $\mathcal{R}$. Since each R_i is a no-gain resistor, it can be replaced by $n_i - 1$ positive linear two-terminal resistors, having the same operating point Q_i. If this procedure is repeated for all resistors R_1, R_2, ..., R_m inside $\mathcal{R}$, the resulting network inside $\mathcal{R}$ contains only two-terminal positive linear resistors, which when imbedded in N will produce the operating point Q. This implies that the operating point Q possesses the no-gain property. In addition, one can use the technique employed in the proof of Theorem 1 to show that all terminal currents of $\mathcal{R}$ also satisfy the no-gain property. Hence $\mathcal{R}$ is a no-gain resistor. ¤

Lemmas 2 and 3 have been formulated with the assumption that the terminals have been ordered and relabelled such that (21) and (23) are satisfied. In the following applications of these lemmas, it is convenient to reformulate them without any terminal relabelling. This can be achieved through the introduction of appropriate notations as given in the following properties.

Property 7 No-Gain Resistor Criteria in Terms of Terminal Currents

An n-terminal resistor $\mathcal{R}$, shown in Fig. 1, is a no-gain element if, and only if, the following conditions are satisfied[12]

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[11] A valid interconnection implies that each terminal of every multi-terminal resistor, say R_i, inside $\mathcal{R}$ is either a terminal of $\mathcal{R}$ or else it must satisfy the following constraints:
i) It is connected to at least one other multi-terminal resistor, say R_j with $j \neq i$, inside $\mathcal{R}$
ii) It is connected to at most one terminal of each multi-terminal resistor inside $\mathcal{R}$
iii) It is not connected to any other terminal of R_i.
This is to insure that the interconnection of R_1, R_2, ..., R_m does not produce short circuit and open circuit elements.

[12] Observe that conditions (1a), (1b), (2a) ... are written in a compact form. When expanded, each will give rise to several inequalities. A detailed expansion of these conditions is given in Corollary 7.2 for the case where n = 3.

(1a) $i_k \geqq 0$ whenever $v_k \geqq v_j$

(1b) $i_k \leqq 0$ whenever $v_k \leqq v_j$

for all $j = 1, 2, \ldots, n$, $j \neq k$; and $k = 1,2,\ldots,n$.

(2a) $i_{k_1} + i_{k_2} \geqq 0$ whenever $v_{k_1} \geqq v_{k_j}$ and $v_{k_2} \geqq v_j$

(2b) $i_{k_1} + i_{k_2} \leqq 0$ whenever $v_{k_1} \leqq v_j$ and $v_{k_2} \leqq v_j$

for all $j = 1, 2, \ldots, n$, $j \neq k_1, k_2$ and
$k_1, k_2 = 1, 2, \ldots, n$ with $k_1 \neq k_2$.

(3a) $i_{k_1} + i_{k_2} + i_{k_3} \geqq 0$ whenever $v_{k_1} \geqq v_j$, $v_{k_2} \geqq v_j$ and $v_{k_3} \geqq v_j$

(3b) $i_{k_1} + i_{k_2} + i_{k_3} \leqq 0$ whenever $v_{k_1} \leqq v_j$, $v_{k_2} \leqq v_j$ and $v_{k_3} \leqq v_j$

for all $j = 1, 2, \ldots, n$, $j \neq k_1, k_2, k_3$ and
$k_1, k_2, k_3 = 1, 2, \ldots, n$ with $k_1 \neq k_2 \neq k_3$

$\vdots$

((n-1)a) $i_{k_1} + i_{k_2} + \ldots + i_{k_{n-1}} \geqq 0$ whenever $v_{k_p} \geqq v_j$

((n-1)b) $i_{k_1} + i_{k_2} + \ldots + i_{k_{n-1}} \leqq 0$ whenever $v_{k_p} \leqq v_j$

for $j = 1, 2, \ldots, n$, $j \neq k_p$ for $p = 1, 2, \ldots, n-1$,
$k_1, k_2, \ldots, k_{n-1} = 1, 2, \ldots, n$ with $k_1 \neq k_2 \neq \ldots \neq k_{n-1}$

where the symbol "$\geqq$" is used to denote that the equality sign on the left can hold only if at least <u>one</u> of the equality signs on the right holds.

<u>Proof</u>: In view of Lemmas 2 and 3, $\mathcal{R}$ is a no-gain element if, and only if, at every operating point where the terminal voltages satisfy (21) {resp.; (23)}, the terminal currents of $\mathcal{R}$ are constrained by (22) {resp.; (24)}. Conditions (1a), (2a),...((n-1)a) of Property 7 are merely a systematic method of representing the

conditions in Lemmas 2 and 3 for an n-terminal resistor with fixed labels. Conditions (1b); (2b),...((n-1)b) follow from Lemmas 4 and 5 which are stated below.

Lemma 4

Using the notation of Lemma 2, we have:

(a) if the operating point node-to-datum voltages of $\mathcal{R}$ satisfy

$$V_{(n)} < v_{(n-1)} < \cdots < v_{(2)} < \cdots < v_{(2)} < v_{(1)} \tag{27}$$

then the corresponding operating point terminal currents of $\mathcal{R}$ must satisfy the following system of strict inequalities:

$$\left.\begin{aligned} &I_{(n)} < 0 \\ &I_{(n)} + I_{(n-1)} < 0 \\ &\vdots \\ &I_{(n)} + I_{(n-1)} + \cdots + I_{(k)} < 0 \\ &\vdots \\ &I_{(n)} + I_{(n-1)} + \cdots + I_{(k)} + \cdots + I_{(2)} < C \end{aligned}\right\} \tag{28}$$

(b) if the operating point node-to-datum voltages of $\mathcal{R}$ satisfy

$$v_{(n)} < v_{(n-1)} < \cdots < v_{(k+1)} = v_{(k)} < \cdots < v_{(2)} < v_{(1)} \tag{29}$$

then the corresponding operating-point terminal currents of $\mathcal{R}$ must satisfy the following system of mixed inequalities:

$$\left.\begin{aligned} &I_{(n)} < 0 \\ &I_{(n)} + I_{(n-1)} < 0 \\ &\vdots \\ &I_{(n)} + I_{(n-1} + \cdot\cdot + I_{(k+2)} < 0 \\ &I_{(n)} + I_{(n-1)} + \cdots + I_{(k+2)} + I_{(k+1)} + I_{(k)} < 0 \\ &I_{(n)} + I_{(n-1)} + \cdots + I_{(k+2)} + I_{(k+1)} \leq 0 \\ &I_{(n)} + I_{(n-1)} + \cdots + I_{(k+2)} + I_{(k)} \leq 0 \end{aligned}\right\} \tag{30}$$

$$I_{(n)} + I_{(n-1)} + \cdots + I_{(k+2)} + I_{(k+1)} + I_{(k)} + I_{(k-1)} < 0$$

$$\vdots$$

$$I_{(n)} + I_{(n-1)} + \cdots + I_{(2)} < 0$$

Proof: The conclusions of Lemma 4 follow from Lemma 2 and the observation that

$$I_{(1)} + I_{(2)} + \cdots + I_{(k)} + \cdots + I_{(n)} = 0 \qquad (31)$$

¤

Lemma 5

Given any set of n-1 node-to-datum voltages satisfying (27) {resp.; (29)}, and any set of terminal currents satisfying (28) {resp.; (30)}, then there exists a connected n-terminal network containing n-1 linear positive two-terminal resistors having the same operating point voltages and currents.

Proof: The proof of Lemma 5 is similar to that of Lemma 3 and hence is omitted.

¤

Corollary 7.1 No-Gain Criteria in Terms of Conductance Representation

Let $\mathcal{R}$ be an n-terminal resistor admitting an (n-1)-port conductance representation

$$i_k = g_k\,(v_1, v_2, \ldots, v_{n-1}) \triangleq g_k(\underset{\sim}{v}), \qquad k = 1,2,\ldots,n-1 \qquad (32)$$

where $\underset{\sim}{v} = [v_1, v_2, \ldots, v_{n-1}]^t$ is the node-to-ground port-voltage vector and node ⓝ is the common ground for all ports, as shown in Fig. 5. Then $\mathcal{R}$ is a no-gain element if, and only if, the following conditions are satisfied,

(1a) $g_k(\underset{\sim}{v}) \geq 0$ whenever $v_k \geq 0$ and $v_k \geq v_j$

(1b) $g_k(\underset{\sim}{v}) \leq 0$ whenever $v_k \leq 0$ and $v_k \leq v_j$

for all $j = 1, 2, \ldots, n-1$, $j \neq k$, and $k = 1, 2, \ldots, n-1$

(2a) $g_{k_1}(\underset{\sim}{v}) + g_{k_2}(\underset{\sim}{v}) \geq 0$ whenever $v_{k_1} \geq 0$, $v_{k_1} \geq v_j$, $v_{k_2} \geq 0$, $v_{k_2} \geq v_j$

(2b) $g_{k_1}(\underset{\sim}{v}) + g_{k_2}(\underset{\sim}{v}) \leq 0$ whenever $v_{k_1} \leq 0$, $v_{k_1} \leq v_j$, $v_{k_2} \leq 0$, $v_{k_2} \leq v_j$

for all $j = 1, 2, \ldots, n-1,\ j \neq k_1, k_2$
and $k_1, k_2 = 1, 2, \ldots, n-1$ with $k_1 \neq k_2$.

(3a) $g_{k_1}(\underset{\sim}{v}) + g_{k_2}(\underset{\sim}{v}) + g_{k_3}(\underset{\sim}{v}) \geq 0$ whenever

$$v_{k_1} \geqq 0,\ v_{k_1} \geqq v_j,\ v_{k_2} \geqq 0,\ v_{k_2} \geqq v_j,\ v_{k_3} \geqq 0,\ v_{k_3} \geqq v_j$$

(3b) $g_{k_1}(\underset{\sim}{v}) + g_{k_2}(\underset{\sim}{v}) + g_{k_3}(v) \leq 0$ whenever

$$v_{k_1} \leqq 0,\ v_{k_1} \leqq v_j,\ v_{k_2} \leqq 0,\ v_{k_2} \leqq v_j,\ v_{k_3} \leqq 0,\ v_{k_3} \leqq v_j$$

for all $j = 1, 2, \ldots, n-1,\ j \neq k_1, k_2, k_3$
and $k_1, k_2, k_3 = 1, 2, \ldots, n-1$ with $k_1 \neq k_2 \neq k_3$.

$\vdots$

((n-1)a) $g_{k_1}(\underset{\sim}{v}) + g_{k_2}(\underset{\sim}{v}) + \ldots + g_{n-1}(\underset{\sim}{v}) \geqq 0$ whenever $v_k \geqq 0$

((n-1)b) $g_{k_1}(\underset{\sim}{v}) + g_{k_2}(\underset{\sim}{v}) + \ldots + g_{n-1}(\underset{\sim}{v}) \leqq 0$ whenever $v_k \geqq 0$

for all $k = 1, 2, \ldots, n-1$

where the symbol "$\geqq$" is used to denote that the equality sign on the left can hold only if at least <u>one</u> of the equality signs on the right holds.

Proof: Corollary 7.1 follows directly from Property 7 with

$$v_n = 0 \tag{33}$$

n

<u>Corollary 7.2</u>

Let $\mathcal{R}$ be a 3-terminal resistor characterized by a two port conductance representation

$$i_1 = g_1(v_1, v_2)$$

$$i_2 = g_2(v_1, v_2)$$

then $\mathcal{R}$ is a no-gain element if, and only if,

(1a) $g_1(v_1,v_2) \geqq 0$ whenever $v_1 \geqq v_2$, $v_1 \geqq 0$

(1b) $g_1(v_1,v_2) \leqq 0$ whenever $v_1 \leqq v_2$, $v_1 \leqq 0$

(2a) $g_2(v_1,v_2) \geqq 0$ whenever $v_2 \geqq v_1$, $v_2 \geqq 0$

(2b) $g_2(v_1,v_2) \leqq 0$ whenever $v_2 \leqq v_1$, $v_2 \leqq 0$

(3a) $g_1(v_1,v_2) + g_2(v_1,v_2) \geqq 0$ whenever $v_1 \geqq 0$, $v_2 \geqq 0$

(3b) $g_1(v_1,v_2) + g_2(v_1,v_2) \leqq 0$ whenever $v_1 \leqq 0$, $v_2 \leqq 0$

Remark

Corollary 7.2 serves as an example of the detailed expansion of Corollary 7.1 for a specific value of n=3. Without the symbol "$\leqq$", as defined in Property 7, the equations would have to be expanded further to convey the proper meaning. For example condition (1a) of Corollary 7.2 could be written as the following 4 statements

$g_1(v_1,v_2) > 0$ whenever $v_1 > 0$ and $v_1 > v_2$ (34a)

$g_1(v_1,v_2) \geq 0$ whenever $v_1 = 0$ and $v_1 > v_2$ (34b)

$g_1(v_1,v_2) \geq 0$ whenever $v_1 > 0$ and $v_1 = v_2$ (34c)

$g_1(v_1,v_2) \geq 0$ whenever $v_1 = 0$ and $v_1 = v_2$ (34d)

where (34d) and its counterpart in condition (1b) of Corollary 7.2 together imply that

$g_1(v_1,v_2) = 0$ whenever $v_1 = 0$ and $v_2 = 0$ (35)

This Corollary corresponds to Theorem 5 of [3], where Willson has listed only three equations, in effect combining (1a) and (1b), (2a) and (2b), and (3a) and (3b). In doing this the boundary value information is lost, and he either requires that $g_1(\cdot)$ and $g_2(\cdot)$ be continuous or an additional 4 equations are required to specify the nature of $g_1(\cdot)$ and $g_2(\cdot)$ on the boundaries.

Property 8 No-Gain Resister Criteria in Terms of Terminal Voltages

Let $\mathcal{R}$ be an n-terminal resistor with terminal currents and voltages defined as in Fig. 1. Then $\mathcal{R}$ is a no-gain element if, and only if, the following conditions are satisfied:

(1) At every operating point where not all the terminal currents of $\mathcal{R}$ are zero, and for every pair of terminals j, k = 1,2,...,n where $j \neq k$, we have

(a) $v_k - v_j > 0$ {resp.; ≥ 0} if either $i_k > 0$ {resp.; $= 0$}, $i_j < 0$ and $i_m \geq 0$; or $i_k > 0, i_j < 0$ {resp.; $= 0$}, and $i_m \leq 0$ for all m = 1, 2, ..., n where $m \neq j$ and $m \neq k$.

(b) $v_k - v_j < 0$ {resp.; ≤ 0} if either $i_k < 0$ {resp.; $= 0$}, $i_j > 0$ and $i_m \leq 0$; or $i_k < 0, i_j > 0$ {resp.; $= 0$}, and $i_m \geq 0$ for all m = 1, 2, ..., n where $m \neq j$ and $m \neq k$.

(c) the terminal current of the highest {resp.; lowest} potential terminal of $\mathcal{R}$ is positive {resp.; negative}. In the case where two or more terminals of $\mathcal{R}$ are at the same highest {resp.; lowest} potential, at least one of them must have a positive {resp.; negative} terminal current.

(2) At the operating point where all terminal currents $\mathcal{R}$ are zero, we have

$$v_k = 0 \quad \text{for all } k = 1, 2, \ldots, n.$$

Remark

Although it is not obvious, the conditions of Properties 7 and 8 are duals to each other. The proof of Property 8 is based on the dual versions of Lemmas 2 to 5. The details of the proof are given in the Appendix.

Corollary 8.1 No-Gain Criteria in terms of Resistance Representation

Let $\mathcal{R}$ be an n-terminal resistor admitting an (n-1)-port resistance representation

$$v_k = r_k(i_1, i_2, \ldots, i_{n-1}) = r_k(\underset{\sim}{i}) \qquad k = 1,2,\ldots,n-1 \tag{36}$$

where $\underset{\sim}{i} = [i_1, i_2, \ldots, i_{n-1}]^t$ are the port-currents, and $\underset{\sim}{v} = [v_1, v_2, \ldots, v_{n-1}]^t$

are the node-to-datum port-voltages as shown in Fig. 5. Then $\mathcal{R}$ is a no-grain element if, and only if, $r_k(0) = 0$ for $k = 1,2,\ldots,n-1$ and the following conditions are satisfied:

(1) For any pair of terminals $j, k = 1,2,\ldots,n-1$ where $j \neq k$

(1a) $r_k(\underset{\sim}{i}) - r_j(\underset{\sim}{i}) > 0$ {resp.; ≥ 0} if either $i_k > 0$ {resp.; $= 0$}, $i_j < 0$, $i_m \geq 0$, and $i_1 + i_2 + \cdots + i_{n-1} \leq 0$; or $i_k > 0$, $i_j < 0$ {resp.; $= 0$}, $i_m \leq 0$, and $i_1 + i_2 + \cdots + i_{n-1} \geq 0$ for all $m = 1, 2, \ldots, n-1$ where $m \neq j$ and $m \neq k$.

(1b) $r_k(\underset{\sim}{i}) - r_j(\underset{\sim}{i}) < 0$ {resp.; ≤ 0} if either $i_k < 0$ {resp.; $= 0$}, $i_j > 0$, $i_m \leq 0$, and $i_1 + i_2 + \ldots + i_{n-1} \geq 0$; or $i_k < 0$, $i_j > 0$ {resp.; $= 0$}, $i_m \geq 0$, and $i_1 + i_2 + \ldots + i_{n-1} \leq 0$ for all $m = 1, 2, \ldots, n-1$ where $m \neq j$ and $m \neq k$.

(2) For any terminal $k = 1,2,\ldots,n$

(2a) $r_k(\underset{\sim}{i}) > 0$ {resp.; ≥ 0} if either $i_k > 0$ {resp.; $= 0$}, $i_1 + i_2 + \cdots + i_{n-1} > 0$, and $i_m \geq 0$; or $i_k > 0$, $i_1 + i_2 + \cdots + i_{n-1} > 0$ {resp.; $= 0$}, and $i_m \leq 0$ for all $m = 1, 2, \ldots, n-1$ where $m \neq k$.

(2b) $r_k(\underset{\sim}{i}) < 0$ {resp., ≤ 0} if either $i_k < 0$ {resp.; $= 0$}, $i_1 + i_2 + \cdots + i_{n-1} < 0$, and $i_m \leq 0$; or $i_k > 0$, $i_1 + i_2 + \cdots + i_{n-1} < 0$ {resp.; $= 0$} for all $m = 1, 2, \ldots, n-1$ where $m \neq k$.

(3) For each $m = 1, 2, \ldots, n-1$ where $i_m = 0$, we have

$$\min_{\substack{j=1,2,\ldots,n-1 \\ j\neq m}} r_j(\underset{\sim}{i}) \leq r_m(\underset{\sim}{i}) \leq \max_{\substack{j=1,2,\ldots,n-1 \\ j\neq m}} r_j(\underset{\sim}{i})$$

Proof: Corollary 8.1 follows directly from Property 8 by noting that $v_n = 0$ and $i_1 + i_2 + \cdots + i_{n-1} + i_n = 0$. Hence the proof of Corollary 8.1 is omitted. ¤

B. Locally No-Gain Elements

Definition 6 Locally No-Gain Elements

An n-terminal resistor $\mathcal{R}$, with terminal currents and voltages as defined in Fig. 1, is said to be locally no-gain at an operating point Q if, and only if, for every pair of incremental terminal voltage and current vector $(\delta\underset{\sim}{v}, \delta\underset{\sim}{i})$ consistent with the characteristics of $\mathcal{R}$ at the point Q, where

$$\delta\underset{\sim}{v} = [\delta v_1, \delta v_2, \ldots, \delta v_{n-1}]^t \text{ and } \delta\underset{\sim}{i} = [\delta i_1, \delta i_2, \ldots, \delta i_{n-1}]^t,$$

there exists a connected network with n-1 positive linear two-terminal resistors having the operating point $(\delta\underset{\sim}{v}, \delta\underset{\sim}{i})$. $\mathcal{R}$ is said to be a <u>locally no-gain element</u> if $\mathcal{R}$ is locally no-gain at every point in the characteristics of $\mathcal{R}$.

<u>Property 9</u> Locally No-Gain Conductance Matrix

Let $\mathcal{R}$ be an n-terminal resistor admitting an (n-1)-port C^1-conductance representation

$$\underset{\sim}{i} = \underset{\sim}{g}(\underset{\sim}{v}) \tag{37}$$

where $\underset{\sim}{v} = [v_1, v_2, \ldots, v_{n-1}]^t$ and $\underset{\sim}{i} = [i_1, i_2, \ldots, i_{n-1}]^t$ are the port-voltage and port-current vectors, as shown in Fig. 5, and $g(\cdot) = [g_1(\cdot), g_2(\cdot), \ldots g_{n-1}(\cdot)]^t$. Terminal ⓝ is the common terminal for all ports and v_k is the voltage across terminals ⓚ and ⓝ and i_k is the current entering terminal ⓚ of $\mathcal{R}$. Then $\mathcal{R}$ is a locally no-gain element if, and only if, at each operating point voltage $\underset{\sim}{v}_Q$ of $\mathcal{R}$, the incremental <u>conductance matrix</u>

$$\underset{\sim}{G} \triangleq [g_{jk}] \triangleq \left[\frac{\partial g_j(\underset{\sim}{v})}{\partial v_k}\right]\Bigg|_{\underset{\sim}{v} = \underset{\sim}{v}_Q} \tag{38}$$

satisfies the following conditions:

(1) $g_{kk} > 0$ for all k = 1, 2, ..., n-1 (39a)

(2) $g_{jk} \leq 0$ for all j, k = 1, 2, ..., n-1, where $j \neq k$ (39b)

(3) $g_{kk} \geq -\sum_{\substack{j=1 \\ j\neq k}}^{n-1} g_{kj} \geq 0$ for all k = 1, 2, ..., n-1 (40a)

(4) $g_{kk} \geq -\sum_{\substack{j=1 \\ j\neq k}}^{n-1} g_{jk} \geq 0$ for all k = 1, 2, ..., n-1 (40b)

(5) For each $\ell \times \ell$ principal submatrix[13] $\underset{\sim}{G}_\ell$ of $\underset{\sim}{G}$, the sum of the diagonal elements of $\underset{\sim}{G}_\ell$ is strictly greater than the negative of the sum of the off diagonal elements, i.e.,

$$\sum_{j=1}^{\ell} \left(\underset{\sim}{G}_\ell\right)_{jj} > - \sum_{\substack{j=1 \\ j\neq k}}^{\ell} \sum_{k=1}^{\ell} \left(\underset{\sim}{G}_\ell\right)_{jk} \tag{41}$$

where $\ell = 1, 2, \ldots, n-1$.

Remark

Property 9 is a direct consequence of Corollary 7.1 with (32) replaced by

$$\delta i_k = g_k(\delta \underset{\sim}{v}) \triangleq \sum_{j=1}^{n-1} g_{kj} \delta v_j \quad \text{for } k = 1, 2, \ldots, n-1 \tag{42}$$

The details for the proof of Property 9 are given in the Appendix.

From (39), the locally no-gain conductance matrix $\underset{\sim}{G}$ is seen to have positive diagonal and non-positive off diagonal elements. A matrix with this property is referred to as a Z-matrix in [12] and an M-matrix in [13]. Equation (40) states that $\underset{\sim}{G}$ is both a row and column dominant matrix. In [14] a matrix that satisfies both (39) and (40) is defined as being hyperdominant. (The column dominance is not specifically mentioned since the matrices considered in [14] are symmetric). Together (40) and (41) imply that $\underset{\sim}{G}$ is positive definite. A matrix that satisfies conditions (1) through (5) of Property 9 will henceforth be called a locally no-gain conductance matrix.

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[13] Let $\underset{\sim}{A} = [a_{jk}]$ be an $m \times m$ matrix. An $\ell \times \ell$ principal submatrix $\underset{\sim}{A}_\ell$ of $\underset{\sim}{A}$ is obtained by deleting $(m-\ell)$ columns and the corresponding $(m-\ell)$ rows, i.e.,

$$\underset{\sim}{A}_\ell = \begin{bmatrix} a_{j_1 j_1} & a_{j_1 j_2} & \cdots & a_{j_1 j_\ell} \\ a_{j_2 j_1} & a_{j_2 j_2} & \cdots & a_{j_2 j_\ell} \\ \vdots & \vdots & & \vdots \\ a_{j_\ell j_1} & a_{j_\ell j_2} & \cdots & a_{j_\ell j_\ell} \end{bmatrix}$$

where $1 \leq j_1 < j_2 < \cdots < j_\ell \leq m$.

Recall that an (n-1) × (n-1) matrix is realizable as the short circuit conductance matrix of a common-ground (n-1)-port resistance network containing only n-terminals if, and only if, the matrix is symmetric, dominant and every off-diagonal element is non-positive [15]. Hence, even if we assume that $\mathcal{R}$ is reciprocal, that is, the locally no-gain conductance matrix is symmetric, a realizable short-circuit conductance matrix need only satisfy conditions (1) through (4) of Property 9. Thus the requirements on a symmetric locally no-gain conductance matrix are stronger than the realizability criteria for a short-circuit conductance matrix. This unexpected result stems from the fact that the circuit used to realize a locally no-gain conductance matrix is required to be connected, as stated in Definition 6 while a circuit realization of a short-circuit conductance matrix is not, in general, required to be connected. It can be shown that every connected resistive (n-1)-port network containing n-1 or more positive linear two-terminal resistors has a short-circuit conductance matrix that satisfies all the criteria of a locally no-gain conductance matrix.

We can relate the locally no-gain requirements and the locally passive criteria by the following two corollarys to Property 9.

Corollary 9.1 Locally No-Gain and Locally Strictly Passive Resistors

A locally no-gain n-terminal resistor $\mathcal{R}$ characterized by a C^1-conductance representation $\underset{\sim}{i} = \underset{\sim}{g}(\underset{\sim}{v})$ is strictly locally passive.

Proof: It follows from Property 2 that $\mathcal{R}$ is strictly locally passive if its incremental conductance matrix

$$\underset{\sim}{G}(\underset{\sim}{v}) = \left[\frac{\partial g_j(\underset{\sim}{v})}{\partial v_k}\right]\Bigg|_{\underset{\sim}{v}=\underset{\sim}{v}_Q}$$

is positive definite for all $\underset{\sim}{v} = \underset{\sim}{v}_Q$. Since the locally no-gain conductance matrix is positive definite at each possible operating point of $\mathcal{R}$, it follows that if $\mathcal{R}$ is a locally no-gain element then it is strictly locally passive. ∎

Observe that the converse of Corollary 9.1 is not true. For example, let $\mathcal{R}$ be a 3-terminal resistor characterized by

$$i_1 = 3v_1 + v_2 \triangleq g_1(v_1,v_2)$$

$$i_2 = v_1 + 3v_2 \triangleq g_2(v_1,v_2)$$

Clearly $\mathcal{R}$ is locally strictly passive but not locally no-gain.

Corollary 9.2 Locally No-Gain and Strictly Passive Resistors

A locally no-gain n-terminal resistor characterized by a C^1-conductance representation $\underset{\sim}{i} = \underset{\sim}{g}(\underset{\sim}{v})$ is strictly passive if, and only if, its constitutive relation passes through the origin.

Proof: This follows immediately from Corollaries 9.1 and 3.2. ∎

Property 10. Locally No-Gain Resistance Matrix

Let $\mathcal{R}$ be an n-terminal resistor admitting an (n-1)-port C^1-resistance representation

$$\underset{\sim}{v} = \underset{\sim}{r}\,(\underset{\sim}{i}) \tag{43}$$

where $\underset{\sim}{i} = [i_1, i_2, \ldots, i_{n-1}]^t$ and $\underset{\sim}{v} = [v_1, v_2, \ldots, v_{n-1}]^t$ are the port-current and port-voltage vectors, v_k is the voltage across terminals ⓚ and ⓝ, i_k is the current entering terminal ⓚ of $\mathcal{R}$ as shown in Fig. 5, and $\underset{\sim}{r}(\cdot) = [r_1(\cdot), r_2(\cdot), \ldots r_{n-1}(\cdot)]^t$ is a C^1 vector-valued function. If $\mathcal{R}$ is a locally no-gain element then for each operating point current $\underset{\sim}{I}_Q$ of $\mathcal{R}$, the incremental resistance matrix

$$\underset{\sim}{R} \triangleq [r_{jk}] \triangleq \left[\frac{\partial r_j(\underset{\sim}{i})}{\partial i_k}\right]\Bigg|_{\underset{\sim}{i}=\underset{\sim}{I}_Q} \tag{44}$$

must satisfy the following conditions:

(1) $r_{kk} > 0$ for all k = 1, 2, ..., n-1

(2) $0 \leq r_{kj} \leq r_{kk}$ for all k, j = 1, 2, ..., n-1 where $k \neq j$

(3) $0 \leq r_{jk} \leq r_{kk}$ for all k, j = 1, 2, ..., n-1 where $k \neq j$

(4) $0 \leq r_{jk} + r_{kj} < r_{kk} + r_{jj}$ for all k, j = 1, 2, ..., n-1 where $k \neq j$

(5) $0 \leq r_{jk} + r_{k\ell} \leq r_{kk} + r_{j\ell}$ for all j, k, ℓ = 1, 2, ..., n-1 where $j \neq k \neq \ell$

(6) $r_{kk}r_{j\ell} \geq r_{k\ell}r_{jk}$ for all j, k, ℓ = 1, 2, ..., n-1 where $j \neq k \neq \ell$

(7) In any n×k submatrix of $\underset{\sim}{R}$, the maximum sum of the elements in each row of

the submatrix must occur at a row which contains a diagonal element.

Remark

Property 10 is a direct consequence of Corollary 8.1 with (36) replaced by

$$\delta v_k = r_k(\delta \underset{\sim}{i}) \triangleq \sum_{j=1}^{n-1} r_{kj}\delta i_j \text{ for } k = 1, 2, \ldots, n-1 \tag{45}$$

The details of the proof of Property 10 are given in the Appendix.

The inverse of the no-gain resistance matrix must be a no-gain conductance matrix. We have not been able to prove that conditions (1) through (7) of Property 10 are sufficient to insure this result. For a symmetric matrix representation it can be shown that all of the conditions are necessary in order to obtain a inverse matrix that has the hyperdominant property.

C. Weakly No-Gain Elements

Before we proceed to introduce the concept of weakly no-gain elements, let us first consider the following property, which can be considered as a generalization of Property 6.

Property 11 No-Gain Networks containing Two-Terminal Elements Only

A network containing nonzero independent voltage and current sources, two-terminal "strictly passive" resistors, and two-terminal "exclusively passive" resistors[14] which do not form loops and cutsets by themselves has the no-gain property.

Proof: Let N be a network satisfying the hypotheses and let Q be an operating-point of N. By Corollary 7.1, a strictly passive two-terminal resistor is a no-gain element. Hence it can be replaced by a two-terminal positive linear resistor having the same operating-point, as indicated by Theorem 1. Let (V_p, I_p) be the corresponding operating-point voltage and current of an "exclusively passive" two-terminal resistor R_p. Then $V_p I_p \geq 0$. Observe that R_p can be replaced by a two-terminal linear element having the same operating-point (V_p, I_p), where the linear two-terminal element is defined by:

[14] An element will henceforth be called an "exclusively passive element" if it is passive but not strictly passive.

(a) a positive linear two-terminal resistor with a resistance equal to V_p/I_p Ω if $I_p V_p \neq 0$, and equal to 1Ω if $I_p = V_p = 0$

(b) a short circuit element if $V_p = 0$

(c) an open circuit element if $I_p = 0$

Let $\hat{N}$ be the circuit obtained from N by replacing each strictly passive two-terminal resistor by a positive linear two-terminal resistor having the same operating point, and each "exclusively passive" two-terminal resistor by either a positive linear resistor or an open or a short circuit element having the same operating-point. Then $\hat{N}$ has the same operating-point Q as N. Since the exclusively passive elements in N do not form loops or cutsets, there are no $\mathcal{S}$-loops or $\mathcal{O}$-cutsets in $\hat{N}$--$\hat{N}$ satisfies all conditions of Property 6 -- and hence the operating-point voltages and currents associated with Q possesses the no-gain property. Consequently, N is a no-gain network. ¤

Observe that Theorem 1 implies that every no-gain resistor is at least strictly passive. This excludes many networks containing exclusively passive elements such as ideal diodes, ideal zener diodes and all kinds of three-terminal resistors having an input-output family of curves in the first quadrant plus a negative axis such as those shown in Fig. 6. However, Property 11 clearly demonstrates that the class of no-gain networks may include "exclusively passive" elements as well. This observation motivates the following definition.

Definition 7 Weakly No-Gain Elements

An n-terminal ($n \geq 2$) resistor $\mathcal{R}$ is said to be a weakly no-gain element if each connected network containing $\mathcal{R}$, positive linear two-terminal resistors, and nonzero independent voltage and current sources possesses the no-gain property.[15]

To derive the basic properties of a weakly no-gain element, we need to develop the following two lemmas.

Lemma 6

Let $\mathcal{R}$ be a "weakly" no-gain n-terminal resistor imbedded in a network N

[15] Willson's definition of a no-gain element coincides with our definition of a "weakly no-gain element" [3]. However, his results are applicable only to networks containing no-gain elements as defined in our Definition 5, and therefore can not allow exclusively passive elements.

containing only positive linear two-terminal resistors and nonzero independent voltage and current sources. Let Q be an operating-point of $\mathcal{R}$. Let us choose the terminal of $\mathcal{R}$ having the lowest potential as the datum node and label the remaining n-1 terminals of $\mathcal{R}$ so that the operating-point terminal voltages of $\mathcal{R}$ satisfy the inequality

$$V_{(1)} \geq V_{(2)} \geq \cdots \geq V_{(k)} \geq \cdots \geq V_{(n-1)} \geq 0 \tag{46}$$

where $V_{(1)}$ {resp.; $V_{(2)}, V_{(3)}, \cdots$} is the voltage between the highest {resp.; second highest, third highest, $\cdots$} and the lowest potential (datum) node of $\mathcal{R}$. Let $I_{(1)}, I_{(2)}, \cdots, I_{(n-1)}$ be the corresponding operating-point currents of $\mathcal{R}$.

(a) If

$$V_{(1)} > V_{(2)} > \cdots > V_{(k)} > \cdots > V_{(n-1)} \tag{47}$$

Then the operating-point currents satisfy the following system of inequalities

$$\begin{aligned} &I_{(1)} \geq 0 \\ &I_{(1)} + I_{(2)} \geq 0 \\ &\vdots \\ &I_{(1)} + I_{(2)} + \cdots + I_{(k)} \geq 0 \\ &\vdots \\ &I_{(1)} + I_{(2)} + \cdots + I_{(k)} + \cdots + I_{(n-1)} \geq 0 \end{aligned} \tag{48}$$

(b) If

$$V_{(1)} > V_{(2)} > \cdots > V_{(k)} = V_{(k+1)} > \cdots > V_{(n-1)} \tag{49}$$

Then the operating-point currents satisfy the following system of inequalities

$$I_{(1)} \geq 0 \tag{50a}$$

$$I_{(1)} + I_{(2)} \geq 0 \tag{50b}$$

$$\vdots$$

$$I_{(1)} + I_{(2)} + \cdots + I_{(k-1)} \geq 0 \tag{50c}$$

$$I_{(1)} + I_{(2)} + \cdots + I_{(k-1)} + I_{(k)} + I_{(k+1)} \geq 0 \qquad (50d)$$

$$I_{(1)} + I_{(2)} + \cdots + I_{(k-1)} + I_{(k)} + I_{(k+1)} + I_{(k+2)} \geq 0 \qquad (50e)$$

$$\vdots$$

$$I_{(1)} + I_{(2)} + \cdots I_{(k)} + \cdots + I_{(n-1)} \geq 0 \qquad (50f)$$

Proof: The proof of Lemma 6 is given in the Appendix.

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Lemma 7

Given any set of n-1 node-to-datum voltages satisfying (47) {resp.; (49)}, and any set of terminal currents satisfying (48) {resp.; (50)}, there exists a (not necessarily connected) n-terminal network containing $m \leq n-1$ positive linear two-terminal resistors and $\ell \leq n-1$ short circuit and open circuit elements which do not form $\mathcal{S}$-loops and $\mathcal{O}$-cutsets respectively, where $m + \ell = n-1$, having the same operating point voltages and currents.

Proof. The proof of Lemma 7 is given in the Appendix.

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Property 12 Criteria for Weakly No-Gain Elements

An n-terminal resistor $\mathcal{R}$ is a weakly no-gain resistor if, and only if, at each dc operating-point Q of $\mathcal{R}$, there exists an n-terminal network N_Q having the same operating point Q, where N_Q contains $m \leq n-1$ positive linear two-terminal resistors and $\ell \leq n-1$ short circuit and open circuit elements which do not form $\mathcal{S}$-loops and $\mathcal{O}$-cutsets respectively, where $m + \ell = n-1$.

Proof: With Lemmas 6 and 7 replacing Lemmas 2 and 3, the proof of Property 12 parallels very closely with the proof of Theorem 1 and is therefore omitted.

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IV. BOUNDING REGIONS FOR DRIVING-POINT AND TRANSFER CHARACTERISTIC PLOTS

We will now apply the results from the preceding section to show that the DP and TC plots of a resistive network containing only no-gain multi-terminal resistors and independent sources must lie within some specific bounding regions. To do this, we must first generalize the well-known "maximum and minimum voltage node" theorem [16] to allow networks containing multi-terminal resistors.

Property 13. Maximum and Minimum Voltage Node Theorem

Let N be a connected resistive network containing only no-gain multi-terminal resistors and independent dc voltage and current sources. Then the highest potential node (resp.; lowest potential node) must necessarily be connected to either a voltage source, or a current source.

Proof. Since all multi-terminal resistors are no-gain by hypothesis, it follows from Theorem 1 that they can all be replaced by an appropriate interconnections of two-terminal positive linear resistors without affecting the node voltages. Hence the result follows immediately from the "maximum and minimum voltage node" theorem for networks containing two-terminal no-gain resistors and sources [16]. ¤

A dual version of Property 13, as well as of the following properties can be proved but are omitted to conserve space.

Property 14. Voltage Bound for No-Gain Networks with Grounded Sources

Let N be a connected resistive network containing only no-gain multi-terminal resistors and grounded dc voltage sources. Then the node-to-ground voltage $v_{\textcircled{k}}$ of any node ⓚ is bounded by

$$-E_{min} \leq v_{\textcircled{k}} \leq E_{max} \tag{51}$$

where E_{max} {resp.; $-E_{min}$} denotes the terminal voltage of the voltage source with the highest {resp.; lowest} node-to-ground voltage.

Proof. The network N can be represented with all voltage sources extracted as shown in Fig. 7, where N_0 contains only no-gain multi-terminal resistors. It follows from the definition of E_{max} and E_{min} that node ⓐ is the highest-potential node while node ⓑ is the lowest-potential node.

Let ⓚ be an arbitrary node of N_0, then

$$v_{\textcircled{k}} = v_{ka} + E_{max} = v_{kb} - E_{min} \tag{52}$$

It follows from Property 13 that

$$-(E_{max} + E_{min}) \leq v_{ka} \leq 0 \tag{53}$$

$$0 \leq v_{kb} \leq (E_{max} + E_{min}) \tag{54}$$

Adding E_{max} to both sides of (53) and adding $- E_{min}$ to both sides of (54), we obtain

$$- E_{min} \leq v_{ka} + E_{max} \leq E_{max} \tag{55}$$

$$- E_{min} \leq v_{kb} - E_{min} \leq E_{max} \tag{56}$$

Substituting either (55) or (56) into (52), we obtain (51). ¤

Corollary 14.1

The magnitude of the node-to-ground voltage of any connected network containing diodes, transistors, operational amplifiers,[16] and other no-gain multi-terminal resistors which are biased by a set of complementary dc power supplies of $\pm E_{CC}$ volts with respect to ground cannot exceed E_{CC}.

We are now ready to derive bounding regions for the v_0 - vs. - v_{in} TC plot of no-gain networks.

Property 15. TC Plot Bounding Region for Ungrounded Two-Ports

Let N be any connected network containing no-gain multi-terminal resistors and dc voltage sources as shown in Fig. 8(a), where nodes ⓑ and ⓓ are not necessarily connected to each other. Then we have:

(a) The TC plot must lie within the shaded region shown in Fig. 8(b), where E_0 denotes the sum of the voltage magnitudes of all internal voltage sources.

(b) If the input terminal ⓐ and output terminal ⓒ are connected together,[17] then the bounding region in Fig. 8(b) shrinks to that shown in Fig. 8(c).

(c) If all internal voltage sources are grounded as in Fig. 7, then the TC plot must lie within the shaded region shown in Fig. 8(d).

(d) If all voltage sources (including the input voltage source v_{in}) are grounded, then the bounding region shown in Fig. 8(d) shrinks further to that shown in Fig. 8(e).

(e) If all voltage sources (including the input voltage source v_{in}) are grounded,

[16] An operational amplifier here is considered as a six-terminal element with two of the six terminals being connected to two complementary power supplies, one with $+ E_{CC}$ and the other with $- E_{CC}$ volts with respect to ground [17].

[17] This somewhat specialized condition will turn out to be quite relevant to the proof of Property 17.

and if the input terminal ⓐ and output terminal ⓒ are connected together, then the bounding region shown in Fig. 8(e) shrinks further to that shown in Fig. 8(f).

Proof.

(a) Since N is a no-gain network, we have

$$|v_0| \leq |v_{in}| + E_0 \tag{57}$$

where

$$E_0 \triangleq \sum_{i=1}^{n} |E_i| \tag{58}$$

and n denotes the number of internal voltage sources. The bounding region defined by (57) is precisely that shown in Fig. 8(b).

(b) Consider first the case $0 \leq v_{in} \leq E_0$ and let v_{bd} denote the voltage between nodes ⓑ and ⓓ ; i.e.,

$$v_0 = v_{in} + v_{bd} \tag{59}$$

Since N contains only no-gain elements and dc voltage sources,

$$v_{bd} \geq - v_{in} - E_0 \tag{60}$$

where E_0 is as defined in (58). It follows from (59) and (60) that

$$v_0 \geq - E_0 \text{ whenever } 0 \leq v_{in} \leq E_0 \tag{61}$$

If $v_{in} \geq E_0$, then node ⓐ becomes the highest-potential node and hence

$$v_0 \geq 0 \quad \text{whenever} \quad v_{in} \geq E_0 \tag{62}$$

The bounding region in the fourth quadrant of Fig. 8(e) is precisely that defined by (61) and (62). A similar analysis shows that

$$v_0 \leq E_0 \quad \text{whenever} \quad - E_0 \leq v_{in} \leq 0 \tag{63}$$

and

$$v_0 \leq 0 \quad \text{whenever} \quad v_{in} \leq - E_0 \tag{64}$$

Equations (63) and (64) defined the shaded region shown in the second quadrant of Fig. 8(c). The bounding regions in the first and third quadrants follow from part (a).

(c) Since the node having the maximum or the minimum potential must be connected to a voltage source and since all internal voltage sources are connected to a common ground as in Fig. 7, the potential between the highest voltage node and the lowest voltage node cannot exceed $|v_{in}| + E_{max} + E_{min}$. Hence,

$$0 \leq v_0 \leq |v_{in}| + (E_{max} + E_{min}) \tag{65}$$

$$-(E_{max} + E_{min}) - |v_{in}| \leq v_0 \leq 0 \tag{66}$$

The bounding region defined by (65) and (66) is precisely that shown in Fig. 8(d).

(d) Since all voltage sources are grounded, using the same argument as above, we obtain

$$|v_0| \leq E_{max} + E_{min}, \text{ whenever } -E_{min} \leq v_{in} \leq E_{max} \tag{67}$$

$$|v_0| \leq v_{in} + E_{min}, \text{ whenever } v_{in} \geq E_{max} \tag{68}$$

$$|v_0| \leq v_{in} - E_{max}, \text{ whenever } v_{in} \leq -E_{min} \tag{69}$$

The bounding region defined by (67), (68), and (69) is precisely that shown in Fig. 8(e).

(e) It suffices to prove that $v_0 \geq 0$ whenever $v_{in} \geq E_{max}$ and $v_0 \leq 0$ whenever $v_{in} \leq -E_{min}$. The former is true since terminal ⓐ is the highest-potential node whenever $v_{in} \geq E_{max}$, while the latter is true because terminal ⓐ is the lowest-potential node whenever $v_{in} \leq -E_{min}$.

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Property 16. TC Plot Bounding Region for Grounded Two-Ports

Let N be a connected grounded network containing no-gain multi-terminal resistors and dc voltage sources as shown in Fig. 9(a).

(a) If all internal sources of N are grounded as in Fig. 7, then the TC plot must lie within the shaded region shown in Fig. 9(b), where E_{max} and $-E_{min}$ denote respectively the maximum and minimum node-to-ground voltage of the internal voltage sources.

(b) If all internal sources of N have their negative terminals grounded, then

the bounding region shown in Fig. 9(b) shrinks to that shown in Fig. 9(c).

(c) If N contains no internal sources, then the TC plot in Fig. 9(c) further shrinks to that shown in Fig. 9(d).

Proof.

(a) Since this configuration corresponds to that shown in Fig. 7, it follows from Property 14 that

$$-E_{min} \leq v_0 \leq E_{max}, \text{ whenever } -E_{min} \leq v_{in} \leq E_{max} \tag{70}$$

$$-E_{min} \leq v_0 \leq v_{in}, \text{ whenever } v_{in} \geq E_{max} \tag{71}$$

$$v_{in} \leq v_0 \leq E_{max}, \text{ whenever } v_{in} \leq -E_{min} \tag{72}$$

The bounding region shown in Fig. 9(b) is precisely that defined by (70), (71), and (72).

(b) In this case $E_{min} = 0$ and the bounding region in Fig. 9(b) shrinks to that shown in Fig. 9(c).

(c) In this case $E_{max} = E_{min} = 0$ and the bounding region shrinks further to that shown in Fig. 9(d).

□

The TC plot bounding regions shown in Figs. 8 and 9 are the sharpest possible since in each case, it is possible to find one or more networks where TC plots contain points which approach the boundaries of each bounding region as closely as possible. However, by introducing additional assumptions, the bounding regions can be further reduced. For example, if the output voltage is taken from the collector of transistors -- as is usually the case for transistor circuits -- then the output voltage is further bounded by the maximum collector supply voltage and the bounding regions in Figs. 8 and 9 can be further sharpened accordingly.

We will now make use of the preceding results to derive bounding regions for DP plots.

Property 17. DP Plot Bounding Region for Ungrounded One-Ports

The DP plot of any connected resistive one-port containing only no-gain

multi-terminal resistors, dc voltage sources, and a positive linear resistor R in series with the driving-point terminals as shown in Fig. 10(a) must lie within the shaded region shown in Fig. 10(b).

Proof.

Since the resistor R is connected to the input voltage source, it follows from (b) of Property 15 that the v_R - vs. - v TC plot must lie within the shaded region shown in Fig. 8(c). Since $i = v_R/R$, the i - vs. - v DP plot must lie within the shaded region shown in Fig. 10(b). ¤

Property 17 has a number of interesting consequences. Among other things, it implies that whenever a resistor is in series with a resistive no-gain one-port, the overall DP plot cannot grow faster than a linear rate O(v) as $|v| \to \infty$, and cannot therefore be modeled by a polynomial with degree greater than one in the high operating voltage region. Since such a series resistor is invariably present in any realistic circuit model of high power devices (it is needed to account for the ohmic resistance of the connecting terminal and the devices bulk resistance), this observation actually suggests the use of piecewise-linear functions for modeling high power devices. Another important consequence of Property 17 can be derived by examining how the shaded area in Fig. 10(b) changes as we decrease the value of R. Notice that in the limit as $R \to 0$, we obtain the region shown in Fig. 10(c). Hence we have proved the following rather surprising general result:

Corollary 17.1

The DP plot of any connected resistive one-port N containing only no-gain multi-terminal resistors and dc voltage sources must lie within the shaded region shown in Fig. 10(c) and N is therefore eventually passive; i.e. N is passive whenever $|v| \geq E \triangleq \sum_{i=1}^{n} |E_i|$.

Property 18. DP Plot Bounding Region for Grounded One-Ports

The DP plot of any connected resistive grounded one-port containing only no-gain multi-terminal resistors and grounded dc voltage sources and a positive linear resistor R in series with the driving-point terminals as shown in Fig. 11(a) must lie within the shaded region shown in Fig. 11(b), where E_{max} and E_{min} denote respectively the maximum and the minimum node-to-ground terminal

voltage of the dc voltage sources.

Proof. Since the resistor R is connected to the input voltage source, Property 18 follows immediately from Fig. 8(f) of Property 15.

¤

Corollary 18.1

The DP plot of any connected resistive grounded one-port N containing only no-gain multi-terminal resistors and dc voltage sources must lie within the shaded region shown in Fig. 11(c) and N is therefore eventually passive; namely, whenever $v \geq E_{max} \geq 0$ or $v \leq -E_{min} \leq 0$.

We will conclude this section by deriving some bounds on the slopes of DP and TC plots of locally no-gain networks. Unlike the previous theorems, we now allow both voltage and current sources to be present simultaneously.

Property 19 Bounds for Slopes of DP and TC Plots of Locally No-Gain Networks

Let N be a connected resistive network containing only locally no-gain multi-terminal resistors and dc voltage and current sources. Then at any point Q where the DP or TC plot associated with N is differentiable, the respective slope at Q is bounded as follows:

(a) the slope of the DP plot across any pair of driving-point terminals of N is positive; i.e.,

$$\frac{di}{dv} > 0 \tag{73}$$

(b) the magnitude of the slope of the TC plot with respect to any pair of input and output terminals is bounded by unity; i.e.,

$$\left|\frac{dv_0}{dv_{in}}\right| \leq 1 \tag{74}$$

(c) In the case where the input and output terminals are grounded, the slope of the TC plot is always non-negative and less than unity; i.e.,

$$0 \leq \frac{dv_0}{dv_{in}} \leq 1 \tag{75}$$

Proof. Since this property is concerned only with incremental variables about an operating point Q, all internal dc voltage and current sources can be set

equal to zero and each multi-terminal resistor can be represented by an incremental representation

$$\delta \underset{\sim}{y} = \underset{\sim}{H} \quad \delta \underset{\sim}{x} \tag{76}$$

where $(\delta \underset{\sim}{y}, \delta \underset{\sim}{x})$ denote the associated incremental variables, and $\underset{\sim}{H}$ denotes the incremental matrix evaluated at the operating point Q. Since each multi-terminal resistor is locally no-gain by hypothesis, then for each admissible incremental signal pair $(\delta \underset{\sim}{y}, \delta \underset{\sim}{x})$ about Q for each n-terminal resistor $\mathcal{R}$, there exist n-1 linear positive resistors having the same admissible pair $(\delta \underset{\sim}{y}, \delta \underset{\sim}{x})$. Since the DP and TC plots are, by hypothesis, differentiable at Q, the slope of di/dv and dv_0/dv_{in} at Q is equal respectively to the input resistance and the voltage transfer ratio of the associated equivalent linear incremental network. Hence (73), (74), and (75) follow immediately from well-known results for linear resistive networks. ¤

Corollary 19.1

Every connected one-port containing only locally no-gain multi-terminal resistors and independent dc voltage and current sources is strictly locally passive.

Remark. This corollary is false for n-ports, when n > 1. Using the results from [18], however, we can prove the following:

Property 20 Strict-Local Passivity Criteria

Every connected n-port N containing only locally no-gain multi-terminal resistors and dc voltage and current sources is strictly locally passive if the external ports of N form neither loops, nor cutsets.

Property 21 Relationship between Slopes of DP and TC Plots of Loaded Two-Ports

Let N be a connected resistive two-port containing only locally no-gain multi-terminal resistors and dc voltage and current sources. Let N be terminated by a locally no-gain load resistor characterized by $i_L = g_L(v_L)$ as shown in Fig. 12. Let the DP and TC plots of the loaded two-port be represented respectively by $i = g(v)$ and $v_0 = v_0(v)$. Then the slope at each corresponding operating point must satisfy the following inequalities:

(a) $$\frac{dg(v)}{dv} > 0 \tag{77}$$

(b) $$\left|\frac{dv_0(v)}{dv}\right| \leq 1 \tag{78}$$

(c) $$\left|\frac{dv_0(v)}{dv}\right| \leq \frac{\frac{dg(v)}{dv}}{\left.\frac{dg_L(v_L)}{dv_L}\right|_{v_L=v_0(v)}} \tag{79}$$

Proof. The inequalities (77) and (78) follow directly from Property 19. To derive (79), we observe that the i_L - vs. - i TC plot must satisfy a dual inequality, namely

$$\left|\frac{di_L}{di}\right| \leq 1 \tag{80}$$

Together, (77) and (80) imply that

$$\left|\frac{di_L}{dv}\right| = \left|\frac{di_L}{di}\frac{di}{dv}\right| = \left|\frac{di_L}{di}\right| \cdot \frac{dg(v)}{dv} \leq \frac{dg(v)}{dv} \tag{81}$$

But

$$\left|\frac{di_L}{dv}\right| = \left|\frac{di_L}{dv_L} \cdot \frac{dv_L}{dv}\right| = \left|\frac{dg_L(v_L)}{dv_L}\right| \left|\frac{dv_0(v)}{dv}\right| \tag{82}$$

It follows from (81) and (82) that

$$\left|\frac{dv_0(v)}{dv}\right| = \frac{\left|\frac{di_L}{dv}\right|}{\frac{dg_L(v_L)}{dv_L}} \leq \frac{\frac{dg(v)}{dv}}{\frac{dg_L(v_L)}{dv_L}} \cdot$$

¤

Corollary 21.1

The magnitude of the slope of the TC plot of any locally no-gain two-port terminated by a linear positive load resistor R_L is bounded by

$$\left|\frac{dv_0(v)}{dv}\right| \leq \frac{R_L}{R_{in}} \tag{83}$$

where R_{in} denotes the smallest incremental resistance of the DP plot of the loaded two-port.

V. PROPERTIES OF NETWORKS EXHIBITING TOPOLOGICAL OR COMPLEMENTARY SYMMETRY

In addition to bounding regions, it is often useful to know whether a DP plot or TC plot exhibits some form of symmetry. For example, the differential amplifier circuit shown in Fig. 13(a) has an odd symmetric TC plot as shown in Fig. 13(b), while the full-wave rectifier circuit shown in Fig. 14(a) has an even symmetric TC plot as shown in Fig. 14(b). That these two TC plots must exhibit some form of symmetry is not surprising in view of the topological symmetry of the associated circuits -- the circuit inside N exhibits "mirror" symmetry about a horizontal axis of symmetry. What is surprising is that there exists a much larger class of circuits having no topological symmetry whatsoever but nevertheless are characterized by an odd symmetric TC plot. For example, the two-operational amplifier circuit shown in Fig. 15(a) has an odd symmetric TC plot as shown in Fig. 15(b) so long as the operational amplifier is represented by the resistive circuit model shown in Fig. 15(c). Observe that this circuit does not display any topological symmetry. However, as will be shown shortly, this circuit possesses a more general form of symmetry called complementary symmetry and our objective in this section is to define these two forms of symmetry precisely so that results of a more general nature may be derived.

Definition 8. Topological Symmetry

A network N is said to exhibit some form of topological symmetry if after subjecting N to a topological transformation $T(\cdot)$ such as a physical rotation or translation, we obtain a new network T(N) which, except possibly for the element labellings, is identical to N; i.e., N and T(N) have identical topology and the corresponding elements have identical constitutive relations. In particular, the class of topologically symmetric networks which exhibits a mirror symmetry with respect to a horizontal axis as shown in Fig. 16 will henceforth be referred to as horizontally symmetric networks.

It is important to observe that even though the "corresponding" elements of a horizontally symmetric network N and the rotated network T(N) are identical by definition, the current and voltage variables associated with these elements are generally distinct since they are associated with distinct elements. For example, element 4 of the network N in Fig. 16 would correspond to element 5

of the rotated network T(N). While they have identical v-i curves, by definition, their respective currents and voltages need bear no relation to each other. However, for those elements which remain in the same position after the rotation -- henceforth referred to as fixed elements -- the corresponding current and voltage variables of N and T(N) are related in a very simple way. For example, terminals ⓐ and ⓑ of element 1 and element 3 in Fig. 16 remain in the same position after rotation and hence i_a and v_{ab} of the corresponding elements in N and T(N) must be equal to each other. In contrast to this, terminals ⓐ - ⓑ of element 2 or terminals ⓔ - ⓕ of element 3 become interchanged after rotation and hence the corresponding voltages of N and T(N) must be the negative of each other. In the following, we will exploit these properties to ascertain the symmetry of DP and TC plots.

Property 22. DP plots of Horizontally-Symmetric Networks

The DP plot across any pair of symmetrically located driving-point terminals (not on the horizontal axis) of any horizontally symmetric resistive network is odd symmetric.

Proof. Let $f(v,i) = 0$ denote the DP plot of N. Since the driving-point terminals are symmetrically located, (v,i) of N corresponds to (-v,-i) of the rotated network T(N). Moreover, since N is horizontally symmetric, we must have $f(v,i) = f(-v,-i) = 0$. ¤

Property 23. TC Plots of Horizontally-Symmetric Networks

Let N be a horizontally symmetric network with a pair of symmetrically located driving-point terminals as shown in the four basic configurations in Fig. 17. Then we have:

(a) The v_0 - vs. - v_{in} TC plot of N is odd symmetric if v_0 is measured across a pair of symmetrically located terminals as shown in Fig. 17(a), and is even symmetric if v_0 is measured across a pair of terminals lying along the axis of symmetry as shown in Fig. 17(b).

(b) The i_0 - vs. - i_{in} TC plot of N is odd symmetric if i_0 is the current through a two-terminal element which intersects the axis of symmetry perpendicularly as shown in Fig. 17(c), and is even symmetric if i_0 is the current through a two-terminal element lying along the axis of symmetry as shown in Fig. 17(d).

Proof.

(a) Let v_j' denote any voltage of the rotated network T(N) corresponding to v_j of N. Since the input and output terminals in Fig. 17(a) are symmetrically located, we must have $v_{in}' = -v_{in}$ and $v_0' = -v_0$ and hence whenever (v_{in},v_0) is a point on the TC plot, then the horizontal symmetry of N implies that $(-v_{in},-v_0)$ is also a point on the TC plot. Hence, $f(v_{in},v_0) = f(-v_{in},-v_0) = 0$ and the TC plot is odd symmetric. In the case where the output terminals are located along the axis of symmetry, $v_0' = v_0$ remains invariant. Hence, we must have $f(v_{in},v_0) = f(-v_{in},v_0) = 0$ and the TC plot is even symmetric.

(b) The proof is similar to that given in (a) and is therefore omitted.

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The class of networks satisfying the hypotheses of Properties 22 and 23 represents only a rather small subset of networks having a symmetrical DP or TC plot. Let us therefore turn our attention to a more general form of symmetry which we now define:

Definition 9. Complementary Elements and Networks

Let $\mathcal{R}$ be an n-terminal resistor characterized by a relation $\underset{\sim}{f}(\underset{\sim}{v},\underset{\sim}{i}) = \underset{\sim}{0}$. We define a complementary resistor $\overline{\mathcal{R}}$ associated with $\mathcal{R}$ to be an n-terminal resistor characterized by $\overline{\underset{\sim}{f}}(\overline{\underset{\sim}{v}},\overline{\underset{\sim}{i}}) = \underset{\sim}{0}$ where

$$\overline{\underset{\sim}{f}}(\overline{\underset{\sim}{v}},\overline{\underset{\sim}{i}}) \triangleq \underset{\sim}{f}(-\overline{\underset{\sim}{v}},-\overline{\underset{\sim}{i}}) \tag{84}$$

and where $\bar{v}_j$ and $\bar{i}_j$ denote respectively the voltage and current (assuming the same set of reference direction and polarity as that of terminal j of $\mathcal{R}$) of terminal j of $\overline{\mathcal{R}}$. A network $\bar{N}$ obtained by replacing each element in N by its associated complementary element is called the complementary network associated with N.

There are many complementary elements of practical interest. For example, the complement of any two-terminal element is the same element but with its terminals interchanged. Hence, the complement of a pn junction diode is an np junction diode. The complement of a pnp transistor is an npn transistor having the same characteristic curves but rotated by 180° about the origin. While the two networks N and its complement $\bar{N}$ are generally distinct, the following theorem shows that their respective solutions are simply related.

Theorem 2. Complementary Network Theorem

If $(\underset{\sim}{V}_Q, \underset{\sim}{I}_Q)$ is the voltage and current distribution of a network N, then $(-\underset{\sim}{V}_Q, -\underset{\sim}{I}_Q)$ is the voltage and current distribution of the associated complementary network $\overline{N}$. In particular, any DP plot or TC plot of N is related to the corresponding DP plot or TC plot of $\overline{N}$ by a 180° rotation through the origin.

Proof. Since N and $\overline{N}$ have identical topology, and since the elements of N and $\overline{N}$ are complements of each other, the following complementary sets of network equations must hold:

	Network N	Complementary Network $\overline{N}$
KCL:	$\underset{\sim}{A}\ \underset{\sim}{I}_Q = \underset{\sim}{0}$	$\underset{\sim}{A}\ \overline{\underset{\sim}{I}}_Q = \underset{\sim}{0} \Rightarrow \underset{\sim}{A}(-\overline{\underset{\sim}{I}}_Q) = \underset{\sim}{0}$
KVL:	$\underset{\sim}{B}\ \underset{\sim}{V}_Q = \underset{\sim}{0}$	$\underset{\sim}{B}\overline{\underset{\sim}{V}}_Q = \underset{\sim}{0} \Rightarrow \underset{\sim}{B}(-\overline{\underset{\sim}{V}}_Q) = \underset{\sim}{0}$
Constitutive Relations:	$\underset{\sim}{f}(\underset{\sim}{V}_Q, \underset{\sim}{I}_Q) = \underset{\sim}{0}$	$\overline{\underset{\sim}{f}}(\overline{\underset{\sim}{V}}_Q, \overline{\underset{\sim}{I}}_Q) = \underset{\sim}{f}(-\overline{\underset{\sim}{V}}_Q, -\overline{\underset{\sim}{I}}_Q) = \underset{\sim}{0}$

where $\underset{\sim}{A}$ and $\underset{\sim}{B}$ denote the reduced-incidence matrix and the fundamental loop matrix, respectively, and where $\underset{\sim}{f}(\cdot,\cdot)$ and $\overline{\underset{\sim}{f}}(\cdot,\cdot)$ denote the collection of the constitutive relations of all elements of N and $\overline{N}$, respectively. Hence $(\underset{\sim}{V}_Q, \underset{\sim}{I}_Q)$ is a solution of N if, and only if, $(\overline{\underset{\sim}{V}}_Q, \overline{\underset{\sim}{I}}_Q)$ is a solution of $\overline{N}$.

Observe that Theorem 2 provides the rigorous basis for the common "ad hoc" rule in logic circuit design for transforming a "positive" diode-transistor logic circuit into a "negative" diode-transistor logic circuit by simply transposing the terminals of all batteries and diodes, and by replacing all pnp transistors by their complementary npn transistors.

Definition 10. Complementary Symmetry

An n-terminal element $\mathcal{R}$ is said to possess complementary symmetry if it is identical to its complement $\overline{\mathcal{R}}$. A network N is said to exhibit complementary symmetry if its complement $\overline{N}$ is identical to N.

Property 24. Complementary Symmetric Criteria

An n-terminal resistor $\mathcal{R}$ possesses complementary symmetry if, and only if, its constitutive relation is odd symmetric in the sense that

$$\underset{\sim}{f}(\underset{\sim}{v},\underset{\sim}{i}) = \underset{\sim}{0} \quad \text{if, and only if,} \quad \underset{\sim}{f}(-\underset{\sim}{v},-\underset{\sim}{i}) = \underset{\sim}{0} \tag{85}$$

Proof. By definition, $\overline{N}$ is the complement of N implies that $\underset{\sim}{f}(\underset{\sim}{v},\underset{\sim}{i}) = \underset{\sim}{0}$ if, and only if, $\overline{\underset{\sim}{f}}(-\overline{\underset{\sim}{v}},-\overline{\underset{\sim}{i}}) = \underset{\sim}{0}$. Hence (85) follows from the hypothesis that $\overline{N}$ and N are identical.

∎

Corollary 24.1

The following elements are complementary symmetric:

1. Any bilateral two-terminal resistor.

2. Any multi-terminal linear element characterized by $\underset{\sim}{f}(\underset{\sim}{v},\underset{\sim}{i}) = \underset{\sim}{A}\ \underset{\sim}{v} + \underset{\sim}{B}\ \underset{\sim}{i} = \underset{\sim}{0}$. This class includes all common linear elements such as gyrators, transformers, controlled sources, negative impedance converters, etc.

3. Any operational amplifier represented by the resistive circuit model shown in Fig. 15(c).

Property 25. Odd Symmetric DP and TC Plot

The DP plot and TC plot of any network containing only complementary symmetric elements are odd symmetric.

Proof. Follows directly from Theorem 2 and Property 24. ¤

As a direct consequence of Theorem 2 and Corollary 24.1, we have the following important special case of Property 25:

Corollary 25.1

The DP plot and TC plot are odd symmetric for any network containing operational amplifiers, gyrators, ideal transformers, controlled sources, negative impedance converters, linear resistors, and bilateral two-terminal nonlinear resistors; regardless of the network topology.

It is possible to further enlarge the class of networks having odd symmetric DP and TC plots by relaxing Definition 10 as follows:

Definition 11. Pseudo-Complementary Symmetry

A network N is said to exhibit pseudo-complementary symmetry if after subjecting portion of its complement $\overline{N}$ to some topological transformation $T(\cdot)$ such as rotation or translation, the transformed network $T(\overline{N})$ can be redrawn such that except possibly for the element labellings, the networks N and $T(\overline{N})$ are identical.

Examples of Networks exhibiting Pseudo-Complementary Symmetry:

1. The operational amplifier circuit considered earlier in Fig. 15(a) exhibits pseudo-complementary symmetry since its complement $\overline{N}$ is identical to N except

that the two terminals of each diode in $\overline{N}$ are interchanged. In this case we can simply redraw $\overline{N}$ to obtain the original circuit. Hence $T(\cdot)$ in this case is just the identity transformation.

2. The diode-clipping circuit shown in Fig. 18(a) is pseudo-complementary symmetric because its complement $\overline{N}$ in Fig. 18(b) can be redrawn so that $\overline{N}$ is identical to N. Again $T(\cdot)$ in this case is the identity transformation.

3. The push-pull transistor amplifier circuit shown in Fig. 19(a) is pseudo-complementary symmetric because its complement $\overline{N}$ shown in Fig. 19(b) can be rotated such that $T(\overline{N}) = N$. In this case, $T(\cdot)$ consists of a 180°-rotation of the entire circuit except the input voltage source.

4. The operational amplifier circuit shown in Fig. 20(a) is pseudo-complementary symmetric because if we rotate the portion of $\overline{N}$ in Fig. 20(b) consisting of the two diodes, the four resistors R_A, R_B, R'_A, and R'_B, and the two batteries by 180°, we obtain $T(\overline{N}) = N$.

It is important to observe that unlike Property 25, the DP plot and TC plot of a pseudo-complementary symmetric network are generally not symmetric because even though the networks $T(\overline{N})$ and N are identical, the corresponding voltages in N and $T(\overline{N})$ are generally not related to each other, as we have also pointed out earlier in the case of rotationally symmetric networks. However, if the output voltage is measured across a pair of terminals which either remain invariant (such as v_0 in Figs. 15(a), 18(a), and 20(a)) or which lies along the horizontal axis of rotation (such as v_0 in Fig. 19(a)), then the TC plot would remain odd symmetric. We will now formalize this observation as follows:

Theorem 3. Pseudo-Complementary Symmetric Network Theorem

Let N be a pseudo-complementary symmetric network and let its complement $\overline{N}$ be partitioned into two parts $\overline{N} = \overline{N}_1 \cup \overline{N}_2$ where $\overline{N}_1$ remains invariant under the topological transformation $T(\cdot)$; i.e., $T(\overline{N}) = \overline{N}_1 \cup T(\overline{N}_2)$, where $T(\overline{N}_2)$ denotes the rotated subnetwork of $\overline{N}_2$ as shown in Fig. 21. Let $\overline{v}_j$ and $\overline{i}_j$ denote the voltage and current of $T(\overline{N})$ corresponding to that of v_j and i_j in N. Then we have

(a) $\overline{v}_j = v_j$ and $\overline{i}_j = i_j$ whenever $(\overline{v}_j, \overline{i}_j)$ belongs to the invariant subnetwork $\overline{N}_1$.

(b) $\bar{v}_j = v_j$ and $\bar{i}_j = i_j$ whenever $(\bar{v}_j, \bar{i}_j)$ belongs to an element of $T(\bar{N}_2)$ which lies along the axis of rotation.

(c) $\bar{v}_k = -v_k$ and $\bar{i}_k = -i_k$ whenever $(\bar{v}_k, \bar{i}_k)$ belongs to an element of $T(\bar{N}_2)$ which intersects the axis of rotation perpendicularly..

(d) $\bar{v}_\ell = -v_\ell$ whenever $\bar{v}_\ell$ pertains to a pair of nodes of $T(\bar{N}_2)$ which are symmetrically located with respect to the axis of rotation.

Proof. The proof is similar to that used in proving Property 23 and is therefore omitted. ¤

Property 26. DP and TC Plots of Pseudo-Complementary Symmetric Networks

Let N be a pseudo-complementary symmetric network and let $T(\bar{N}) = \bar{N}_1 \cup T(\bar{N}_2)$ as shown in Fig. 21. Then we have:

(a) The DP plot across any pair of driving-point terminals located in N_1 is odd symmetric.

(b) The v_0 - vs. - v_{in} TC plot is odd symmetric whenever the driving-point terminals belong to $\bar{N}_1$, and whenever the output voltage v_0 is measured either across a pair of nodes belonging to N_1 or across a "fixed" element of $T(\bar{N}_2)$ lying along the axis of rotation.

Proof. Follows directly from Theorem 3. ¤

It follows from Property 26 that the v_0 - vs. - v_{in} TC plots of the circuits shown in Figs. 15(a), 18(a), 19(a), and 20(a) are all odd symmetric.

VI. CONCLUDING REMARKS

The objective of this research was to achieve practical design criteria on the qualitative behaviour of nonlinear resistive networks that contain multi-terminal resistors. The results presented in this paper are concerned with the bounding regions and symmetrical properties of the TC and DP plots of resistive networks. Most of these results are applicable to networks that contain operational amplifiers, which are considered throughout as multi-terminal resistors.

One of the main results given in this paper, the generalization of the no-gain criteria to include multi-terminal elements, allowed this very basic

concept to be extended to include a large number of practical devices. In particular, bounding regions for the TC plots and DP plots of networks using operational amplifiers -- the most practical and widely used multi-terminal element -- were obtained for a large number of very general circuit configurations. The tightest possible bounding regions were obtained for the class of networks considered.

In addition to the generalization of the no-gain criteria a general characterization for grounded n-terminal no-gain elements is given in Corollaries 7.1 and 8.1. This characterization is mainly of theoretical interest, except in the case of a three- or four-terminal element, where it leads to a simple interpretation of graphical characteristics -- the type often given by device manufacturers. When these general characterizations were applied to an incremental matrix representation of the device's constitutive relation about an operating point, a locally no-gain concept emerged which led to several interesting properties related to the yet unsolved classical resistance n-port synthesis problem. In the restricted case where the locally no-gain incremental conductance and resistance matrices are symmetric (reciprocal), the conditions placed on the matrices should be similar to the conditions required for a general resistance network synthesis. In the former case these conditions were shown to be more stringent than the necessary and sufficient conditions for the realization of a grounded resistive network described by a conductance matrix. This difference was shown to be a result of the connection requirements placed on the locally no-gain network.

The incremental resistance case is much more difficult -- the necessary and sufficient conditions for the inverse of a resistance type matrix to be realizable as a conductance matrix remains an unsolved problem even for the more restricted case where the conductance matrix is hyperdominant. Several of the conditions listed in Property 10 appear to be new. They can, by means of specific examples, be shown to be necessary for the inverse to be a hyperdominant conductance matrix. It should be noted that most of these conditions do not come into play for a three-terminal element but only for higher order systems. As the order of the system is increased more conditions become necessary, thus making the generalization difficult and as yet unsolved.

The concept of symmetric and complementary symmetric networks was defined and used to show that various classes of networks exhibit either even or odd symmetric TC and DP plots. These plots for many operational amplifier circuits

were shown to have odd symmetry. The symmetric properties and bounding regions of TC and DP plots of resistive networks are two of the main qualitative properties.

With respect to the no-gain property several problems reamin unsolved. These include, generalizing the local no-gain property to include a hybrid representation; specifying all of the necessary and sufficient conditions for the inverse of a locally no-gain resistance matrix to be a locally no-gain conductance matrix. The conditions for the local no-gain property to hold were shown to be extemely restrictive. This observation seems to suggest that the more terminals there are in a multi-terminal device, the more likely that it is capable of small-signal amplification.

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APPENDIX

A-1. Proof of Lemma 2

(a) Consider the no-gain n-terminal resistor $\mathcal{R}$ shown in Fig. A-1, where the terminals have been relabelled such that the operating-point voltages satisfy the strict inequality of (21). To prove that the system of strict inequalities in (22) follows from that of (21), let us suppose the contrary. That is, suppose all inequalities in (22) are satisfied except the kth one which is replaced by

$$i_k \triangleq I_{(1)} + I_{(2)} + \cdots + I_{(k)} \leq 0 \tag{A-1}$$

Now suppose we connect a linear resistor with a resistance value

$$R_k \triangleq \frac{V_{(k)} - V_{(k+1)}}{-i_k} > 0 \quad \text{if } i_k < 0 \tag{A-2}$$

$$= \infty \qquad \text{if } i_k = 0$$

from node (k+1) to node (k), and connect n-2 independent current sources across the remaining nodes with values as indicated in Fig. A-1. Applying KCL at each terminal of $\mathcal{R}$ shows that the resulting current entering each terminal (j) is precisely equal to the operating-point current $I_{(j)}$. Hence, the terminal voltages of $\mathcal{R}$ must necessarily distribute themselves so that they too agree with the associated operating-point voltages.

Now, observe that the sum of the magnitudes of the voltages across the n-2 independent current sources is given by

$$\sum_{j=1}^{n-2} \left| v_{s_j} \right| = (V_{(1)} - V_{(2)}) + (V_{(2)} - V_{(3)}) + \cdots + (V_{(k-1)} - V_{(k)})$$

$$+ (V_{(k+1)} - V_{(k+2)}) + \cdots + (V_{(n-2)} - V_{(n-1)}) + V_{(n-1)}$$

$$= V_{(1)} - (V_{(k)} - V_{(k+1)}) < V_{(1)} \tag{A-3}$$

Note that Eq. (A-3) violates the no-gain property since the voltage across node (1) and node (n) is equal to $V_{(1)}$. Hence (A-1) can not be true. The same procedure can be applied, *mutatis mutandis*, to the case where two or more strict

inequalities in (22) are violated. In each case, we can obtain a contradiction and hence Lemma 2(a) is proved.

(b) To prove that the system of mixed inequalities of (24) must necessarily follow the mixed inequalities of (23), let us suppose the contrary and assume that all mixed inequalities of (24) are true except one. If one of the strict inequality equation in (24) is violated, we can use the procedure in the proof of part (a) of this lemma to arrive at a contradiction. Hence, all strict inequalities in (24) must hold.

Suppose now (24e) is violated, i.e. assuming

$$I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k-1)} < 0 \tag{A-4}$$

Let us connect n-2 linear resistors, a short circuit element and an independent current source with $\mathcal{R}$ as shown in Fig. A-2. If we choose I_s such that

$$I_s > \left|I_{(1)}\right| + \left|I_{(2)}\right| + \cdots + \left|I_{(n-1)}\right| \tag{A-5}$$

Then the linear resistors will all have positive resistance values. From Fig. A-2, the current flowing through the short circuit element is given by

$$i_k \triangleq I_s - (I_{(1)} + I_{(2)} + \cdots + I_{(k-1)}) \tag{A-6}$$

From (A-4) and (A-6), we obtain

$$i_k > I_s$$

which is impossible because this would mean the network in Fig. A-2 is not a no-gain network, thereby implying that $\mathcal{R}$ is not a no-gain resistor -- contrary to our assumption. Hence, (24e) must hold. Similary (24f) also must hold. Hence, Lemma 2(b) is proved. ¤

A-2. Proof of Lemma 3

Consider first the case when the strict inequalities of (21) and (22) hold. Observe that we can always construct the connected network shown in Fig. A-3 (containing n-1 positive linear two-terminal resistors) having an identical operating-point voltages and currents, where the resistors have

resistance values given by

$$R_1 = \frac{V_{(1)} - V_{(2)}}{I_{(1)}} > 0 \qquad \text{(A-7a)}$$

$$R_2 = \frac{V_{(2)} - V_{(3)}}{I_{(1)} + I_{(2)}} > 0 \qquad \text{(A-7b)}$$

$$\vdots$$

$$R_k = \frac{V_{(k)} - V_{(k+1)}}{I_{(1)} + I_{(2)} + \cdots + I_{(k)}} > 0 \qquad \text{(A-7c)}$$

$$\vdots$$

$$R_{n-2} = \frac{V_{(n-2)} - V_{(n-1)}}{I_{(1)} + I_{(2)} + \cdots + I_{(n-2)}} > 0 \qquad \text{(A-7d)}$$

$$R_{n-1} = \frac{V_{(n-1)}}{I_{(1)} + I_{(2)} + \cdots + I_{(n-1)}} > 0 \qquad \text{(A-7e)}$$

Next, let us consider the mixed inequality case of (23) and (24). Observe that (24d) implies that the equality sign in (24e) and (24f) can not hold simultaneously. Hence, without loss of generality, let us assume that (24f) is satisfied with a strict inequality. Under this assumption, there are four exhaustive possibilities.

Case 1: $$I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k-1)} = 0 \text{ and } I_{(k)} > 0 \qquad \text{(A-8)}$$

In this case, the same network shown in Fig. A-3 can be used to realize the desired operating-point, where all resistors except R_{k-2}, R_{k-1} and R_k are specified by (A-7) and where

$$R_{k-2} = \frac{V_{(k-2)} - V_{(k-1)}}{I_{(1)} + I_{(2)} + \cdots + I_{(k-2)}} > 0 \qquad \text{(A-9a)}$$

$$R_{k-1} = 1\Omega > 0 \qquad \text{(A-9b)}$$

$$R_k = \frac{V_{(k)} - V_{(k+1)}}{I_{(k)}} > 0 \qquad \text{(A-9c)}$$

Case 2: $$I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k-1)} > 0 \text{ and } I_{(k)} = 0 \qquad \text{(A-10)}$$

In this case, the network shown in Fig. A-4 can be used to realize the desired operating-point, where all resistors except R_{k-1} are specified by (A-7). Observe that R_{k-1} may be set equal to any positive value since $I_{(k)} = 0$. This resistor is used here merely to ensure the network is connected.

Case 3: $$I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k-1)} > 0 \text{ and } I_{(k)} < 0 \qquad \text{(A-11)}$$

In this case, the network shown in Fig. A-5 can be used to realize the desired operating-point, where all resistors except R_{k-2}, R_{k-1}, and R_k are specified by (A-7) and

$$R_{k-2} = \frac{V_{(k-2)} - V_{(k-1)}}{I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k)}} > 0 \qquad \text{(A-12a)}$$

$$R_{k-1} = \frac{V_{(k-2)} - V_{(k)}}{-I_{(k)}} > 0 \qquad \text{(A-12b)}$$

$$R_k = \frac{V_{(k-1)} - V_{(k+1)}}{I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k-1)} + I_{(k)}} > 0 \qquad \text{(A-12c)}$$

Case 4: $$I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k-1)} > 0 \text{ and } I_{(k)} > 0 \qquad \text{(A-13)}$$

In this case, the network shown in Fig. A-6 can be used to realize the desired operating point provided R_{k-1} and R_k are specified by

$$R_{k-1} = \frac{V_{(k-1)} - V_{(k+1)}}{I_{(1)} + I_{(2)} + \cdots + I_{(k-2)} + I_{(k-1)}} > 0 \qquad \text{(A-14a)}$$

$$R_k = \frac{V_{(k)} - V_{(k+1)}}{I_k} > 0 \qquad \text{(A-14b)}$$

and the remaining resistors are given by the same formulas as in (A-7).

This completes the proof of Lemma 3. ¤

A-3. Proof of Property 8

A. Sufficiency: Let $\mathcal{R}$ be imbedded in any connected network N containing only positive linear two-terminal resistors, short and open circuit elements which do not form $\mathcal{S}$-loops and $\mathcal{O}$-cutsets, respectively, and nonzero independent voltage and current sources. Let $\hat{Q}$ be an operating point of the network and Q the corresponding operating point of $\mathcal{R}$ which satisfies the conditions of Property 8. We will show that a Network N_Q containing (n-1) positive linear two-terminal resistors can be constructed which has the same operating point as $\mathcal{R}$. With N_Q replacing $\mathcal{R}$ in N the same operating point $\hat{Q}$ will be maintained. Since N_Q possesses the no-gain property it follows that $\mathcal{R}$ also possesses the no-gain property. Hence, the construction of N_Q establishes that $\mathcal{R}$ possesses the no-gain property.

The construction procedure is carried out by assuming an operating point exists that satisfies conditions (1a), (1c) and (2) of Property 8. With condition (1a) terminals ⓚ and ⓙ exist such that $I_k > 0$ {resp; = 0}, $I_j < 0$, $I_m \geq 0$ for $m = 1,2,\ldots,n-1$ with $m \neq k$ and $m \neq j$. With this assumption, and terminal ⓙ taken as reference, all terminal to reference voltages are non-negative . These terminals with the exception of ⓙ can be partioned into four sets S_1, S_2, S_3 and S_4. The set $S_1 = \{\alpha_1\}$ is a terminal at the maximum potential with a positive current i.e. $I_{\alpha_1} > 0$. Condition (2) of Property 8 guarantees that such a terminal exists. The set $S_2 = \{\alpha_2,\alpha_3,\ldots,\alpha_\ell\}$ is defined as the set of remaining terminals with positive terminal currents, i.e., $I_{\alpha_p} > 0$ for $p = 2,3,\ldots,\ell$ with $1 < \ell \leq n-1$. The set $S_3 = \{\alpha_{\ell+1},\alpha_{\ell+2},\ldots,\alpha_{\ell+q}\}$ is defined as the set of terminals with zero terminal current and zero terminal-to-reference voltage, i.e., $V_{\alpha_{\ell+p}} - V_j = 0$ and $I_{\alpha_{\ell+p}} = 0$ for $p = 1,2,\ldots,g$ with $\ell+1 < q \leq n-1$. The remaining terminals $S_4 = \{\alpha_{\ell+q+1},\alpha_{\ell+q+2},\ldots,\alpha_{n-1}\}$ are those terminals with positive terminal-to-reference voltage and zero terminal current, i.e., $V_{\alpha_p} - V_j > 0$ and $I_{\alpha_p} = 0$ for $p = \ell+q+1,\ell+q+2,\ldots,n-1$.

Figure A-7(a) is a realization of N_Q. For the terminals belonging to S_2, the resistors are specified as

$$R_{\alpha_p} = \frac{V_{\alpha_p} - V_j}{I_{\alpha_p}} \qquad p = 2,3,\ldots,\ell \qquad \text{(A-15)}$$

For terminals belong to S_3 the resistors are specified by

$$R_{\alpha_p} = 1\Omega \qquad p = \ell+1, \ell+2, \ldots, \ell+q \tag{A-16}$$

The terminals corresponding to S_1 and S_4 are considered together. Without loss of generality we can assume

$$V_{\alpha_1} \geq V_{\alpha_{\ell+q+1}} \geq V_{\alpha_{\ell+q+2}} \geq \ldots \geq V_{n-1} > V_j \tag{A-17}$$

If all the strict inequality signs in (A-17) hold, the network of Fig. A-7(a) realizes N_Q with

$$R_{\alpha_1} = \frac{V_{\alpha_1} - V_{\alpha_{\ell+q+1}}}{I_{\alpha_1}} \tag{A-18}$$

$$R_{\alpha_p} = \frac{V_{\alpha_p} - V_{\alpha_{p+1}}}{I_{\alpha_1}} \qquad p = \ell+q+1, \ell+q+2, \ldots, n-2 \tag{A-19a}$$

$$R_{\alpha_{n-1}} = \frac{V_{n-1} - V_j}{I_{\alpha_1}} \tag{A-19b}$$

When one of the equality signs in (A-17) holds, for example,

$$V_{\alpha_1} > V_{\alpha_{\ell+q+1}} = V_{\alpha_{\ell+q+2}} > \ldots > V_{n-1} > V_j \tag{A-20}$$

then the portion of the network N_Q involving the terminals associated with S_1 and S_4 can be realized, as shown in Fig. A-7(b) with

$$R_{\alpha_1} = \frac{V_{\alpha_1} - V_{\alpha_{\ell+q+1}}}{I_{\alpha_1}} \tag{A-21a}$$

$$R_{\alpha_{\ell+q+1}} = 1\Omega \tag{A-21b}$$

$$R_{\alpha_p} = \frac{V_{\alpha_p} - V_{\alpha_{p+1}}}{I_{\alpha_1}} \qquad p = \ell+q+2, \ell+q+3, \ldots, n-2 \tag{A-21c}$$

$$R_{\alpha_{n-1}} = \frac{V_{n-1} - V_j}{I_{\alpha_1}} \tag{A-21d}$$

In case other terms are equal in (A-17) a similar construction procedure can be used.

If an operating point exists that satisfies one of the other possible conditions of (1a) or (1b) in Property 8 a similar construction procedure will realize a network N_Q with the desired operating point. This then completes the sufficiency part of the proof.

B. Necessity: The necessity of conditions (1c) and (2) of Property 8 are obvious. In order to consider the necessity of condition (1a), let us assume that all terminal currents are non-negative except for terminal ⓙ, which is assumed to have negative current, i.e. current flowing away from the element $\mathcal{R}$. With terminal ⓙ taken as the reference terminal in order to satisfy condition (1a) of Property 8 all the other terminal to reference voltages must be non-negative. Suppose this condition is violated for some terminal ⓚ, that is assume an operating point for $\mathcal{R}$ exists where $V_k - V_j \leq 0$ {resp.; < 0} with $I_k > 0$ {resp.; = 0}, $I_j < 0$ and $I_m \geq 0$ for all m = 1,2,...,n with m≠k and m≠j. With this assumption we can arrange the remaining terminals $\{\alpha_1, \alpha_2, \ldots, \alpha_{n-2}\}$ so that the terminal voltages satisfy the following inequalities.

$$V_{\alpha_1} \geq V_{\alpha_2} \geq V_{\alpha_3} \geq \cdots V_{\alpha_{n-2}} \geq V_j \tag{A-22}$$

If $I_k > 0$ and $V_k - V_j < 0$, then the network of Fig. A-8 has the required operating point but does not possess the no-gain property. This is because the current through the short circuit element shown is given by

$$I_A = I_K + I_s > I_s \tag{A-23}$$

which is greater than the source current I_s, and therefore violates the no gain property. If $V_k - V_j = 0$ then with R a short circuit the same network still violates the no-gain property.

If $I_K = 0$ and $V_k - V_j < 0$ then, with R replaced by an open circuit, the voltage

$$V_{\alpha_1} - V_K > V_{\alpha_1} = V_s \qquad \text{(A-24)}$$

exceeds the source V_s, and the network again violates the no-gain property.

We have assumed that a single terminal voltage violates condition (1a) of Property 9 and we have shown that the resulting operating-point violates the no-gain property. If more than one terminal voltage violates condition (1a) of Property 9 the same method of proof can be used to show that the resulting operating-point does not satisfy the no-gain criteria. The remaining conditions of (1a) and (1b) can be shown to be necessary in a similar manner. ¤

A-4. Proof of Property 9

We will prove Property 9 using Property 7 and Corollary 7.1, where i_k is replaced by δi_k, v_k is replaced by δv_k and (32) is replaced by

$$\delta i_k = g_k(\delta \underline{v}) \triangleq \sum_{j=1}^{n-1} g_{kj}\, \delta v_j \qquad \text{for } k = 1,2,\ldots,n-1 \qquad \text{(A-25)}$$

A. Necessity. By selecting a particular $\delta \underline{v}$ for (A-25) the 5 conditions listed in Property 9 can be shown to be necessary

(i) By letting $\delta v_k > 0$ and $\delta v_\ell = 0$ for $\ell = 1,2,\ldots,n-1$ where $\ell \neq k$, (A-25) becomes

$$\delta i_k = g_{kk}\, \delta v_k \qquad \text{(A-26)}$$

To satisfy condition (1a) of Corollary 7.1, we require $g_{kk} > 0$. Clearly this is true for $k = 1,2,\ldots,n-1$ making condition (1) of Property 7 a necessary condition.

(ii) With $\delta v_j < 0$ and $\delta v_\ell = 0$ for $\ell = 1,2,\ldots,n-1$ where $\ell \neq j$, (A-25) becomes

$$\delta i_k = g_{kj}\, \delta v_j \qquad \text{(A-27)}$$

To satisfy condition (1a) of Corollary 7.1, we require $g_{kj} \leq 0$. Since this is true for all $k,j = 1,2,\ldots,n-1$ where $k \neq j$, condition (2) of Property 9 is a necessary condition.

(iii) Next, by letting $\delta v_1 = \delta v_2 = \ldots = \delta v_{n-1} \triangleq \alpha > 0$, (A-25) becomes

$$\delta i_k = \alpha \sum_{j=1}^{n-1} g_{kj} \qquad \text{(A-28)}$$

To satisfy condition (1a) of Corollary 7.1 we require

$$\sum_{j=1}^{n-1} g_{kj} \geq 0$$

implying

$$g_{kk} \geq - \sum_{\substack{j=1 \\ j\neq k}}^{n-1} g_{kj} \geq 0 \tag{A-29}$$

Hence, we have shown that condition (3) is necessary.

(iv) By summing all the n-1 equations in (A-25), we obtain

$$\sum_{k=1}^{n-1} \delta i_k = \sum_{k=1}^{n-1} \left(\sum_{j=1}^{n-1} g_{kj} \, \delta v_j \right) = \sum_{j=1}^{n-1} \left(\sum_{k=1}^{n-1} g_{kj} \right) \delta v_j \tag{A-30}$$

If we now let $\delta v_j > 0$, and $\delta v_\ell = 0$ for $\ell = 1,2,\ldots,n-1$ and $\ell \neq j$, (A-30) reduces to

$$\sum_{k=1}^{n-1} \delta i_k = \left(\sum_{k=1}^{n-1} g_{kj} \right) \delta v_j \tag{A-31}$$

To satisfy condition ((n-1)a) of Corollary 7.1 we need

$$\sum_{k=1}^{n-1} g_{kj} \geq 0$$

or

$$g_{jj} \geq - \sum_{\substack{k=1 \\ k\neq j}}^{n-1} g_{jk} \geq 0 \tag{A-32}$$

This proves condition (4) of Property 9.

(v) Finally, let us consider the sum of any p equations in (A-25) as

$$\sum_{k=1}^{p} \delta i_{\alpha_k} = \sum_{j=1}^{n-1} \left(\sum_{k=1}^{p} g_{\alpha_k j} \right) \delta v_j \tag{A-33}$$

If we now let $\delta v_{\alpha_1} = \delta v_{\alpha_2} = \ldots = \delta v_{\alpha_p} = \alpha > 0$ and let all other components of $\delta \underset{\sim}{v}$ be zero, then (A-33) becomes

$$\sum_{k=1}^{p} \delta i_{\alpha_k} = \left[\sum_{j=1}^{p}\sum_{k=1}^{p} g_{\alpha_k \alpha_j}\right]\alpha \qquad \text{(A-34)}$$

To satisfy condition (pa) of Corollary 7.1, p = 1,2,...,(n-1), we require that

$$\sum_{j=1}^{p}\sum_{k=1}^{p} g_{\alpha_k \alpha_j} > 0 \qquad p = 1,2,\ldots,(n-1) \qquad \text{(A-35)}$$

This proves the necessity of Condition (5) Property 9.

B. Sufficiency: To show that Conditions (1) through (5) form a set of sufficient conditions for $\mathcal{R}$ to be locally no-gain, let us partition the set of integers $\{1,2,\ldots,n-1\}$ into two sets; namely, $S_1 = \{\alpha_1,\alpha_2,\ldots,\alpha_\ell\}$ and $S_2 = \{\beta_1,\beta_2,\ldots,\beta_m\}$, where $\ell+m = n-1$, $S_1 \cup S_2 = \{1,2,\ldots,n-1\}$ and $S_1 \cap S_2 =$ empty set. Consider the sum of the p equations in (A-25) corresponding to a subset of the indices in S_1, where $p = 1,2,\ldots,\ell$:

$$\sum_{k=1}^{p} \delta i_{\alpha_k} = \sum_{j=1}^{n-1}\left(\sum_{k=1}^{p} g_{\alpha_k j}\right)\delta v_j$$

$$= \sum_{j=1}^{\ell}\left(\sum_{k=1}^{p} g_{\alpha_k \alpha_j}\right)\delta v_{\alpha_j} + \sum_{j=1}^{m}\left(\sum_{k=1}^{p} g_{\alpha_k \beta_j}\right)\delta v_{\beta_j} \qquad \text{(A-36)}$$

If we let $\delta\underset{\sim}{v}$ satisfy

$$\delta v_{\alpha_1} > \delta v_{\alpha_2} > \ldots > \delta v_{\alpha_\ell} > 0 > \delta v_{\beta_1} > \ldots > \delta v_{\beta_m} \qquad \text{(A-37)}$$

Then Conditions (1) through (5) imply that (A-36) gives

$$\sum_{k=1}^{p} \delta i_{\alpha_k} > 0 \qquad \text{for } p = 1,2,\ldots,\ell \qquad \text{(A-38)}$$

In addition, if we let $\delta\underset{\sim}{v}$ satisfy

$$\delta v_{\alpha_1} > \delta v_{\alpha_2} > \ldots > \delta v_{\alpha_k} = \delta v_{\alpha_{k+1}} > \ldots > \delta v_{\alpha_\ell} > 0 > \delta v_{\beta_1} > \ldots > \delta v_{\beta_m} \qquad \text{(A-39)}$$

Then condition (1) through (5) imply that (A-36) gives

$$\sum_{j=1}^{p} \delta i_{\alpha_j} > 0 \qquad \text{for } p = 1,2,\ldots,k-1,\ k+1,\ \ldots,\ \ell \tag{A-40a}$$

$$\sum_{j=1}^{k} \delta i_{\alpha_j} \geq 0 \text{ and } \sum_{\substack{j=1 \\ j\neq k}}^{k+1} \delta i_{\alpha_j} \geq 0 \tag{A-40b}$$

By Lemma 3, (A-37) through (A-40) imply that we can construct an n-terminal network containing n-1 positive linear two-terminal resistors having the operating-point voltage $\delta\underset{\sim}{v}$ and current $\delta\underset{\sim}{i}$. Hence $\mathcal{R}$ is locally no-gain. This completes the proof of Property 9. ¤

A-5. Proof of Property 10

We will prove Property 10 using Property 8 and Corollary 8.1 with i_k replaced by δi_k, v_k replaced by δv_k and (36) replaced by

$$\delta v_k = \sum_{j=1}^{n-1} r_{kj}\ \delta i_j \quad \text{for } k = 1,2,\ldots,n-1 \tag{A-41}$$

Each of the 7 conditions listed in Property 10 can be shown to be necessary. We will select specific $\delta\underset{\sim}{i}$ for each condition to be considered.

(i) By letting $\delta i_k > 0$ and $\delta i_m = 0$ for all $m = 1,2,\ldots,n-1$ where $m \neq k$, (A-41) becomes

$$\delta v_k = r_{kk}\ \delta i_k \tag{A-42a}$$

To satisfy condition (2a) of Corollary 8.1 will require that $r_{kk} > 0$ for all $k = 1,2,\ldots,n-1$, hence condition (1) of Property 10 is necessary.

(ii) By letting $\delta i_j > 0$ and $\delta i_m = 0$ for all $m = 1,2,\ldots,n-1$ where $m \neq j$, (A-41) becomes

$$\delta v_k = r_{kj}\ \delta i_j \tag{A-42b}$$

In order to satisfy condition (2a) of Corollary 8.1, we require that $r_{kj} \geq 0$ for all $k,j = 1,2,\ldots,n-1$ where $k \neq j$. With $-\delta i_j = \delta i_k > 0$ and $\delta i_m = 0$ for all $m = 1,2,\ldots,n$ where $m \neq k$ and $m \neq j$; $j,k = 1,2,\ldots,n$ where $j \neq k$ (A-41) becomes

$$\delta v_k = r_{kk}\ \delta i_k - r_{kj}\ \delta i_k \tag{A-42c}$$

In order to satisfy condition (2a) of Corollary 8.1 we require that $r_{kk} - r_{kj} \geq 0$. Since this is true for all k,j = 1,2,...,n where $k \neq j$, this constraint, coupled with the constraint that $r_{kj} \geq 0$, makes (2) of Property 10 necessary.

(iii) By letting $\delta i_k > 0$ and $\delta i_m = 0$ for all m = 1,2,...,n-1 where $m \neq k$, (A-41) gives

$$\delta v_k - \delta v_j = (r_{kk} - r_{jk})\delta i_k \qquad \text{(A-43a)}$$

In order to satisfy condition (1a) of Corollary 8.1 we require that $r_{kk} - r_{jk} \geq 0$ for all j,k = 1,2,...,n-1 where $k \neq 1$. This constraint and the requirement that $r_{jk} \geq 0$ imply that condition (3) of Property 10 is necessary.

(iv) With $\delta i_k = -\delta i_j > 0$ and $\delta i_m = 0$ for all m = 1,2,...,n-1 where $m \neq k$ and $m \neq j$; j,k = 1,2,...,n-1 where $j \neq k$; then (A-41) gives

$$\delta v_k - \delta v_j = (r_{kk} - r_{kj})\delta i_k + (r_{jj} - r_{jk})\delta i_k \qquad \text{(A-43b)}$$

Condidtion (1a) of Corollary 8.1 requires that $r_{kk} + r_{jj} > r_{jk} + r_{kj}$. Since this must be true for all j,k where $j \neq k$ condition (4) of Property 10 is a necessary condition.

(v) By letting $\delta i_k = -\delta i_\ell > 0$, $\delta i_m = 0$ for all m = 1,2,...,n-1 where $m \neq \ell$ and $m \neq k$; ℓ,k = 1,2,...,n-1 where $\ell \neq k$; (A-41) gives

$$\delta v_k - \delta v_j = (r_{kk} - r_{k\ell})\,\delta i_k - (r_{jk} - r_{j\ell})\,\delta i_k \qquad \text{(A-43c)}$$

In order to satisfy condition (1a) of Corollary 8.1, it is required that $r_{kk} + r_{j\ell} \geq r_{k\ell} + r_{jk}$. Since this must hold for all j,k, ℓ where $j \neq k \neq \ell$ Condition (5) of Property 10 is required.

(vi) Assuming $r_{k\ell} > 0$ and by letting $\delta i_k > 0$, $\delta i_\ell = -\dfrac{r_{kk}}{r_{k\ell}}\,\delta i_k$ and $\delta i_m = 0$ for all m = 1,2,...,n-1 where $m \neq \ell$ and $m \neq k$, ℓ,k = 1,2,...,n where $k \neq \ell$, (A-41) gives

$$\delta v_k = r_{kk}\,\delta i_k - r_{k\ell}\left(\frac{r_{kk}}{r_{k\ell}}\right)\delta i_k = 0 \qquad \text{(A-43d)}$$

and

$$\delta v_j = r_{jk}\,\delta i_k - r_{j\ell}\left(\frac{r_{kk}}{r_{k\ell}}\right)\delta i_k \qquad \text{(A-43e)}$$

where j = 1,2,...,n-1 with $j \neq k$ and $j \neq \ell$. In order to satisfy condition (3) of Corollary 8.1, (A-43e) must be non-positive or $r_{kk}\, r_{j\ell} \geq r_{jk}\, r_{k\ell}$. If $r_{k\ell} = 0$, this condition is automatically satisfied. This inequality must hold for all j,k,ℓ hence Condition (6) of Property 10 is a necessary condition.

(vii) Consider a set $S_1 = \{\alpha_1, \alpha_2, \ldots, \alpha_\ell\}$ with $\ell < n-1$, $\alpha_i \neq \alpha_j$ if $i \neq j$ and $\alpha_i \in \{1,2,\ldots,n\}$ for $i = 1,2,\ldots,\ell$. Suppose for some $j \notin S_1$ that

$$\sum_{i=1}^{\ell} r_{j\alpha_i} > \max_{i=1,2,\ldots,\ell} \left\{ \sum_{j=1}^{\ell} r_{\alpha_i \alpha_j} \right\} \tag{A-44a}$$

then with $\delta i_1 = \delta i_2 = \ldots = \delta i_\ell = \alpha > 0$, and with all other incremental currents set to zero, the voltage

$$\delta v_j > \max_{i=1,2,\ldots,\ell} \delta v_{\alpha_i} \tag{A-44b}$$

This contradicts condition (3) of Corollary 8.1. Hence condition (7) of Property 10 is necessary. ■

A-6. Proof of Lemma 6

(a) To prove that the inequalities of (48) follows from that of (47), let us suppose the contrary; i.e., assuming all inequalities in (47) hold except one, say

$$I_{(1)} + I_{(2)} + \ldots + I_{(k)} < 0 \tag{A-45}$$

Consider the network in Fig. A-9 where $\mathcal{R}$ is imbedded in a network containing positive linear two-terminal resistors and an independent current sources I_s satisfying

$$I_s \geq \sum_{j=1}^{n-1} |I_{(j)}| \tag{A-46}$$

Observe that the current i_k through R_k is given by

$$i_k = I_s - [I_{(1)} + I_{(2)} + \ldots + I_{(k)}] \tag{A-47}$$

Equations (A-46) and (A-47) imply that $i_k > I_s$ which says that the network in Fig. A-9 is not a no-gain network. This contradicts the fact that $\mathcal{R}$ is a weakly no-gain resistor as defined in Definition 7. Hence (A-45) can not be true and (48) follows from (47).

(b) Consider the network in Fig. A-10(a) for the case when $I_{(k)} > 0$ and Fig. A-10(b) for the case when $I_{(k)} < 0$. The value of each resistor R_j

is assigned is equal to the ratio between the voltage and the current (corresponding to the operating point) across R_j. The imbedding network contains only positive linear resistors and one independent current source I_s. One possible choice of values is as follows:

(i) $I_s > \sum_{j=1}^{n-1} |I_{(j)}|$

(ii) $V_A = \frac{V_{(k-1)} - V_{(k)}}{2}$ and $V_B = \frac{V_{(k+1)} - V_{(k+2)}}{2}$

Since $\mathcal{R}$ is a weakly no-gain n-terminal resistor, the networks in Figs. A-10 (a) and (b) possess the no-gain property. If (49) holds but at least one of the inequalities in (50) does not hold, then there exists at least one current through an imbedding resistor having a current magnitude greater than $|I_s|$. For example, if (50c) {resp.; (50d)} is not true, i.e., suppose

$$I_{(1)} + I_{(2)} + \ldots + I_{(k-1)} < 0 \qquad \text{(A-48a)}$$

$$\{\text{resp.; } I_{(1)} + I_{(2)} + \ldots + I_{(k-1)} + I_{(k)} + I_{(k+1)} < 0\} \qquad \text{(A-48b)}$$

then the current i_{k-1} {resp.; i_{k+1}} through R_A {resp.; R_{k+1}} is given by

$$i_{k-1} = I_s - [I_{(1)} + I_{(2)} + \ldots + I_{(k-1)}] \qquad \text{(A-49a)}$$

$$\{\text{resp.; } i_{k+1} = I_s - [I_{(1)} + I_{(2)} + \ldots + I_{(k-1)} + I_{(k)} + I_{(k+1)}]\} \qquad \text{(A-49b)}$$

In view of (A-48) and (A-49), i_{k-1} {resp.; i_{k+1}} is greater than I_s. Clearly this is impossible since the networks in Figs. A-10(a) and (b) are no-gain networks. Hence (A-48) can not be true and (50) must follow from (49). This completes the proof of Lemma 6. ∎

A-7. Proof of Lemma 7

Consider the network shown in Fig. A-11 where each element R_k (k=1,2,...,n-1) is chosen as follows:

Case 1. When $V_{(k)} - V_{(k+1)} \neq 0$ and $[I_{(1)} + I_{(2)} + \ldots + I_{(k)}] \neq 0$, R_k is a positive linear two-terminal resistor with a resistance value of

$$R_k = \frac{V_{(k)} - V_{(k+1)}}{I_{(1)} + I_{(2)} + \ldots + I_{(k)}} \quad \Omega$$

Case 2. When $V_{(k)} - V_{(k+1)} = 0$ and $[I_{(1)} + I_{(2)} + \ldots + I_{(k)}] \neq 0$, R_k is a short circuit element.

Case 3. When $[I_{(1)} + I_{(2)} + \ldots + I_{(k)}] = 0$ and $V_{(k)} - V_{(k-1)} \neq 0$, R_k is an open circuit element.

Case 4. When $V_{(1)} - V_{(k+1)} = 0$ and $[I_{(1)} + I_{(2)} + \ldots + I_{(k)}] = 0$, R_k is a 1Ω resistor

Clear, this network has the same operating-point voltages and currents as those of $\mathcal{R}$. ¤

FIGURE CAPTIONS

Figure 1. A multi-terminal resistor with reference voltage and current directions defined.

Figure 2. A typical terminal in a network composed of positive linear two-terminal resistors.

Figure 3. Replacement of resistors R_a, R_b by resistors R'_a, R'_b, R_c with the same operating point.

Figure 4. A typical terminal following repeated replacement of a two-resistor network by a three-resistor network that maintains the same operating point.

Figure 5. Grounded (n-1)-port representation of an n-terminal resistor where reference voltage and current directions are defined.

Figure 6. Regions where families of v-i characteristics are given for elements that are not strictly passive.

Figure 7. A network with all internal independent sources extracted.

Figure 8. Bounding regions of TC plots described in Property 15. (a) Ungrounded case (nodes ⓑ and ⓓ are not necessarily connected). (b) General case; E_0 = sum of magnitudes of voltage sources, (c) nodes ⓐ and ⓒ are connected together, (d) all internal sources are grounded (e) all voltage sources (including v_{in}) are grounded (f) all voltage sources (including v_{in}) are grounded and nodes ⓐ and ⓒ are connected together.

Figure 9. Bounding regions for TC plots described in Property 16, (a) Grounded case (nodes ⓑ and ⓓ connected), (b) all internal sources are grounded, (c) all internal sources have their negative terminals grounded, (d) N contains no internal sources.

Figure 10. Bounding regions for DP plots described in Property 17, (a) general network with series resistor R, (b) bounds on resulting DP plot, (c) bounds on DP plot as $R \to 0$.

Figure 11. Bounding regions for DP plots described in Property 18, (a) general network configuration with series resistor R, (b) bounds on corresponding DP plot, (c) bounding region when $R \to 0$.

Figure 12. General network configuration used in Property 21.

Figure 13. Differential amplifier, (a) circuit realization, (b) TC plot.

Figure 14. Full-wave rectifier, (a) circuit realization, (b) TC plot.

Figure 15. Limiter circuit, (a) two-operational amplifier realization, (b) TC plot, (c) operational amplifier model.

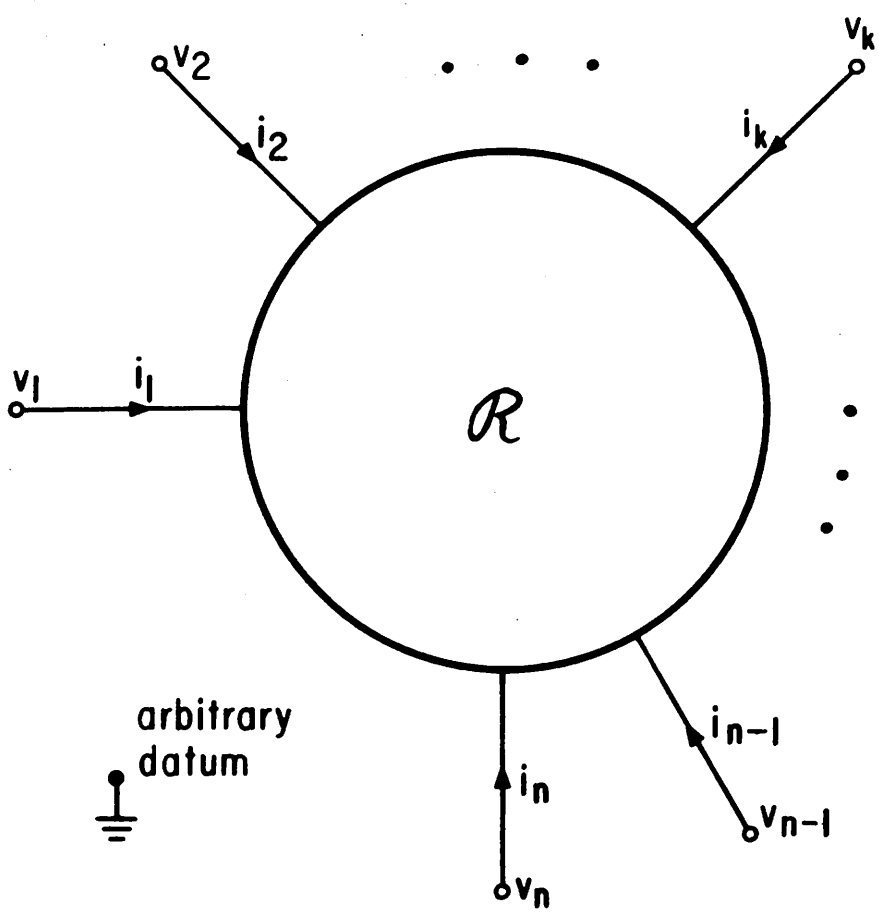

v_2
i_2
v_k
i_k
v_1
i_1
$\mathcal{R}$
arbitrary datum
i_n
v_n
i_{n-1}
v_{n-1}

Fig. 1

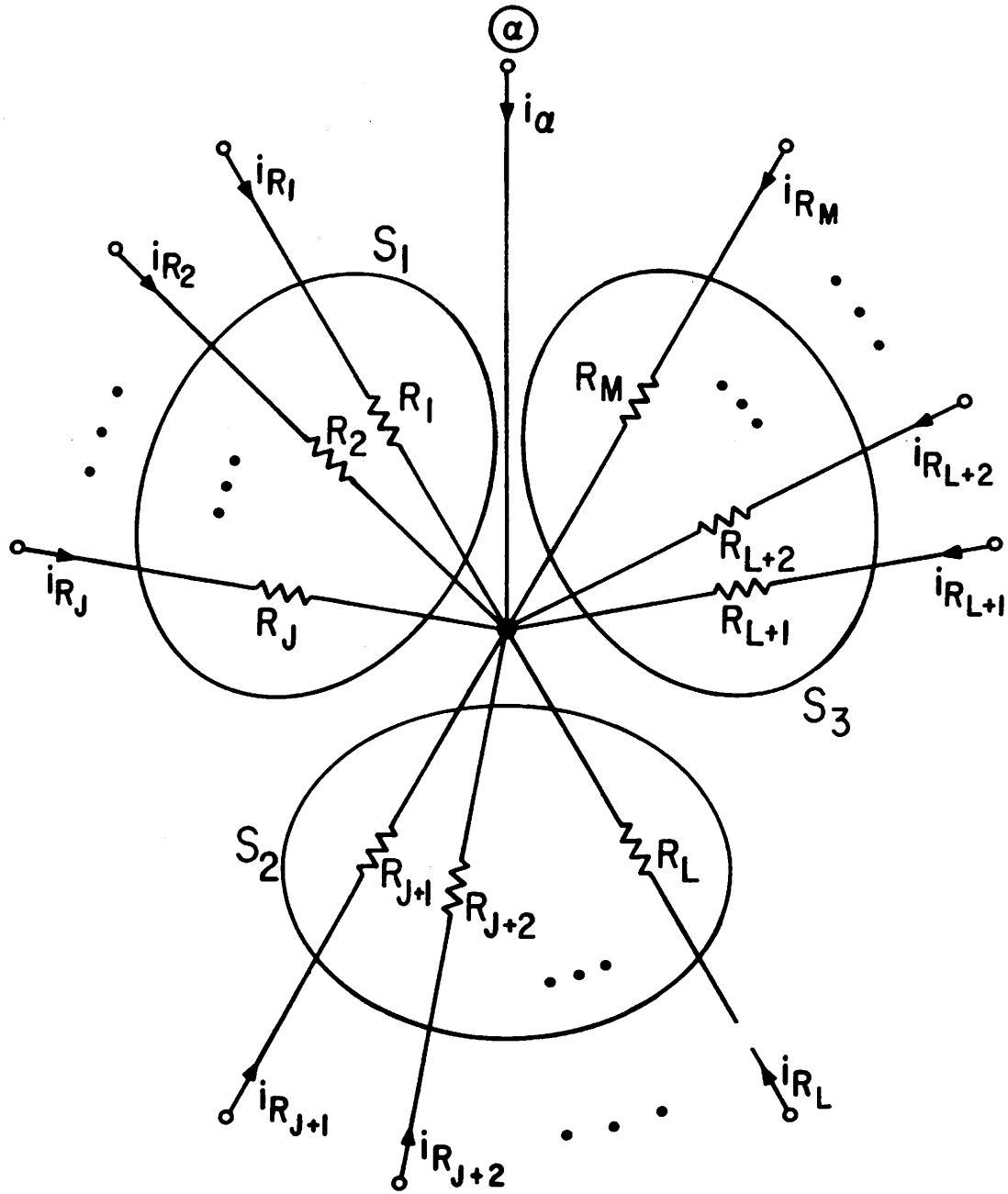
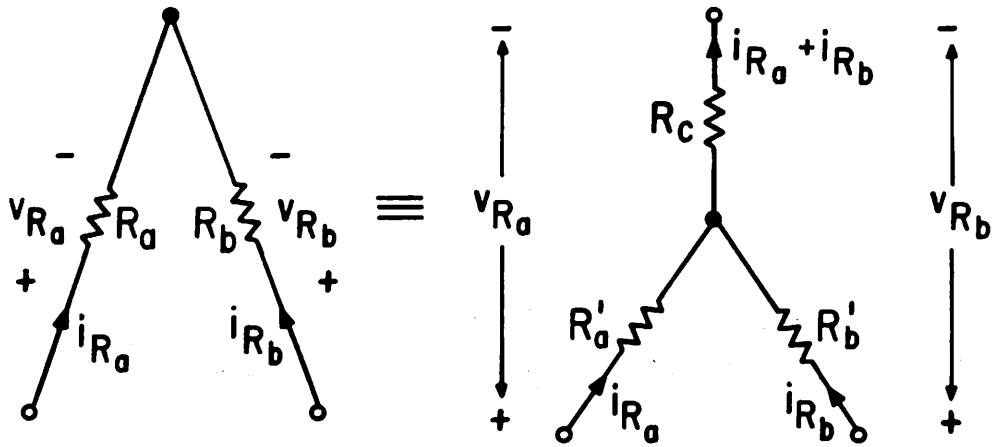

α
i_α
i_{R_1}
i_{R_2}
S_1
R_1
R_2
i_{R_J}
R_J
i_{R_M}
R_M
$i_{R_{L+2}}$
R_{L+2}
$i_{R_{L+1}}$
R_{L+1}
S_3
S_2
R_{J+1}
R_{J+2}
R_L
$i_{R_{J+1}}$
$i_{R_{J+2}}$
i_{R_L}

Fig. 2

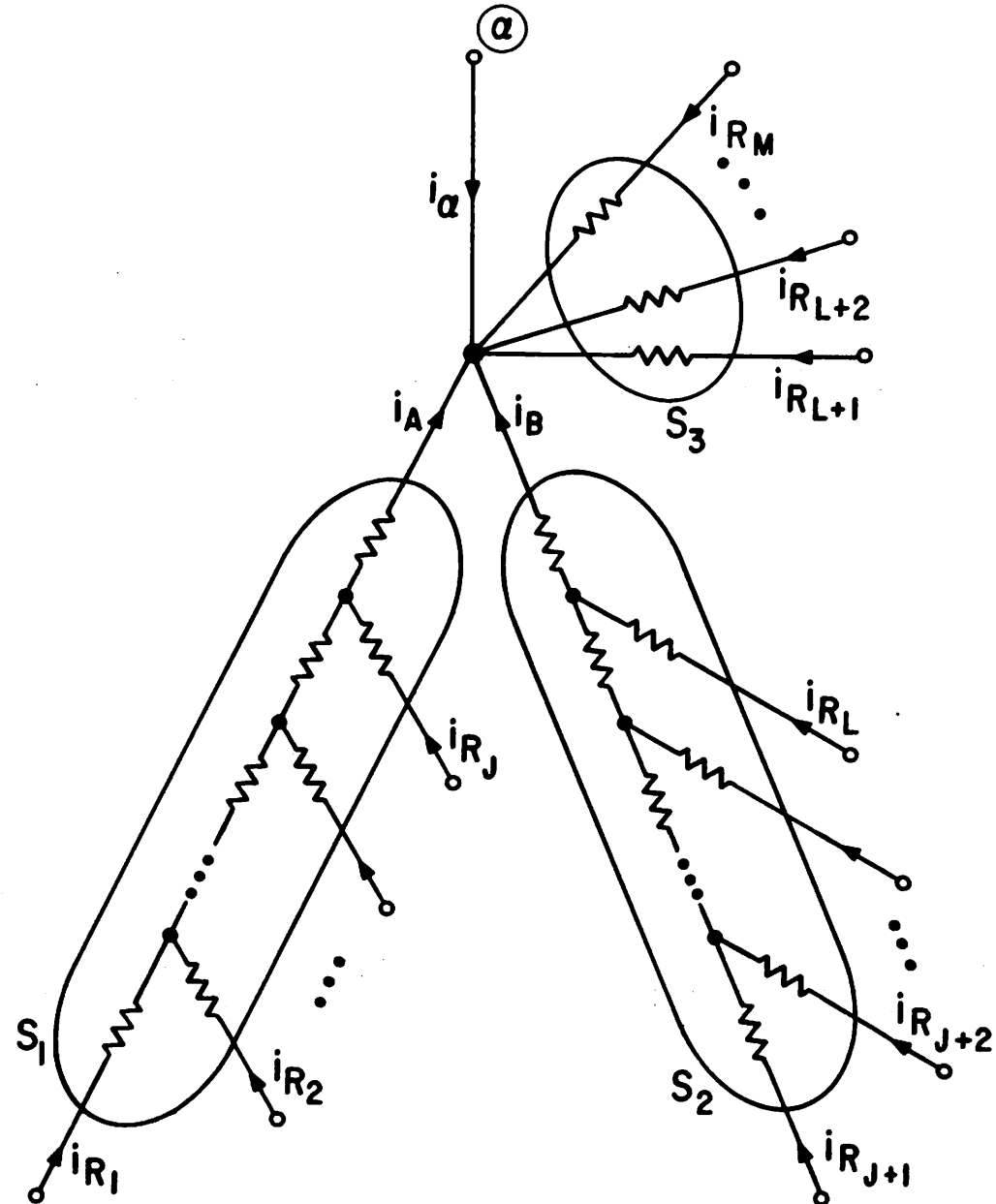


$$R'_a = \frac{|v_{R_a}| - \frac{1}{2}\min\left\{|v_{R_a}|, |v_{R_b}|\right\}}{|i_{R_a}|}$$

$$R'_b = \frac{|v_{R_b}| - \frac{1}{2}\min\left\{|v_{R_a}|, |v_{R_b}|\right\}}{|i_{R_b}|}$$

$$R_c = \frac{\frac{1}{2}\min\left\{|v_{R_a}|, |v_{R_b}|\right\}}{|i_{R_a}+i_{R_b}|}$$

Fig. 3



$$i_A = \sum_{k=1}^{J} i_{R_k} \quad , \quad i_B = \sum_{k=J+1}^{L} i_{R_k}$$

Fig. 4

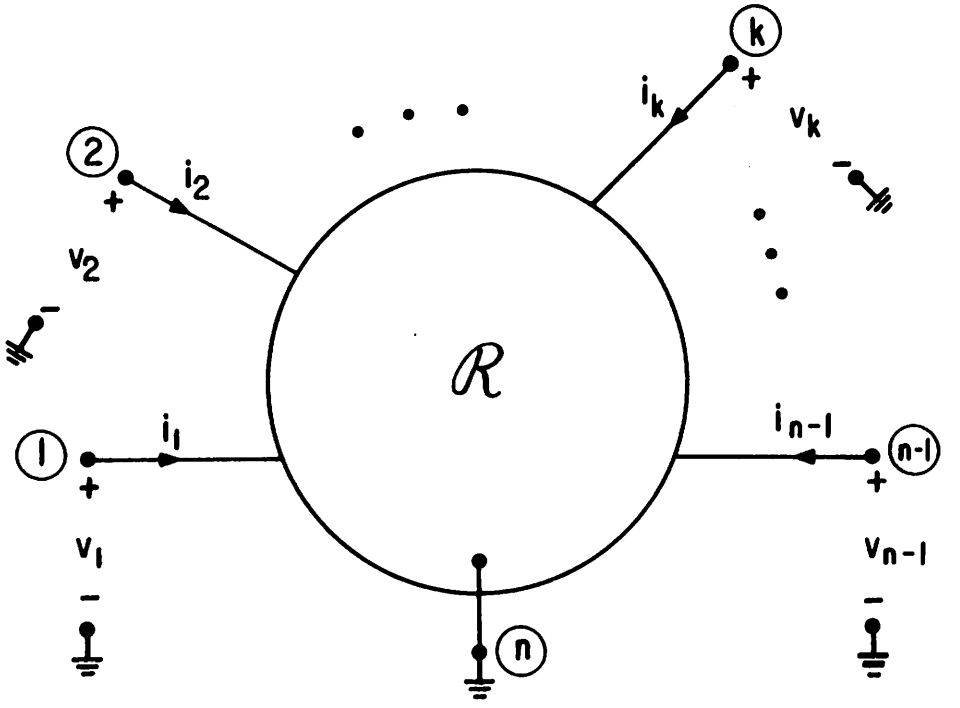

k
i_k
v_k
2
i_2
v_2
$\mathcal{R}$
1
i_1
i_{n-1}
n-1
v_1
v_{n-1}
n

Fig. 5

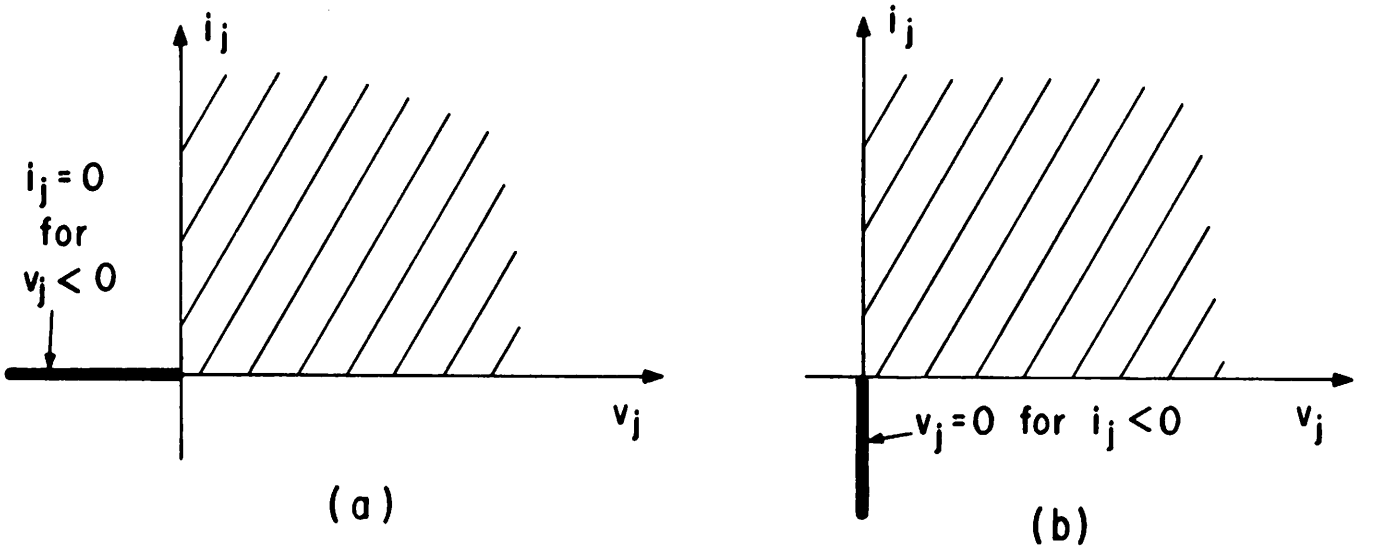

i_j
$i_j = 0$ for $v_j < 0$
v_j
(a)
i_j
$v_j = 0$ for $i_j < 0$
v_j
(b)

Fig. 6

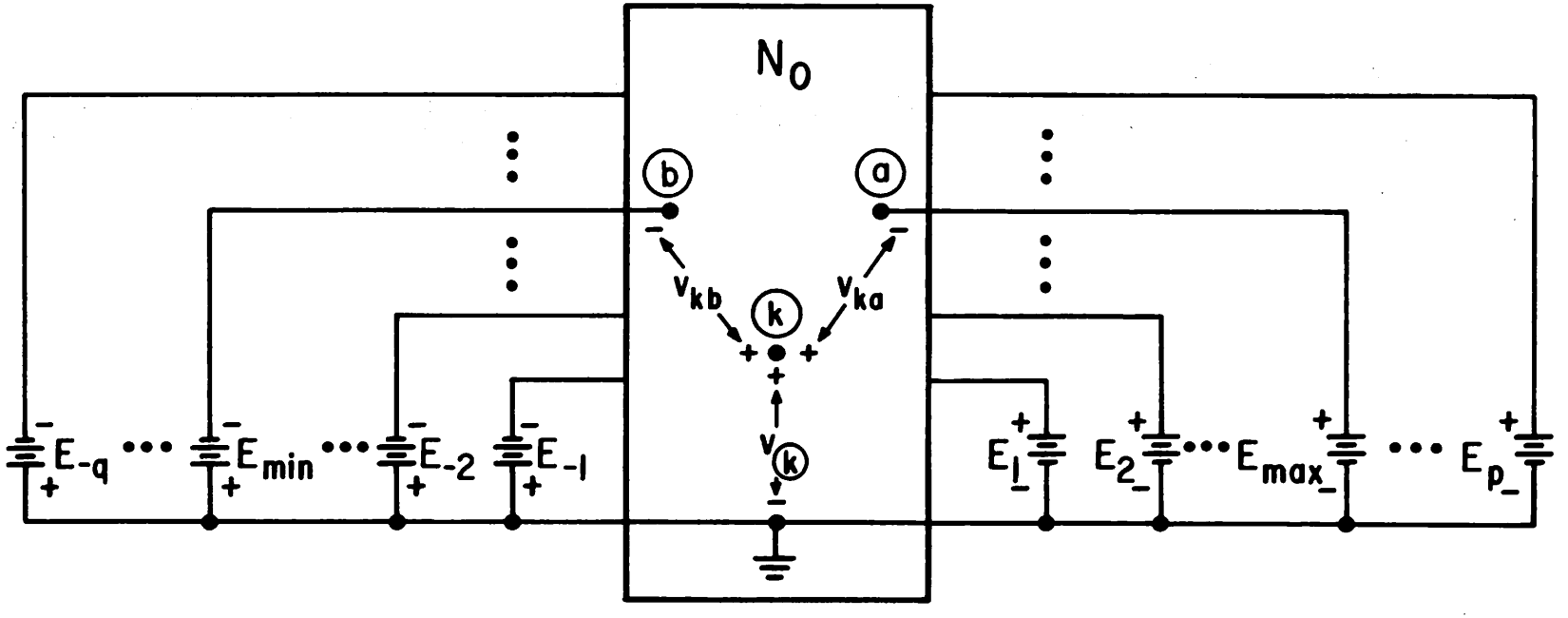
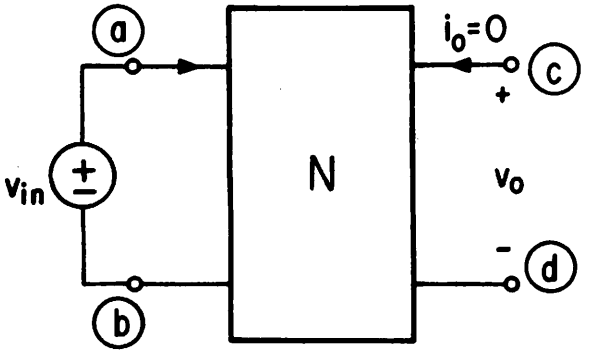
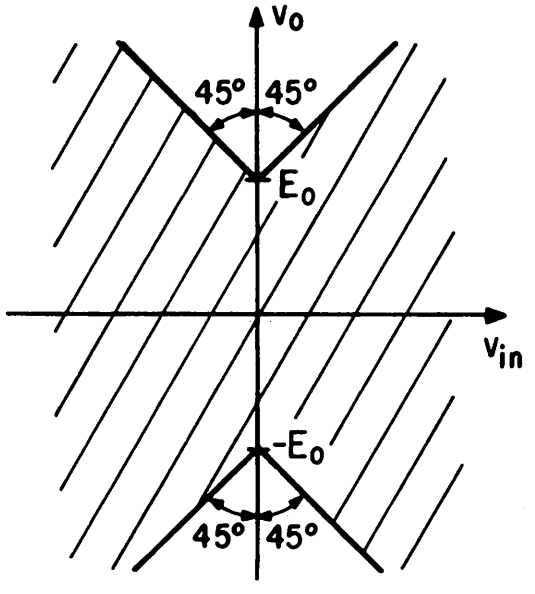


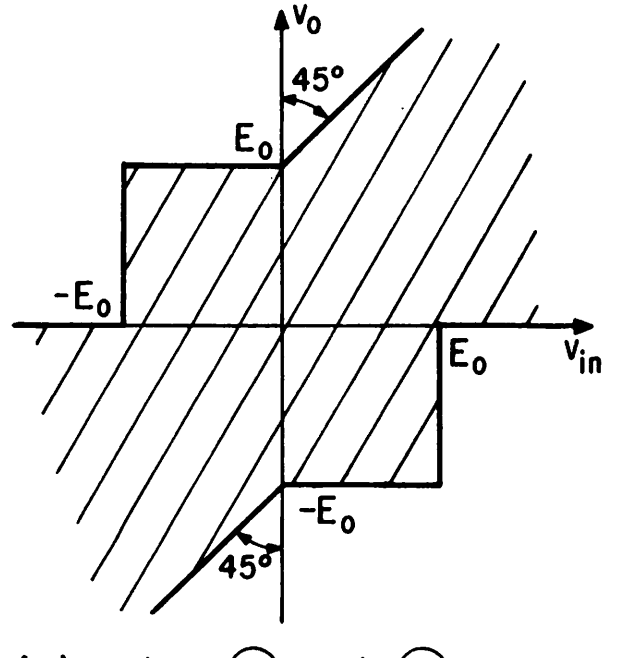
Fig. 7



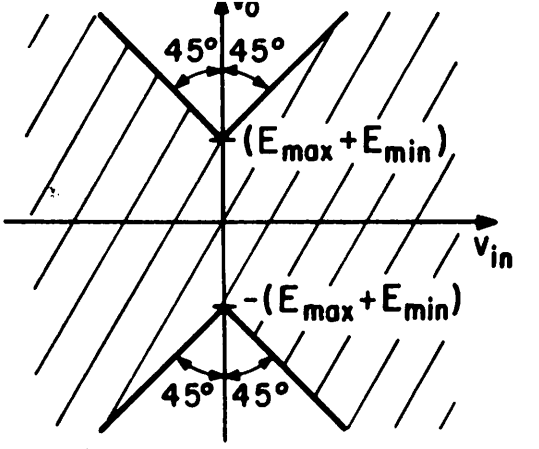
(a) ungrounded case (nodes (b) and (d) are not necessarily connected)



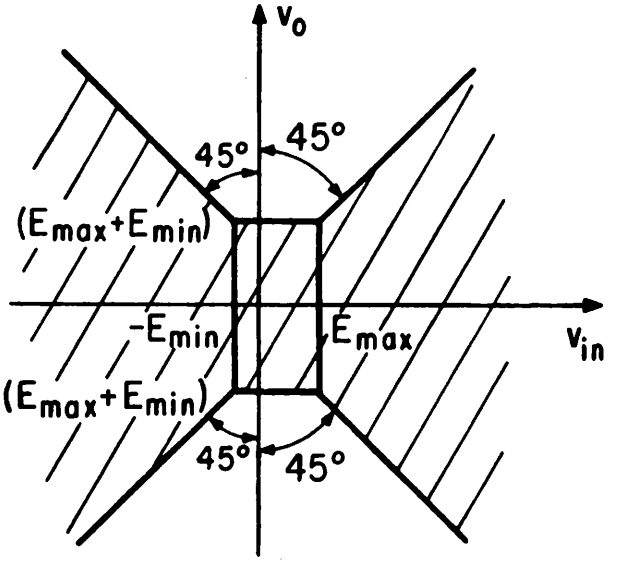
(b) general case; E_o = sum of magnitude of voltage sources



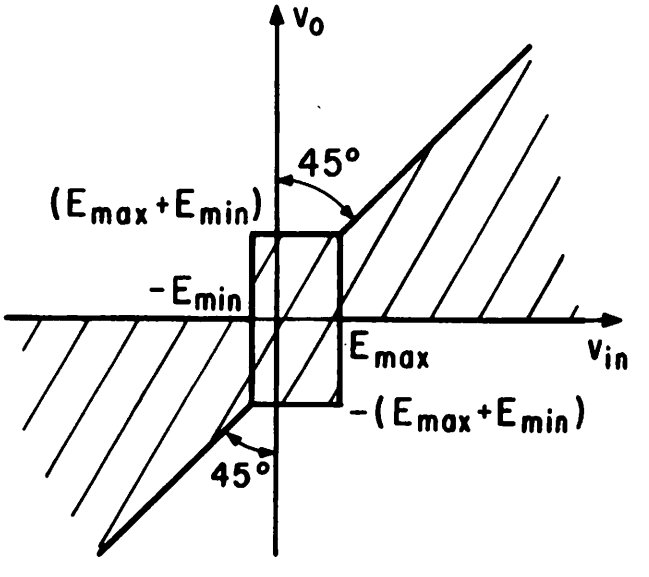
(c) nodes (a) and (c) are connected together



(d) all internal sources are grounded

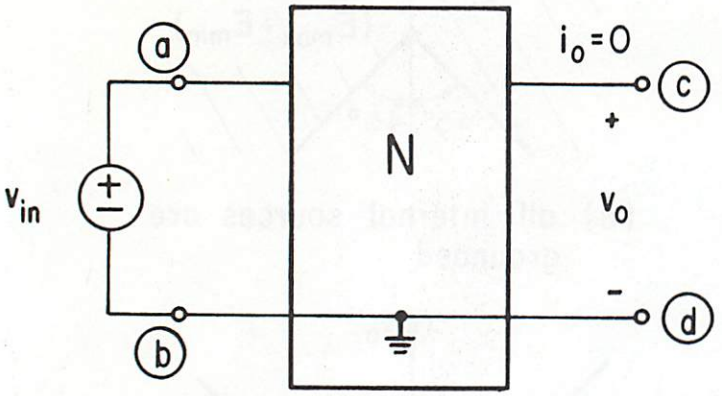


(e) all voltage sources (including v_{in}) are grounded

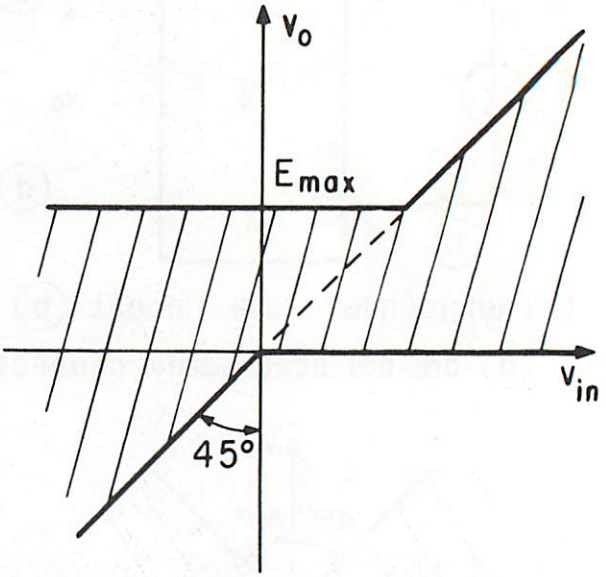


(f) all voltage sources (including v_{in}) are grounded, and nodes (a) and (c) are connected together

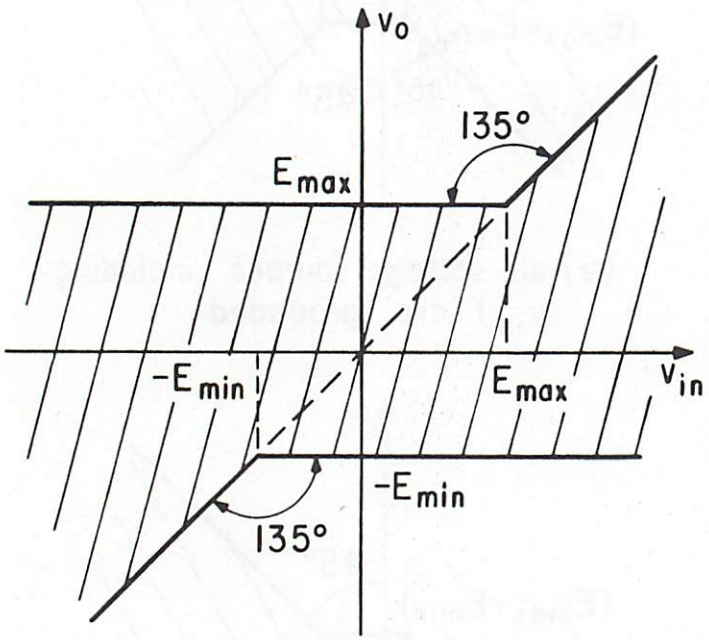
Fig. 8



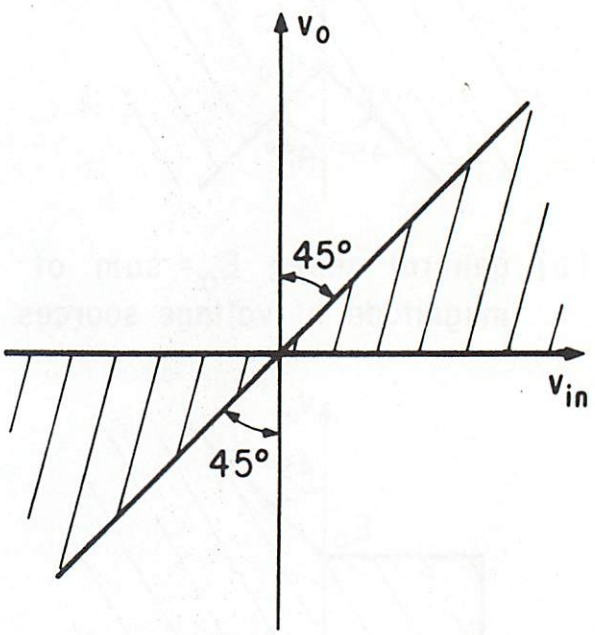
(a) grounded case (nodes (b) and (d) connected)



(c) all internal sources have their negative terminals grounded

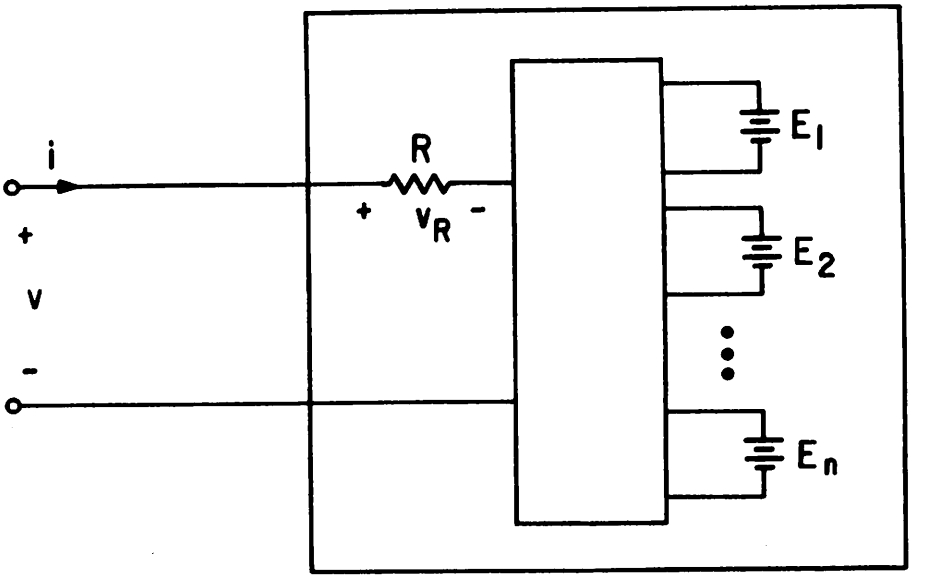


(b) all internal sources are grounded

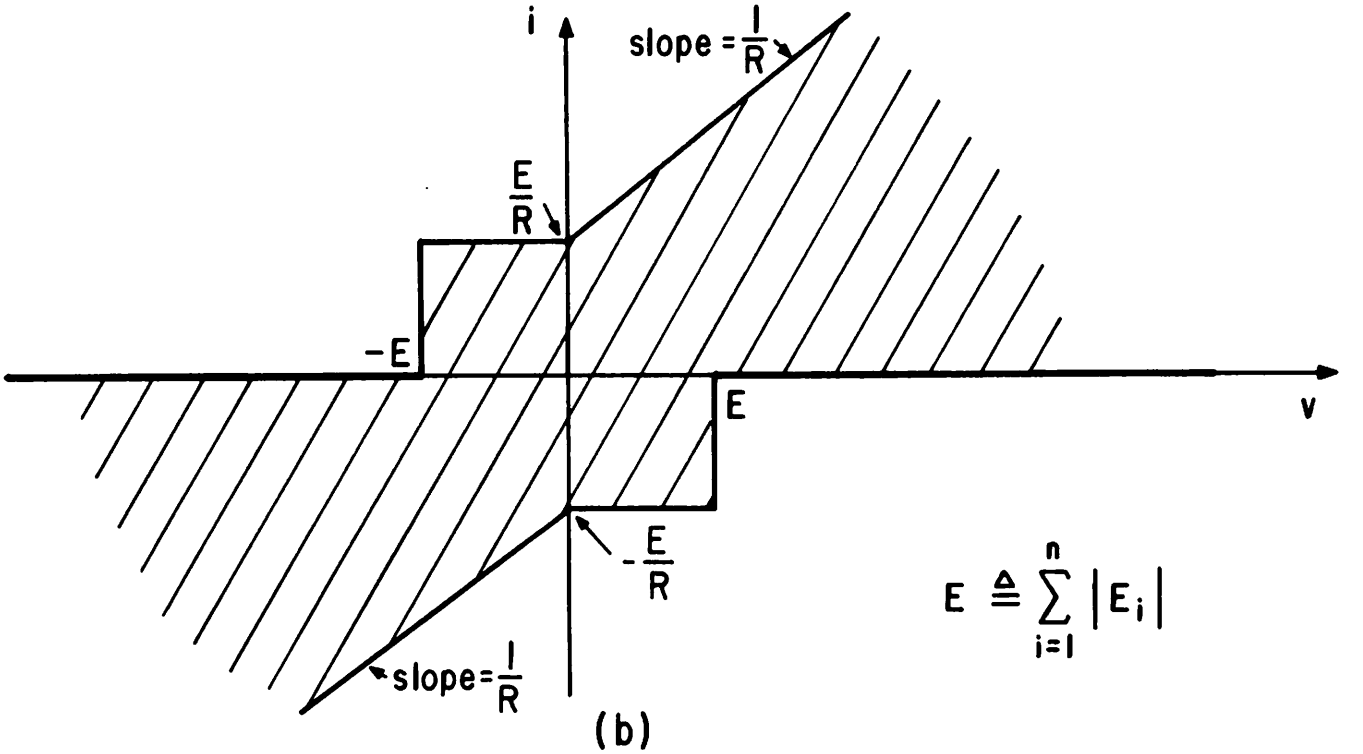


(d) N contains no internal sources

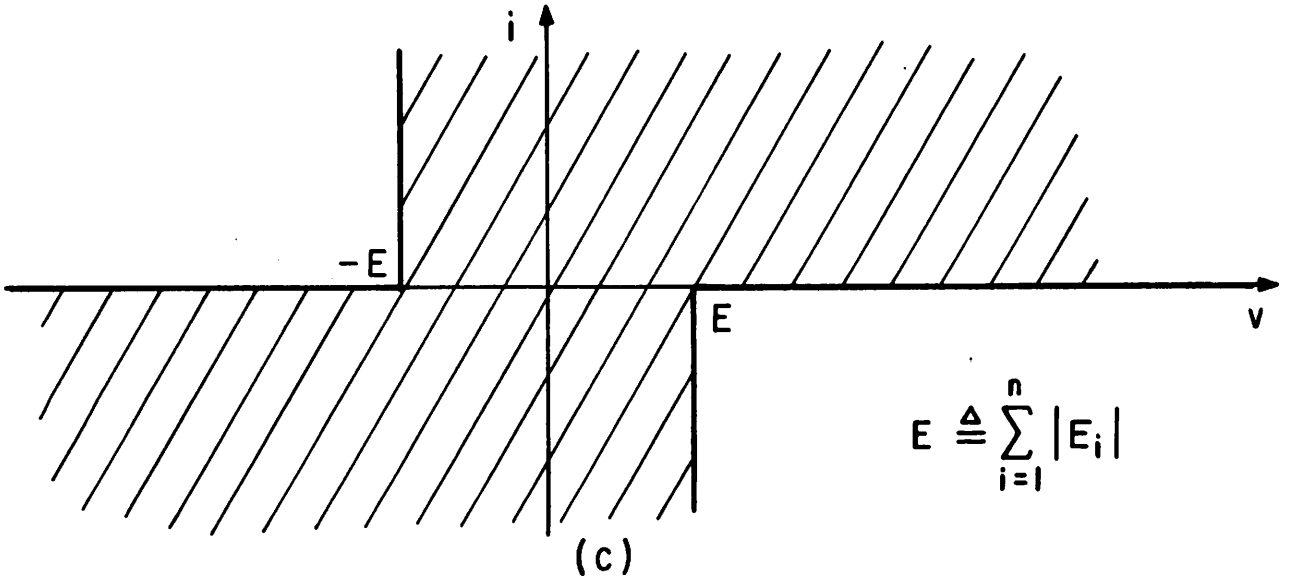
Fig. 9


i
R
+
v_R
-
+
v
-
E_1
E_2
E_n

(a)

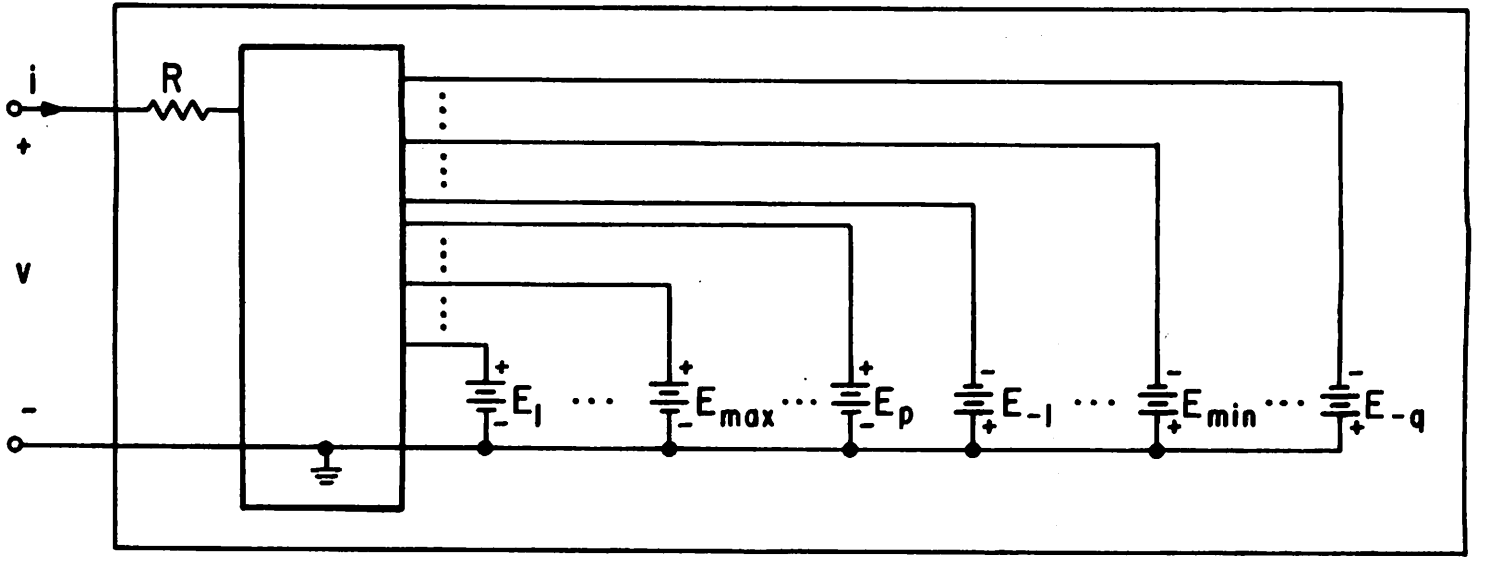

i
slope = 1/R
E/R
-E
E
v
-E/R
slope=1/R
$E \triangleq \sum_{i=1}^{n} |E_i|$

(b)

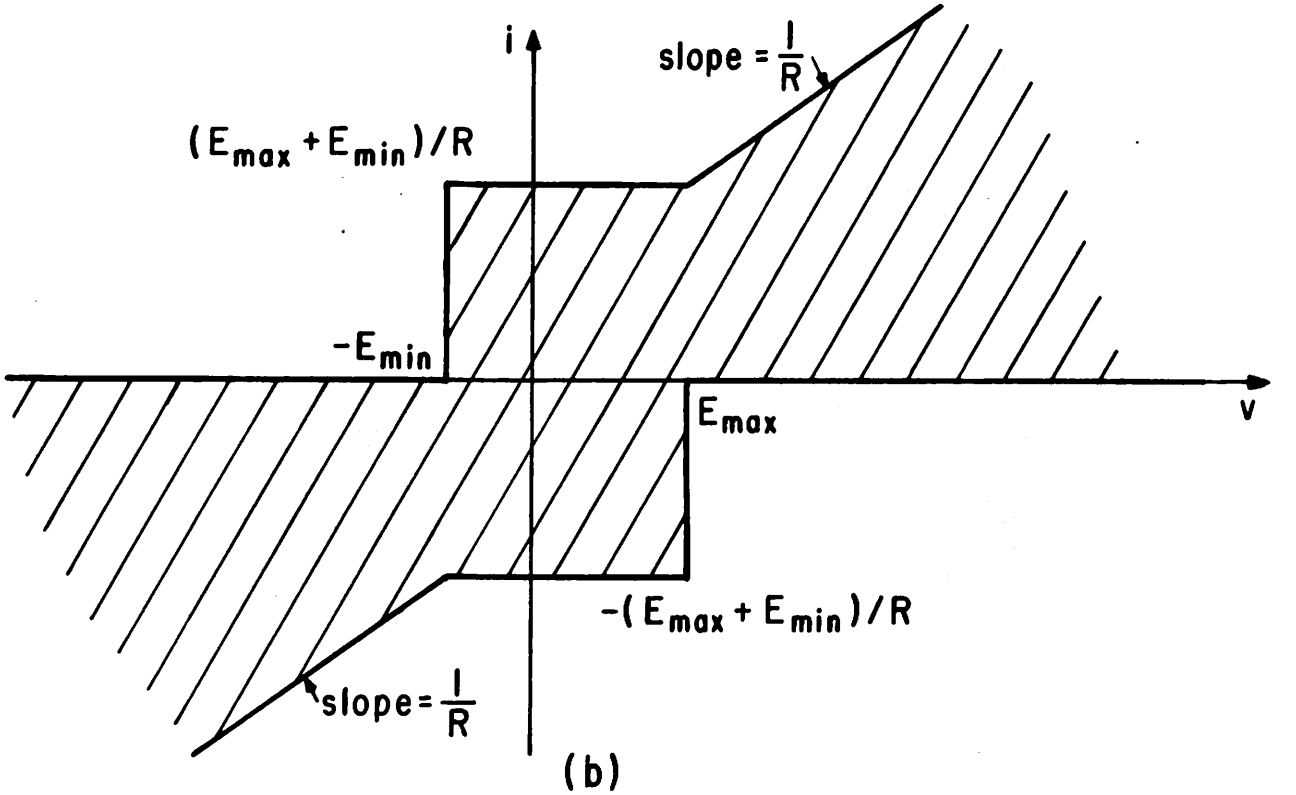

i
-E
E
v
$E \triangleq \sum_{i=1}^{n} |E_i|$

(c)

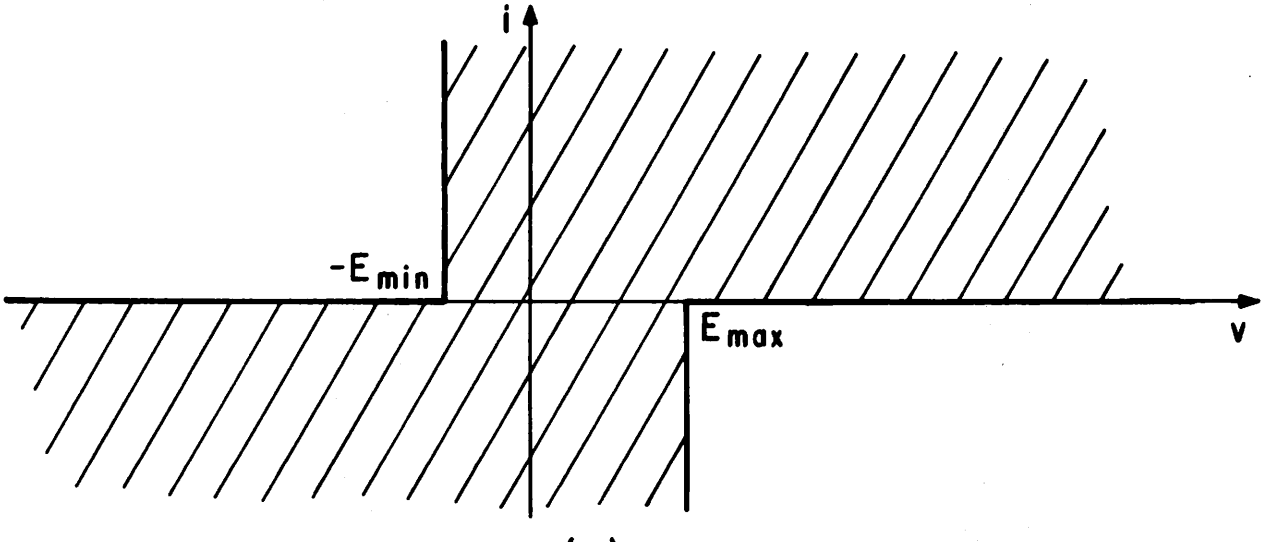
Fig. 10


i
R
+
v
-
E_1
E_{max}
E_p
E_{-1}
E_{min}
E_{-q}

(a)


i
slope = $\frac{1}{R}$
$(E_{max} + E_{min})/R$
$-E_{min}$
E_{max}
v
$-(E_{max} + E_{min})/R$
slope = $\frac{1}{R}$

(b)


i
$-E_{min}$
E_{max}
v

(c)

Fig. 11

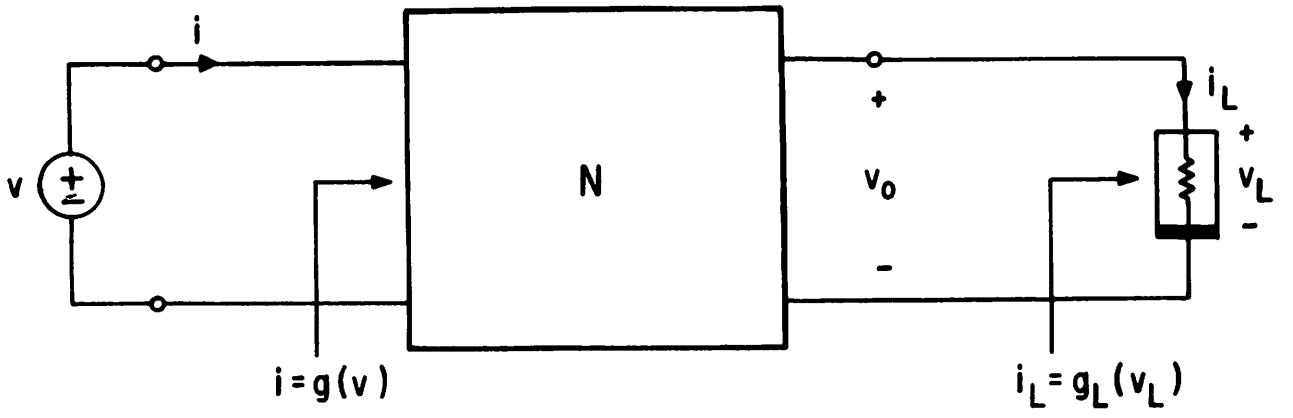


Fig. 12

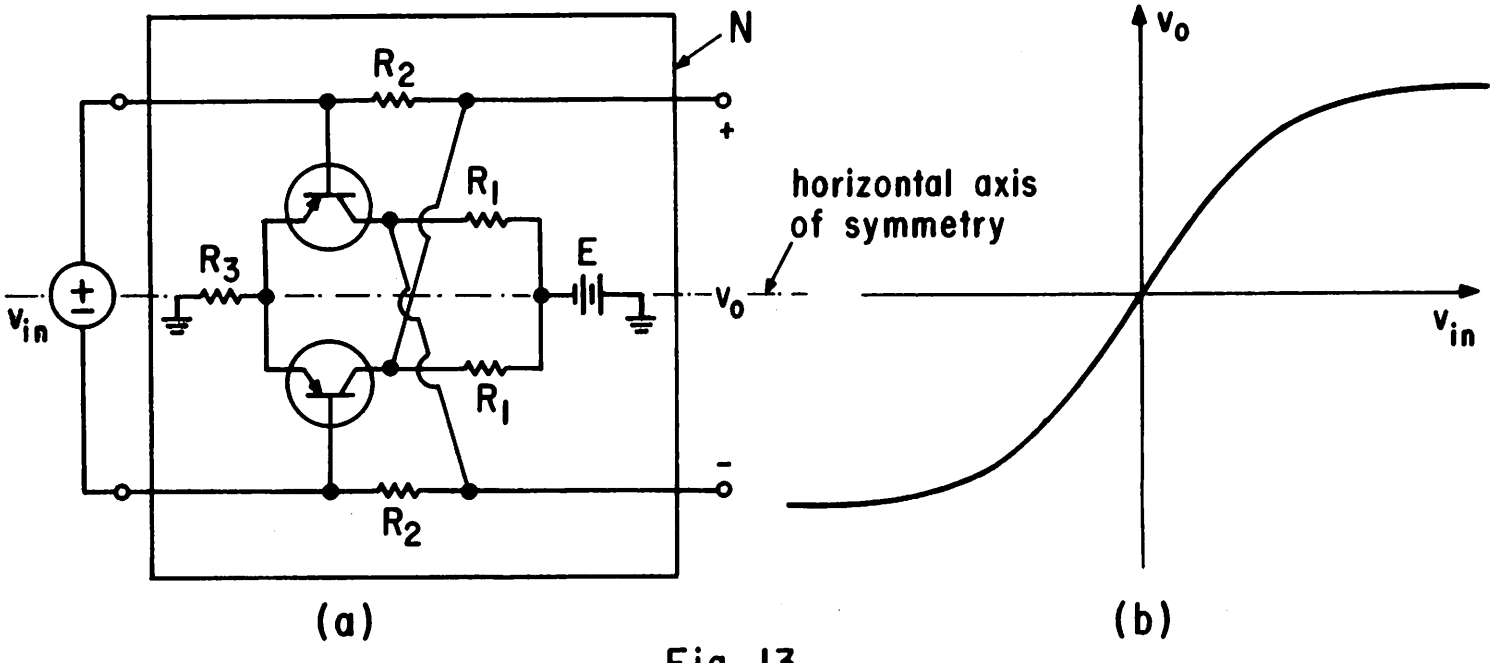


Fig. 13

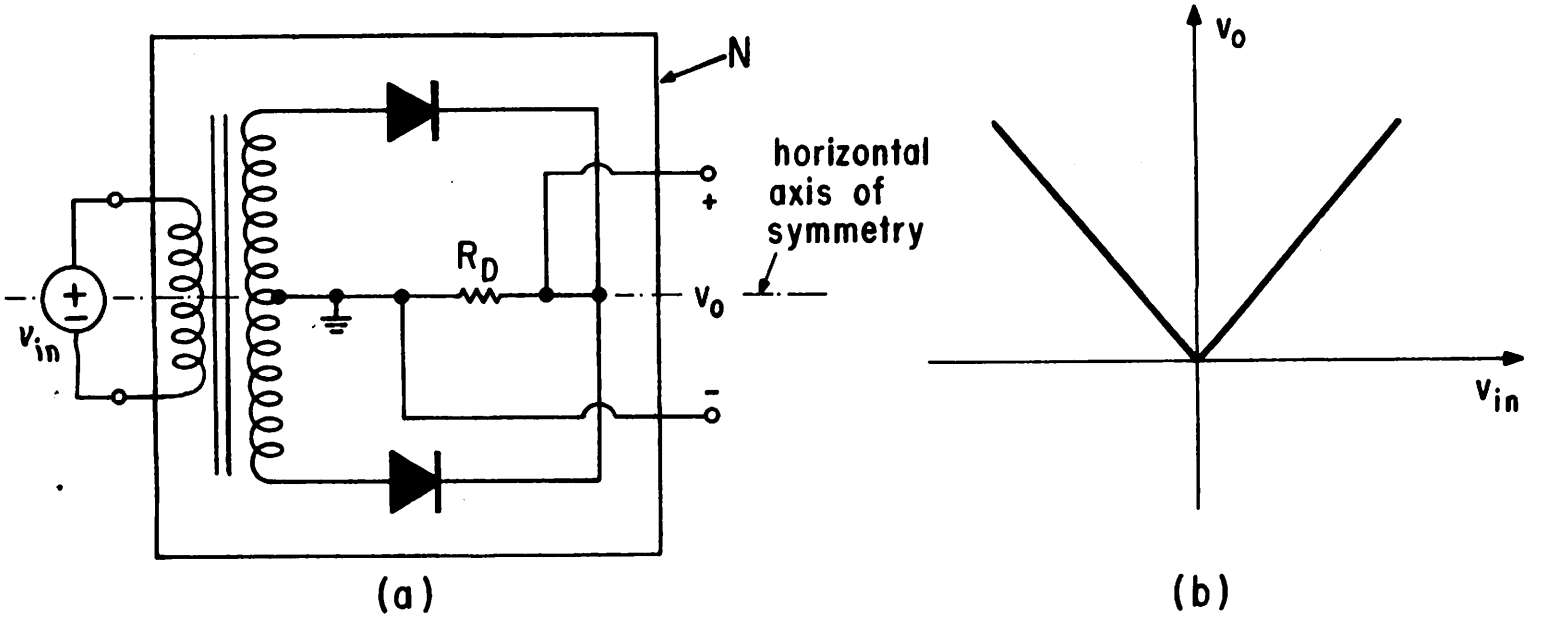


Fig. 14

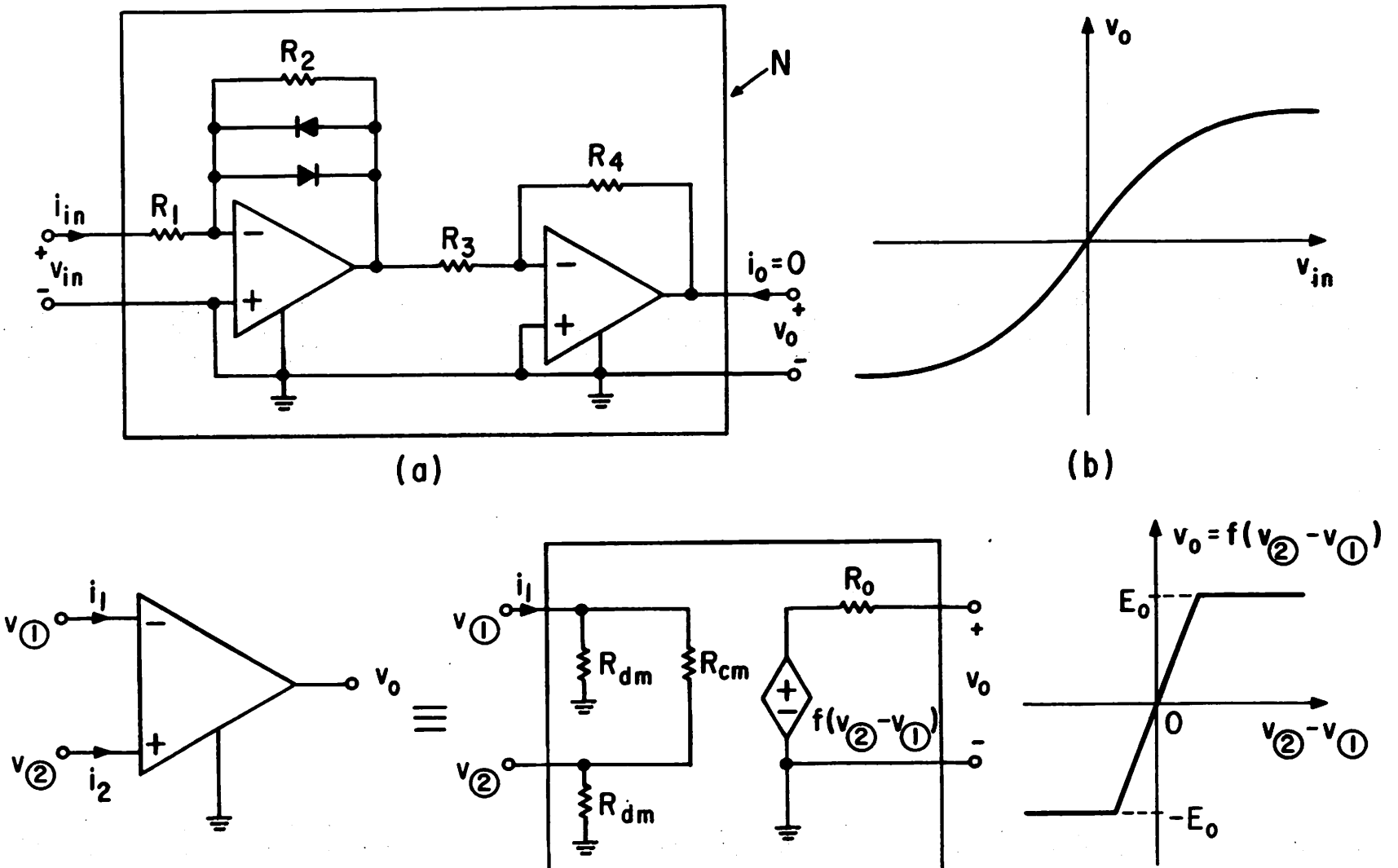

R2
N
R4
iin
R1
R3
io=0
+
vin
-
+
vo
-
(a)
vo
vin
(b)
i1
v①
v②
i2
vo
≡
i1
R0
v①
Rdm
Rcm
+
vo
-
f(v②-v①)
v②
Rdm
vo = f(v② - v①)
Eo
0
v② - v①
-Eo
(c)

Fig. 15

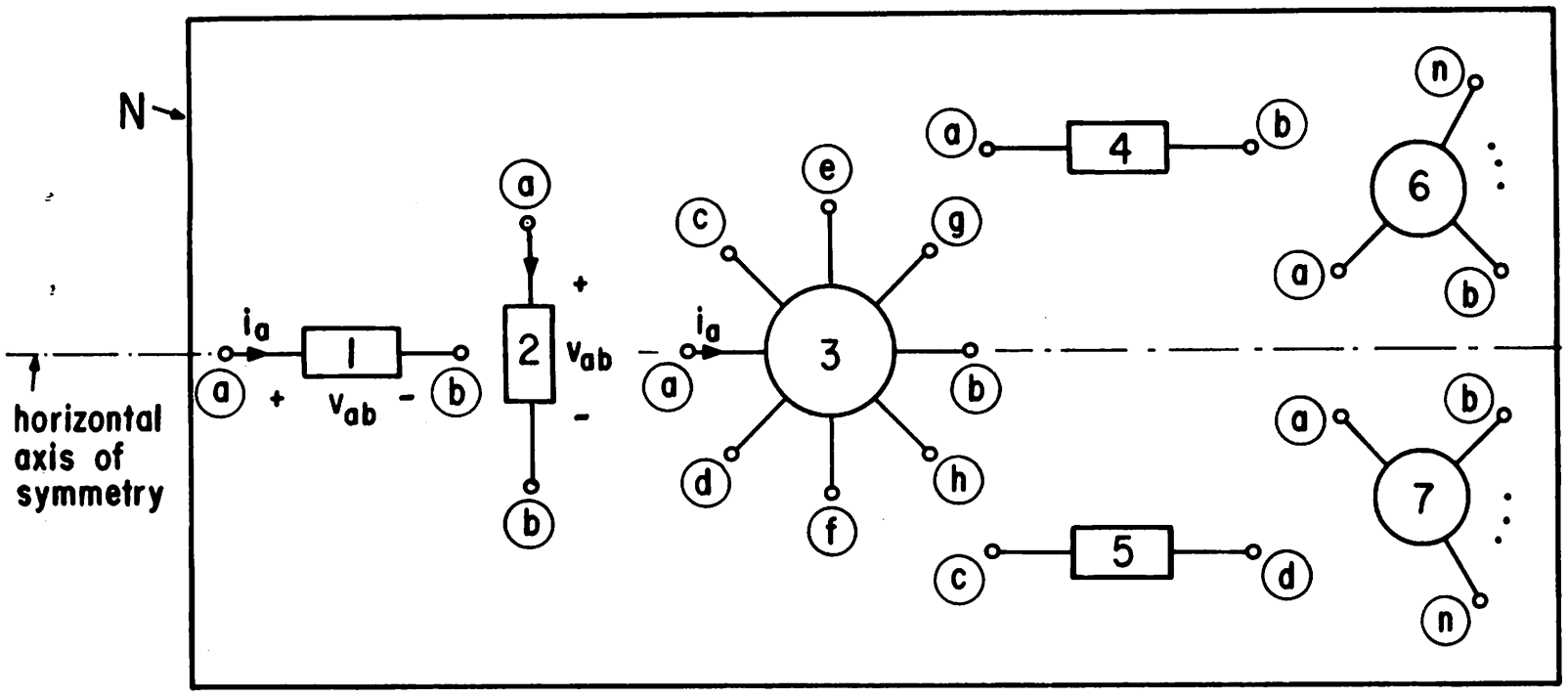

N
horizontal axis of symmetry
i_a
1
v_{ab}
2
3
4
5
6
7
a
b
c
d
e
f
g
h
n

Fig. 16

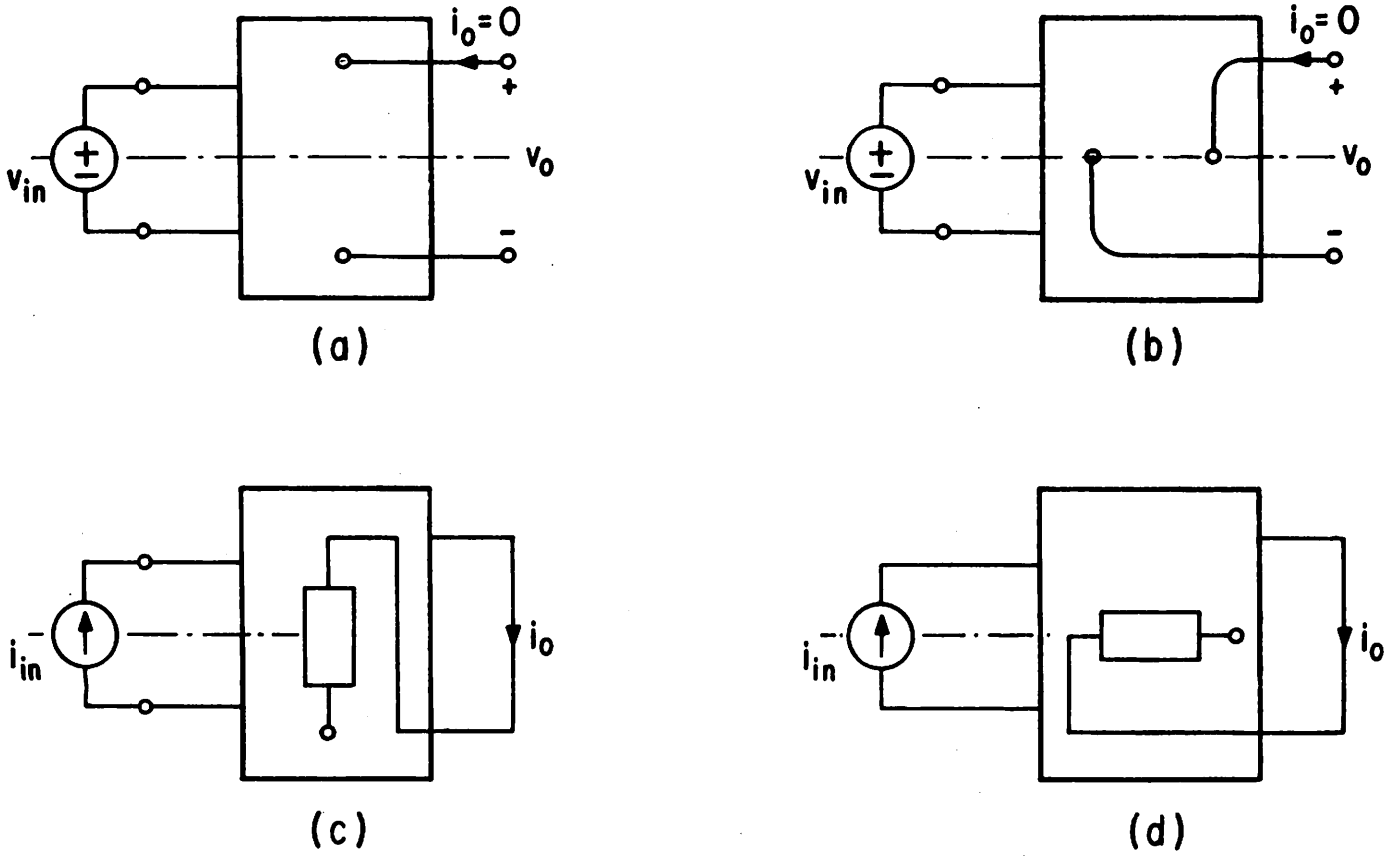
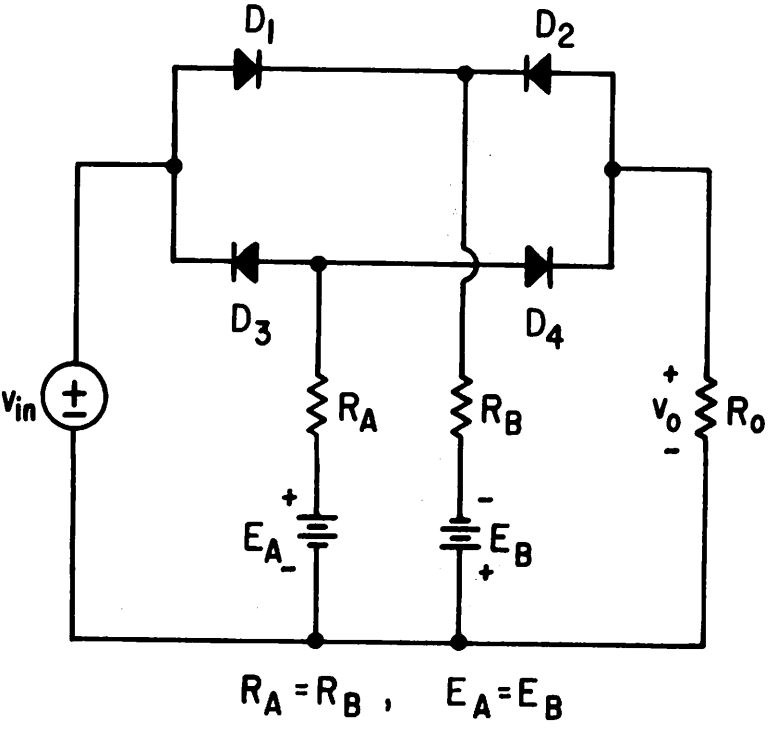
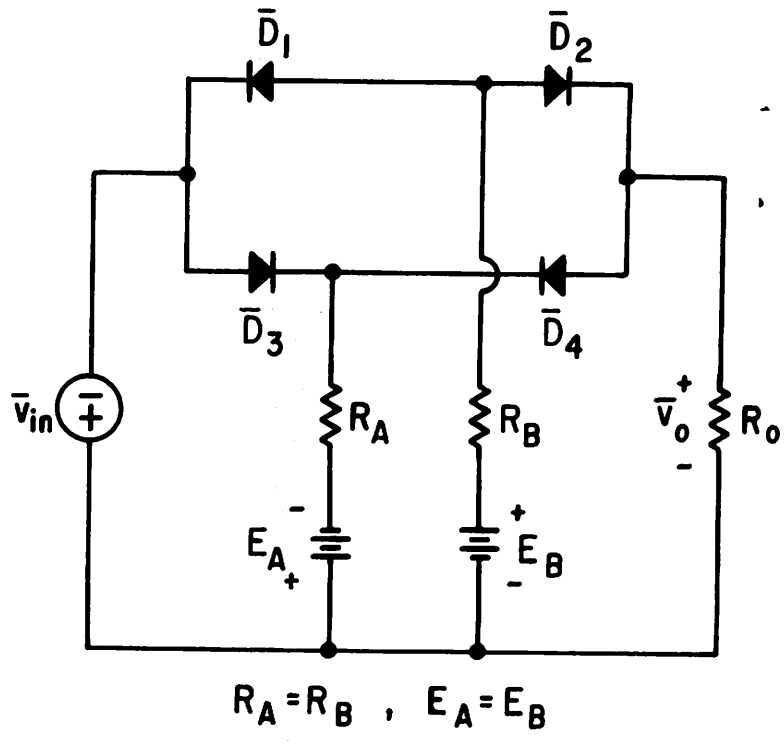

$i_o = 0$
v_{in}
v_o
(a)
(b)
i_{in}
i_o
(c)
(d)

Fig. 17

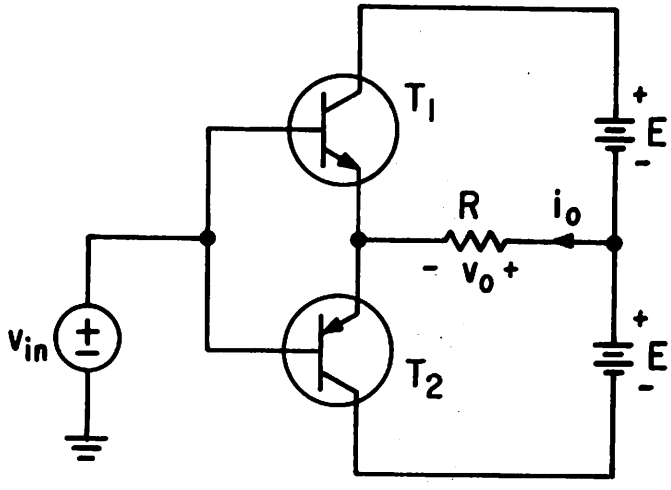


(a) N

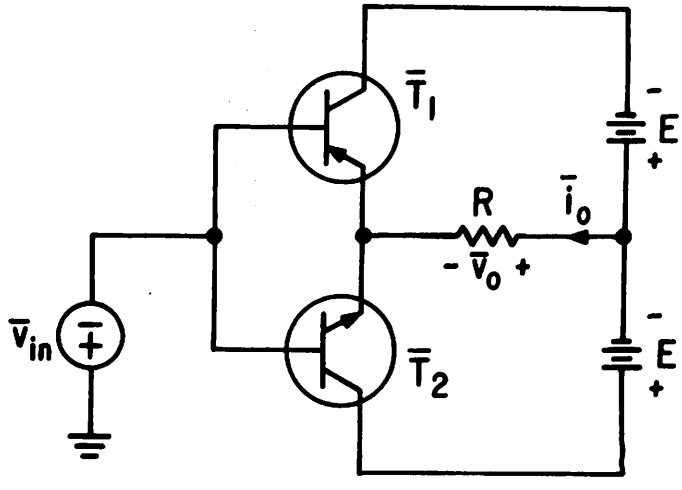


(b) N̄

Fig. 18



(a) N



(b) N̄

Fig. 19

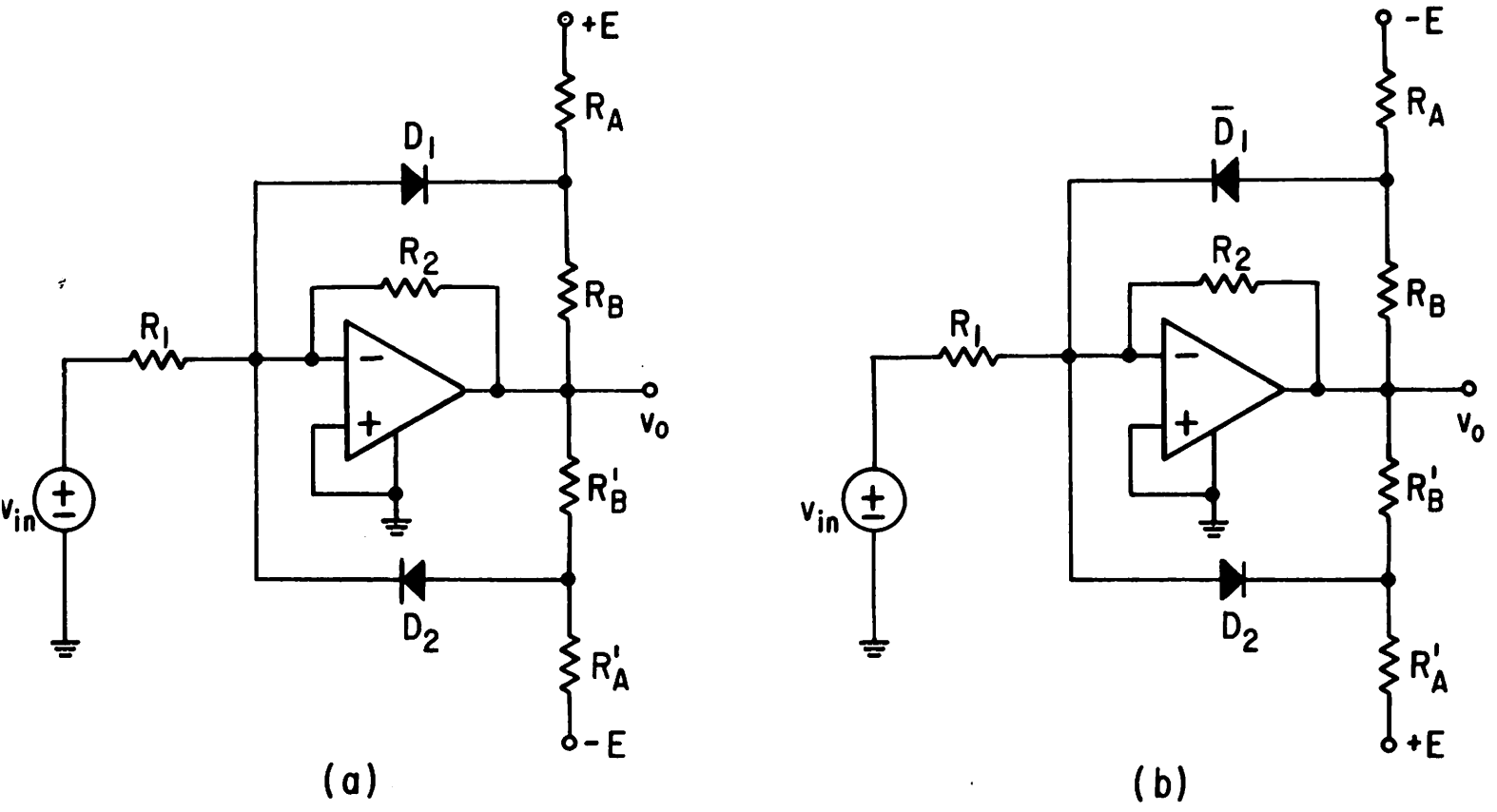

+E
R_A
D_1
R_2
R_B
R_1
v_o
v_in
R'_B
D_2
R'_A
-E
(a)
-E
R_A
D̄_1
R_2
R_B
R_1
v_o
v_in
R'_B
D_2
R'_A
+E
(b)

Fig. 20

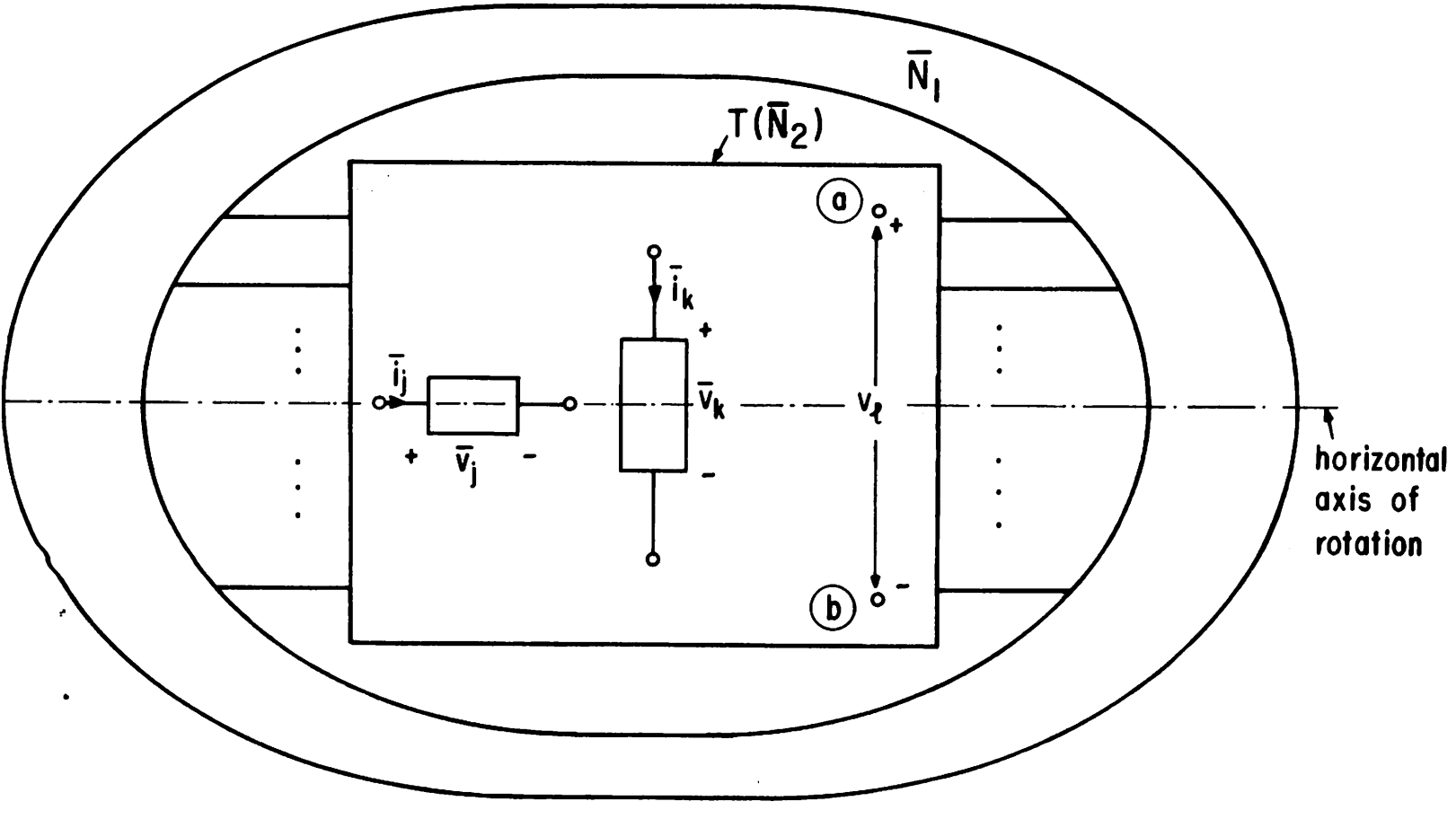

N̄_1
T(N̄_2)
a
+
ī_k
+
ī_j
v̄_k
v_t
+
v̄_j
-
-
b
-
horizontal
axis of
rotation

Fig. 21

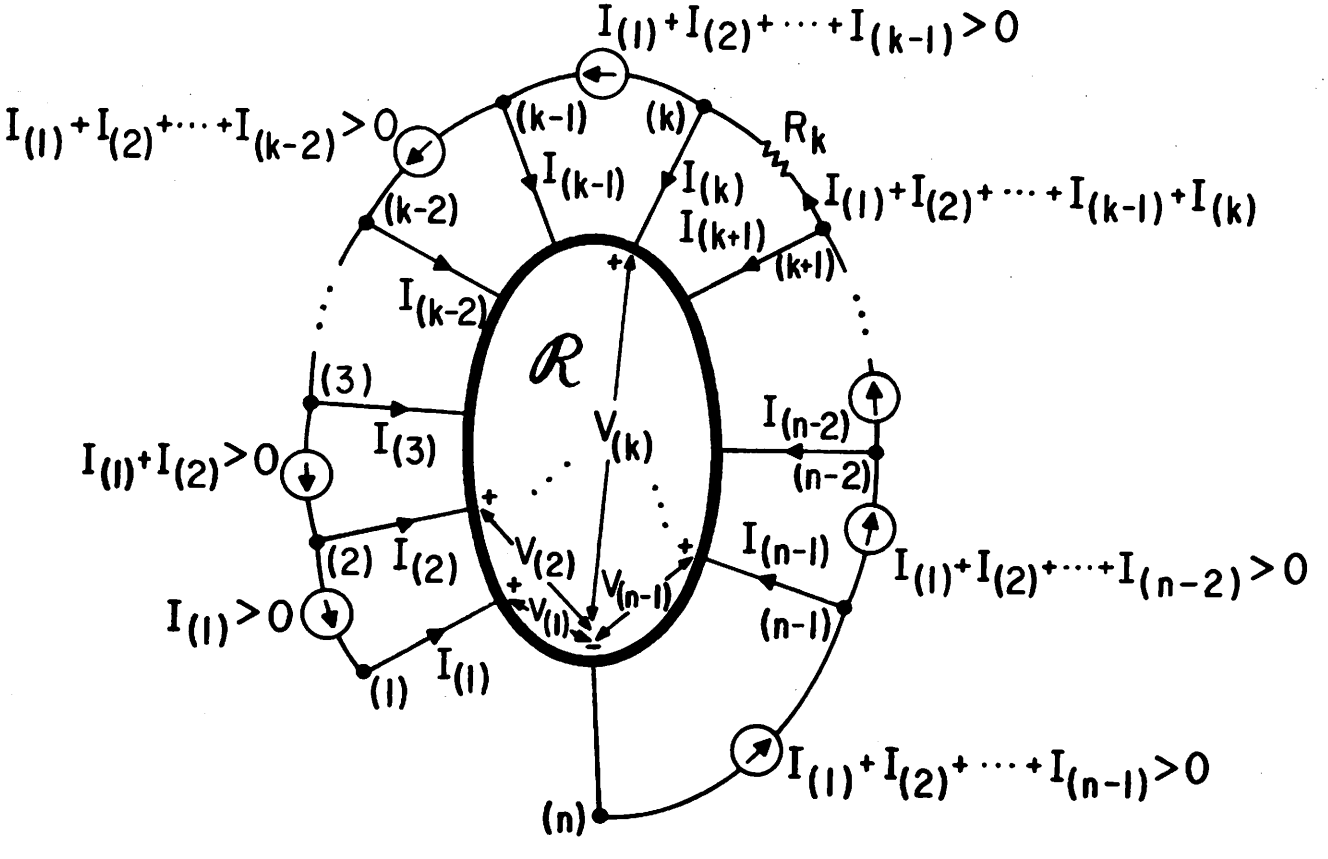

$I_{(1)}+I_{(2)}+\cdots+I_{(k-1)}>0$
$I_{(1)}+I_{(2)}+\cdots+I_{(k-2)}>0$
$I_{(1)}+I_{(2)}>0$
$I_{(1)}>0$
$I_{(1)}+I_{(2)}+\cdots+I_{(k-1)}+I_{(k)}$
$I_{(1)}+I_{(2)}+\cdots+I_{(n-2)}>0$
$I_{(1)}+I_{(2)}+\cdots+I_{(n-1)}>0$
R_k
$\mathcal{R}$
$V_{(k)}$
$V_{(2)}$
$V_{(n-1)}$
$V_{(1)}$
$I_{(k-2)}$
$I_{(k-1)}$
$I_{(k)}$
$I_{(k+1)}$
$I_{(3)}$
$I_{(2)}$
$I_{(1)}$
$I_{(n-2)}$
$I_{(n-1)}$
(1)
(2)
(3)
(k-2)
(k-1)
(k)
(k+1)
(n-2)
(n-1)
(n)

Fig. A-1

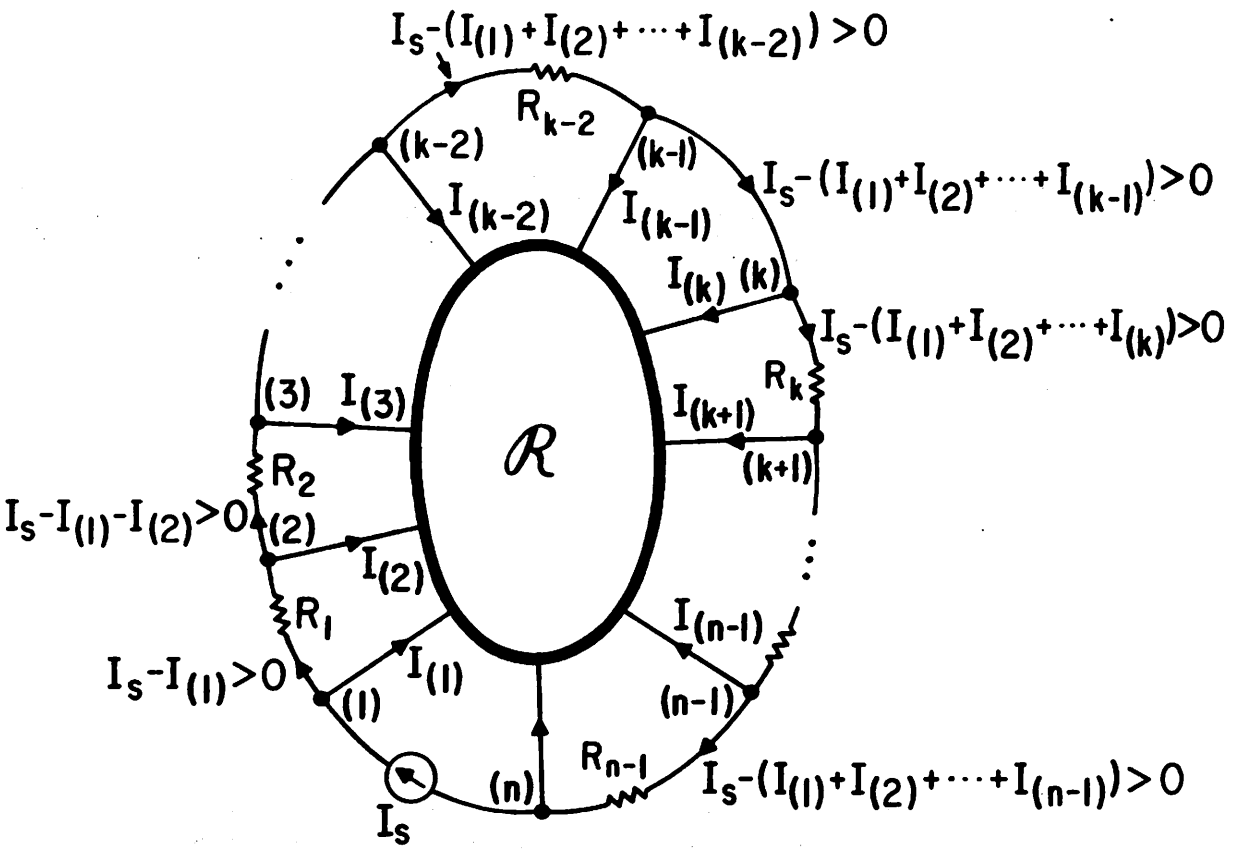

$I_s-(I_{(1)}+I_{(2)}+\cdots+I_{(k-2)})>0$
R_{k-2}
(k-2)
(k-1)
$I_s-(I_{(1)}+I_{(2)}+\cdots+I_{(k-1)})>0$
$I_{(k-2)}$
$I_{(k-1)}$
$I_{(k)}$ (k)
$I_s-(I_{(1)}+I_{(2)}+\cdots+I_{(k)})>0$
R_k
(3) $I_{(3)}$
$I_{(k+1)}$
$\mathcal{R}$
(k+1)
R_2
$I_s-I_{(1)}-I_{(2)}>0$
(2)
$I_{(2)}$
R_1
$I_{(n-1)}$
$I_s-I_{(1)}>0$
$I_{(1)}$
(1)
(n-1)
R_{n-1}
(n)
$I_s-(I_{(1)}+I_{(2)}+\cdots+I_{(n-1)})>0$
I_s
$I_s>|I_{(1)}|+|I_{(2)}|+\cdots+|I_{(n-1)}|$

Fig. A-2

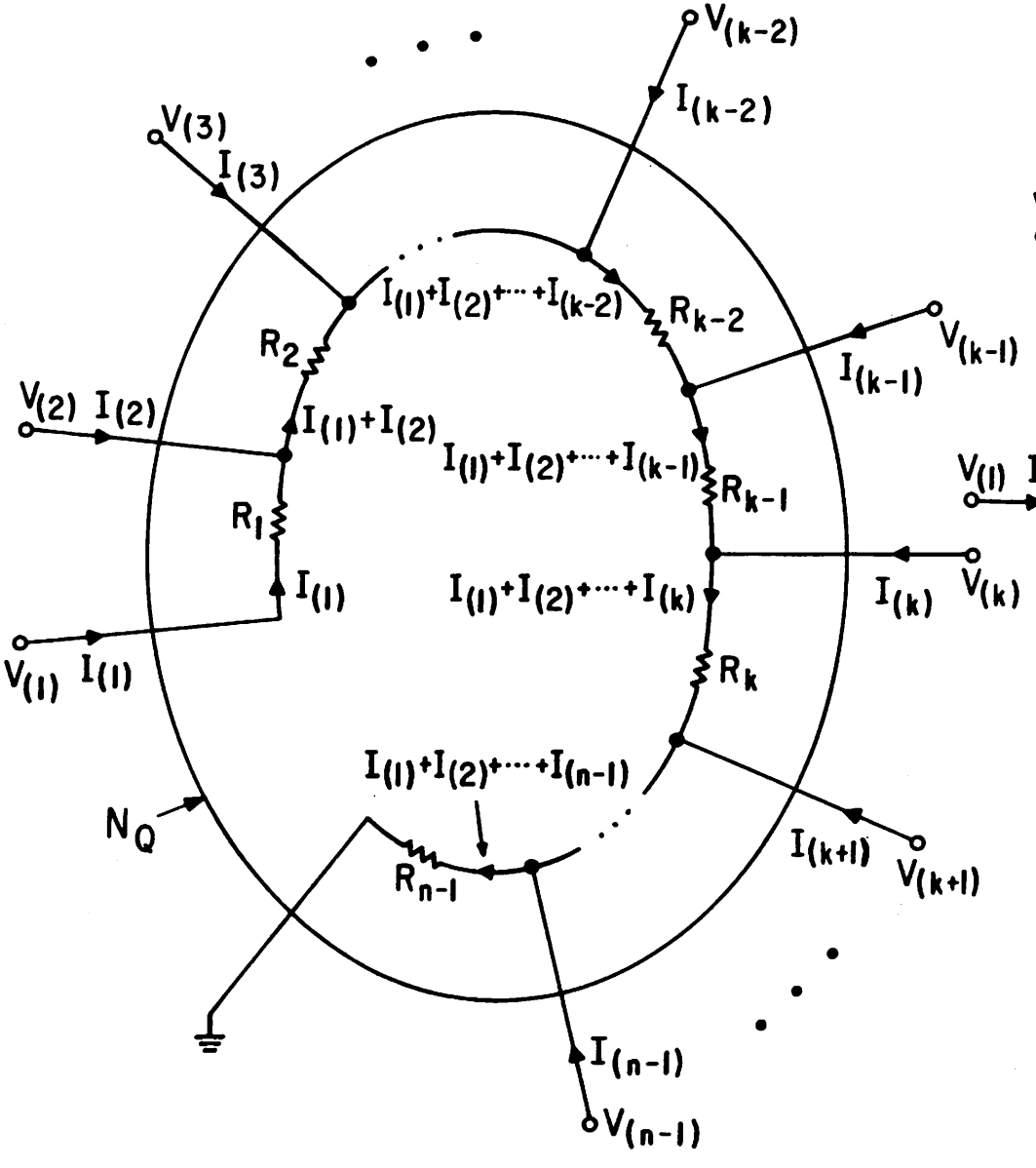

V(k-2)
I(k-2)
V(3)
I(3)
I(1)+I(2)+···+I(k-2)
R k-2
R 2
V(k-1)
I(k-1)
V(2) I(2)
I(1)+I(2)
I(1)+I(2)+···+I(k-1)
R k-1
R 1
I(1)
I(1)+I(2)+···+I(k)
I(k)
V(k)
R k
V(1) I(1)
I(1)+I(2)+···+I(n-1)
N Q
R n-1
I(k+1)
V(k+1)
I(n-1)
V(n-1)

Fig.A-3

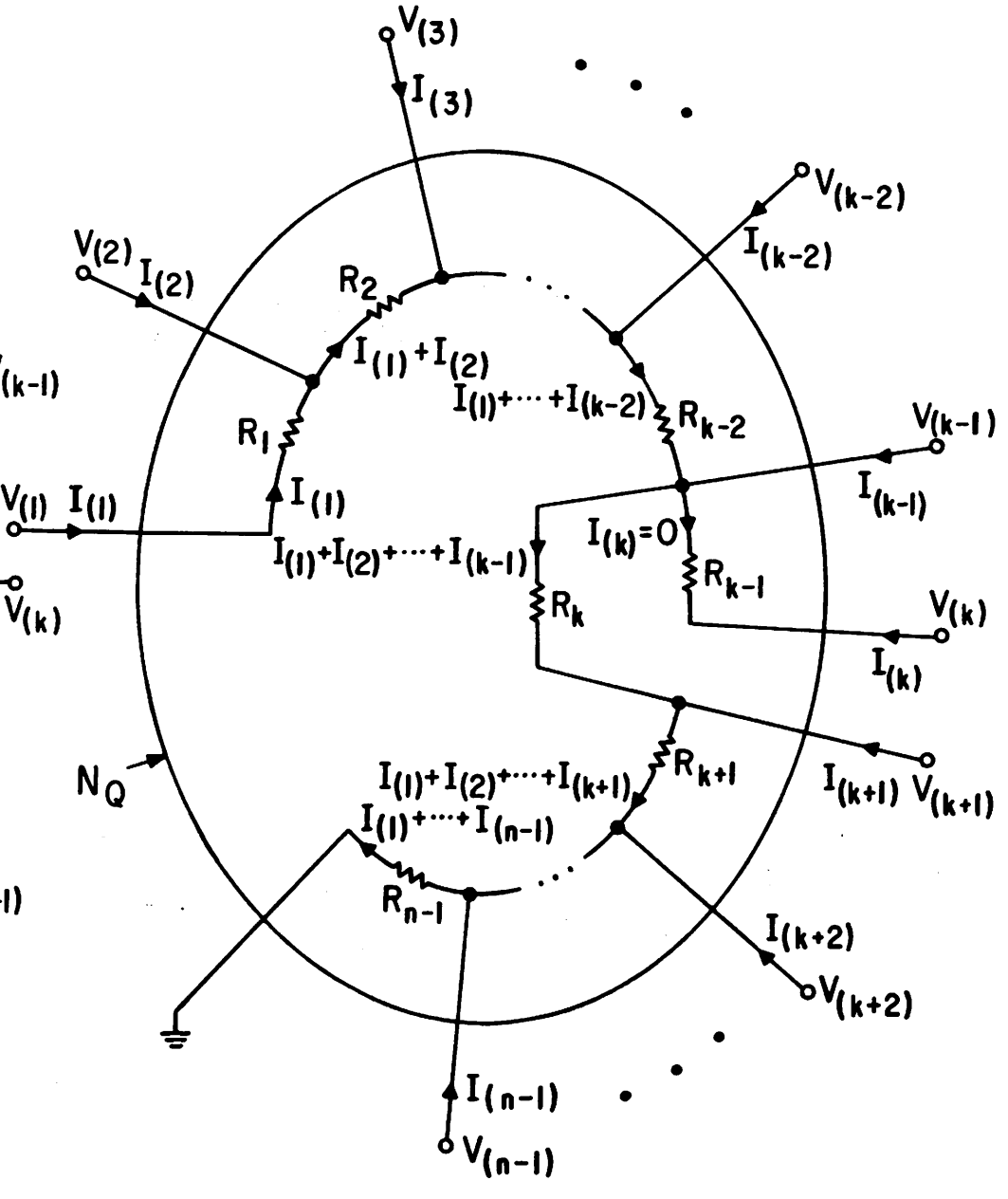

V(3)
I(3)
V(k-2)
I(k-2)
V(2) I(2)
R 2
I(1)+I(2)
I(1)+···+I(k-2)
R k-2
V(k-1)
I(k-1)
R 1
V(1) I(1)
I(1)
I(1)+I(2)+···+I(k-1)
I(k)=0
R k-1
V(k)
I(k)
R k
N Q
I(1)+I(2)+···+I(k+1)
R k+1
I(k+1) V(k+1)
I(1)+···+I(n-1)
R n-1
I(k+2)
V(k+2)
I(n-1)
V(n-1)

Fig. A-4

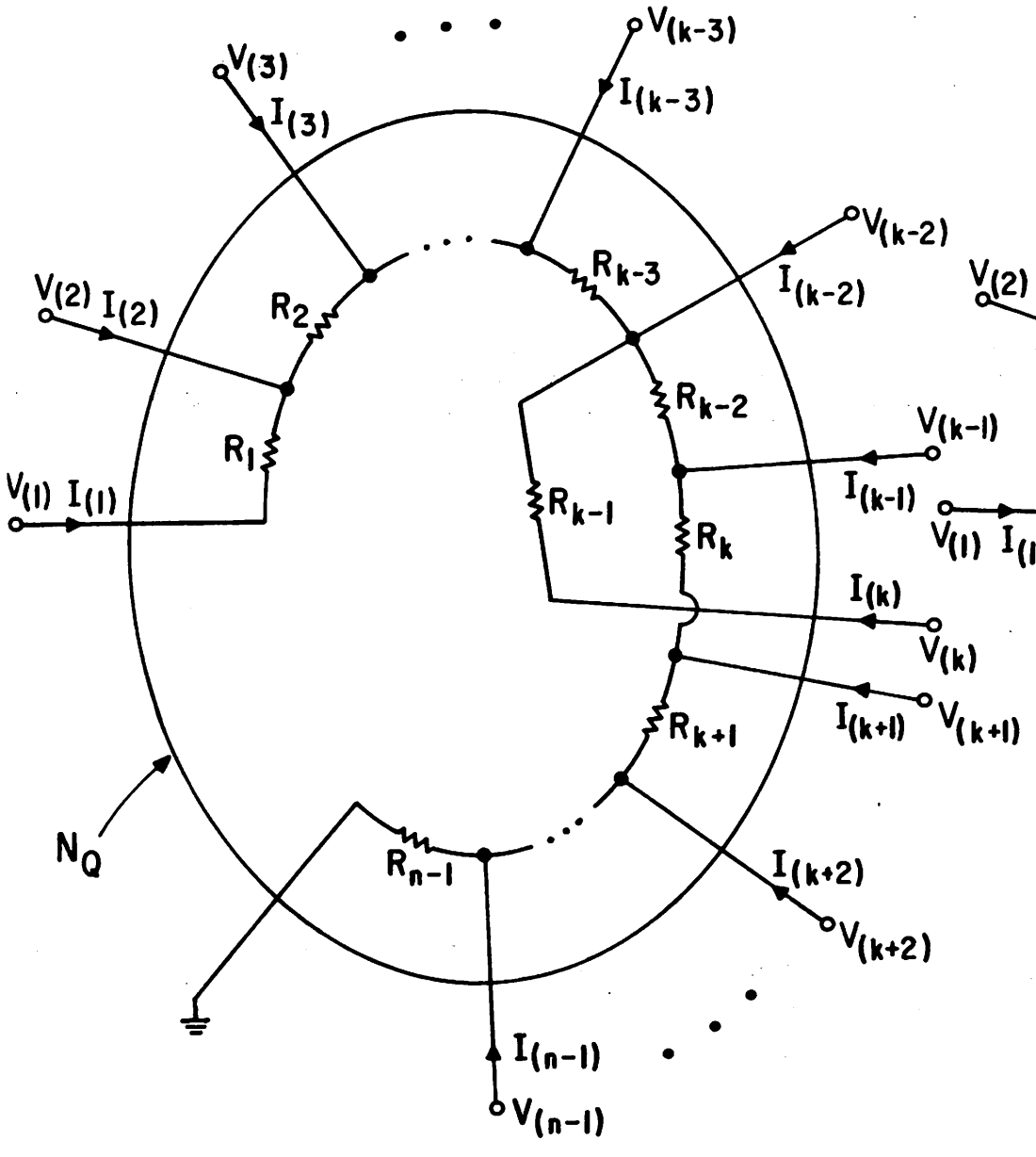

V(3)
I(3)
V(k-3)
I(k-3)
V(2) I(2)
R2
Rk-3
V(k-2)
I(k-2)
Rk-2
V(k-1)
R1
Rk-1
I(k-1)
V(1) I(1)
Rk
I(k)
V(k)
I(k+1)
V(k+1)
Rk+1
NQ
Rn-1
I(k+2)
V(k+2)
I(n-1)
V(n-1)

Fig. A-5

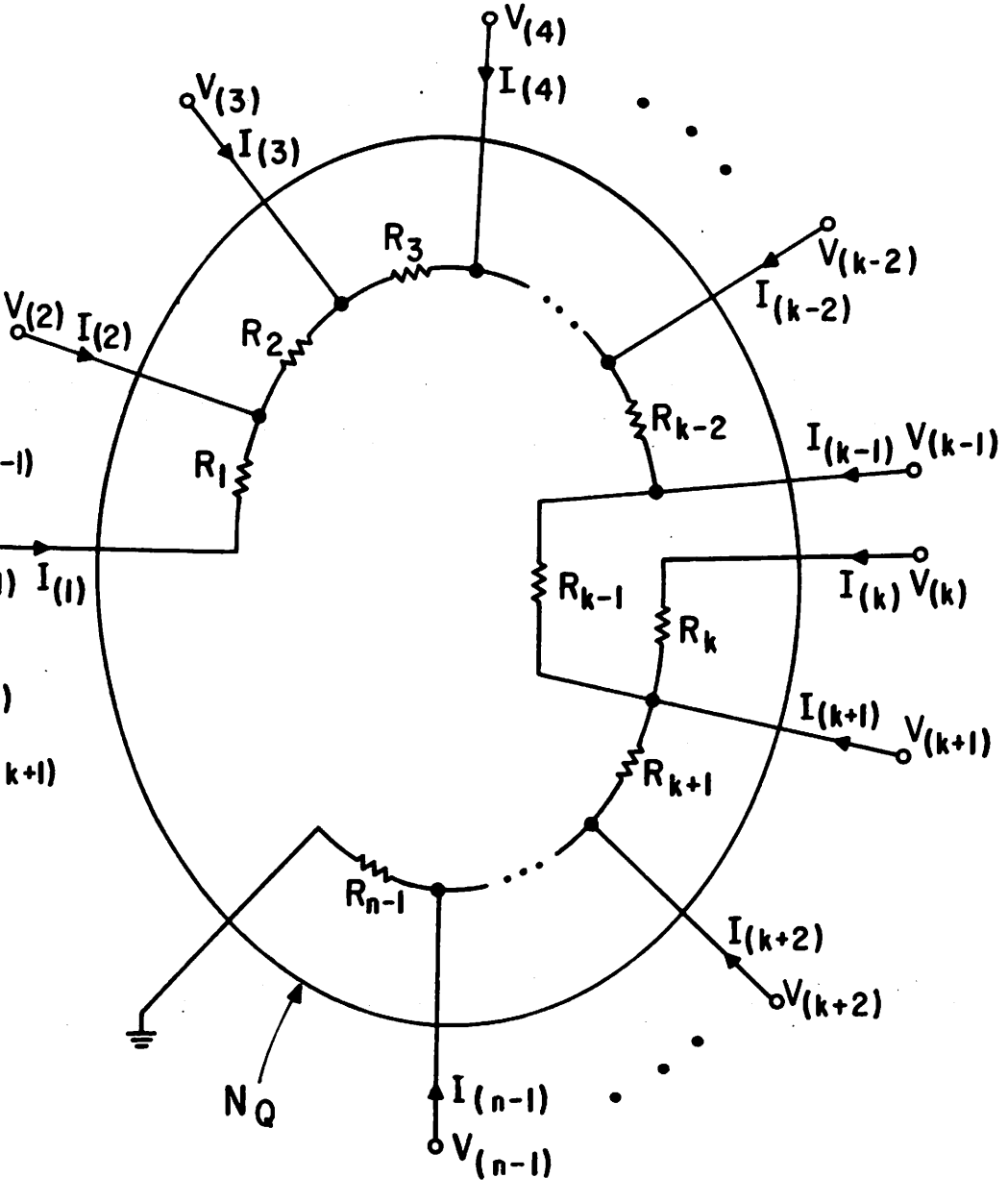

V(4)
I(4)
V(3)
I(3)
R3
V(k-2)
I(k-2)
V(2) I(2)
R2
Rk-2
I(k-1) V(k-1)
R1
V(1) I(1)
Rk-1
I(k) V(k)
Rk
I(k+1)
V(k+1)
Rk+1
Rn-1
I(k+2)
V(k+2)
NQ
I(n-1)
V(n-1)

Fig. A-6

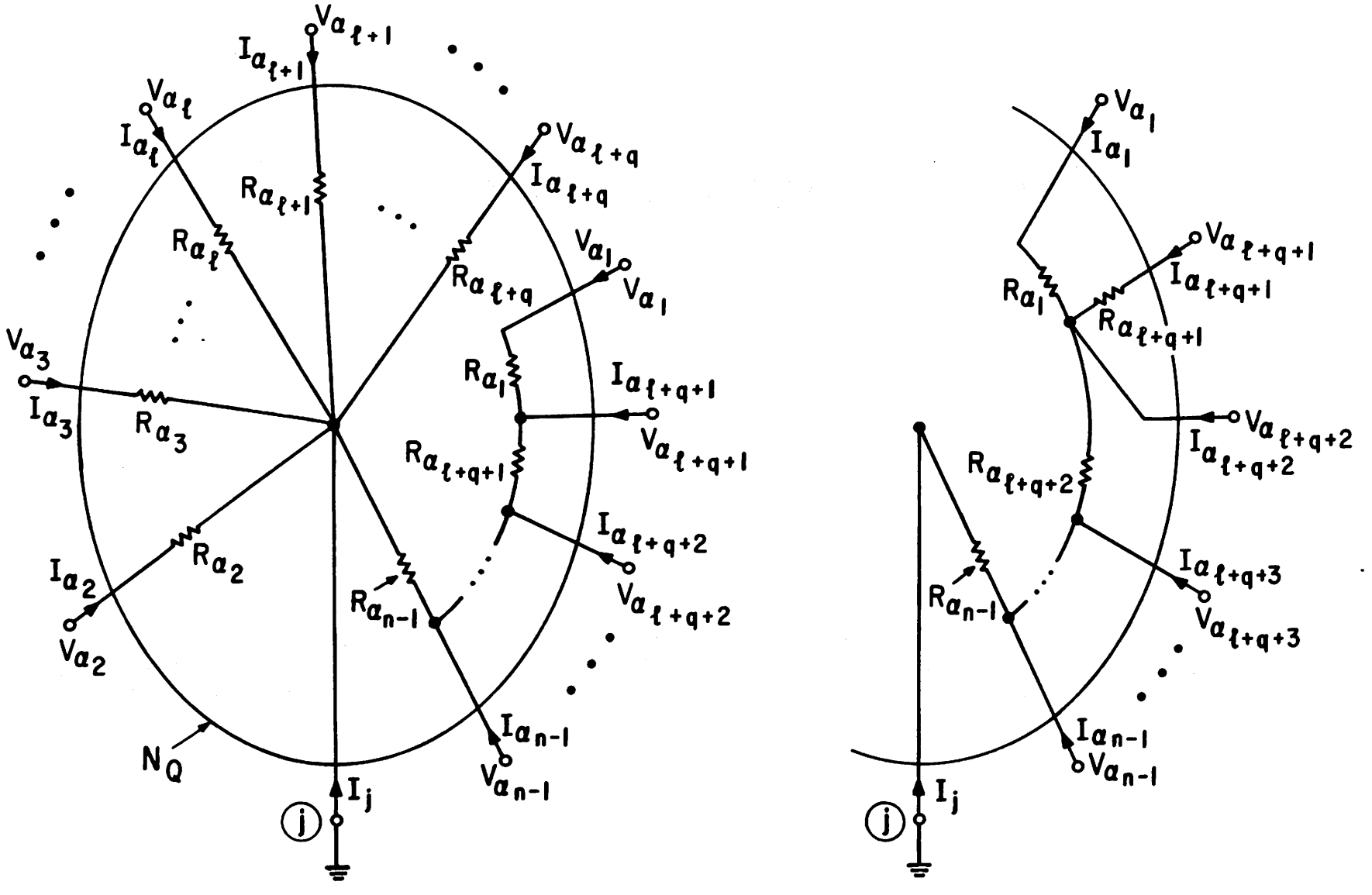
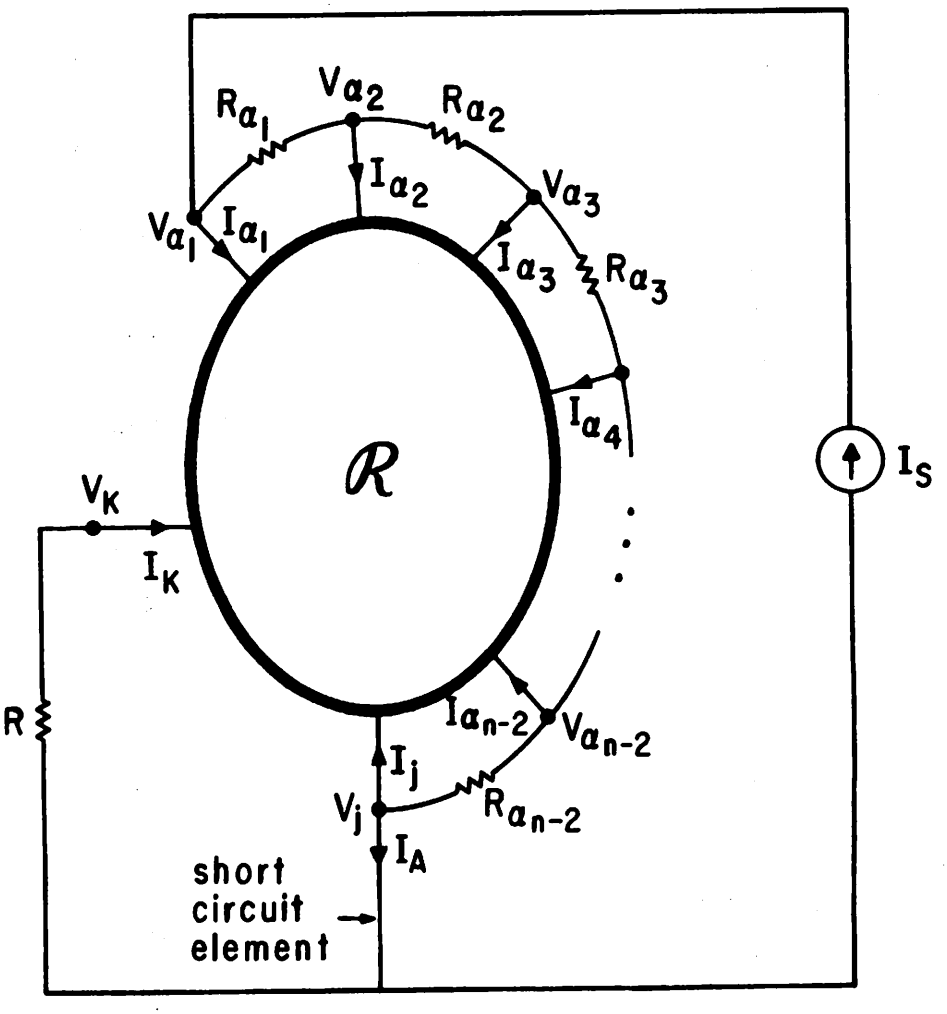

$V_{\alpha_{\ell+1}}$
$I_{\alpha_{\ell+1}}$
V_{α_ℓ}
I_{α_ℓ}
$R_{\alpha_{\ell+1}}$
$V_{\alpha_{\ell+q}}$
$I_{\alpha_{\ell+q}}$
R_{α_ℓ}
$R_{\alpha_{\ell+q}}$
V_{α_1}
V_{α_3}
I_{α_3}
R_{α_3}
R_{α_1}
$I_{\alpha_{\ell+q+1}}$
$V_{\alpha_{\ell+q+1}}$
$R_{\alpha_{\ell+q+1}}$
$I_{\alpha_{\ell+q+2}}$
$V_{\alpha_{\ell+q+2}}$
I_{α_2}
R_{α_2}
$R_{\alpha_{n-1}}$
V_{α_2}
$I_{\alpha_{n-1}}$
$V_{\alpha_{n-1}}$
N_Q
I_j
j
(a)
V_{α_1}
I_{α_1}
$V_{\alpha_{\ell+q+1}}$
$I_{\alpha_{\ell+q+1}}$
R_{α_1}
$R_{\alpha_{\ell+q+1}}$
$V_{\alpha_{\ell+q+2}}$
$I_{\alpha_{\ell+q+2}}$
$R_{\alpha_{\ell+q+2}}$
$I_{\alpha_{\ell+q+3}}$
$R_{\alpha_{n-1}}$
$V_{\alpha_{\ell+q+3}}$
$I_{\alpha_{n-1}}$
$V_{\alpha_{n-1}}$
I_j
j
(b)

Fig. A-7



$$R_{\alpha_j} = \frac{V_{\alpha_j} - V_{\alpha_{j+1}}}{I_{\alpha_j}} \quad , \quad j = 1, 2, \ldots, n-2$$

$$R = \frac{-(V_K - V_j)}{I_K} \quad , \text{ if } \quad (V_K - V_j) < 0$$

$$R = 0 \quad , \qquad \text{if} \quad (V_K - V_j) = 0$$

Fig. A-8

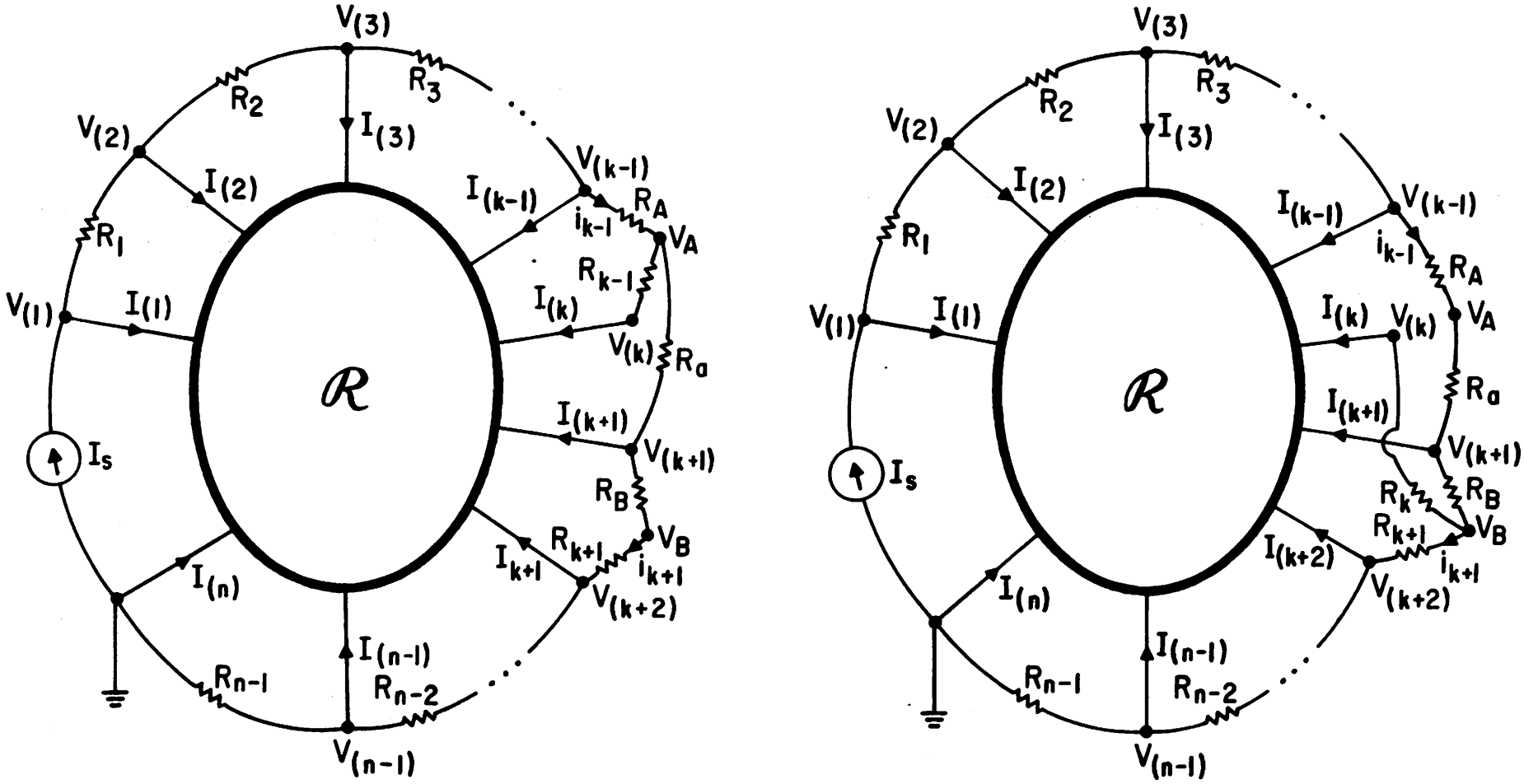

V(3)
R2
R3
V(2)
I(3)
I(2)
V(k-1)
I(k-1)
RA
ik-1
VA
R1
Rk-1
V(1)
I(1)
I(k)
V(k)
Ra
R
I(k+1)
V(k+1)
Is
RB
VB
Rk+1
ik+1
I(n)
Ik+1
V(k+2)
I(n-1)
Rn-1
Rn-2
V(n-1)
(a) I(k) > 0
(b) I(k) < 0

Fig. A-10

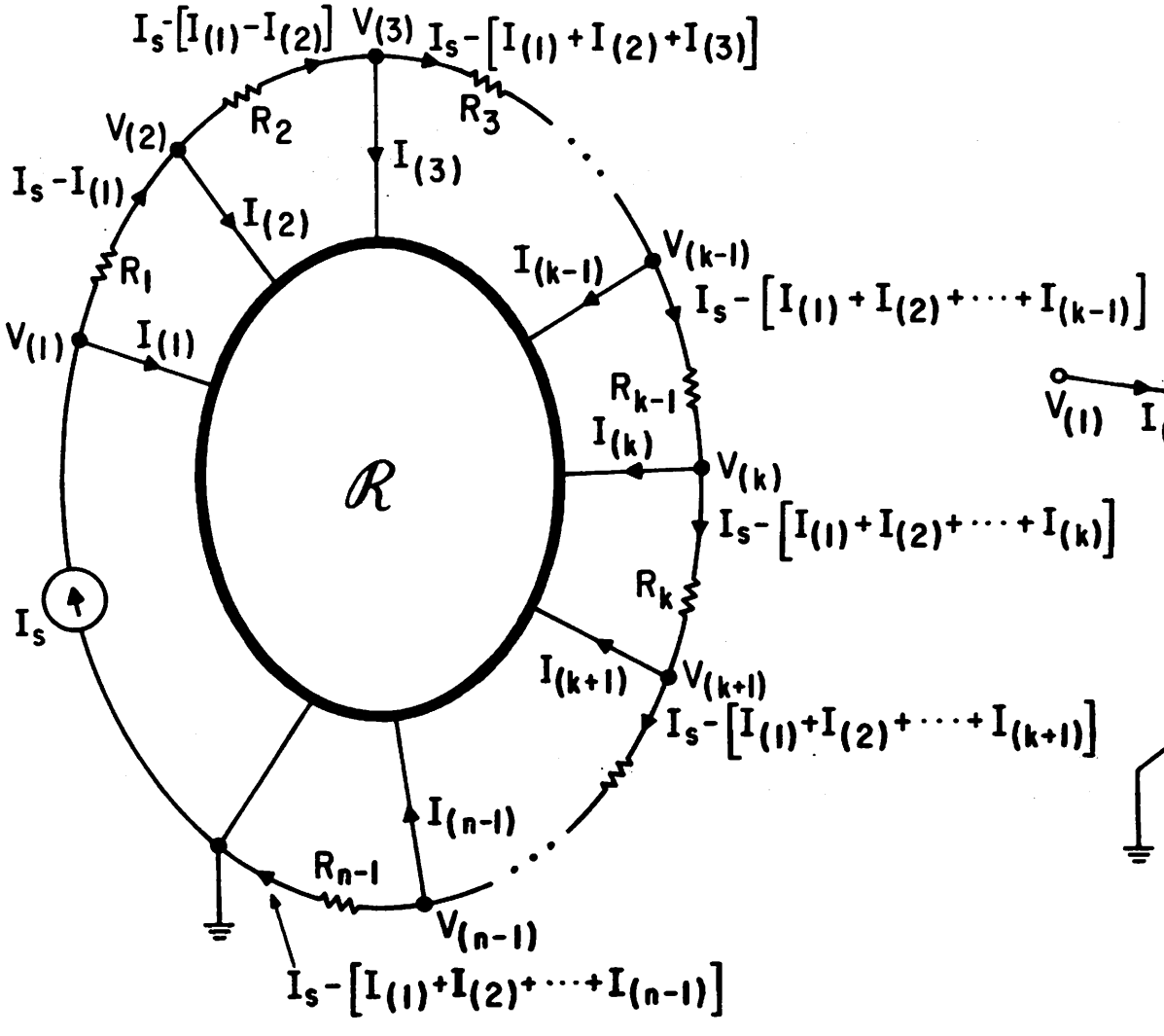


Fig. A-9

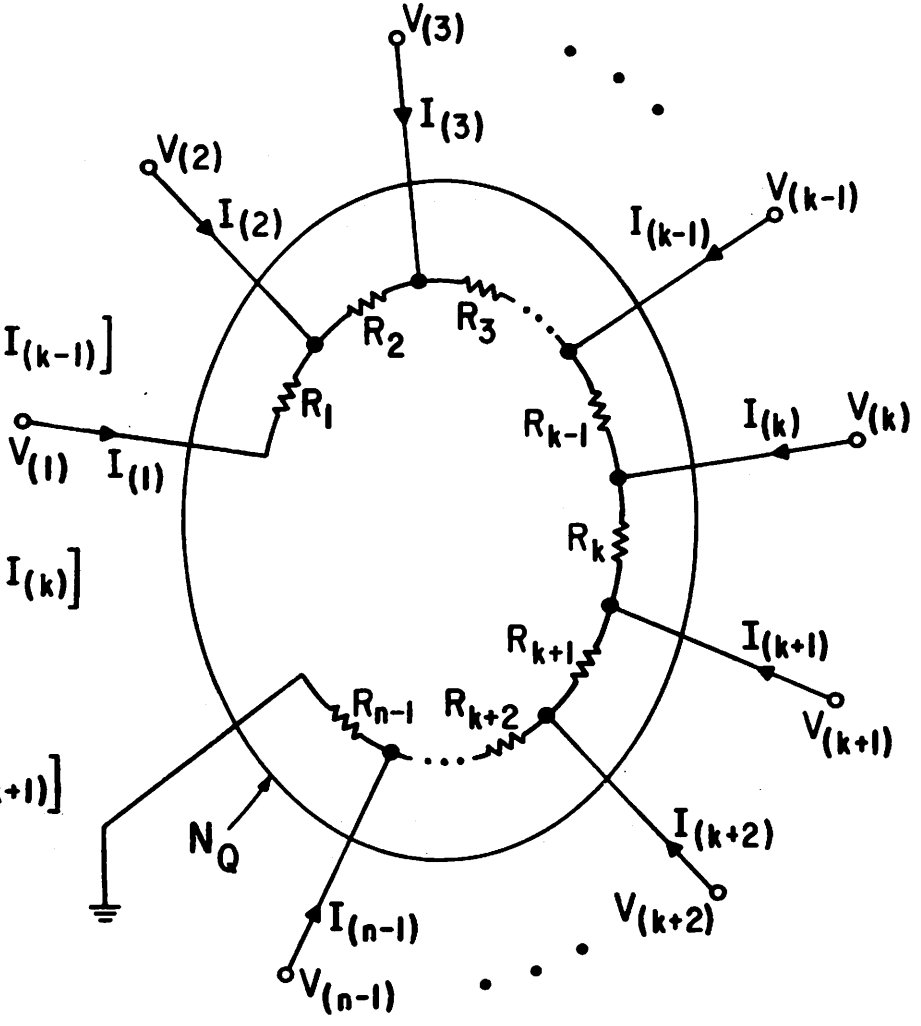


Fig. A-11