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AN IMPROVED VERSION OF SLIC



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ABSTRACT

SLIC is a computer program which simulates and analyses linear integrated circuits. SLIC performs the following four types of analyses: nonlinear dc analysis, linear small-signal analysis, noise analysis, and sensitivity analysis. The dc analysis computes the dc node voltages and the transistor operating points. The smallsignal analysis first generates linearized small-signal transistor models and then computes the poles and zeros and/or frequency response of a specified transfer function. The noise analysis computes the the equivalent thermal and shot noise sources and at five frequencies computes the noise at the output port. The sensitivity analysis computes the sensitivities (partial derivatives) of the transistor operating points and the specified transfer function (at five frequencies) with respect to specified passive circuit elements. In addition SLIC allows the temperature and a single dc source to be varied and also allows analyses of altered versions of the original circuit.

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I. INTRODUCTION

The SLIC (simulator for linear integrated circuits) program has undergone a number of modifications and additions since the original work of Idleman [1] [2] was completed. Larger circuits (up to 100 nodes) can be simulated and simulation times have been reduced with the implementation of sparse matrix techniques. Voltage-controlled current sources, mutual inductors, and junction and MOS field-effect transistor models have been added. The option to plot a specified dc voltage as a single source is varied (dc transfer curve) has been added. The provision to bypass the dc analysis and proceed directly into a small-signal analysis has also been included. The implementation of Muller's method which is used to compute poles and zeros has been modified to reduce pole-zero computation times. The optional noise analysis now computes the rms output port noise generated by each equivalent thermal and shot noise source at up to five user specified frequencies. Previously, only the total rms output noise was computed. An optional sensitivity analysis has been added which computes the sensitivities (partial derivatives) of the transistor junction voltages with respect to certain user specified passive circuit elements. At up to five user specified frequencies, the sensitivities of a defined transfer function with respect to the transistor small-signal parameters and the selected passive elements are also computed. The input data format has been modified to allow the use of keywords in the description of transistor

models. Of the above modifications and additions, William McCalla was responsible for implementing sparse matrix techniques, adding mutual inductors, modifying the implementation of Muller's method, and adding the sensitivity analysis.

The bipolar transistor model used in SLIC is described by McCalla [3]. The dc model is a nonlinear hybrid-pi equivalent of the Ebers and Moll transport model [4]. Incorporated in this model are basewidth modulation effects, a current-dependent short-circuit dc current gain β_F , high level injection effects, and temperaturedependent effects. A linear, small-signal hybrid-pi model is used for the small-signal analyses. The junction and MOS field-effect transistor models used are based on the insulated-gate field-effect transistor model of Shichman and Hodges [5] [11].

SLIC consists of approximately 5100 Fortran statements and has a field length of 41000 decimal words. It is capable of simulating and analyzing circuits of up to 100 nodes with the following limitations: 40 resistors, 20 capacitors, 20 inductors, 20 voltagecontrolled current sources, 10 mutual inductors, 30 bipolar and field-effect transistors, 10 bipolar transistor models, 10 fieldeffect transistor models, 10 current sources, and 10 grounded voltage sources.

II. USER'S GUIDE

This section contains the SLIC user's guide which describes the input data language and the various analysis options. An example is also included to illustrate circuit and analysis descriptions.

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WHEFE T IS THE TEMPERATURE OF INTEREST AND TOL AND TO2 ARE FIRST- AND SECOND-ORDER TEMPERATURE COEFFICIENTS, PESPECTIVELY. BIPCLAR TRANSISTOR JUNCTION SATURATION CURRENTS, CUTPUT CONDUCTANCE, TRANSIT TIME, AND JUNCTION CAPACITANCES ARE VARIED FOR BOTH LARGE AND SMALL-SIGNAL ANALYSES ACCORDING TO THE THEORETICALLY DERIVED RELATIONSHIPS FOR SILICON TRANSISTORS.

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INFUT DATA FORMAT.

THE INPUT DATA FORMAT OF SLIC IS OF THE FREE FORMAT TYPE. FIELDS ON A CARD ARE SEPARATED BY ONE OR MORE DELIMITERS. BLANKS, COMMAS, EQUAL SIGNS, LEFT PAPENTHESES, AND RIGHT PARENTHESES ARE ALL DELIMITERS.

ALL CARDS MUST REGIN WITH A NAME FIELD STARTING IN COLUMN 1, WITH THE EXCEPTION OF TITLE CARDS, COMMENT CARDS, AND CONTINUATION CARDS.

A NAME FIELD MUST CONTAIN FROM ONE TO FOUR CHARACTERS. ANY TRAILING CHARACTERS ARE IGNORED. THE FIRST CHARACTER OF A NAME FIELD MUST BE A LETTER AND ONLY CERTAIN LETTERS WHICH ARE DESCRIBED BELOW IN THE GUIDE MAY BE USED. THE REMAINING (UP THI THREE) CHARACTERS MAY BE COMPOSED OF ANY COMBINATION OF ALPHANUMERIC CHARACTERS EXCEPT DELIMITERS.

A NUMERIC FIELD MAY BE AN INTEGER FIELD (12, -44), A FLOATING POINT FIELD (3.14159), EITHER AN INTEGER OR A FLOATING POINT NUMBER FOLLOWED BY AN INTEGER EXPORENT (1E-14, 2.65E0), OR EITHER AN INTEGER OR A FLOATING POINT NUMBER FOLLOWED BY ONE OF THE FOLLOWING SCALE FACTORS -

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к	1.0E+3	
M	1.02-3	<u> </u>
U	1.02-6	
N	1.02-9	
Р	1.02-12	

ANY LETTERS IMMEDIATELY FOLLOWING A NUMBER THAT ARE NOT SCALE FACTORS ARE IGNORED, AND ANY LETTERS IMMEDIATELY FOLLOWING A SCALE FACTOR ARE IGNORED. HENCE 10, 10V, LOVOLTS, AND 10HZ ALL REPRESENT THE SAME NUMBER, AND M, MA, MSEC, AND MMHDS ALL REPRESENT THE SCALE FACTOR M. NOTE THAT 1000, 1000.0, 100CHZ, 1E3, 1.0E3, 1KHZ, AND 1K ALL REPRESENT THE SAME NUMBER. VALUES IN NUMERIC FIELDS MAY BE DEFAULTED BY A SLASH, /, AND DELIMITERS NEED NOT RE USED RETWEEN SUCCESSIVE SLASHES. FOR EXAMPLE, THE GROUP OF NUMBER FIELDS (10K//9.6U) IS EQUIVALENT TO (10K 0.0 0.0 9.6U).

CONTINUATION CARDS ARE BEGUN WITH A PLUS, +, IN COLUMN 1 AND MAY BE USED IN DESCRIBING TRANSISTOR MODELS, VARIABLE CURRENT SOURCES, AND VARIABLE GROUNDED VOLTAGE SOURCES.

THE FIRST CARD OF AN INPUT DECK MUST BE A TITLE CAFD AND THE LAST CARD AN END CARD. THE ORDER OF ALL OTHER CARDS IS ARBITHARY.

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	CENTROL CARDS
	1) TITLE CARD A CARD WHOSE CONTENTS ARE PRINTED OUT VERBATIM AT THE HEAD OF EACH SECTION OF OUTPUT.
	EX1MPLE -
	SOLOMON AND WILSON SERIES-SERIES TRIPLE BROADBAND AMPLIFIER
	2) COMMENT CARDS CAROS (CFTICMAL) WHOSE CONTENTS ARE PRINTED OUT VEPRATIM WHEN READ.
	EXAMPLE -
	* GPEN LOOP NO FEEDBACK
	COLUMN 1 MUST CONTAIN AN ASTERISK, *. THE FEST OF THE CARD MAY CONTAIN ANY COMMENTS.
	3) PRINT CARD A CARD WHICH SPECIFIES THE TYPE OF CC AND/OR SMALL-SIGNAL ANALYSIS DESIRED.
	GENERAL FORM -
	PRINT DEMODE ACMODE VAR(PTS, FMIN, FMAX) OUTPUT(NO+, NO-) INPUT(NI+, NI-)
	EXAMPLES -
-	PRINT CC PZ FLOG(10,1HZ,100MFGHZ) VOUT(7,0) IIN(1,C) PRINT AC FLIN 10 95KHZ 105KHZ VOUT 15 0 VIN 2 C PRINT DC
	DCMODE IS THE LETTERS DC IF A DC ANALYSIS IS DESIRED OR BLANK IF NONE IS DESIRED.
	ACMODE IS THE LETTERS PZ IF POLES AND ZEROS (WITH OR WITHOUT A FREQUENCY FESPONSE) ARE DESIRED, THE LETTERS AC IF ONLY A FREQUENCY RESPONSE IS DESIRED, OR BLANK IF NEITHER IS DESIRED.
	IF ACMODE IS PZ TWO OPTIONAL NUMERIC FIELDS MAY IMMEDIATELY FOLLOW THE LETTERS PZ. THE FIRST NUMERIC FIELD IS THE UPPER FREQUENCY LIMIT FOR POLES AND THE SECOND NUMERIC FIELD IS THE UPPER FREQUENCY LIMIT FOR ZERDS. THESE LIMITS ARE SPECIFIED IN HERTZ. THE EITHER NO POLES OR NO ZEROS ARE DESIRED. THE NUMBER O (2000) SHOULD BE SPECIFIED. THE SPECIFICATION OF A / (SLASH) WILL CAUSE ALL POLES OR ZERDS TO BE FOUND.
	THE VAR SPECIFICATIONS MUST BE PRESENT IF ACMODE IS AC. IF ACMODE IS PZ AND A FREQUENCY RESPONSE IS ALSO DESIRED, THEN THE VAR SPECIFICATIONS SHOULD BE PRESENT. TWO TYPES OF FREQUENCY VARIATION ARE ALLOWED. VAR IS THE LETTERS FLOG FOR A LOGARITHMIC VARIATION AND PTS IS THE NUMBER OF FREQUENCY POINTS PER

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18WPE RATURE OF 299 026REES. DEGREES. IN THE SECTIND EXAMPLE, ONLY ONE ANALYSIS IS PERFORMED AT THE NOMINAL TEMPERATURES AT WHICH THE CIRCUIT IS TO BE EVELYZED. IN THE FIRST EXAMPLE ABOVE, THEM IS 300 DEGREES AND THE CIRCUIT IS AVELYZED AT 300, 305 AND 310 THOM IS THE NOMIMAL TEMPERATURE. TI, T2, T3, T4, AND IS ARE THE UP TO FIVE) 568 TEMP TEMP 303 3CC 3CS 3LO 9 - SEIGHAXE SI VI EL ZI II WONI dWAI Ż - WEDE TVEENED TEMPERATURE SPECIFIED ON ITS #TRANSISTCR CARD*. THIS TEMPERATURE. THIS CARD HAS NO EFFECT ON A TRANSISTUR WHICH HAS A 7 IF ONLY THE WOMINAL TEMPERATURE IS SPECIFIED, A SUNCLE ANALYSIS IS PERFORMED AT ANIVIES 2393030 005 40 BRUTABERKET JANIMON GEMILSEA EHT TA GEMEGREG SI SISYJANA TEMPERATURES ARE SPECIFIED IN DEGREES KELVIN. IF THIS CARD IS CMITTED, AN TURE AND UP TO FIVE TEMPERATURES AT WHICH THE CIFCUIT IS TO RE ANALYZED.) TEMPERATURE CARD -- A CARC (OPTICAEL) WHICH SPECIFIES THE NOWINAL TEMPERA-(5) SP ONA IN INCREMENT. ONAME IS THE NAME OF THE OUTPUT VOLTAGE WHICH EXISTS BETWEEN NODES) THE INITIAL SOURCE VALUE, STOP IS THE FINAL SCURCE VALUE, AND STEP IS THE SOURCE THEY ALSO BE SPECIFIED ON A #VOLTAGE OR CUPRENT SOURCE CARD#. START IS SNAME IS THE AAME OF THE VOLTAGE OR CURRENT SCURCE THAT IS VARIED. SIHT DC II 0.0 144 1001 441 0.0 11 30 0 L 100A AK0+ S*0+ S*0- SA 00) - SJIGHAXE DC SNAME START STOP STEP ONAME VI N2) - WADE JAFENSO SOURCE IS VARIED. THE NUMBER CF POINTS FLOTTED CANNOT EXCEED 101. CUPVE. A SPECIFIED DC OUTPUT VOLIAGE IS PLOTTED AS A SINGLE VCLIAGE OR CURRENT `) 4) DC CVED -- V CVED (JETICAAL) WHICH SPECIFIES THE PLUTTING DF A DC TRANSFER) 6 ARE THE POSITIVE AND NEGATIVE INPUT NODES, RESPECTIVELY. -IN ONA +IN ONA TURNI TNERRUD FOR UIL ERTER THE AD TURNI RADIN POR NIV [THE DUSTINE AND NECKINE COLDAL NODES' EESPECTIVELY. INPUT IS THE LETTERS FUNCTION FOR POLES AND ZEROS AND/OR FREQUENCY RESPONSE. OUTPUT IS THE LETTERS VOLTER POLES AND NO+ AND NO- YOUTPOL POLED AND YOU FOR YOU) THE OUTPUT AND INPUT SPECIFICATIONS SPECIFY THE TRANSFER OR DRIVING PCINT POINTS STARTING WITH FMIN AND ENDING WITH FMAX. 5 12 THE LETTERS FLIN FOR A LINEAR VAPIATION AND PIS IS THE WUNBER OF FREDUENCY EWIN IS THE STARTING FROUTNEY AND EMAX IS THE FINAL FPEDENCY. 4Vh • EGADE•

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	ELEMENT CARDS
	1) RESISTOR, CAPACITOR, AND INDUCTOR CARDS
	GENERAL FORM -
	PXXX N1 N2 VALUE TC1 TC2 VAP CXXX N1 N2 VALUE TC1 TC2 VAR LXXX N1 N2 VALUE TC1 TC2 VAR
	EXAMPLES -
•	P1 01 21 300K 2.0F-3 C1 01 00 12.0P // V LZRD 02 10 0.000001
	THE FIRST FIELD MUST CONTAIN AN ELEMENT NAME THAT BEGINS WITH THE LETTER R FOR RESISTOR CARDS, C FOR CAFACITOR CARDS, AND L FOR INDUCTOR CARDS. NI AND N2 APE THE NODES OF THE ELEMENT. VALUE IS THE NOMINAL RESISTANCE IN OHMS FOR RESISTOR CARDS, NOMINAL CAPACITANCE IN FARADS FOR CAPACITOB CARDS.
	AND NOMINAL INDUCTANCE IN HENRIES FOR INDUCTOR CAPDS. VALUE CANNOT BE ZERD OR MEGATIVE. TOI AND TO2 ARE THE FIRST- AND SECOND-ORDER TEMPERATURE
· ·	COEFFICIENTS, PESPECTIVELY. UNSPECIFIED TEMPERATURE COEFFICIENTS ARE ASSUMED TO BE 0.0. VAR IS AN OPTIONAL FIELD USED TO SPECIFY A SENSITIVITY ANALYSIS VARIABLE. IF VAR IS THE LETTER V AND A #SENS CARD# IS INCLUDED IN THE DATA
	DECK, SENSITIVITIES (PARTIAL DERIVATIVES) WITH RESPECT TO THE SPECIFIED ELEMENT WILL BE PERFORMED.
	2) VOLTAGE-CONTROLLEC CURRENT SOURCE CARDS
•	GENERAL FORM -
	GXXX N+ N- NC+ NC- VALUE TC1 TC2 VAP
	EXAMPLE -
	GM2 7 0 3 0 3M 2E-3
3	GXXX IS THE VOLTAGE-CONTROLLED CURRENT SOURCE NAME WHICH MUST BEGIN WITH THE LETTER G. N+ AND N- ARE THE POSITIVE AND NEGATIVE MODES, RESPECTIVELY, OF THE CONTROLLED SOURCE. A POSITIVE CURRENT FLOWS FROM N+ THROUGH THE SOURCE TO N NC+ AND NC- ARE THE POSITIVE AND NEGATIVE CONTROLLING NODES, RESPECTIVELY. VALUE IS THE NOMINAL TRANSCONDUCTANCE IN MHOS. TOI AND TOZ ARE THE FIRST- AND SECOND-ORDER TEMPERATURE COEFFICIENTS, PESPECTIVELY. UNSPECIFIED TEMPERATURE COEFFICIENTS ARE ASSUMED TO BE 0.0. VAP IS AN OPTIONAL FIELD USED TO SPECIFY A SENSITIVITY ANALYSIS VARIABLE. IF VAR IS THE LETTER V AND A #SENS CARD# IS INCLUDED IN THE DATA DECK, SENSITIVITIES (PARTIAL DERIVATIVES) WITH RESPECT TO THE SPECIFIED ELEMENT WILL BE PERFORMED.
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	•★CAAD ERUTAREGMET★ EHT NO DELEIDEGE ZA
	HELD. IF OMITTED, THE TRANSISTOR WILL BE ALLOWED TO FOLLOW THE TEMPERATURES
	TEMP IS THE TEMPERATURE IN DEGREES KELVIN AT WHICH THE FRANSISTOR IS TO BE
	•CXB1212NAN1
	ED& ADLY VER VS20480° CO& VAD ADLY AVE ADL SPECIFIED FOR FIELD-EFECT
	SAALL-SIGNAL PARAMETERS. JE DEFAULTED, VALUTS OF 0.1 MA FOR CUR AND 1.0 VLLI
	BYPASSED, THESE VALUES WILL BE USED AS THE OPERATING POINT TO GENERATE THE
-	AND COLLECTOR-EMITTER JUNICTION VOLTAGE, RESPECTIVELY. IF THE CC ANALYSIS IS
	FOR BIPOLAR TRANSISTOFS, CUP AND VOLT ARE VALUES OF THE COLLECTOR CURRENT
	10000 TUH 000 UNH 100
	ערבי עמש עדע אסג מטווטו בט האייאררכרי מבמרבי במעי אסו המראי ועממסוסומיי עם אות ער אים האראנת אמור בי אסא
	TAPELIES THAT THE TRANDISTICALE THE TUDGE TO A RELET OF SEVENCES IN Districts - Denies a stories of the transferes of and of add the vences of 1964.
-	TH DEFAULIED A VALUE UP 1.0 15 F550% AN AREA FACIUM OF 2.0 FUX EXAMPLET
	ABGAF IS THE AREA FACTOR THAT IS TO BE USED WITH THE TRANSIER WODEL.
	TRANSISTOR MODEL.
	LETTER & FOR A RIPOR COMMECTER TRANSICIAL MELE LETTER F FOR A FIELD-EFFECT
	HI HIM NIGHT IS THE HALF AND LEGENDE WAR WILL BEEN WILL BEEN MILLE THE BEEN WILL BEEN WILL BEEN WILL BE AND
	NODE.
	NODE, NZ IS THE CATE NODE, N3 IS THE SCURCE NODE, AND W. IS THE SUBSTRATE (BULK)
	AND NA IS NOT SPECIFIED. FOR MOS FIELD-BFEET TPANSISTORS, WE IS THE DRAIN
	THANSISTARS. NI IS THE DRAIN NODE, NS IS THE GATE NODE, N3 IS THE SOURCE NODE,
	US IS THE EMITTER NODE, AND NA IS NOT SPECIFIED. FOR JUNCTION FIELD-EFECT TRANSISTORS, NI IS THE DRAIN NODE, NS IS THE GATE NODE, N3 IS THE SQUACE NODE,
-	FOR BIPOLAR TRANSISTORS, NI IS THE COLLECTOR NODE, NZ IS THE BASE NODE, NJ IS THE ENITTER NODE, AND N4 IS NOT SPECIFIED. FOR JUNCTION FIELD-EFFECT TRANSISTORS, NI IS THE DRAIN NODE, NZ IS THE GATE NODE, NJ IS THE SOURCE NODE,
-	AXXX IS THE TRANSISTOR NAME WHICH MUST BEGIN WITH THE LETTER Q. For bipolar transistors, al is the collector wode, as is the base wode, w3 is the emitter wode, and up is und specific. For Junction Field-Effect transistors, al is the drain wode, as is the gate wode, as is the source wode,
	AXXX IS THE TRAMSISTOR NAME WHICH MUST BEGIN WITH THE LETTER Q. For bipolar transistors, NL IS the collector wode, N2 IS the base wode, N3 IS the emitter wode, Jud N4 IS wot specified. For Junction Field-Effect Transistors, NL IS the drain wode, N2 IS the gate wode, W3 IS the source wode,
	OSS IL LOO FROS 2 AXXX IS THE TRANSISTOR NAME WHICH MUST BEGIN WITH THE LETTER Q. For bipolar transistors, NL IS the collector wode, N2 is the base wode, N3 IS THE ENTITER NODE, JUD NA IS WOT SPECIFIEC. FOR JUNCTION FIELD-EFFECT TRANSISTORS, NL IS THE DRAIN WODE, N2 IS THE SQUACE WODE, TRANSISTORS, NL IS THE DRAIN WODE, N2 IS THE SQUACE WODE,
	010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 9XXX IS THE TRANSISTOR NAME WHICH MUST BEGIN WITH THE LETTER Q. FOR BIPOLAR TRANSISTOR NAME WHICH MUST BEGIN WITH THE LETTER Q. N3 IS THE EMITTER NODE, AND N4 IS NOT SPECIFIED. FOR JUNCTION FIELD-EFFECT TRANSISTORS, NJ IS THE DRAIN NODE, NZ IS THE SQUACE NODE, TRANSISTORS, NJ IS THE DRAIN NODE, NZ IS THE SQUACE NODE,
	05 7 6 3 BNS 2 14A 3.0 010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 025 11 1 0 0 FMCS 2 03 15 THE TRAWSISTOR NAME WHICH MUST BEGIN WITH THE LETTER 0. FOR BIPOLAR TRAWSISTOR NAME WHICH MUST BEGIN WITH THE LETTER 0. 13 15 THE EWITTER NODE, AND N4 15 NOT SPECIFIED. FOR JUNCTION FIELD-EFFECT 15 THE EWITTER NODE, AND N4 15 NOT SPECIFIED. FOR JUNCTION FIELD-EFFECT 15 THE EWITTER NODE, AND N4 15 NOT SPECIFIED. FOR JUNCTION FIELD-EFFECT 15 THE EWITTER NODE, AND NCDE, N2 15 THE GATE NODE, N3 15 THE SQUACE NODE, 15 THE EWITTER NODE, ALL NODE, N2 15 THE GATE NODE, N3 15 THE SQUACE NODE, 16 ANSISTORS, N1 15 THE DRAIN NCDE, N2 15 THE GATE NODE, N3 15 THE SQUACE NODE,
	EXAMPLES - OS 7 6 3 BNS 2 14A 3.0 OS 7 6 3 BNS 2 14A 3.0 FOR BIPOLAR TRANSISTOR NAME WHICH MUST BEGIN WITH THE LETTER Q. FOR BIPOLAR TRANSISTOR NAME WHICH MUST BEGIN WITH THE LETTER Q. NJ 15 THE EMITTER NODE, NU 15 THE COLLECTOR NODE, NZ 15 THE BASE NODE, TRANSISTORS, NI 15 THE DRAIN NCDE, NZ 15 THE SQUACE NODE, TRANSISTORS, NI 15 THE DRAIN NCDE, NZ 15 THE SQUACE NODE,
	EXAMPLES - OS 7 6 3 BNS 2 14A 3.0 OS 7 6 3 BNS 2 14A 3.0 FOR BIPOLAR TRANSISTOR NAME WHICH MUST BEGIN WITH THE LETTER O. FOR BIPOLAR TRANSISTOR NAME WHICH MUST BEGIN WITH THE LETTER O. FOR BIPOLAR TRANSISTOR NAME WHICH MUST BEGIN WITH THE LETTER O. TRANSISTORS, NI IS THE DRAIN NODE, NZ IS THE BASE NODE, TRANSISTORS, NI IS THE DRAIN NODE, NZ IS THE SQUACE NODE, TRANSISTORS, NI IS THE DRAIN NODE, NZ IS THE SQUACE NODE, TRANSISTORS, NI IS THE DRAIN NODE, NZ IS THE SQUACE NODE,
	OXXX NI N2 N3 N4 MODEL AREAF CUR VOLT TEMP EXAMPLES - 05 7 6 3 BNS 2 14A 3.0 010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 035 11 1 0 0 FMCS 2 035 11 1 0 0 FMCS 2 041 15 THE LETTER 0. 055 11 1 0 0 FMCS 2 055 11 1 0 0 FMCS 2 056 11 10 10 FMCS 2 056 11 10 10 FMCS 2 057 11 10 10 FMCS 2 058 10 10 FMCS 2 0 FMCS
	OXXX NI NZ NJ N4 MODEL AREAF CUR VOLT TEMP EXAMPLES - 05 7 6 3 BNS 2 1MA 3.0 070 7 3 4 FJUN 025 11 1 0 0 FMCS 2 010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 010 7 3 4 FJUN 025 11 1 0 0 FMCS 2 026 11 1 0 0 FMCS 2 027 11 1 0 0 FMCS 2 028 11 1 0 0 FMCS 2 029 10 FMCS 2 020 1 15 THE CALLECTOR MODE, N2 15 THE COLLECTOR MODE, N2 15 THE SQUACE NODE, TEMPLET 029 10 FMCS 2 020 1 1 1 0 0 FMCS 2 020 1 1 1 0 0 FMCS 2 010 7 3 4 FJUN 020 1 1 1 0 0 FMCS 2 010 7 3 4 FJUN 020 1 1 1 0 0 FMCS 2 020 1 1 1 1 0 0 FMCS 2 020 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
	GENERAL FCRM - GENERAL FCRM - GENERAL FCRM - GENERAL FCRM - GST LI IO O FWCS 2 14A 3.0 OIO 7 3 4 FJUN OSS III IO O FWCS 2 M3 IS THE EMITTER NODE, N2 IS THE OLEFECT M3 IS THE EMITTER NODE, N2 IS THE OLEFECT TRANSISTORS, N1 IS THE DRAIN NCDE, N2 IS THE BASE NODE, TRANSISTORS, N1 IS THE DRAIN NCDE, N2 IS THE SOURCE NODE, TRANSISTORS, N1 IS THE DRAIN NCDE, N2 IS THE SOURCE NODE, TRANSISTORS, N1 IS THE DRAIN NCDE, N2 IS THE GATE NODE, N3 IS THE SOURCE NODE, TRANSISTORS, N1 IS THE DRAIN NCDE, N2 IS THE GATE NODE, N3 IS THE SOURCE NODE, TRANSISTORS, N1 IS THE DRAIN NCDE, N2 IS THE GATE NODE, N3 IS THE SOURCE NODE, TRANSISTORS, N1 IS THE DRAIN NCDE, N2 IS THE GATE NODE, N3 IS THE SOURCE NODE,
	 6) TRANSISTOR (BIPALAR AND FIELG-EFECT) CARDS 6) TRANSISTOR (BIPALAR AND FIELG-EFECT) CARDS 6ENERAL FERM - 6ENERAL FERM - 6ENERAL FERM - 65 73 4 FUU 73 4 FUU 73 4 FUU 75 76 76 76 76 76 76 76 76 77 76 76 76 76 7
	6) TRANSISTOR (BIPOLAR AND FIELD-EFECT) CARDS GENERAL FORM - GENERAL FORM - GENERAL FORM - GENERAL FORM - GENERAL FORM - GENERAL FORM SISTOR NAME WHICH MUST BEGIN WITH THE LETTER Q. GOT 7 3 4 FUUN OLO 7 3 4 FUUN OCS 7 6 3 BNS 2 1MA 3.0 OC 7 3 4 FUUN OC 7 6 FUUN OC 7 6 FUUN OC 7 6 FUUN OC 7 6 FUUN OC 7 7 6 FUUN OC 7 7 6 FUUN OC 7 7 6 FUUN OC 7 6 FUUN OC 7 6 FUUN OC 7 7 6 FUUN OC 7 6 FUUN OC 7 7 6 FUUN OC 7 6 FUUN OC 7 7 6 FUUN OC 7 7 7 7 FUUN OC 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7
. 	 6) TRANSISTOR (RIPOLAR AND FIELD-EFFECT) CARDS 6) TRANSISTOR (RIPOLAR AND FIELD-EFFECT) CARDS 65NTRAL FCRM - 65NTRAL FCRM - 65T 6 3 RNS 2 14A 3.0 73 4 FJUW 74 50151505, NI 15 THE COLLECTOR NODE, NZ 15 THE RASE NODE, NO F, NZ 15 THE RASE NODE, NZ 15 THE COLLECTOR NODE, NZ 15 THE RASE NODE, NZ 15 THE RA
	 INP CONSERVE SOURCE CARDS. ISANSISTOR (BIPOLAR AND FIELD-EFECT) CARDS ISANSISTOR (BIPOLAR TRANSISTOR NAME WHICH MUST BEGIN WITH THE LETTER Q. OSS 7 6 3 BNS 2 14A 3.0 OSS 11 1 0 0 FYGS 2 OSS 11 1 0 0 FYGS 2 O FYGS 2
• •	VILOES TOP WHICH THE CREDIT IS TO BE AMERICED MAT BE TWIENED AS DESCRIBED SUDER THE CURRENT SOURCE CARDS. 6) TRANSISTOR (BIPOLAR AND FIELD-EFECT) CARDS 010 7 3 4 FJUW 025 11 1 0 0 FMCS 2 1MA 3.0 010 7 3 4 FJUW 025 11 1 0 0 FMCS 2 010 7 3 4 FJUW 026 7 6 3 BNS 2 1MA 3.0 010 7 3 4 FJUW 027 6 3 BNS 2 1MA 3.0 010 7 3 4 FJUW 028 7 6 3 BNS 2 1MA 3.0 010 7 3 4 FJUW 029 7 6 3 BNS 2 1MA 3.0 010 7 3 4 FJUW 020 7 8 FJUW 020 7 8 FFFE 020 7
	FOR A SINGLE GROUNDED VOLTAGE SOUGCE (OR CUPRENT SOURCE) UP TO TWENTY YALUES FOR WHICH THE CIRCUIT IS TO BE ANALYZED MAY DE ENTERED AS DESCRIBED UNDER THE CURRENT SOURCE CARDS. 6) TRANSISTOR (BIPOLAR AND FIELD-EFECT) CARDS 05 7 6 3 BNS 2 1MA 3.0 05 7 6 3 BNS 2 1MA 3.0 05 7 6 3 BNS 2 1MA 3.0 05 7 6 3 BNS 2 1MA 3.0 010 7 3 4 FJUN 025 16 10 0 FMS 2 1MA 3.0 026 7 6 3 BNS 2 1MA 3.0 027 6 3 BNS 2 1MA 3.0 026 7 6 3 BNS 2 1MA 3.0 027 6 3 BNS 2 1MA 3.0 026 7 6 3 BNS 2 1MA 3.0 027 6 3 BNS 2 1MA 3.0 026 7 6 3 BNS 2 1MA 3.0 027 7 6 3 BNS 2 1MA 3.0 026 7 6 3 BNS 2 1MA 3.0 027 6 3 BNS 2 1MA 3.0 028 11 1 0 0 FMS 7 030 7 3 4 FJUN 028 11 1 0 0 FMS 7 040 7 3 4 FJUN 058 11 1 0 0 FMS 7 050 7 6 3 BNS 2 1MA 3.0 050 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7
	FOR A SINCLE GROUNDED VOLTAGE SOUGCE (OR CUPRENT SOURCE) UP TO TWENTY FOR A SINCLE GROUNDED VOLTAGE SOUGCE (OR CUPRENT SOURCE) UP TO TWENTY VALUES FOR WHICH THE CIRCUIT IS TO BE ANALYZED MAY OF ENTERED AS DESCRIBED UNDER GENERAL FORM (BIPOLAR AND FIELG-EFECT) CARDS OF 7 6 3 BNS 2 1MA 3.0 OS 7 6 3 BNS 2 1MA 4.0 OS 7 6 3
	 INAL VOLTAGE (POSITIVE DR MEGATIVE) IN VOLTA OF THE VOLTAGE SOLACE. FOR A SINGLE GROUNDED VOLTAGE SOURCE (OR CUPRENT SOURCE) UP TO TWENTY FOR A SINGLE GROUNDED VOLTAGE SOURCE (OR CUPRENT SOURCE) UP TO TWENTY VALUES FOR WHICH THE CIRCUIT IS TO BE ANALYZED MAY BE FNITERED AS DESCRIBED UNDER AVALUES FOR WHICH THE CIRCUIT IS TO BE ANALYZED MAY BE FNITERED AS DESCRIBED UNDER AVALUES FOR WHICH THE CIRCUIT IS TO BE ANALYZED MAY BE FNITERED AS DESCRIBED UNDER AVALUES FOR WHICH THE CIRCUIT IS TO BE ANALYZED MAY BE FNITERED AS DESCRIBED UNDER AVALUES FOR WHICH THE CIRCUIT IS TO BE ANALYZED MAY BE FNITERED AS DESCRIBED UNDER AVALUES FOR WHICH THE CIRCUIT IS THE COLLECTOR NODE, WZ IS THE BASE NODE, ANALYZAN IN NZ NJ NA MODEL AREAF CUR VOLT TEMP ANAN FILL FORMERS ANA REALE FORM - ANAN FILL FRANSISTORS, NIL IS THE COLLECTOR NODE, WZ IS THE BASE NODE, ANAVPLES - ANA F FUNK ANAN F FUNK ANAN FILLE FRANSISTORS, NIL IS THE COLLECTOR NODE, WZ IS THE BASE NODE, ANAN F FUNK ANAN
	 V. W. IS THE ENGINED OF THE CREDIES OF THE CREDIES OF THE YOUT AND THE WOMEN VELTAGE STUDGE. V. W. IS THE POSITIVE OR NEGATIVE) IN VOLIS OF THE VOLIAGE STUDGE. INAL VOLIAGE (POSITIVE OR NEGATIVE) IN VOLIS OF THE YOUTAGE SOURCE. FOR A SINGLE GROUNDED VALUE STUDGE (OR CURRENT SOURCE) UP TO THENTY VLUES FOR WHICH THE CIRCUIT IS TO BE ANALYZED MAY RE FNIERED AS DESCRIBED UNDER OXXX NI NZ NA NADEL AREAF CUR YOLT TEMP OXXX NI NZ NA NADEL AREAF CUR YOLT TEMP OXXX NI NZ NA NADEL AREAF CUR YOLT TEMP OXXX NI NZ NA NADEL AREAF CUR YOLT TEMP OST 6 3 BNS 2 1MA 3.0 OST 6 3 BNS 2 1MA 4.00F. NOIL TEMP OST 6 3 BNS 2 1MA 3.0 OST 6 3 BNS 2 1MA 4.00F. NOIL TEMP OST 7 6 3 BNS 2 1MA 4.00F. NOIL TEMP OST 7 6 3 BNS 2 1MA 4.00F. NOIL TEMP OST 7 6 3 BNS 2 1MA 4.00F. NOIL TEMP OST 7 6 3 BNS 2 1MA 4.00F. NOIL TEMP OST 7 6 3 BNS 2 1MA 4.00F. NOIL TEMP OST 7 6 3 BNS 2 1MA 4.00F. NOIL TEMP
	 YXXX IS THE GROUNDED YOLIAGE SOUNDED YOLIAGE STURCE WAYE WHICH WHIT REGIN WITH THE LETTER NOW- V. WHIS THE GROUNDED YOLIAGE SOUNDED YOLIAGE STURCE. VALUES FOR WHICH THE CROUNDED YOLIAGE SOURCE OR CURRENT SOURCE) UP TO TWENTY FOR A SINGLE GROUNDED YOLIAGE SOURCE (OR CURRENT SOURCE) UP TO TWENTY ANALUES FOR WHICH THE CIRCUIT IS TO BE AMALYZED MAY DE FNIERED AS DESCRIBED UNDER FOR A SINGLE GROUNDED YOLIAGE SOURCE (OR CURRENT SOURCE) UP TO TWENTY ANALUES FOR WHICH THE CIRCUIT IS TO BE AMALYZED MAY DE FNIERED AS DESCRIBED UNDER FOR A SINGLE GROUNDED YOLIAGE SOURCE (OR CURRENT SOURCE) UP TO TWENTY ANALUES FOR WHICH THE CIRCUIT IS TO BE AMALYZED MAY DE FNIERED AS DESCRIBED UNDER GENERAL FORM GENERAL FORM - GENERAL - GENERAL FORM - GENERAL FORM - GENERAL - GENERAL FORM - GENERAL - GENERAL FORM - GENERAL - GENERAL - GENERAL - GENERAL - G
· · · ·	VXXX IS THE GROUNDED VALIAGE SOUNCE VAYE WHICH WHIST REGIN WITH THE LETTER V. W+ IS THE GROUNDED VALIAGE SOUNCE VAYE WHICH WHIST REGIN WITH THE LETTER FOR A SINCLE GROUNDED VALIAGE SOUNCE OF RUPERED AS DESCRIBED UNDER FOR A SINCLE GROUNDED VALIAGE SOUNCE (OR CUPRENT SOUNCE) UP TO THENTY FOR A SINCLE GROUNDED VALIAGE SOUNCE (OR CUPRENT SOUNCE) UP TO THENTY FOR A SINCLE GROUNDED VALIAGE SOUNCE (OR CUPRENT SOUNCE) UP TO THENTY FOR A SINCLE GROUNDED VALIAGE SOUNCE (OR CUPRENT SOUNCE) UP TO THENTY FOR A SINCLE GROUNDED VALIAGE SOUNCE (OR CUPRENT SOUNCE) UP TO THENTY FOR A SINCLE GROUNDED VALIAGE SOUNCE (OR CUPRENT SOUNCE) UP TO THENTY FOR A SINCLE GROUNDED VALIAGE SOUNCE (OR CUPRENT SOUNCE) UP TO THENTY FOR A SINCLE GROUNDED VALIAGE SOUNCE (OR CUPRENT SOUNCE) UP TO THENTY FOR A SINCLE GROUNDED VALIAGE SOUNCE (OR CUPRENT SOUNCE) UP TO THENTY FOR A SINCLE GROUNDED VALIAGE SOUNCE (OR CUPRENT SOUNCE) UP TO THENTY FOR A SINCLE GROUNDES AND FIELO-EFFECT) CARDS OID 776 7 6 7 MUS ZIMA 3.0 OND 776 7 6 7 MUS ZIMA 3.0 FOR A SINCLE CARDS. OND 776 7 FUN FOR A SINCLE CARDS. OND 776 7 FUN FOR A SINCLE OR THE OFFICE FOR UNCTION FIELO FOR A SINCLE OR OFFICE FOR A OUNCE, AND FIELO-EFFECT) CARDS OND 776 7 FUN FOR A SINCLE OR OUNCE OFFICE FOR A OUNCE OFFICE FOR A SINCLE OFFICE FOR A SINCLE FOR A SINCLE OFFI
	VXXX IS THE CROUNDED YOLINGE SOURCE WAYE WHICH WIST REGIN WITH THE LETTER V. W+ IS THE CROUNDED YOLINGE SOURCE WAYE WHICH WIST REGIN WITH THE LETTER V. W+ IS THE CROUNDED VOLINGE OF THE CREUNED VOLINGE SOURCE. VALUES FOR WHICH THE CROUNDED VOLINGE OF THE VOLINGE SOURCE) UP TO THE WITH FOR BIPOLER THE CROUNDED VOLINGE AND FIELCEFFECT) CARDS OD 76 A RUN SOURCE CARDS. OD 76 A RUN SOURCE CARDS. OD 76 A RUN SOURCE CARDS. VILUES THE CHITTER NOTE SOURCE OF COR NOTE THE LETTER O. CREATER FORMANS SOULT IS TO BE ANALYZED MAY DE ENTERED AS DESCRIBED UNDER FEXAMPLES - OD 76 A RUN SOURCE CARDS. OD 76 A RUN SOURCE CARDS. OD 76 A RUN SOURCE CARDS. NUT IS THE CHITTER NOTE FOR THE COLLECTOR NOTE, NZ IS THE RUNCE NOTE, NUT IS THE CHITTER NOTE. CORNEL FOR THE CHILD AND FILL TEMP OD 76 A RUN SOURCE CARDS. OD 77 A RUN SOURCE CARDS. OD 77 A RUN SOUR

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BIPOLAR TRANSISTOR MODEL CARDS

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THESE CARDS DESCRIBE THE BIPOLAR TRANSISTOR MODELS USED IN THE CIRCUIT. THE MODIL PARAMETERS ARE ENTEPED AS GROUPS OF NUMBERIC FIELDS PRECEDED BY SPECIFIC KEYWORDS WHICH ARE DESCRIBED BELOW. THE CROER IN WHICH GROUPS OF PARAMETERS ARE ENTERED IS ARBITRARY AND ANY GROUP MAY BE CMITTED, IN WHICH CASE THE DEFAULT VALUES ARE ASSUMED. WITHIN A GROUP SLASHES MAY BE USED TO DEFAULT LEADING NUMERIC FIELDS AND ANY OMITTED TRAILING NUMERIC FIELDS TAKE ON DEFAULT VALUES. AS MANY CONTINUATION CARDS (SPECIFIED BY A PLUS, +, IN COLUMN 1) AS NECESSARY MAY BE USED.

GENERAL FORM -

BXXX TYPE BF=BFMAX,ICMAX,BFLCW,ICLOW,VCE,TC1,TC2 BR=VALUE + R0=VALUE,IC,VBE,VCE RB=VALUE,TC1,TC2 RC=VALUE,TC1,TC2 + FT=VALUE,IC,VCE,LE/WB,ICO TSAT=VALUE CJE=VALUE,VBE,PHIE,NE

+ CJC=VALUE, VBC, PHIC, NC, RATIO CSUB= VALUE TEMP= VALUE ISS=VALUE

+ TF=VALUE VA=VALUE

EXAMPLES -

BNPM=NPN BF=100,1.0MA(40,1.0UA,3.0V,6.667M,-36.0U) BR=1 ISS=2.02-14 + RB=150.(2.0M,9.6U) RC=100.0(1.5M,7.0U) PC=50K,2MA + CJE=3.0PF,0.65V CJC=1.0PF,-5.0V CSUB=2.0PF + FT=600MEGHZ(1.0MA,5.0V)

BNS NPN BF 290 BR 1 ISS 1.26E-15 RB 670 RC,300 RD 180K 1M + FT 703MEG 1M CJE .65P CJC .36P CSUS 3.2P VA 50.0V

BPNP RB=100 CSUB=3.2PF BF=110 PNP

1) NAME

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BXXX IS THE BIPOLAR TRANSISTOP MODEL NAME WHICH MUST BEGIN WITH THE LETTER B.

2) TYPE KEYWORD : NEN CR PNP

TYPE IS EITHER THE KEYWORD NPN OR PNP DEPENDING ON WHETHER THE BIPCLAR MODEL TYPE IS NPN OR PNP, RESPECTIVELY. IF CMITTED, NPN IS ASSUMED.

3) FORMARD BETA KEYWORD : BF

BEMAX IS THE NOMINAL FORWARD BETA. FOR A CURRENT-DEPENDENT FORWARD BETA, BEMAX IS THE MAXIMUM VALUE OF THE FORWARD BETA, ICMAX IS THE COLLECTOR CURRENT AT WHICH BEMAX OCCURS, BELOW IS A VALUE OF THE FORWARD BETA AT A CUPRENT BELOW ICMAX, AND ICLOW IS THE COLLECTOR CURRENT AT WHICH BELOW CCCURS. VCE IS THE CONSTANT VALUE OF THE COLLECTOR-EMITTER VOLTAGE AT WHICH BETH BEMAX AND BELOW CCCUR. TOI AND TO2 ARE THE FIRST- AND SECOND-ORDER TEMPERATURE COEFFICIENTS, RESPECTIVELY, FOR BOTH THE FORWARD AND REVERSE BETAS.

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	4 1	DEVLOCE DETA		í			
	41	REVEPSE DETA	KETWUND (F BR				
		VALUE IS THE NOWLAA	I REVERSE RETA	NOTE THAT T	HE TEMPERAT	HEE COSELLC	TENTS
	FOR	THE REVERSE BETA ARE	THE SAME AS THOS	7 FOR THE F	C2WARD BETA	AND ARE	
	SPEC	IFIED IN THE BE GREU	P. THE REVERSE B	ETA IS NOT	COLLECTOR C	URRENT DEPE	NDENT.
				•			
1	5)	OUTPUT RESISTANCE	KEYWORD :	RO			
	<u></u>	VALUE IS THE USTPUT	RESISTANCS. IC,	VB-, AND V	CE ARE INE	VALUES OF	C
· •	DUCL	TVGLV. AT NUTCH THE	INTER VULIAGE, A	AND COLLECT		VULIANC, NC	5- 5-
	FEUR TC N	OT SPECIFIED, THE RO	DATA IS DEED TO	CUNDITE THE	SARLY VOLT	267 (S75 ±6	
,	νοιτ	AGE DESCRIPTION BELL	W). NOTE THAT V	BE AND VOR	ARE OPTIONA	I. IE SPEC	IFIFD.
	THE	DATA IS USED TO COMPL	JTE THE REVERSE S	ATURATION C	UPPENT AS D	ESCRIBED BE	LOW
. 1	UNDE	R #REVERSE SATURATIO	V CUPRENT#. IF C	MITTEC, A-D	EFAULT OR E	XPLICITLY	
	SPIC	IFIED VALUE FOR THE !	EVERSE SATURATIO	N CURPENT I	S ASSUMED.		
		•	•				•
		ALCC DECLETANCE		•	•	`.	· · ·
•	01	BASE RESISTANCE	KEYWURD I RI	8			
		VALUE IS THE NOMEN M	CHATC BASE DEST		1 AND TO 2 A	-	т_
	AND	SECOND-OFDER THMPERAT	THRE CONFETCIENTS	RESPECT IV	FLY.		
•	~	SECOND SABER REALING	one der rierent				
•	•	•				4	
•	7)	COLLECTOR RESISTANCE	E KEYWOR	DI: RC	•		
			•		· · · · · ·		
	<u> </u>	VALUE IS THE NOMINAL		PESISTANCE	. TEL AND	ICZ ARE THE	
I	F 185	I- AMD SECUND-OFFICER	CEMPERATURE CUEFF.	ICIENIS, RE	SPECITVELT		
			•	•	• • •		
	9)	SMALL-SIGNAL UNITY (GAIN FREQUENCY	KEYN	ORD : FT		
					•		
		VALUE IS THE FREQUES	VCY AT WHICH THE	SMALL-SIGNA	L SHORT-CIR	CUIT CCMMCN	-
	MIT	TER CURRENT GAIN IS U	JNITY. IC AND VC	E APE THE C	OLLECTOP CU	RRENT AND	
1	COLL	ECTOR-EMITTER VOLTAGE	E, RESPECTIVELY,	AT WHICH FT	IS MEASURE	D. FT, IC,	AND
	VCE	ARE USED TO COMPUTE T	THE FURWARD TRANS	IT TIME, TH	LETWE AN	U ICU ARE U	51.U T.C.C
	10 M 10 T M 11	JUEL HIGH-LUPKEN FI	RULL-UPP. LEVWS	CHEDENT AT	10 OF 188 L 10 NF 188 L	815886 2911 TARTS TO PC	128
	OFF.	TO ACCOUNT FOR HIGH	A CHRISTING IS THE	-CEEL THE C	INPUTED VAL	UF OF TE IS	4- 6-
	MITT	TPLIED BY THE FACTOR	T CORRECT TT REEL				
		(1 + 0.25 * ()	LE/WB) **2 * (IC/I	CC - 1)**2)		
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	9)	SATURATION TIME CONS	STANT KE	YHORD : TSA	T	•	
		WALLIE TS THE SATURAT	TTON TIME CONSTAN	T WHICH IS	PRESENTLY N	OT USED IN	SLIC.
-		THE IS THE STOCKA	TACHT FERE CONJEMP				
		· ·	•	•			
	10)	EMITTER JUNCTION CAR	PACITANCE	KEYWORD :	CJE		
						777 - P11	
		VALUE IS THE EMITTER	JUMETIN CAPACT	TANCE AND V	BE IS THE B	ASE-EMITTER	
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WHERE VA IS THE CARLY VOLTACE AND VI THE THERMAL VOLTAGE.	
122 = IC \ ((I + ACB\AV) * EXP(VE-VI))	
LE 155 IS NOT SPECIFIED AND IF VAE AND VGE OF THE RD SPECIFICATION ARE ALSC NOT Specified, then iss is deraulted to 1.06-14 Amperis. If iss is not specified but Vae And VGE Are specified for RD, then iss is computed from the RD nate by the following equation	2
- SSI ★ βΔΗ9Jξ = S∃I ★ ∃ΔΗ9Jξ = SSI	
VALUE IS THE NOVINAL REVERSE SATURATION CURRENT AND IS PELATED TO THE SHORT-CIPCUIT EBERS-YELL SATURATION CURRENT AND IS PELATED TO THE	6
221 : QAQMYAN TAPRADA GUTARUTAS ERREVER (41	
VALUE IS THE TEMPERATURE AT WHICH THE MODEL PARAMETERS ARE MEASURED.	
I3) LENDE&VLNKE KEYWC30: LEND	•
ASUMED TO EXIST SETMERT THE EXTERNAL COLLECTCR AND GROUND, WHILE FOR A PNP Transister to exist between the internal base and ground.	
IS) SUBSTRATE CAPACITANCE KEYNERC : CSUB VALUE IS THE SUPETE CAPACITANCE. FOR AN NEW TRANSIETCR. CSUB. 12	
FOR A REVERSE BLASED JUNCTION.	
TOR AND THE BASE CONTACT AND (1.0-PATIC)*CUC IS THE CAPACITANCE THAT EXISTS Between the collector and the base active regions. For both NPN and PNP Devices, vec should be positive for a formard elason junction and Negative	
RATIO IS THE FRACTION OF THE ABOVE DESCRIBED CJC THAT OVERLAPS THE BASE OHMIC Retio is the fraction of the above described cjc that exists between the collec-	
C1C = C1C(ABC=0) \ (1 - ABC\bHIC)**NC	
VOLTAGE AT WHICH.TH" COLLECTOR JUNCTION CAPACITANCE IS MEASURED. PHIC IS THE CONTACT POTENTIAL AND NO IS THE CRADIENT FACTOR. THE COLLECTOR JUNCTION CAPACI- TANCE AT A GIVEN VAC IS DESCRIBED.BY THE FOLLOWING EQUATION	
LL) CCLLECTOR JUNCTION CAPACITANCE KEYWORD : CJC	
FOR BOTH NPN AND PNP DEVICES, VRS SHOULD DE PCSITIVE FOP A FCRWARD BIASED	
VULIAGE AL MHTH THE EMITTER JUNCTION CAPACITANCE IS MEASURED. PHIE IS THE CONTACT POTENTIAL AND FE IS THE GRADIENT FACTOR. THE EMITTER JUNCTION CAPACI- TANCE AT A GIVEN VAR. IS DESCEIRED BY THE FELLOWING EQUATION	-

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21.

VALUE IS THE FORMARD TRANSIT TIME. IF UNSPECIFIED, TF IS COMPUTED FROM THE	HE
 THIS VALUE REPLACES ANY FT DERIVED VALUE.	
16) EAPLY VOLTAGE KEYWORD : VA	
VALUE IS THE EARLY VOLTAGE. IF UNSPECIFIED, VA IS COMPUTED FROM THE RO DATA BY THE FORMULA	
 VA = RO * IC	
IF RO IS UNSPECIFIED, THEN VA IS SET TO INFINITY. IF VA IS SPECIFIED, THIS VALUE REPLACES ANY RO DERIVED VALUE.	•
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) 0 ٦) SEE DESCRIPTION ABOVE 30144=44 FE=VALUE 226 DESCRIPTION ABOVE BUJAY=SSI SEE DESCRIPTION ABOVE ENDAY/=9MET ١ 300 DEC K 0.0 COB=AVFR 0.0 PATIO 0 ЗN -ST JOV 2.0 PHIC 0.0 ABC SUJAVEOLO) 0*0 55555.0 <u>PN</u> 0.5 VCLTS (PNP) Ċ (NAN) SITCA LO 5 IHd 381 0.0 بو 0.0 · CJE=VALUE \odot SUJAV=TA2T 0.0 <u>1001 "</u> ICNCRED 84/27 1640850 Э IGNCSED ACE -LCACKED . C 3UJ AV=T7 **JINIINI TC2** 0.0 101 0.0 BUJAV=0A 0.0 `} 0.0 201 · 101 0.0 20JAV=89 0.0 Э '2ΟΛ 0380N01 **78**E IGNCKED 21 16NCPED) FO=VALUE **STINIANI** 0• T BO=VALUE 0.0 10.2 J 101 0.0 0.0 20V ICCOM **ICNCRED** RELOW GENOND1 XVWOI **D**BADNOI X AM AR=AH 100.0 ١ TYPE NON DEFAULT VALUE DARANGTEP

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61.

SATJOV STAD THE TRANSCONDUCTANCE PARAMETER DETERAINE THE VARIATION OF DRAIN CURRENT WITH VALA IS THE TPANSCONDUCTANCE PARAVETER. BUTH THE THRESHOLD VCLTAGE AND (5 KEYWCRD : DETA ABTEMARA BONATOUONOD SWART THE CHANNEL SURFACE POTENTIAL. THIS PARAMETER IS FOR MOS FIELC-REFECT TRANSISTOR MODELS CNLY. VALE IS (5 KEYWORD : PHI SURFACE PETENTIAL • 300k DEVICES, VTO SHOULD BE POSITIVE FOR ENHANCEMENT MORE AND MEGATIVE FOR DEPLETION VALI IS THE THRESHOLD VELIFIES FOR BETH & CHANNEL AND P CHANNEL THRESHOLD VOLTAGE 15 KEAMORD : ATO RESPECTIVELY. KENNDRO UNCS OR PMOS DEPENDING ON WHETHER THE MODEL IS N CHANNEL OR P CHANNEL. RESPECTIVELY. FOR MCS FIELD-EFFECT TRANSISTOR MCDSLS, TYPE IS EITHER THE AUDA OR PUUN DEPENDING ON WHETHER THE MODEL IS A CHANNEL OR P CHANNEL. FOR JUNCTION FLALD-BEFECT TRANSISTOR MODELS. TYPE IS EITHER THE REYMORD KEAMORD : NOUN' PUUN' WORL ON FMOR TYPE 12) A SETTER FXXX IS THE FIELD-EFFECT TRANSISTOR MODEL NAME WHICH MUST BEGIN WITH THE · (T 3MAN) NWUZ ALO I'O BELV I'SZA GAMAN O'S COB O'SSAF CBD O'SDE CB2 O'SDE 783 EJI NJIN: ALD=-3 BELT=0.001 LAMADA=0.05 RD=500 FS=500 CGS=10PF CGD=10PF) - SEINAXA) 7170A=S1 XX IADE ALCEAVER CON=AVED COB=AVEIO CHD=AVEII CO2=AVELS DB=AVEI3 XX IADE ALCEAVER CON=AVED COB=AVEIO CHD=AVEII CO2=AVER BUANEA F X X X - WHOH TVVENED ACCESSERY MAY BE USED. ASSUMED. 25 MANY CONTINUATION CARDS (SPECIFIED RY A PLUS, +, IN COLUMN 1) AS ARETRARY AND ANY PASANETER MAY BE CALITED. IN WHICH CASE THE PERAULT VALUE IS FOLLOWED BY THE PARAMATER VALUE. THE CREEK IN WHICH PARAMATERS ARE ENTERED IS CIRCUIT. THE MODEL PARAMETERS ARE ENTERED BY SECIFYING A PARAMETER KEYWORD THESE CARDS DESCRIPE THE FISLO-FFFECT TRANSISTOR MODELS USED IN THE ETELD-EFECT TPANSISTOR MODEL CARDS

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 6)	BULK THRESHOLD PARAMETER KEYWORD : GAMMA
BULK	THIS PAFAMETER IS FOR MCS FIELD-REFECT TRANSISTOR MODELS CNLY. VALA IS THE SUBSTRATE) THEESHOLD PARAMETER. BOTH THE SURFACE POTENTIAL AND THE BULK SHOLD PARAMETER DEFERMINE THE VARIATION OF THE THRESHOLD VOLTAGE WITH
SUB S	TRATE VOLTAGE.
7)	CHANNEL LENGTH MODULATION PARAMETER KEYWORD : LAMBDA
 COND	VALS IS THE CHANNEL LENGTH ACOULATION PARAMETER WEICH DETERMINES THE OUTPU
COND	
8)	DRAIN RESISTANCE KEYWORD : RD
 	VALG IS THE DHMIC DRAIN RESISTANCE.
9)	SOURCE RESISTANCE KEYWORD : RS
	VAL7 IS THE OHMIC SOURCE RESISTANCE.
10)	GATE-SOURCE CAPACITANCE KEYWORD : CG3
- S DUP. VOLT	FOR JUNCTION FIELD-EFFECT TRANSISTOR MODELS, VALB IS THE ZEFO BIAS GATE- CE JUNCTION CAPACITANCE WHICH VAPIES AS THE -1/2 POWER OF THE GATE-SOURCE AGE. FOR MOS FIELD-EFFECT, TRANSISTOR MODELS, VALB IS THE LINEAR GATE-
 SOUR	CE CAPACITANCE.
11)	GATE-DRAIN CAPACITANCE KEYWORD : CGD
	FOR JUNCTION FILLD-SEFECT TRANSISTOR MODELS, VALS IS THE ZERO BIAS GATE-
VOLT CAPA	N JUNCTION CAPACITANCE WHICH VAFIES AS THE -172 POWER OF THE GATE-DRAIN AGE. FOR MOS FILLD-EFFECT TRANSIST or models, VAL9 IS THE LINEAR GATE-DRAIN CITANCE.
 12)	GATS-BULK CAPACITANCE KEYWERD : CGB
THE	THIS PARAMETER IS FOR MOS FIELD-EFFECT TRANSISTOR MODELS CNLY. VALIO IS LINUAR GATE-BULK CAPACITANCE.
13)	BULK-ERAIN CAPACITANCE KEYWORD : CBD
тне Орт	THIS PAPAMETER IS FOR MOS FIELD-EFFECT TRANSISTER MODELS CNLY. VALID IS ZERD BIAS BULK-DRAIN JUNCTION CAPACITANCE WHICH VARIES AS THE -1/2 POWER HE BULK-DRAIN VOLTAGE.
	BULK-SOURCE CAPACITANCE KEYWORD : CBS
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	JUNCTION VOLTAGE	TANCES AT & GIVEN Ing Equation	104470 046400 346400 350 87 THE FOLLOW	אר מר דאב אמטען 19 סר דאב אמטען 19 סר געון	NOTE : EACI (VJI
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	THE SET OF DATA CARDS BELOW DESCRIBE A BROADBAND AMPLIFIER AND ILLUSTRATE THE CODING FORMAT FOR SLIC. ANALYSES ARE PERFORMED FOR TWO TEMPERATURES AND A NOISE ANALYSIS IS PERFORMED FOR THREE FREQUENCIES.
	SCLOMON AND WILSON SERIES-SERIES TRIPLE BROADBAND AMPLIFIER PRINT DC AC FLOG(10,1MEGHZ,100MEGHZ) VOUT 14 0 VIN 1 0 TEMP 300 300 305 NOISE 1MEGHZ 10MEGHZ
	* BNPN=NPN BF=100,1.0MA(40,1.0UA,3.0V,6.667M,-36.0U) BR=1 ISS=2.0E-14 + RB=150.(2.0M,9.6U) RC=100.0(1.5M,7.0U) RD=50K,2MA + CJE 3.0PF 0.65V CJC 1.0PF -5.0V CSUB 2.0PF
	+ ET=600MEGHZ(1.0MA, 5.0V) *
	VS(1,0)=0.0 RS 1 2 50.0 CC.S(2,3)=1.0UF
	Q1 5 3 4 BNPN RE1(4,0)=100.0 RA 13 5 9K
	Q2 6 5 0 BNPN CP 6 5 3PF PB(13,6)=5.0K O3 8 6 7 BNPN
	RE2(7,0)=100.0 PF(7,4)=1.0K
	Q4 13 8 9 EMPN PG(9,10)=3.0K BK(12.11)=6.0K
	Q5(13 13 12)=BNPN Q6 10 11 0 BNPN CBYP 10 0 10UF
	RD(10,3)=12.0K 07 (11,11,0) ENPN 1.0 08 9 11 0 BNPN
	Q10 9 11 0 BMPN
	CCL 9 14 1UF FL(14,0)=50.0 VCC(13,0)=6.0VCLTS
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III. PROGRAM DESCRIPTION

The following sections describe the operation of the SLIC program. The total program consists of a main program and thirtyfive subroutines. A written description and a flowchart of the execution sequence are provided for the main program and each subroutine. A description of the function of each common block variable is also included.

Main program:	SLIC
Data read-in subroutines:	READ
	ELEMNT
	BMODEL
	VJCT
	FIT
	FMODEL
· · · ·	INLIST
•	CHECK
	CLKST
Matrix set-up subroutines:	SETUP
	NCODE
	OPTORD
	NUMSET

DC subroutines:

AC subroutines:

Pole-zero subroutines:

Other subroutines:

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. . . DCTRAN PLOT DCANAL

DCMOD

JFET

BJTDC

MOSFET

UPDATE

DCSOLV

DCADJ

ACMOD

ACANAL ACSOLV

ACADJ

PZANAL

MULLER

CDET

LOG2

SORT

SENSE

NOISE

CLOCK

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MAIN PROGRAM SLIC

SLIC controls the overall program execution sequence. The first step is the reading of input data describing the circuit and the the types of analyses. Subroutine READ reads and checks the input data and subroutine CHECK prints transistor model parameters and processes transistors. If fatal errors are discovered in the input data, the job is aborted and a new job is begun. If no fatal errors are found, the specified analyses are performed.

For the dc analysis, subroutine SETUP sets up the dc sparse matrices and subroutine DCMOD computes the dc circuit models. If a dc transfer curve is requested, subroutine DCTRAN computes and plots the transfer curve. Next, subroutine DCANAL computes and prints the dc node voltages and transistor operating points. If a frequency response or pole-zero analysis is not also requested, subroutine ACMOD computes and prints the small-signal transistor parameters. If one of these analyses is also requested, ACMOD will be called later.

SLIC performs two types of small-signal analyses: a frequency response or a pole-zero analysis with an optional frequency response. Only one of these two analyses can be requested for a job.

For the frequency response, subroutine SETUP sets up the ac sparse matrices and subroutine ACMOD computes and prints the smallsignal transistor parameters. Subroutine ACANAL then computes the magnitude, phase, real part, and imaginary part of the transfer

function directly from the complex nodal admittance equations and prints these values.

For the pole-zero analysis, subroutine ACMOD first computes and prints the small-signal transistor parameters. Next, subroutine PZANAL computes and prints the poles and zeros of the transfer function. If a frequency response is also requested, PZANAL computes and prints the magnitude, phase, real part, and imaginary part of a pole-zero derived transfer function.

For the noise analysis, subroutine NOISE computes and prints the equivalent noise sources and at each requested frequency the rms noise at the output port. For the sensitivity analysis, subroutine SENSE computes and prints the sensitivities (partial derivatives).

If a variable source and/or temperature variations are specified, the requested analyses are repeated for each source and/or temperature value.

Throughout the execution of a job, subroutine CLKRD computes and prints the elapsed job time. The elapsed time is printed at the end of each type of analysis. Also, if a fatal error is encountered during the execution, the job is aborted.










SUBROUTINE READ

This subroutine controls the reading and processing of input data. Subroutine INLIST reads an input data card and if recognizable, control-is transferred to a section of READ that handles the particular type of card. If unrecognizable, an error message is printed. The PRINT, TEMP, NOISE, SENS, and DC cards are read and processed within READ. Subroutine ELEMNT reads and processes resistor, voltage-controlled current source, capacitor, inductor, mutual inductor, transistor, voltage source, and current source cards. Subroutine EMODEL reads and processes bipolar transistor model cards while subroutine FMODEL reads and processes fieldeffect transistor model cards. The reading and processing of input data continues until an ALTER or END card is read.

SUBROUTINE READ









(TEMPERATURE CARD)







(TRANSISTOR CARDS)



(VOLTAGE SOURCE AND CURRENT SOURCE CARDS)



(BIPOLAR TRANSISTOR MODEL CARDS)



(FIELD-EFFECT TRANSISTOR MODEL CARDS)



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SUBROUTINE ELEMNT

This subroutine reads and processes data on resistor, voltagecontrolled current source, capacitor, inductor, mutual inductor, transistor, voltage source, and current source cards. A different set of arguments is passed from subroutine READ for each type of card. Subroutine INLIST is called each time a new data record is needed.

Execution is started by checking if the element has previously been read. If so, the new data replaces old stored data. Next, the element nodes are obtained and if a transistor card is being processed, the transistor model name is also obtained. Then the element values are obtained. Finally any additional values are obtained for voltage and current sources; and resistor,voltagecontrolled current source, capacitor, and inductor cards are checked for sensitivity analysis variable designation.

SUBROUTINE ELEMNT



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SUBROUTINE BMODEL

This subroutine reads and processes data on bipolar transistor model cards. Subroutine INLIST is called each time a new data record is needed. If the model has previously been read, the new data replaces old stored data. The model parameters are first read, stored, and checked for negative values. Next a number of additional model parameters are computed from the user specified parameters. The thermal voltage $(V_T = \frac{kT}{q})$, basewidth modulation factor (n), reverse saturation current (I_g), currentdependent β_F coefficients, zero bias junction capacitances $(C_{jeo} \text{ and } C_{jco})$, and forward base transit time (τ_F) are computed for each model. Subroutines VJCT and FIT are called during these calculations.



SUBROUTINE VJCT

This function subroutine computes the base-emitter junction voltage of a bipolar transistor from supplied values of collector current and collector-emitter voltage. A modified Newton-Raphson method similar to that of the BIAS-3 program [4] is used. VJCT is called from the subroutines BMODEL and CHECK.



SUBROUTINE FIT

This function subroutine computes the three current-dependent β_F coefficients from two sets of β_F and I_c specifications. The linear equations are first assembled [3] by a method of least squares. Next the equations are solved by the Gauss-Jordan elimination method. Finally a check is made for any negative coefficients. If any are found, FIT is set to -1.0.



SUBROUTINE FMODEL

This subroutine reads and processes data on field-effect transistor model cards. Subroutine INLIST is called each time a new data record is needed. If the model has previously been read, the new data replaces old stored data. The model parameters are first read, stored, and checked for negative values. Finally any unspecified parameters are set to default values.



SUBROUTINE INLIST

This function subroutine reads and interprets the free-format input data. INLIST is called each time a new data record is needed.

Before reading a new data card, any error messages from the previous card are printed. The first record of the card is then read, the type of card identified, and the card printed. For element cards, the element name is also obtained. Control is then returned to the calling subroutine.

INLIST interprets a single data record as follows: first, a slash (/) indicating a default value is checked for. If found, control is returned to the calling subroutine. For a numeric data record, the value is obtained. Four forms of numeric data can be interpreted. A number may be an integer, a floating point number, either an integer or floating point number followed by an integer exponent (e.g., 1E-14 or 2.65E3), or either an integer or a floating point number followed by an engineering scale factor (G,MEG,K,M,U,N, or P). For a name data record, the type of keyword is determined. After interpretation of the data record, INLIST is set to -1 if no data was found, to 0 is a number was found, or to +1 if a name was found. Control is then returned to the calling subroutine.

SUBROUTINE INLIST



SUBROUTINE CHECK

This subroutine begins by printing a summary of the transistor models. Bipolar transistor model parameters and then field-effect transistor model parameters are printed. Next transistors are checked for the presence of required models. Finally, initial values of bipolar and field-effect transistor junction voltages are determined.



SUBROUTINE CHECK

SUBROUTINE CLKST/CLKRD

This subroutine computes and prints the elapsed job time. A system library subroutine SECOND is called to obtain the time. At the beginning of each new job CLKST calls SECOND to obtain the initial job time. Entry CLKRD calls SECOND to obtain the present job time and then computes and prints the elapsed job time (the difference between the present job time and the initial job time).





SUBROUTINE SETUP

This subroutine controls the generation of pointers used in a sparse matrix solution of a system of linear equations or in a sparse-matrix determinant evaluation. A square integer matrix called an indicator matrix is used here. This indicator matrix records the non-zero structure of the indefinite nodal admittance matrix.

First, the indicator matrix is zeroed and the circuit topology checked for missing and single branch nodes. Next, subroutine NCODE loads element positions into the indicator matrix. Subroutine OPTORD then optimally reorders the nodes and subroutine NUMSET numbers the non-zero entries of the indicator matrix and establishes arrays which store the singly dimensioned admittance matrix locations where the element values are later loaded.



SUBROUTINE NCODE/DCODE

This subroutine loads and interprets the indicator matrix. Element nodes are received as arguments from the calling subroutine SETUP. For each element, NCODE loads non-zero values into four indicator matrix locations corresponding to locations in a square indefinite admittance matrix. Entry DCODE interprets the reordered indicator matrix by storing four locations of the singly dimensioned matrix where the element value is later loaded. SUBROUTINE NCODE/DCODE



SUBROUTINE OPTORD

This subroutine optimally reorders the nodes to minimize the number of operations required in a sparse matrix solution of a system of linear equations or in a sparse matrix determinant evaluation. The method used is equivalent to that described by Berry [6]. A pseudo Gaussian elimination is performed on the indicator matrix to establish the optimal order. The node reordering process is conducted as follows: nodes incident with voltage sources are chosen first. Next selected are all nodes which as the pivot node in a Gaussian elimination create no new non-zero entries called fill-ins. Finally, the remaining nodes are reordered choosing at each step the node which creates the least number of fill-ins. In case of ties, nodes having the greatest number of off-diagonal entries are chosen first.

SUBROUTINE OPTORD



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SUBROUTINE NUMSET

This subroutine first numbers the non-zero entries of the indicator matrix and then establishes the indirect reference pointers used in a sparse matrix solution of a system of linear equations or in a sparse matrix determinant evaluation. First, current vector entries are numbered. Next, entries on or above the matrix diagonal are numbered by rows from top to bottom and entries below the diagonal are numbered by columns from left to right. Finally, voltage source and datum node entries are numbered.

The indirect reference pointers are established in the following order: first, pointers for voltage source reduction, then pointers for the LU decomposition, followed by pointers for the forward substitution, and finally pointers for the backward substitution. For a small-signal analysis additional pointers are established for the forward substitution with the U transpose and the backward substitution with the L transpose. These additional pointers are used in computing the complex adjoint node voltages.





SUBROUTINE DCMOD

This subroutine computes the dc circuit models at the present analysis temperature. First, the saturation current, dc current gain β , basewidth modulation factor η , and the base and collector ohmic resistances are computed for each bipolar transistor. The thermal voltage and the drain and source ohmic resistances are computed for each field-effect transistor. Next, the resistor and voltage-controlled current source values are computed from the nominal values, first- and second-order temperature coefficients, and the present analysis temperature. Inductors and mutual inductance windings are modeled as 1 ohm resistances for the dc analysis. These element values are then stored for later loading into the singly dimensioned admittance matrix. Finally, the node voltage vector is zeroed and voltage source values are loaded into this vector.

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SUBROUTINE DCMOD

SUBROUTINE DCTRAN

This subroutine controls the calculation and plotting of a dc transfer curve. A single voltage or current source is stepped over a specified range. A maximum of 101 values is allowed. For each of these source values, a dc analysis is performed by calling subroutine DCANAL and a specified voltage between two nodes is stored. Next, subroutine PLOT plots this voltage as a function of the varied source. Finally, the dc circuit values are restored for the operating point dc analysis.

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SUBROUTINE PLOT

This subroutine plots the dc transfer curve. Two arrays containing the source and output voltage values are passed from the calling subroutine DCTRAN. The minimum and maximum values of output voltage are first determined. Next, a scaling operation is performed to determine the output voltage coordinates. These coordinates are then printed. Finally, each point of the dc transfer curve is printed along with the source and output voltage values.

SUBROUTINE PLOT



SUBROUTINE DCANAL

This subroutine controls the nonlinear dc analysis which computes the node voltages, transistor operating points, and power dissipation. The approach used is a modified Newton-Raphson procedure of BIAS-3 [4] in which changes in forward blased junction voltages are limited to values of less than $2V_m$ between iterations This method involves repeating a number of steps until node [7]. and transistor junction voltages agree with their previous values. First, trial transistor operating points are computed from the present set of node voltages, the nonlinear transistor models are linearized about these operating points, and a set of linear algebraic equations is assembled in terms of unknown node voltages. Next, a new set of node voltages is obtained by solving these equations and the new and old node voltage sets are compared. If there is no agreement to within 10 μ V, the new node voltage set is used to generate new trial operating points and the process is repeated. This iterative process concludes when each node voltage agrees with two previous values and each junction voltage agrees with one previous value to within 10 μ V.

The operation of DCANAL is now described. The singly dimensioned admittance matrix is first zeroed. Next, the transistor models are updated and linearized by calling subroutine BJTDC for bipolar transistors, subroutine JFET for junction field-effect transistors, and subroutine MOSFET for field-effect transistors. The resistors, inductors (modeled as 1 ohm resistors), and linearized transistor model elements are then loaded into the admittance matrix and subroutine DCSOLV computes a new set of node voltages. For circuits with no transistors, only one iteration is needed to obtain the dc solution. For circuits containing transistors, three iterations are performed before circuit convergence is checked. At each iteration the present node voltage set and the previous two sets are stored. During the fourth and all following iterations circuit convergence is checked. If the present node voltage fails to agree with the previous two sets to within 10 μ V, a new iteration is started. If agreement is reached, the present set of transistor junction voltages is compared with the previous set. If no agreement to within 10 μV , a new iteration is started. If agreement is reached, the iterative process is complete and the node voltages are printed. The transistor operating points and the circuit power dissipation are also printed for circuits containing transistors.





SUBROUTINE BJTDC

This subroutine computes the incremental bipolar transistor models used in the nonlinear dc analysis. Based on the present set of node voltages, new base-emitter and base-collector junction voltages are first determined by subroutine UPDATE. UPDATE limits a new forward biased junction voltage to changes of less than $2V_T$ from the previous value [7]. Next, eight incremental model elements (g_{mf} , $g_{\pi f}$, g_{mr} , $g_{\pi r}$, I_{CCN} , I_{CBN} , I_{ECN} , and I_{EBN}) [3] are computed. The incremental model is shown on the next page. Finally, the model elements are stored for later loading into the singly dimensioned admittance matrix and current vector.

The following equations are used to compute the incremental model elements (refer to McCalla [3] for details):

$$n = \frac{V_{T}}{V_{A}}$$

$$X = 1 - n \frac{V_{BC}}{V_{T}}$$

$$\theta = \left[\frac{C_{3}I_{SS}}{C_{1}}\right]^{1/2}$$

$$I_{CC} = \frac{XI_{SS}}{1 + \theta e^{V_{BE}/2V_{T}}} e^{V_{BE}/V_{T}}$$

$$I_{EC} = XI_{SS} e^{V_{BC}/V_{T}}$$

$$I_{CT} = I_{CC} + XI_{SS}$$





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$$\beta_{F} = \frac{X}{c_{1} + c_{2}I_{CT}^{-1/2} + c_{3}I_{CT}}$$

$$\beta_{R} = X\beta_{R0}$$

$$\beta_{0} = \frac{X\beta_{R0}}{c_{1} + \frac{1}{2}c_{2}I_{CT}^{-1/2} + 2c_{3}I_{CT}}$$

$$g_{mf} = \frac{I_{CC}}{V_{T}} \frac{1 + \frac{\theta}{2}e^{V_{BE}/2V_{T}}}{1 + \theta e^{V_{BE}/2V_{T}}}$$

$$g_{\pi f} = \frac{1}{\beta_{0}}g_{mf}$$

$$g_{\pi r} = \frac{I_{EC}}{V_{T}} + \frac{1}{XV_{T}} n(I_{CC}-I_{EC})$$

$$g_{\pi r} = \frac{1}{\beta_{R}}\frac{I_{EC}}{V_{T}}$$

$$I_{CC1} = \frac{XI_{SS}}{1 + \theta e^{V_{BE}/2V_{T}}} (e^{V_{BE}/V_{T}} - 1)$$

$$I_{EC1} = XI_{SS}(e^{V_{BC}/V_{T}} - 1)$$

$$I_{CCN} = \frac{I_{CC1}}{X} - g_{mf}V_{BE}$$

$$I_{CBN} = \frac{I_{EC1}}{\beta_{F}} - g_{\pi f}V_{BE}$$

$$I_{ECN} = \frac{I_{EC1}}{X} - \frac{I_{EC}}{V_{T}} V_{BC}$$

$$\mathbf{I}_{\mathbf{EBN}} = \frac{\mathbf{I}_{\mathbf{EC1}}}{\beta_{\mathbf{R}}} - \mathbf{g}_{\mathbf{\pi r}} \mathbf{V}_{\mathbf{BC}}$$

where:

re: V_A = Early voltage C₁,C₂,C₃ = coefficients of the current dependent forward β I_{SS} = reverse saturation current

 β_{R0} = reverse β



SUBROUTINE JFET

This subroutine computes the incremental models of junction field-effect transistors for the nonlinear dc analysis. The model used is based on the insulated-gate field-effect transistor model of Shichman and Hodges [5] [11]. Based on the present set of node voltages, new gate-drain and gate-source junction voltages are first determined by calling subroutine UPDATE. Next, the gate junction model elements (g_{GD} , g_{GS} , I_{EQGD} , and I_{EQGS}) are computed. The drain current and derivatives (g_M and G_{DS}) are then computed for either the normal mode or inverse mode depending on the polarity of the drain-source voltage. Next, an equivalent drain current source (I_{DREQ}) is computed. Finally, the model elements are stored for later loading into the singly dimensioned admittance matrix and current vector.

The following equations are used to compute the incremental model elements:

I. Gate Junction Models

$$I_{GS} = I_{S}(e^{V_{GS}/V_{T}} - 1)$$

$$g_{GS} = \frac{I_S + I_{GS}}{V_T}$$

$$I_{EQGS} = I_{GS} - g_{GS}V_{GS}$$

$$I_{GD}^{\cdot} = (e^{V_{GD}^{\prime}/V_{T}} - 1)$$
$$g_{GD} = \frac{I_{S} + I_{GD}}{V_{T}}$$

 $I_{EQGD} = I_{GD} - g_{GD}V_{GD}$

II. Drain Current and Derivatives A. Normal Mode $[V_{DS} \ge 0]$

1. Cutoff region $(V_{GS} - V_{TO}) \leq 0$

 $I_D = g_M = g_{DS} = 0$

2. Saturation region $0 \leq (V_{GS} - V_{T0}) \leq V_{DS}$ $I_{D} = \beta (V_{GS} - V_{T0}) [(V_{GS} - V_{T0}) + \lambda V_{DS}]$

$$g_{M} = \beta [2(V_{GS} - V_{TO}) + \lambda V_{DS}]$$

$$g_{\rm DS} = \beta \lambda (V_{\rm GS} - V_{\rm TO})$$

3. Linear region $(V_{GS} - V_{TO}) \ge V_{DS}$

- $I_{D} = \beta V_{DS} [(2+\lambda) (V_{GS} V_{T0}) V_{DS}]$
- $g_{M} = \beta(2+\lambda)V_{DS}$

$$g_{DS} = \beta [(2+\lambda)(V_{GS} - V_{T0}) - 2V_{DS}]$$

- B. Inverse Mode $[V_{DS} < 0]$
 - 1. Cutoff region $(V_{GS} V_{DS} V_{TO}) \le 0$

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$$I_{D} = g_{M} = g_{DS} = 0$$
2. Saturation region $0 \leq (V_{GS} - V_{DS} - V_{TO}) \leq -V_{DS}$

$$I_{D} = -\beta(V_{GS} - V_{DS} - V_{TO})[(V_{GS} - V_{DS} - V_{TO}) - \lambda V_{DS}]$$

$$g_{M} = -\beta[2(V_{GS} - V_{DS} - V_{TO}) - \lambda V_{DS}]$$

$$g_{DS} = \beta\lambda(V_{GS} - V_{DS} - V_{TO}) - g_{M}$$
3. Linear region $(V_{GS} - V_{DS} - V_{TO}) \geq -V_{DS}$

$$I_{D} = \beta V_{DS}[(2+\lambda)(V_{GS} - V_{DS} - V_{TO}) + V_{DS}]$$

$$g_{M} = \beta V_{DS}(2+\lambda)$$

$$g_{DS} = \beta[(2+\lambda)(V_{GS} - V_{DS} - V_{TO}) + 2V_{DS}] - g_{M}$$

III. Equivalent Drain Current Source

$$\mathbf{I}_{\mathrm{DREQ}} = \mathbf{I}_{\mathrm{D}} - \mathbf{g}_{\mathrm{M}} \mathbf{V}_{\mathrm{GS}} - \mathbf{g}_{\mathrm{DS}} \mathbf{V}_{\mathrm{DS}}$$

where: V_{TO} = threshold voltage β = transconductance parameter λ = channel length modulation factor I_{S} = gate junction saturation current



Incremental Junction Field-effect Transistor Model

SUBROUTINE JFET



SUBROUTINE MOSFET

This subroutine computes the incremental models of MOS fieldeffect transistors for the nonlinear dc analysis. The model used is based on the insulated-gate field-effect transistor model of Shichman and Hodges [5] [11]. Based on the present set of node voltages, new substrate-drain and substrate-source junction voltages are first determined by calling subroutine UPDATE. Next, the substrate (bulk) junction model elements (g_{BD} , g_{BS} , I_{EQBD} , and I_{EQBS}) are computed. The drain current and derivatives (g_M , g_D , and g_{MBS}) are then computed for either the normal mode or inverse mode depending on the polarity of the drain-source voltage. Next, an equivalent drain current source (I_{DREQ}) is computed. Finally, the model elements are stored for later loading into the singly dimensioned admittance matrix and current vector.

The following equations are used to compute the incremental model elements:

I. Substrate Junction Models

$$I_{BD} = I_{S}(e^{V_{BD}/V_{T}} - 1)$$
$$g_{BD} = \frac{I_{S} + I_{BD}}{V_{T}}$$
$$I_{EQBD} = I_{BD} - g_{BD}V_{BD}$$

$$I_{BS} = I_{S} (e^{V_{BS}/V_{T}} - 1)$$

$$s_{BS} = \frac{I_{S} + I_{BS}}{V_{T}}$$

$$I_{EQBS} = I_{BS} - s_{BS}V_{BS}$$
Drain Current and Derivatives
A. Normal Mode $[V_{DS} \ge 0]$

$$v_{T} = v_{T0} + \gamma [(\phi - V_{BS})^{1/2} - \phi^{1/2}]$$
1. Cutoff region $(V_{GS} - v_{T}) \le 0$

$$I_{D} = s_{M} = s_{DS} = s_{MBS} = 0$$
2. Saturation region $0 \le (V_{CS} - V_{T}) \le V_{DS}$

$$I_{D} = \beta (V_{CS} - V_{T}) [(V_{GS} - V_{T}) + \lambda V_{DS}]$$

$$s_{MBS} = \frac{s_{M}\gamma}{2} [\phi - V_{BS}]^{-1/2}$$
3. Linear region $(V_{GS} - V_{T}) = V_{DS}$

$$I_{D} = \beta (2(\lambda) (V_{CS} - V_{T}) - V_{DS}]$$

$$s_{M} = \beta (2+\lambda) (V_{CS} - V_{T}) - 2V_{DS}]$$

11.

$$g_{\rm MBS} = \frac{g_{\rm M}\gamma}{2} \left[\phi - V_{\rm BS}\right]^{-1/2}$$

B. Inverse Mode [V_{DS} < 0]

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$$V_{T} = V_{TO} + \gamma [(\phi + V_{DS} - V_{BS})^{1/2} - \phi^{1/2}]$$

1. Cutoff region $(V_{GS} - V_{DS} - V_T) \leq 0$

$$I_D = g_M = g_{DS} = g_{MBS} = 0$$

Saturation region $0 \leq (V_{GS} - V_{DS} - V_T) \leq -V_{DS}$ $I_D = -\beta(V_{GS} - V_{DS} - V_T)[(V_{GS} - V_{DS} - V_T) - \lambda V_{DS}]$ $g_M = -\beta[2(V_{GS} - V_{DS} - V_T) - \lambda V_{DS}]$

$$g_{DS} = \beta \lambda (V_{GS} - V_{DS} - V_T)$$

$$= g_{M} [1 + \frac{\gamma}{2} (\phi + V_{DS} - V_{BS})^{1/2}]$$

$$g_{MBS} = \frac{g_{M} \gamma}{2} [\phi + V_{DS} - V_{BS}]^{-1/2}$$

3. Linear region $(V_{GS} - V_{DS} - V_T) \ge -V_{DS}$ $I_D = \beta V_{DS} [(2+\lambda) (V_{GS} - V_{DS} - V_T) + V_{DS}]$ $g_M = \beta V_{DS} (2+\lambda)$ $g_{DS} = \beta [(2+\lambda) (V_{GS} - V_{DS} - V_T) + 2V_{DS}]$ $- g_M [1 - \frac{\gamma}{2} (\phi + V_{DS} - V_{BS})^{-1/2}]$

$$g_{\rm MBS} = \frac{g_{\rm M} \gamma}{2} \left[\phi + V_{\rm DS} - V_{\rm BS}\right]^{-1/2}$$

III. Equivalent Drain Current Source

$$I_{DREQ} = I_D - g_M V_{GS} - g_{DS} V_{DS} - g_{MBS} V_{BS}$$

where:

V_{T0} = threshold voltage

 ϕ = surface potential

 β = transconductance parameter

 γ = substrate threshold parameter

 λ = channel length modulation factor

 I_{S} = substrate junction saturation current



Incremental MOS Field-effect Transistor Model

SUBROUTINE MOSFET



SUBROUTINE UPDATE

This subroutine determines a new transistor junction voltage from the previous value and the new node voltages. A forward biased junction voltage is limited to changes of less than $2V_{T}$ from the previous value. The difference between the previous junction voltage and the junction voltage obtained from the new node voltages is first computed. If the magnitude of this difference is less than or equal to $2V_{T}$, the new junction voltage is the value obtained from the node voltages. If the magnitude is greater than $2V_{T}$, the polarity of this difference is checked. For a negative difference and a previous junction voltage less than or equal to $10V_{T}$, the new junction voltage is the value obtained from the node voltages. For a negative difference and a previous junction voltage greater than $10V_{\rm T}$, the new junction voltage is the previous value decreased by $2V_{T}$. For a positive difference and a value from the node voltages of less than or equal to $10V_{T}^{}$, the new junction voltage is this value. For a positive difference and a value from the node voltages of greater than $10V_{\rm T}$, the new junction voltage is the previous value increased by $2V_T$ or $10V_T$, whichever is greater. The above method is equivalent to that described by Nagel [7][11].

SUBROUTINE UPDATE



SUBROUTINE DCSOLV

This subroutine solves the sparse system of linear nodal admittance equations for the dc node voltages. First, the admittance matrix elements of the column corresponding to a voltage source node are multiplied by the value of the source and subtracted from the current vector. This is called voltage source reduction and is done for each voltage source. Next, an LU decomposition is performed on the singly dimensioned admittance matrix. This is equivalent to partitioning a square admittance matrix into upper and lower triangular matrices. Forward substitution is then performed which effectively transfers the lower triangular matrix into the current vector. Finally, backward substitution is performed resulting in the dc node voltages and voltage source currents.



SUBROUTINE DCADJ

This subroutine computes the sensitivity (partial derivative) of each bipolar transistor junction voltage with respect to each sensitivity designated resistor. The adjoint method of Director and Rohrer [8] is used. The admittance matrix is first zeroed and loaded and then an LU decomposition is performed. Finally, for each bipolar transistor junction the following steps are performed: adjoint excitation vector computation, forward substitution with U transpose, backward substitution with L transpose, and storage of the partial derivatives.

SUBROUTINE DCADJ



SUBROUTINE ACMOD

This subroutine computes the small-signal circuit models at the present analysis temperature. First, the small-signal bipolar transistor model parameters and their sensitivities (partial derivatives) with respect to the dc junction voltage are computed [3]. Next, the small-signal model parameters for the junction and MOS field-effect transistors are computed. These small-signal model parameters are computed based on the operating point of each transistor and are stored for later admittance matrix loading. The small-signal models for the three types of transistors are shown on the following pages. These small-signal transistor model parameters are then printed. Next, the values at the present analysis temperature of the resistors, voltage-controlled current sources, capacitors, inductors, and mutual inductors are computed and stored for later admittance matrix loading. Finally, the complex node voltage vector is zeroed.



Small-signal Bipolar Transistor Model



Small-signal Junction Field-effect Transistor Model



Small-signal MOS Field-effect Transistor Model



SUBROUTINE ACANAL

This subroutine controls the frequency response analysis in which the magnitude, phase, and real and imaginary parts of a specified transfer function is computed. The frequency response is obtained from a direct solution of the complex nodal admittance equations. For each frequency in the analysis, the following steps are performed: the complex admittance matrix is first zeroed and loaded with inductors, capacitors, and resistors; subroutine ACSOLV then solves the complex nodal equations; and finally the magnitude gain, db gain, phase, real part, and imaginary part of the transfer function are computed and printed.



SUBROUTINE ACSOLV

This subroutine solve the sparse system of complex nodal admittance equations. The method used is identical to that of subroutine DCSOLV except that the admittance matrix and node voltage vector are complex. The complex nodal equations are solved in four steps: voltage source reduction, LU decomposition, forward substitution, and backward substitution.


SUBROUTINE ACADJ

This subroutine solves for the set of complex adjoint node voltages in two steps. First, a forward substitution with the U transponse is performed, and second, a backward substitution with the L transpose is performed.



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SUBROUTINE PZANAL

This subroutine controls the calculation of the poles and zeros of a specified transfer function and if requested, computes a frequency response from a pole-zero derived transfer function. The poles are first computed. Subroutine SETUP sets up the sparse determinant, subroutine MULLER computes the poles, and subroutine SORT rearranges the stored poles in an ascending order in terms of the magnitudes of the real parts. The zeros are then computed in a similar manner by calling subroutines SETUP, MULLER, and SORT. Next the poles and zeros are printed. If a frequency response is also requested, the following two steps are performed for each frequency: the specified transfer function is computed from the poles and zeros; and then the magnitude gain, db gain, phase, real part, and imaginary part of the transfer function are computed and printed.



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SUBROUTINE MULLER

This subroutine solves for the zeros of a complex determinant using Muller's method [9]. First, three initial trial points are set up. The three initial points are presently chosen to be 1.0×10^6 , -1.0×10^9 , and -1.0×10^4 . Next, subroutine CDET evaluates the complex determinant at each of these three trial points. Throughout MULLER, determinant values are scaled in terms of their integer logarithm to the base two. A quadratic interpolation polynomial is constructed through the determinant values of the three trial points. This polynomial is then solved for two The smaller zero replaces the oldest of the three previous zeros. trial points and the above process is repeated until the magnitudes of two successive trial points agree to within 5.0 x 10^{-7} . This smaller zero is then checked for a negligible real or imaginary part. The real part is considered negligible if its magnitude is six orders of magnitude smaller than the magnitude of the imaginary part, and likewise the imaginary part is negligible if it is six orders of magnitude smaller than the real part. If a negligible part is found, it is set to zero. The zero is then stored and its imaginary part is checked. If non-zero, a conjugate zero exists and the entire process is repeated using the conjugates of the three trial points. If zero, the two oldest trial points generate a third trial point by Newton-Raphson approximation and the entire process is repeated. All zeros of the complex determinant are

assumed found when the magnitudes of three successive determinant values agree to within 5.0×10^{-7} .



SUBROUTINE CDET

This subroutine evaluates a complex determinant using sparse matrix techniques. The complex admittance matrix is first zeroed and then loaded with inductors, capacitors, and resistors. If the output port is not referenced to the datum (ground) node, a floating output reduction is performed. Next, an LU decomposition is performed and a determinant value is obtained. If any previously calculated zeros of the determinant exist, the determinant value is divided by the difference between each previous zero and the trial point.



SUBROUTINE LOG2

This function subroutine computes the integer logarithm to the base two of the passed argument. If the argument is zero a value of -128 is returned. The process is initialized by setting the argument to its absolute value and setting the integer logarithm to 1. If the argument is less than 1, it is doubled and the integer logarithm is decreased by 1. This is repeated until the argument is greater than or equal to 1. The present value of the integer logarithm is returned. If the argument is between 1 and two, the initial integer logarithm value of 1 is returned. If the argument is greater than 2, it is halved and the integer logarithm is increased by 1. This is repeated until the argument is less than or equal to 2. The present value of the integer logarithm is then returned.



SUBROUTINE SORT

This subroutine rearranges a set of stored complex roots so that the magnitudes of the real parts are in an ascending order. The root with the smallest real part magnitude is first found. This root becomes first in order. Of the remaining roots, the root with the smallest real part magnitude is again found. This root becomes second in order. The process continues until all the roots have been rearranged. SUBROUTINE SORT



SUBROUTINE SENSE

This subroutine controls the sensitivity analysis in which sensitivities (partial derivatives) with respect to selected passive elements called variables are computed by the adjoint method [8]. A nonlinear dc analysis is first performed with calls to subroutines SETUP, DCMOD, and DCANAL. Then a dc adjoint analysis is performed by calling subroutines SETUP, ACMOD, and DCADJ. Next the following three types of sensitivities are computed and printed for the bipolar transistors: sensitivities of dc junction voltages to the variables, sensitivities of small-signal parameters to the dc junction voltages, and sensitivities of small-signal parameters to the variables. Finally for each of the up to five specified sensitivity frequencies, the following steps are conducted: subroutine ACANAL performs an ac analysis, subroutine ACADJ computes the complex adjoint node voltages, and the sensitivities of the transfer function to the bipolar transistor small-signal parameters and to the variables are computed and printed.

SUBROUTINE SENSE



SUBROUTINE NOISE

This subroutine uses the adjoint method and computes the noise at the output port from each thermal and shot noise source in the circuit [10]. First, the equivalent noise current sources are computed and printed. These noise sources are of two types: thermal noise sources due to the circuit resistors, bipolar transistor ohmic base and collector resistances, and field-effect transistor ohmic drain and source resistances; and shot noise sources due to the dc base and collector currents of bipolar transistors and the dc drain currents of field-effect transistors. Then for each of the up to five specified noise frequencies, the following steps are conducted: subroutine ACANAL performs an ac analysis; subroutine ACADJ computes the complex adjoint node voltages; and the rms output noise, and the total rms noise referred to the input are computed and printed.



SUBROUTINE CLOCK

This subroutine is written in Control Data COMPASS assembly language and obtains the time and date of job execution. Due to its special nature, no description or flowchart is included for this subroutine.

COMMON BLOCK VARIABLES

This section lists and describes the common block variables.

NPOS(2000) - storage for the pointers to the terms of the sparse Y-matrix and current vector that are modified during a sparse matrix solution

COMMON/NAM/

TITLE(20)

- "Title card" image

COMMON/RES/

KR	-	the total number of resistors
RNAM(40)	-	names of the resistors
NR(40,2)	-	nodes of the resistors
R(40,3)	-	nominal resistances and first-order and
		second-order temperature coefficients,

respectively, of the resistors

COMMON/GM/	:		
KG		-	the total number of voltage-controlled
			current sources
GNAM(20)	•	-	names of the voltage-controlled current

sources

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-	positive and negative current source
	nodes and positive and negative control-
	ling nodes, respectively, of the voltage-
	controlled current sources

nominal transconductances and firstorder and second-order temperature coefficients, respectively, of the voltagecontrolled current sources

COMMON/CAP/

NG(20,4)

G(20,3)

KC	- the total number of capacitors
CNAM(20)	- names of the capacitors
NC(20,2)	- nodes of the capacitors
C(20,2)	- nominal capacitances and first-order
	and second-order temperature coefficients,

respectively, of the capacitors

respectively, of the inductors

COMMON/IND/

KL	- the total number of the inductors
ALNAM(20)	- names of the inductors
NL(20,2)	- nodes of the inductors
AL(20,3)	- nominal inductances and first-order and
	second-order temperature coefficients,

COMMON/MUL/

KML	•	-	the	total	number	of	mutual	inductors
AMLNAM (10)		-	name	s of	the mutu	Jal	inducto	ors

 primary winding and secondary winding
nodes, respectively, of the mutual
inductors

nominal primary self-inductances, nominal mutual inductances between the primary and secondary windings, nominal secondary self-inductances, and firstorder and second-order temperature coefficients, respectively, of the mutual inductors

COMMON/CUR/

KCS	-	the total number of current sources
CSNAM(10)	-	names of the current sources
NCS(10,2)	-	positive and negative nodes, respectively,
		of the current sources
CS (10)	-	values of the current sources

COMMON/VOL/

KVS	-	the total number of voltage sources
VSNAM(10)	-	names of the voltage sources
NVS(10,2)	-	positive and negative nodes, respectively,
		of the voltage sources
VS(10)	-	values of the voltage sources

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AML(10,5)

NML(10,4)

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NQ(30,6)

KQ	-	the	total	number	of	bipolar	and	field
		effe	ect tr	ansisto	rs			

- ONAM(30) names of the transistors
 - external collector, external base,
 emitter, internal collector, and internal
 base nodes, respectively, for the bipolar
 transistors or external drain, gate,
 external source, internal drain, internal
 source, and substrate (MOSFET's only)
 nodes, respectively, for the field-effect
 transistors

QMOD (30)	-	names of the referenced transistor models
QARF (30)	-	area factors in relation to the referenced
		transistor models

- QCUR(30) initial collector currents for the bipolar transistors
- QVOL(30) initial collector-emitter voltages for the bipolar transistors
- QTEMP(30) temperatures at which the transistors are to be maintained
- NQTYP(30) indicators denoting the types of the transistors (1 for bipolar transistors, 2 for

junction field-effect transistors, or 3
for MOS field-effect transistors)
- the total number of bipolar transistors

IBJT

IJFET	- the total number of junction field-
	effect transistors
IMFET	- the total number of MOS field-effect
· · ·	transistors

COMMON/VAR/

KV	-	the total number of variable elements
VNAM(20)	-	names of the variable elements
VSCAL(20)	-	values of the variable elements
NPE (20)	-	pointers to the variable elements
NTV (20)	-	indicators denoting the type of variable
		element (1 for resistors, 2 for voltage-
		controlled current sources, 3 for capacitors,
•		or 4 for inductors)

COMMON/BJT/

NBMOD (30)	- names of the referenced bipolar transistor
	models
VBE (30)	- base-emitter voltages of the bipolar
	transistors
VBC (30)	- base-collector voltages of the bipolar
	transistors
CC (30)	- collector currents of the bipolar
•	transistors
· CB(30)	 base currents of the bipolar transistors
COMMON/FET/	

NFMOD(30) - names of the referenced field-effect

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ITC	-	indicator denoting the type of input
•		source (0 for a voltage source or 1
		for a current source)
TCVAL1	-	initial value of the input source
TCVAL2	-	final value of the input source
TCDEL	-	increment of the input source

TCNAMO - name of the output voltage NTC1 - positive node of the output voltage NTC2 - negative node of the output voltage KNTC - pointer to the input source IVS - pointer to the input voltage source in the sparse matrix

COMMON/CNTRL/

KDC-dc analysis indicator (0 for no dc
analysis or 1 for a dc analysis)KAC-frequency response only indicator (0
for no frequency response or 1 for a
frequency response)

KPZ - pole-zero analysis indicator (O for no pole-zero analysis or 1 for a pole-zero analysis)

KALTR - altered analysis indicator (O for no altered analysis or 1 for an altered analysis)

COMMON/LIST/

KTEMP1

indicator to denote which temperature value is presently being used

KTEMP 2	- the total number of temperature values
TNOM	- the nominal temperature
TEMP (5)	- the temperature values at which the
	circuit is to be analyzed
KVARS1	- indicator to denote which variable
	source value is presently being used
KVARS2	- the total number of variable source
	values
VARNAM	- the name of the variable source
VARVAL (20)	- the variable source values
KNOIS1	- indicator to denote which noise analysis
	frequency is presently being used
KNOIS2	- the total number of noise analysis
	frequencies
FNOIS(5)	- the noise analysis frequencies
KSENS1	- indicator to denote which sensitivity
	analysis frequency is presently being
	used
KSENS2	- the total number of sensitivity analysis
	frequencies
FSENS(5)	- the sensitivity analysis frequencies

- COMMON/TRFN/
 - NOUT

indicator to denote the type of small-signal output (1 for voltage output or 2 for current output)

the positive output node

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NOM	-	the negative output node
NINP	-	indicator to denote the type of small-
		signal input (1 for voltage input or
		2 for current input)
NIP	-	the positive input node
NIM	-	the negative input node
PLIM	-	the upper frequency limit for poles
ZLIM	-	the upper frequency limit for zeros
KFREQ	-	indicator to denote the type of frequency
		variation (1 for no frequency response,
		2 for logarithmic variation, or 3 for
		linear variation)
GOUT	-	the conductance across the output nodes
DIV	-	the number of points per decade for a
		logarithmic frequency variation, or the
		number of frequency points for a linear
		frequency variation
FMIN	-	the initial frequency
FMAX	-	the final frequency
GSCAL	-	the small-signal analysis scale factor
•		for conductances
CSCAL	-	the small-signal analysis scale factor
_		for capacitances
ALSCAL	-	the small-signal analysis scale factor
		for inductances
FSCAL	-	the small-signal analysis scale factor
		for frequencies

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COMMON/CRKT

VALU(500)	- temporary storage for the v	values of
	all elements (including tra	nsistor
	model elements)	· .
KODE (500)	- indicators denoting each el	lement type
LOC1 (500)		
LOC2 (500)	temporary storage for the r	nodes of
LOC3(500)	all elements	
LOC4 (500))	
NELT	- the total number of element	ts

COMMON/NODE/

VDC(101)	-	dc node voltages
VAC (101)	•	complex ac node voltages
PSIDC(101)	-	dc adjoint node voltages
PSIAC(101)	-	complex ac adjoint node voltages
NINC(101)	-	number of incident branches to each
		circuit node
NORD (101)	-	the user specified nodes
NLOC (101)		the optimally ordered nodes
NMAX	-	the maximum user specified node number
NDMR	-	maximum number of rows in the indicator
5		matrix
NDMC	-	maximum number of columns in the indicator

matrix

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COMMON/SPARSE/

NMOD

maximum number of user specified nodes

- 4

number of elements in the upper-triangular

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NLT	-	number of elements in the lower-triangular
		matrix
NTOT	-	total number of elements in the singly
		dimensioned admittance matrix and current
		vector
NADJ	-	starting pointer for ac adjoint analysis
NFO	_	number of extra elements due to floating
		output
NVC (10)	-	number of non-zero entries in the rows
		with voltage sources
NUR (101)	-	number of non-zero entries in each row
		of the upper-triangular matrix
NLC (101)	· •	number of non-zero entries in each column
		of the lower-triangular matrix
NFS (101)	-	number of entries per column used in forward
		substitution
NBS (101)	-	number entries per row used in backward
		substitution
COMMON/FILE/		
CARD (80)	-	temporary storage for eighty column data
		card
COL (80)	-	error pointers for an eighty column data
•2.		card
FNUM	-	floating point free-format value

matrix

NUT

IPT- data card column that is being processedISTRT- starting column of free-format field that

is being processed

 indicator to denote continuation card
 (0 for non-continuation cards and 1 for continuation cards)

- number of errors on a card

 indicators denoting the types of card errors

indicator to denote the type of card for keyword interpretation (1 for bipolar transistor model cards, 2 for PRINT cards, and 3 for field-effect transistor model cards)

COMMON/BJTMOD/

INUM

ISET

NERR

KERR(80)

IPARAM

KBMOD

BNAM(10) BMOD(40,10) - the total number of bipolar trnasistor models

names of the bipolar transistor models bipolar transistor model parameters (both user-defined and computed): 1. type (+1.0 for NPN or -1.0 for PNP) 2. $\beta_F : \beta_{FMAX}$

- 3. ^ICMAX
- 4. ^βFLOW

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			· .	· ·	4
γ •	•	5.	•	ICLOW	
		6.	•	V _{CE}	
		7.		^T C1	•
		8.		^T C2	•
		9.	β _R		
•••		10.	r ₀ :	r ₀	
•		11.		I C	•
		12.		V _{BE}	
		13.		V _{CE}	
44 m * *	•	14.	r _B :	r _B	
· · ·		15.	. •	^T C1	•
		16.		^T C2	
		17.	r _C :	r _C	
		18.		TC1	- - -
		19.	- · ·	^T C2	
· · ·		20.	f _T :	fT	•
		21.		^I C	
•		22.		VCE	•
		23.		L _E /W _B	
		24.		I ^{CO}	
		25.	^t SAT		•
	•	26.	C _{je} :	^C je	
· · · · · · · · · · · · · · · · · · ·		27.		V _{BE}	. •
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 V_{BC}

 33.
 ϕ_C

 34.
 ratio

 35.
 C_{SUB}

 36.
 temperature

 37.
 I_S

 38.
 τ_F

 39.
 V_A

	BCC(10,3)	- three coefficients that model F vs. IC
	CSO(19)	- reverse saturation currents at their
		· defined temperatures
-	ETA(10)	- basewidth modulation factors at their
		defined temperatures
	CJ0(10,2)	- zero bias values of C _{je} and C _{jc} ,
		respectively
	TAUO (10)	- forward transit times at their defined

temperatures

IV. CLOSING NOTES

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SLIC has undergone a number of changes which provide for more versatile use. However, there are two areas where improvement could be made. First, a considerable amount of core storage could be reduced by eliminating the use of a square indicator matrix in the sparse matrix set up. With the 100 node capability, a 101 by 101 square matrix or approximately 10,000 words of core storage is needed. Assuming that circuits will contain no more than 10 incident branches to each node, then only 1,000 (100 nodes times 10 off-diagonal terms) words of core storage will be needed. The time required to set up the sparse matrix would also be reduced since the sparse square indicator matrix would not have to be searched for non-zero terms. Changes to subroutines SETUP, NCODE, OPTORD, and NUMSET would be required. The second area concerns the way transistor data is stored. Presently, all types (bipolar, junction field-effect, and MOS field-effect) of transistor data are stored together in one storage area. Since each transistor type has a different model, a search is required to find the transistors of each type. This searching could easily be eliminated by creating a separate storage area for each transistor type.

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