LOW-PHASE-NOISE, LOW-TIMING-JITTER DESIGN TECHNIQUES FOR DELAY CELL BASED VCOS AND FREQUENCY SYNTHESIZERS

by

Todd Charles Weigandt

Memorandum No. UCB/ERL M98/5

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
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Abstract

Low-Phase-Noise, Low-Timing-Jitter Design Techniques for Delay Cell Based VCOs and Frequency Synthesizers

by

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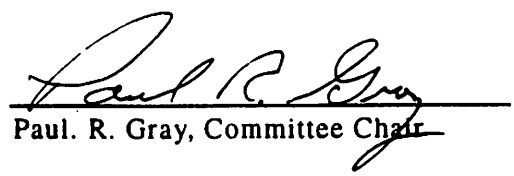
Timing jitter and phase noise are important design considerations in almost every type of communications system. Yet the desire for high levels of integration in many communications applications works against the minimization of these, and other, sources of timing error - especially for systems which employ a phase-locked loop for timing recovery or frequency synthesis. With the growing interest in high-integration implementations there has been an increasing demand for fully-monolithic, on-chip VCO and synthesizer designs. Delay cell based VCOs (ring-oscillators) and delay chains have been used successfully in many applications, but thermal-noise induced timing jitter and phase noise have limited their applicability to some systems. Of particular interest are RF frequency synthesizers, used in wireless communications transceivers, which have stringent requirements on oscillator phase noise but stand to benefit greatly from a highly integrated solution.

In this thesis the fundamental performance limits of ring oscillator VCOs and delay buffers are investigated. The effects of thermal noise in transistors on timing jitter and phase noise in such these circuits is explored, with particular emphasis on source-coupled differential resistively-loaded CMOS delay cell implementations. The relationship between delay element design parameters and the inherent thermal noise-induced

jitter of the generated waveform are analyzed. These results are compared with simulated results from a Monte-carlo analysis and experimental results for a ring-oscillator test array fabricated in 0.6μm CMOS technology with good agreement. The implications of this analysis for the design of low-timing-jitter and low-phase-noise buffers, VCOs and PLLs using inverter delay cells are described.

The analysis shows that timing jitter is inversely proportional to the square root of the capacitance at the output of each inverter, and inversely proportional to the gate-source bias voltage above threshold of the source-coupled devices in the balanced state. Furthermore, these dependencies imply an inverse relationship between jitter and power consumption for an oscillator with a fixed output period. Phase noise and timing jitter are predicted to improve at a rate of 10 dB per decade increase in power consumption (and area). For a given output frequency and power consumption an oscillator with a minimum number of delay cell elements is desired to minimize timing jitter. These conclusions, as well as many practical considerations for ring-oscillator VCO design are described. The results show that delay cell based VCOs and synthesizers have significant potential for at least some range of RF frequency synthesizer applications.

Approved By: 

Paul. R. Gray, Committee Chair

In loving memory of my grandparents

Charles and Helen Weigandt

TABLE OF CONTENTS

CHAPTER 1

Introduction

1.1 Motivation 1

1.2 Thesis Organization 4

CHAPTER 2

Jitter and Phase Noise in Communication Systems

2.0 Introduction 5

2.1 Timing Signals in Communication Systems 6

2.2 Introduction to Phase-Locked Loops 11

2.3 Timing Jitter and Phase Noise 17

2.3.1 Phase Noise in Oscillators 17

2.3.2 Timing Jitter in Oscillators 20

2.3.3 Phase Noise and Timing Jitter in Buffers and Delay Cells 22

2.3.4 Phase Noise in Phase-Locked Loops 24

2.3.5 Timing Jitter in Phase-Locked Loops 26

2.3.6 Timing Jitter / Phase Noise Summary 29

2.4 System Impact of Timing Errors: Sample Applications 31

2.4.1 Clock Synchronization in High Bandwidth Digital I/O Interfaces 32

2.4.2 Clock Drivers for A/D Conversion 34

2.5 References 37

CHAPTER 3

RF Frequency Synthesizer Design

3.0 Introduction 41

3.1 RF Transceivers for Wireless Communications 41

3.1.1 System Level Impact of Phase Noise and Spurious Tones 44

3.1.2 Requirements for Different Synthesizer Applications 48

3.2 Frequency Synthesizer Design 53

3.2.1 Synthesizer Architectures and Components 54

3.2.2 Phase Noise and Spurious Tones 58

3.3 References 68

CHAPTER 4

Jitter in CMOS Ring Oscillator Delay Cells

4.0 Introduction 70

4.1 Related Analyses of Jitter and Phase Noise in Oscillators 72

4.2 Individual Delay Cell Timing Jitter 74

4.2.1 Modeling Circuit Noise Induced Timing Jitter 78

4.2.2 First Pass: Simplified Analysis 84

4.2.3 Second Pass: Advanced Analysis 89

4.2.4 Third Pass: Complete Analysis 102

4.3 Implications for Low-Jitter Delay Cell Design 113

4.4 Conclusions 117

4.5 References 120

CHAPTER 5

Jitter and Phase Noise in CMOS Ring Oscillators and Buffers

5.0 Introduction 122

5.1 Timing Jitter in Ring Oscillator VCOs 123

5.1.1 Timing Jitter as a Function of Power Consumption 125

5.1.2 Timing Jitter as a Function of Configuration 126

5.1.3 Timing Jitter as a Function of Output Period 128

5.1.4 Common Misconceptions in Low-Jitter VCO Design 129

5.2 Phase Noise 131

5.2.1 Phase Noise / Timing Jitter Relationship 134

5.2.2 Phase Noise in Ring Oscillators 136

5.3 Timing Jitter and Phase Noise in Buffers and Delay Chains 140

5.3.1 Timing Jitter in Buffers 140

5.3.2 Phase Noise in Buffers 141

5.4 References 144

CHAPTER 6

Ring Oscillator VCO Design

6.0 Introduction 145

6.1 Basic Delay Cell Design 146

6.1.1 Voltage Swing Considerations 148

6.1.2 Gain Considerations 150

6.1.3 Biasing Considerations 151
6.2 Ring Oscillator VCO Design 154
6.2.1 Oscillator Frequency Limits 155
6.2.2 VCO Center Frequency Variation 157
6.2.3 VCO Control Path Tuning 160
6.2.4 Lower Frequency Ring-Oscillator Design 163
6.3 Delay Cell Design and Implementation 164
6.3.1 VCO Tuning 167
6.4 References 169

CHAPTER 7

Experimental Results

7.0 Introduction 170
7.1 Ring Oscillator VCO Results 170
7.2 Jitter and Phase Noise Results 175
7.2.1 Transient Noise Simulations 176
7.2.2 Phase Noise Measurements 182
7.3 References 187

CHAPTER 8

Conclusions 188

Appendix A 191

Autocorrelation Function Analysis for Time-varying Noise Sources

Appendix B 202

Autocorrelation Function Analysis with Interstage Gain Considerations

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Chapter 1

Introduction

1.1 Motivation

In most modern communication systems timing information, in the form of clock or oscillator signals, plays a critical role in system performance. In many of these applications, clock signals are used to drive mixers or sampling circuits in which variations in the sampling instant, both random and systematic, are important performance parameters. For some systems, the timing information is provided through a local crystal oscillator, or an externally supplied timing source. In this case, the task of minimizing timing error amounts to minimizing the noise introduced through the distribution and buffering of clocks in the system. In many other applications, however, a local version of the clock is required at a different frequency or phase than the reference, in which case a phase-locked-loop (PLL), or similar circuit, is often employed to create the required signal. For systems such as these, minimizing timing error requires careful attention to all of the sources of noise in the PLL, and their interactions in the PLL system as a whole.

Applications which require phase-locked-loops are often the most challenging, since attaining high performance levels often contributes considerable expense and

complexity to the system. Furthermore, for any given application, there are a number of different timing error sources which may be important to the system. Systems which employ PLLs include applications such as optical communication systems, disk drive systems, and local area networks, where a PLL is used for clock and data recovery. Other systems include radio transmitters and receivers which use phase-locked-loops for frequency synthesis. And, in complex digital systems such as microprocessors, network routers, and digital signal processors, the clocks used at various points in the system are often synchronized through a phase-locked or delay-locked loop to minimize clock skew.

The are several types of timing error, or uncertainty, that are important in communication systems. The first is random variations in the sampling phase of a signal, called timing jitter, or in the frequency domain, phase noise. This is often due to thermal noise and 1/f noise in the active and passive devices which make up the components of the PLL system, particularly the voltage-controlled-oscillator (VCO). In addition, systematic variations in sampling phase can occur due to injection of signals from other parts of the circuit causing AC variation in the phase, called spurious tones. Sudden changes in the supply or substrate can also cause frequency offsets and phase drift. These sources of noise can often be minimized through advanced circuit techniques. The effect of device thermal noise, however, is fundamental, and in applications such as RF frequency synthesis, it often sets the performance limit for the system.

In most RF frequency synthesis applications, a low phase noise oscillator is employed for optimal performance. This usually requires an external resonator, such as a varactor tuned LC-tank, with a high quality factor ("Q"). In an increasing number of applications, however, a fully-monolithic solution to the VCO is desired. Already present in clock synthesis and clock recovery applications, on-chip ring-oscillators and voltage-controlled-delay chains have resulted in a reduced cost and complexity in many systems. But the phase noise requirements of radio receiver applications is generally more restrictive, raising questions as to their applicability for RF frequency synthesis.

This dissertation describes the fundamental, thermal noise-induced performance limits in ring-oscillator VCO's and their applicability to RF frequency synthesis. Design techniques for low phase noise and low timing jitter circuits are described, that are useful to all applications. The key trade-offs available to the designer at the buffer/ delay cell level, the oscillator level, and the phase-locked loop level are all explored. Furthermore, this dissertation describes the design of frequency synthesizers for high-integration radio receivers, where a monolithic implementation to the VCO is desired. Comparisons are made with other implementations, including implementations with on-chip LC-tuned circuits.

The key contributions of this work are:

1. An analytical method for analyzing thermal noise-induced timing jitter in delay stages, taking into account time varying noise sources and interstage amplification. With this technique the jitter performance of CMOS differential, resistively loaded, source-coupled delay cells has been tied to delay cell design parameters and shown to have an inverse dependence on the square root of the load capacitance at the output of each inverter stage and an inverse dependence on the gate-to-source bias above threshold of the source coupled devices in the balanced state.

2. The application of delay cell jitter analysis to low-timing-jitter, low-phase-noise design techniques for buffers, ring-oscillator VCOs, and phase-locked-loops. Timing jitter and phase noise performance for each of these applications have been tied together. Improvements of 10 dB per decade increase in power consumption (and area) are predicted for a fixed output period. Timing jitter, for a fixed output period and power consumption, is shown to be minimized by a ring-oscillator with a minimum number of delay cells.

3. The design and implementation of ring oscillator VCOs using the above mentioned delay cell topology has been described, including issues such as coarse and fine tuning, maximum frequency of operation, and design of low frequency VCOs.

4. Experimental and monte-carlo simulation results for a ring-oscillator test array fabricated in a 0.6μ, double-poly double-metal CMOS process are described, which show good agreement with the analytical predictions for timing jitter and phase noise.

1.2 Thesis Organization

In chapter two an overview of timing error sources in various communications applications will be presented. In particular, the effects of timing jitter and phase noise at several levels of system implementation will be discussed. Chapter three is an introduction to frequency synthesizers and the issues concerning the design of local oscillators for highly integrated RF transceiver applications. In chapter four the analysis of timing jitter and phase noise is initiated with a look at thermal noise induced timing jitter in inverter delay cells. This analysis is extended in chapter five to determine the implications for low-jitter and low-phase VCO design. Expressions for timing jitter and phase noise at several levels of system implementation will be derived in terms of basic delay cell and oscillator design parameters. In the following chapter, chapter six, the circuit implementation of ring-oscillators and delay cells will be described. And in chapter seven, experimental results and simulation results will be provided.

Chapter 2

Jitter and Phase Noise in Communication Systems

2.0 Introduction

Timing jitter and phase noise are important considerations in a number of communications applications. Timing errors in the clock or oscillator signals used by a system can limit the maximum speed of a digital I/O interface, the bit error rate of a communications link, or even the dynamic range of an A/D converter. And these are only a few of many examples. Furthermore, in many of these applications a phase-locked-loop, or similar circuit, is required to generate the necessary timing signals. Minimizing the timing errors in a phase-locked-loop involves attention to a number of important factors.

The goal of this chapter is to outline the impact of timing signal errors, and timing jitter and phase noise in particular, on communication systems. The first step in this outline involves answering basic questions such as: what are the different roles a timing signal can take in a communication system?, how are timing signals generated in different applications?, what are the different types of errors a timing signal can posses?, what are their sources? and how do these errors effect system performance? These questions will be touched on at the beginning of the chapter, followed by a brief introduction to phase-locked-loops. Next, a detailed summary of phase noise and timing jitter in

buffers, VCOs and PLLs will be given. And finally, the impact of timing jitter, and other error sources, on several sample applications will be described. In the next chapter an even more detailed look at one particular application, RF frequency synthesis, will be provided.

2.1 Timing Signals in Communication Systems

Timing signals play a number of different roles in communication systems. In digital systems, for example, clock signals are used to transfer logic signals in and out of registers at times when their values are valid. The maximum clock frequency is usually limited by the propagation delay of the logic circuits between registers. In high bandwidth digital I/O systems, however, the date transfer rate can be limited by uncertainty in the clocks used to transfer the data [1 - 5]. This uncertainty is comprised of fixed skew (or offsets) between the transmit and receive clocks, timing jitter due to noise, and modulation of the timing source due to coupling from interfering signals elsewhere in the system.

Timing signals in the form of clocks are also used to drive the sampling circuits found in the signal paths of many communication systems. Sampling circuits are used in A/D converters and in discrete time analog signal processing circuits, such as switched capacitor filters. Clock signals are also important for the generation of continuous signals from discrete time samples, as well (e.g. D/A conversion). Usually the errors that are important in a signal processing application are noise, distortion and offsets due to non-idealities in the circuit elements which make up the signal path. Thermal noise, non-linearities, and mismatch in devices are all key contributors. However, the effects of errors in the time base of the signal, due to timing jitter or modulation, can also limit the dynamic range and other performance parameters of the system [6,7].

A third role of timing signals is as oscillator signals for frequency translation in narrowband communication systems. RF and microwave radio transceivers use local oscillators to drive mixing circuits which up-convert or down-convert narrowband sig-

nals for transmission or reception over the air waves [8,9,10,11]. Phase noise and spurious tones (due to frequency modulation) in the oscillator signal can limit the "selectivity" of a radio system - the ability to receive a desired signal in the presence of strong interferers. This topic will be addressed in great detail in chapter 3.

And finally, a fourth role of timing signals, is as the communications signal itself. In many digital and analog communications systems, the information is not stored in the amplitude of the signal but in the phase of frequency of the signal being transmitted across the communications channel. Examples include QPSK and FSK digital communications formats [12, 13], as well as analog communication applications such as AM or FM radio [14]. The transceivers in many of these applications use the internal signals of a PLL to modulate or demodulate the desired information. Timing errors in these systems can effect the signal information itself.

The different types of timing errors encountered in electronic systems can be loosely classified by the four categories depicted in figure 2.1. As described in the

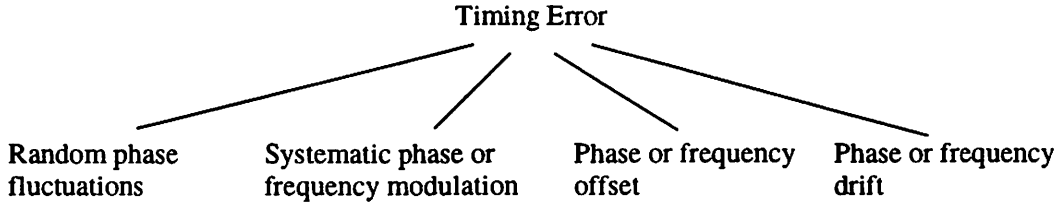


Figure 2.1 Types of timing error and uncertainty

introduction, random variations in the phase, called timing jitter or phase noise, are often the result of thermal noise and 1/f noise in the active and passive devices that make up a circuit. The noise present in oscillators is particularly important since a phase error during one period of oscillation determines the starting point of the next, effecting the future time-base of the signal in that manner. In clock buffers on the other hand, noise can effect the phase from one cycle to the next, but the inherent time-base of the signal, which depends on the oscillator that is its source, is not directly affected.

A more detailed description of this phenomenon will follow. In clock and data recovery applications, the clock signal used for interpreting incoming data is generated locally based on transitions in the incoming data stream. Different patterns of data in the incoming data stream may provide slightly different timing estimates, which can result in modulation of the phase of the sampling clock. This type of modulation is called signal dependent timing jitter. Although the modulation of the timing waveform is systematic for a given input sequence, the sequence itself is random and the net effect on the receive clock is a random variation.

A second category of timing errors, shown in figure 2.1, is systematic variations in the phase of a signal due to interfering signals from elsewhere in the circuit. Interfering signals may be coupled to a clock or oscillator signal, inadvertently, through the power supply or substrate. In other cases they may be unavoidable signals, such as reference feed-through in a PLL, which are inherent to the operation of the circuit. In the frequency domain, this type of interference results in spurious modulation tones in the sidebands of the oscillator spectrum, often referred to as spurious tones. In the time domain, modulation can cause an AC variation in the phase of a signal in addition to timing jitter[1]. If random fluctuations in phase can be thought of as timing "noise", then systematic phase fluctuations can be thought of as timing "distortion".

A third category of timing errors are DC errors, or offsets in phase or frequency between different parts of a system. Clock skew, for example, can result when a clock is used in different parts of a widely distributed system. The added delay of a clock buffer, in some systems, may also skew the position of the clock edge relative to the data. These errors, as mentioned before, can limit the maximum speed of operation for the system. Frequency offsets are also concern. Frequency matching between a transmitter and receiver in a narrowband communications system depends on how well the reference crystals at each end match. In other applications, such as quadrature modulators,

---

1. The phrase timing jitter is sometimes used in the literature to refer to systematic variations in phase (such as AC modulation) as well as random variations. In this writing, however, the term *timing jitter* will be used exclusively to refer to a random variations in phase.

the matching of I and Q phase oscillator signals is limited by device mismatch between the two timing paths. Phase offsets in these systems can result in incomplete rejection of the unwanted modulation sideband.

And finally, the fourth category of timing errors shown in figure 2.1 is phase or frequency drift. This category is used to describe long term, or occasional variations in the phase or frequency of a signal. Examples include drift of an oscillator due to temperature variations. Glitches in the power supply due to changes in operating conditions (like a microprocessor suddenly going into a high-activity mode), can also change the frequency of a timing source. This can result in a large phase error when accumulated over several cycles of oscillation [4]. Another example, found in RF systems, is the "pulling" of the VCO frequency when the power amplifier turns on.

Up to this point in the section we have discussed the different roles of timing signals in communications systems and the types of timing errors that a signal can posses. We have also mentioned a few examples of the sources of timing errors and some of the possible impacts on system performance. The last part of this introduction involves the different ways in which a timing signal can be generated.

As mentioned in chapter 1, timing information in many systems comes from a local crystal oscillator or an external reference in which case the task of minimizing timing errors amounts to minimizing the noise, offsets, etc. introduced in the buffering and distribution of the clock throughout the system. This scenario usually has the lowest timing jitter and spurious modulation since noise or interference introduced downstream of the crystal oscillator does not influence the oscillator's internal time-base directly.

A number of other communication systems, however, require phase-locked-loops, or similar circuits, to generate clock or oscillator signals. These applications are often the most interesting, from a timing signal perspective, since the timing signal generation may be a significant part of the overall system, and since PLLs are more sensitive to noise and interference. Examples of applications which use PLLs include clock

and data recovery, clock synthesis or synchronization, frequency synthesis, and PLL modulator or de-modulator applications. In clock and data recovery applications the PLL is used to generate a synchronized sampling signal, where none existed before, from transitions in the incoming data stream [13,15,16,18]. Clock synchronization systems use a PLL to lock a local clock signal, generated by a VCO, to an incoming clock signal that already exists. In this way, skew between the data and clock signals can be eliminated, even when there are delay differences between the two paths due to clock buffering and other factors[1,2]. In some designs, such as high frequency microprocessor implementations, an internal clock is needed at a higher frequency than the external reference. In this case the PLL clock generator is actually a frequency synthesizer [4,5]. Other frequency synthesizer applications include RF transceiver applications where a number of closely spaced RF local oscillator frequencies need to be created to select the desired incoming channel [8,9,19]. A high frequency VCO can be locked to a high-accuracy (low frequency) crystal reference to get the desired RF output frequency. Changes in the divide ratio of the PLL can be used to tune the output to the desired frequency (this will be discussed in detail in the next chapter). And finally, the internal signals of a PLL may also be used for modulation, or demodulation, in communication applications where the signal information is contained in the phase or frequency of the signal itself [12, 13]. A number of different examples of PLL and non-PLL based timing signal applications are summarized in table 1.

Table 1: Applications areas and examples.

PLL Based Applications

PLL Based Clock and Data Recovery

- Fiber optic data transceivers [20, 21]
- Disk drive read channels [22]
- Local area network transceivers [15]
- DSL transceivers [24]

PLL Based Clock Synthesis / Synchronization

- Internal, de-skewing PLL clock generators for microprocessors, DSP, and DRAMs [1,2,4,5]
- Clock generators for network router/switchers [23]
- RAMDAC clock generators [25]

PLL Based Frequency Synthesis

- Local oscillators for RF or microwave transceivers [19, 46]

PLL Modulator and Demodulators

- Non-coherent mod./demod. in communications [13, 26, 37]

Non-PLL Based Applications

Clock buffer / drivers

- A/D and D/A converter clock drivers [27]
- Local oscillator buffers [28]

Other clock and frequency synthesis, clock recovery

- Crystal oscillators [29,30]
- Direct frequency synthesis [31,32]
- Non-PLL based clock recovery for DSL, disk drive channels, etc. [12, 13]

2.2 Introduction to Phase-Locked Loops

Since phase-locked-loops are important to a number of the applications consid-

ered here, some introductory remarks are in order. For an introduction to PLLs the texts in [37] and [38] are highly recommended. This is a very broad topic, since phase-locked-loops, and similar circuits are used in so many different applications. Most phase-locked-loops (PLLs) have the basic structure of the system in figure 2.2. There

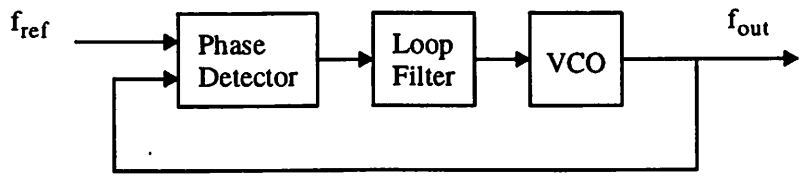


Figure 2.2 Basic PLL block diagram

are many variations however, since each of the components can be implemented in unique ways. Digital implementations exist for many components and, in some lower frequency applications, the entire PLL can be implemented in the digital domain [39,40]. Furthermore, new architectures are being used, such as the delay-locked-loop, which have a similar function to a PLL, but differ in significant ways, often particular to a given application [41, 42]. Understanding the operation of the PLL in figure 2.2, however, is still a good starting point. In addition, many of the more challenging applications, (higher frequency, higher-performance) still rely on a traditional and mostly analog PLL.

The components of a basic phase-locked-loop (PLL) generally include a phase detector, loop filter, and a voltage-controlled-oscillator (VCO). A phase detector is capable of comparing the phase of two signals and producing an output (usually a voltage) proportional to the difference. A low-pass filter is generally used to filter the error signal coming from the phase detector and is designed to correctly compensate the feedback loop in the PLL. The voltage-controlled-oscillator produces an output frequency that is proportional to the voltage at its input. Also, since phase is the integral of fre-

quency over time, controlling the voltage over time can be used to control the output phase, as well.

As illustrated in the previous section, there are many different applications of PLLs. Some of these applications differ in the types of input signals applied, the use of the VCO output, or other modifications to the signal in the loop. However, at heart of all of them is the basic phase-locking operation of the PLL. This is usually described by an s-domain model for the phase at various points in the system. If the response of the components in a PLL are linearized, then for small perturbations in phase the small-signal, AC model of the PLL in figure 2.3 can be applied.

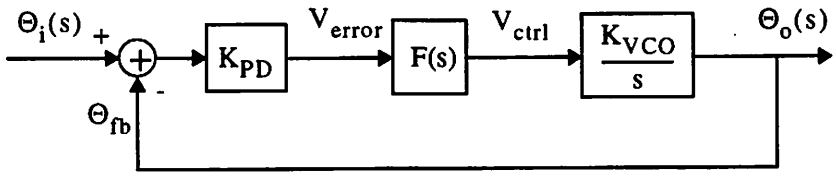


Figure 2.3 Linearized, small-signal, AC, model of phase-locked-loop

In this model the phase of the output is compared to the input through the phase detector, and an error signal proportional to the difference is produced. The constant of proportionality is the phase detector gain, which generally has units of volts /radian (the error signal can also be a current or charge, however).

$$V_{error}(s) = K_{PD} \cdot (\Theta_i(s) - \Theta_{fb}(s)) \tag{1}$$

The error signal is low-pass filtered by the loop filter with transfer function F(s), and used to drive the VCO. The VCO output frequency is generally given by an equation such as

$$f_{out} = f_c + K_{VCO} \cdot V_{CTRL} \tag{2}$$

where f_c is the nominal or free running frequency of the VCO with a control voltage of

zero. The output phase is the integral of frequency over time. Assuming that the loop has first attained frequency lock between the input and the output, then the small signal phase at the output is given in the s-domain by

$$\Theta_o(s) = \frac{K_{VCO}}{s} \cdot V_{CTRL}(s) \tag{3}$$

where the factor of 1/s is due to the integration. Putting all of these pieces together, a negative feedback loop is attained with a closed loop transfer function of

$$H(s) = \frac{\Theta_o(s)}{\Theta_i(s)} = \frac{K_{PD}K_{VCO}F(s)}{s + K_{PD}K_{VCO}F(s)} \tag{4}$$

The exact nature of the transfer function in equation (4) is not clear until an expression for the loop filter is given. In its simplest form F(s) could be a mere constant, representing gain or attenuation. In that case the loop is a first order system. More practical implementations however, use a low-pass filter for F(s) which adds another pole to the system. This allows more flexibility in the design of the PLL and trade-offs in its performance parameters. However, the addition of a second pole to the system usually requires a compensating network to be added to the filter to guarantee stability. One of the most common loop filters has a pole at the origin and a zero at a frequency, $\omega_z = 1/\tau_z$, just below the unity gain frequency of the PLL loop transmission. In this case

$$F(s) = K_F \cdot \frac{(\tau_z s + 1)}{s} \tag{5}$$

and

$$H(s) = \frac{\Theta_o(s)}{\Theta_i(s)} = \frac{K_{PD}K_{VCO}K_F(\tau_z s + 1)}{s^2 + K_{PD}K_{VCO}K_F\tau_z s + K_{PD}K_{VCO}K_F} \tag{6}$$

The resulting PLL transfer function in (6) is that of a second order system and is characterized by its natural frequency, ω_n, and its damping factor, ζ. This is described in detail in most references on phase-locked-loops [37], [38] (also see [1]). The general

form for a second order system is given by:

$$H(s) = \frac{\Theta_o(s)}{\Theta_i(s)} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{7}$$

In this example

$$\zeta = \frac{1}{2} \cdot \omega_n \tau_z \tag{8}$$

and

$$\omega_n = \sqrt{K_{PD} K_{VCO} K_F} \tag{9}$$

The topic of loop-filters and the overall PLL system design will be covered in more detail in later chapters. At this point, however, our purpose is to show just two ideas. First, the phase at various points in the system can be modeled in the s-domain. And, second, the response of a PLL to various phase disturbances will depend on the overall action of the loop, which depends on the bandwidth and damping factor that characterize it.

The equation in (4) is useful for determining phase disturbances at the output of the system in response to phase perturbations at the input. Similar transfer functions can be derived for disturbances injected at other points in the system, such as those in figure 2.4. The response to voltage noise injected at the output of the loop filter, for example is

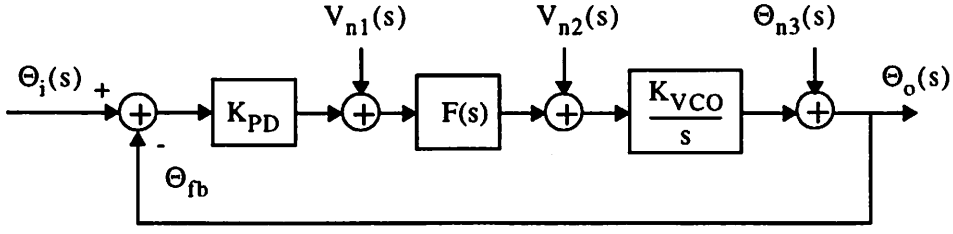


Figure 2.4 Linearized, small-signal AC model with noise sources

$$\frac{\Theta_o(s)}{V_{n2}(s)} = \frac{s \cdot K_{VCO}}{s^2 + K_{PD}K_{VCO}K_F\tau_z \cdot s + K_{PD}K_{VCO}K_F} \tag{10}$$

where the loop filter in equation (5) has been assumed. Also, the response to phase errors injected by the VCO can be determined from

$$\frac{\Theta_o(s)}{\Theta_{n3}(s)} = \frac{s^2}{s^2 + K_{PD}K_{VCO}K_F\tau_z \cdot s + K_{PD}K_{VCO}K_F} \tag{11}$$

Notice that this transfer function is a high-pass filter. For $\omega \gg \omega_n$ the result in (11) approaches unity.

As a final piece of this introductory section on PLLs some remarks on the acquisition of phase-lock are in order. The small-signal AC model described in this section applies to PLLs which have attained lock and are in equilibrium. The process by which a PLL reaches this point is related to the operation of the components in the loop. When the loop is first turned on the VCO center frequency is not likely to be the exact output frequency needed for steady state operation. The phase detector indicates whether the phase of the fed-back signal is early or late and speeds up or slows down the VCO accordingly. If the center frequency is not too far from the desired output frequency then the low pass filtered phase detector error signal can drive the VCO to the desired frequency, after which phase locking ensues. On the other hand, if the frequency difference is too great then the phase of the VCO may "wrap-around" causing the phase detector to mistake an early signal edge for a late edge. With wide enough differences in frequency, this situation can persist and phase-lock is not attained. The range of frequencies over which acquisition can occur is called the capture range of the PLL. Many practical phase detectors provide useful frequency update information during frequency acquisition to enable a wide capture range [37]. The time required for acquisition also depends on details of the phase detector and the PLL loop bandwidth [37], [38]. Wider loop bandwidths result in faster acquisition times.

2.3 Timing Jitter and Phase Noise

Since timing jitter and phase noise are critical to a number of applications, a closer look at them is in order. Both are manifestations of random variation in phase. One is the time domain characterization of this error. The other is its frequency domain characterization. Timing jitter and phase noise can be further classified by category and a distinction can be made between timing jitter in a clock buffer, jitter in a VCO, and jitter in a PLL. Likewise for phase noise. In this section a brief overview is attempted of how jitter and phase noise manifest themselves at each of these levels.

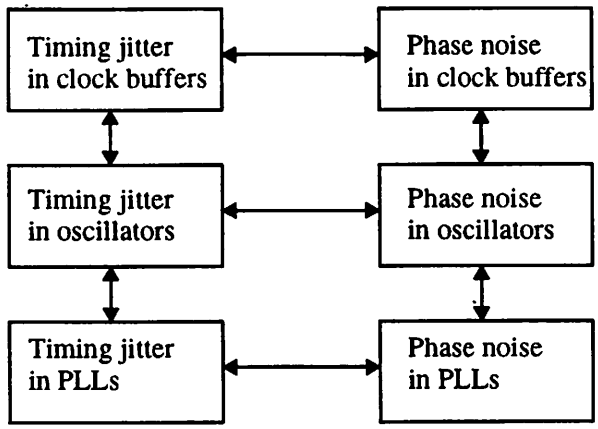


Figure 2.5 Timing jitter / Phase noise classification

This is depicted in figure 2.5. Our goal is a brief description of each of the areas in this figure and the linkages between them. This is a very big subject area. A detailed explanation of any of these is not possible here. What is provided is a brief survey, with the chance to establish naming conventions. The key relationships between the different representations and levels will be outlined. Some of these linkages are derived later in this dissertation, and will be summarized here as a preview. Others are part of the wide body of literature on PLLs and oscillators, and references will be given.

2.3.1 Phase Noise in Oscillators

As a starting point in the overview we will consider phase noise in oscillators.

The presence of random fluctuations in a signal manifests itself as phase noise in the frequency domain. A plot of an oscillator signal with phase noise is given in figure 2.6(a). Without phase noise, the entire power of the oscillator would be focused at the

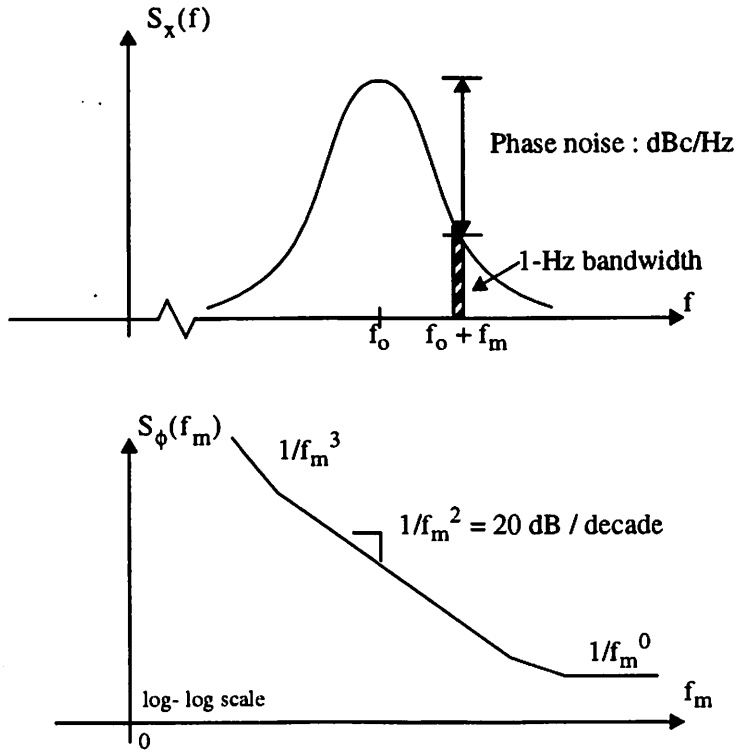


Figure 2.6 Oscillator phase noise : (a) power spectrum of oscillator (b) phase fluctuation power spectral density

frequency $f=f_0$[2]. However, the presence of phase noise spreads some of the power of the oscillator to neighboring frequencies, creating phase noise sidebands. In this plot, the sidebands are shown falling off as $1/f_m^2$ for frequencies far enough away from the carrier. This spectral shape is referred to as lorentzian, and is described in more detail in chapter 5. The frequency, f_m is the offset frequency from the center. Phase noise is usually specified in dBc/Hz at a given offset, where dBc refers to the level in dB relative to the carrier. Therefore, the phase noise of an oscillator at a given offset, is found from

2. For non-sinusoidal oscillators there is additional harmonic energy at multiples of the center frequency. For the spectrum in figure 2.6, however, only the energy in the vicinity of $f=f_0$ is shown.

the ratio of the power in a 1-hz bandwidth at the offset frequency, to the total power of the carrier. In figure 2.6(a) this would be the ratio of the area of the rectangle with 1-hz bandwidth at offset f_m, to the total area under the power spectrum curve. For reasonable resolution bandwidths, as described in [43], this is related to the difference in the heights of the spectrum at the center and at f_m, which is also indicated in the figure.

The spectrum in figure 2.6(a) is the power spectrum of an oscillator with a noisy phase angle. The spectrum of the phase fluctuations themselves can also be shown, as in figure 2.6(b). This is described in more detail, in later chapters. For an oscillator signal given by

$$X(t) = A\cos(2\pi f_o t + \theta(t)) \tag{12}$$

the spectrum in 2.6(a) is the power spectrum of X(t), and the spectrum in 2.6(b), is that of the noisy phase angle term, $\theta(t)$, and is called the spectral density of phase fluctuations. For offsets sufficiently far from carrier, the phase noise in dBc/Hz measured from the power spectrum in figure 2.6(a) is equal to the value of the spectral density of phase fluctuations in figure 2.6(b).

The spectrum in 2.6(b) is shown on a log-log scale, with phase noise sidebands that fall as $1/f_m^2$, or 20dB/decade. In practice, as described in [43] and [44], there are regions in the sidebands where the phase can fall as $1/f^3$, $1/f^2$, and even $1/f^0$ depending on the noise process involved. The $1/f^2$ region is referred to as the "white frequency" variation region, since it is due to white, or uncorrelated, fluctuations in the period of the oscillator. The behavior in this region is dominated by the thermal noise in the devices of the oscillator circuit. For low enough offset frequencies the flicker noise of devices generally comes into play and the spectrum in this region falls as $1/f^3$.

Also worth noting, the sidebands in 2.6(b) grow towards infinity as the offset frequency approaches zero. This is consistent with the behavior expected for timing jitter in free-running oscillators, and will be described shortly.

2.3.2 Timing Jitter in Oscillators

The random fluctuations of phase that are responsible for phase noise, can also be observed in the time domain as timing jitter. The cycle-to-cycle jitter of an oscillator is defined as the r.m.s. variation in its output period. For an oscillator with a nominal period of T_0, random fluctuations in the phase cause a timing error Δt_{vco} to accompany each period of oscillation. For white noise disturbances, the timing error is gaussian with mean zero, and a variance that we will denote by $\overline{\Delta t_{vco}}^2$. In this case the timing

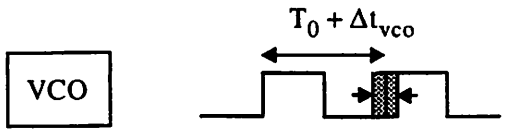


Figure 2.7 Cycle-to-cycle timing jitter

error between one cycle of oscillation and the next is uncorrelated. This behavior is consistent with the $1/f^2$, or white frequency noise, region of the phase noise sidebands. For other noise spectral shapes, such as $1/f^3$, jitter may be correlated from cycle to cycle, and distributions other than gaussian may result. In chapter 5 of this dissertation, a link will be made between timing jitter and phase noise, where it will be shown that the height of the phase noise sidebands due to thermal noise in devices is proportional to the normalized timing jitter variance.

$$S_\phi(f) = \frac{f_0}{f^2}\left(\frac{\Delta t_{vco\text{-}rms}}{T_0}\right)^2 \tag{13}$$

The effects of 1/f noise, and other noise processes which have left their signature on the phase noise sidebands of a signal, can be linked back to timing jitter through a more general relationship in [43].

$$\overline{\Delta t_{tot}}^2(t) = \int_{1/t}^{\infty} S_\phi(f)df \tag{14}$$

The jitter variance $\overline{\Delta t_{tot}}^2(t)$ is different than the cycle-to-cycle jitter. It is the total error variance with respect to an ideal time base, as illustrated in figure 2.8. This

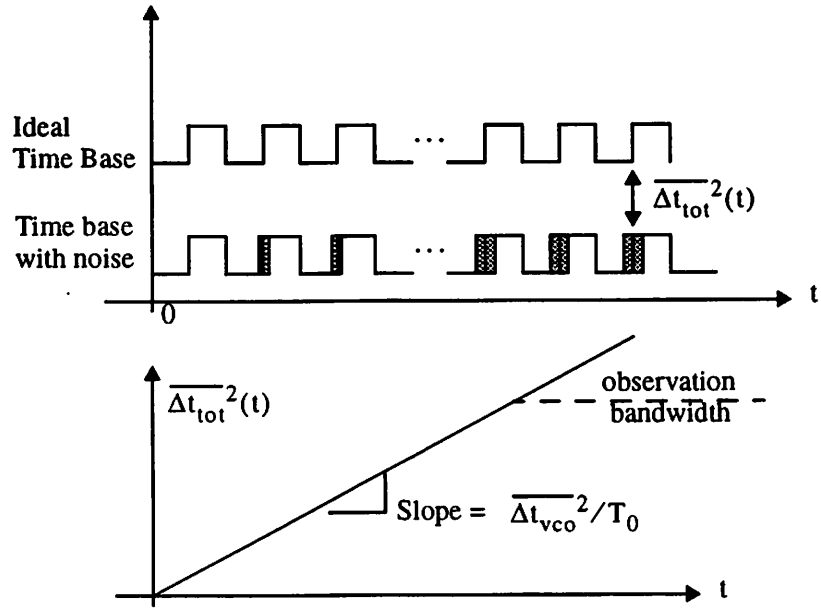


Figure 2.8 Oscillator timing jitter variance versus time

term represents the accumulated timing error from time zero to time t. In an oscillator, a perturbation in the phase during one period of oscillation changes the starting point of the next. For independent, gaussian errors the jitter variance of the timing error for each cycle of oscillation adds and the total error variance grows linearly. The phase in such a system exhibits the phenomenon of random walk. The total timing error variance tends towards infinity for long enough time, but practical observation bandwidths will always limit the value to a finite number.

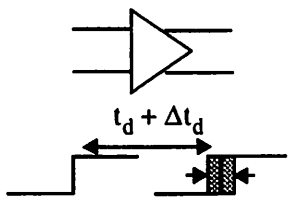
For "white frequency" variations, with $1/f^2$ phase noise sidebands, the integral in (14) predicts the linear ramp in figure 2.8. For regions with other spectral shape, the total jitter variance will exhibit a different shape. For many applications the region of the phase noise spectrum effected by 1/f noise in devices is not as important as one may first think. As will be seen shortly, when configured in a PLL, the effects of 1/f noise in

a VCO are reduced by the action of the loop which tries to correct for errors in the VCO within its loop bandwidth.

2.3.3 Phase Noise and Timing Jitter in Buffers and Delay Cells

Before extending the phase noise and timing jitter considerations for oscillators to the realm of PLL's which employ them, a step back will be taken to consider buffers and delay cells. The timing jitter or phase noise of a buffer is important, in its own right, for understanding the performance of systems that employ them. In addition, the timing jitter of delay cells is an important starting point for a number of systems. For applications which use a delay-locked-loop, or similar architectures, rather than a PLL, the jitter in chains of delay cells which are not configured as a ring-oscillator, is an important parameter. And in the analysis of systems which use ring-oscillators, the cycle-to-cycle jitter of the VCO is related to the jitter of the individual delay cells, themselves.

A detailed analysis of timing jitter in CMOS inverter delay cells is given in chapter 4, where delay cell jitter is related to circuit design parameters. An individual delay cell contributes a delay t_d and a timing error Δt_d to transitions which pass through it. The timing error is usually zero mean, and gaussian, with variance of $\overline{\Delta t_d}^2$. A useful



$\overline{\Delta t_d}^2$ Single-stage jitter variance

$\frac{\Delta t_{d\text{-rms}}}{t_d}$ Single-stage figure of merit

Figure 2.9 Individual delay cell timing jitter

figure of merit for delay cells is shown in chapter 4, called the normalized timing jitter. This expression is defined as the ratio of the r.m.s. timing jitter per stage to the nominal time delay per stage.

The phase noise of an individual delay stage of a buffer is different than for an oscillator. This topic will be covered in more detail in chapter 5. In an oscillator the jitter accompanying a cycle of oscillation changed the starting point of the next. It was the "integration" of these phase errors over time that gave the phase noise sidebands their shape. Independent gaussian errors, for example, led to the $1/f^2$ noise sidebands referred to as "white frequency" variations. Each cycle's timing jitter error perturbed the instantaneous frequency of that cycle of oscillation. Hence, independent, "white" timing errors lead to "white frequency" variations.

In a buffer, on the other hand, the independent timing errors which accompany each cycle perturb the output phase, but do not change the period of the time-base which produces the next cycle of oscillation. In this sense, they produce "white phase noise". This is illustrated in figure 2.10. The height of the phase noise floor in such a

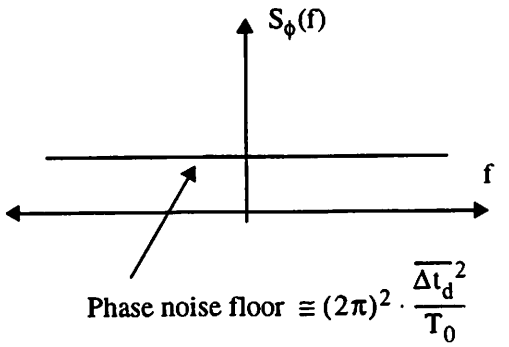


Figure 2.10 Buffer phase noise spectrum

case is proportional to the jitter variance of the delay stage, as derived in chapter 5. This figure shows the power spectrum of the phase fluctuations, $S_\phi(f)$. The power spectrum of a signal passed through such a buffer, $S_x(f)$, with a reasonably low noise floor, is approximately the same as the input spectrum with a white phase noise floor added.

2.3.4 Phase Noise in Phase-Locked Loops

The next level in this overview of timing jitter and phase noise, is the phase-locked-loop level. When configured in a PLL, the phase noise of a VCO is changed by the action of the loop. In addition, the reference input to the PLL has its own phase noise spectrum and the output phase noise depends on this contribution as well.

The basic operation of a PLL was described in section 2.2. A block diagram and small-signal model for a basic PLL is repeated in figure 2.11. In this figure an addi-

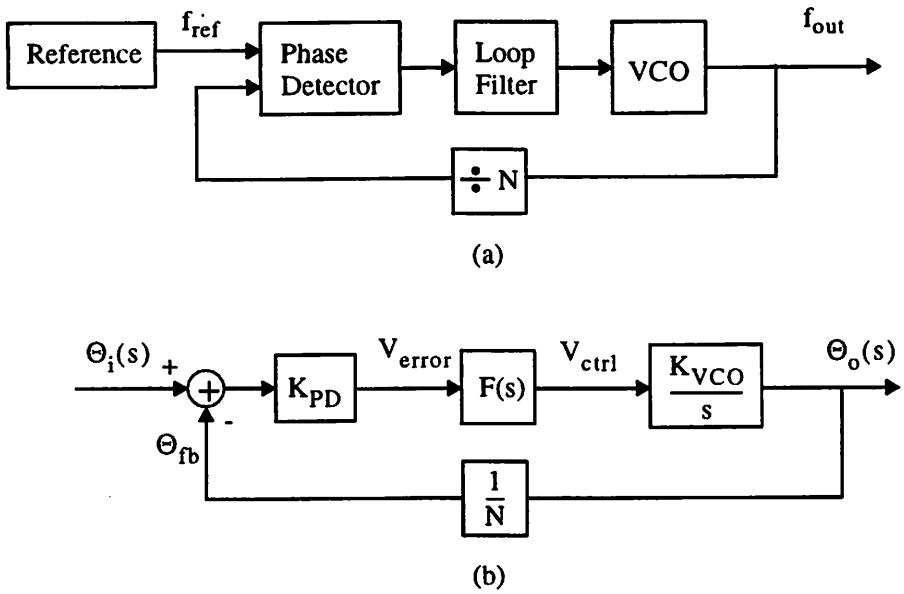


Figure 2.11 Basic phase-locked-loop: (a) block diagram (b) small-signal, AC, model

tional block called a divider has been added in the feedback loop. Dividers are frequently used in frequency synthesizer PLLs. With a divide-by-N in the feedback path, the output frequency is equal to N times the reference frequency. For applications without a divider, N is effectively one.

The total output phase noise for a PLL can be expressed in terms of the phase noise of the reference and of the VCO according to equation (15).

$$S_{out}(\omega) = S_{ref}(\omega) \cdot N^2 \cdot |H_1(\omega)|^2 + S_{vco}(\omega) \cdot |H_2(\omega)|^2 \qquad (15)$$

This result is described in [37]. Since the VCO is in the forward path of a feedback loop, the loop corrects for its errors, but only for frequencies within the bandwidth of the PLL. The transfer function $H_2(\omega)$ can be shown to be a high-pass filter. Low frequency phase noise is rejected by the loop, but high frequency phase noise passes directly to the output. The transfer function from the input of the PLL to the output, $H_1(\omega)$, however, has a low-pass characteristic. The PLL rejects high frequency phase noise in the reference but allows low frequency errors to pass. The filter corner frequency for both H_1 and H_2 depend on the bandwidth of the PLL. Therefore the choice of PLL bandwidth involves a direct trade-off between the noise of the VCO and the reference.

When considering applications with a frequency divider, the reference phase noise is boosted by an additional factor of N^2, when referred to the output. For a divide ratio of N=10, this would be 20dB. However, we will see later that phase noise is usually inherently smaller for lower frequency oscillators. Therefore, even with the factor of N^2, the reference phase noise may be lower. In fact, in applications such as frequency or clock synthesis the reference is usually derived from a crystal-oscillator circuit having very low phase noise, often lower than the VCO. In that case, the phase noise spectrum for the output of the PLL is as shown in figure 2.12(a). Here, the phase noise of the output follows the higher, VCO phase noise sideband for frequencies outside the bandwidth of the PLL and follows the lower, reference frequency sideband inside the bandwidth of the loop. In figure 2.12(b) an example is given in which the VCO is much noisier than the reference. Ideally, the VCO phase noise would be rejected completely within the bandwidth of the loop. But in practice, the loop filter skirts, falling as $1/\omega^2$, just cancel the phase noise which is rising with the same slope, leaving a flat spectrum within the bandwidth of the PLL. In this case, a higher PLL loop bandwidth will result in a lower phase noise for a given offset frequency within the bandwidth of the loop, as pictured in figure 2.12(c).

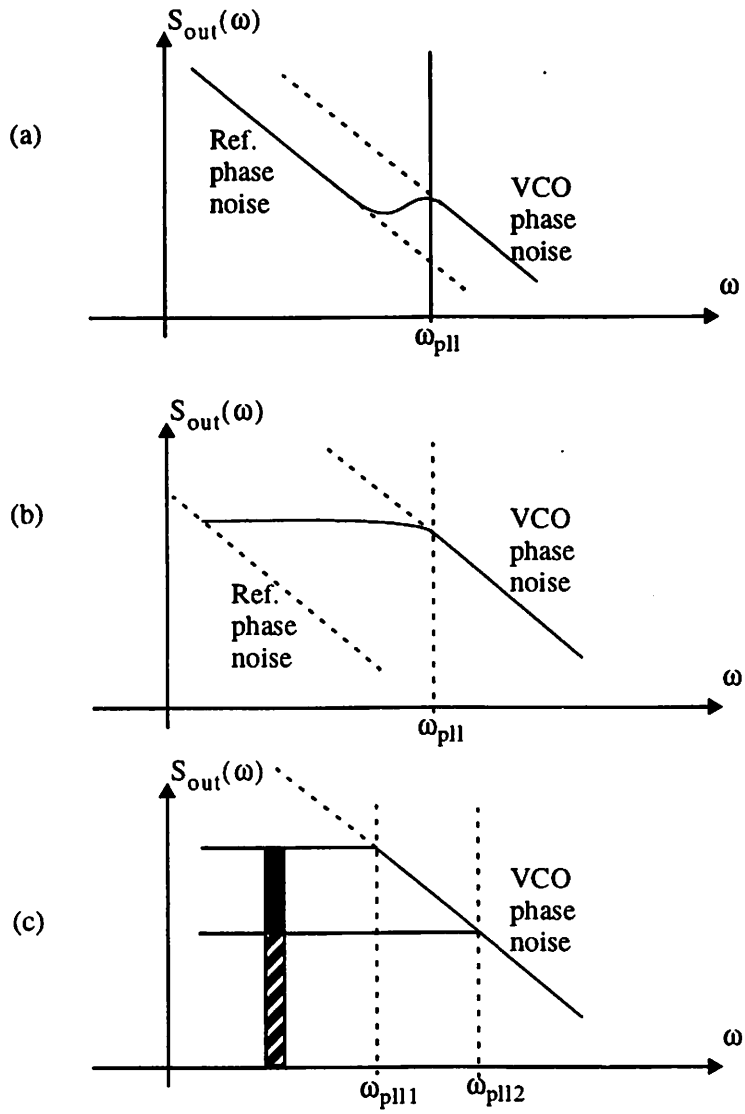


Figure 2.12 PLL output phase noise spectrum: (a) nominal case: low reference phase noise, moderate VCO phase noise (b) extreme case: very low ref. phase noise, high VCO phase noise (c) extreme case with different PLL loop bandwidths

2.3.5 Timing Jitter in Phase-Locked Loops

The final segment of this overview involves timing jitter in phase-locked loops. This topic is described in a references [21], [33, 34, 35] and [36]. As in the case of phase noise, the output jitter depends on the jitter of the VCO, the jitter of the PLL input source, and the bandwidth of the loop. For clock and data recovery applications the jitter of the input signal, which is derived from transitions in the data is often the

primary source of error. In that case a low PLL bandwidth is desired. In applications such as clock synthesis, however, the PLL output jitter is often dominated by the jitter of the VCO. In these cases, a higher loop bandwidth helps to reduce the total PLL output jitter.

To understand timing jitter in PLLs we return to the accumulated output jitter of a VCO described in section 2.3.2. In figure 2.8, it was shown that the total output jitter for a free-running VCO grows over time as the variance of the phase error from each cycle of oscillation adds. The jitter as a function of time, t, was also said to be related to the integral of the sideband energy, from high frequencies, down to the frequency of 1/t, as shown in equation (14). For a VCO configured in a phase-locked-loop, however, the total output jitter looks more like that shown in figure 2.13. Recall that the total jit-

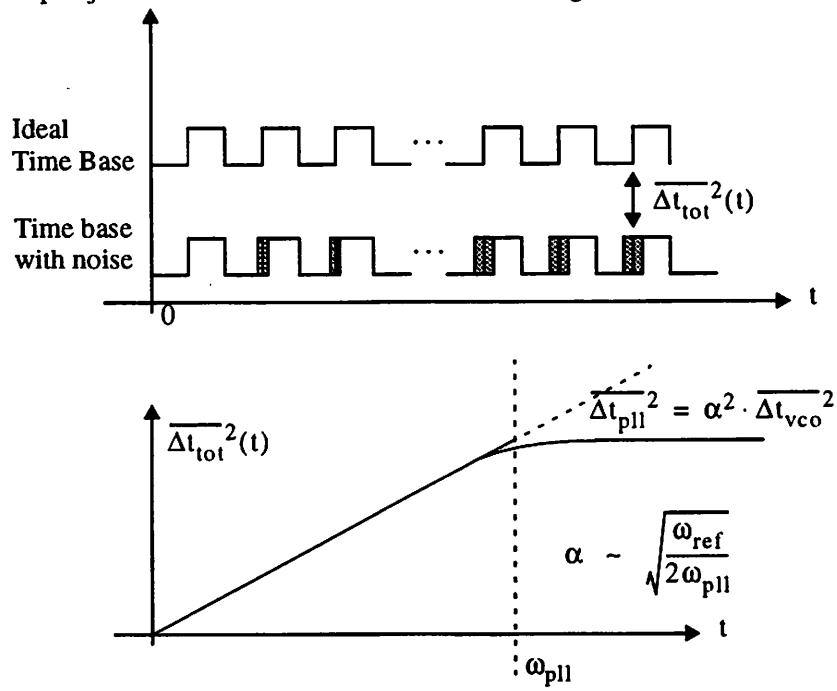


Figure 2.13 PLL output jitter

ter at a given time, t_1, represents the accumulated jitter from the time t=0 until t=t_1. For small time differences, t, the jitter accumulates in the same way as the free running VCO case. For larger time differences, on the order of the reciprocal of the PLL loop

bandwidth, the total jitter variance reaches an equilibrium value. This can be explained from two different points of view.

In [33] the response of a PLL to an isolated timing error is described. For a free-running VCO an isolated time error in the VCO would effect the time-base of the oscillator from that point on. In a PLL, the loop acts to correct for the resulting phase error, and the timing error will be reduced towards zero over time, with a settling time inversely proportional to the bandwidth of the loop. For a first order loop this would be a simple decaying exponential. A higher PLL bandwidth results in a quicker decay towards zero.

The net jitter variance at the output of the PLL is the sum of all past error events weighted by the response of the system. Therefore, for time delays greater than the reciprocal of the loop bandwidth, the output variance reaches a steady state value since for each new error event added, another past event's contribution has been correspondingly reduced. The equilibrium value of the PLL output jitter, as shown in figure 2.13, will improve with a higher loop bandwidth. In [33], the total PLL output jitter is shown to reach a final value of

$$\overline{\Delta t_{pll}}^2 = \alpha^2 \cdot \overline{\Delta t_{vco}}^2 \tag{16}$$

where $\alpha \cong \sqrt{\omega_{ref}/2\omega_{pll}}$. For typical loop bandwidths α^2 is on the order of 10-100. Therefore the total output jitter for a PLL is just a multiple of the cycle-to-cycle jitter of its VCO.

Another interpretation of the graph in figure 2.13 can be found by relating the output jitter, $\overline{\Delta t_{tot}}^2(t)$, to the integral of the PLL output spectrum sidebands using equation (15). Since the VCO phase noise is rejected within the bandwidth of the PLL, the jitter variance at the output is expected to flatten as well.

2.3.6 Timing Jitter / Phase Noise Summary

This section has provided an overview of phase noise and timing jitter at three levels of implementation - the buffer / delay cell level, the oscillator level, and the PLL level. The key relationships between each of these levels of consideration have been described, as well as links between the timing jitter and phase noise domains. These conclusions are summarized in figure 2.14 (two pages) where the main results of each subsection are combined into one large map of the subject matter. This figure appears on the next two pages.

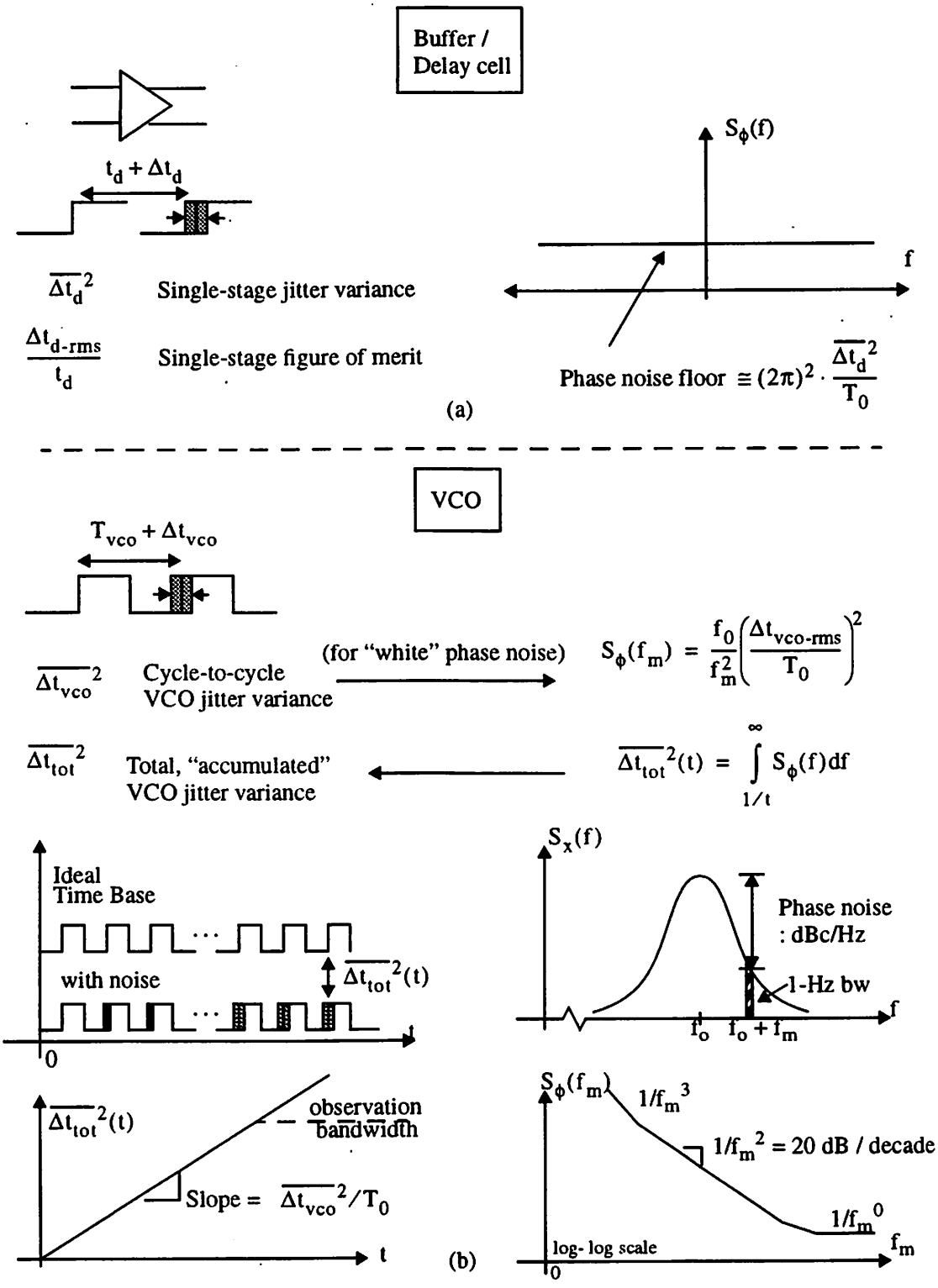
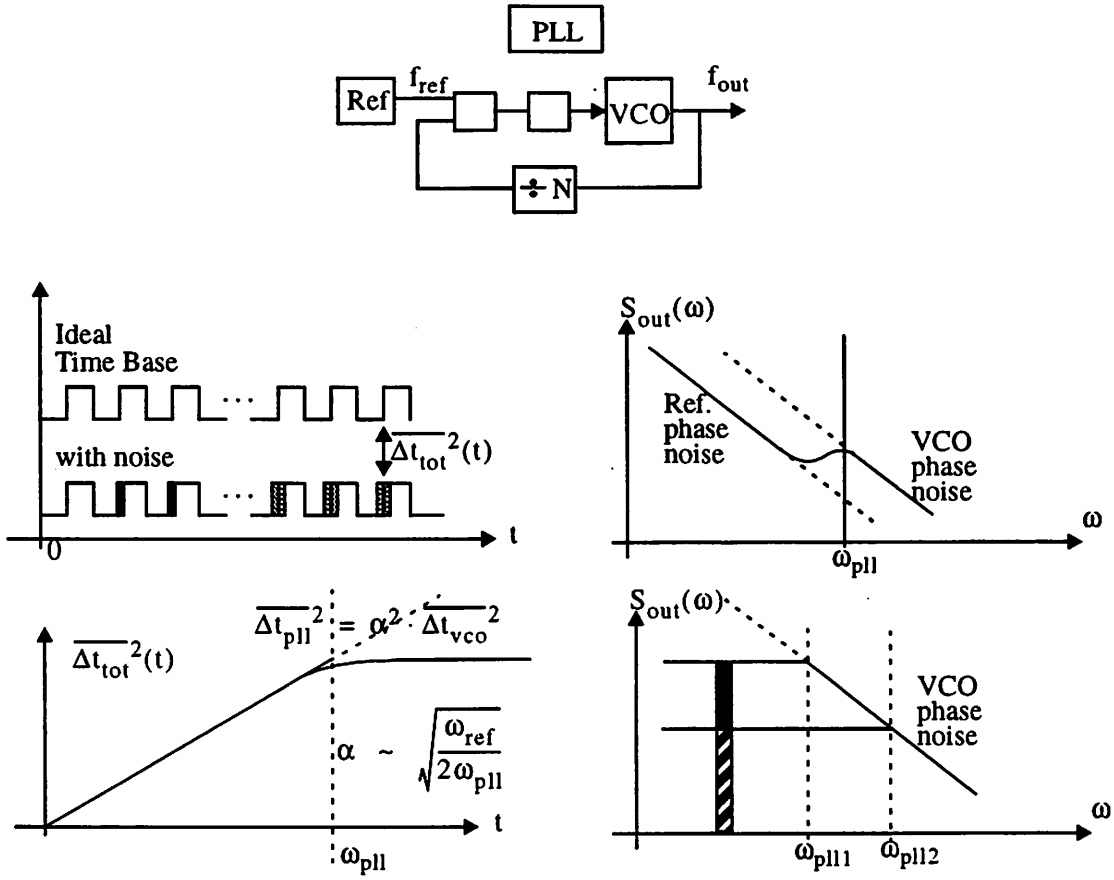


Figure 2.14 Summary of timing jitter and phase noise relationship in: (a) buffer / delay cells, (b) Oscillators, (c) PLLs (next page)



$$S_{out}(\omega) = S_{ref}(\omega) \cdot N^2 \cdot |H_1(\omega)|^2 + S_{vco}(\omega) \cdot |H_2(\omega)|^2$$

(c)

Figure 2.14 (cont.) Summary of timing jitter and phase noise relationships in: (c) PLLs

2.4 System Impact of Timing Errors: Sample Applications

In this section the effects of timing jitter, phase noise, and other timing errors on the performance of some key sample applications will be described. This chapter began with an overview of the various roles that clock and oscillator signals perform in communication systems as well as the different ways in which they are generated. Timing errors and their impact on system performance were also described, but at a superficial level. In this section a more detailed look will be taken at two particular applications; clock synchronization in high bandwidth digital I/O systems, and clock buffering in A/

D converters. The impacts of timing jitter, the phenomena that was explored in the preceding section, and other timing error sources will be considered. In these systems timing jitter can be quite important, though not necessarily the limiting factor for overall performance. In the next chapter an even more detailed look at another application, RF frequency synthesis, will be provided. In frequency synthesizer design, the phase noise or timing jitter of the VCO is often the limiting factor.

2.4.1 Clock Synchronization in High Bandwidth Digital I/O Interfaces

In complex digital systems, such as microprocessors or DSP processors, a large internal clock buffer and distribution network are needed to drive the various parts of the system [3,4,5]. In high bandwidth digital I/O interfaces, such as those found in some DRAM circuits [1,2] an internal clock buffer is also needed to drive the input and output registers. The clock buffers in both of these applications can result in timing skew between the input data and clock signals. For this reason a phase-locked or delay-locked loop is often used to create a buffered clock signal that is phase aligned with the data. Typical block diagrams for both a PLL and DLL implementation are illustrated in figure 2.15.

The maximum speed at which the system can be clocked is given by:

$$f_{max} \leq \frac{1}{T_{min}} \cong \frac{1}{t_{sh} + \Delta t_{error}} \tag{17}$$

where t_{sh} is the setup and hold time of the input register, or sampling circuit. The timing error is comprised of both random and systematic components. The error at any given time is the sum of all of the various error sources. Without the use of a synchronizing PLL or DLL circuit, as shown in figure 2.15, the timing error would typically be limited by the skew between the data and clock introduced by the clock buffer. With this delay tuned out by the on-chip PLL, however, other systematic and random timing errors in the system limit the maximum data rate (the setup/hold time of the input regis-

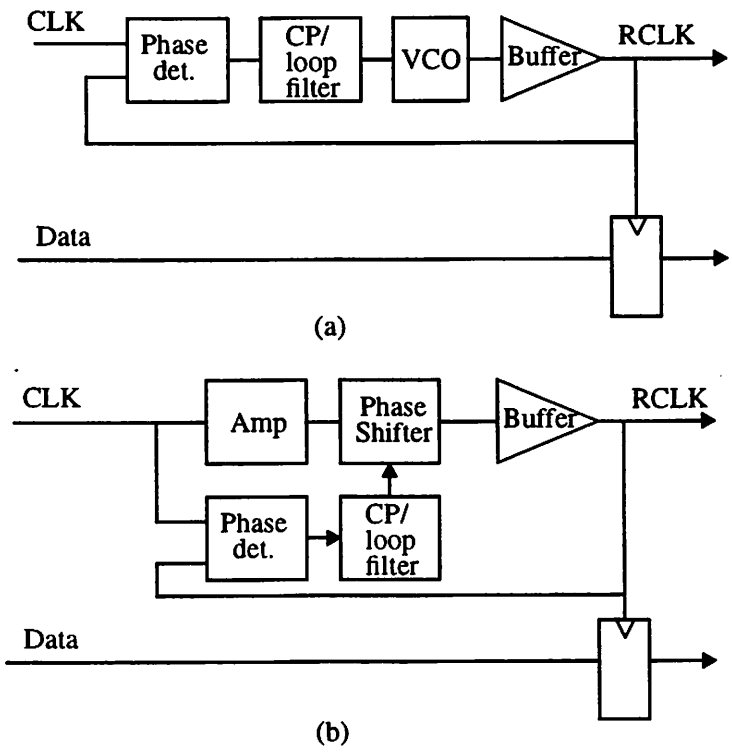


Figure 2.15 Clock synthesis / synchronization circuits: (a) PLL-based, (b) DLL-based

ter can be made quite small).

Timing skew due to phase offsets in the system are one concern. Path differences between the buffered clock signal fed to the phase detector and that used by the input registers need to be carefully controlled. In addition, some PLL and DLL implementations have a static phase error in their steady state operation. This phase error, between the buffered clock and received transmit clock, may be required to generate the control voltage needed for the correct VCO output frequency. This source of error should be minimized through proper design.

Timing jitter at the PLL output due thermal noise in the VCO is also a concern. The analysis in the last section suggests that the total PLL output jitter depends on the jitter of the VCO and the bandwidth of the PLL. A higher bandwidth PLL can result in less jitter in the internal clock. In applications where the internal clock frequency is the same as the external reference, a delay-locked-loop circuit can often be used in place of

a PLL. A DLL employs a voltage-controlled delay chain or delay element which does not recirculate noise from one clock period to the next like an oscillator does, resulting in significantly lower output jitter [1,33].

The main source of timing error in high bandwidth digital interfaces, however, is usually not thermal noise-induced timing jitter, but errors induced through the power supply. These can come in two forms. Signals from elsewhere on the chip (such as other clock frequencies) may couple to the VCO or delay element through the power supplies. This can result in modulation of the phase of the output. If the rejection of interfering signals is not sufficient, the AC variation in the output phase can easily exceed the r.m.s. timing jitter due to thermal noise.

In addition to an AC modulating signal, an abrupt change in supply voltage, or step, can also result for a variety of reasons. In this case the frequency of the VCO changes abruptly and may require several cycles to recover. This frequency error can integrate into a large phase error over time. Higher bandwidth PLLs will recover more quickly and result in a lower peak phase error. However, as will be described in the next chapter, a higher loop bandwidth may make the PLL more susceptible to reference feed-through - another source of modulation. As in the case of timing jitter, a DLL has the possibility of significantly lower peak phase error. This is discussed in more detail in the DRAM interface described in [1]. The interface in this case was operated at 250 MHz, and achieved a data rate of 500 MB/s (per pin). The peak-to-peak timing jitter on the internal sampling clock was 140ps with no activity in the core. The timing error in the output data showed a 80ps skew and a 250ps peak-to-peak jitter with activity in the DRAM core.

2.4.2 Clock Drivers for A/D Conversion

Timing jitter in the clocks used to drive sampling circuits in an A/D converter can have an adverse effect on a converter's dynamic range. This is especially important for higher resolution converters as their maximum operating frequency is extended. At

higher frequencies the effects of timing jitter become more pronounced and in some systems can be a limiting factor in the resolution [6, 7, 27].

The simplest picture of the effect of timing jitter in an A/D converter is given in figure 2.16. If the input to the converter is assumed to be a simple sinusoid with frequency f_o

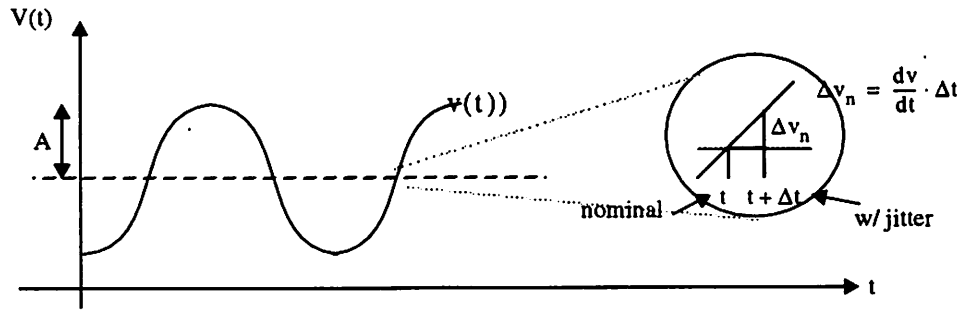


Figure 2.16 Timing error due to sampling with jittery clock

and amplitude A, then the maximum rate of change of the output voltage (found from the derivative of v(t)) is given by

$$\left(\frac{dv}{dt}\right)_{max} = 2\pi f_0 A \tag{18}$$

As depicted in figure 2.16, for small timing errors an offset in the sampling time of size Δt will result in a voltage shift of magnitude Δv which is related to the timing error through the slope of the line, or slew rate, at the nominal sampling point.

$$\Delta v \cong \left(\frac{dv}{dt}\right) \cdot \Delta t \tag{19}$$

Therefore, if the waveform is sampled at the point of maximum slope, a voltage error of

$$\Delta v = 2\pi f_0 A \cdot \Delta t \tag{20}$$

will result. One design strategy (albeit somewhat simplified) might be to insure that the maximum voltage error for an r.m.s. timing error (one standard deviation away from the mean of zero) is less than the voltage associated with the least significant bit (LSB) of

the A/D converter. In this case the resolution of a converter with an applied signal with amplitude of one-half the full-scale voltage can be shown to be limited to

$$B \leq \log_2\left[\frac{1}{2\pi f_0 \Delta t_{rms}}\right] \tag{21}$$

where B is the number of bits of resolution, f_0 is the maximum frequency of the converter and Δt_{rms} is the r.m.s. timing error associated with the clocking source. The reciprocal of the timing error ($1/\Delta t_{rms}$) is assumed to be greater than f_0, so that the argument to the log function is always greater than 1. This means that for a desired resolution, accommodating a higher nyquist frequency for the converter requires lower r.m.s. timing jitter. For a factor of two increase in the nyquist frequency a factor of two improvement is required in the r.m.s. timing jitter. The normalized timing jitter ($\Delta t_{rms}/T_0$) of the clock source remains constant.

The above model is a somewhat simplistic view of the effect of sampling jitter on the performance of a converter. In most systems what really matters is the impact of timing jitter on the dynamic range of the converter. This is usually measured in the frequency domain at the output of the A/D converter under certain test conditions. With a sufficiently active input signal the quantization noise of an A/D converter results in a white noise floor at the output of the converter with a spectral density of

$$S_n(f) = \Delta^2/12 \cdot f_s \tag{22}$$

where Δ is the size of 1 LSB for the converter [47]. If the sampling phase of the signal is sufficiently random with respect to the input signal then a similar noise floor could be expected from timing jitter. The height of the noise floor would depend on the r.m.s. timing jitter as well as an "average" rate of change for the output signal, instead of just the point of maximum slope. Finding an input signal so that these conditions are met is more complicated than for the quantization noise floor measurement however. If the sampling signal and test signal have a synchronous relationship then the noise floor

height may not be the same. If the test signal were close to synchronous, but not quite aligned with the sampling frequency, there may be a modulation in the noise floor related to the beat frequency between the two. In general, the impact of timing jitter depends on the details of the system which employs the A/D converter [48,49].

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Chapter 3

RF Frequency Synthesizer Design

3.0 Introduction

In the previous chapter a very broad look was taken at classes of systems in which timing signals play an important role in system behavior. Aspects of timing signal behavior were looked at as well as types of timing errors. In this chapter a closer look is taken at one particular class of systems, RF frequency synthesizers, with an emphasis on their application to RF transceivers for wireless communications. The importance of phase noise and spurious tones in the oscillator signals used in such transceivers is discussed, and design trade-offs for PLL based frequency synthesizers are described. The chapter begins with an introduction to RF receivers for wireless communications systems and the effect of phase noise and spurious tones on overall system performance. Next, the design of frequency synthesizer PLL's and their components is considered.

3.1 RF Transceivers for Wireless Communications

Frequency synthesizers are used to generate the local oscillator signals (LOs)

used in radio transceivers to translate signals to different frequency bands for transmission and/or reception. Phase noise and spurious tones in local oscillators can degrade the "selectivity" of a radio transceiver- its ability to separate neighboring, interfering channels from a particular channel of interest.

The two key performance factors for a radio systems are sensitivity and selectivity. Both of these can be thought of from the transmit or receive perspective as well as from the perspective of a mobile user (i.e. cellular communications) or base station. The sensitivity of a receiver is a measure of the smallest RF signal that can be received at the input and still result in a recovered output of a given signal to noise ratio, or bit error rate (BER) for the case of a digital communications system. The ability to recover the incoming RF signal over a wide dynamic range, from low power levels to high, is important in radio receivers. One reason is that the smallest recoverable signal determines the maximum range of a transmission link, for a given transmit power level. Another reason is the fact that the frequency response of the transmission channel separating the transmitter from the receiver often has a widely varied response with deep notches that can result in very large signal attenuation, even for small physical distances of separation [50], [51]. In mobile applications this response can even vary rapidly with time.

The sensitivity of a radio receiver is ultimately limited by the noise introduced by the components, both passive and active that make up the system. A key performance specification for the system and its individual components is the noise figure (NF), which is the ratio of the signal to noise ratio at the input to that at the output (always greater than 1, or positive when expressed in dB) [50], [52].

The other important factor for a receiver (or transmitter) is selectivity, or the ability to receive one particular channel in the presence of neighboring interferers. This is significant for several reasons, one of which was alluded to in the discussion on sensitivity. The notches in the frequency response of the transmission channel can be very narrow, causing received power levels to vary widely, even for adjacent channels. Fur-

thermore, the transmitter of the desired signal may be very distant, physically, while the interferer is in close proximity. This problem, called the "near-far" problem, means that there are always some scenarios which result in much stronger signals in adjacent channels or even other channel bands [50],[51]. Therefore it is important that the receiver have high selectivity in order to insure reliable reception. This is illustrated in figure

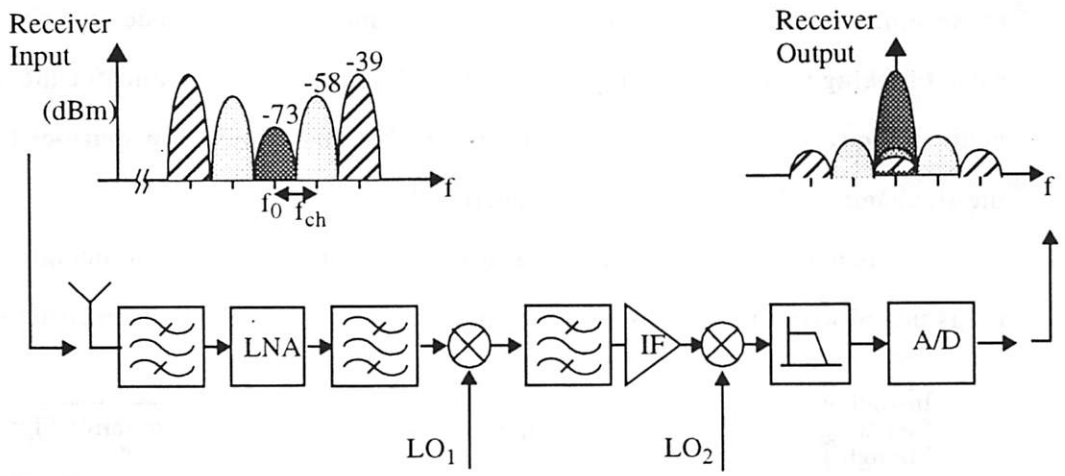


Figure 3.1 Conventional super-heterodyne receiver

3.1. In this example the desired incoming signal is at the frequency f_o, and is being received at a power level of -73dBm. Neighboring signals one channel away (at f_o +/- f_{ch}) are being received at -58dBm, and neighboring signals two channels away at -39 dBm. The receiver in this example translates the desired channel to an intermediate frequency (IF) and then baseband, through selection of appropriate local oscillator frequencies, and filters away out-of-band as well as neighboring channels along the way. In the process, however, any non-linearities in the transfer function of components in the receive path (mixers, LNA, etc.) can cause distortion, which will result in mixing of some of the energy in adjacent channels on top of the desired signal. If the signals involved in the distortion products are too strong, the resulting interference may swamp out the desired signal. Ample intermodulation specifications are required for these components to insure that receiver selectivity goals are met under worst case input signal

scenarios. These scenarios are usually specified in great detail for different radio standards and are often referred to as blocking requirements.

3.1.1 System Level Impact of Phase Noise and Spurious Tones

Phase noise and spurious tones in the local oscillators in an RF receiver can also cause some of the energy in adjacent channels to mix on top of the desired channel. The same blocking requirements that influence the linearity specifications for the components in the receiver also determine the acceptable phase noise and spurious levels in the sidebands of the local oscillator spectrum[1].

This phenomenon is illustrated in figure 3.2. In this figure an incoming RF signal is mixed with the local oscillator to produce a copy of the input spectrum shifted to

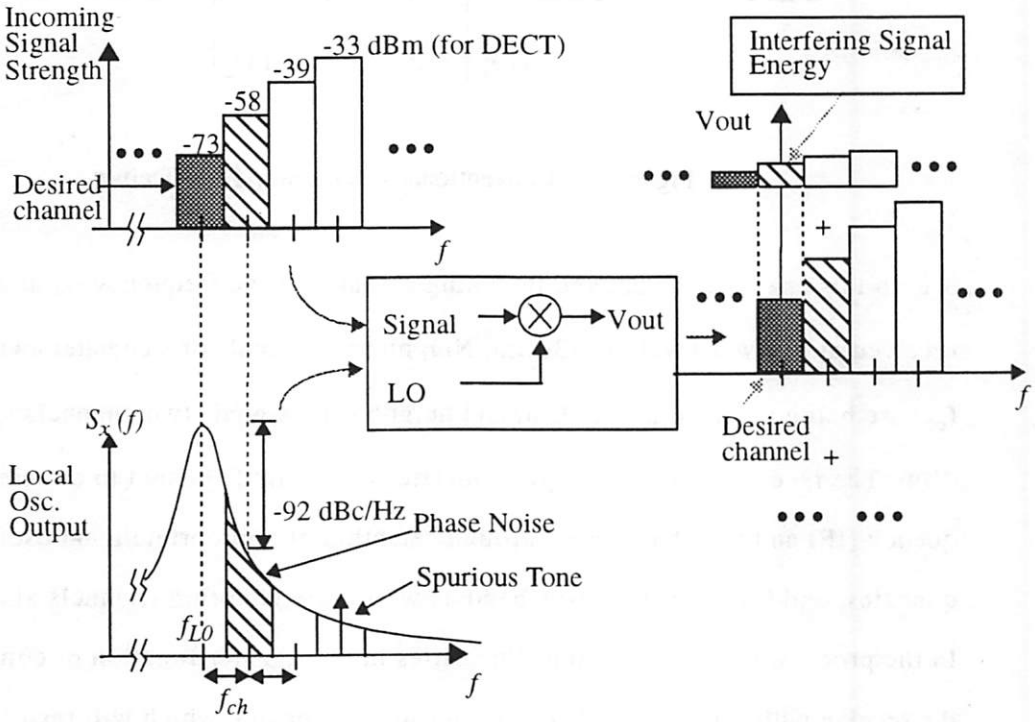


Figure 3.2 Local oscillator phase noise example (incoming signal strength profile for DECT cordless telephone standard).

1. In practice, phase noise blocking specifications are usually generated from the performance expectations for reasonable oscillator designs. This data along with the characterization of the transmission channel help determine the ultimate capacity of the radio system.

a lower frequency (either IF or baseband depending on the receiver architecture and the particular LO being considered)[2]. The incoming signal spectrum in this example consists of a small desired signal at a power level of -73 dBm and three neighboring signals with power levels of -58, -39, and -33 dBm respectively. If the local oscillator spectrum where perfectly sharp, with all of its power centered at f_{LO}, then the output of the mixing operation would just be a shifted copy of the input spectrum. However, in practice the power of the local oscillator is spread in part to adjacent frequencies due to the effects of phase noise. And, as will be described later, modulation of the signal that controls the center frequency of the LO can result in sideband energy in the form of spurious tones. This is also depicted in figure 3.2. The energy in the sidebands of the local oscillator spectrum also mixes with the incoming signal spectrum, producing unwanted and shifted copies of the incoming spectrum. For example, the energy at one channel away from the LO center frequency mixes with the -58dBm signal to produce an unwanted interference signal that winds up on top of the desired channel.

In order to meet receiver blocking requirements the LO phase noise and spurious tone levels need to be low enough that any interfering signal is small compared to the desired. How small depends on the signal-to-noise or signal-to-interferer levels required at the end of the receive chain. Typical requirements for a system are 15 to 20dB [50], [52], [53]. For a spurious tone, the height of the tone needs to be below that of the carrier by an amount equal to the worst case difference in signal power levels plus the minimum signal-to-interferer ratio required at the end of the receive chain. For the example in figure 3.2, with a signal-to-interferer requirement of 15 dB this means the spurious tone at $f_{LO}+3f_{ch}$ must be at a level of -55dBc or lower. That is -55 dB relative to the power of the carrier. This insures that with the worst case power difference of 40 dBm between the desired signal and the interferer, the power of the interferer mixed

2. In a conventional super-heterodyne receiver there are two local oscillators. The first can be tuned in increments of the channel frequency spacing and is used to mix the desired signal down to a predetermined intermediate frequency (IF). At IF, the signal is passed through a sharp bandpass filter which rejects adjacent channels. Then the signal is mixed again with a second local oscillator for translation to baseband.

on top of the desired signal will still be 15 dB down.

The requirements for phase noise are similar to those for spurious tones except for the fact that phase noise is not coherent but has its power spread over a range of frequencies. To find the total power in a given neighboring channel band, the power spectral density of the oscillator is integrated over that channel's bandwidth. For most sidebands a reasonable approximation to this is just the power spectral density at the center of the channel, in dBc/Hz, times the channel bandwidth in Hz[3]. This power level when mixed with the power of the neighboring channel signal must fall below the receiver's signal-to-noise/interferer requirements. This criterion is somewhat ill-defined since the result of mixing phase noise with a neighboring channel is not the same as mixing with a pure tone. However an experienced receiver system designer knows how to properly specify the acceptable phase noise level, and resulting interferer for adequate receiver performance.

To illustrate phase noise requirement calculations, consider the example in figure 3.2. If the signal to noise ratio requirement is 15 dB at the output of the receiver and the neighboring signal one channel away can be at a height of -58 dBm (worst case) compared to a desired channel of power -73dBm, then the total phase noise energy allowable in the neighboring channel band is -30dBc. That is -30dB relative to the power of the carrier; 15dBc for the SNR requirement and 15dBc to cover the difference in incoming power levels. For the DECT radio standard (the European cordless phone standard on which the numbers in figure 3.2 are modeled) the spacing between channels is 1.728 MHz. This translates to a net power spectral density of -92 dBc/Hz, as illustrated in equation (23).

$$P = -30\,\frac{dBc}{1.728MHz} = -30 - 10\log(1.728 \cdot 10^6)\,\frac{dBc}{Hz} = -92\frac{dBc}{Hz} \qquad (23)$$

In a heterodyne receiver, their are two local oscillators in use, and the phase

3. For reasonable channel bandwidths this is usually a good approximation. In this case the spectrum is approximated by a series of piecewise constant rectangular regions. With the height of the rectangle specified from the center of the channel the errors in the estimate on both sides tend to cancel.

noise blocking requirement is divided between them. The second LO is usually not as big of a problem, however since: (1) it is at a lower frequency which usually means inherently lower phase noise, and (2) channel select filtering at IF will reduce the power of the interfering signal before the second frequency translation step. In some alternative receiver architectures, however these facts may not be true. In a high integration RF receiver, for example, the second LO may be implemented with an on-chip VCO. Although lower phase noise (for a given offset) is possible at lower frequencies, the integrated VCO circuit may have higher phase noise due to its implementation. Another situation where the second LO's phase noise is important is in receivers which employ a broadband IF approach, saving channel selection filtering until after the second frequency translation step. This approach has potential in high integration portable receivers [54, 55] as well as in low-cost multi-channel base-station applications [56].

There are a few more points about receiver phase noise worth clarifying here. For one, receiver blocking requirements for worst case interferers are usually meant to be satisfied with only one interferer present at a time. That is to say the neighboring channel interferers at -58 dBm, -39dBm, etc. in figure 3.2 will not all be present at the same time. Also, the increasing power levels allowed for adjacent channel interferers is usually compensated for by falling noise sidebands in the local oscillator. The critical channel can be any of the adjacent channels, however, not necessarily the first[4].

For example, the DECT requirement for the phase noise one channel away was just determined to be -92dBc/Hz (assuming 15dB SNR requirement for the receiver). The phase noise requirement for the second adjacent channel, using the power profile in figure 3.2, is

$$P = -34 - 15 - 10\log(1.728 \cdot 10^6)\ \frac{dBc}{Hz} = -111\ \frac{dBc}{Hz} \tag{24}$$

4. In fact some systems, such as the GSM based PCS-1900 specification, relax the requirements on the neighboring channel or first few channels and target the spec at channels a little further away. The frequency re-use pattern employed by the cellular network can be designed to help reduce the likelihood of "near-far" interference problems for the most critical, adjacent frequencies.

However, the phase noise of the oscillator is usually inversely proportional to the square of the offset frequency (this was described in chapter 2)

$$S_{\phi}(f_m) \cong K \cdot \left(\frac{f_0}{f_m}\right)^2 \tag{25}$$

If the requirement in (24) is met by the oscillator at an offset of two channels away (3.456 MHz) from center, then the extrapolated phase noise at a 1.728 MHz offset is a factor of four higher, or 6dBc higher in power. This means the phase noise at one channel away is -105dBc/Hz, which is much lower than the -92dBc/Hz needed to meet the first channel's requirements. Therefore the ultimate phase noise requirements for an oscillator depends on careful consideration of the each of the interferers in figure 3.2. In this case, the blocking requirement for the second channel away limits the phase noise of the oscillator.

One final point of clarification is that the selectivity requirements of an RF transceiver are also important in signal transmission. An LO signal with significant phase noise will mix part of the signal being transmitted into neighboring channels as well, creating a problem for other receivers downstream in the radio system. Oscillator phase noise requirements can also be calculated for a radio standard based on the spectral crowding requirements for the transmitter.

3.1.2 Requirements for Different Synthesizer Applications

Different RF applications have varying degrees of sensitivity to phase noise. Cellular phones and cordless phones require low-phase noise for selectivity reasons. The local oscillator in a spectrum analyzer needs to be low to increase the dynamic range of the measurements it can make. These systems and the phase noise specifications they impose on oscillators are generally more demanding than other applications, even high frequency ones, where the oscillator is used as a timing source rather than a frequency source.

For example a clock synthesizer PLL for use in a microprocessor or DRAM I/O

interface may have a timing jitter requirement of around 3%. That is the net timing jitter at the output of the PLL can be 3 percent of the total clock period. Suppose the clock frequency were 1GHz and the PLL loop bandwidth was 250KHz. In that case the normalized cycle-to-cycle timing jitter requirement, using equation (16) from chapter 2, would be $0.95 \cdot 10^{-3}$. If this number is substituted in equation (13) from chapter 2, then the equivalent phase noise at a 1MHz offset from a 1GHz carrier would be -90dBc/Hz. For the local oscillator frequency used in a DECT cordless phone (a typical first LO is around 1.7GHz) this would correspond to a phase noise of -93dBc/Hz at 1.728MHz away from carrier. This is barely enough to meet the phase noise blocking requirements for the first neighboring channel and is 12 dBc/Hz higher than the equivalent requirement for the second channel (as was described previously). Furthermore, as will be shown shortly, the phase noise requirements for a DECT cordless phone are very easy to meet compared to those required for cellular telephony. The requirements for the GSM based, DCS-1800 specification in Europe require an equivalent phase noise (normalized to the same offset frequency) that is -28dBc/Hz better than DECT, or more. Requirements for spectrum analyzers are even tighter.

The main point of this discussion is that phase noise requirements are generally the most demanding in frequency synthesizer applications, especially those at RF. Other timing error sources, such as input jitter or power supply pulling, may limit the performance of clock recovery and clock synthesizer PLLs. But for RF applications, where selectivity is important, the basic phase noise sidebands, due to thermal noise in the devices which make up an oscillator, is often the key.

Within the various RF frequency synthesizer applications, however, there are a range of different performance levels that may be required by a system. This is illustrated in table 1, with examples of phase noise requirements for a DECT cordless phone receiver, a PCS-1900 cellular phone receiver, a PCS-1900 base-station, and the HP-71209, a typical RF spectrum analyzer. The numbers in this table are determined from the worst case interferer power profiles in the DECT and PCS-1900 radio standard doc-

Table 1: Local oscillator phase noise requirement comparison

Application	Center freq.	Channel bandwidth	Critical phase noise spec.	Equivalent normalized phase noise (1.7GHz, 100kHz offset)
DECT cordless phone receiver	~1.7 G	1.728 MHz	-111 dBc/Hz @ 3.4 MHz	-80 dBc/.Hz
GSM/PCS-1900 cellular handset receiver	~1.7 G	200 kHz	-132 dBc/Hz @ 1.6 MHz	-108 dBc/Hz
GSM/PCS-1900 cellular base-station receiver	~1.7 G	200 kHz	-149 dBc/Hz @ 800 KHz	-130 dBc/Hz
HP-71209 Spectrum analyzer 1L- freq. band	2.7G-6.2G	n.a.	-115 dBc/Hz @ 100 kHz	-123 dBc/Hz

uments, with the added assumption of a system SNR requirement of 15dB at the receiver output. The spectrum analyzer numbers are from product documentation. A first LO frequency of around 1.7GHz (leaving an IF of about 200MHz) is assumed for the cordless and cellular receivers. Phase noise is listed for the most critical neighboring channel requirement. If the phase noise is assumed to be limited by device thermal noise at the critical offset frequency then equation (25) can be used to compare the requirements of the various applications for a given center frequency at a given offset. The normalized, equivalent phase noise for a 1.7 GHz oscillator at a 100 kHz offset is listed in the last column[5]. The spectrum analyzer's required performance at the middle of the L-band is used to extrapolate its normalized phase noise for comparison purposes. Performance requirements for the high end of the L-band (6.2 GHz) are even higher.

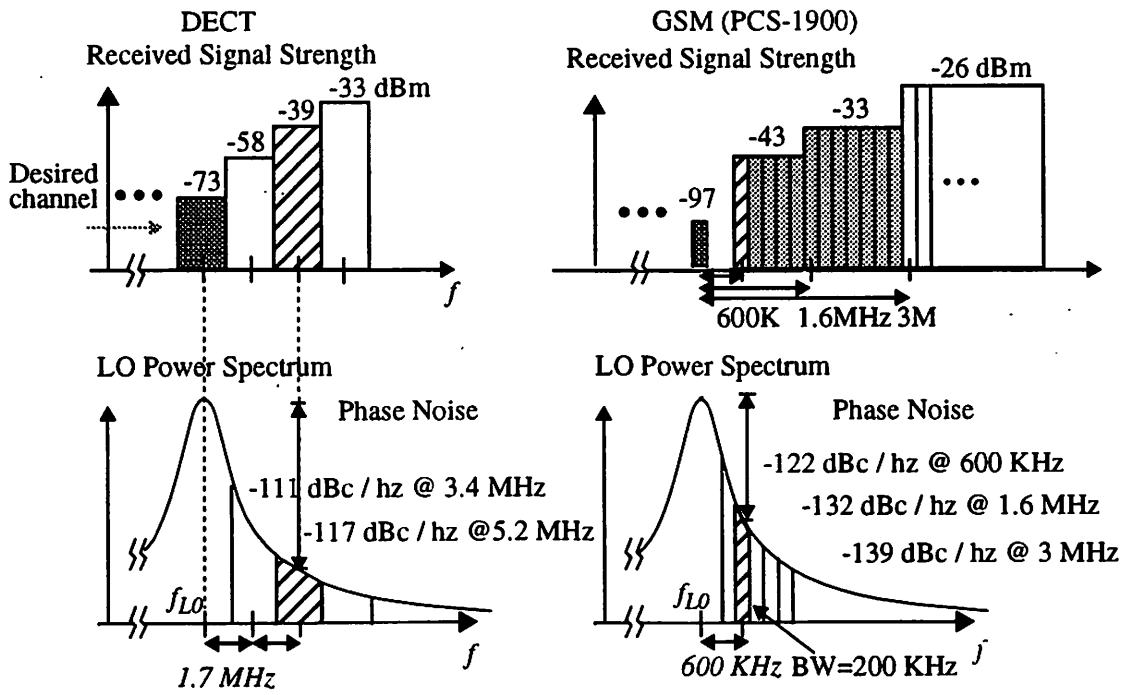
5. A practical comparison of phase noise requirements for different offset frequencies and different center frequencies requires consideration of PLL loop bandwidth and many other factors. The phase noise relationship predicted by equation (25) is just one dimension of a multi-dimensional problem. However, in most cases it is one of the most important dimensions.

The cordless telephone environment is usually less hostile than that of a cellular phone. There is one base-station per phone and interfering signals which come from other users, or their base stations, usually have more walls or distance to traverse. DECT uses wide channel spacings and achieves further diversity through time-division multiplexing in each channel [57]. Wide channel spacing means that neighboring channels are further away from the LO center frequency and have lower phase noise. Although the bandwidth of each channel grows with increased spacing, the $(1/f_m)^2$ roll-off in phase noise results in a net improvement in an oscillator's ability to meet phase noise requirements.

The second example in table 1 is for the PCS-1900 cellular telephone standard, the latest generation personal communications (cellular) system being employed in North America. One of the main advantages of good selectivity in the cellular telephone environment is not just the possibility of better quality phone calls, on average, but the ability to accommodate more users for a given quality of service. Increased capacity means a better return on investments in infastructure and lower air time charges for the end-user. For this reason, phase noise requirements are generally very tight in cellular communications systems, requiring excellent VCO's in both portable handsets and base-stations. The phase noise requirements for a PCS-1900 handset compared to those for a DECT cordless phone are illustrated in figure 3.3. This standard requires lower phase noise then DECT at even closer offset frequencies. The normalized, equivalent phase noise requirement for the same offset frequency is 28dBc/Hz lower for PCS-1900.

Base station phase noise requirements are even more stringent since they are deployed in relatively low numbers, compared to handsets, and can afford to bear more of the burden of interferer power management. Also there is more interfering energy atop a base-station tower due to all of the other transmit channels which are present.

Finally, spectrum analyzers, and other instruments which use local oscillators,



Normalized, equivalent phase noise @ 100 KHz offset:
DECT -80 dBc/hz *PCS-1900 -108 dBc/hz*

Figure 3.3 DECT / PCS-1900 phase noise specification comparison

require low phase noise to increase the dynamic range of their measurements. Most instrumentation applications are produced in lower volume, with less need for integration and more emphasis on performance. Synthesizers for these applications are free to have the highest quality oscillator sources. Also, since finer frequency spacings than in wireless communications are required, more complicated frequency synthesizer architectures are often needed [58],[59]. Advanced synthesizer architectures include numerous mixers and filters in addition to the basic oscillator source or sources. There are also classes of synthesizers, called direct frequency synthesizers, which do not use a PLL at all [58].

With different performance levels required for different applications, there is a considerable range of engineering trade-offs involved in the design of RF frequency synthesizers. This fact will be investigated in the next section, which deals with the dif-

ferent issues surrounding PLL and PLL component design. The synthesizer in a cordless telephone application, for example, may be a prime target for a lower-cost, high integration solution. If the opportunity exists to integrate most of the PLL components in a single IC (maybe even with other parts of the receiver) then there is a large added benefit to integrating the VCO as well. Although on-chip VCO's are usually noisier than those which employ off-chip resonance elements, it may still be possible to meet the less aggressive phase noise requirements of the cordless telephone environment. On the other hand, the exceptional phase noise and stability required in high end applications may warrant exceptional cost and complexity in the synthesizer design and its components. For example the temperature stability required in some military and space applications often requires an oven-controlled-crystal-oscillators (OCXO), where a thermal feedback loop is established to control the reference oscillators operating temperature.

3.2 Frequency Synthesizer Design

The topic of frequency synthesizer design is a very broad one and is as old as the subject of radio itself. There has been a considerable amount of work done over the past four decades in this area. Key application areas include RF and microwave transceivers for military and space applications as well as high performance instrumentation. The books by Manassewitsch, U.L. Rohde and W.P. Robins ([58],[59],[60]) are good references on the subject, covering the many issues surrounding the design of synthesizer components as well as trade-offs in the design of the system. A brief overview of this subject will be presented in this section with an emphasis on the simple, single-loop PLL based frequency synthesizers found commonly in RF transceivers. This introduction will also have a bias towards the design trade-offs and component characteristics most relevant to moderate performance level transceivers for cordless and cellular telephony applications. Since these applications also have higher market volume there is a

considerable interest in highly integrated, or even fully-monolithic, synthesizer implementations. High integration can also result in smaller form factor, lower cost, and lower power consumption, which results in longer battery lifetimes for portable handsets. Some of the design trade-offs for such systems will be investigated.

3.2.1 Synthesizer Architectures and Components

One of the most common frequency synthesizer architectures in RF transceiver applications is the indirect, PLL synthesizer introduced in chapter 2. This structure, which is depicted in figure 3.4, can be used to generate a number of closely spaced RF

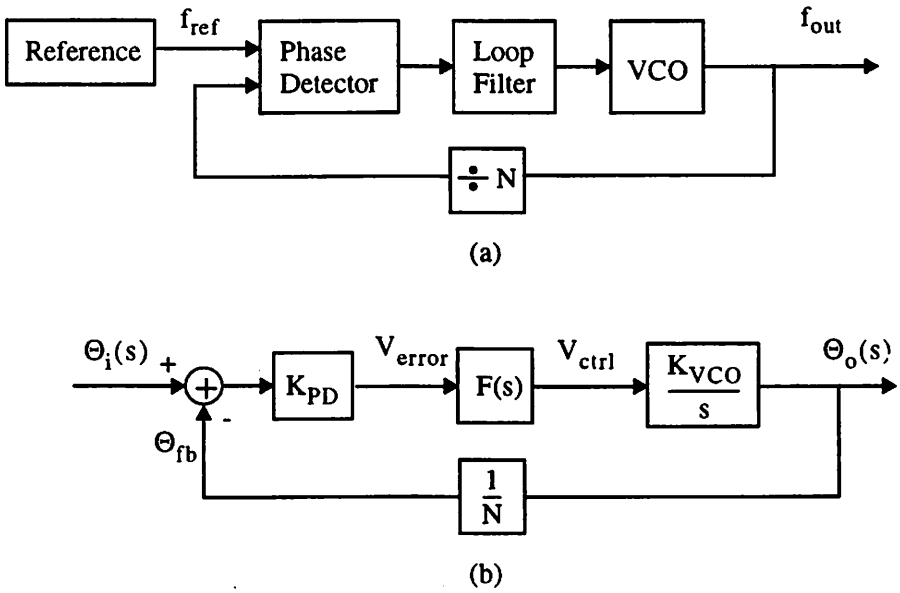


Figure 3.4 Single loop PLL frequency synthesizer: (a) block diagram, (b) small-signal AC model

output frequencies. A relatively small number of components are needed for this function, helping to keep costs down - an important consideration for systems where portable handsets are deployed in large numbers.

A phase-locked-loop frequency synthesizer consists of two oscillators (a reference oscillator and a VCO), a phase detector, loop filter, and a frequency divider. Depending on where the output signal needs to be delivered an RF output buffer may be

needed as well. The VCO is tuned by the phase-locked-loop to be a multiple of the reference frequency. A crystal oscillator is generally employed for the reference due to its low phase noise as well as its high accuracy which insures good frequency matching between the transmitter and the receiver. If RF crystal oscillators existed which could be tuned in multiples of a basic reference frequency then there would be no need for the phase-locked-loop. However, the absence of such ideal devices means that the use of PLL with an RF VCO is the best approach for most applications. The alternative, called direct synthesis [58], is to have an array of crystals oscillators- one for each output frequency that needs to be synthesized - and an array of frequency multipliers to translate the crystal osc. outputs to the desired RF frequency (RF crystal oscillators are not easily implemented). This approach is very expensive by comparison, except for the case of a fixed frequency oscillator. Even then, however, the design of a PLL may be easier than a chain of multipliers, which requires multiple mixing and filtering stages [58]. One of the advantages of non-pll based synthesizers, however, is that there is only one oscillator's phase noise to worry about rather than two.

When the phase-locked-loop in figure 3.4 is in equilibrium, the negative feedback loop forces the phase and frequency of the output to match that of the reference. Since the output frequency is divided by N before comparison with the reference, its frequency in lock is given by

$$f_{out} = N \times f_{ref} \tag{26}$$

In general, there can also be a divide by M block in the forward path, between the reference oscillator and the phase detector, in which case

$$f_{out} = \frac{N}{M} \times f_{ref} \tag{27}$$

The frequency divider in the feedback loop is usually implemented as a programmable divider, allowing the output frequency to move in increments of the reference frequency. For example, suppose the nominal LO output frequency in a radio

receiver for the first LO is 800 MHz, and the reference frequency is 1MHz. With a programmable divider capable of dividing by $N = \{800, 801, 802, ..., 810\}$, output frequencies in the range of 800, 801, ...810 MHz can be synthesized with the selection of the appropriate divider ratio. The output frequency of the LO is used to determine which incoming channel is translated to IF in the radio receiver. By changing the setting on the programmable divider, the LO can be moved in increments of the reference frequency and used to tune-in the desired radio channel. The channel spacing is set by the reference frequency and is based on the radio standard being implemented by the receiver. For a GSM cellular phone receiver the channel spacing is 200 KHz and there are 60 channels. With an 800 MHz LO1 frequency for the first channel, this would require a programmable divider with a range of $N = \{4000, 4001, ..., 4060\}$, for example. This may seem rather large at first, but is actually reasonable to implement.

There are a number of other trade-offs which depend on the choice of reference frequency and divide-ratio, however, some of which will be discussed shortly. A good reference on dividers can be found in [61], in addition to the coverage in [58] and [59]. A programmable divider is usually implemented with a dual-modulus prescaler and additional counters to determine how many times to divide by each modulus for a given divider setting. Prescalar design can often be challenging due to the high input frequencies involved.

The loop filter in a phase-locked-loop is used to compensate the negative feedback loop used in the system. The s-domain small signal AC model of the PLL in figure 3.4(b) was first introduced in the section 2.2. The loop filter is used to set the appropriate unity gain frequency and guarantee stability when the other parts of the system have been specified (phase detector gain, VCO gain, divider ratio, etc.). The design of the loop filter is similar to the design of compensating networks in operational amplifier applications [62],[63]. One goal is to allow for as much low-frequency open loop gain in the system as possible (this helps the loop to reject noise and phase noise added within the loop). This can be accomplished by a second order filter with a pole at DC, a

leading zero before the nominal unity gain frequency, to provide for adequate phase margin, and a second pole after the unity gain frequency to help improve high frequency rejection [64]. Transfer functions for the loop filter and the resulting loop transmission are shown in figure 3.5. A network with this transfer function (from current in to volt-

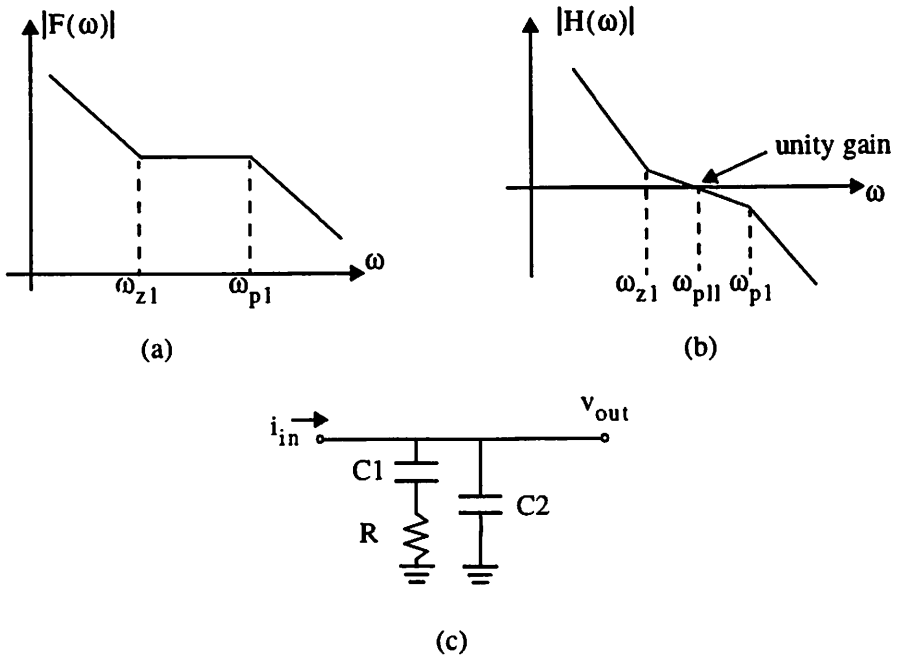


Figure 3.5 Transfer functions for: (a) Second order loop filter F(s), (b) PLL loop transmission (c) Second order loop filter network example

age out) is shown in figure 3.5(c).

In some instrumentation applications such as spectrum analyzers and RF signal sources, frequencies with much finer spacings than those encountered in wireless communications need to be synthesized. In this case, the basic single loop PLL in figure 3.4 is not likely to adequately address all of the trade-offs in the system design. If 1 kHz channel spacings are desired at an output frequency of 2 GHz, for example, a loop with a divide ration of $2 \cdot 10^6$ is not likely to be the most practical solution. The use of multi-loop synthesizers and additional offset mixers in frequency synthesis are often the solution for these systems. More details on the design of such systems can be found in [58] and [59].

3.2.2 Phase Noise and Spurious Tones

With an introduction to PLL based frequency synthesis in place, our attention now returns to the matter of phase noise and spurious tones. Section 2.3.4 introduced the phase-locked-loop and described the influence of reference and VCO phase noise on the output spectrum. Equation (15), a well known result from [64] and other references, predicted that the phase noise of the VCO was suppressed for frequencies within the bandwidth of the PLL and the phase noise of the reference was suppressed for frequencies above the bandwidth of the PLL. This equation is repeated here for reference.

$$S_{out}(\omega) = S_{ref}(\omega) \cdot N^2 \cdot |H_1(\omega)|^2 + S_{vco}(\omega) \cdot |H_2(\omega)|^2 \tag{28}$$

Despite the factor of N^2 which multiplies the reference phase noise, this term is usually much lower since the "Q", or quality factor, of a crystal resonance element is extremely high, usually better than that attainable for LC-tank based VCO's. In addition, phase noise is inherently lower at lower center frequencies. Therefore the effect of multiplying a crystal with the same "Q" as an LC-tank based oscillator to the same frequency would result in the same phase noise (consider equation (25)).

Given that the reference oscillator phase noise is lower than that of the VCO, the discussion in section 2.3.4 (summarized in figure 2.12) seems to indicate that the PLL bandwidth should be increased for optimum performance. This, however, is not the case because of other non-idealities which also limit the performance of the PLL. The most notable of these is spurious tones due to the non-ideal operation of the phase detector. This is the main topic of the rest of this section.

The closed loop transfer function of the PLL from input to output is has a low-pass filter transfer function. This filter is represented by $H_1(\omega)$ in equation (28). For noise or distortion sources whose contributions are applied directly to the input node, a lower PLL loop bandwidth helps reduce the impact of the source on the output signal. Raising the PLL loop bandwidth has a contrary effect. One of the key phenomenon in a

PLL is the feedthrough of energy at the reference frequency to the VCO causing spurious modulation tones in the sidebands of the oscillator. To see where this comes from consider the open loop PLL block diagram in figure 3.6.

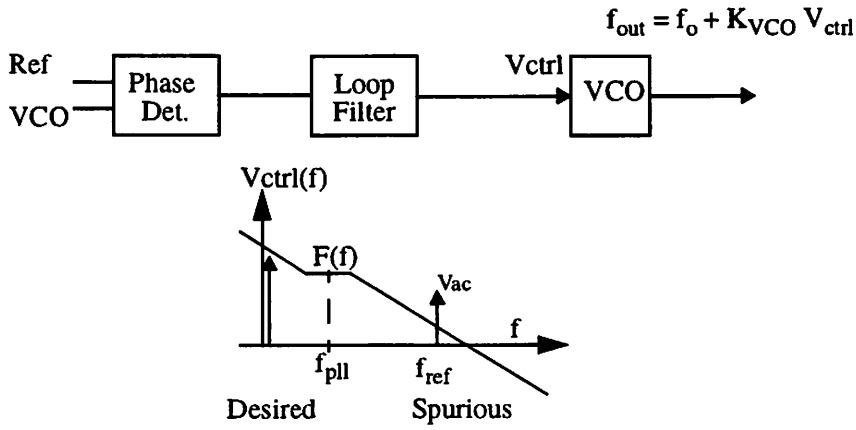


Figure 3.6 Open loop PLL

The ideal input signal to the VCO is simply a DC value which determines the correct output frequency. The output frequency determined from the DC control voltage value is

$$f_{out} = f_c + K_{VCO} \cdot V_{ctrl} \tag{29}$$

where f_c is the center frequency of the VCO with zero control voltage applied. If the spectrum of the control voltage signal includes AC energy at the reference frequency due to the non-ideal operation of the phase detector, however, then the output will be modulated.

For small interfering signals this can often be modeled as classic narrowband FM modulation [65]. This situation is depicted in figure 3.7. If a sinusoidal interfering signal with amplitude v_{ac} and frequency f_m is added to the ideal DC input of a VCO, then the output waveform is given by

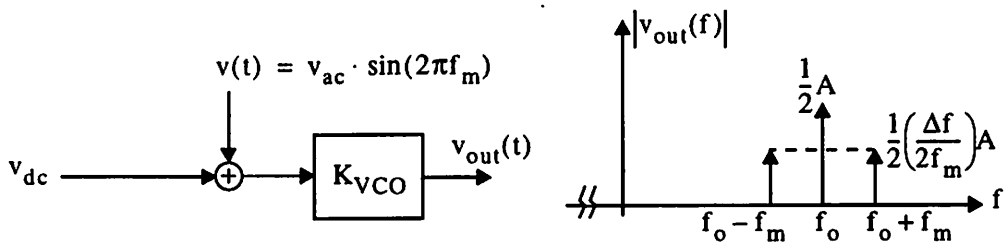


Figure 3.7 Narrowband FM spurious tone generation (only positive frequencies shown)

$$v_{out}(t) = A\cos(2\pi f_o + \Delta f \cdot \sin(2\pi f_m)) \tag{30}$$

where $\Delta f = K_{VCO} \cdot v_{ac}$ is defined as the peak frequency deviation. For small modulation factors, when $\Delta f \ll f_m$, the output has the spectrum shown in figure 3.7. There are two spurious tones in the output, one at $f_o + f_m$ and one at $f_o - f_m$. The height of these tones relative to the carrier is given by $\Delta f / 2f_m$. In power (dBc), this corresponds to a level of

$$P = \left(\frac{\Delta f}{2f_m}\right)^2 = \frac{(K_{VCO} \cdot v_{ac})^2}{4f_m^2} \text{ dBc} \tag{31}$$

The important part of equation (31) to consider at this point is its dependence on v_{ac}. Other aspects of it will be considered later. Equation (31) suggests that the height of a spurious tone is improved by lowering the amplitude of the interfering signal which modulates the VCO. The key signal of interest here is the feedthrough energy of the phase detector. And this energy, as suggested in figure 3.6, is the product of the AC output component of the phase detector and the rejection factor for the loop filter. Lower spurious tones can be attained through lower PLL loop bandwidths, which result in better filtering of the unwanted signal, or better phase detectors which limit the amplitude of the unwanted signal to begin with. These two topics will be dealt with in succession.

First, since spurious tones can be reduced with lower PLL loop bandwidths, there is a direct trade-off between them and VCO output phase noise. In many frequency synthesizer applications the phase noise of the VCO, although higher than the crystal oscillator, is not so large as to be the dominant factor. In these situations the best strategy is often to use a good VCO, a good crystal reference and then make the PLL loop bandwidth as small as possible. If there are no other factors which influence the choice of the PLL loop bandwidth, then this is often the best approach since it can push the spurious tones below the noise floor of the oscillator and minimize the impact of other noise sources which couple into the system[6].

There are some applications, however, where higher PLL loop bandwidths are required. Examples include local oscillators for frequency-hopped spread spectrum systems which require an agile synthesizer which can switch quickly across a range of different frequencies. Even DECT and GSM phone systems require reasonably fast frequency acquisition by the PLL synthesizer. This places a lower bound on the PLL loop bandwidth. In addition, there is increasing interest in using high PLL loop bandwidths to reject VCO phase noise in some applications. This idea was introduced in section 2.3.4. Figure 2.12 from that discussion is repeated again below for convenience (figure 3.8). If VCO phase noise is reasonably low, then there is not a tremendous advantage in raising the loop bandwidth. However, a VCO with higher phase noise, such as those being pursued for fully-monolithic implementations, may benefit from a higher PLL loop bandwidth. In such cases, the phase noise improvement within the bandwidth of the loop increases with a higher loop bandwidth, as illustrated in figure 3.8 (c).

The second way to improve spurious tones in a PLL is to reduce the amplitude of the unwanted signal at the output of the phase detector to begin with. This requires an understanding of phase detector design and the various contributors to the AC compo-

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6. Interferers which occur after the loop filter, such as power supply noise coupling to the VCO control line, are not improved with reduced loop filter bandwidths. However, many other important factors do show up as input-referred signals.

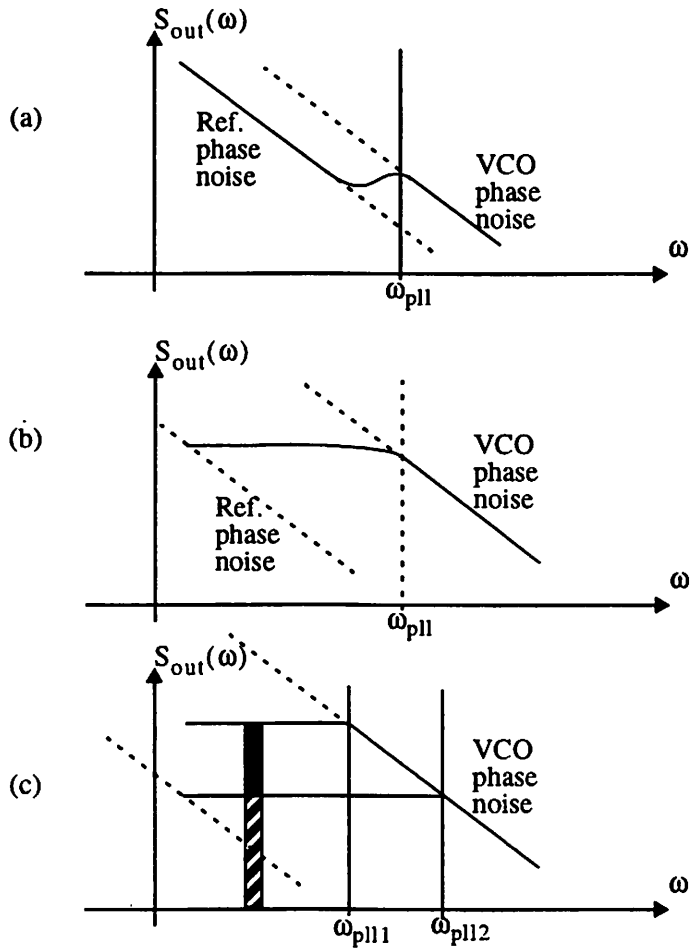

Figure 3.8 PLL phase noise spectrum: (a) nominal case: low reference phase noise, moderate VCO phase noise (b) extreme case: very low ref. phase noise, high VCO phase noise (c) extreme case with different PLL loop bandwidths

nents in its output. A complete summary of phase detector design options is too cumbersome to include here due to the sheer number of different phase detectors options that exist. A good introduction to phase detectors can be found in [64]. What will be provided here, however, is a summary of the nominal output spectrums for various phase detectors, and phase detector / charge pump combinations (see figure 3.9). This information can be deduced from examination of phase detector output signals in [64] and [66].

The first example in figure 3.9 is a conventional mixer type phase detector. When the incoming signal is mixed with the fed back signal from the VCO an output signal at the sum and difference frequencies results. The signal at the difference fre-

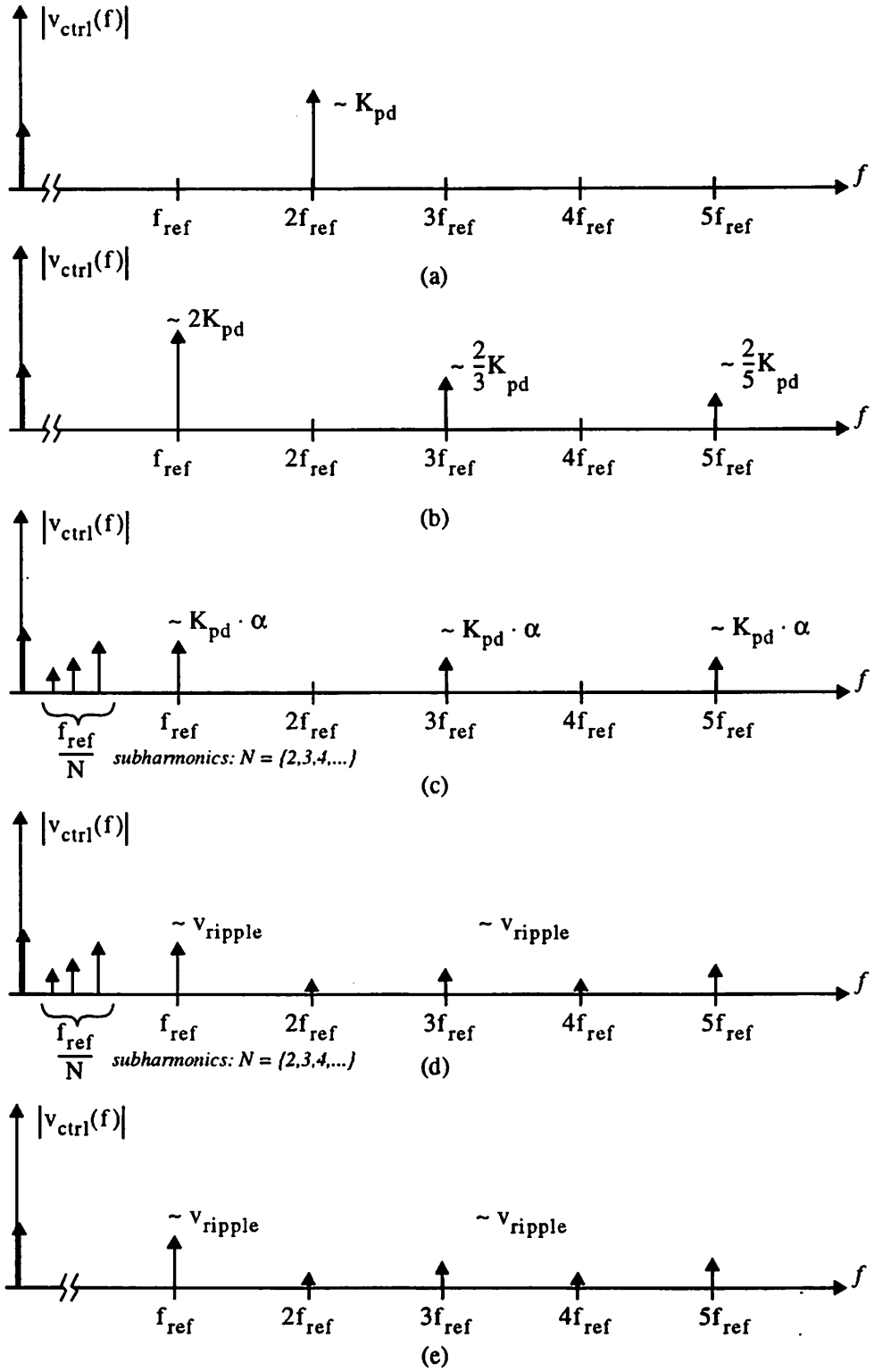

Figure 3.9 Phase detector output spectrum for typical operation: (a) Mixer type PD, (b) Exclusive OR PD, (c) Three state PD, (d) z-state PD, (e) Dead-zone free PD w/ charge pump

quency, which is DC, is proportional to the phase difference between the two inputs to the phase detector. This is the desired phase detector output. In addition, however, there is an unwanted signal at $f = 2f_{ref}$, due to the natural operation of the mixer, which will cause spurious modulation. The height of this signal can be shown to be related to the phase detector gain itself, and therefore cannot be arbitrarily minimized.

The second example in figure 3.9 is for an exclusive OR type phase detector. This spectrum is for the particular case that the DC output control voltage is half-way between its minimum and maximum value. In this case the phase detector output is a square wave with an amplitude that is related to the phase detector gain. The energy in the third, fifth, etc. harmonics follows the fourier series for a square wave. Other DC output control voltages will also result in significant energy at the fundamental as well as the odd harmonics.

A three state phase detector (fig. 3.9(c)) is an improvement over the exclusive OR type arrangement. In this case the energy at the harmonics is proportional to $K_{pd} \cdot \alpha$, where $\alpha = 0$ for the case that the DC control voltage being generated is zero (half way between its minimum and maximum values). This means that the spurs can be very small for frequencies near the center of the VCO tuning range. An additional problem, called the dead-zone problem, does cause concern, however. Very small phase differences are not detectable with a three state phase detector. Phase error may need to accumulate for several cycles of oscillation before there is enough timing difference to trigger the phase detector. In this case the update energy occurs at a sub-harmonic frequency. Spurious tones due to sub-harmonic modulation are often more damaging since there is more spurious energy for a lower frequency modulating source, as predicted by equation (31).

A fourth type of phase detector, with even better performance than the three-state PD, is given in figure 3.9(d). This PD is called a z-state phase detector. In this case the control voltage output is left as a high impedance node for most of the time and is only updated occasionally by connecting it temporarily to the low or high supply. The

AC feedthrough for this phase detector can approach zero for any of the desired output control voltages (not just at the center of its range). The only ripple at the output is due to non-idealities in the update switching. This can be much smaller than the systematic feedthrough of the first three phase detectors in figure 3.9. The conventional z-state phase detector does suffer from the dead-zone problem, however, and can have sub-harmonic tones.

The final phase detector output spectrum in figure 3.9 is for a phase detector / charge-pump combination with a dead-zone free phase detector. This combination is described in more detail in [66], [67], and [68]. A dead-zone-free phase detector produces a small width "pump up" and "pump down" update pulse every reference cycle. A charge pump then uses these signals to gate fixed current sources onto a high impedance node (the loop filter input). The "pump up" signal turns on a current source which raises the output voltage (to speed up the VCO) and the "pump down" signal turns on a current which lowers the output voltage. In steady state the "pump up" and "pump down" signals match and there is no net change in the output. Since the update occurs every reference cycle, sub-harmonic tones are avoided. The only spurious energy is due to non-ideal matching of the opposing current sources and/or the timing of the "pump up" and "pump down" gating signals. Although there will inevitably be some mismatch, this effect is much smaller than the other types of phase detector feedthrough considered to this point. The use of a fully differential charge pump, and other techniques described in [67], can result in very low output ripple.

The conclusion of this discussion of phase detectors is that there has been a considerable amount of research done on the topic and detectors with lower and lower output feedthrough have evolved over the years. If a wide bandwidth PLL is desired for an application, then spurious tones can be minimized through the use of one of these advanced phase detector techniques. Of course sufficient attention to detail must also be provided to insure the phase detector feedthrough is minimized over all operating conditions.

The previous discussion has shown how spurious tones in a frequency synthesizer can be improved by lowering the PLL loop bandwidth or lowering the un-desired reference feedthrough by using a better phase detector / charge pump. A third possibility involves using a higher reference frequency in the frequency synthesizer design. Equation (31) predicted that the power of a spurious tone is inversely proportional to the frequency of the modulating source. In conventional single-loop PLL designs, the reference frequency needs to be equal to the desired channel spacing. Therefore the location of the spurs is determined by the radio standard specification. In GSM systems, for example, the channel frequency spacing is 200 kHz.

One exception to this rule is the use of fractional-N frequency synthesizers [69]. In this scenario a divider capable of dividing by an integer multiple plus a rational fraction (e.g. 25 1/4) is used in the feedback path of the PLL. The output frequency is then tunable in multiples of the reference frequency times the fractional modulus of the divider. For a given channel spacing the reference frequency can be increased, and the PLL loop bandwidth can be increased as well (while still meeting stability requirements). In this situation however, there is still spurious energy at the channel spacing frequency due to the operation of the fractional divider. A fractional divider is normally implemented by dividing by two different integer multiples with a duty cycle that results in the desired "average" fractional divider ratio. This effect results in a small, systematic phase error signal referred to the input of the PLL. As a result there is spurious energy at sub-harmonics of the reference frequency. For some of these divider ratios the sub-harmonic is at the channel spacing frequency, leaving us back to where we started with regard to the spur problem.

Another possibility for increasing the reference frequency, however, does exist if changes are allowed in the overall radio receiver architecture. This idea involves the reversal of the roles of the first and second LO's in a conventional super-heterodyne receiver. Normally the first LO is used to mix the desired incoming channel down to an intermediate frequency (IF) and a fixed-frequency second LO is used to mix the narrow-

band signal at the IF down to baseband. Since the IF signal is at a fixed frequency, a highly selective filter can be employed at that stage to reject adjacent channels. Another approach, however, is to use a fixed-frequency first LO to mix the signal down to IF and a variable-frequency second LO to translate the desired signal down to baseband. This approach has been described recently in [54] and [55]. In this case the signal at IF is wide-band and the channel select filtering is saved for baseband. The benefit of this approach is that it eliminates some of the classic constraints for RF frequency synthesizer design. Now, since the first local oscillator is at a fixed frequency, a higher reference frequency can be used to help reduce spurious tone energy. In addition, if the reference frequency is high enough, the spurious tone may even be pushed out of band. In this case the front-end filters in the receiver help reduce interferer signal strength before it is even mixed with the spurious tone. With spurious tones reduced, the possibility of raising the PLL loop bandwidth to help reduce in-band phase noise exists. A fixed-frequency first LO also leaves room for new types of monolithic local oscillator designs, such as approaches using delay-locked-loops, to be used as low phase noise sources [70].

The second local oscillator benefits from the fact that phase noise, for a given offset frequency, is usually lower for a lower frequency oscillator. This means that the phase noise specifications for a radio standard may be more easily met, even with an on-chip VCO solution, without the need to resort to very high PLL loop bandwidths. As a result, the loop bandwidth can be kept small to reduce spurious tones and the channel frequency spacing can be used as the reference frequency.

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Chapter 4

Jitter in CMOS Ring Oscillator Delay Cells

4.0 Introduction

In the preceding chapters, the role of phase-locked-loops (PLLs) for frequency synthesis and timing recovery applications has been introduced. Phase noise and timing jitter were shown to be important performance specifications in such systems. Particularly critical in PLL systems is the phase noise of the VCO. As described in the last chapter, a high "Q" off chip resonant element is often the most desirable design option. But for highly integrated systems a fully monolithic, on-chip solution to the VCO may be required. Delay cell based VCOs, although noisier than those employing on-chip LC tanks, have significant potential for at least some portion of frequency synthesizer applications. In addition, delay cell based VCOs have been used widely in a number of other applications, such as clock and data recovery, which do not have as serious constraints on thermal noise induced timing jitter as radio applications do.

The question to be answered here is what are the intrinsic, thermal-noise-induced timing jitter and phase noise limits for delay cell based VCOs and how do they depend on delay cell design parameters. Delay cell based approaches include ring-oscillator VCOs as well as voltage controlled delay chains, or VCDs that are used in archi-

tectures such as delay-locked-loops. In both cases a fundamental performance limit arises from the thermal noise and 1/f noise in the transistors that make up the delay stages themselves. Other noise sources, such as power supply noise, substrate noise, and control voltage ripple (as well as many others) can cause fluctuations in the phase of timing signals, as described in the previous chapters. These effects are not the focus of this chapter, however, since they can often be reduced through careful circuit design techniques.

The strategy for analyzing timing jitter and phase noise in the next two chapters is as follows. This chapter attempts to determine, analytically, the relationship between the design parameters of the inverter cell used in a ring-oscillator and the resulting noise-induced timing jitter. The class of circuits analyzed is source-coupled differential delay cells with resistive loads, implemented in CMOS technology, where the loads are realized by PMOS transistors in the triode region. This particular implementation has proven useful in practical implementations because of its high speed and rejection of supply noise [71,72]. The starting point of a single delay stage is not a stage in isolation, but a stage assumed to be part of a delay chain or ring. Amplification of noise from one stage to another is considered, as well as the continuation of jitter passed around the loop in ring-oscillators.

In the next chapter, these results are extended to determine their implications for the design of low-jitter VCO's and buffers. A link from timing jitter to the frequency domain phenomenon of phase noise will also be made at that time. With this, the consideration of phase noise and timing jitter at the buffer / delay cell level, oscillator level, and even the PLL level, as described in chapter 2, can be tied to the design parameters of the individual delay cells. With these results a fair comparison can also be made between the fundamental limits of ring-oscillator VCOs and other VCOs, including those with on-chip or off-chip resonant LC networks.

4.1 Related Analyses of Jitter and Phase Noise in Oscillators

The analysis in this dissertation includes timing jitter and phase noise considerations for several levels of system implementation. Of particular interest in this work are frequency synthesizer applications where the phase noise of the VCO is a critical parameter for the system. Before proceeding with this analysis of ring-oscillators it is worth pointing out the similarities and differences to other analyses of timing jitter or phase noise in oscillators.

There is a wide body of work on phase noise in LC-tuned oscillators, including Leeson [73], Underhill [74], and others [75]. These analyses use a linear circuit model for the oscillator feedback circuit. Analysis is then carried out in the frequency domain to determine phase noise sidebands directly. Experimental results have been matched well with theory, showing among other things, that phase noise improves with the quality factor (Q) of the resonance squared. A comparison of ring-oscillators to LC-tank oscillators will follow in chapter 5. In addition, the link from the frequency spectrum of phase noise back to timing jitter can be made by integrating the noise sidebands ([87]), as described in chapter 2.

Relaxation oscillators and ring oscillators are less amenable to a linear analysis. Analysis for these types of oscillators has been carried out in a number of ways. For relaxation oscillators, Abidi [77] has taken a time domain approach to arrive directly at timing jitter performance. No link, however, is made to phase noise in the frequency domain. In Boon [78], attempts have been made at a linearized model for noise and switching in a relaxation oscillator. The result is a frequency domain derivation of phase noise. Other models mapping voltage noise directly to FM modulated sidebands have also been proposed.

The analysis of noise in ring oscillators has followed in a similar vein as relaxation oscillators, with results for both time domain and frequency domain approaches. In this analysis, timing jitter is derived directly in the time domain, and a link is made

back to the frequency domain to determine phase noise sidebands which result from device thermal noise in the inverter delay cells which make up the ring. This translation will be shown to map well to the $1/f^2$ and $1/f^0$ regions of the phase noise sidebands described in section 2.3.

The time domain analysis in this dissertation relates the internal device thermal noise, to output phase uncertainty directly. For clock buffers and voltage controlled delay chains, this is correct approach since there is no feedback in the structure which forces oscillation. For long chain ring-oscillators, where delay stages have a chance to fully switch before the next period of oscillation, the time domain approach is also the right approach. A linear feedback model for determining phase noise, like that used in LC analysis, does not naturally apply in this case.

A time domain analysis, similar to the approach used in this work has been carried out for bipolar ring-oscillators by McNeill [79,80]. The experimental results in [79,80] also match well with theory. The general conclusions for jitter in bipolar delay cells presented there compare well with the conclusions for CMOS inverters presented in this work. That approach did not include some of the higher-order considerations, such as interstage amplification, that are particularly important in CMOS designs, however. In this work, the implications of delay cell jitter to the trade-offs involved in designing the overall VCO are also derived. This result expresses VCO jitter in a way which separates out the choice of configuration (number of stages, etc.) from the fundamental delay cell design trade-offs, and can be extended to both CMOS and bipolar ring oscillators.

In addition to the time domain approach, phase noise in ring-oscillators has also been investigated directly in the frequency domain. In the limit that a ring is oscillating at a high enough frequency that delay stages do not have a chance to fully switch, then a feedback model can be applied. It has been suggested that a ring oscillator is a feedback oscillator with an effective Q of one. A more detailed analysis, carried out by Razavi [81], defines Q in terms of the derivative of the phase angle function in a linear-

ized version of the ring oscillator loop. Typical Q's in this analysis are in the range of 1.3 to 1.4.

4.2 Individual Delay Cell Timing Jitter

In this section the analysis of ring-oscillator and delay-chain timing jitter begins. The starting point is an individual delay cell, not in isolation, but as part of a ring-oscillator or voltage controlled delay chain. The phrases ring-oscillator, delay chain, VCO, and VCD (for voltage-controlled-delay chain) will be used interchangeably in this section. Also worth noting is that the means by which the oscillation frequency or stage delay is controlled (making it a "voltage-controlled-" element) is not important at this point either. A typical VCO and a voltage controlled delay chain are pictured in figure 4.1.

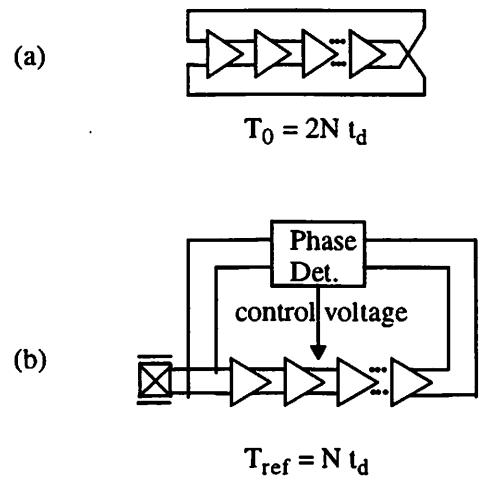

Figure 4.1 (a) Ring oscillator VCO and (b) Voltage controlled delay chain (VCD) configured in delay locked loop.

A ring-oscillator has a total period of $T_0 = 2N \cdot t_d$, where t_d is the nominal delay per stage and N is the number of stages in the ring. A voltage controlled delay chain is usually configured in a delay-locked-loop (DLL) which tunes the delay per stage so that the delay of the entire chain matches the period of the input.

$$T_{ref} = X \cdot t_d \tag{32}$$

In both of these structures the actual delay, t_d, encountered per stage is corrupted by noise in the transistors making up the delay elements, leading to timing jitter[1]. The goal of this section is to determine the total timing jitter imparted to the delay chain from the noise sources present in the delay cell. What is desired is an analytical relationship between the design cell parameters of an inverter cell and the resulting noise-induced jitter in the ring oscillator or delay chains it is employed in: an expression for the r.m.s. timing error Δt_d, that accompanies each nominal delay of t_d (figure 4.2).

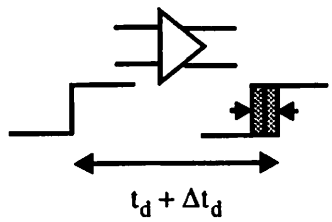

Figure 4.2 Intrinsic timing error per delay stage

As mentioned in the introduction of this chapter, the class of circuits that will be considered initially are source-coupled differential delay cells with triode region PMOS transistors serving as resistive loads (figure 4.3). This particular implementation is useful in practical applications because of its high speed and rejection of supply noise [72]. Focussing on a particular circuit configuration at this point will greatly facilitate the analysis. The results which follow, however, are readily generalized to other configurations[2].

This delay cell consists of NMOS differential pairs with triode region PMOS

1. Mismatch between devices can also create differences in the time-delay from stage to stage, but this is a systematic error for any given delay chain. This has an important impact in some DLL applications, but is not the fundamental thermal noise (and 1/f noise) problem being analyzed at this point.

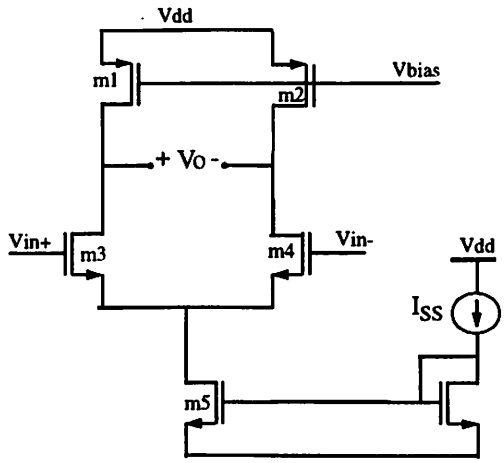

Figure 4.3 Differential delay cell

resistive loads. The gate drive for the PMOS transistors is carefully controlled by a replica biasing circuit (to be described later) so that the voltage swing is kept constant over process and temperature variations. In the circuit implementations described later in this thesis, the voltage swing for a stage was chosen to be 1 V. This means that with all of the current flowing through one side of the differential pair, the replica bias circuit adjusts the PMOS gate bias so that there will be a 1V drop across the triode PMOS resistor. Larger swings are often desirable, but conflict with other circuit design criterion. A typical DC transfer characteristic for the cell is shown in figure 4.4.

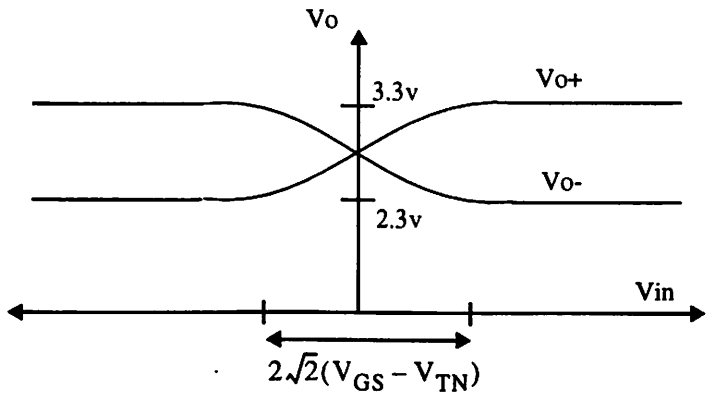

Figure 4.4 DC transfer characteristic of inverter cell with 1v swing.

2. As this analysis proceeds from individual delay cell jitter to the overall jitter in ring-oscillator and delay-chain structures, many of the higher level conclusions will be independent of the details of the individual cell circuit configuration.

The aspect of the delay cell of primary concern in this section is device thermal noise and its impact on timing jitter. The schematic for this inverter cell is repeated in figure 4.5 with thermal noise sources added. These are the intrinsic output referred ther-

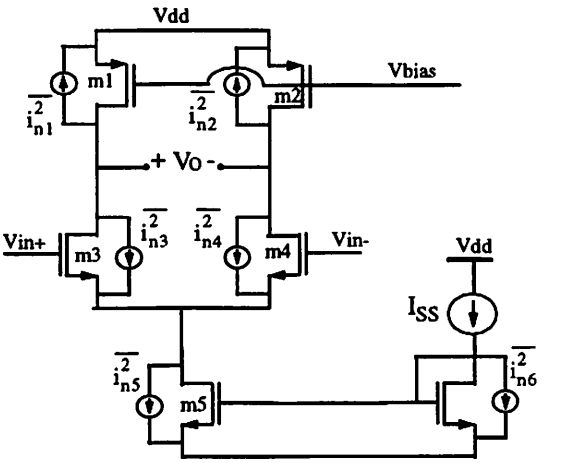

Figure 4.5 Differential delay cell with noise sources

mal noise current sources for each transistor, and should not be confused with the input referred noise sources used at other times when modeling noise [82]. The NMOS transistors in the delay cell circuit are operated in saturation. For saturation region devices the thermal noise current power spectral density is given by:

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma g_m \tag{33}$$

where g_m is the transconductance for a given bias condition and γ is also function of bias. In traditional noise analysis, γ is usually 2/3. This result is a good approximation for long channel devices. For short channel devices, however, experimental results ([84][85]) suggest that γ 's value is higher, and increases with increasing v_{ds}. For short channel devices in deep saturation γ can be as high as 2 or 3.

The PMOS devices in the circuit in figure 4.5 are operated in the triode region of operation. The thermal noise current power spectral density in this case is modeled by:

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma g_{dso} \tag{34}$$

where g_{dso} is the zero-bias drain to source conductance and γ varies from $1 < \gamma < 2/3$ as v_{ds} varies from zero to the onset of saturation [83]. A more complicated model for triode region current noise in short channel devices is given in [85], which models both the triode and saturation regions well. However, for devices that are biased well into the triode region, the usual case here, the simpler model in [83] suffices, and for the most part γ will be fairly close to one.

4.2.1 Modeling Circuit Noise Induced Timing Jitter

The noise sources described in the previous section introduce timing jitter by corrupting the rising and falling edges that propagate through chains of delay cells. To understand this process models are needed for both the noise and for signal propagation in delay chains. Consider the chain of inverters and the associated timing waveforms in figure 4.6

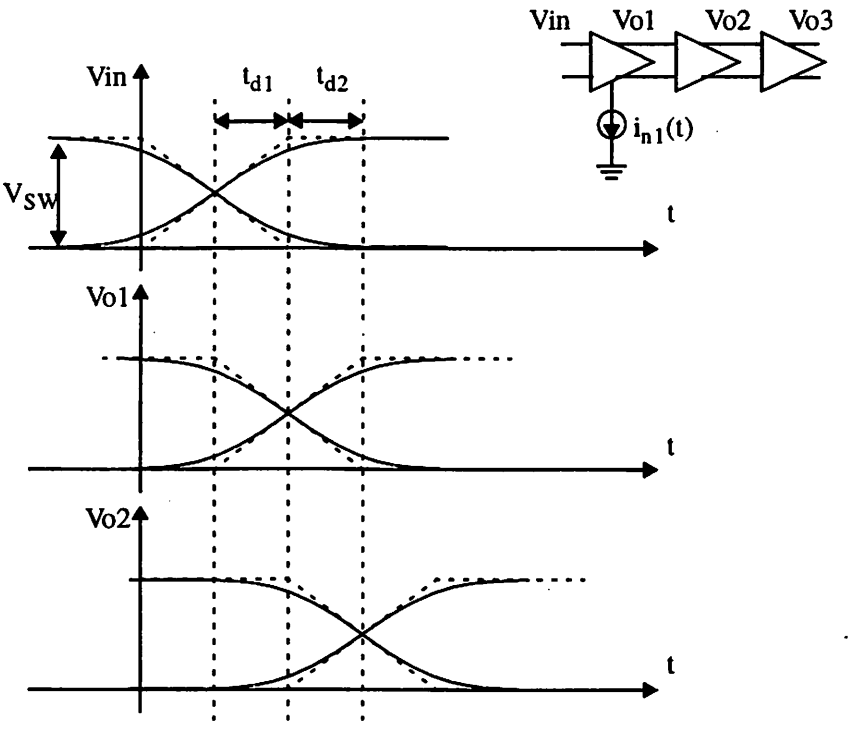

Figure 4.6 Inverter cell delay chain timing waveforms

The timing waveforms in this figure are a potential source of confusion. It is important to distinguish between the DC transfer function characteristics for a delay cell, as shown back in figure 4.4, and the time varying signal considered here. When a given differential input voltage is applied to an inverter, it produces a differential output current which begins to change the state of the output. The integration of this current over time produces the output waveform. At the same time, however, the differential input voltage is changing, creating a time varying current. At some point, for large enough differential input voltage, the inverter delay cell's current is fully tilted to the opposite side after which the output simply settles in a combined slew-rate / rc limited fashion with a current that no longer depends on the applied input voltage! This behavior has been approximated by the idealized waveforms in figure 4.6, where waveforms have been drawn with an effective "overlap of two". For this case we show the first stage output beginning to switch strongly when the differential input reaches zero. The input continues to settle for the second half of its ascent while the output of the first stage is proceeding with the first half of its ascent. Likewise, when the output of the first stage reaches a differential voltage of zero, the second stage begins switching strongly, and the pattern repeats. The timing delay is measured from the midpoint of one stages output transition to the midpoint of the next.

Most analyses of noise in inverter chains assume a timing waveforms model similar to the one considered above, with a further assumption that simplifies noise analysis [71]. They assume a situation much like that experienced in a relaxation oscillator [77]. The assumption, in effect, is that each stage is separated by an ideal, noiseless buffer as in figure 4.7. The ideal buffer outputs initiate switching in the next stage when the differential output voltage of the previous stage crosses zero. The time delay per stage can easily be calculated in this case, as

$$t_d = \frac{C_L V_{SW}}{I_{ss}} \tag{35}$$

where V_{SW} is the total change in the differential output voltage at the 50% point of the

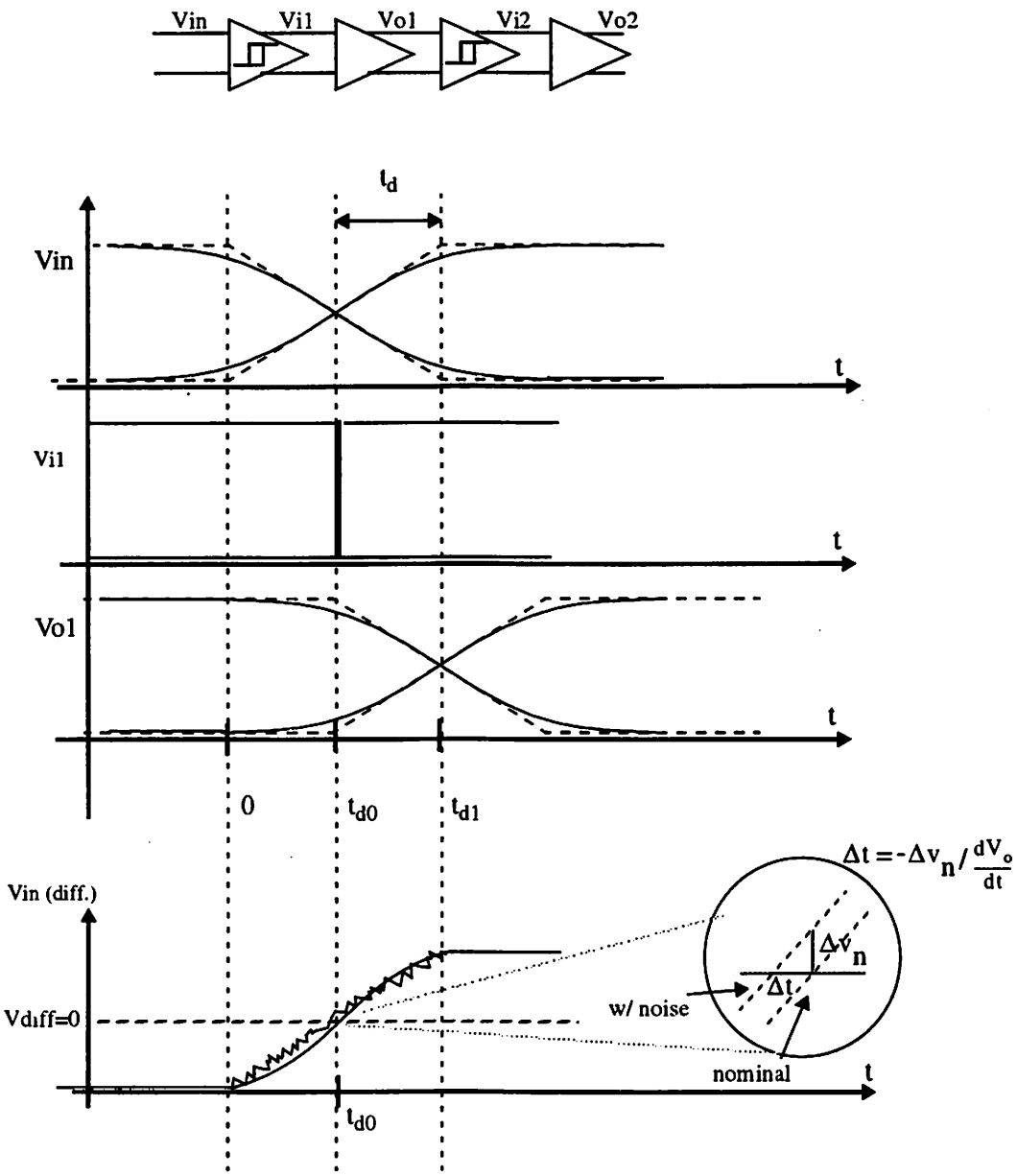

Figure 4.7 Inverter delay cell chain with ideal buffers between stages.

transition, and I_{SS}/C_L is the average (differential) slew-rate. Incidentally, this picture is consistent with "overlap of two" waveforms shown in figure 4.6.

The timing error per stage due to noise can also be easily calculated thanks to the assumption that the next stage will begin switching abruptly when the differential output voltage reaches zero. In exact terms, this amounts to a problem known as the "first crossing problem" [76, 77], the problem of predicting the time of the first thresh-

old crossing in the presence of noise. A useful approximation, frequently employed in this case is called the "first crossing approximation", and is illustrated at the bottom of figure 4.7. For a voltage error at the nominal time of crossing of magnitude Δv_n, the actual time of crossing would be offset by an amount equal to Δv_n divided by the slope the line through zero, or the slew rate. The first crossing approximation predicts that the variance of the timing jitter in this case is equal to the variance of the voltage noise divided by the slew rate squared, or

$$\overline{\Delta t_d}^2 = \overline{\Delta v_n}^2 \cdot \left(\frac{C_L}{I_{SS}}\right)^2 \tag{36}$$

This equation serves as a link from voltage noise uncertainty to timing jitter uncertainty and will be employed frequently in the analysis which follows. Although the "ideal buffer" assumption illustrated in figure 4.7 will be relaxed and a better model will be employed later, the basic form of the relationship in (36) will still be useful. The timing jitter accumulated by a signal passing through multiple delay stages is also readily determined with the "ideal buffer" assumption. Since full switching is initiated when the differential input voltage reaches zero, the voltage noise of one stage simply shifts the timing of the beginning of the next and has no further effect. For independent noise sources the total jitter variance at the end of N stages is just $N \cdot \overline{\Delta t_d}^2$. The "ideal buffer" assumption does neglect some very important effects, however, like the amplification and filtering of noise in one stage by the stage which follows. These will be dealt with in the analysis which follows.

The timing jitter equation in (36) has some interesting implications when combined with (35). Normalizing the timing error experienced per delay, Δt_d, to the time delay per stage $t_d = C_L V_{SW}/I_{SS}$ we have

$$\frac{\overline{\Delta t_d}^2}{t_d^2} = \overline{\Delta v_n}^2 \cdot \left(\frac{C_L}{I_{SS}}\right)^2 \left(\frac{I_{SS}}{C_L V_{SW}}\right)^2 \tag{37}$$

Taking the square root of each side and simplifying this yields

$$\frac{\Delta t_{d\,rms}}{t_d} = \frac{\Delta v_{n\,rms}}{V_{SW}} \tag{38}$$

This equation shows that the timing error encountered per delay stage normalized to the time delay, is equal to the r.m.s. noise voltage at the output normalized to the output voltage swing V_{SW}. This is a very simple, yet powerful result. It states the intuitively pleasing conclusion that the timing error, as a percentage of the total timing delay, can be improved by improving the output voltage noise as a percentage of the total output swing. Therefore normalized timing error can be improved by lowering the output voltage noise for a given swing, or raising the voltage swing for a given level of noise. This has practical implications of this for design of low jitter delay cells.

Later, in chapter 5, these implications will be shown to be a key factor in the design of low-jitter ring-oscillators and delay-chains. At this point, however, our goal is to further refine (38) through successively better approximations to the voltage noise $\Delta v_{n\text{-}rms}$ present at the output of our inverter delay cells, and to express the ratio $\Delta t_{d\,rms}/t_d$ in terms of basic delay cell design parameters.

The basic path for this analysis is to proceed from the intrinsic device thermal noise current sources outlined previously, to voltage noise at the output of the inverter cells in a delay chain, to timing jitter. There are several complications along the way, however. For one, the noise sources in a switching delay cell are time-varying, requiring a more sophisticated set of mathematical tools to analyze than the ac noise analysis approach that could be applied to constant noise sources. Secondly, the switching times of adjacent stages in a CMOS inverter chain overlap and there are times when more than one stage is in the active region of amplification. In this case the "ideal buffer" assumption (figure 4.7) comes into question. It is not sufficient to consider the noise contribution of a single inverter alone, in this case, since noise from one inverter may be amplified and filtered by the next stage, contributing to the jitter in subsequent stages in that manner.

The approach taken in this section will be to break the analysis up into three passes. On the first pass, simplifying assumptions, including constant noise sources, will be made so that the basic path from current noise to output voltage noise to timing jitter can be illustrated. On the second pass, the effects of time varying noise sources will be added and a more sophisticated analysis approach using autocorrelation functions for the noise sources will be employed. And finally, on the third pass a complete analysis will be performed using the tools from the second pass but applying them to a higher order system, taking into account the effects of interstage amplification. The key assumptions for each of these analyses are summarized in Table 2.

Table 2: Timing jitter analysis assumptions

	Simplified analysis	Advanced analysis	Complete analysis
Diff. pair transistor noise model	constant equilibrium value	time-varying piecewise constant model	time-varying piecewise constant model
Current source trans. noise model	constant equilibrium value	time-varying piecewise constant model	time-varying piecewise constant model
PMOS load trans. noise model	constant	constant	constant
Noise analysis	freq. domain	time domain / autocorrelation function analysis	time domain / autocorrelation function analysis
Jitter translation	first crossing approximation at output of first stage	first crossing approximation at output of first stage	modified first crossing at output of next stage
Interstage amplification	none	none	next stage amplification

4.2.2 First Pass: Simplified Analysis

The first step in determining the timing jitter in delay chains is to find the output voltage noise which results from the intrinsic thermal noise current sources in the inverter delay cells. For an inverter cell in equilibrium (no inputs changing) the output noise voltage can be determined through traditional noise analysis techniques [82]:

$$\overline{v_{on}}^2 = \int_0^\infty \overline{i_{n1}}^2(f)|H_1(f)|^2 + \overline{i_{n2}}^2(f)|H_2(f)|^2 + \ldots + \overline{i_{n6}}^2(f)|H_6(f)|^2 df \qquad (39)$$

where $\overline{i_{n1}}^2(f), \overline{i_{n2}}^2(f), \ldots, \overline{i_{n6}}^2(f)$ are the noise power spectral densities for transistors M1, ... M6 in the inverter cell (figure 4.5) and $H_1(f), H_2(f), \ldots, H_6(f)$ are the transfer functions for those noise sources referred to the output. In the first pass analysis the noise sources are assumed constant, with values given by the condition where the delay cell is biased with zero differential input. An approximate small-signal equivalent circuit for the inverter delay cell, in this case, is shown in figure 4.8(a). The triode region PMOS transistor is replaced by a resistor with value, R_L, equal to the output resistance of the load device. And the capacitance C_L represents the total capacitance at the output node. Using this simplified circuit, the approximate transfer functions for each of the noise sources, $i_{n1}, i_{n2}, \ldots, i_{n6}$ can be determined.

For AC noise calculations, the equivalent circuit in figure 4.8(b) can be used. Here, the approximate transfer function to the output for each of the noise sources is shown. For the current source and biasing transistors (M5,M6), approximately half of the current noise shows up on each side of the differential output. Therefore a common mode noise signal results at the output, but not a differential one. The PMOS load transistor (M1,M2) noise sources each contribute their full current to the output on their respective sides. And finally, the approximate transfer function to the output of the NMOS differential pair noise sources (M3,M4), is as shown in the figure. The transfer

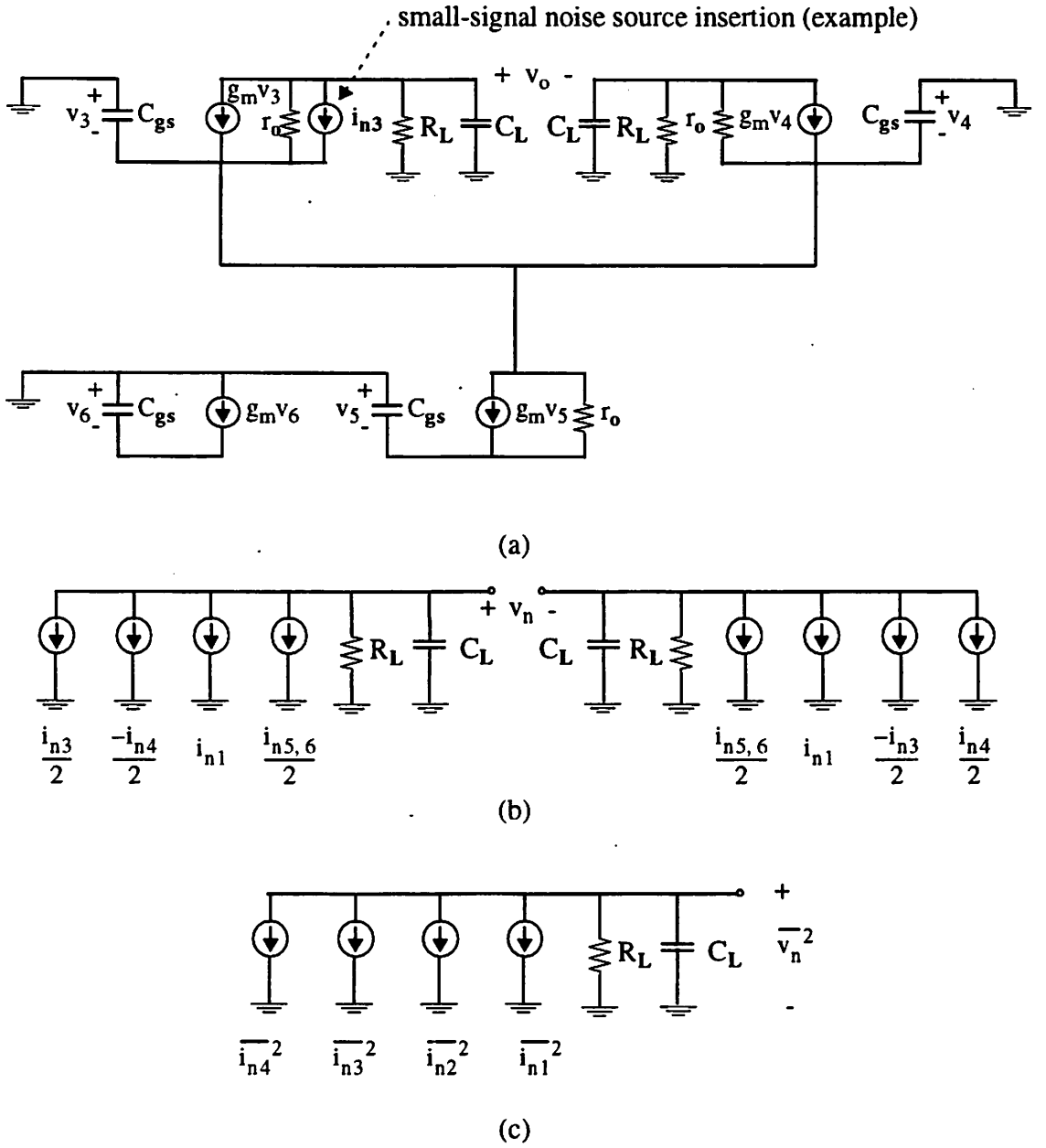

Figure 4.8 Small signal equivalent circuit for inverter delay cell: (a) overall circuit, (b) equivalent circuit for AC noise calculations, (c) Simplified, diff. AC noise calculation circuit

function for these noise sources is more complicated since they shunt the transistors in the differential pair. It can be shown, by inserting the current noise generators for M3 and M4 into the small signal equivalent in figure 4.8(a), that approximately half of the noise current will show up at each side, with an inversion in the sign between one side and the other[3].

For differential noise calculations, the circuit in figure 4.8(b) can be replaced by the circuit in figure 4.8(c). This circuit is equivalent for determining the output, AC, differential voltage noise. In this circuit the noise sources from each side are combined with common mode signals cancelling themselves, and differentially ones adding. The common mode noise sources associated with the current mirror transistors (M5, M6) in figure 4.5, for example, cancel. The noise currents of the NMOS diff. pair transistors (M3, M4), however, show up differentially. The transfer function to the output is given by Z_L, the impedance seen at the output node. Using the noise expression in equation (33), the noise contribution of the NMOS differential pair transistors is given by

$$\overline{v_{on(3,4)}}^2 = \int_0^\infty 4kT\gamma_3 g_m \left| \frac{R_L}{1 + j2\pi f R_L C_L} \right|^2 df \tag{40}$$

where R_L is the effective resistance of the triode load and C_L is the total capacitance at the output, including the input capacitance of the next stage. If the 3-db bandwidth of the RC circuit is denoted

$$f_0 = \frac{1}{2\pi R_L C_L} \tag{41}$$

then the integral in (40) simplifies to

$$\overline{v_{on(3,4)}}^2 = 4kT\gamma_3 g_m R_L^2 \int_0^\infty \left| \frac{1}{1 + f/f_0} \right|^2 df \tag{42}$$

The definite integral in (42) is commonly encountered in noise analysis. As described in [82], its value is just $\pi/2 \cdot f_0$.

Therefore

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3. The noise current i_{n3}, for example divides equally at the common source point since the impedance looking both ways is approximately $1/g_m$. Most of the ac current that flows into M4 shows up at the output node, but with the opposite sign as the other side. The current flowing into M3 cancels half of the current drawn from the drain of M3, resulting in a net current of $+i_{n3}/2$ on one side and $-i_{n3}/2$ on the other.

$$\overline{v_{on(3,4)}}^2 = 4kT\gamma_3 g_m R_L^2 \cdot \left(\frac{\pi}{2} \cdot \frac{1}{2\pi R_L C_L}\right) \tag{43}$$

which simplifies to

$$\overline{v_{on(3,4)}}^2 = \frac{kT}{C_L}\gamma_3 \bullet a_v \tag{44}$$

where a_v is the small-signal gain of the delay stage, $g_m R_L$.

The contribution of the PMOS load transistor noise sources can be determined in a similar way. Using the noise expression from equation (34), we have

$$\overline{v_{on(1,2)}}^2 = \int_0^\infty 4kT\gamma_1 \frac{1}{R_L}\left|\frac{R_L}{1 + j2\pi f R_L C_L}\right|^2 df \tag{45}$$

where $1 / R_L$ is the zero bias drain to source conductance ($g_{ds} = 1/R_L$), and γ_p is the multiplier for device in the triode region of operation. This integral simplifies to

$$\overline{v_{on(1,2)}}^2 = \frac{kT}{C_L}\gamma_1 \tag{46}$$

Combining the results of (44) and (46), the total differential output voltage noise is given by:

$$\overline{v_{on}}^2 = \frac{kT}{C_L}(2\gamma_1 + 2\gamma_3 a_v) \tag{47}$$

The γ_1 term has a value of 1 for a drain-to-source bias of 0v, and approaches 2/3 as the drain-to-source bias is brought towards saturation. An equation for γ_1 as a function of v_{ds} and v_{gs}-v_t is given in [83]. For the differential delay cells considered here, γ_1 , is generally very close to 1. The contribution of the NMOS differential pair transistors is captured by the $2\gamma_3 a_v$ component. As discussed previously γ varies from 2/3 for long channel devices, to as high as 2 or 3 for devices exhibiting short channel effects. The interstage gain term a_v is usually constrained by voltage swing considerations and the requirement that it be greater than 1. Typical values for a_v are in the range of 1.5 to 3.

The important conclusion from equation (47) to consider at this point, however, is simply that the output voltage noise variance is given by the product of kT/C and a term we will call the noise contribution factor, ξ^2.

$$\overline{v_{on}}^2 = \frac{kT}{C_L} \cdot \xi^2 \tag{48}$$

where

$$\xi^2 = 2\gamma_p + 2\gamma a_v \tag{49}$$

The proportionality to kT/C is a situation that arises frequently in noise analyses, such as the case of voltage noise sampled by a noisy resistor onto a capacitor [93], for example. This term is weighted by the relative contributions of the four transistors in the delay cell: two contributions of γ_p each for the PMOS loads, and two contributions of $a_v\gamma$ for the NMOS differential pair transistors. Recall that the tail current source noise contribution is zero for this first pass noise analysis since the differential pair is assumed to be in a balanced state and that noise shows up at the output as a common mode signal. These noise contributions are conveniently summarized by the noise contribution factor term, ξ^2. This term will prove very useful in the second pass, and third pass analyses which follow. What will be shown is that most of the differences which arise from including time varying noise sources, and interstage amplification can be reflected by a change in ξ^2, while the rest of the terms in the relevant equations remain the same.

The next step in the analysis is to use the first crossing approximation to relate the output timing uncertainty at the output of the noisy delay stage to the voltage noise. Using equation (38) we have

$$\overline{\Delta t_d}^2 = \frac{kT}{C_L} \cdot \xi^2 \cdot \left(\frac{C_L}{I_{SS}}\right)^2 \tag{50}$$

or more usefully, using the normalized timing jitter result in (40)

$$\frac{\Delta t_{d\,rms}}{t_d} = \sqrt{\frac{kT}{C_L}} \cdot \xi \cdot \frac{1}{V_{SW}} \tag{51}$$

This equation is the final result of our first pass analysis! It shows, as mentioned before, that the timing error encountered per delay stage normalized to the time delay, is equal to the r.m.s. noise voltage at the output normalized to the output voltage swing V_{SW}. This analysis has shown that for the first pass assumptions in Table 2, this r.m.s. noise voltage is just

$$v_{n\,rms} = \sqrt{\frac{kT}{C_L}} \cdot \xi \tag{52}$$

where ξ (equation (49)) is the noise contribution factor. The practical implications of this for design of low jitter delay cells will be deferred at this point, however, and saved until the second pass and third pass analyses are completed.

4.2.3 Second Pass: Advanced Analysis

The first pass analysis, outlined the basic path from device current noise to output voltage noise to output timing uncertainty in a delay cell. In this pass through the analysis we will add the effects of time-varying noise sources. The assumptions for this case are outlined by the level 2 assumptions in Table 2. One of the key differences is the method for determining the output voltage noise. In the first pass analysis, the power spectral densities were specified for the various noise sources and the output voltage noise was determined by integrating those p.s.d.'s times the transfer function to the output, as in equation (39). In this analysis the autocorrelation functions for the time varying noise sources will be specified and the output voltage noise (which is now a function of time) will be determined by convolving these with the impulse response of the overall system. This was the approach used in [71], and the second pass analysis presented here builds on that work.

Timing waveforms and noise source power spectral densities as a function of time for a typical delay chain are shown in figure 4.9. The noise sources are shown for the first stage. There are three different p.s.d. plots given (i_{na}, i_{nb}, i_{nc}) which will be

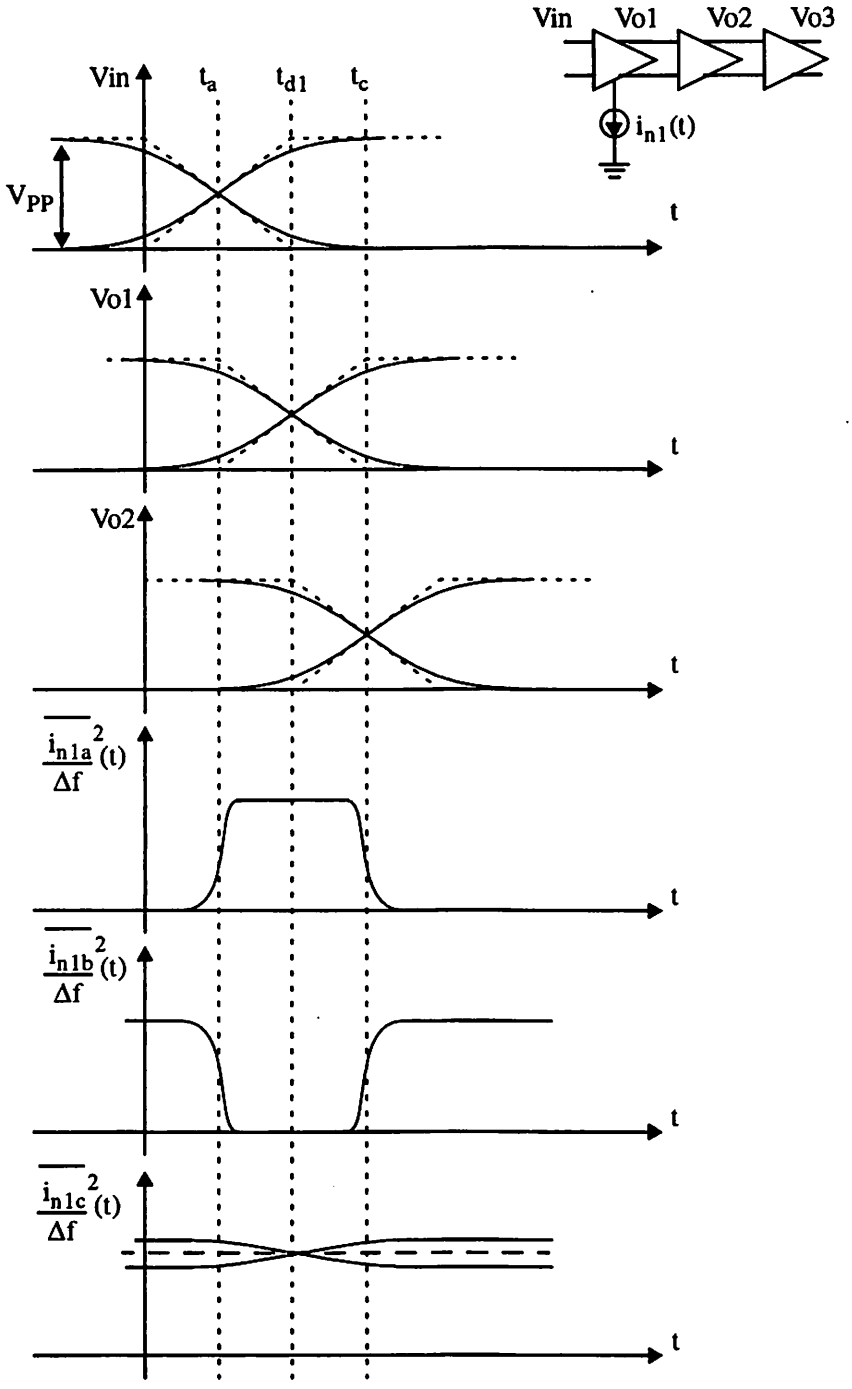


Figure 4.9 Waveforms and noise sources for inverter cell delay chain

shown to apply to the NMOS differential pair transistors, the NMOS tail current source transistors, and the PMOS load transistors, respectively.

The timing waveforms have been drawn with an effective "overlap of two", as before. For this case we show the first stage output beginning to switch strongly when the differential input reaches zero. The input continues to settle for the second half of its ascent while the output of the first stage is proceeding with the first half of its ascent. Likewise, when the output of the first stage reaches a differential voltage of zero, the second stage begins switching strongly, and the pattern repeats. The time "ta" denotes the point at which the differential input to the first stage reaches zero. The time delay for the first stage is measured from this point to the point where its output differential voltage crosses zero as well. In figure 4.9 this time is denoted as "t_{d1}", and occurs at $t = t_a + t_d$. Finally, at time "t_c" the output of the first stage will have finished its switching. With the "overlap of two" used here, this corresponds to a time $t = t_a + 2t_d$.

The noise current sources for the transistors M1-M6 in figure 4.5 were assumed constant in the first pass analysis, with values given by the balanced condition with a differential input voltage of zero (figure 4.5 is repeated for convenience below).

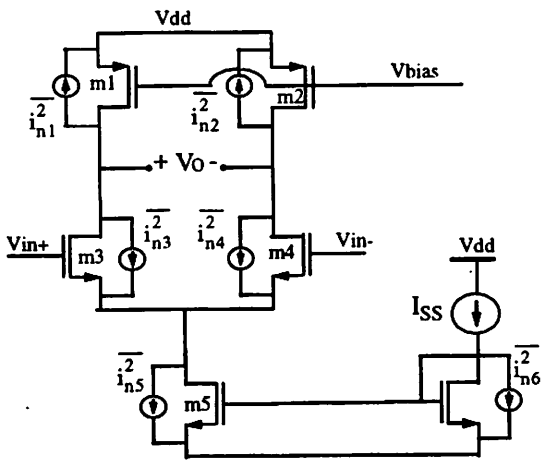


Figure 4.10 Differential delay cell with noise sources (repeat of figure 4.5).

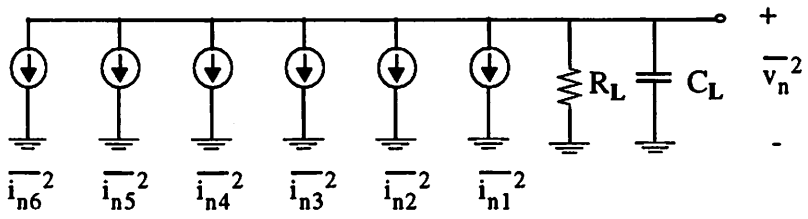
The assumption that the voltage noise variance is the same as its equilibrium value is not valid for the NMOS differential pair transistors, however, since each side switches from fully on to fully off, during which the transconductance, and hence the noise contribution changes dramatically. Furthermore, the tail current noise, although rejected by the circuit when balanced, contributes to the output voltage noise during other parts of the switching transient.

To extend the noise analysis to include these time-varying effects, we break up the noise contributions into two piecewise constant regions of operation. For the time range $t_a < t < t_c$, when the first stage outputs are switching we approximate the noise by its value for the balanced case. The differential pair transistors, for example, are assumed to be have a power spectral density of

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma_3 g_m \tag{53}$$

as before. In the second region, for times $t<t_a$ and $t>t_c$, the differential pair is assumed to be fully switched. In this case the current noise from one side of the differential pair is zero, since the transistor is off. The contribution from the noise current on the other side is found by evaluating its transfer function to the output with a large degeneration resistor (output resistance of M5) at the source (note that the source is not a differential ground in this case). This contribution is typically very small and we approximate it as zero.

In the first pass analysis, an equivalent, small-signal circuit model was used when computing the differential output noise (figure 4.8(c)). In this section a similar model is desired. Rather than use a separate circuit for each region of the timing transient, a single AC circuit is used and the noise sources are assumed to be time varying. In this case, variations in the output referred contribution of a noise source between one region and the next are modeled by a change in the value of the noise source itself. For



Noise Source Approximations

Noise generator	Region I ($t_a < t < t_c$)	Region II ($t < t_a$ or $t > t_c$)
$\overline{i_{n1}}^2, \overline{i_{n2}}^2$	$4kT\gamma_1(1/R_L)\Delta f$	$4kT\gamma_1(1/R_L)\Delta f$
$\overline{i_{n3}}^2, \overline{i_{n4}}^2$	$4kT\gamma_3 g_{m3}\Delta f$	0
$\overline{i_{n5}}^2$	0	$4kT\gamma_5 g_{m5}\Delta f$
$\overline{i_{n6}}^2$	0	$4kT\gamma_5\beta g_{m5}\Delta f$

Figure 4.11 Small-signal equivalent circuit for computing AC differential output voltage noise in inverter delay cell

example, in region II ($t<t_a$ or $t>t_c$) we have said that one side of the differential pair is off, and its noise p.s.d., which is proportional to g_m is equal to zero. The transistor on the other side, however, is fully on but has an output referred contribution of approximately zero. We model this second case as if the noise source for that side were equal to zero in region II as well, thereby allowing us to simply sum the noise source contributions at the output node of a single equivalent circuit as before. The equivalent circuit is shown in figure 4.11, along with the assumptions on the value of the noise sources for both parts of the timing transient.

The assumptions for modeling the noise contribution of the PMOS load transistors (M1,M2) and the current source and biasing transistors (M5.M6) are also included in figure 4.11. The noise generators for the latter had no differential output contribution in the balanced circuit considered in the first pass analysis. This condition is used to approximate their behavior over all of region I and the noise generators are assumed to be zero in this region. When the differential pair is fully switched (region II), however,

the noise of these current generators is directed to one side and a differential output voltage results. In this case, the power spectral densities for the current noise generators of M5 and M6 are modeled as shown in figure 4.11. The contribution of M6 depends on the ratio of the size of the transconductances of M5 and M6 (In practice M6 may be of the same current density but different size). The noise source at M6 actually represents that transistor's thermal noise source plus any other thermal noise in the bias chain that generates the reference current for I_{SS}. We account for the difference with a multiplying factor called β.

The final pair of noise sources to consider are those of the PMOS load transistors. The noise power spectral density for these devices, which are biased in the triode region of operation, was shown previously to be

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma_1 g_{dso} \tag{54}$$

where g_{ds0} is the zero bias drain-to-source conductance and γ is a term which varies from 1 for $V_{DS} = 0$, to 2/3 at the onset of saturation ($V_{DS}=V_{GS}-V_{TP}$). For the usual operating conditions of the differential delay cells considered here, $V_{GS}-V_{TP}$ is made as large as possible (this results in faster delay cells and better resistor linearity). The output swing, V_{SW}, is also kept small with respect to $V_{GS}-V_{TP}$. In this case γ does not vary too dramatically over the course of the output transient and can be approximated as constant. Therefore we use the same p.s.d. for the PMOS load transistors in both regions of the transient, as shown in figure 4.11, where the output resistance, R_L, is very close to $1/g_{ds0}$ and the value of γ_1 is the average value of γ over the transient, very close to one.

The assumptions for the contributions of the differential pair, current source, and load transistors in the balanced and unbalanced region of operation are summarized by the p.s.d. curves for $\overline{i_{na}^2}$ and $\overline{i_{nb}^2}$ and $\overline{i_{nc}^2}$ in figure 4.9. The output noise voltage resulting from these will vary in time since the noise current sources themselves do. To

find the output voltage noise we use autocorrelation functions for each of the noise processes and use the following relationship:

$$R_{vv}(t_1, t_2) = R_{ii}(t_1, t_2) \otimes h(t_1) \otimes h(t_2) \tag{55}$$

This equation shows that the output voltage noise autocorrelation function equals the autocorrelation function for a given noise source convolved with the impulse response seen by the noise source when referred to the output. Summing the results of (55), for each of the noise sources, gives us an equation similar to (40) for the constant noise source case. This convolution can be written as:

$$R_{vv}(t_1, t_2) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h(\tau_1)h(\tau_2)R_{ii}(t_1-\tau_1, t_2-\tau_2)d\tau_2 d\tau_1 \tag{56}$$

Recall that the autocorrelation function for a random variable is expected value of the product of the random variable at one time instant times its value at another:

$$R_{vv}(t_1, t_2) = E\{V(t_1)V(t_2)\} \tag{57}$$

For wide-sense-stationary noise processes [94] the actual times, t_1 and t_2, are not important, just their difference $\tau=t_1-t_2$. In that case the autocorrelation function can be expressed as

$$R_{vv}(\tau) = E\{V(t_1)V(t_1+\tau)\} \tag{58}$$

However, the time varying noise sources considered here are not wide-sense-stationary (with the exception of the PMOS noise source which is assumed constant) and we will have to resort to using equation (57) in general. Once the autocorrelation function of the output noise is found, the voltage noise variance as a function of time can be found by evaluating

$$\overline{v_n}^2(t_1) = R_{vv}(t_1, t_1) = E\{V^2(t_1)\} \tag{59}$$

In the first pass analysis, with constant noise sources, the transfer function for a noise current source referred to the output was

$$H(j\omega) = Z_L(j\omega) = \frac{R_L}{1 + j\omega R_L C_L} \tag{60}$$

where R_L is the effective triode load resistance, $1/g_{ds}$, and C_L is the total load capacitance at the output, consisting largely of the input capacitance seen looking into the next stage. This is just the impedance seen at the output node- a resistor in parallel with the output capacitance. The impulse response for such a system is given by the inverse fourier transform of (60), or

$$h(t) = \frac{1}{C_L} e^{\frac{-t}{R_L C_L}} u(t) \tag{61}$$

Along with the impulse response, we need an expression for the autocorrelation of the current noise process. For the constant noise sources considered previously, the autocorrelation function can easily be found as the inverse fourier transform of the noise power spectral density. Since the inverse fourier transform of a constant is just a delta function centered at zero, a white noise source with a p.s.d. as in (53), would have an autocorrelation function of

$$R_{ii}(\tau) = 2kT\gamma g_m \delta(\tau) \tag{62}$$

which is an impulse centered at $\tau = 0$. The area of the impulse is proportional to 2kT rather than 4kT, which might be expected from (53), because we need to consider the double-sided power spectral density when finding the autocorrelation function. More details on this issue are presented in appendix A. This represents a correction by a factor of two compared to work in [71].

For the time-varying noise sources considered here the autocorrelation function depends on the times of interest t_1 and t_2, and not just their difference τ. For the NMOS

differential pair transistors, for example, the autocorrelation function is

$$R_{ii}(t_1, t_2) = \begin{cases} 0 & \text{for } t_1 \text{ or } t_2 \le t_a \\ 2kT\gamma g_m \delta(t_1 - t_2) & \text{for } t_a \le t_1, t_2 \le t_c \\ 0 & \text{for } t_1 \text{ or } t_2 \ge t_c \end{cases} \tag{63}$$

The times t_a and t_c are the turn-on and turn-off times for the noise source (figure 4.9). Substituting (63) into the convolution in (56), we have

$$R_{vv}(t_1, t_2) = \int_{t_1 - t_c}^{t_1 - t_a} h(\tau_1) \int_{t_2 - t_c}^{t_2 - t_a} h(\tau_2) 2kT\gamma g_m \delta[(t_1 - \tau_1) - (t_2 - \tau_2)] d\tau_2 d\tau_1 \tag{64}$$

where the limits of integration come from

$$\left.\begin{aligned} t_a \le t_1 - \tau_1 \le t_c \\ t_a \le t_2 - \tau_2 \le t_c \end{aligned}\right\} \Rightarrow \begin{cases} t_1 - t_c \le \tau_1 \le t_1 - t_a \\ t_2 - t_c \le \tau_2 \le t_2 - t_a \end{cases} \tag{65}$$

To simplify the math which follows, a time origin of $t_a = 0$ will be assumed: that is, the time at which the first diff pair begins strongly switching will be considered time zero.

If the impulse response in (61) is substituted into (64) and the evaluation carried out, then a final expression for the autocorrelation function of the output voltage noise is attained. The details of this derivation are presented in appendix A, where careful attention is paid to limits of integration, and various special cases. For a good understanding of this noise analysis and its conclusions, the details of appendix A are recommended. (Similarly, appendix B will cover the math for the third pass analysis which follows.)

The final result of the autocorrelation function noise analysis is what is of interest here, however. For the NMOS differential pair transistor contribution, the result is the autocorrelation function in (66).

$$R_{vv}(t_1, t_2) = \frac{kT\gamma g_m R_L}{C_L}\left(e^{\frac{-1}{R_L C_L}|t_2 - t_1|}\right)\left[1 - e^{\frac{-2}{R_L C_L}t}\right] \tag{66}$$

This expression shows that the correlation in the noise at two different instances in time decreases exponentially with the magnitude of their separation, $|t_1 - t_2|$. The last term in this expression gives it an envelope which rises exponentially towards a constant. The variable t in that term is taken to be the lesser of t_1 and t_2. Also assumed in equation (66) are limits on t_1 and t_2 similar to those in (63) (see appendix A).

Of primary concern, however, is not the autocorrelation function in (66) itself, but its value at $t = t_1 = t_2$. As described previously, the voltage noise variance as a function of time is given by

$$\overline{v_n}^2(t) = R_{vv}(t, t) \tag{67}$$

Therefore,

$$\overline{v_n}^2(t) = \frac{kT\gamma a_v}{C_L}\left[1 - e^{\frac{-2}{R_L C_L}t}\right] \tag{68}$$

where $a_v = g_m R_L$ is the small signal gain per stage. This is the result we have been after. It says that for a thermal noise current source which turns on at time zero, the output voltage noise rises exponentially towards the constant predicted in the first pass analysis (equation (44)). A plot of the voltage variance versus time is shown in figure 4.12. It rises with a time constant of $2/R_L C_L$, which can be shown, incidentally, to be related to the time delay per stage. In fact, noting that $R_L = V_{SW}/I_{SS}$ for the inverter delay cells of interest here, the time constant in (68) is just $\tau = t_d/2$.

The envelope shaping term in equation (68) is an important factor and will be

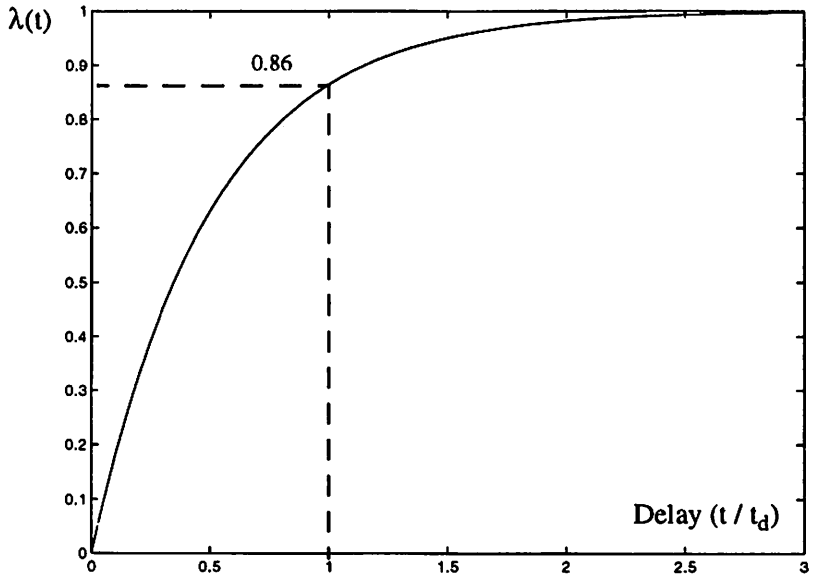


Figure 4.12 Output voltage noise envelope

referred to as the noise evolution factor.

$$\lambda(t) = \left[1 - e^{\frac{-2}{R_L C_L} t}\right] = \left[1 - e^{-2\left(\frac{t}{t_d}\right)}\right] \tag{69}$$

Therefore, the output noise for an inverter can be thought of in terms of its final value, times the noise evolution factor which captures its dependence on time.

$$\overline{v_n}^2(t) = \frac{kT}{C_L} \cdot \gamma_3 a_v \cdot \lambda(t) \tag{70}$$

This is the result for the NMOS differential pair transistors in the inverter delay cell, and is analogous to the result in (44). The total output noise, however, is also comprised of the contributions of the PMOS load transistors, the noise in the tail current source, and biasing noise. The analysis for these sources is very similar to the one just considered and is described in more detail in appendix A. For the PMOS loads, which were assumed to contribute a constant noise level,

$$\overline{v_n}^2(t) = \frac{kT}{C_L} \cdot \gamma_1 \tag{71}$$

which is the same result as in the constant noise analysis case (equation (46)).

The tail current noise source, which passes directly to the output in the unbalanced case and is assumed to show up as a common mode signal during the switching transient has a contribution of

$$\overline{v_n}^2(t) = \frac{kT}{C_L} \cdot \gamma_5 a_v \cdot \sqrt{2\alpha} \cdot \lambda_b(t) \tag{72}$$

where the $\sqrt{2\alpha}$ term accounts for the difference in the transconductance of M5 and M3(M4). If the devices used are the same size (W/L) then the difference in their transconductances is just $\sqrt{2}$, due to the higher current in M5. Alpha is just the ratio of the size of M5 to M3. Also included in (72) is a new noise evolution factor, $\lambda_b(t)$. This term is expected to contribute its full output voltage at time zero, and then decay towards zero over time. Not surprisingly the noise evolution factor is just a decaying exponential

$$\lambda_b(t) = e^{\frac{-2}{R_L C_L} t} = e^{-2\left(\frac{t}{t_d}\right)} \tag{73}$$

As mentioned before, the relative contribution of M6, and other biasing noise showing up through it, is covered by a multiplying factor of β, capturing the level of the noise power relative to that in M5.

$$\overline{v_n}^2(t) = \frac{kT}{C_L} \cdot \gamma_5 a_v \cdot \beta\sqrt{2\alpha} \cdot \lambda_b(t) \tag{74}$$

If the values of each of the noise sources contributing to the output are combined, then the total output voltage noise can be expressed by

$$\overline{v_n}^2(t) = \frac{kT}{C_L} \cdot \xi^2 \tag{75}$$

where ξ^2 is the new noise contribution factor

$$\xi^2 = 2\gamma_1 + 2\gamma_3 a_v \cdot \lambda_a(t) + \gamma_5 a_v \sqrt{2\alpha}(1+\beta) \cdot \lambda_b(t) \tag{76}$$

This is the same form in which the noise was expressed for the first pass analysis in equation (48). The noise contribution factor there was somewhat simpler and given by

$$\xi^2 = 2\gamma_1 + 2\gamma_3 a_v \tag{77}$$

This term captured the contribution of each of the two output load transistors and each of the differential pair transistors. The new noise contribution factor, derived in this analysis, just extends this term to include the effects of time varying noise sources. Since the PMOS noise is constant, its contribution does not change. The NMOS differential pair transistors have the same contribution, but weighted by the noise evolution factor $\lambda_a(t)$. And finally, the tail current noise, which had no impact for the balanced case considered in the first pass, shows up now, weighted by its noise evolution factor $\lambda_b(t)$.

The result in (75) and (76) is the final point in this second pass analysis. The implications of this voltage noise for timing jitter could be considered, as they were briefly in the first pass case, but those conclusions will be saved until the effects of interstage amplification are added in the next section. The normalized r.m.s. timing jitter predicted here, is the same as in the first pass analysis, with the new noise contribution factor, ξ, substituted into equation (51) instead of the previous one.

An interesting question worth considering now, however, is how large are $\lambda_a(t)$ and $\lambda_b(t)$ at the time of interest. Equation (73) showed that the time constant for noise evolution factor is related to the time delay of the stages themselves. For the first crossing approximation, considered previously, the output timing jitter is proportional to the voltage noise at the nominal time of threshold crossing, $t=t_d$. In this case $\lambda_a(t_d)$ is just the constant $(1-e^{-2})$ which equals 0.86. And $\lambda_b(t_d)$ is simply $e^{-2} = 0.14$. So, the contribution of the NMOS differential pair noise sources to the output voltage noise variance has reached 86% of its final value at the critical time of interest. And similarly, the

noise contributions of the current source transistors have decayed to 14% of the value they held in the unbalanced case[4].

4.2.4 Third Pass: Complete Analysis

In the previous two sections, the basic path from device thermal noise to timing jitter has been completed, and then extended to include the effects of time-varying noise sources. With these results in place, it is now relatively straightforward to extend the analysis again to include the important additional effect of inter-stage amplification, and to re-evaluate and clear up some of the confusion surrounding the "first-crossing" approximation used previously. This is our third and final pass through the analysis, and the assumptions for it are outlined in Table 2.

Another look at the timing waveforms in figure 4.13, below, shows that for a typical CMOS inverter chain the switching times of adjacent stages overlap and there are times when more than one stage is in the active region of amplification. In this case it is not sufficient to consider the noise contribution of a single inverter alone since noise from one inverter may be amplified and filtered by the next stage, contributing to the jitter in the subsequent stages in that manner. A better model is to consider two successive stages, and determine the voltage noise at the output of the second stage directly from the thermal noise current sources in the first.

Included in figure 4.13, along with the voltage waveforms and noise sources is a plot of the transconductance of the differential pair in the second stage inverter delay cell versus time. The transconductance of a differential pair, Gm, is the ratio of the small signal differential output current to the small signal differential input voltage for a given bias condition. For a MOS differential pair, a DC input voltage of

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4. The factor of 1/2 in the time constant for the noise evolution factor may seem like a cause for concern at first. The multiplying constant in the exponential expressions in (69) and (73) is -2/RC, twice the usual value for settling in a first order RC circuit. This is consistent with the fact that we are considering voltages noise variances, however. The r.m.s. noise voltage at the output for a given noise source would go as the square root of the variance, and would settle proportional to exp(-t/RC), as expected.

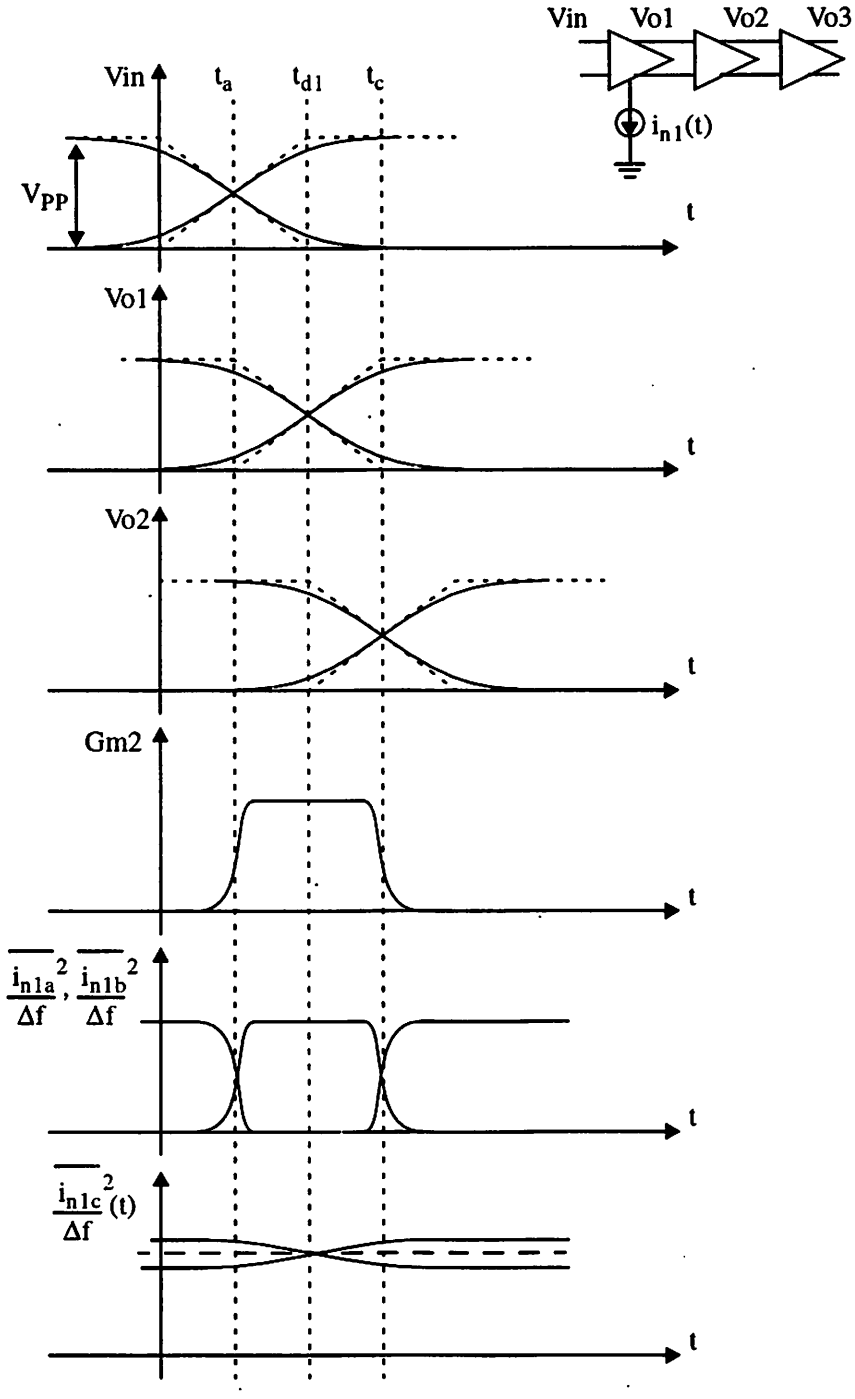

Figure 4.13 Signal and noise source waveforms with delay cell transconductance

$\sqrt{2}(V_{GS} - V_T)$ is enough to turn one side completely off, at which point the DC transfer characteristic is said to be saturated [82]. For the part of the transient where the differential input voltage has magnitude less than this, the differential pair is said to be in its active region of amplification. During this time a small signal input voltage will produce a differential output current, given by

$$i_n(t) = G_m v_n(t) \tag{78}$$

For the second inverter delay cell in figure 4.13, its input voltage (the output voltage from stage one), places it in the active region of amplification for $t_a < t < t_c$. This is the same region over which the noise sources of the first stage are considered on and are modeled by their value in the balanced condition[5]. We approximate the transconductance of the second stage as a constant over this interval, with value equal to its value for the balanced condition. In this case, the differential G_m is just equal to small signal transconductance g_m of the devices that make up the differential pair.

For times outside of the region $t_a < t < t_c$, the transconductance of the differential pair in the second stage is approximately zero, and a noise voltage signal at the input will have no effect on the output of the next stage. At first glance, one might expect the behavior of noise in the inverter chain to be similar to the behavior one would expect for a chain of amplifiers with a small signal, noisy input. In that case, the voltage noise variance at the output of the second stage would just be a_v^2 times the noise computed at the output of the first. But this is not the situation encountered for signals propagating through a delay chain.

Consider again the evolution of the timing waveforms in figure 4.13. As the outputs of the first inverter are switching, they create a change in the differential input

5. Note that the transconductance of the differential pair, G_m, is considered non-zero for times when changes in its differential input voltage can create a change in its output current. For a given delay cell, this is different than the region over which its noise sources, some of them proportional to the device small signal transconductance g_m, are approximated by their value in the balanced case.

voltage to the second inverter, which change that stage's differential output current. The changing output current begins to change the state of the second stage output voltages. The integral of this time-varying current shapes the voltage waveforms which "evolve" at the output of the next stage. For times t>tc, the differential inputs to the second stage have fully switched and the second stage differential pair is "saturated". In this case, changes in the input voltage will have no further effect on the differential current shaping the voltage waveforms at that stages output. But for times in the range $t_a < t < t_c$, a change in the differential input voltage creates a change in the differential output current, effecting the voltage waveform at the output in that manner. This effect can be modeled by the second order circuit in figure 4.14.

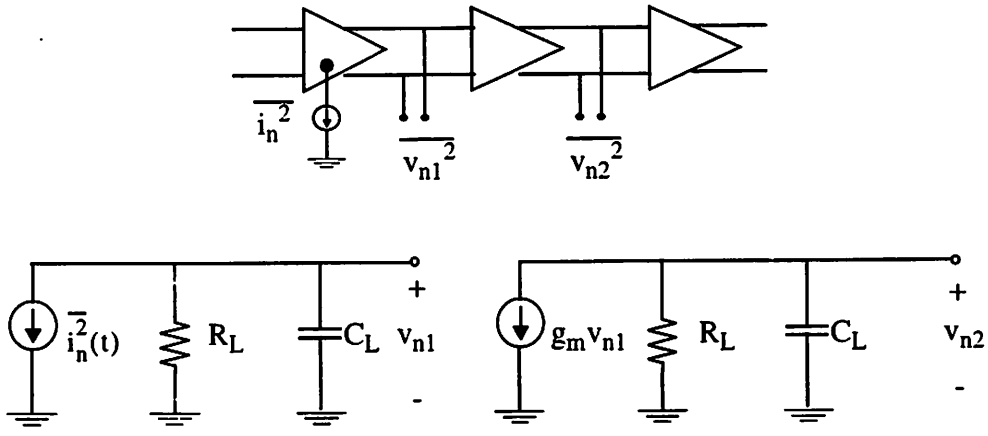

Figure 4.14 Extended circuit model for inter-stage interaction

In this model, the voltage noise at the output of the first stage creates a small signal current noise at the input of the second through the transconductance, g_m. This current noise is accumulated and filtered to create the output noise voltage, v_{n2} at the output of the second stage. Of course, the device noise sources for the second stage transistors need to be considered as well, but in this case we are just determining the timing jitter impact of the noise sources in the first stage, by looking at their impact on the output of the next stage. Provided that the first and second stage noise sources are

independent, the effects of each on the jitter variance can be added, and it is acceptable to consider them each individually. To determine the jitter contribution of noise sources in the second stage, the same approach is taken and their impact is measured at the output of the third stage, and so forth.

Since the noise sources in the first stages are considered time-varying, as they were in the second pass analysis, autocorrelation functions are employed again. The contribution of the NMOS differential pair transistors, for example is computed by

$$R_{vv}(t_1, t_2) = R_{ii}(t_1, t_2) \otimes h'(t_1) \otimes h'(t_2) \tag{79}$$

where $R_{ii}(t_1,t_2)$ is given by

$$R_{ii}(t_1, t_2) = \begin{cases} 0 & \text{for } t_1 \text{ or } t_2 \le t_a \\ 2kT\gamma g_m \delta(t_1 - t_2) & \text{for } t_a \le t_1, t_2 \le t_c \\ 0 & \text{for } t_1 \text{ or } t_2 \ge t_c \end{cases} \tag{80}$$

as before, and h'(t) is the combined impulse response of the second-order circuit in 4.14. In appendix B this filter's impulse response is shown to be

$$h'(t) = \frac{g_m}{C_L^2} \cdot t \cdot e^{\frac{-t}{R_L C_L}} u(t) \tag{81}$$

Solving for (79), once again requires evaluating the expression

$$R_{vv}(t_1, t_2) = \int_{t_1 - t_c}^{t_1 - t_a} h(\tau_1) \int_{t_2 - t_c}^{t_2 - t_a} h(\tau_2) 2kT\gamma g_m \delta[(t_1 - \tau_1) - (t_2 - \tau_2)] d\tau_2 d\tau_1 \tag{82}$$

As before, the details of the mathematical solution for (82) are saved for an appendix. For a complete look at that analysis, including further assumptions, special cases, and determination of evaluation limits, appendix B is recommended. The integrals to be evaluated here are even more complicated than in the previous section. However, a thorough analysis yields results that are very intuitive.

The contribution of the NMOS differential pair transistors, has the autocorrelation function given in (83) (compare with second pass analysis eq. (66)).

$$R_{vv}(t_1, t_2) = B\left((t_2 - t_1) + \frac{1}{a}\right)[1 - e^{-2at_1} - 2at_1 e^{-2at_1}] - B2at_1^2 e^{-2at_1} \tag{83}$$

where

$$B = \left(\frac{kT\gamma g_{m3} a_v^2}{2}\right) e^{-a(t_2 - t_1)} \tag{84}$$

and the constant a is

$$a = \frac{1}{R_L C_L} \tag{85}$$

resulting in the same time constant as before. Once again a time origin of t_a=0 has been assumed.

The voltage noise variance versus time is found by evaluating the autocorrelation function for $t=t_1=t_2$. This results in

$$\overline{v_n}^2(t) = R_{vv}(t, t) = \frac{kT}{C_L} \cdot \gamma a_v \cdot \frac{a_v^2}{2} \cdot \lambda_{a2}(t) \tag{86}$$

where $\lambda_2(t)$ is the new noise evolution factor for our second order system.

$$\lambda_{a2}(t_1) = \left[1 - [1 + 2at_1 + 2a^2 t_1^2] e^{-2at_1}\right] \tag{87}$$

So the noise contribution of the NMOS differential pair has a very similar form to before (equations (68), (70)). The only differences are an additional multiplicative factor of $a_v^2/2$ and a new noise evolution factor, $\lambda_2(t)$, capturing a more complicated envelope with respect to time. This is a very intuitive result! In the second pass analysis the noise variance at the output of the first stage rose exponentially, when the noise source was turned on, towards its value for the balanced, constant noise case. The result here shows that the noise variance at the output of the next stage also rises towards a constant level. This level is just the noise variance at the input of the second stage times

its noise power gain, $a_v^2/2$.[6]

The noise evolution factor, $\lambda_{a2}(t)$, is more complicated than before and is plotted in figure 4.15. The noise envelope in this case starts more slowly before growing expo-

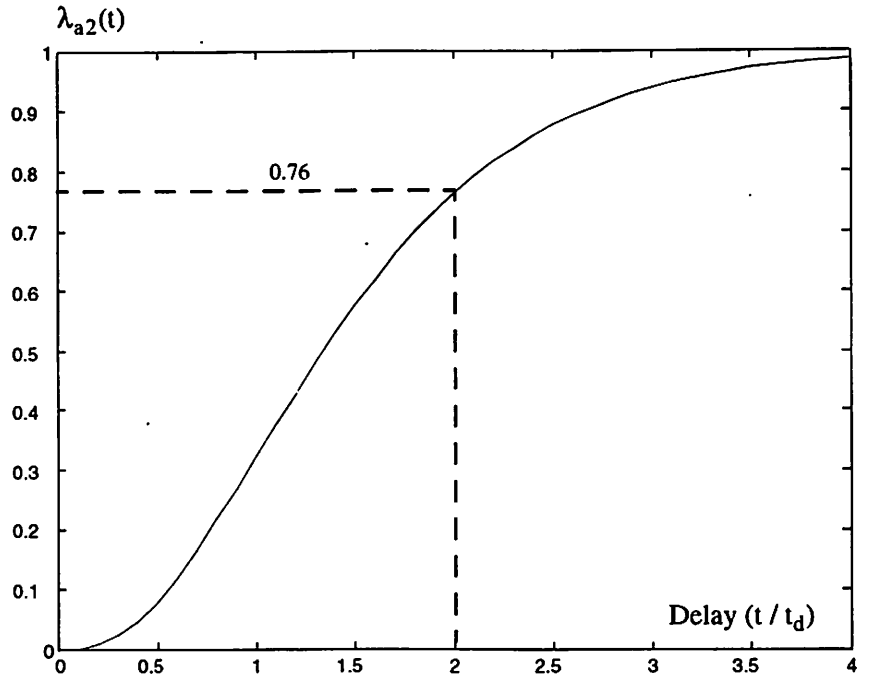

Figure 4.15 Noise evolution factor for second order system

nentially towards one. A useful comparison of the second pass and third pass analysis results is given by the graphs in figure 4.16. In this example, the relative level of noise at the output is compared for the case of inter-stage gains of both a_v=1.8 and 2.3 in the second stage. Here, it is evident that the output voltage noise rises to a significantly higher level than determined before. In the second pass analysis the noise at the output of the first stage at time $t=t_d$ was considered to determine the timing jitter imparted to future stages through the first crossing approximation. In this analysis, it is the noise at the output of the second stage, due to the noise sources in the first stage that has been

6. The squaring of a_v is due to the fact that we are considering voltage noise variance. The r.m.s. noise voltage is proportional to a_v.

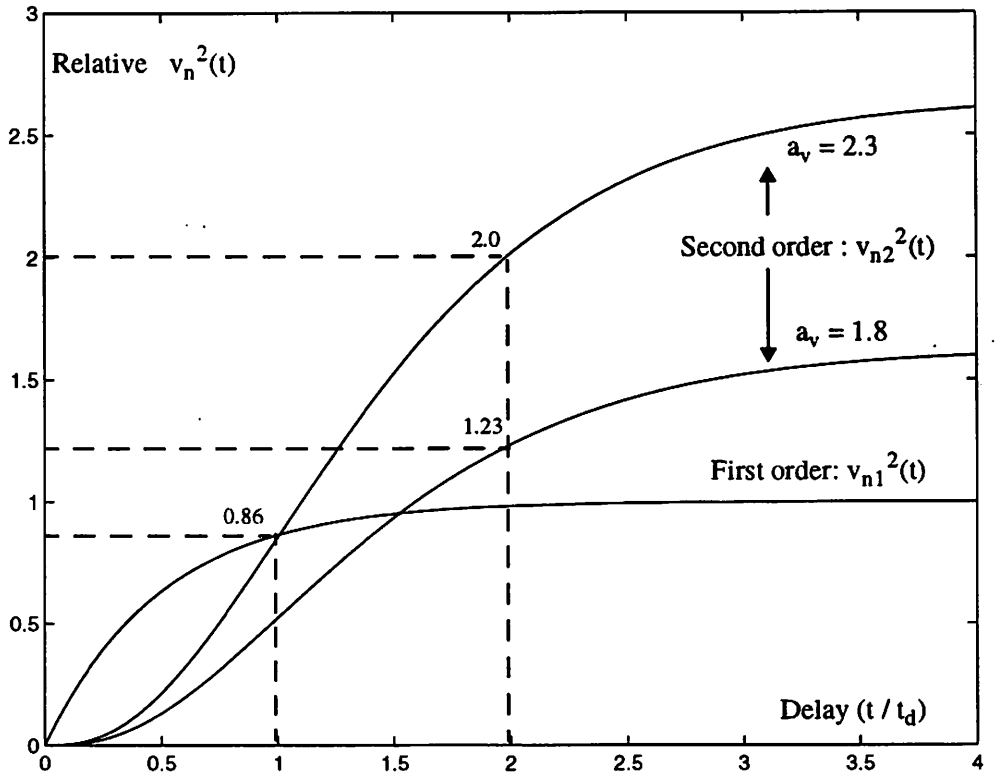

Figure 4.16 Voltage noise variance comparison with interstate gain of a_v=1.6

determined. This noise imparts timing jitter to future stages by its influence on the time when the third stage begins switching. So the voltage noise at time $t=2t_d$, the nominal time at which the third stage's differential input reaches zero, determines the resulting timing jitter. In this case, the noise has risen to a higher level than predicted by the previous analysis. With a gain of 1.8 it has risen to a value of 1.23, compared to the level of 0.86 considered previously. With a gain of 2.3 it has risen to a level of 2.0 - more than twice as high as predicted in the previous analysis.

More scrutiny will be given to the validity of the first crossing approximation shortly. It turns out that by considering the noise two stage into the future, as we have, the timing jitter problem maps more naturally into the form of the first crossing approximation without the need to resort to the "ideal buffer" assumption used in previous

work! Before examining this, however, the total output noise will be summarized with all of the noise sources contributing to the output.

The derivations of the effects of the other noise sources are covered in detail in appendix B. Noise sources in the PMOS loads have the same contribution as before since they are assumed to be approximately constant. The NMOS current source and biasing transistor noise contribution also takes the same form as before, except for a new noise evolution factor

$$\lambda_{b2}(t) = [1 + 2at + 2a^2t^2]e^{-2at} \tag{88}$$

If all of these terms are combined, then the noise can be expressed in a similar form as for the second pass analysis, with the addition of the factor of $a_v^2/2$.

$$\overline{v_n}^2(t) = \frac{kT}{C_L} \cdot \frac{a_v^2}{2} \cdot \xi^2 \tag{89}$$

where ξ^2 is the new noise contribution factor

$$\xi^2 = 2\gamma_1 + 2\gamma_3 a_v \cdot \lambda_{a2}(2t_d) + \gamma_5 a_v \sqrt{2\alpha}(1+\beta) \cdot \lambda_{b2}(2t_d) \tag{90}$$

The noise contribution factor is essentially the same as before, except that the noise evolution factors, $\lambda_{a2}(t)$ and $\lambda_{b2}(t)$, have changed. The trailing subscript of 2 is used to denote that these are the evolution factors for the output of a second-order system.

The link from voltage noise to timing jitter has been established previously using the "first-crossing" approximation. In figure 4.7 a voltage error of size Δv was shown to produce a timing error Δt, where Δt equaled Δv divided by the slope of line, or slew-rate. In this case, the timing jitter variance was given by

$$\overline{\Delta t_d}^2 = \overline{\Delta v_n}^2 \cdot \left(\frac{C_L}{I_{SS}}\right)^2 \tag{91}$$

The troubling aspect of this approximation is that it says that the timing uncertainty imparted to future stages depends solely on the value of the noise at one time instant, the nominal time of threshold crossing. We would expect, however, that the value of the noise throughout the switching transient would be relevant, especially times just after and just before the threshold crossing. In this sense the ideal buffer assumption shown back in figure 4.7, seems inadequate.

Fortunately, much of this confusion is removed with the assumptions made in this section. Consider the signal and noise source waveforms in figure 4.13 again. We have been considering the impact of the thermal noise current sources of the first stage, on the output of the second stage. The time when the second stage reaches a differential output voltage of zero is $t=t_c$. This is also the time at which the second stage's inputs have fully switched and its G_m has dropped to zero. This means that the noise sources in the first stage can have no further effect on the output of the second stage from t_c on. Therefore the value of the noise just after the nominal time of threshold crossing is not important since there is no additional noise from the first stage. From this point on the outputs are just settling to their final state, offset it time by the same amount they were at their midpoint, when their differential voltage equaled zero.

This resolves the issue of noise just after the nominal time of threshold crossing. What about the noise just before? Here, we also benefit from considering the noise at the output of the next stage. As described previously, the noise voltage which arises at the output of the first stage is not directly amplified to the output of the second, but instead serves to change the next stages differential output current, through G_m, changing the evolution of the voltage waveforms at the output and effecting future stages in that manner. The deviation from the noiseless waveform transition is a filtered and averaged version of the first stage current noise. Therefore the value of this deviation at the nominal time of threshold crossing is closely related to its values just before.

Using the relationship in equation (91) the timing jitter variance per delay stage is found to be

$$\overline{\Delta t_d^{\,2}} = \frac{kT}{C_L} \cdot \xi^2 \cdot \frac{a_v^2}{2} \cdot \left(\frac{C_L}{I_{SS}}\right)^2 \tag{92}$$

As expected, this is almost the same expression as before, with the additional factor of $a_v^2/2$ added and a new noise contribution factor. Back in section 4.2.1, a useful ratio was defined which was called the normalized timing jitter (equation (38)). This expression is found by normalizing the result in (92) to $t_d^{\,2}$.

$$\frac{\overline{\Delta t_d^{\,2}}}{t_d^{\,2}} = \frac{kT}{C_L} \cdot \xi^2 \cdot \frac{a_v^2}{2} \cdot \left(\frac{C_L}{I_{SS}}\right)^2 \left(\frac{I_{SS}}{C_L V_{SW}}\right)^2 \tag{93}$$

or

$$\frac{\Delta t_{d\,rms}}{t_d} = \sqrt{\frac{kT}{2C_L}} \cdot \xi \cdot a_v \cdot V_{SW} \tag{94}$$

This can be simplified further however. The small signal inverter gain a_v, is equal to the product $g_m R_L$. But these two terms can both be expressed in terms of other delay cell design parameters. The transconductance of the differential pair devices can be expressed as

$$g_m \equiv \frac{2(I_{SS}/2)}{(V_{GS} - V_T)} \tag{95}$$

and the load resistance of the PMOS triode device is approximately

$$R_L \equiv \frac{V_{SW}}{I_{SS}} \tag{96}$$

This means that the gain can be expressed as the ratio of the output swing, V_{SW} to the gate bias voltage above threshold for the balanced state, $(V_{GS}-V_T)$.

$$a_v = g_m R_L \equiv \frac{V_{SW}}{(V_{GS} - V_T)} \tag{97}$$

With this result, equation (94) simplifies to

$$\frac{\Delta t_{d\,rms}}{t_d} \cong \sqrt{\frac{kT}{2C_L}} \cdot \frac{1}{(V_{GS}-V_T)} \cdot \xi \tag{98}$$

This is the final result of the third pass analysis! It shows that the normalized timing error is related to the square root of kT/C as before (equation (51)), and to the noise contribution factor, ξ. And whereas before it was inversely proportional to the voltage swing, V_{SW}, with the effects of interstage gain included, it is now inversely proportional to the gate bias voltage above threshold for the differential pair transistors, $(V_{GS}-V_T)$. This equation links timing jitter in delay cells to basic delay cell design parameters. It holds the information needed to explore the trade-offs involved in low-jitter design.

4.3 Implications for Low-Jitter Delay Cell Design

Earlier in the chapter, it was shown that with the first crossing approximation, the link from voltage noise to timing jitter in the class of inverter cells considered here (source-couple devices with triode, resistive loads) could be expressed as

$$\frac{\Delta t_{d\,rms}}{t_d} = \frac{\Delta v_{n\,rms}}{V_{SW}} \tag{99}$$

That is, the ratio of the timing error encountered per stage for signals propagating in an inverter delay chain to the time delay per stage, is equal to the ratio of the r.m.s. voltage noise at the output of a stage, to the output voltage swing. Over the course of the analysis which followed, successively better approximations for $\Delta v_{n\,rms}$ have been derived, culminating with the result of the third pass analysis in equation (89). This result, in turn, gave rise to our final result of

$$\frac{\Delta t_{d\,rms}}{t_d} \cong \sqrt{\frac{kT}{2C_L}} \cdot \frac{1}{(V_{GS}-V_T)} \cdot \xi \tag{100}$$

Now, the question of the practical implications of this equation for inverter delay cell device design is addressed.

When designing a ring-oscillator or a voltage-controlled delay chain, there are a number of levels at which a design can be optimized. In fact, many of the trade-offs concerning low-jitter - and later, low phase-noise - designs are evident at a level above the basic delay cell, when the jitter and the delay of several stages are combined. These matters will be addressed shortly and are the focus of the next chapter. At this point, however, some of the basic implications of equation (100) are considered.

Equation (100) shows that in the final analysis, the normalized timing error is equal to the ratio of a noise level, related to $\sqrt{kT/C}$ as before, and the $V_{GS} - V_T$ bias point of the differential pair transistors in the inverter delay cell. The noise contribution factor, ξ, from equation (90) is relatively insensitive to changes in delay-cell design parameters.

As a starting point, consider the trade-offs involved in choosing V_{GS}-V_T. This bias point is largely constrained by the choices of voltage swing and inter-stage gain. The small signal gain of an inverter cell was shown in equation (97) to equal the ratio of V_{SW} / V_{GS}-V_T. Since the voltage swing attainable at the output of the inverter cells is limited by the supply voltage and by other biasing constraints in the delay cell, its value does not change appreciably for various designs. It is generally made as large as possible. For the delay cells considered in chapter 6, with a 3V power supply, a swing of 1V was chosen. The V_{GS}-V_T bias point for the inverter cells is chosen as large as possible, to reduce jitter, but needs to be small enough to guarantee a gain greater than one. This is required so that the signals propagating through delay chains are not attenuated in passage. And for a ring-oscillator a gain of greater than one is required for oscillation. In practice an even higher gain is required and, with a safety margin to guard over process variations, would typically be as high as 1.7. Therefore, the V_{GS}-V_T bias point for

the delay cells is chosen to be as large as possible, but is constrained by voltage swing and gain considerations. For the 1V swing and gain of 1.7 considered here, this translates to a maximum V_{GS}-V_T of around 600mV.

The next consideration for minimizing delay cell jitter is to reduce the contribution of the $\sqrt{kT/C_L}$ term, by increasing the load capacitance at the output of each stage. This capacitance consists of several components including the input capacitance looking into the next stage which is proportional to the product of the gate width, gate length and oxide capacitance per unit area, WLC_{OX}. More details on this capacitance are provided in chapter 6. An important conclusion, however, is that most of its components scale to first order with the gate width of the input devices for the inverter cell. To make a useful comparison of the jitter in delay cells with different values of C_L, the ratio in equation (100) should be computed for delay cells with the same time delay per stage. The delay per stage is

$$t_d = \frac{C_L V_{SW}}{I_{SS}} \tag{101}$$

A consistent comparison can be facilitated in the following way. The load capacitance is proportional to the gate width of the input devices, and the current for a given (V_{GS}-V_T) bias point is proportional to the gate width as well. Therefore, by scaling the input device gate width, W, and scaling the tail current, I_{SS}, per stage a constant delay is maintained as well as a constant (V_{GS}-V_T). In this scenario, the only factor in equation (100) which changes is the term C_L. The gain per stage is also assumed to be held constant and the triode loads are assumed to be scaled likewise so that their (V_{GS}-V_T) remains the same. This means that for a doubling of the current, the resistance of the triode loads is halved, so that the voltage swing remains the same at the output.

In this case, C_L is increased and the normalized timing jitter will improve with the square root of the scaling factor. Therefore normalized timing jitter can be improved freely through changes in C_L, but at the cost of power consumption and circuit area.

The power increases proportionally since the class of delay cells considered draw a static current of magnitude I_{SS} from the power supply. And the circuit area increases, since increases in C_L were accompanied by proportional increases for all of the transistors in the inverter delay cell.

It is also possible to increase the load capacitance at the output of an inverter delay cell through other means - adding an extra circuit capacitance in parallel, for instance - which do not imply proportional changes in current and area. In these cases, the delay per stage also changes, and the implications for low-jitter design need to be considered at a higher level, taking into account the overall structure being designed. In a ring-oscillator, for example, adding extra capacitance at the output of each stage in this manner would change the overall period of the oscillator. To attain the same period, fewer stages could be used, which in turn would lower the total jitter in the overall ring-oscillator even further. Considerations such as these are the topic of the next chapter!

The last term in equation (100), the noise contribution factor ξ, was said to be relatively insensitive to delay cell design parameters. A close look at ξ in equation (90) shows that it is effected by changes in the interstage gain, a_v, and by changes that effect the biasing conditions which determine, γ_1, γ_3 and γ_5. The design constraints surrounding the choice of the small signal inverter gain were just described with the considerations for choosing V_{GS}-V_T. There it was shown that a typical value for a_v was around 1.7. Values much smaller than this would be unusable, and values much larger would fail to optimize jitter through large V_{GS}-V_T. Therefore practical delay cell gains are expected to vary over a small range, say 1.5 to 3. Also, the biasing conditions effecting γ_1 , γ_3 and γ_5 are constrained by some of the same trade-offs that determine the gain. The relative size of M5 to M3 and M6 to M5 determine the constants α and β. These should be kept as small as possible. From the top level perspective, however, the noise contribution factor, ξ, is not a significant parameter in minimizing timing jitter in delay cells. Its value is important, but is set by other circuit design considerations. And, in addition, the parameters which determine it are not likely to vary much from one design to the

next. Typical values for ξ will be derived in chapter 7 when actual delay cell designs are considered. ξ is generally constrained to the range of 2 to 3.

As a final note, the normalized timing jitter in equation (100) is an important figure of merit, but in some cases the absolute jitter is of more use. This r.m.s. timing jitter per delay stage is given by

$$\Delta t_{d\text{-}rms} = \sqrt{\frac{kTC_L}{2}} \cdot \frac{a_v}{I_{SS}} \cdot \xi \qquad (102)$$

the implications of this equation are saved for the next chapter.

4.4 Conclusions

This chapter has provided a model for circuit noise induced timing jitter in the delay cells which make up CMOS ring-oscillators and delay-chains. The fundamental timing error accompanying signals propagating through delay chains has been determined from the thermal noise sources in the devices that make up the inverter delay cells themselves. This result has been refined through a series of analyses, each using a successively more sophisticated set of assumptions and models. Included were the effects of time varying noise sources, and the amplification of noise from one stage to the next. The end result was summarized in a single equation (equation (100)) which expressed the timing error per stage, normalized to the time delay, in terms of basic inverter cell design parameters. And finally, the practical implications of this result, for the design of low-jitter, individual delay cells has been described. The assumptions for each of the three passes through the analysis in this chapter, and the resulting predictions for timing jitter, are summarized again in the tables 3 and 4 which follow.

Table 3: Timing jitter analysis assumptions (repeated)

	Simplified analysis	Advanced analysis	Complete analysis
Diff. pair transistor noise model	constant equilibrium value	time-varying piecewise constant model	time-varying piecewise constant model
Current source trans. noise model	constant equilibrium value	time-varying piecewise constant model	time-varying piecewise constant model
PMOS load trans. noise model	constant	constant	constant
Noise analysis	freq. domain	time domain / autocorrelation function analysis	time domain / autocorrelation function analysis
Jitter translation	first crossing approximation at output of first stage	first crossing approximation at output of first stage	modified first crossing at output of next stage
Interstage amplification	none	none	next stage amplification

Table 4: Summary of timing jitter analysis results

	Normalized timing jitter
First pass	$\frac{\Delta t_{d\,rms}}{t_d} = \sqrt{\frac{kT}{C_L}} \cdot \frac{1}{V_{SW}} \cdot \xi$
	where $\xi^2 = 2\gamma_p + 2\gamma a_v$
Second pass	$\frac{\Delta t_{d\,rms}}{t_d} = \sqrt{\frac{kT}{C_L}} \cdot \frac{1}{V_{SW}} \cdot \xi$
	where $\xi^2 = 2\gamma_1 + 2\gamma_3 a_v \cdot \lambda_a(t_d) + \gamma_5 a_v \sqrt{2\alpha}(1+\beta) \cdot \lambda_b(t_d)$
Third pass	$\frac{\Delta t_{d\,rms}}{t_d} = \sqrt{\frac{kT}{2C_L}} \cdot \frac{1}{(V_{GS} - V_T)} \cdot \xi$
	where $\xi^2 = 2\gamma_1 + 2\gamma_3 a_v \cdot \lambda_{a2}(2t_d) + \gamma_5 a_v \sqrt{2\alpha}(1+\beta) \cdot \lambda_{b2}(2t_d)$

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Chapter 5

Jitter and Phase Noise in CMOS Ring Oscillators and Buffers

5.0 Introduction

This chapter completes the analysis of thermal noise induced timing jitter started in the previous chapter by extending the results to VCOs and relating timing jitter to the frequency domain equivalent of phase noise. Chapter 2 highlighted the importance of timing jitter and phase noise in communications systems. Both are manifestations of random fluctuations in the phase of a signal. The relationships between timing jitter and phase noise at the buffer / delay cell level, the oscillator level, and the PLL level were introduced in section 2.3. In chapter 4, the thermal noise induced jitter contribution of an individual delay cell was determined in terms of delay cell design parameters. In this chapter, we will complete the picture by looking at the implications for the design of low-jitter and low-phase-noise VCOs using inverter delay cells. Also considered will be the phase noise and timing jitter of buffers, or inverter delay chains, not configured in a ring.

5.1 Timing Jitter in Ring Oscillator VCOs

In this section the cycle-to-cycle jitter of a ring oscillator VCO will be determined from the thermal noise induced jitter in the inverter cells that it is composed of. Although some observations on low-jitter delay cell design where made in the last chapter, there are a number of important conclusions about ring-oscillator design that are not evident at the individual delay cell level. The cycle-to-cycle jitter of a VCO is also useful for determining the steady state output jitter in a PLL and for determining the phase noise spectrum of an oscillator.

Suppose the goal is to design a ring-oscillator with a fixed period, T_0, and minimal timing jitter. For an N-stage configuration the period of the oscillator is given by

$$T_0 = 2N \cdot t_d \tag{103}$$

If the noise sources in successive stages are independent then the total jitter variance for once cycle of oscillation is, similarly

$$\overline{\Delta t_{vco}}^2 = 2N \cdot \overline{\Delta t_d}^2 \tag{104}$$

since the jitter variances of each stage will add. In fact, for multiple cycles of oscillation, the total timing error variance relative to a reference transition at time t=0 is given by

$$\overline{\Delta t_{tot}}^2(t) = \frac{\overline{\Delta t_{vco}}^2}{T_0} \cdot t \tag{105}$$

This result was shown in figure 2.8 in the overview section on timing jitter in chapter 2. There is an important assumption underlying this equation, however. This equation assumes that not only are the noise sources independent between delay stages, but the noise sources themselves have a "white" spectrum so that the noise in different periods of oscillation is uncorrelated. When 1/f noise is considered, this is not true. In that case the linear accumulation of timing jitter in (105) will change to a different

slope. This is described in [95]. However, for time differences smaller than the reciprocal of the 1/f noise corner frequency, the result in (105) holds.

In the work presented here we are primarily interested in ring-oscillators as VCO's for use in phase-locked-loops. In that case, errors in the VCO output are corrected for frequencies within the bandwidth of the loop. For reasonable 1/f noise corner frequencies and reasonable loop bandwidths, the impact of 1/f noise on the output of the PLL is not significant. Therefore the focus of this section will be devoted to the impact of device thermal noise.

The cycle-to-cycle jitter of a VCO can therefore be found by substituting the result for the jitter of an individual delay stage, equation (103) from the last chapter, into (104). This yields

$$\overline{\Delta t_{vco}}^2 \cong 2N \cdot \frac{kTC_L}{2(I_{SS})^2} \cdot (a_v \xi)^2 \tag{106}$$

The equation is problematic, however, since it depends on the number of delay stages, making it hard to separate this issue from other design parameters when trying to minimize timing jitter. A much better equation results by making the substitution of $2N = T_0/t_d$ from equation (103). In that case

$$\overline{\Delta t_{vco}}^2 \cong T_0\left(\frac{I_{SS}}{C_L V_{SW}}\right) \times \frac{kTC_L}{2(I_{SS})^2} \cdot (a_v \xi)^2 \tag{107}$$

which simplifies to

$$\overline{\Delta t_{vco}}^2 \cong \frac{kT}{I_{SS}} \cdot \frac{a_v \xi^2}{2(V_{GS} - V_T)} \cdot T_0 \tag{108}$$

The last step employs the approximation for the interstage gain, $a_v \cong V_{SW}/(V_{GS} - V_T)$, described previously.

Equation (108) is a very useful result. The cycle-to-cycle jitter of the VCO is now expressed in terms of the period of the oscillator being designed, rather than in terms of the number of stages. The rest of this section will be devoted to understanding

the implications of this result which answers a number of important questions regarding low-jitter VCO design. Along the way some common misconceptions about ring-oscillator design will be discussed, and some fallacies dispelled.

To design for low jitter, equation (108) suggests that the $(V_{GS}-V_T)$ bias point of the NMOS differential pair transistors in the inverter cells should be made as large as possible. This is consistent with the observations at the end of the last chapter. It was also shown there, that $(V_{GS}-V_T)$ was constrained by voltage gain and voltage swing considerations. In general, $(V_{GS}-V_T)$ is chosen as large as possible while maintaining an interstage gain, $a_v \equiv V_{SW}/(V_{GS}-V_T)$, greater than one, by a sufficient safety margin.

Also suggested by equation (108) is that the gain should be minimized[1], as well as the noise contribution factor, ξ^2. This is also consistent with the analysis of jitter in individual delay stages in the last chapter. The conclusion from that section, was that a_v and ξ where relatively insensitive to the circuit design parameters that could be freely changed in a design, and therefore less important in optimizing for low timing jitter. In typical inverter cells a_v ranges from 1.5 to 3 and ξ, which will be computed for sample circuits in chapter 7, can vary from around 2 to 3 depending on the design.

5.1.1 Timing Jitter as a Function of Power Consumption

The main result of equation (108) is that with everything else fixed, the timing jitter variance improves linearly with an increase in supply current. Since power consumption depends on the quiescent current level, this implies, at least for the class of circuits considered here, a direct trade-off between power consumption and timing jitter. If the tail current, I_{ss}, per stage is increased, then the jitter variance of the ring-oscillator will decrease proportionally. In order to keep $(V_{GS}-V_T)$ constant as well as

1. This contradicts some of the conventional wisdom for minimizing jitter in delay cells. This issue will be addressed shortly.

the delay per stage, this implies scaling the widths of the diff. pair and load transistors along with the current. This is also consistent with the observations for low-jitter delay cell design in the previous chapter. Here we see the result of these implications for the minimization of jitter in the VCO.

Therefore, the timing jitter variance can be improved freely for a ring oscillator with an increase in power consumption, and a corresponding increase in the active circuit area of the ring. This observation is approximately true over a wide range of currents. Increasing the current by a factor of two will improve the r.m.s. jitter by a factor of the square root of 2. Increasing the current by a decade, will reduce the jitter variance by 10 dB.

Interestingly, the implications of equations (108) to *first order* do not change with changes in supply voltage and technology scaling. If $(V_{GS}-V_T)$ is proportional to the supply voltage, then for a constant jitter, decreasing the supply voltage requires increasing the supply current by the same amount. This means that the power consumption stays the same. Scaling of the gate length gives access to higher speeds, but equation (108) states that for a fixed period, T_0, the jitter is proportional to the current itself, and does not depend directly on the gate length. The effects of velocity saturation for very short gate lengths will not have a major impact on this equation either since no form for the current equation has been assumed[2].

5.1.2 Timing Jitter as a Function of Configuration

Another interesting result of equation (108) is that the jitter variance of the ring-oscillator depends on the period of the oscillator itself, and not (to first order) on the exact configuration. Consider the following example. Each of the oscillators in figure 5.1 have the same output period. The first is a six stage differential inverter ring with

2. One assumption in the previous chapter was that $g_m = 2I_d/(V_{GS}-V_T)$. For devices limited by velocity saturation effects the general form of this is approximately the same, but a different constant factor is introduced [96], $g_{msat} \equiv I_{dsat}/(V_{GS}-V_T)$.

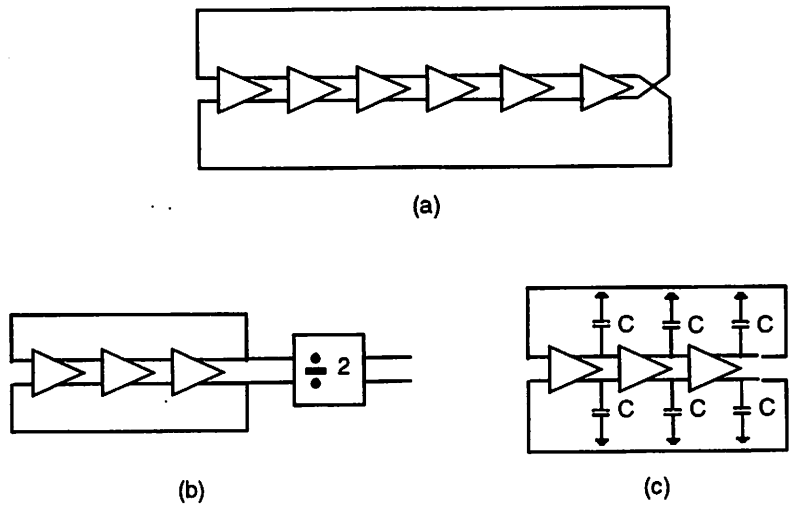

Figure 5.1 Multiple oscillator configurations with same output period

time delay, t_d, per stage (the ring is configured with an odd number of inversions so that it will oscillate). The second oscillator is a smaller, three-stage ring assumed to have delay cells with the same tail current, I_{SS}, and $(V_{GS}-V_T)$, but with a divider following it so that it has the same output period. The jitter in the divider will not effect the phase of the signal being passed around the ring and can therefore be neglected in this example. Divider jitter is similar to jitter in buffers. It effects the phase of the output, but does not effect period of VCO. The third oscillator is also configured as a three stage ring, but extra load capacitance has been added to the output of each stage so that they have a delay of twice that in the other two oscillators $t_d' = 2 \cdot t_d$. Therefore this ring also has the same period.

Since each the oscillators in figure 5.1 has the same period, and each is assumed to have delay cells with same tail current, I_{SS}, and $(V_{GS}-V_T)$, equation (108) predicts that they will all have the same output timing jitter. This is an important result. It says that there is no inherent advantage to using a longer ring-oscillator, unless multiple, parallel phases with closer spacing are needed. In fact, oscillators (b) and (c) are superior from the perspective of power consumption. For a given power specification a

three-stage ring can use twice the current per stage and therefore have an jitter variance that is lower by a factor of two.

The decision between the divider approach in (b) and the slower delay cell approach in (c) depends on the application. The divider power can often be kept small compared to that in the ring, and the addition of a divider adds a fixed amount of additional area. For frequencies that are much slower than the natural frequency of the three stage ring, it is often easier to cascade dividers to attain a lower frequency than to continue to scale up the load capacitance in between stages. For frequencies closer to the natural frequency of a three stage ring, however, the approach in (c) is often the most straightforward.

The idea of lowering the time-delay per stage by lowering the slew-rate of the output transition as in configuration (c) goes against the grain of conventional thinking. This situation will be reconciled shortly, in the section on common misconceptions in low-jitter VCO design.

5.1.3 Timing Jitter as a Function of Output Period

The final implications of equation (108) involve the timing jitter performance as a function of the output period, T_0, of the ring-oscillator being designed. This equation predicts that the jitter variance is actually larger for lower-frequency designs. However, a more useful figure of merit in some applications in the normalized timing jitter. If the jitter of the VCO is normalized to the output period, then we find:

$$\frac{\Delta t_{vco\text{-}rms}}{T_0} = \sqrt{\frac{kT}{I_{SS}} \cdot \frac{a_v \xi^2}{2(V_{GS} - V_T)} \cdot \frac{1}{T_0}} \tag{109}$$

This equation shows that the VCO timing error as a percentage of the overall output period improves for lower frequency designs and increases for higher frequencies. This implies that higher frequency oscillators will have more timing jitter for the same power consumption, and suggests that thermal noise induced timing jitter considerations are increasingly important with higher frequency designs.

5.1.4 Common Misconceptions in Low-Jitter VCO Design

There are a few common misconceptions in low-jitter VCO and buffer design that are addressed by the result in equation (108). The first pertains to the role of the interstage gain in determining jitter and the second to the optimal number of stages for a ring.

In section 4.2.1 the basic path from voltage noise to timing jitter through the first crossing approximation was illustrated. The output timing jitter was said to be related to the voltage noise through the slope of the output waveform (as a function of time) at the nominal threshold crossing time. A common misconception is to confuse the DC transfer characteristic of an inverter delay cell with its slewing behavior. For a DC sweep at the input of an inverter cell, a higher gain inverter will have a differential output that responds with a sharper slope. Does an improvement in slope mean an improvement in timing jitter? The answer is "not-necessarily" since the slope of the output transient is related to the slew-rate of the inverter and not the DC gain.

For inverter delay cells with reasonable gains ($a_v \geq 1$), the slope of the output transient is given by the average slew rate. For the class of circuits considered here, this is approximately I_{SS}/C_L. While it is true that an inverter with a higher gain can switch current from one side of the delay cell to the other more sharply in response to a changing input, it is also true that a lower gain cell will begin switching the current sooner, since its output characteristic is in its active region (not saturated) for a wider range of input voltages. The end result is that, with the exception of very low gain cells ($a_v \leq 1$), which are not useful in general anyway, the effects of small-signal gain on the slope of the output transient and on the time-delay per stage are second-order.

The small-signal gain does effect the timing jitter, however, through interstage amplification. A higher gain per stage means that their is more amplification of noise between stages. This is the reason for the a_v term in the numerator of equation (108). Note that the proportionality to a_v^2 seen in the expression for voltage noise (equation

(89)) is stronger, but one factor of a_v is used when simplifying the expression for the normalized timing jitter, allowing the result to be expressed in terms of $(V_{GS}-V_T)$ rather than V_{SW}. Also effected by the interstage gain is the noise contribution factor, ξ^2 (equation (90)). For a given output resistance, higher gain means a larger g_m for the NMOS devices, and hence a higher noise contribution relative to the PMOS.

Therefore, contrary to one line of thinking, the timing jitter of a VCO is not improved by increasing the gain per stage, but is actually improved through inverter cells with a lower small-signal gain, reducing the interstage amplification and the relative NMOS device noise contributions.

The second misconception which is common in low-jitter VCO design is that the timing jitter improves for ring-oscillators with a higher number of stages. In the section on jitter as a function of configuration, however, a different claim was made. Namely, that VCO timing jitter for a fixed output period was independent of the number or stages used. And furthermore, from a power consumptions perspective, VCOs with fewer stages are preferred.

The reasoning behind using a larger number of stages stems from the following chain of ideas. First, the jitter variance per cycle for a ring oscillator with N stages is given by

$$\overline{\Delta t_{VCO}}^2 = 2N \cdot \overline{\Delta t_d}^2 \tag{110}$$

and the output period is

$$T_0 = 2N \cdot t_d \tag{111}$$

Next, consider doubling the number of stages. If the output period is to be preserved, then the slew-rate per stage has to double so that the time delay is half of its original value. This means that the jitter variance per delay stage which is proportional to the output voltage noise divided by the slew-rate squared decreases by a factor of

four. The jitter variance for the ring oscillator is now given by

$$\overline{\Delta t_{VCO-2}}^2 = 2(2N) \cdot \frac{\overline{\Delta t_d}^2}{4} = \frac{1}{2} \cdot 2N \cdot \overline{\Delta t_d}^2 \tag{112}$$

which is an improvement by a factor of two. The r.m.s. jitter for the VCO improves by $\sqrt{2}$.

This chain of reasoning overlooks a critical point, however. Namely, when changing the slew-rate of the inverters the output bandwidth changes as well. If the time delay per stage is doubled, by reducing C_L at the output, or increasing the current per stage (note that $R_L=V_{SW}/I_{SS}$), then the noise bandwidth is doubled as well. The timing jitter variance per stage, therefore will increase by a factor of two due to noise bandwidth, and decrease by a factor of four due to the slew-rate enhancement. The net change is an improvement by a factor of two, and the total output jitter is the same as before.

$$\overline{\Delta t_{VCO-2}}^2 = 2(2N) \cdot \frac{\overline{\Delta t_d}^2}{2} = 2N \cdot \overline{\Delta t_d}^2 \tag{113}$$

5.2 Phase Noise

In the previous section the cycle-to-cycle jitter of a ring-oscillator VCO was determined from the thermal noise sources in the devices which make up the ring. Useful relationships have been established between jitter performance and delay cell design parameters. In this section the attention turns back to phase noise and to finding a link from VCO timing jitter to the frequency domain. The impact of oscillator phase noise in RF transceivers was shown in chapter 3. The goal of this section is to derive an expression for VCO phase noise in terms of the basic design parameters of the VCO.

In chapter 2 the impact of phase noise on an oscillator output spectrum was illustrated. Phase noise was measured in dBc/Hz at an offset frequency, f_m, away from the carrier. This measure was a comparison of the power in a 1-hz bandwidth at that off-

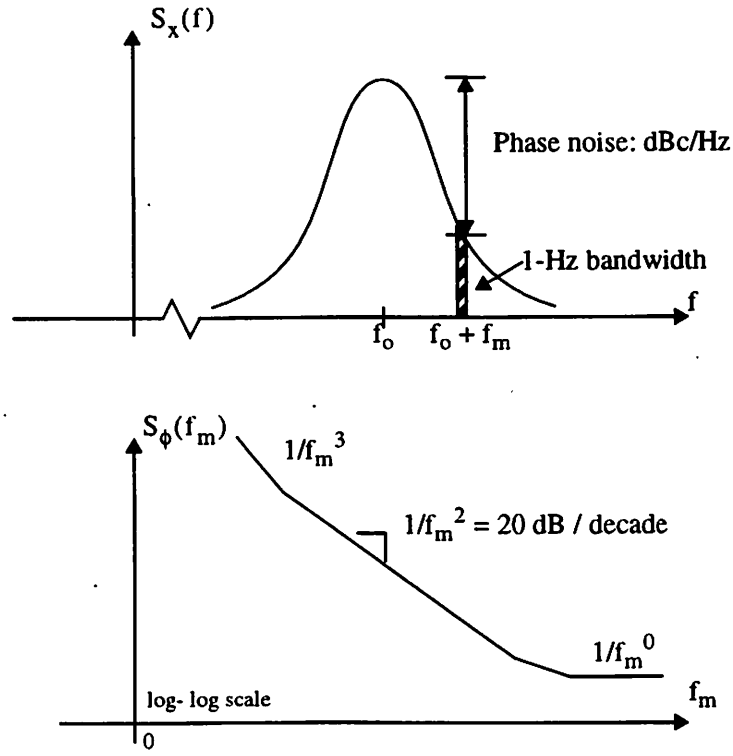

Figure 5.2 Oscillator phase noise: (a) power spectrum of oscillator (b) phase fluctuation power spectral density

set to the total power of the carrier. Figure 2.6 from that chapter is repeated here for reference.

As mentioned in chapter 2, the phase noise output spectrum can also be considered directly, as shown in figure 5.2(b). In this case the phase noise is represented with a single sideband instead of a double, with the x-axis being the offset frequency itself. This is a plot of the spectral density of phase fluctuations, as opposed to the spectrum of an output sinusoid with a given phase noise, which is the plot in figure 5.2(a).

This distinction is worth noting here, since the analysis will focus on deriving phase noise from phase and frequency fluctuations directly, rather than the output spectrum. Consider a signal

$$X(t) = A\cos(2\pi f_o t + \theta(t)) \qquad (114)$$

If $\theta(t)$ is a noisy, random signal then X(t) is said to exhibit phase noise. The power spectrum of the signal X(t) in such a case, looks like $S_x(f)$ in figure 5.2(a). The sidebands of the output signals power spectrum are related to $\theta(t)$. Another perspective on the noise process, however, is to look at the spectral representation of $\theta(t)$ directly. This is called the spectral density of phase fluctuations, $S_\theta(f)$, and is the representation pictured in figure 5.2(b)[3]. Still other useful characterizations of the signal in (114) exist, including the spectral density of frequency fluctuations and normalized frequency fluctuations. The instantaneous frequency of the signal in (114) is given by the time derivative of the cosine argument.

$$f_{inst}(t) = f_o + \frac{d\theta}{dt} \tag{115}$$

The spectral density of $\Delta f = f_{inst} - f_o$ is called the spectral density of frequency fluctuations. Similarly, the spectrum of $y = \Delta f / f_o$ is called the spectral density of normalized frequency fluctuations. Relationships between each of these expressions are given in [97] and can be summarized by

$$S_\theta(f) = \left(\frac{1}{f_m}\right)^2 S_{\Delta f}(f) = \left(\frac{f_o}{f_m}\right)^2 S_y(f) \tag{116}$$

For frequencies far enough away from carrier, the phase noise in dBc/Hz measured from the power spectrum of X in figure 5.2(a), is the same as the spectral density of phase fluctuations in rad^2 / Hz shown in 5.2(b). This is discussed in [97][4].

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3. Although the single-sided phase representation is used for illustration in figure 5.2(b), most of the analysis which follows will be for a double-sided $S_\phi(f_m)$. Therefore $S_\phi(f_m)$ is the term commonly referred to as phase noise, or L(f) in some references. The single-sided p.s.d. for phase fluctuations is larger by a factor of two.

4. This property can also be readily shown by taking the power in the phase fluctuation p.s.d. in 1-hz bandwidth slice at a given offset, and treating it as a FM modulation source for the oscillator. If the power where y rad^2/Hz, then using the narrowband FM approximation the resulting sideband in the oscillator p.s.d. can be shown to be down from the total carrier power by y dB. This corresponds to a phase noise of y dBc/Hz.

5.2.1 Phase Noise / Timing Jitter Relationship

In this section a link is sought from cycle-to-cycle timing jitter in a VCO to its output phase noise spectrum. Consider a VCO with nominal period T_o, and with a timing error accompanying each period that is gaussian, with zero mean and variance $\overline{\Delta t_{vco}}^2$. If this timing error is expressed in terms of phase ($\Delta\phi = 2\pi\,\Delta t/T_0$), then the variance of the phase error per cycle of oscillation is given by

$$\sigma_\phi^2 = (2\pi)^2\left(\frac{\Delta t_{vco-rms}}{T_0}\right)^2 \tag{117}$$

The total phase error as a function of time is the sum of all past phase errors. For the thermal noise sources considered here, the noise contributions are white and there is no correlation from cycle-to-cycle. With independent timing errors for each cycle of oscillation, the total phase error is a random variable which exhibits a random walk. The phase noise of the output spectrum can be modeled as a Wiener process and will be analyzed similarly to a laser phase noise analysis performed by Barry in [98]. A second approach to this analysis can also be taken which yields the same result. This approach will be illustrated in section 5.3.2 when deriving phase noise for a delay buffer.

A Wiener process is a one in which the variance of a random variable increases linearly with time. This is a good model for independent cycle-to-cycle timing errors in a VCO. Written as a continuous signal the phase error is given by

$$\phi(t) = \int_0^t \phi'(t)dt \tag{118}$$

where the time derivative, or instantaneous frequency error $\phi'(t)$ is considered to be a zero mean white gaussian process with power spectral density

$$S_{\phi'}(\omega) = 2\pi\Delta\vartheta \tag{119}$$

Since phase is the integral of frequency, the power spectral densities of phase and frequency fluctuations are related by a factor of $1/\omega^2$.

$$S_\phi(\omega) = \frac{1}{\omega^2}(2\pi\Delta\vartheta) \tag{120}$$

The term $\Delta\vartheta$ is called the "line-width" of the spectrum. And is the general specification for phase noise in lasers. In this analysis, this term will be related back to the cycle-to-cycle jitter σ_T^2.

The phase error accumulated between any two points in time can be denoted by the random variable

$$\Phi(t1, t2) \equiv \phi(t1) - \phi(t2) = \int_{t2}^{t1} \phi'(u)du \tag{121}$$

The variance of this random variable is shown in [98] to be

$$\sigma_\Phi^2 = E\left[\int_{t2}^{t1}\int_{t2}^{t1} \phi'(u)\phi'(v)dudv\right] \tag{122}$$

$$\sigma_\Phi^2 = 2\pi\Delta\vartheta \int_{t2}^{t1}\int_{t2}^{t1} \delta(u-v)dudv = 2\pi\Delta\vartheta|t1 - t2| \tag{123}$$

The variance of the phase error, therefore increases linearly with time. However, we also know that for a separation of one period of oscillation, t_1-t_2 = T_o, the variance of the phase error is σ_ϕ^2, as in equation (117).

$$E\{|\phi(t)|^2\} = (2\pi)^2\left(\frac{\Delta t_{vco-rms}}{T_0}\right)^2 \tag{124}$$

Therefore

$$(2\pi)^2\left(\frac{\Delta t_{vco-rms}}{T_0}\right)^2 = 2\pi\Delta\vartheta T_0 \tag{125}$$

and from (120), the phase noise power spectral density is given by

$$S_{\phi}(\omega) = \frac{1}{\omega^2}(2\pi\Delta\vartheta) = 2\pi\frac{\omega_0}{\omega^2}\left(\frac{\Delta t_{vco-rms}}{T_0}\right)^2 \tag{126}$$

Expressed in terms of frequency, f, (using $\omega=2\pi f$) this result is

$$S_{\phi}(f) = \frac{f_0}{f^2}\left(\frac{\Delta t_{vco-rms}}{T_0}\right)^2 \tag{127}$$

Plotted on a log-log scale, the phase noise as a function of offset frequency looks like the graph in figure 5.3. The absolute height depends on the center frequency of oscillation, f_0, and the ratio of the timing error per cycle of oscillation to the oscillation period. This means that for a fixed percentage jitter ($\Delta t_{vco\text{-}rms} / T_0$), higher frequencies of oscillation have inherently higher phase noise at a given offset frequency.

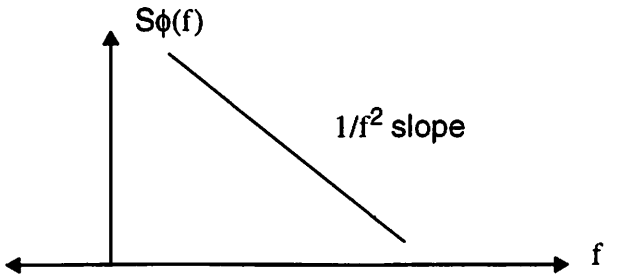


Figure 5.3 Phase noise power spectral density.

5.2.2 Phase Noise in Ring Oscillators

With the relationship between phase noise and timing jitter established in equation (127), phase noise can now be related to the delay-cell design parameters considered earlier. Using the result for cycle-to-cycle jitter from the previous section (equation (108)) and rearranging terms, we arrive at

$$S_{\phi}(f_m) = \left(\frac{f_0}{f_m}\right)^2 \bullet \left(\frac{F_1 kT}{I_{SS}(V_{GS} - V_T)}\right) \tag{128}$$

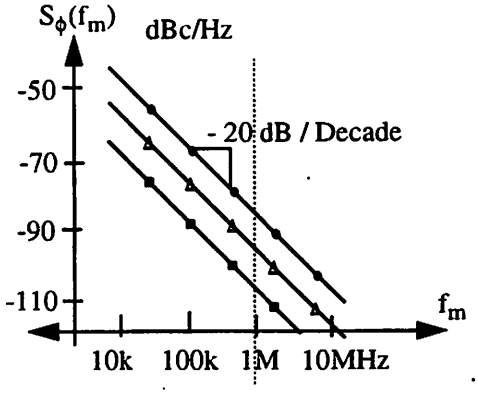
where the offset frequency is now denoted by f_m, the distance of the offset frequency from carrier. This equation shows that phase noise is related to the ratio of the center frequency to the offset frequency squared, times a factor related to delay cell device design. The familiar thermal noise factor kT is in the numerator, and is multiplied by the term F_1. This term is just a simplified constant equal to the 1/2 times the interstage gain, a_v , times the noise contribution factor ξ^2.

$$F_1 = \frac{a_v \cdot \xi^2}{2} \tag{129}$$

These two parameters where discussed in the section on cycle-to-cycle VCO jitter, where it was determined that were relatively insensitive to delay cell design tradeoffs. For typical ring-oscillators, a_v is in the range of 1.5 to 3 and ξ is in the range of 2 to 3. In the denominator of the second term in (128) we also find the product of the tail current per delay stage times the gate-to-source bias above threshold for the NMOS differential pair transistors. As described previously, $(V_{GS}-V_T)$ is constrained by voltage swing and gain requirements, but I_{SS} can be scaled to reduce cycle-to-cycle jitter, or in this case, phase noise. Once again, a scaling of I_{SS} implies a corresponding scaling of gate width W, so that $(V_{GS}-V_T)$ remains constant.

From equation (128), it is apparent that increasing the current consumed per delay stage will reduce the phase noise. The rate of improvement is 10dB per decade increase in current. For the current-mode-logic delay cells considered here, which consume static power, the power consumption is proportional to the current as well. In addition, if gate widths are scaled proportionally with the ratio of current to $(V_{GS}-V_T)$, then total circuit area will increase as well.

A comparison of predicted performance for a typical ring-oscillator design at three different power levels is shown in figure 5.4. Here, the phase noise is plotted on a log-log scale versus offset frequency, falling at a rate of 20 dB/decade with increasing



Example; Four Stage 1.6 GHz Ring Oscillator

Power Consumption	Phase Noise @ 1 MHZ Offset
o 1 mW	-91 dBc/Hz
Δ 10 mW	-101 dBc/Hz
□ 100 mW	-111 dBc/Hz

Figure 5.4 Phase noise versus power consumption

offset due to the $(1/f_m^2)$ term in (128). Predicted phase noise at a 1 MHz offset is given for 1mW, 10mW, and 100 mW designs. The phase noise at a given offset improves 10 dBc/Hz with each decade increase in power consumption.

The general form of the phase noise equation in (128) is in good agreement with the classical phase noise derivation for LC-tank oscillators. Analysis in [99], [100] and [101] predict a phase noise expression that has the same dependence on the ratio of center frequency to offset frequency $(f_o / f_m)^2$.

$$S_\phi(f_m) = \left(\frac{f_0}{f_m}\right)^2 \bullet \left(\frac{1}{Q^2}\right)\left(\frac{FkT}{4P}\right) \tag{130}$$

In addition, phase noise depends on a factor F, related to the amplifier in the LC oscillator forward path, times the thermal noise energy kT. The factor F is analogous to the F_1 term in (128). Also common to both equations is a term with units of power in the denominator. For the LC oscillator this is the output power of the oscillator itself. In the ring-oscillator case, the product of I_{SS} and $(V_{GS}-V_T)$ has units of power and is proportional to the static power consumed in the ring oscillator VCO (since $(V_{GS}-V_T)$ is related to Vdd through the interstage gain, and the product of I_{SS} and Vdd is the total power consumption per cell). What differs between the two is the additional factor of

$(1/Q^2)$ in equation (130). This term shows that LC type oscillators have an additional phase noise improvement related to the quality factor of the resonator. This quality factor depends on resistive losses in the elements comprising the LC tuned circuit. For typical off-chip LC tank elements, Q's on the order of 100-1000 are possible, resulting in phase noise improvements of 40 to 60 dBc/Hz, everything else being the same. For LC VCO's employing on-chip elements for the LC, such as spiral or bond-wire inductors, and varactors integrated with the rest of the active circuitry, Q's on the order of 3-to-8 have been observed [102, 103, 104, 105]. This corresponds to phase noise improvements on the order of 9.5 to 18 dBc/Hz. Of course the other parameters, the factor F, and the power consumed in an oscillator vary from case to case as well.

Unlike ring-oscillator VCO's however, the trade-off between power consumption and phase noise is complicated by other circuit design considerations. The power consumed in an LC oscillator is related to the resistive loss in its circuit elements, which are in turn related to the Q of the LC-tank. Therefore, changing the power term in equation (130) implies a change in the circuit Q. Ultimately, the choice of center frequency and the range of practical inductor and varactor sizes available to the designer determine the circuit Q and the power consumption in the oscillator. In some cases, as described in [102], the phase noise actually improves with lower power consumption, P, due to these other considerations.

For ring-oscillator VCOs, however, there is freedom for the designer to change the current per stage, I_{ss}, over several orders of magnitude, allowing for a range of possible phase noise performance levels. Since device sizes are scaled with the current, this implies an increase in area as well. In some applications there are other incentives to increase the size and power consumption of the ring as well. In a PLL for instance, it makes sense that the VCO power budget is at least as high as for the other components of the system. Also, for applications where the VCO is called upon to drive mixers or sampling circuits with reasonably high capacitive loads, a larger VCO is favored. Ultimately there will be buffers between the ring-oscillator and the load, but starting with a

larger ring can ease the requirements on buffer design.

5.3 Timing Jitter and Phase Noise in Buffers and Delay Chains

The preceding sections have investigated timing jitter and phase noise for ring-oscillator VCOs. In this section their impact is considered for clock buffers and for chains of delay cells (voltage-controlled-delay chains) that are not configured in a ring.

5.3.1 Timing Jitter in Buffers

In addition to use in ring oscillator VCOs, the inverter delay circuit considered in the previous chapter, and similar circuits, can be used to buffer clock or oscillator signals in a communications system. The normalized timing error accompanying such a delay stage was shown to be

$$\frac{\Delta t_{d\ rms}}{t_d} = \sqrt{\frac{kT}{2C_L}} \cdot \frac{1}{(V_{GS} - V_T)} \cdot \xi \tag{131}$$

and the non-normalized timing error was given by

$$\Delta t_{d\text{-}rms} = \sqrt{\frac{kTC_L}{2}} \cdot \frac{a_v}{I_{SS}} \cdot \xi \tag{132}$$

The second of these, which is the net timing jitter at the output of a buffer due to its thermal noise sources, is the parameter of interest in buffer design. The implications of (131) were covered in section 4.3, where selection of $(V_{GS}\text{-}V_T)$ and scaling of C_L was discussed to minimize the normalized timing jitter. But this is not the same as minimizing the total output jitter.

Equation (132) predicts that the timing jitter of a buffer will improve by reducing the load capacitance at its output and by increasing the tail current of the stage. A low gain, and low noise contribution factor are desirable, as before, but are generally constrained to a narrow range of values.

If the load capacitance is dominated by the circuit being driven by the buffer, then we expect a linear improvement in the r.m.s. jitter with increases in the tail current. As considered previously, increasing the current calls for a corresponding increase in the gate widths of the devices in the delay cell, to keep other parameters constant. For large enough current, the parasitic capacitances at the buffers output, such as the triode region gate to drain capacitance of the load ($1/2 \cdot WL \cdot C_{ox}$), can dominate the capacitance being driven. At this point, the net timing jitter improvement with further increases in current (and gate widths) will go as the square root of I_{SS}. In both cases the r.m.s. timing jitter improves with an increase in power consumption.

Further improvements can be achieved by minimizing unwanted parasitic capacitances at the output, and even minimizing the input capacitance of the stage being driven, when possible.

5.3.2 Phase Noise in Buffers

Timing jitter in clock buffers also translates into phase noise when viewed in the frequency domain. It has already been suggested in chapter 2 that the phase noise introduced by a clock buffer is different than that introduced in an oscillator. For the oscillator case, timing jitter introduced with each cycle of oscillation corrupts the instantaneous frequency of the oscillator. The result was shown to be phase noise sidebands which fall as $1/\omega^2$. In the clock buffer case, timing jitter corrupts the phase of the output signal, but does not change the instantaneous frequency of the source which drives it. This can be shown to create a white phase noise spectrum ($1/\omega^0$).

The introduction of timing jitter to a clock source and the resulting phase noise are illustrated in figure 5.5. A timing error with variance $\overline{\Delta t_d}^2$ is added to each edge in the output signal. If just the thermal noise sources in the buffer circuit are considered, then noise from once cycle of oscillation to the next is uncorrelated. Samples of the output phase error as a function of time might appear as in figure 5.6, where the variance of

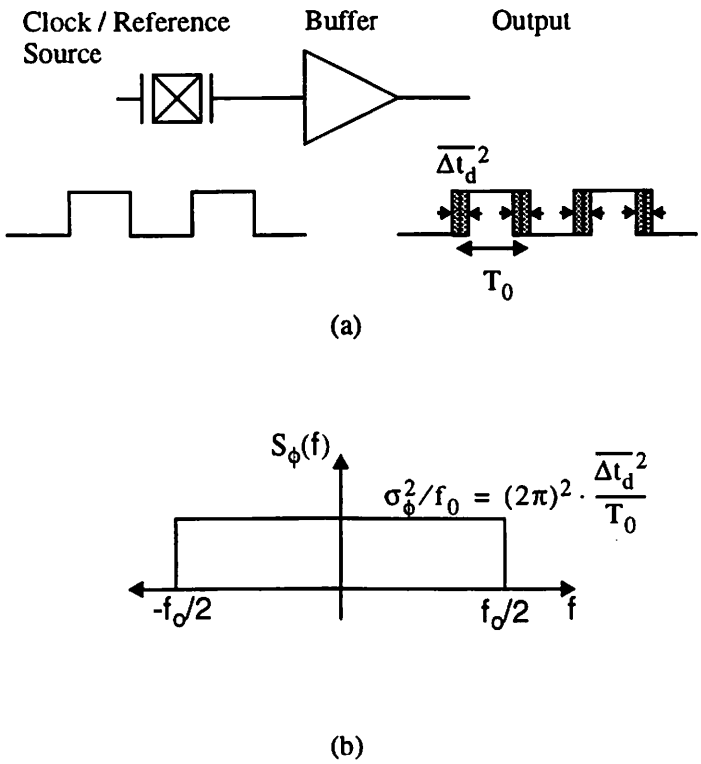


Figure 5.5 Timing jitter in clock buffers: (a) addition of timing jitter to output signal, (b) resulting output phase noise spectrum

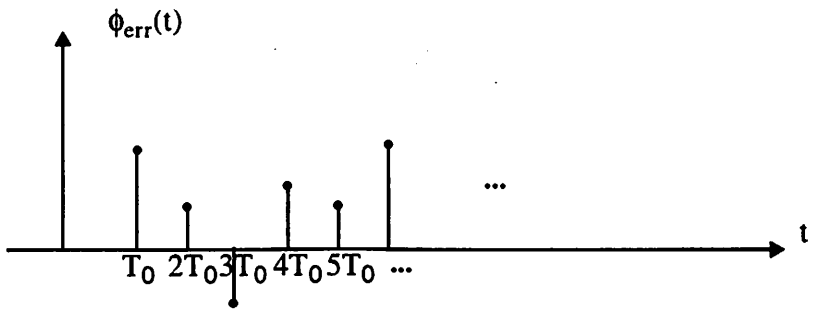


Figure 5.6 Phase error as a function of time

each sample is given by

$$\sigma_\phi^2 = (2\pi)^2 \cdot \frac{\overline{\Delta t_d}^2}{T_0^2} \tag{133}$$

If the phase error is actually considered to be zero in between the time instances T_0, $2T_0$, ... , then there are problems related to the analysis of non-bandlimited continuous time white noise [107], [108]. The autocorrelation function for this noise process and the output power spectral density (which is the fourier transform of the autocorrelation function) can be more readily found with a further assumption for the value of the phase noise between "samples". If the phase error samples are assumed to be nyquist rate samples of a white noise process bandlimited to $(-f_o/2, f_o/2)$, then a reasonable answer can be attained. The result is a band-limited approximation to the phase noise with a power spectral density of height σ_ϕ^2/f_0 in band, as pictured in figure 5.5.

This means that the phase noise in band is white with power spectral density

$$S_\phi(f) = \sigma_\phi^2/f_0 = (2\pi)^2 \cdot \frac{\overline{\Delta t_d}^2}{T_0} \tag{134}$$

Therefore phase noise can be improved through the same techniques described in the last subsection for reducing the jitter of the buffer stage. This means that the phase noise floor will improve with higher power consumption. Also, the phase noise floor for a given output jitter is higher for higher frequency sources.

5.4 References

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Chapter 6

Ring Oscillator VCO Design

6.0 Introduction

There are many critical issues surrounding the implementation of ring-oscillator VCOs and voltage controlled delay chains for high performance phase-locked-loop systems. The realization of VCOs with good supply noise rejection, low-jitter, and high frequency capability requires careful attention to circuit design issues. In addition, the center frequency of a VCO can vary with changes in the power supply, temperature, or even with variations in processing. Designing a VCO which is resistant to drift and has an ample tuning range to cover process variations is important. These topics and other practical implementation issues are the subject of this chapter.

The focus will be on structures employing the class of differential inverter circuits analyzed in the preceding chapters on timing jitter. This differential delay cell and the replica biasing technique used for the PMOS load transistors was introduced by B. Kim for use in disk drive clock recovery PLLs ([109], [110],[111]). This topology has proven successful because of its rejection of substrate and power supply noise, relatively high-speed capability, and relatively low thermal noise-induced jitter.

The chapter will begin with a look at the basic delay cell operation, including

the replica bias circuit used to establish the output swing. Voltage gain and swing considerations will be described. A brief look at other biasing circuits which are important to temperature and supply insensitive operation will also be presented. The next section will investigate the range of frequencies attainable with a ring-oscillator. Performance as a function of process technology will be considered. Ring-oscillators employing the differential delay circuit considered here can be tuned over a broad range of frequencies. However, they are also sensitive to device processing variations. Strategies for the coarse tuning of a VCO's center frequency will be addressed as well as the approach to the "voltage-control" path of the VCO.

The conclusions from the first two sections will be applied in section 6.3 to the design of ring-oscillator inverter delay cells in a 0.6u n-well CMOS process. These delay cells are used in the ring-oscillator VCOs and test arrays described in the next chapter. The complete design sequence for the delay cells will be described, and transistor sizes determined.

6.1 Basic Delay Cell Design

The basic differential delay cell is shown in figure 6.1. It features a source coupled differential pair with resistive loads which are implemented by PMOS transistors in the triode region of operation. Also shown in the figure is a typical DC sweep for an inverter cell biased with a 1V swing at the output. The differential input voltage required to fully switch the differential pair is approximately $\sqrt{2}$ times the $(V_{GS} - V_T)$ bias point of the diff. pair in the balanced case with a differential input of zero [112]. A replica biasing circuit is used to adjust the gate bias of the PMOS load devices for a fixed swing at the output. A simplified schematic of the replica biasing circuit is shown in figure 6.2. In this circuit a current source with the same magnitude (or current density) used in the differential delay cell draws current from a replica of the PMOS load transistor. A feedback loop using a simple operational amplifier gain block sets the

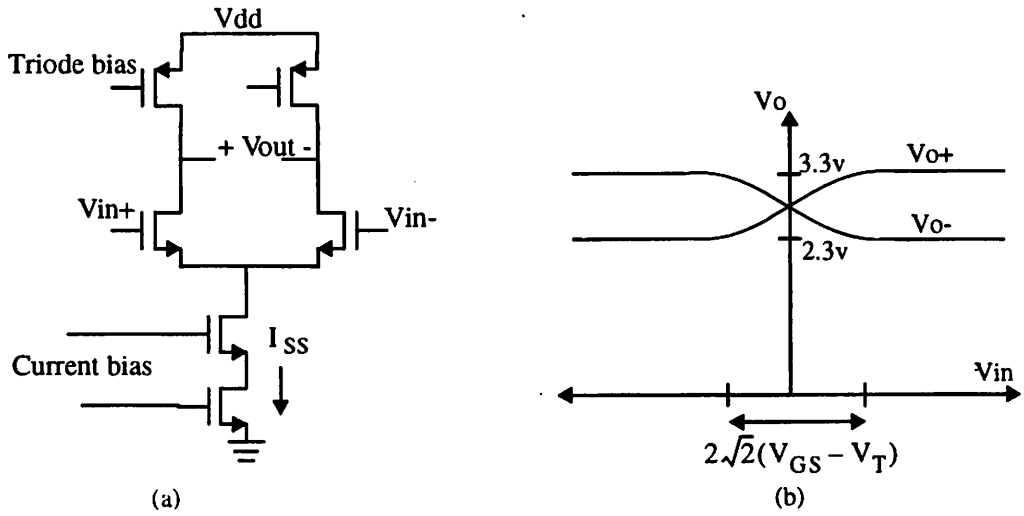

Figure 6.1 (a) Differential delay cell circuit (b) DC transfer characteristic

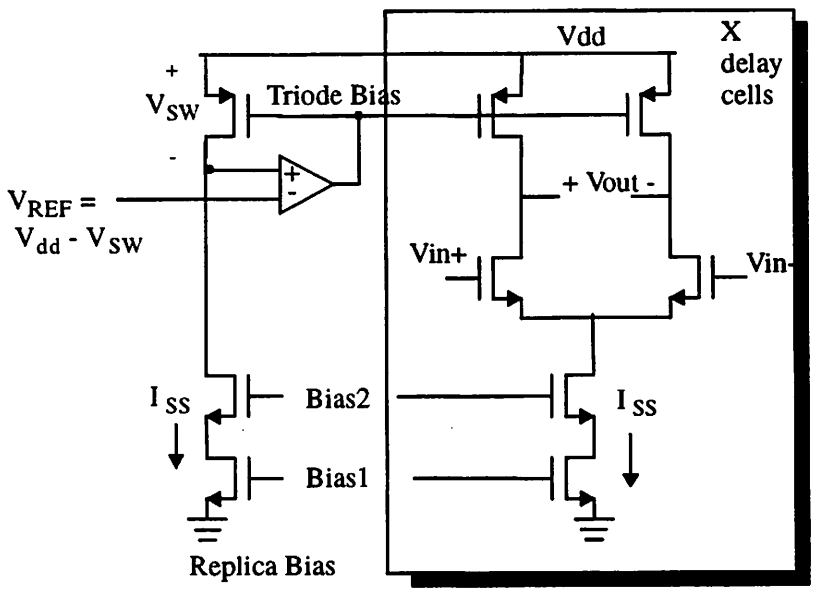

Figure 6.2 Simplified replica biasing circuit schematic

PMOS gate bias voltage so that with the full I_{SS} flowing through the load device a drain-to-source voltage of V_{SW} is seen across it. This gate bias voltage is drives the loads in the differential delay cells, resulting in a DC swing of V_{SW} for each side (total

differential output swing of $2V_{SW}$).

This circuit can be used to set the swing at the appropriate level over a wide range of supply, and biasing conditions. The nominal time delay per stage in a delay chain employing such elements is $t_d = C_L V_{SW}/I_{SS}$. If the current source, I_{SS}, is swept over a range of values and the swing is held constant by the replica bias, then a wide range of frequencies can be attained. This gives the ring-oscillator a wide coarse tuning range. In effect, by changing the current and allowing the replica biasing circuit to adjust the gate bias for the triode load, we are tuning the resistance of the output load device. This changes the time delay per stage, or equivalently the 3dB frequency ($\omega_{-3db} = 1/RC$) of the output of each delay cell.

6.1.1 Voltage Swing Considerations

The choice of output swing, V_{SW}, is influenced by several competing factors. At the top level there is the trade-off between speed, which favors low output swing, and noise margins, which favor high. There are many other factors as well. For one, the gain of each inverter stage must be greater than one (with a sufficient safety margin) for a ring to oscillate. The gain of a stage is approximately equal to the ratio of the output swing to the $(V_{GS}-V_T)$ bias point of the NMOS differential pair devices.

$$a_v = g_m R_L \cong \frac{2(I_{SS}/2)}{(V_{GS}-V_{TN})} \cdot \frac{V_{SW}}{I_{SS}} = \frac{V_{SW}}{V_{GS}-V_{TN}} \tag{135}$$

This means that a low swing will require a low $(V_{GS}-V_T)$ bias point as well, which results in a higher thermal noise-induced jitter per stage, as discussed in chapters 4 and 5.

In many applications, a suitably large output swing is required to drive the mixers or sampling circuits which use the VCO output. A buffer is usually placed in between, but for high frequency signals, there are trade-offs in the gain and bandwidth of the buffer circuits themselves. Providing sufficient gain to boost a small VCO output

signal as well as enough bandwidth to drive a large load may be too difficult. For this reason, a reasonably large output swing in the VCO is desired.

There are also considerations which limit how large of an output swing is useful. First, it is desirable to keep the resistive PMOS load transistors in the triode region of operation. This requires a drain-to-source voltage that is kept below the (V_{GS}-V_{TP}) bias point of the PMOS transistors

$$V_{SW} \leq V_{GS} - V_{TP} \tag{136}$$

The gate-to-source voltage for the PMOS loads can be close to the full supply voltage, allowing for reasonably large swings. With a supply voltage of 3V and a threshold voltage of around 1V, swings as large as 2V could be achieved, for example. However, it is usually preferable to keep the load devices deep in the triode region over the entire range of the output voltage swing. This provides a more linear output resistance which helps with the shape of the output waveforms, including the matching between the rising and falling waveform shapes. It also guarantees good performance over process variation. For this reason an even smaller output swing is desired.

A third limit on the output swing comes from considerations of the differential pair transistors. Generally, level shifting buffers are not used between stages when high frequency operation is a concern. When one differential delay stage drives a similar, second stage, then the differential pair transistor with a high input voltage requires a large enough Vds to remain in saturation

$$V_{DS} \geq V_{GS} - V_{TN}$$

or

$$(V_{DD} - V_{SW}) - V_S \geq (V_{DD}) - V_S - V_{TN}$$

which simplifies to

$$V_{SW} \leq V_{TN} \tag{137}$$

In an n-well CMOS process the threshold voltage of the NMOS differential pair devices is influenced by the body effect. A good choice of V_{SW} in a typical process is often around 1V. This was the value used for the practical delay cells described later, implemented in a 0.6μm CMOS process.

The biasing of the inverter circuits such that equation (137) is satisfied is not absolutely critical to delay cell operation. However, exceeding this limit will result in more unusual output waveforms since devices are changing regions of operation during the transient. An excessive swing is also disruptive from the perspective of the other transistor in the differential pair. The voltage needed to fully switch a diff. pair is around $\sqrt{2}(V_{GS} - V_{TN})$ (ref. [112]). Swings larger than this drive the transistor with a low input voltage further into the cut-off region of operation, requiring more time to recover when the inputs begin switching the other way.

6.1.2 Gain Considerations

Equation (135) expressed the gain per stage as the ratio of the output swing, V_{SW}, to the gate bias voltage above threshold, $(V_{GS}-V_T)$, for the NMOS differential pair devices. Once the voltage swing for the inverter delay cells is determined, the $(V_{GS}-V_T)$ bias point, for a given gain per stage, is governed by that relationship.

It was suggested previously that the gain per stage needs to be sufficiently larger than one for the ring-oscillators to oscillate. The gain should be sufficiently high to insure oscillation over a range of different process and temperature conditions. In the analysis of timing jitter, however, it was concluded that higher gains are not beneficial, but actually increase timing jitter through interstage noise amplification. Therefore the gain is kept as small as possible, while leaving a sufficient safety margin for process and temperature variations. In the practical delay cell design described in section 6.3 a gain of 1.7 was chosen.

The $(V_{GS}-V_T)$ bias point for the differential pair transistors in this case is predicted by equation (135) to be around 590mV for an output swing of 1V. A more accurate approximation to $(V_{GS}-V_T)$ is found from the drain-to-source current equation for the device. This value is usually smaller than that predicted above. An example will be given in section 6.3. In both cases, however, the bias voltage is consistent with the voltage swing considerations of the last section.

6.1.3 Biasing Considerations

The time delay per stage of $t_d = C_L V_{SW}/I_{SS}$ can be made stable over supply variations and temperature variation by stabilizing V_{SW} and I_{SS}. This is achieved through a combination of three bias circuits; a voltage reference, a current reference, and the replica bias. These circuits are shown in figures 6.3, 6.4, 6.5 respectively. These building blocks are described in more detail in references [109], [111] and [113].

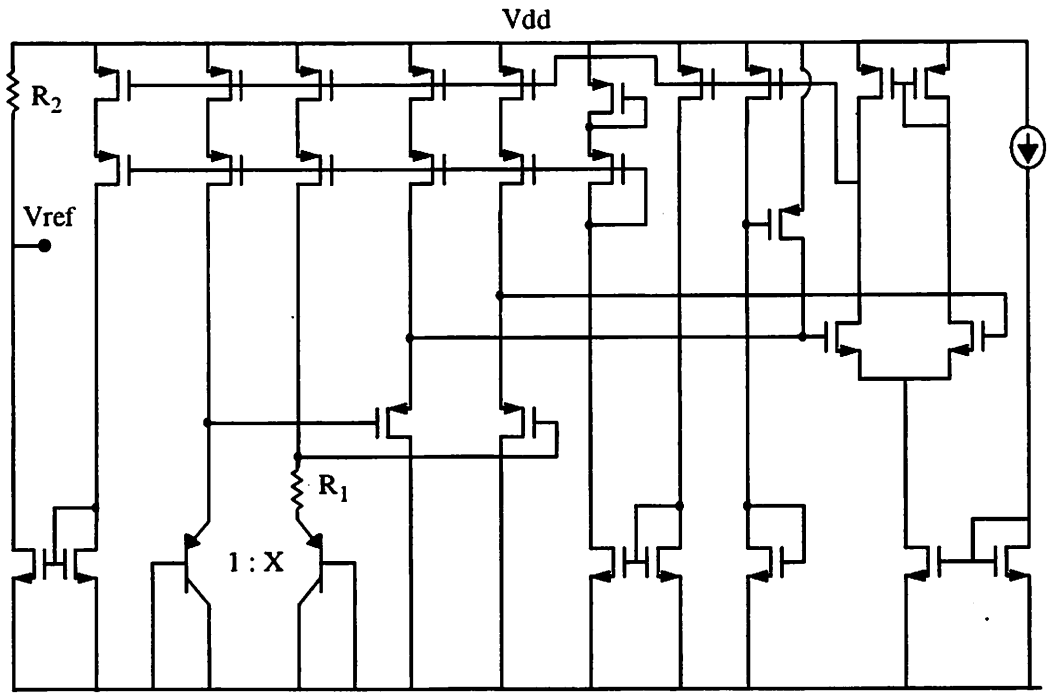

Figure 6.3 Voltage reference generator

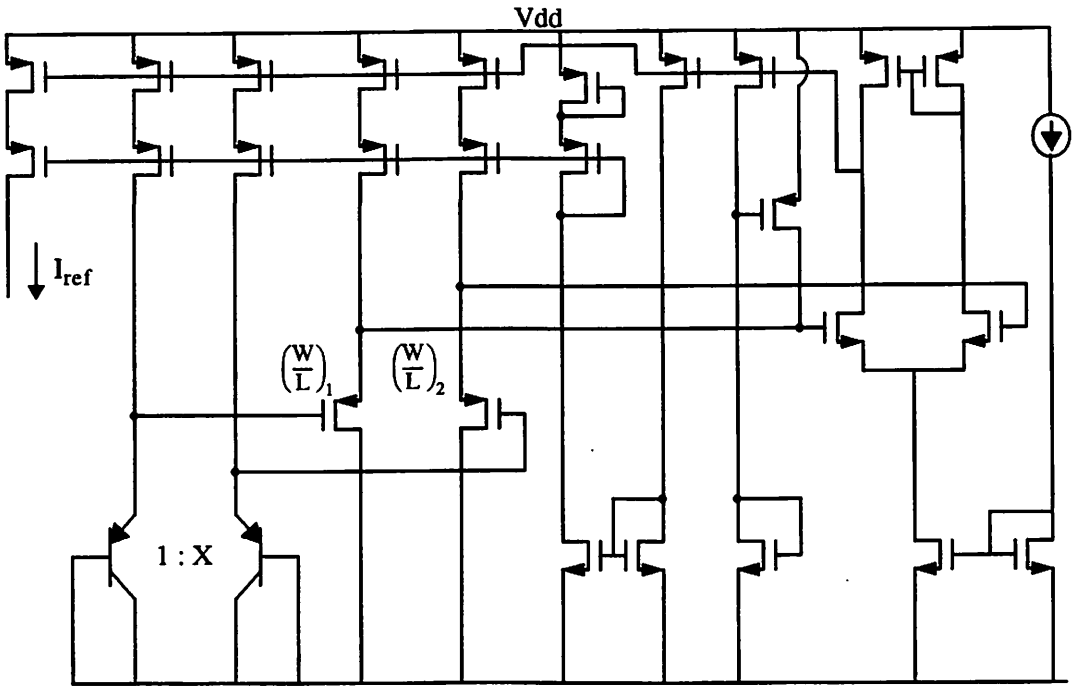

Figure 6.4 Current reference generator

The voltage reference develops a ΔV_{be} mismatch across a fixed resistance to generate a PTAT current. This current is then drawn through another resistor attached to the supply to give a reference voltage of

$$V_{ref} = Vdd - \frac{kT}{q} \cdot \ln(X) \cdot \frac{R_2}{R_1} \tag{138}$$

where X is the ratio of the PNP device sizes. This reference voltage is used in the replica bias circuit to set the nominal DC output swing. The swing is therefore proportional to absolute temperature and is insensitive to the power supply variations. It depends on a ratio of resistances, which match reasonably well over process variations, and to a ratio of device areas.

$$V_{SW} = \frac{kT}{q} \cdot \ln(X) \cdot \frac{R_2}{R_1} \tag{139}$$

The current reference uses a feedback loop match a ΔV_{be} mismatch in pair of

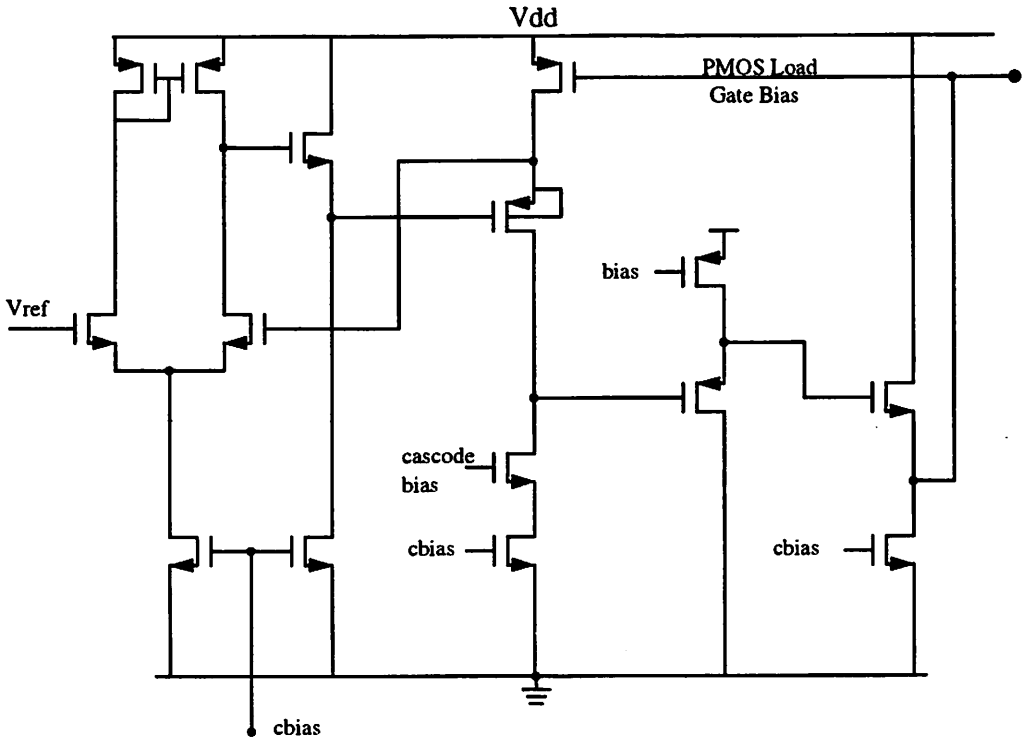

Figure 6.5 Replica bias circuit

bipolar devices to a $\Delta(V_{GS} - V_T)$ mismatch in a pair of MOS devices. The end result is a current that depends on the thermal voltage kT/q, device sizes, and device mobility

$$I_{SS} = \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)_1 \frac{\left[\frac{kT}{q} \cdot \ln(X)\right]^2}{\left[1 - \sqrt{\frac{(W/L)_1}{(W/L)_2}}\right]} \tag{140}$$

Including the effects of temperature on device mobility, this current has a net temperature dependence of somewhere between $T^{(1/2)}$ and T^1. Therefore, the time delay per stage has a net temperature dependence that is between $T^{(1/2)}$ and constant. This current is also supply independent, so the time delay per stage is independent of supply voltage, to first order, as well. There are some second order effects, such as the variation in some of the load capacitance parasitics with supply voltage, but the net effect is a circuit which is resilient to variations in supply and temperature.

The replica bias circuit and voltage reference also insure a swing which is relatively independent of process variations, another important consideration. In the next section, however, we will see that the center frequency of a VCO does change substantially with process changes, due to changes in the current and in the load capacitance. Therefore some range of tunability in the current reference is desirable, and a current DAC can be used to supply less current for the fast process case and more current for the slow.

Bypass capacitors are an important consideration for the replica bias and current and voltage reference circuits. On-chip bypass capacitors can be used within these circuits to help reduce their noise contribution to the ring-oscillator delay cells which can result in timing jitter. Even more critical are large bypass capacitors on the key input nodes to the inverter delay cells. Namely, the PMOS load gate bias and the current source gate bias. As will be seen in the next section, the output frequency is very sensitive to variations in these bias voltages. Supply noise and other sources which couple on to these bias nodes can modulate the VCO creating spurious tones in the output spectrum. Therefore a large bypass capacitance to Vdd for the PMOS gate bias, and to ground for the current source transistor are required.

6.2 Ring Oscillator VCO Design

High performance ring-oscillator VCOs for a number of different applications can be realized with the inverter delay cell introduced in the preceding section. The requirements for these applications vary in performance parameters such as the required jitter, but also in the range of frequencies needed for the VCO. Center frequencies can vary from the 10's to 100's of MHz in some lower frequency clock recovery applications to the 1-2 GHz range in a RF frequency synthesizer design. This section will explore the performance limits for the speed of a ring oscillator as a function of technology while suggesting a design approach for lower frequency applications as well.

6.2.1 Oscillator Frequency Limits

The period of a ring oscillator with N delay stages is approximately 2N times the delay per stage. This translates to a center frequency of

$$f_{osc} = \frac{1}{2N \cdot t_d} \cong \frac{I_{SS}}{2N \cdot C_L V_{SW}} \tag{141}$$

A useful substitution is made by noting that the term I_{SS}/V_{SW} is actually the reciprocal of the effective resistance of the triode load. The small signal resistance of the PMOS load is given by

$$R_L = \left(\frac{dI_D}{dV_{DS}}\right)^{-1} \cong \frac{1}{\mu C_{OX}\left(\frac{W}{L}\right)[V_{GS} - V_T - V_{DS}]} \tag{142}$$

If the load is biased well into the triode region so that its output resistance is not too non-linear, then the small signal resistance at the midpoint of the V_{DS} vs. I_D curve is a good representation of the average resistance. This is the point where $V_{DS}=V_{SW}/2$. In this case, the expression in (142) can be substituted for V_{SW}/I_{SS} in equation (141).

Another simplification comes from examining the load capacitance term, C_L. The load capacitance seen at the output consists of the gate-to-source capacitance of the next stage, the drain-to-gate capacitance of the triode load, as well as drain to bulk parasitic capacitances and wiring capacitances. The input capacitance of the next stage is either $(2/3)W_3L_3C_{OX}$ or $W_3L_3C_{OX}$ depending on whether the device is in the saturation region of operation or cut-off. The triode load capacitance is approximately $(1/2)W_1L_1C_{OX}$. Likewise, the drain-to-bulk parasitics are approximately proportional to the product of the gate width and gate length of the respective devices. When making changes in the basic delay cell, such as increasing the current per stage for example, the gate widths of the NMOS and PMOS are generally scaled together. This was discussed with the low jitter delay cell design considerations in chapter 4 as a means of keeping

the current density in the devices constant. In this case, the total output capacitance can be reasonably modeled as a constant times WLC_{OX}, where the constant is made up of the contributions of each of the capacitances at the output.

$$C_L = K_L \cdot WLC_{OX} \tag{143}$$

If this is expressed in terms of the gate width and length of the triode load device, then it can be substituted into equation (141). Making this substitution along with simplification from equation (142) we arrive at

$$f_{osc} = \frac{1}{2N} \cdot \frac{\mu}{K_L \cdot L^2} \cdot [(V_{GS} - V_{TP}) - V_{SW}/2] \tag{144}$$

This equation captures the basic trade-offs and technology limitations which influence ring-oscillator design. First, the frequency depends on the number of stages. The minimum number of practical stages is three[1]. A maximum frequency is attained with as few stages as possible. The use of differential inverter delay cells allows for rings with an even number or stages. To arrive at a net signal inversion around the loop, one of the stages is wired to the next as a buffer rather than inverter.

The next factor influencing the output frequency is the capacitance factor K_L. This term is made smaller by minimizing all of the parasitic capacitances seen at the output. A smaller K_L results in a higher maximum output frequency.

The technology limitations of output frequency are evident in the μ/L^2 dependence. Interestingly, the maximum output frequency has the same technology dependence as the unity current gain frequency of the individual devices, f_t. Moving to a processes with narrower gate lengths gives a rapid improvement in the maximum output frequency proportional to the scaling factor squared.

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1. Two stages may also be used if extra phase shift is added to the loop through buffers in the signal path, between stages. This approach was used in [114]. These buffers add extra delay however and the maximum frequency of oscillation is reduced accordingly.

And finally, the output frequency depends on the (V_{GS}-V_T) bias point of the PMOS load and the voltage swing at the output. Higher output frequencies favor a large gate-to-source bias which is consistent with the goal of maintaining good linearity in the triode region output resistance. The output frequency is also improved for smaller output swings, but this parameter is governed by the design trade-offs discussed in the previous section. The gate-to-source voltage, however, can be made very large, approaching the total supply voltage, Vdd, in the limit. However, when designing a circuit which is capable of adapting to process variations, as described in the next subsection, it is important to keep the gate-to-source bias somewhat below its maximum value so that it can be adjusted for the slow process parameter case to maintain the desired output center frequency.

6.2.2 VCO Center Frequency Variation

The sensitivity of the VCO output frequency to changes in device process parameters is evident in equation (144). The dependence on μ/L^2 means the center frequency varies greatly with the lateral diffusion parameter and the defined gate length of devices. Process variations of +/- 0.05u for a 0.6u gate length, for example would yield a center frequency variation of around +/- 18%. Variations of +/- 0.1u result in a factor of two separation between the lowest frequency and highest frequency case. Other process parameter variations effect this as well.

Fortunately, differential delay cells with a triode load (and replica biasing) are easily tunable over a wide range of frequencies. As described in the first section of this chapter, the current per stage can be tuned over a wide range while the replica bias adjusts the resistance of the load so that a fixed swing, V_{SW}, is maintained. The range over which this approach works depends primarily on the range of resistance values that can be achieved in the triode load by varying its (V_{GS}-V_T) bias point.

For a fixed output load device size, the output resistance is at its minimum value when a full supply voltage, Vdd, is applied across the PMOS gate. The resistance increases as the gate-to-source bias is decreased until the point where $V_{GS} - V_{TP} = V_{SW}$ and the load device falls out of the triode region of operation (the resistance then increases to a very high value, but the inverter circuit does not perform well in this mode of operation). Therefore the range of output resistances that can be tuned is bounded by

$$V_{TP} + V_{SW} \leq V_{GS} \leq V_{DD} \tag{145}$$

Substituting this range into the equation for the oscillator center frequency (eq (144)) shows the practical range of output frequencies. With a threshold voltage of 0.8V, a supply voltage of 3V and an output swing of 1V, this translates into a tuning range of +/- 25%, which is very wide. In a 1GHz oscillator for example, this would correspond to a tuning range the extends from 800MHz to 1.25 GHz. In practice even wider spans are possible. Relaxing the requirement in (145) by 100mV on the low side, for example, and increasing the supply to 3.3V yields a tunability range of +/- 32%.

The range in (145) is the fundamental limit defined by the PMOS load device. Care must be taken that the replica biasing circuit can deliver the full range of voltages without imposing un-necessary limitations due to its operation. This can be somewhat challenging since the process variations which are being tuned out effect the biasing circuitry as well. Critical voltage swing considerations in the biasing circuits need to leave margins for process variation as well.

The method for tuning to VCO center frequency is also an important consideration. In most PLL applications, the VCO control voltage tunes the output frequency over its entire useful range. In the 1GHz oscillator example just given, this would be a tuning range of 450 MHz. If useful control voltage range in PLL is 1V, for example, this would result in a VCO gain of 450 MHz/V. This may be okay in some applications, but is too high for many. A high VCO gain imposes constraints on the range of other PLL

design parameters such as the gain (or attenuation in the loop filter) and the gain of the phase detector. Also, a high VCO gain makes a PLL very sensitive to ripple at the loop filter output which causes spurious modulation sidebands in the output spectrum. The effects of other noise sources, such as substrate noise coupling to the VCO control node are also enhanced. Furthermore, the use of low pass filtering in the replica bias loop to reduce noise coupling into the VCO may place a low-frequency pole in the forward path of the PLL which limits the maximum bandwidth attainable for the loop.

Therefore, it is desirable in some applications to use a combination of coarse and fine tuning. The coarse tuning can be achieved through a current DAC which adjusts the current in the replica bias and in the delay cells to tune the desired center frequency over its entire range. A higher frequency control voltage path is then used to adjust some smaller portion of the tuning range, resulting in a lower VCO gain for the PLL.

There are some draw-backs to the coarse/fine tuning approach as well as some benefits. One of the key issues, of course, is how an application chooses the correct coarse setting. This implies an additional feedback loop in addition to the PLL itself. Typically, coarse tuning could be accommodated in a pre-amble period, or synchronization period if one exists for a given application. This can often be controlled through the digital-signal-processing (DSP) block which frequently follows the analog signal processing path (and the PLL) in many applications.

Although it adds to system complexity, coarse tuning can also result in some side benefits when it is applied. One example is in a frequency synthesizer application employing a fully differential charge-pump circuit. A fully differential charge pump, which was discussed briefly in section 3.2, is used to reduce ripple at the output of the phase detector / loop filter [115]. The spurious tones in a frequency synthesizer depend on the amount of undesired ripple at the output of the charge pump circuit. A differential charge pump has significantly lower ripple, particularly when its differential output (which is the control voltage for the VCO) is very close to zero. For large control volt-

age outputs (one side at +500mV, the other at -500mV, for example), the output ripple is still better than for the single-ended approach, but not as good as for a control voltage of zero, when the two sides of the circuit completely match. When coarse tuning is available, the possibility of centering the VCO frequency exists, so that the resulting control voltage in the PLL is close to zero, thus reducing the spurious tones in the synthesizer.

6.2.3 VCO Control Path Tuning

With the coarse tuning of the ring-oscillator center frequency achieved through the use of a current DAC, a fine tuning technique is needed for the PLL voltage control path. This can be achieved by steering additional current into the delay cells which is not mirrored in the replica triode device, as illustrated in the simplified schematic in figure 6.6. In this circuit the differential control voltage input drives a differential pair and steers some portion of additional biasing current through a current mirror into the delay cell devices. Benefits of this approach include a differential control voltage input

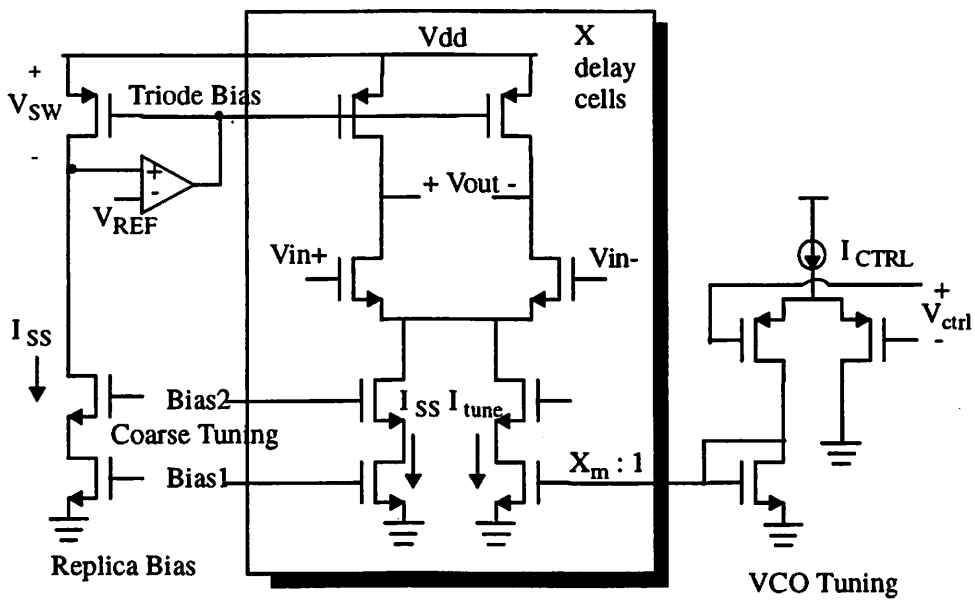

Figure 6.6 VCO control voltage tuning path

which is compatible with differential implementations of the loop filter and charge pump circuits preceding the VCO. As was just described, this approach has much lower output ripple than the single ended case and can greatly reduce output spurious tones. Furthermore power supply and substrate noise coupling are reduced as well. Another benefit is that this control path can be a high bandwidth path, not limiting the bandwidth of the PLL, while the replica biasing circuit can be heavily bypassed to help reduce coupling of noise sources to the sensitive gate bias of the PMOS load devices.

To first order, increasing the current in the delay cells would have no effect on the frequency of the output. This is because the time delay per stage, $t_d = C_L V_{SW}/I_{SS}$, depends on the ratio of V_{SW} to I_{SS}. If the load where actually a linear resistor then increasing the current would increase the swing proportionally and the time delay per stage would remain constant. With the triode device, however, there is a second order variation, in the output swing with respect to changes in current. This non-linearity allows the VCO to be tuned over a small range through variations in the supply current.

The VCO gain is given by

$$K_{VCO} = \frac{\partial f_0}{\partial Vctrl} \equiv \frac{\partial f_0}{\partial I_{tune}} \cdot \frac{\partial I_{ctrl}}{\partial Vctrl} \cdot X_m \qquad (146)$$

where I_{tune} is the amount of additional current being supplied to the delay cells (and not to the replica) and X_m is the ratio of device sizes in the current mirror in figure 6.6, which is also the ratio of I_{tune} to I_{ctrl}. The middle term in equation (146) is just one half of the transconductance of the differential pair used to steer the current in the control path, or Gm/2. This term can be adjusted along with the factor X_m to generate the desired overall VCO gain.

The first term on the right hand side of (146) depends on the non-linearity in the resistance. It is best measured from simulation since it is hard to predict accurately from device current equations. This term can actually be expanded by considering the expression for output frequency in equation (141). If the nominal output resistance R_L

is substituted for V_{SW}/I_{SS}, then the contribution of this term can be determined from

$$\frac{\partial f_0}{\partial I_{tune}} \cong -\frac{1}{4N \cdot C_L} \cdot \left[\frac{\partial}{\partial I_d}\left(\frac{1}{R_L}\right)\right] \cong -\frac{f_0}{R_L} \cdot \frac{\partial R_L}{\partial I_d} \tag{147}$$

Therefore this term depends on the center frequency of the VCO, the nominal load resistance, and the sensitivity of that resistance to changes in current. If the load were a linear resistor instead of a triode region device, then the resistance would not change with operating current and the expression in (147) would evaluate to zero, The non-linearity in the resistive load, however, results in a usable VCO gain which can be tailored to a given applications requirement by adjusting the other parameters in (146).

The total tuning range of the VCO accessible through the control voltage path is given by

$$\text{Tuning Range} \cong \frac{\partial f_0}{\partial I_{tune}} \cdot I_{CTRL} \cdot X_m \tag{148}$$

where I_{CTRL} is the total tuning current available to the control path differential pair. The tuning range can be set through I_{CTRL} and X_m. The transconductance which determines VCO gain is further defined through the choice of the device sizes of the differential pair. However, this also determines how wide the linear voltage range of the differential pair input is. The input control range is nominally

$$+/-\sqrt{2}(V_{GS} - V_T)$$

For noise considerations it is best to keep the input controlling signal as large as possible. With a large $(V_{GS}-V_T)$ bias point for the differential pair devices ranges of around +/- 750mV are reasonable.

6.2.4 Lower Frequency Ring-Oscillator Design

In many applications the goal is not to push the VCO center frequency to its fundamental performance limits. There are several design approaches to adjusting a ring-oscillator's operating range to a lower band of frequencies. Several of these ideas were discussed in section 5.1.2 which looked at timing jitter as a function of the configuration of the ring. A lower than maximum frequency oscillator can be realized by using more inverter stages in the ring, by adding additional capacitance to the output of each stage to slow down the time delay per stage, or by following a higher frequency ring with a divider circuit. These approaches are illustrated again in figure 6.7. As described

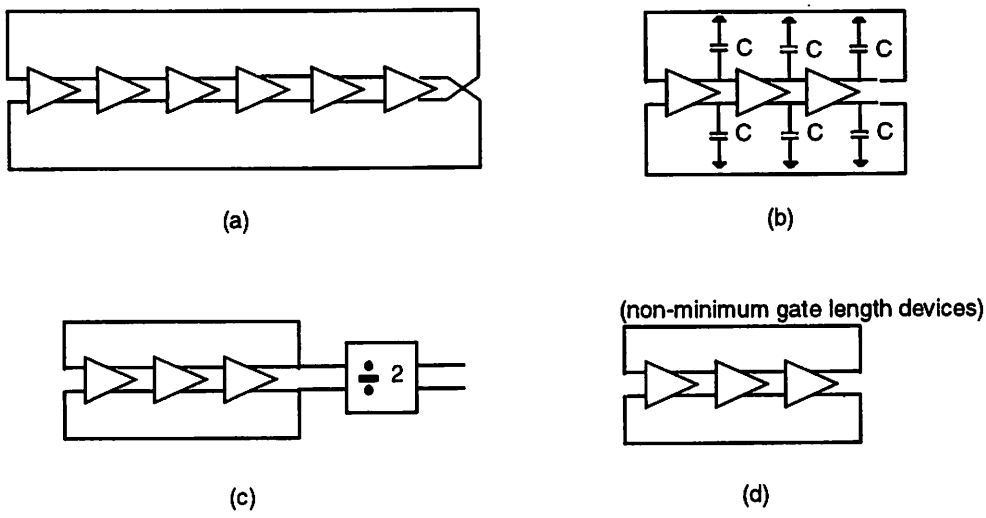

Figure 6.7 Multiple oscillator configurations with same output period

in the discussion of timing jitter, each of these approaches has the same nominal jitter performance, except that the longer chain ring requires more total power consumption.

When frequencies significantly lower than the nominal output frequency for a short chain (three or four stages) ring oscillator are desired, a fixed divider circuit, often requiring only a few D-flip flop cells can be used. Circuits which divide by two, three, or other practical multiples can readily be designed with the same differential styled logic as used in the inverter delay cells. A good discussion of frequency dividers

can be found in [113].

The frequency range of a VCO can also be adjusted by adding additional load capacitance at the output. This is the best approach when the ring needs to be slowed down from its maximum frequency operating range, but not by a factor of two or more as would be achieved with a divider. As discussed in the last chapter, there is not a timing jitter penalty associated with the slower output slew rates. Lower slew rates do hinder jitter performance in buffer design, but not in a ring-oscillator. When additional load capacitance is added to each stage's output, the frequency of the ring-oscillator has a form similar to equation (144), but with the additional effects of the added load

$$f_{osc} = \frac{1}{2N} \cdot \left[\frac{\mu}{K_L \cdot L^2} + \frac{\mu C_{ox}}{C_{added}} \left(\frac{W}{L} \right) \right] \cdot [(V_{GS} - V_{TP}) - V_{SW}/2] \qquad (149)$$

A fourth possibility is also included in figure 6.7(d). This approach involves using non-minimum gate lengths, and increased gate widths to achieve a higher capacitance per stage. This is always an option for slowing down the delay per stage in a ring. In some cases it may provide area benefits over the approach in (c). The trade-off depends on the overhead for adding additional capacitors to a design versus the increase in the active area of the devices.

6.3 Delay Cell Design and Implementation

The previous two sections have outlined the basic operation and the range of frequencies possible for ring-oscillators employing differential inverter delay cells. In the process a number of design considerations have been introduced. These considerations and the low-jitter design conclusions from the previous chapter will now be applied to the design of an actual inverter cell.

We know from the discussions so far that timing jitter and phase noise can be improved through increased power consumption. In fact, by scaling the current per

- Choose output swing, V_{SW}
- Set target current, I_{SS}
- Set target (V_{GS}-V_{TP}) bias point for PMOS load devices (including margin for process variation)
- Determine PMOS load device sizes $(W/L)_1$
- Determine NMOS differential pair device sizes $(W/L)_3$ to meet target gain while maximizing (V_{GS}-V_T)
- Determine current source device sizes and configuration

Figure 6.8 Delay cell design steps

delay stage along with device sizes (so that the current density remains constant) the phase noise performance of a ring can be improved systematically, within the limits of the power budget and practical constraints on area. In this section, however, the focus is on optimizing the core delay cell so that regardless of the amount of scaling, the relative device sizes in the circuit are optimized for speed and timing jitter performance. The basic cell developed here will then be used in several different ring configurations described in chapter 7.

The discussion in this section will be based on a 0.6u n-well CMOS process offered by TSMC. This process includes three metal layers and two poly layers. The basic design sequence is outlined in figure 6.8. The first step is to choose the desired output swing. In this case a swing of 1V is chosen for the reasons described in section 6.1.1. The supply voltage in this design is 3.3V. A target current per stage of 1.25mA will be used in this design. This corresponds to a total of 5mA for a four stage ring-oscillator. This figure, however can be arbitrarily scaled (within the limits of practical device sizes) as suggested previously.

The next step is to determine the (V_{GS}-V_{TP}) bias point of the PMOS load devices. These considerations where described in section 6.2.2. For typical-typical process model parameters we will aim for a nominal V_{GS} of 2.8V, leaving a margin of 500mV for lowering the resistance (increasing the center frequency). Next, the PMOS

load device sizes need to be chosen so that with a the desired current set as well as the gate-to-source voltage the resulting drain to source voltage is V_{SW} as desired. This can be determined from the current equation for a device in triode region. A more accurate approach, however, is to look at device curve traces from simulation or measurement. For example, setting V_{DS} to 1V and looking at a trace of I_D versus V_{GS} for several different (W/L) ratios, the appropriate device size can be determined. For a current of 1.25 mA per stage and a gate-to-source voltage of 2.8V the PMOS load devices, in this 0.6u CMOS process, should be sized

$$\left(\frac{W}{L}\right)_1 = \frac{25\mu}{0.6\mu}$$

The actual layout implementation features two devices of width 12.5μ sharing a common drain (for reduced drain to bulk capacitance, and layout symmetry). Minimum channel length devices are used for higher speed.

The NMOS differential pair devices sizes are chosen for the correct small-signal gain. Gain considerations were described in section 6.1.2. Smaller gate widths result better speed as well as a larger (V_{GS}-V_T) bias point, which is beneficial from a jitter perspective. The small-signal gain needs to be kept sufficiently above one however for oscillation, including a margin for process variation. The gain with typical-typical process models in this case was chosen to be 1.7, resulting in a device size of

$$\left(\frac{W}{L}\right)_3 = \frac{37.5\mu}{0.6\mu}$$

for the target current level of 1.25 mA. This gate width was determined through simulation to insure the target gain was met. This results in a (V_{GS}-V_T) bias point of around 370 mV, which can be found from device current equations. Once again the layout implementation features two parallel devices with size 18.75μ.

The final consideration is the delay cell current source transitor(s). Here there is a choice between a cascoded current source which offers potentially better resistance to

noise coupling and a single current source transistor. The drawback of the cascoded current source approach is that smaller saturation voltages (Vdsat) are required to insure that the current source transistors stay in saturation. For a fixed current, this translates into a higher transconductance, g_m , which results in a larger thermal noise contribution for the current source devices. This sizing issue shows up in the noise contribution factor for the timing jitter of a delay cell as the parameter α (equation (90)). A single current source device favors lower jitter.

In this design a cascoded current source was used for safety at the expense of slightly higher jitter. The total jitter contribution of the current source transistors (as shown in the next chapter) is still a reasonably small percentage of the overall jitter in the delay cell. High swing biasing techniques are used to set the cascode gate voltage. A saturation voltage of around 400 mV for each of the current source transistors is acceptable for swing considerations. The resulting device size was

$$\left(\frac{W}{L}\right)_5 = \frac{9x15\mu}{0.8\mu}$$

This completes the specification of the basic inverter delay cell. In chapter 7 the performance of several ring-oscillators using this circuit will be described.

6.3.1 VCO Tuning

The last aspect of the inverter cell design to consider is the fine-tuning VCO control path. In section 6.2.3, tuning considerations where described and equations (146) and (148) where given to describe the VCO gain and tuning range. The VCOs to be described in the next chapter require a gain of around 10 MHz / V and a tuning range of around 10 MHz. The tuning approach introduced in section 6.2.3 is also quiet amenable to implementation of a programmable VCO gain. By allowing additional current segments to be switched into I_{ctrl} , the VCO gain (and range) can be changed as well. For example, in the VCOs to be presented in the next chapter, an optional high gain mode of nominally 40MHz/V and tuning range of around 40 MHz was added. To pre-

serve the input tuning range of the control path differential pair, additional diff. pair devices (extra gate width) should be added with additional current segments for constant current density.

The VCO gain using this approach was shown previously to be

$$K_{VCO} \cong \frac{\partial f_0}{\partial Vctrl} \cong \frac{\partial f_0}{\partial I_{tune}} \cdot \frac{g_m}{2} \cdot X_m \tag{150}$$

where the transconductance, g_m, is that of the control path differential pair transistors in the balanced state. As mentioned before the first term on the right hand side of this equation is best measured from simulation since it is not accurately predicted using conventional device current equations. Simulations for the cells considered here showed a current sensitivity of around 200MHz / mA. For an input voltage tuning range for the V/I converter of 1.3V (+/- 650mV differential) the diff. pair transistors should have

$$V_{GS} - V_T = \frac{650mV}{\sqrt{2}} = 460mV \tag{151}$$

The nominal control current for the tuning path was chosen to be 116uA. This results in a transconductance of

$$g_m \cong \frac{2(I_{ctrl}/2)}{(V_{GS} - V_T)} = 250\ uA/V \tag{152}$$

For a VCO gain of 10 MHz/V, this requires a mirror ratio of $X_m = 2/5$. The tuning range, given by equation (148), is 9.28 MHz, close to the 10MHz nominal specification. By choosing the control current and mirror ratio appropriately, the desired VCO gain and tuning range were achieved as well as the correct input voltage range for the V/I converter. Device sizes for the V/I converter are W/L = 2.5u/0.6u. The nominal tuning current per cell is $(2/5) \cdot (116uA/2) = 23.3uA$; which is just 2% of the total supply current per stage.

6.4 References

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Chapter 7

Experimental Results

7.0 Introduction

This chapter presents experimental and simulation results for an array of ring-oscillator test structures intended to validate some of the design considerations in chapters 5 and 6. The wide range of operating frequencies attainable in a ring-oscillator through coarse tuning of the tail current is demonstrated as well as the high bandwidth VCO tuning approach described in section 6.2.3. Experimental measurements of phase noise and timing jitter are also discussed. VCO phase noise measurements where carried out for an array of test structures with different center frequencies, demonstrating some of the predictions from chapter 5. Timing jitter was investigated through transient noise simulation using a novel monte-carlo simulation approach. Jitter simulations for a VCO test array with constant frequency and varying current levels were used to demonstrate the improvement of cycle-to-cycle VCO jitter with power consumption.

7.1 Ring Oscillator VCO Results

Using the ring-oscillator delay cell design described in section 6.3 a group of

ring-oscillator test structures were developed to investigate phase noise and timing jitter performance over a range of design conditions. The structures implemented included an array of five ring-oscillators with varying capacitive load, covering a range of frequencies from around 275 to 700 MHz, and two high frequency ring-oscillators for use in RF frequency synthesizer applications. The two high frequency VCOs were designed to operate at frequencies of around 1.7 Ghz, and 800 MHz respectively.

Figure 7.1 shows the schematics for the ring-oscillators array. The differential

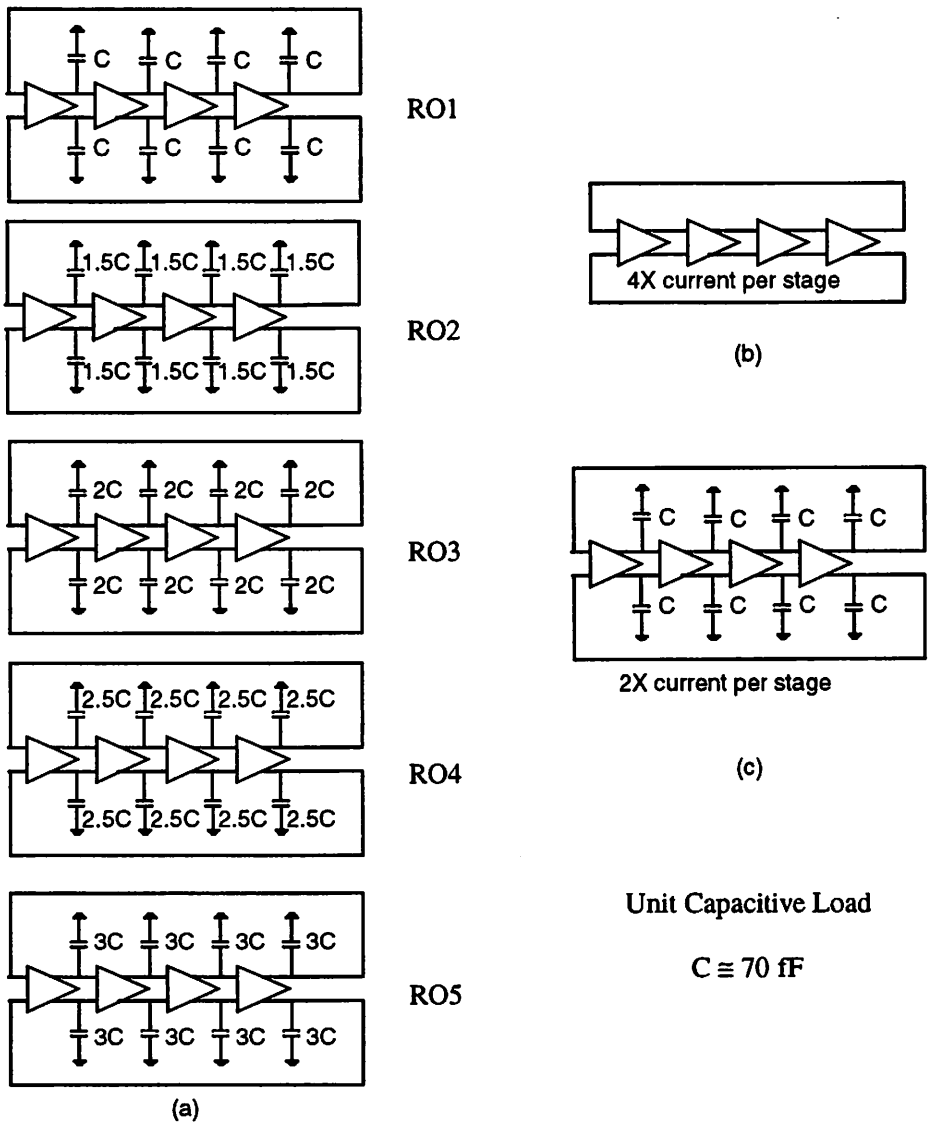

Figure 7.1 Ring oscillator test structures: (a) capacitively loaded test array, (b) VCO for LO1 frequency synthesizer, (c) VCO for LO2 frequency synthesizer (followed by modulus 4 divider)

delay cells are the same as those described in section 6.3. Each of these test structures is a four stage ring-oscillator. One unit inverter cell is used per delay stage for the test array. For the two frequency synthesizer test VCOs, however, each stage is implemented with multiple, parallel unit cells to improve phase noise. Phase noise and/or timing jitter is reduced through the increase in power consumption per stage. The same effect can also be accomplished with larger unit cells (this also minimizes unwanted wiring parasitics). With multiple unit cells, however, a common-centroid-like layout is possible. By distributing the unit cell components of each stage in the ring appropriately, better matching of the delay per stage can be accomplished, helping to minimize timing skew. This parameter is important in applications which use multiple oscillator output phases. Quadrature mixers, for example, require in-phase (I) and quadrature (Q) oscillator pouts. The phase matching between these two signals affects the unwanted sideband rejection attainable for the system [116].

The coarse tuning range of a ring-oscillator VCO was described in section 6.2.2. The replica bias circuit can adjust the load over a wide range of resistances in response to a swept supply current. This insures that the output swing will remain fixed and the ring-oscillator can track a changing bias current to cover a wide range of different output frequencies. This is illustrated with the measured results for the ring-oscillator test array in figure 7.2. The center frequency of R01, for example can be tuned over the range of around 400 MHz to 700 MHz as the current per stage is increased from 0.3mA to 1.1mA. This is a tuning range of +/-27% from the midpoint frequency of 550MHz. The lowest frequency oscillator, R05, was tunable from 275 MHz to 450 MHZ, a range of +/- 24%. With careful design even wider tuning ranges are possible. The 1.25 mA per stage design target was not met due to ground shifts and other difficulties with the test IC.

Also demonstrated in figure 7.2 are the results of using additional load capacitance to modify the VCO center frequency. This topic was discussed in section 6.2.4. Equation (149) in that section showed that by varying the added load capacitance at the

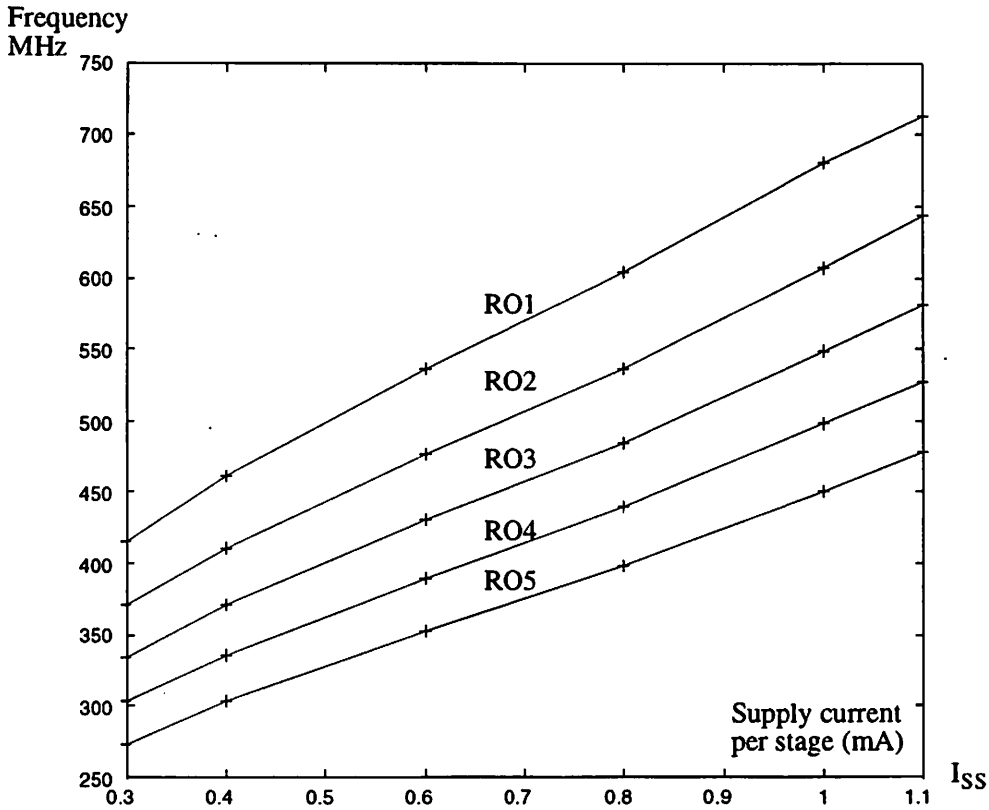

Figure 7.2 Ring oscillator test array center frequencies vs. supply current (coarse tuning; V_{SW} set by replica bias loop)

output of each stage, the VCOs operating range could be adjusted to the desired band of frequencies.

The VCO tuning path used to control the center frequency of the VCO in a PLL was described in sections 6.2.3 and 6.3.1. VCO gain and tuning range measurements for the 800 MHz VCO are illustrated in figure 7.3[1]. A VCO gain of 8.5 MHz/ V is realized for the low-gain mode and 33.4 MHz/V for the high-gain mode. The VCO gain for the latter is approximately four times larger, consistent with its factor of four larger control current. The tuning ranges are 8 MHz and 28 MHz respectively. The VCO gain and tuning range are slightly lower than the predicted values from chapter 6 due to the fact that

1. A curve tracer was not available for this measurement. Unevenness in the measurements are partially due to non-idealities in the test setup.

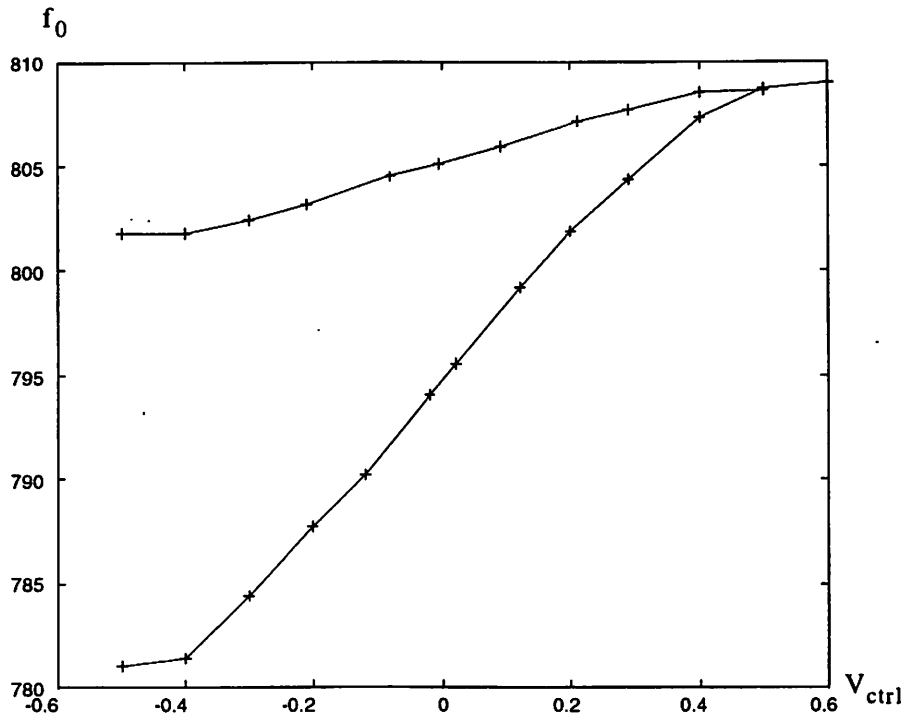

Figure 7.3 VCO gain measurements for programmable gain oscillator.

the VCO center frequency used here is 800 MHz, while the VCO control path was designed around a nominal 880 MHz. Equation (147) from chapter 6 predicts a correction factor of 10%. With this factor the measured results here are very close to the predicted values.

The 800 MHz VCO was coarse-tunable over a range of 580 to 1100 MHz. The high frequency VCO covered a range of 0.9GHz to 1.6GHz with nominal bias conditions, lower than expected due to excessive wiring parasitics. An output frequency of 1.7Ghz was attainable with a supply voltage of 4.0V. Measurements for the high frequency VCO where hampered by complications with the output buffer. A differential 50 ohm driver was used to bring the VCO signals off chip [117]. An additional multi-stage buffer is required between the ring and the driver stage to buffer that stage's relatively high load capacitance. (Similar buffers are required to drive the divider and/or mixer

inputs when the VCO is used in a frequency synthesizer application). DC offsets in the cascaded buffer sections were amplified to near saturation for the last stage. This effect can be overcome for frequencies where the AC gain of the buffer chain is near that of the DC gain. At high frequencies, however, the output power of the buffers are greatly reduced, approaching one at the high end of expected range of output frequencies.

7.2 Jitter and Phase Noise Results

In this section the timing jitter and phase noise predictions of chapter 5 will be investigated with a combination of simulations and experimental results. The two key equations from that chapter which formed the basis for a lot of the discussion on low-jitter and low-phase noise design techniques are repeated below. These equations link timing jitter and phase noise to delay cell design parameters. They also predict how timing jitter and phase noise depend on the center frequency of the oscillator and the offset frequency of interest.

$$\overline{\Delta t_{vco}}^2 = \frac{kT}{I_{SS}} \cdot \frac{a_v \xi^2}{2(V_{GS} - V_T)} \cdot T_0 \tag{153}$$

$$S_\phi(f_m) = \left(\frac{f_0}{f_m}\right)^2 \bullet \left(\frac{a_v \xi^2 \cdot kT}{2I_{SS}(V_{GS} - V_T)}\right) \tag{154}$$

Ideally, two arrays of test structures could be used to verify these equations: one array spanning a range of different center frequencies and the second covering a range of different power consumption levels. Both measurement and simulation results would be desired. Practical limitations, however, have limited the scope of this investigation to simulation results for timing jitter and experimental results for phase noise. Simulation is used to explore the improvement in timing jitter with higher power

consumption, for a fixed output frequency. And phase noise measurements are made for an array of test structures with fixed power consumption and varying center frequency.

Measurement of cycle-to-cycle timing jitter for the thermal noise induced levels seen here is not possible. Timing jitter can often be inferred from measurements of the net timing jitter between two edges as a function of edge separation. This approach was taken successfully in [118]. The noise floor of this measurement approach, however, was significantly above that which was needed for this investigation, even with a good sampling scope like the Tektronix 11801. This is partly due to the higher frequencies involved (resulting in lower absolute jitter), as well as the use of on-chip biasing circuitry. Measurements for an array of test oscillators with a fixed output frequency and variable power consumption levels were also attempted. This array was at a high center frequency though (1.5G), and the dynamic range of the measurement was limited by the VCO buffer problem described earlier.

7.2.1 Transient Noise Simulations

Simulation tools for analyzing oscillator phase noise and timing jitter have been evolving over the past several years. Most of these simulators, however, are only accurate for resonance based oscillators, such as LC-tanks, and have difficulty with relaxation and ring oscillators. This investigation uses a novel, monte-carlo bases transient noise simulation technique to measure timing jitter in ring-oscillators and delay chains. The simulation is run with a conventional SPICE based simulator. This approach is significantly slower than that of commercial based simulators and because of its "brute-force" nature it can only handle a few noisy devices at a time. The absolute accuracy of this technique is not certain either, but it has proven to be very useful in comparing timing jitter performance of different ring oscillator configurations as well as the relative contributions of the various noise sources in the ring-oscillator delay cell. Simulation of phase noise with this technique is not practical, unfortunately, due to the long simu-

lation times needed.

The transient noise simulation uses a random noise sources for each of the thermal noise current sources (output referred) in the devices which make up a ring-oscillator or delay chain. The random noise inputs begin with a sequence from a random number generator. This sequence is converted into a set of 10ps samples of the noise current by multiplying it with $\sqrt{4kT\gamma g_m \alpha}$ for the NMOS transistors and $\sqrt{4kT\gamma g_{d0} \alpha}$ for the triode PMOS loads. The transconductance (or drain-to-source conductance) is determined from the actual transistor in question for each sample point by biasing two replica transistors in a sub-circuit and measuring the change in current for a small difference in applied gate voltage (drain voltage). Best simulation results are obtained when the replica devices are stripped of un-necessary capacitor parasitics to avoid unintentional transient effects. A transient analysis is then run in which cycle-to-cycle delay is measured for multiple cycles of oscillation. The standard deviation of this delay is taken to be the r.m.s. timing jitter.

The piecewise constant noise source created in this simulation resembles the output of a sampling stage with a zero-order-hold transfer function. This is illustrated in figure 7.4. The scaled samples from the random number generator have a variance of

$$\sigma^2 = 4kT\gamma g_m \cdot \alpha \tag{155}$$

where α is a factor which is yet to be described. If the samples of the random number generator are uncorrelated then the power spectral density of the signal is white with a constant height of

$$S_x(f)/\Delta f = 4kT\gamma g_m \cdot \alpha \tag{156}$$

These samples are convolved with a zero order hold of width T_n, where T_n = 10ps in this case. The fourier transform of this transfer function is a sin(f)/f signal with height T_n and a first zero-crossing of $f = 1/T_n$.In this case f = 100GHz. The output spec-

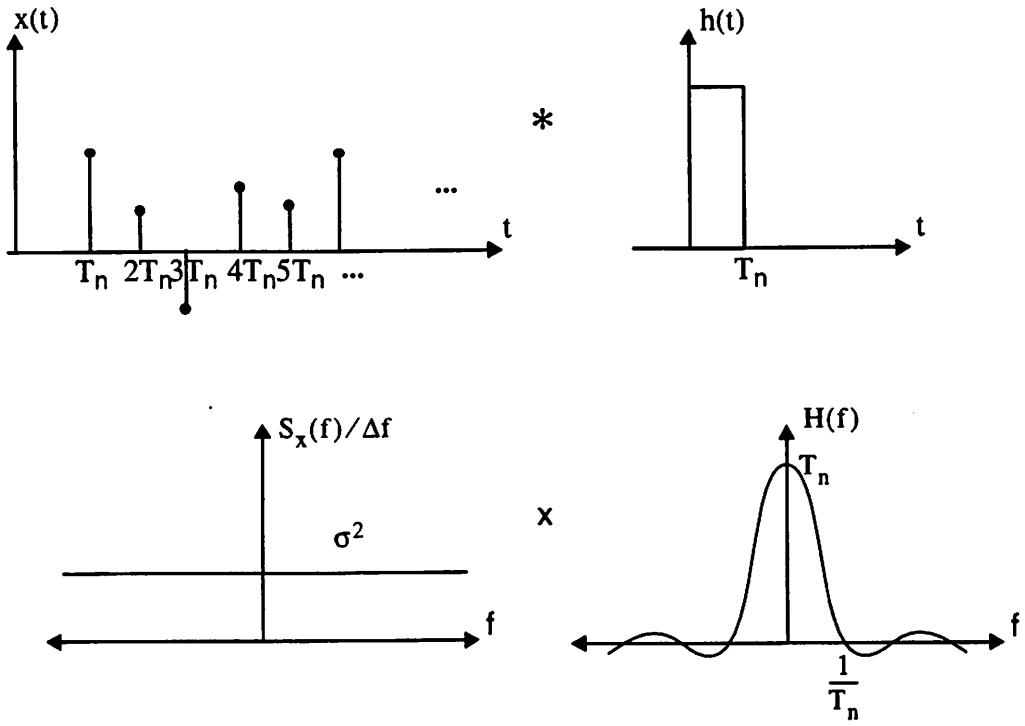

Figure 7.4 Output spectrum for piecewise constant current noise source

trum of such a signal is found from multiplying the white power spectrum of x(t) with the fourier transform of the zero-order hold. The resulting spectrum is a good approximation to white noise for frequencies $f \ll 1/T_n = 100GHz$. For correct scaling the factor α needs to be set to $1/T_n$.

A further complication in transient noise simulations is the variation in time-step selection by the SPICE simulation engine. This variation was found to produce timing jitter on the order of that expected for the devices under test, even when random noise sources where not included. Simulations where performed at enhanced current noise levels to exceed the numerical noise floor of spice. The cycle-to-cycle jitter measured for simulations with 100 times and 10 times larger noise levels yielded variances which differed by a factor of 10, as would be expected from theory. A similar ratio was assumed to be accurate for extrapolation of jitter measured from a 10X noise simulation to a 1X noise level.

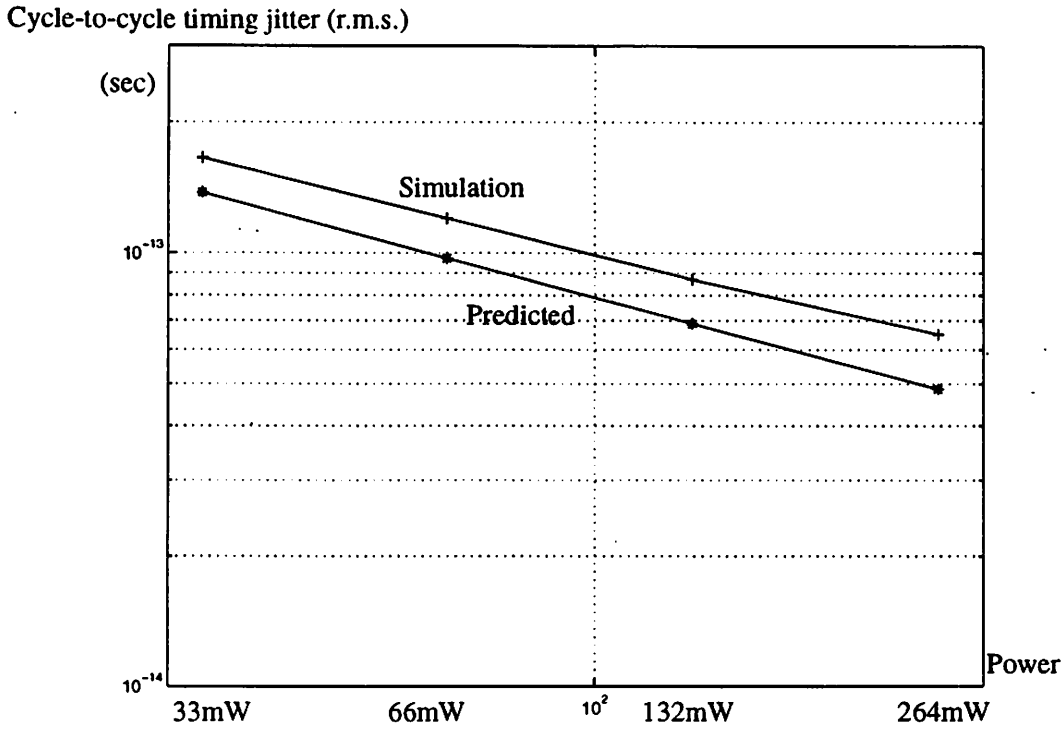

Figure 7.5 VCO timing jitter simulation results

Timing jitter simulations were carried out for an array of four ring-oscillators with a center frequency of 1.78 GHz. The current consumption for the base ring was 1.25ma per stage, using the same basic stage as described in section 6.3. With a 3.3V supply and four inverter stages per ring, the total power consumption is 33mW. The other rings were scaled up from the base ring by factors of 2, 4, and 8 respectively. Scaling was achieved through parallel cells of the same current density, meaning a corresponding increase in area and power consumption. The results of these simulations are shown in figure 7.5.

These results indicate that timing jitter improves with the square root of power consumption as predicted. The cycle-to-cycle timing jitter for the base ring design, with 1.25 mA per stage is 166 fs. Thereafter the jitter improves with the square root of the increase in power consumption, following a line with slope 1/2 in log-log space. The

Parameter	Value	Comments
I_{SS}	1.25 mA	base cell
a_v	1.7	key design target - verified with simulation
T_o	562 ps	from simulation
$V_{GS} - V_{TN}$	369 mV	
kT	$4.11 \cdot 10^{-21}$	room temperature

Noise Contribution Factor				
$\xi^2 = 2\gamma_1 + 2\gamma_3 a_v \cdot \lambda_{a2}(2t_d) + \gamma_5 a_v \sqrt{2\alpha}(1+\beta) \cdot \lambda_{b2}(2t_d)$				ξ^2 contribution
PMOS loads	$\gamma_1 = 1$			2
NMOS diff. pair	$\gamma_3 = 2/3$	$\lambda_{a2}(2t_d) = 0.76$		1.72
NMOS Current source	$\gamma_5 = 2/3$	$\lambda_{b2}(2t_d) = 0.24$	$\alpha = 3.6$ $\beta = 0$	0.73
				Total = 4.45

$$\Delta t_{vco} = \sqrt{\frac{kT}{I_{SS}} \cdot \frac{a_v \xi^2}{2(V_{GS} - V_T)}} \cdot T_0 = 137.6 \text{ fs}$$

Figure 7.6 Delay cell design parameters for timing jitter calculations

predicted timing jitter for the base ring design is 137 fs, which is lower by only 19%. The discrepancy in surprisingly small considering the number of approximations involved in producing equation (153). The parameter values used to generate the predicted results are given in figure 7.6. This result is quite sensitive to the selection of parameter values, however. For example, the $(V_{GS}-V_T)$ bias point used in the calculation was determined from the bias current and devices sizes rather than the loose approximation in equation (135). A $(V_{GS}-V_T)$ bias point of 588mV would be predicted

using that equation, resulting in an r.m.s. jitter of only 109 fs - lower by a factor of 41%. Aside from concerns over absolute numbers, however, the results in figure 7.5, demonstrate that timing jitter improves with higher power consumption, as predicted.

Simulations for this array were also used to compare the relative contributions of the different noise sources in the delay cell. These results are shown in figure 7.7.

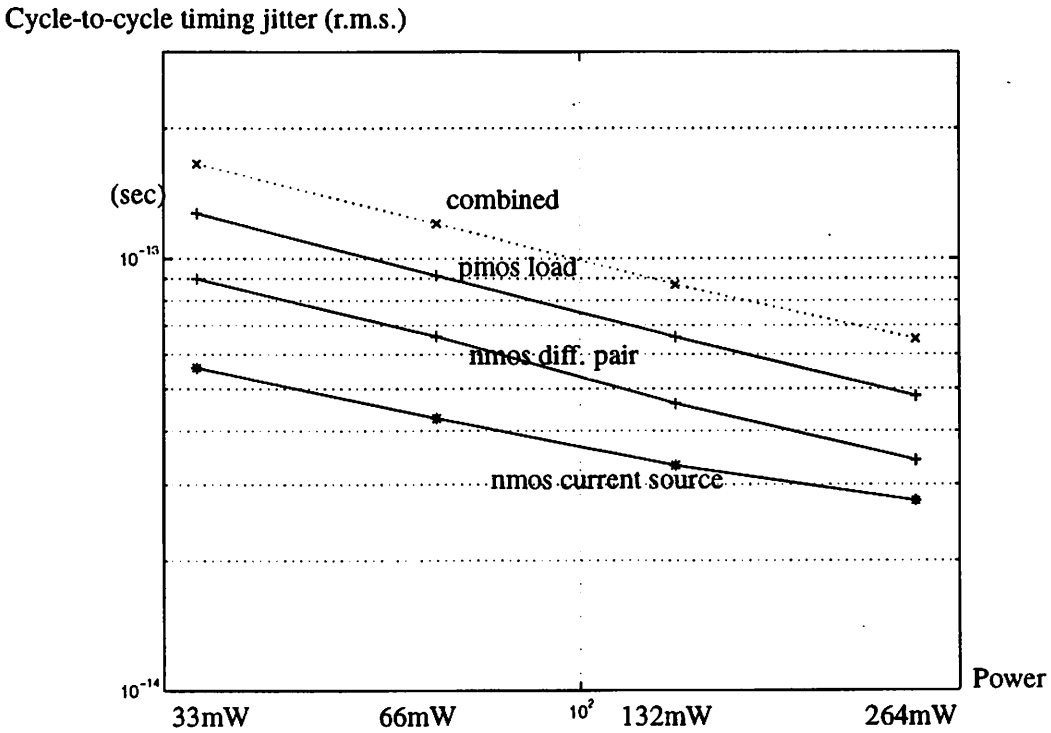

Figure 7.7 Relative noise contribution simulation results

The PMOS load transistor contribution was somewhat higher than expected. Its r.m.s. timing jitter contribution for the base stage was 127 fs as opposed to the 90 fs contribution for the NMOS diff. pair transistors - a factor of 1.4. This is significantly larger than the difference calculated in figure 7.6. The jitter contribution of the NMOS current source transistors is significantly lower than that of the other two sources, as expected. Its value compared to that of the diff pair transistors is on target. With an r.m.s. jitter contribution of 56 fs for the base case, it comes in at a factor of 1.6 below that of the

NMOS diff. pair. The predicted ratio is $\sqrt{1.72/0.73} = 1.54$.

7.2.2 Phase Noise Measurements

Ring oscillator phase noise measurements for the test array shown in figure 7.1 have been performed to characterize the dependence of phase noise on oscillator center frequency and offset frequency. The goal is to verify the predictions of equation (154) for a group of rings with identical biasing conditions for the delay cells, but varying center frequency due to different capacitive loads between stages. Phase noise is expected to decrease by 6dBc/Hz per octave increase in offset frequency and expected to improve by a similar factor for decreases in the center frequency of oscillation.

Good comparison between ring oscillators running at different frequencies requires good matching of the biasing conditions between different structures in the test array. Best results were obtained for a lower bias current than the target current of 1.25 mA per stage used in simulation. This was due in part to ground shift considerations which were minimized with lower supply current. Running at a lower supply current also results in a lower output frequency which helps to alleviate dynamic range concerns due to the buffer problem discussed earlier. For these reasons, the test array was biased with a current of 400uA per stage with a 3.3v supply. This corresponds to a power consumption of 5.3 mW per ring (buffers excluded). The output frequencies in this case are 463, 412, 372, 357, and 304 MHz respectively.

Measurement of phase noise for free-running oscillators is more difficult than for VCO's that are locked to a stable low frequency reference in a PLL. Excessive low frequency phase noise or drift can upset the stability of the measurement, especially for low offset frequencies which require more time to measure. The on-chip bias current generator used by the test array had a small bypass capacitor on-chip which did not sufficiently reduce low frequency 1/f noise. An added external bypass network was required to improve the stability to the point that phase noise for reasonable offsets

could be measured. Phase noise was measured for 500kHz, 1MHz, 1.7MHz and 3.4MHz offsets, the latter two corresponding to the first and second neighboring channel frequencies in a DECT cordless phone transceiver, as described in chapter 3.

Phase noise measurements were performed with an HP 8560 RF spectrum analyzer. Direct measurement of phase noise from the oscillator's power spectrum is possible for the high levels of phase noise present in a ring-oscillator. Other measurement techniques using frequency discriminators or phase detectors are often required for lower phase noise levels [119, 120]. A numerical correction factor is required, however, to account for a number of effects which accompany direct spectrum phase noise measurements. These include a noise power bandwidth correction factor which subtracts from the measured result and a log display mode and envelope correction factor which adds. These effects are described in [120]. The net result for the conditions in this test setup is a +1.5 dBc/Hz correction factor (i.e. phase noise is higher than measured value !).

The results of the phase noise measurements, with the correction factor added, are shown in figure 7.8 for each of the five test oscillators. As predicted by equation (154), phase noise falls off at around 6 dBc/Hz per octave increase in offset frequency. The measured value for the high frequency oscillator (R01), for example, falls 17dBc/Hz from 500kHz to 3.4 MHz. This corresponds to a slope of 6.1 dBc/Hz per octave (20.4 dBc/Hz per decade). The relative behavior of the oscillators in the test array, however, is not as good as expected. Phase noise does improve for lower center frequencies, as predicted, but there is considerable skew in the measured results. This can be attributed to a number of factors. For one, ground shift differences result in different biasing levels for the oscillators in the array, even with the relatively low current levels seen here[2]. In addition, the oscillation frequency for the rings in the test

2. A post-mortem simulation shows ground drops due to supply line sheet resistance as high as 75mV between different oscillators in the test array.

array are not in uniform steps (these are determined by the convergence of a number of biasing factors). The phase noise measurements seem to be considerably lower for the two lower frequency oscillators. A spread of 3.7 dBc/Hz is expected between the high frequency and low frequency oscillator, but the actual difference is around 6 dB. This may be due to problems in the measurement set up which favor measurements at a lower frequency. Perhaps this is related to the low-frequency phase drift present in VCO's which are not locked to a reference.

The absolute values in figure 7.8 are somewhat higher than those predicted by equation (154). Calculation of the predicted phase noise values is done with the delay cell parameters shown in figure 7.9. The value of the noise contribution factor, ξ^2, depends on the assumed values for γ_3 and γ_5 in the NMOS current sources. As discussed in chapter 4, the value of γ is 2/3 for a long-channel MOS device but can be

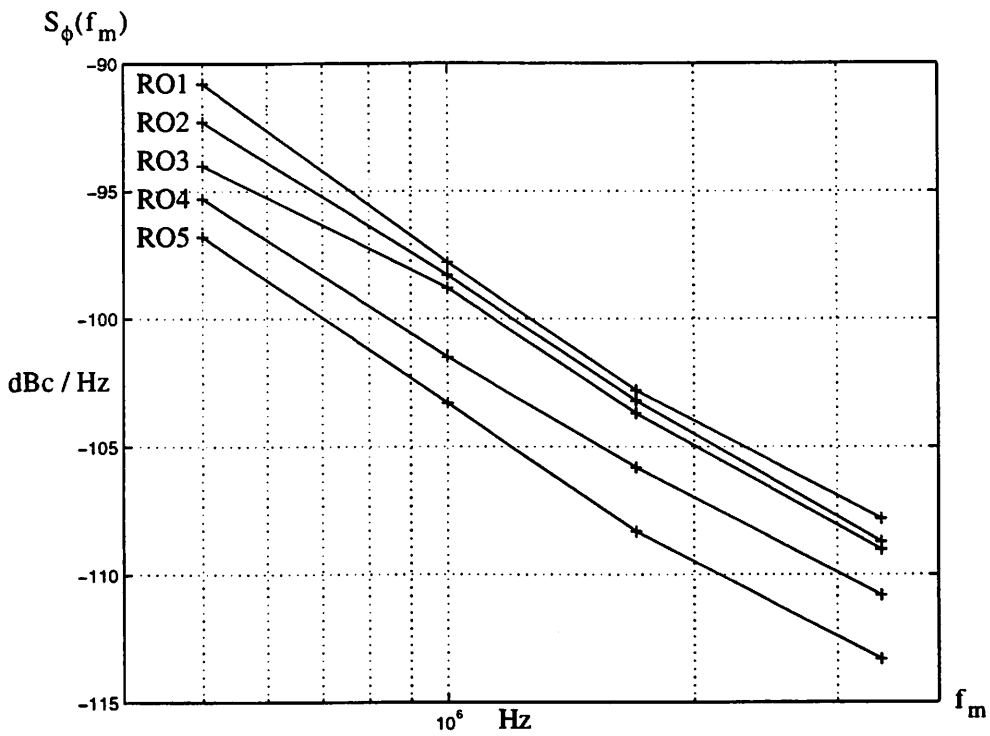

Figure 7.8 Ring oscillator phase noise measurements

Parameter	Value	Comments
I_{SS}	0.4 mA	(lower than in timing jitter simulations)
a_v	3.0	$a_v = g_m R_L \equiv K/(\sqrt{I_{SS}})$
$V_{GS} - V_{TN}$	208 mV	from drain-source current equation
kT	$4.11 \cdot 10^{-21}$	room temperature

Noise Contribution Factor				
$\xi^2 = 2\gamma_1 + 2\gamma_3 a_v \cdot \lambda_{a2}(2t_d) + \gamma_5 a_v \sqrt{2\alpha}(1+\beta) \cdot \lambda_{b2}(2t_d)$				ξ^2 contribution
PMOS loads	$\gamma_1 = 1$			2
NMOS diff. pair	$\gamma_3 = 2/3$	$\lambda_{a2}(2t_d) = 0.76$		3.04
NMOS Current source	$\gamma_5 = 2/3$	$\lambda_{b2}(2t_d) = 0.24$	$\alpha = 3.6$ $\beta = 0.2$	1.55
				Total = 6.59

If $\gamma_3 = \gamma_5 = 1$, then $\xi^2 = 8.89$ ----> + 1.3 dBc/Hz

f $\gamma_3 = \gamma_5 = 2$, then $\xi^2 = 15.8$ ----> + 3.8 dBc/Hz

$$S_\phi(f_m) = \left(\frac{f_0}{f_m}\right)^2 \bullet \left(\frac{a_v \xi^2 \cdot kT}{2I_{SS}(V_{GS} - V_T)}\right)$$

Figure 7.9 Delay cell design parameters for phase noise calculations

as high as 1 or 2 when biasing conditions make short channel effects important for a device. In this analysis a conservative value of $\gamma = 2/3$ will be assumed. The noise contribution factors for the cases of $\gamma = 1$ and $\gamma = 2$ are shown to be higher by 1.3 dBc/ Hz and 3.8 dBc/Hz respectively, corresponding to a simple shift in the phase noise sidebands. Figure 7.10 shows a comparison of the predicted and measured results for the highest frequency oscillator (RO1) and the lowest frequency oscillator (RO5) in the

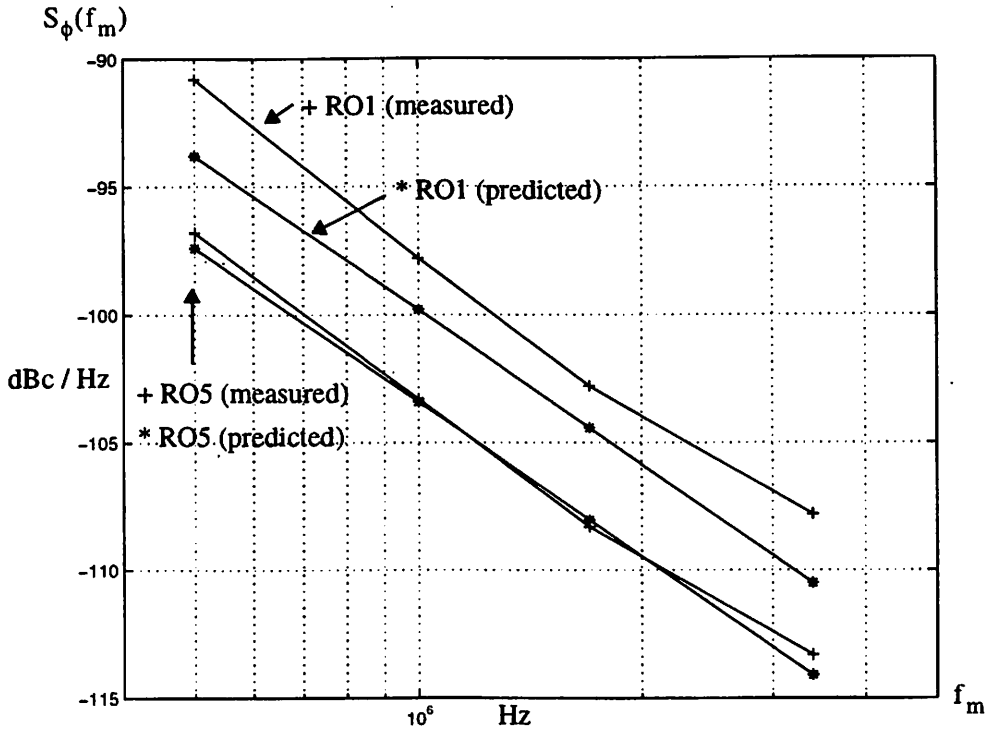

Figure 7.10 Predicted vs. measured phase noise for R01 and R05

test array. With the parameter values used in figure 7.9, the predicted results for RO5 are very close measured. The predicted values for R01 are about 3 dBc/Hz lower than measured, consistent with the wider spread between low and high frequency oscillators described previously. Although it is clear that the matching between predicted and measured results depends on a number of approximations and assumptions (e.g. the estimate of γ), the predictions of equation (154) are remarkably close. This equation predicts the right dependence of phase noise with offset frequency as well as the trend of reduced phase noise for lower center frequencies.

7.3 References

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Chapter 8

Conclusions

Timing jitter and phase noise are important design considerations in almost every type of communications system. Yet the desire for high levels of integration in many communications applications works against the minimization of these, and other, sources of timing error - especially for systems which employ a phase-locked loop for timing recovery or frequency synthesis. This thesis has explored the fundamental performance limits of delay-cell based VCOs and buffers in PLL systems. It has successfully tied the design parameters for delay cells and ring-oscillators to the thermal noise-induced timing jitter and phase noise performance in such systems. With this understanding it is possible to explore the applicability of delay cell based VCOs and delay chains to a number of different communication applications. Their usefulness in clock and data recovery applications, where they are commonly employed today, is confirmed with the timing jitter predictions of chapters four and five, as well as the simulation results in chapter seven. And their potential for at least some range of RF frequency synthesizer applications, where the thermal noise of the VCO is often the limiting factor, has been demonstrated as well. Furthermore, the minimization of phase noise and timing jitter in a system through careful consideration of design trade-offs at the delay cell level, the VCO level and the PLL level has been described.

The main contributions of this thesis have been the following:

1. A careful analysis of thermal-noise-induced jitter in delay cells, taking into account interstage amplification and time-varying noise sources, resulting in the predictions of equations (90), (98), (102). Namely, that timing jitter is inversely proportional to the square root of the capacitance at the output of each inverter and inversely proportional to the gate-source bias above threshold of the source-coupled devices in the balanced state.

2. The application of this analysis to low-timing-jitter, low-phase-noise design techniques for buffers, ring-oscillator VCOs, and phase-locked-loops. Timing jitter and phase noise performance for each of these applications have been tied together. Improvements of 10 dB per decade increase in power consumption (and area) are predicted for a fixed output period. Timing jitter, for a fixed output period and power consumption, have been shown to be minimized in a ring-oscillator with a minimum number of delay cells.

3. The design and implementation of ring oscillator VCOs using differential source-coupled, resistively loaded, CMOS delay cells has been described, including issues such as coarse and fine tuning, maximum frequency of operation, and design techniques for low frequency VCOs.

4. Experimental and monte-carlo simulation results for a ring-oscillator test array fabricated in a 0.6μ, double-poly double-metal CMOS process are described, which show good agreement with the analytical predictions for timing jitter and phase noise.

The numerical predictions and experimental results in this thesis indicate that with proper design the timing jitter in ring oscillators can be kept small enough for many communication systems. Although the phase noise of ring oscillators is higher than for those employing on-chip LC tanks, this work has shown that for at least some range of RF transceiver applications a ring oscillator may be used for the VCO in RF frequency synthesizer designs. With reasonable power consumption a ring-oscillator

VCO has been shown to be capable of the phase noise performance requirements for DECT cordless telephony (chapter three). And, with the design trade-offs available in the delay cell, the oscillator, the synthesizer, and even the radio receiver as a whole, the opportunity to apply this work to even more restrictive standards in the future is a worthwhile goal.

Appendix A

Autocorrelation Function Analysis for Time-varying Noise Sources

This appendix serves as a complement to the analysis in section 4.2.3. Included here is the complete derivation of output voltage noise in inverter delay cells with time-varying noise sources. This analysis includes evaluation of the key integrals from section 4.2.3 as well as clarification of noise modeling issues.

The class of circuits considered here are source-coupled differential delay cells with resistive loads, where the loads are realized by PMOS transistors in the triode region. A typical delay cell, including device thermal noise sources is shown in figure A.1. For a noise source whose power spectral density changes over time (not wide-sense stationary [121]), the output noise is determined through the convolution integral in (157):

$$R_{vv}(t_1, t_2) = R_{ii}(t_1, t_2) \otimes h(t_1) \otimes h(t_2) \tag{157}$$

This equation shows that the output voltage noise autocorrelation function equals the autocorrelation function for a given noise source convolved with the impulse response seen by the noise source when referred to the output. Since we are dealing with probabilistic, rather than deterministic signals, autocorrelation functions are used

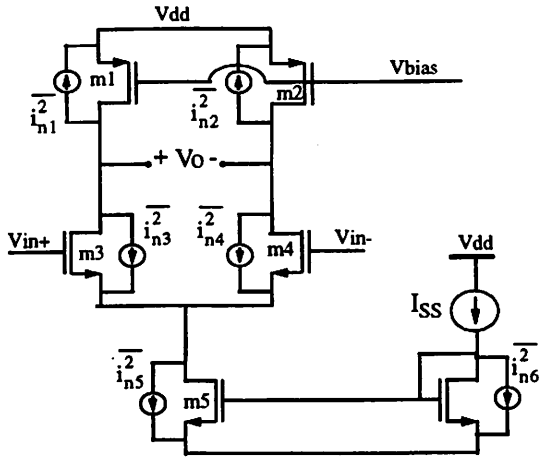


Figure A.1 Differential delay cell with noise sources (repeat of figure 4.5).

to represent noise processes, and a "double" convolution is performed. This integral can be expressed as:

$$R_{vv}(t_1, t_2) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h(\tau_1)h(\tau_2)R_{ii}(t_1-\tau_1, t_2-\tau_2)d\tau_2 d\tau_1 \tag{158}$$

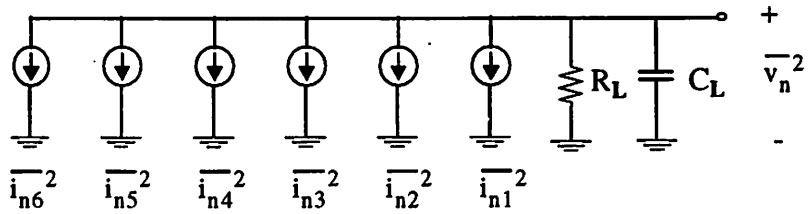
In section 4.2.3 an equivalent small-signal AC circuit for analyzing the differential voltage noise at the output of an inverter cell was proposed, and is repeated below in figure A.2. This impulse response of this circuit for a current source referred to the output is given by

$$h(t) = \frac{1}{C_L} e^{\frac{-t}{R_L C_L}} u(t) \tag{159}$$

Also shown in figure A.2 are the assumed values for the noise source power spectral densities during both regions of the switching transient. With these assumptions, the autocorrelation function for the noise sources can be expressed as follow.

For the NMOS differential pair current sources (M3,M4):

$$R_{ii}(t_1, t_2) = \begin{cases} 0 & \text{for } t_1, t_2 \le t_a \\ 2kT\gamma_3 g_{m3}\delta(t_1 - t_2) & \text{for } t_a \le t_1, t_2 \le t_c \\ 0 & \text{for } t_1, t_2 \ge t_c \end{cases} \tag{160}$$



Noise Source Approximations

Noise generator	Region I ($t_a < t < t_c$)	Region II ($t < t_a$ or $t > t_c$)
$\overline{i_{n1}}^2, \overline{i_{n2}}^2$	$4kT\gamma_1(1/R_L)\Delta f$	$4kT\gamma_1(1/R_L)\Delta f$
$\overline{i_{n3}}^2, \overline{i_{n4}}^2$	$4kT\gamma_3 g_{m3}\Delta f$	0
$\overline{i_{n5}}^2$	0	$4kT\gamma_5 g_{m5}\Delta f$
$\overline{i_{n6}}^2$	0	$4kT\gamma_5\beta g_{m5}\Delta f$

Figure A.2 Small-signal equivalent circuit for computing AC differential output voltage noise in inverter delay cell

where t_a and t_c are the beginning and ending points of the switching transient for the first stage, as shown previously (figure 4.9 in section 4.2.3). The autocorrelation function shows the correlation in the current noise at times t_1 and t_2. If either t_1 or t_2 is outside of the region ($t_a < t < t_c$) then the correlation is zero since at one of those times the noise source is off. If both t_1 or t_2 are in this region, then the autocorrelation function is given by an impulse at $t_1 = t_2$. This is the typical autocorrelation function for a white noise process. Recall that the autocorrelation function is the fourier transform of the power spectral density. A white noise source has a constant p.s.d. for all frequencies, which transforms to a delta function in the time domain (autocorrelation function).

Double-sided / Single-sided noise spectrum

The height of the delta function in equation (160) is proportional to 2kT, rather

than 4kT as it was for the power spectral density given in figure A.2. This has to do with the issue of double-sided versus single-sided noise spectrums. In the first pass analysis of section 4.2.2, single-sided noise p.s.d.'s were used. This is the typical approach in AC circuit noise analysis [122]. In this case the output voltage noise due to a current noise source is determined by

$$\overline{v_{on}}^2 = \int_0^\infty \overline{i_{n1}}^2(f)\left|H_1(f)\right|^2 df \tag{161}$$

where the integration limits are from 0 to ∞. The correct p.s.d. for the noise source in this case is the single-sided version, proportional to 4kT, as shown in figure A.3(a). If

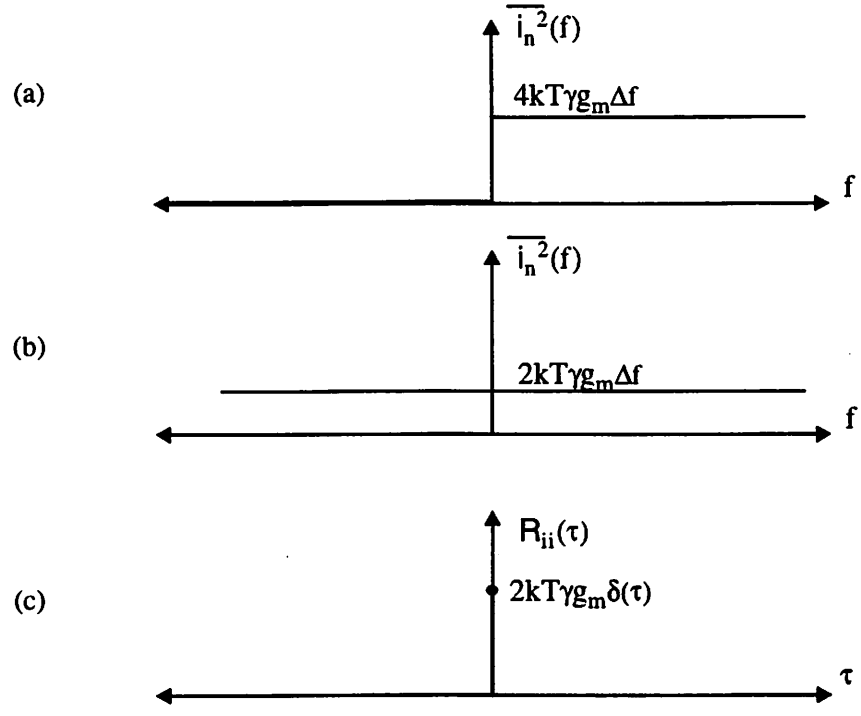


Figure A.3 Noise power spectral density and autocorrelation functions for : (a) single-sided noise representation, (b) double-sided noise representation, (c) equivalent autocorrelation function

the integration limits in (161) were to include the range $-\infty$ to ∞, then the p.s.d. in figure A.3(b) would be appropriate, and would yield the same answer in noise calcula-

tions. The autocorrelation function for the noise process is found from the fourier transform of the double-sided noise spectrum in (b) and also has a height proportional to 2kT. To check for correctness, the noise for a simple R-C circuit with noisy resistor can be calculated using both (161) and the time domain approach in (157). The correct answer for the noise variance is the familiar expression KT/C. This result is obtained with the time domain approach if an impulse proportional to 2kT is used for the noise in the resistor rather than 4kT.

The autocorrelation functions for the other noise sources can be expressed in a form similar to (160). For the current source and biasing transistors (M5,M6):

$$R_{ii}(t_1, t_2) = \begin{cases} 2kT\gamma_5 g_{m5}\delta(t_1 - t_2) & \text{for } t_1, t_2 \le t_a \\ 0 & \text{for } t_a \le t_1, t_2 \le t_c \\ 2kT\gamma_5 g_{m5}\delta(t_1 - t_2) & \text{for } t_1, t_2 \ge t_c \end{cases} \tag{162}$$

The autocorrelation function for M6 includes an additional factor of β, equal to the ratio of its transconductance relative to M5. The PMOS load transistors are approximated by the same value for both regions and, hence, are constant. The autocorrelation function in this case be expressed as

$$R_{ii}(\tau) = 2kT\gamma_1\left(\frac{1}{R_L}\right)\delta(t_1 - t_2) \tag{163}$$

Computing Output Voltage Noise Variance

Using the autocorrelation functions for the noise sources, just determined, and the system transfer function given in (159), the output voltage noise can be determined from the convolution integral in (158). As described in section 4.2.3, the voltage noise variance, which is now a function of time, can be determined from the autocorrelation function:

$$\overline{v_n}^2(t_1) = R_{vv}(t_1, t_1) = E\{V^2(t_1)\} \tag{164}$$

For the NMOS differential pair noise sources with the autocorrelation function given in (160), the convolution integral is:

$$R_{vv}(t_1,t_2) = \int_{t_1-t_c}^{t_1-t_a} h(\tau_1) \int_{t_2-t_c}^{t_2-t_a} h(\tau_2) 2kT\gamma g_m \delta[(t_1-\tau_1)-(t_2-\tau_2)]d\tau_2 d\tau_1 \qquad (165)$$

where the limits have integration have been determined from

$$\left.\begin{aligned} t_a \le t_1-\tau_1 \le t_c \\ t_a \le t_2-\tau_2 \le t_c \end{aligned}\right\} \Rightarrow \begin{cases} t_1-t_c \le \tau_1 \le t_1-t_a \\ t_2-t_c \le \tau_2 \le t_2-t_a \end{cases} \qquad (166)$$

To simplify the math which follows, a time origin of $t_a = 0$ will be assumed; that is, the time at which the first differential pair begins strongly switching will be considered time zero. Substituting the impulse response in (159), we have

$$R_{vv}(t_1,t_2) = \int_0^{t_1}\left[\frac{1}{C_L}e^{\frac{-\tau_1}{R_LC_L}}\right]\int_0^{t_2}\left[\frac{1}{C_L}e^{\frac{-\tau_2}{R_LC_L}}\right]2kT\gamma g_m\delta[(t_1-\tau_1)-(t_2-\tau_2)]d\tau_2 d\tau_1 \qquad (167)$$

The new lower integration limits come from the $u(\tau_1)$ and $u(\tau_2)$ terms in $h(\tau_1)$ and $h(\tau_2)$. We will choose to focus on the noise at times $t_1, t_2 \le t_c$, in which case $t_1 - t_c \le 0$ and $t_2 - t_c \le 0$. Simplifying (167),

$$R_{vv}(t_1,t_2) = \frac{2kT\gamma g_m}{C_L^2}\int_0^{t_1} e^{\frac{-\tau_1}{R_LC_L}}\left[e^{\frac{-1}{R_LC_L}\tau_1}\, e^{\frac{-1}{R_LC_L}(t_2-t_1)}\right]d\tau_1 \qquad (168)$$

This step involves the "sifting property" of the delta function. This integral is valid if

$(t_2-t_1)+\tau_1 \ge 0$, or ,

$\tau_1 \ge t_1 - t_2$

For the case that $t_1 - t_2 \le 0$, a lower limit of 0 is used for the integral in (168) and this equation further simplifies to:

$$R_{vv}(t_1,t_2) = \frac{2kT\gamma g_m}{C_L^2}\left(e^{\frac{-1}{R_LC_L}(t_2-t_1)}\right)\int_0^{t_1} e^{\frac{-2}{R_LC_L}\tau_1}\, d\tau_1 \qquad (169)$$

$$R_{vv}(t_1, t_2) = \frac{kT\gamma g_m R_L}{C_L}\left(e^{\frac{-1}{R_L C_L}(t_2 - t_1)}\right)\left[1 - e^{\frac{-2}{R_L C_L}t_1}\right] \tag{170}$$

If $t_1 - t_2 \geq 0$ then the lower limit of the integration in (168) is $t_1 - t_2$ rather than 0. In this case, the final result is similar and can be shown to be

$$R_{vv}(t_1, t_2) = \frac{kT\gamma g_m R_L}{C_L}\left(e^{\frac{-1}{R_L C_L}(t_1 - t_2)}\right)\left[1 - e^{\frac{-2}{R_L C_L}t_2}\right] \tag{171}$$

This is very similar to (170), except that $t_1 - t_2$ has replaced $t_2 - t_1$.

So in general

$$R_{vv}(t_1, t_2) = \frac{kT\gamma g_m R_L}{C_L}\left(e^{\frac{-1}{R_L C_L}|t_2 - t_1|}\right)\left[1 - e^{\frac{-2}{R_L C_L}t}\right] \tag{172}$$

Therefore the value of the autocorrelation function for voltage depends on the magnitude of the separation of t_1 and t_2 and not on the sign. Also, the autocorrelation function grows exponentially towards a constant with time. Note that the value of t in the last part of (172) is actually the smaller of t_1, t_2.

The voltage noise variance that results from this equation is

$$\overline{v_{n3,4}}^2(t) = R_{vv}(t, t) = \frac{kT\gamma_3 g_{m3} R_L}{C_L}\left[1 - e^{\frac{-2}{R_L C_L}t}\right] \tag{173}$$

where the subscript 3 has been added to γ and g_m to denote the correct noise source. The implications of equation (173) are discussed in section 4.2.3. The rising exponential term in this equation is given the name of the "noise evolution factor". This term is

$$\lambda_a(t) = \left[1 - e^{\frac{-2}{R_L C_L}t}\right] = \left[1 - e^{-2\left(\frac{t}{t_d}\right)}\right] \tag{174}$$

where t_d, the time delay per stage is shown to be related to R_L and C_L.

The voltage noise variance at the output of the inverter due to the current source and biasing transistor noise sources (M5,M6) can also be computed using the autocorrelation function in (162). At this point, we are interested in the noise at the output of the inverter for times $t>t_a$, due to the current noise that was present for the time $t<t_a$. In this case the noise can be determined as follows[1]. The convolution integral is:

$$R_{vv}(t_1,t_2) = \int_{t_1-t_a}^{\infty} h(\tau_1) \int_{t_2-t_a}^{\infty} h(\tau_2) 2kT\gamma g_m \delta[(t_1-\tau_1)-(t_2-\tau_2)]d\tau_2 d\tau_1 \qquad (175)$$

where the limits have integration have been determined from

$$\left.\begin{aligned} t_1-\tau_1 \le t_a \\ t_2-\tau_2 \le t_a \end{aligned}\right\} \Rightarrow \begin{cases} \tau_1 \ge t_1-t_a \\ \tau_2 \ge t_2-t_a \end{cases} \qquad (176)$$

Once again a timing origin of $t_a = 0$ will be used for simplicity.

$$R_{vv}(t_1,t_2) = \int_{t_1}^{\infty}\left[\frac{1}{C_L}e^{\frac{-\tau_1}{R_LC_L}}\right]\int_{t_2}^{\infty}\left[\frac{1}{C_L}e^{\frac{-\tau_2}{R_LC_L}}\right]2kT\gamma g_m\delta[(t_1-\tau_1)-(t_2-\tau_2)]d\tau_2 d\tau_1 \qquad (177)$$

To determine the noise for $t_1, t_2 \ge 0$, the lower integration limits in (177) are used, which are more exclusive of the limits of zero that come from the $u(\tau_1)$ and $u(\tau_2)$ terms in $h(\tau_1)$ and $h(\tau_2)$. Simplifying (167),

$$R_{vv}(t_1,t_2) = \frac{2kT\gamma g_m}{C_L^2}\int_{t_1}^{\infty} e^{\frac{-\tau_1}{R_LC_L}}\left[e^{\frac{-1}{R_LC_L}\tau_1}\, e^{\frac{-1}{R_LC_L}(t_2-t_1)}\right]d\tau_1 \qquad (178)$$

where the "sifting property" of the delta function has been used again. This integral is valid if $(t_2-t_1)+\tau_1 \ge t_2$, or $\tau_1 \ge t_1$, which is consistent with the already established lower integration limit.

Therefore

$$R_{vv}(t_1,t_2) = \frac{2kT\gamma g_m}{C_L^2}\left(e^{\frac{-1}{R_LC_L}(t_2-t_1)}\right)\int_{t_1}^{\infty} e^{\frac{-2}{R_LC_L}\tau_1}\, d\tau_1 \qquad (179)$$

---

1. The noise envelope for times $t > t_c$ is not of interest now. The equations which follow will be correct for determining voltage noise for times in the range of $t_a < t < t_c$.

$$R_{vv}(t_1, t_2) = \frac{kT\gamma g_m R_L}{C_L}\left[e^{\frac{-1}{R_L C_L}(t_2 - t_1)}\right]\left[e^{\frac{-2}{R_L C_L}t_1}\right] \tag{180}$$

This result is valid for $t_2 \geq t_1$. In the case that $t_1 \geq t_2$, the autocorrelation for the noise source in equation (162) should be written as $\delta(t_2 - t_1)$, in which case the result in (180) is the same, except that t_1 and t_2 are reversed.

Therefore the autocorrelation function for the NMOS current source and biasing transistors is given by

$$R_{vv}(t_1, t_2) = \frac{kT\gamma g_m R_L}{C_L}\left[e^{\frac{-1}{R_L C_L}|t_2 - t_1|}\right]\left[e^{\frac{-2}{R_L C_L}t}\right] \tag{181}$$

This is nearly the same as the result for the NMOS differential pair transistors in (172), except that the rising exponential is replaced by a decaying one with the same time constant. The voltage noise variance at the output can now be expressed as

$$\overline{v_{n5}}^2(t) = R_{vv}(t, t) = \frac{kT\gamma_5 g_{m5} R_L}{C_L}\left[e^{\frac{-2}{R_L C_L}t}\right] \tag{182}$$

The result for M6 is the same, with the additional factor of β, included.

This result has a very simple interpretation, as described in section 4.2.3. Namely, the voltage noise at the output is at a constant level at time zero, defined by its equilibrium value when the differential pair is fully switched. As the switching region is entered, where the noise current source is approximated as zero, the voltage noise decays exponentially towards zero. The second term in (182) is the "noise evolution factor" for these noise sources, and is denoted

$$\lambda_b(t) = e^{\frac{-2}{R_L C_L}t} = e^{-2\left(\frac{t}{t_d}\right)} \tag{183}$$

Notice that the voltage noise is proportional to $g_{m5}R_L$. This is not the same as

the interstage gain, $a_v = g_{m3}R_L$. When equation (182) is used, however, it is often convenient to use the following substitution

$$g_{m5}R_L = a_v \cdot \sqrt{2\alpha} \tag{184}$$

where α is the ratio of the size (W/L) of the current source transistors to the size of the transistors used in the differential pair. The factor of $\sqrt{2}$ is due to the larger current flowing through the current source, than through the differential pair transistor in the balanced case.

The final pair of noise sources to consider are those of the PMOS load transistors (M1,M2). The autocorrelation function for these noise sources is given in (163). These noise sources are modeled as constant, and the voltage noise for them could be determined directly in the frequency domain. The response can also be found in the autocorrelation function domain, however, with the same approach taken for the other noise sources. Using this approach, the convolution integral is given by:

$$R_{vv}(t_1, t_2) = \int_0^\infty \left[\frac{1}{C_L} e^{\frac{-\tau_1}{R_L C_L}}\right] \int_0^\infty \left[\frac{1}{C_L} e^{\frac{-\tau_2}{R_L C_L}}\right] 2kT\gamma_1 \left(\frac{1}{R_L}\right) \delta[(t_1 - \tau_1) - (t_2 - \tau_2)] d\tau_2 d\tau_1 \tag{185}$$

Using the sifting property of the exponential we have

$$R_{vv}(t_1, t_2) = \frac{2kT\gamma_1}{R_L C_L^2} \left(e^{\frac{-1}{R_L C_L}(t_2 - t_1)} \right) \int_0^\infty e^{\frac{-2}{R_L C_L}\tau_1} d\tau_1 \tag{186}$$

Accounting for the cases of $t_2 \geq t_1$ and $t_1 \geq t_2$, as before, gives

$$R_{vv}(t_1, t_2) = \frac{kT\gamma_1}{C_L} \left(e^{\frac{-1}{R_L C_L}|t_2 - t_1|} \right) \tag{187}$$

The voltage noise variance is therefore given by a constant, as expected

$$\overline{v_{n1,2}}^2(t) = R_{vv}(t, t) = \frac{kT}{C_L} \cdot \gamma_1 \tag{188}$$

References

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Appendix B

Autocorrelation Function Analysis with Interstage Gain Considerations

This appendix serves as a complement to the analysis in section 4.2.4. It extends the analysis in appendix A, where output voltage noise was computed for a small signal, AC circuit with time varying noise sources. In this appendix, the effects of interstage gain are taken into account, as described in section 4.2.4, with a more complicated, second-order, circuit for computing the output, differential voltage noise. This circuit is shown in figure B.1.

The goal of this appendix is to find the output voltage noise, as a function of time, for each of the noise sources described previously when applied to the small-signal equivalent circuit below. The total output voltage noise variance is given by the superposition of the responses due to each of these independent noise sources. The autocorrelation function approach described in appendix A is used again in this analysis.

The impulse response of the circuit in figure B.1 is given by $h(t) = h_1(t) \otimes h_2(t)$ where

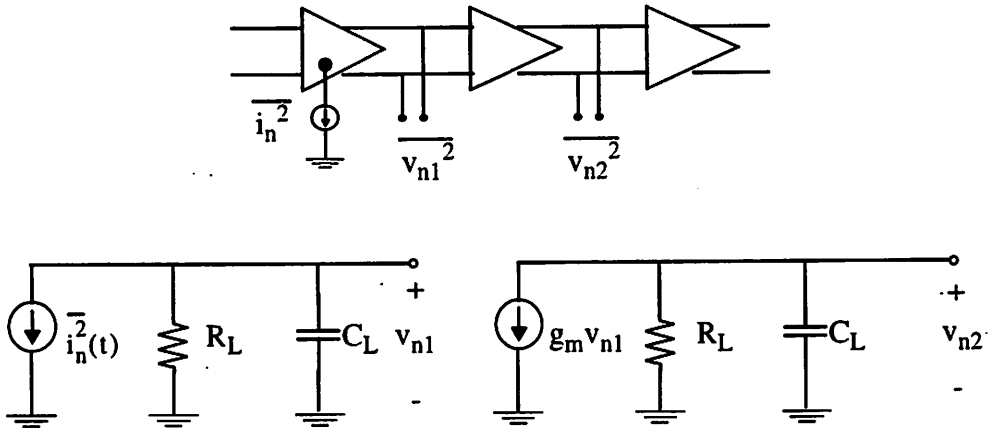

Figure B.1 Extended circuit model for interstage interaction

$$h_1(t) = \frac{1}{C_L} e^{\frac{-t}{R_L C_L}} u(t) \tag{189}$$

and

$$h_2(t) = \frac{g_m}{C_L} e^{\frac{-t}{R_L C_L}} u(t) \tag{190}$$

This convolution can be evaluated as

$$h(t) = \int_{-\infty}^{\infty} \frac{1}{C_L} e^{\frac{-1}{R_L C_L}\tau} u(\tau) \cdot \frac{g_m}{C_L} e^{\frac{-1}{R_L C_L}(t-\tau)} u(t-\tau) d\tau \tag{191}$$

The $u(\tau)$ and $u(t-\tau)$ limits require $\tau \geq 0$ and $\tau \leq t$ respectively.

$$h(t) = \frac{g_m}{C_L^2} \cdot e^{\frac{-1}{R_L C_L}t} \cdot \int_0^t e^{\frac{-1}{R_L C_L}\tau} \cdot e^{\frac{-1}{R_L C_L}\tau} d\tau = \frac{g_m}{C_L^2} \cdot e^{\frac{-1}{R_L C_L}t} \cdot \int_0^t d\tau \tag{192}$$

For $t \geq 0$ the value in the integral evaluates to simply t. For $t < 0$ it equals 0. Therefore

$$h(t) = \frac{g_m}{C_L^2} \cdot t \cdot e^{\frac{-t}{R_L C_L}} u(t) \tag{193}$$

The autocorrelation function of interest here, is that for the noise voltage at the output of the second linear stage. This is given by the input current noise autocorrelation function convolved with the combined impulse response h(t).

$$R_{vv}(t_1, t_2) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h(\tau_1)h(\tau_2)R_{ii}(t_1 - \tau_1, t_2 - \tau_2)d\tau_2 d\tau_1 \quad (194)$$

Noise contribution of PMOS load transistors

The first set of noise sources to consider are the PMOS load transistors. These noise sources are modeled as a constant in both regions of operation, as described in appendix A. The convolution approach in (194) can be used here, but for variety, the voltage noise variance will be solved in the frequency domain. The single-sided noise power spectral density for the current noise generators in M1 and M2 is given by

$$\overline{i_n}^2(f) = 4kT\gamma_1(1/R_L)\Delta f \quad (195)$$

And the output voltage noise variance is found from

$$\overline{v_{on}}^2 = \int_0^{\infty} \overline{i_{n1}}^2(f)\left|H_1(f)\right|^2 df \quad (196)$$

where $H_1(f)$ is the transfer function of the noise source referred to the output. With the simple RC circuit described in section 4.2.2, the output voltage noise was just

$$\overline{v_{on}}^2 = \frac{kT}{C_L}\cdot\gamma_1 \quad (197)$$

In this case, the noise source is applied to the second order circuit in figure B.1. At first glance, one might expect an output noise variance that was a_v^2 times the value at the output of the first stage. But this neglects the additional filtering of the second RC stage.

If the noise source in (195) is applied to the second order circuit considered here, then (196) is equal to

$$\overline{v_{on(1,2)}}^2 = \int_0^{\infty} 4kT\gamma_1\frac{1}{R_L}\left|\frac{R_L}{1 + j2\pi R_L C_L}\right|^2\left|\frac{g_m R_L}{1 + j2\pi f R_L C_L}\right|^2 df \quad (198)$$

If the 3-db bandwidth of a single RC stage is denoted

$$f_0 = \frac{1}{2\pi R_L C_L} \tag{199}$$

then,

$$\overline{v_{on(1,2)}}^2 = 4kT\gamma_1 g_m^2 R_L^3 \int_0^\infty \left[\frac{1}{1+(f/f_0)^2}\right]^2 df \tag{200}$$

The definite integral in (200) is more complicated than the one considered for the first order analysis. Using an integral form from [124], its solution can be shown to be

$$\int_0^\infty \left[\frac{1}{1+(f/f_0)^2}\right]^2 df = f_0^4 \cdot \left[\frac{f_0^{-3}}{2} \cdot \frac{\Gamma(1/2)(\Gamma(3/2))}{\Gamma(2)}\right] \tag{201}$$

or

$$\int_0^\infty \left[\frac{1}{1+(f/f_0)^2}\right]^2 df = \frac{f_0}{2} \cdot \frac{\sqrt{\pi}(\sqrt{\pi}/2)}{1} = \frac{\pi}{4} \cdot f_0 \tag{202}$$

Therefore, the voltage noise variance is given by

$$\overline{v_{on(1,2)}}^2 = 4kT\gamma_1 a_v^2 R_L \left(\frac{\pi}{4} \cdot \frac{1}{2\pi R_L C_L}\right) \tag{203}$$

or

$$\overline{v_{on(1,2)}}^2 = \frac{kT}{C_L} \cdot \gamma_1 \cdot \frac{a_v^2}{2} \tag{204}$$

The factor of $a_v^2/2$ in equation (204) shows the effect of considering the noise at the output of the second stage. We will find consistent results for the other two sets of noise sources. This analysis yields more insight into its origin, however. For a general small-signal noise source applied to the input of the second stage, the output power would be a_v^2 times larger at the output. In this case, however, the bandwidth of the combined circuit is determining how much noise power is integrated. The two pole system

here has a sharper roll-off, and lower 3-db frequency than that for a one pole system. This analysis shows that effective noise bandwidth is reduced in this case by a factor of two. Combining the power gain with the reduced noise bandwidth gives a net increase of $a_v^2/2$ in the voltage noise at the output of the second stage.

Noise contribution of NMOS differential pair transistors

The autocorrelation functions for the current noise generators are assumed to be the same as in appendix A. The NMOS differential pair transistors (M3,M4) have a noise autocorrelation function of

$$R_{ii}(t_1,t_2) = \begin{cases} 0 & \text{for } t_1,t_2 \le 0 \\ 2kT\gamma g_m \delta(t_1-t_2) & \text{for } t_a \le t_1,t_2 \le t_c \\ 0 & \text{for } t_1,t_2 \ge t_c \end{cases} \tag{205}$$

In this case, the output voltage autocorrelation function is

$$R_{vv}(t_1,t_2) = \int_{t_1-t_c}^{t_1} h(\tau_1) \int_{t_2-t_c}^{t_2} h(\tau_2) 2kT\gamma g_m \delta[(t_1-\tau_1)-(t_2-\tau_2)]d\tau_2 d\tau_1$$

where a time origin of t_a=0 is assumed, and the mapping of the limits in (206) has been used again

$$\left.\begin{aligned} 0 \le t_1-\tau_1 \le t_c \\ 0 \le t_2-\tau_2 \le t_c \end{aligned}\right\} \Rightarrow \begin{cases} t_1-t_c \le \tau_1 \le t_1 \\ t_2-t_c \le \tau_2 \le t_2 \end{cases} \tag{206}$$

Since $t_1-t_c \le 0$ and $t_2-t_c \le 0$, the u(τ) terms in $h(\tau_1)$ and $h(\tau_2)$ restrict the lower limits to 0.

$$R_{vv}(t_1,t_2) = \int_0^{t_1}\left[\frac{g_m}{C_L^2}\cdot\tau_1\cdot e^{\frac{-1}{R_LC_L}\tau_1}\right]\int_0^{t_2}\left[\frac{g_m}{C_L^2}\cdot\tau_2\cdot e^{\frac{-1}{R_LC_L}\tau_2}\right] 2kT\gamma g_m \delta[\tau_2-(t_2-t_1)-\tau_1]d\tau_2 d\tau_1$$

To simplify the equations which follow the following constants will be defined.

$$b = 2kT\gamma g_m\left(\frac{g_m}{C_L^2}\right)^2$$

and

$$a = \frac{1}{R_L C_L}$$

Using the "sifting property" of the delta function, this integral evaluates to

$$R_{vv}(t_1, t_2) = b\int_0^{t_1}[\tau_1 \cdot e^{-a\tau_1}][(t_2 - t_1) + \tau_1][e^{-a(t_2 - t_1)} \cdot e^{-a\tau_1}]d\tau_1 \qquad (207)$$

provided that

$$0 \le (t_2 - t_1) + \tau_1 \le t_2$$

or equivalently

$$t_1 - t_2 \le \tau_1 \le t_1$$

We will first consider the case that $t_1 - t_2 \le 0$ in which case the lower limit of 0 for τ_1 is already more restrictive. The other condition $t_1 - t_2 \ge 0$ can also be evaluated, as in the analysis for the first order system in the previous section, yielding the other part of the result. The combined result gives an autocorrelation function $R_{vv}(t_1, t_2)$ which is proportional to the magnitude of $|t_2 - t_1|$ only and not the sign.

Continuing the evaluation of (207) we have

$$R_{vv}(t_1, t_2) = be^{-a(t_2 - t_1)}\int_0^{t_1}[(t_2 - t_1)\tau_1 + \tau_1^2][e^{-2a\tau_1}]d\tau_1 \qquad (208)$$

This integral can be broken up into two parts.

$$R_{vv}(t_1, t_2) = X + Y \qquad (209)$$

Where

$$X = be^{-a(t_2-t_1)}\int_0^{t_1}(t_2-t_1)\tau_1[e^{-2a\tau_1}]d\tau_1 \tag{210}$$

and

$$Y = be^{-a(t_2-t_1)}\int_0^{t_1}\tau_1^2[e^{-2a\tau_1}]d\tau_1 \tag{211}$$

The integral in X can be shown to evaluate to

$$X = \frac{b(t_2-t_1)}{4a^2}e^{-a(t_2-t_1)}[(-2a\tau_1-1)e^{-2a\tau_1}]\Big|_{\tau_1=0}^{\tau_1=t_1} \tag{212}$$

or

$$X = B(t_2-t_1)[1-e^{-2at_1}-2at_1e^{-2at_1}] \tag{213}$$

Where the constant B is defined as

$$B = \frac{b}{4a^2}e^{-a(t_2-t_1)} \tag{214}$$

The second part of the integral in (208) is even more complicated. It can be evaluated as follows.

$$Y = be^{-a(t_2-t_1)}\int_0^{t_1}\tau_1^2[e^{-2a\tau_1}]d\tau_1 \tag{215}$$

In [124] the integral of $x^2 \cdot e^{-cx} \cdot dx$ is shown to be

$$\int x^2 \cdot e^{-cx} \cdot dx = \frac{-x^2}{c}e^{-cx} + \frac{2}{c}\int x \cdot e^{-cx} \cdot dx \tag{216}$$

The second part of this formula is similar to the one evaluated for X. Applying this formula to Y, expanding the second integral, and rearranging terms we can arrive at

$$Y = be^{-a(t_2-t_1)}\left[-\frac{\tau_1^2e^{-2a\tau_1}}{2a}-\frac{2\tau_1e^{-2a\tau_1}}{4a^2}-\frac{2e^{-2a\tau_1}}{8a^3}\right]\Big|_{\tau_1=0}^{\tau_1=t_1} \tag{217}$$

Evaluating (217) at the limits of integration, rearranging terms and substituting

the constant B, from before, we have

$$Y = \frac{B}{a}\left[1 - e^{-2at_1} - 2at_1 e^{-2at_1} - 2a^2 t_1^2 e^{-2at_1}\right] \tag{218}$$

Combining X and Y gives the desired output voltage noise autocorrelation function.

$$R_{vv}(t_1, t_2) = B\left((t_2 - t_1) + \frac{1}{a}\right)[1 - e^{-2at_1} - 2at_1 e^{-2at_1}] - B2at_1^2 e^{-2at_1} \tag{219}$$

This is a fairly complicated expression. Of interest here is the voltage noise variance as a function of time. This is just R_{vv} evaluated at $t_1 = t_2$. In this case

$$R_{vv}(t_1, t_1) = \frac{B}{a}[1 - e^{-2at_1} - 2at_1 e^{-2at_1} - 2a^2 t_1^2 e^{-2at_1}] \tag{220}$$

Recall that

$$B = \frac{b}{4a^2} e^{-a(t_2 - t_1)} \quad , \; b = 2kT\gamma g_m \left(\frac{g_m}{C_L^2}\right)^2 , \text{ and } a = \frac{1}{R_L C_L}$$

In this case,

$$\overline{v_{n(3,4)}}^2(t_1) = R_{vv}(t_1, t_1) = \frac{kT}{C_L} \cdot \gamma_3 a_v \cdot \frac{a_v^2}{2} \cdot \lambda_{a2}(t_1) \tag{221}$$

where λ_2 is the noise evolution factor for this second order system.

$$\lambda_{a2}(t) = [1 - [1 + 2at + 2a^2 t^2]e^{-2at}] \tag{222}$$

The noise evolution factor λ_2 is a time varying term capturing the evolution of the output noise from its value of zero at the time origin, to its final, steady state value of one. The implications of equation (221) are described in section 4.2.4.

Noise contribution of current source and biasing transistors

The autocorrelation functions for the current noise generators of the current

source and biasing transistors (M5,M6) is given by:

$$R_{ii}(t_1, t_2) = \begin{cases} 2kT\gamma_5 g_{m5}\delta(t_1 - t_2) & \text{for } t_1, t_2 \le t_a \\ 0 & \text{for } t_a \le t_1, t_2 \le t_c \end{cases} \tag{223}$$

As in appendix A, we will be not consider the noise at times $t > t_c$. In this case the convolution integral for the output voltage noise is

$$R_{vv}(t_1, t_2) = \int_{t_1}^{\infty} h(\tau_1) \int_{t_2}^{\infty} h(\tau_2) 2kT\gamma g_m \delta[(t_1 - \tau_1) - (t_2 - \tau_2)] d\tau_2 d\tau_1 \tag{224}$$

where a time origin of $t_a=0$ is assumed, and the mapping of the limits in (206) has been used again

$$\left.\begin{matrix} t_1 - \tau_1 \le 0 \\ t_2 - \tau_2 \le 0 \end{matrix}\right\} \Rightarrow \begin{cases} \tau_1 \ge t_1 \\ \tau_2 \ge t_2 \end{cases} \tag{225}$$

This expression expands to

$$R_{vv}(t_1, t_2) = \int_{t_1}^{\infty} \left[\frac{g_m}{C_L^2} \cdot \tau_1 \cdot e^{\frac{-1}{R_L C_L}\tau_1} \right] \int_{t_2}^{\infty} \left[\frac{g_m}{C_L^2} \cdot \tau_2 \cdot e^{\frac{-1}{R_L C_L}\tau_2} \right] 2kT\gamma g_m \delta[\tau_2 - (t_2 - t_1) - \tau_1] d\tau_2 d\tau_1$$

To simplify the equations which follow the constants below will be used again.

$$b = 2kT\gamma g_m \left(\frac{g_m}{C_L^2} \right)^2$$

and

$$a = \frac{1}{R_L C_L}$$

Using the "sifting property" of the delta function, this integral evaluates to

$$R_{vv}(t_1, t_2) = b \int_{t_1}^{\infty} [\tau_1 \cdot e^{-a\tau_1}][(t_2 - t_1) + \tau_1][e^{-a(t_2 - t_1)} \cdot e^{-a\tau_1}] d\tau_1 \tag{226}$$

provided that

$$(t_2 - t_1) + \tau_1 \ge t_2$$

or equivalently

$$\tau_1 \geq t_1$$

which is already an integration limit for the second integral. This integral breaks up into the same pieces as in the NMOS differential pair transistor case just considered (see equations (209),(210), and (211)). The only difference is the limits of integration. In this case

$$X = \frac{b(t_2 - t_1)}{4a^2} e^{-a(t_2 - t_1)} [(-2a\tau_1 - 1)e^{-2a\tau_1}] \Big|_{\tau_1 = t_1}^{\tau_1 = \infty} \tag{227}$$

or

$$X = B(t_2 - t_1)[2at_1 + 1]e^{-2at_1} \tag{228}$$

Similarly

$$Y = be^{-a(t_2 - t_1)} \left[-\frac{\tau_1^2 e^{-2a\tau_1}}{2a} - \frac{2\tau_1 e^{-2a\tau_1}}{4a^2} - \frac{2e^{-2a\tau_1}}{8a^3} \right] \Bigg|_{\tau_1 = t_1}^{\tau_1 = \infty} \tag{229}$$

which simplifies to

$$Y = \frac{B}{a} \left[e^{-2at_1} + 2at_1 e^{-2at_1} + 2a^2 t_1^2 e^{-2at_1} \right] \tag{230}$$

Combining X and Y gives

$$R_{vv}(t_1, t_2) = B\left((t_2 - t_1) + \frac{1}{a}\right)[1 + 2at_1]e^{-2at_1} + B2at_1^2 e^{-2at_1} \tag{231}$$

The voltage noise variance as a function of time is then given by:

$$R_{vv}(t_1, t_1) = \frac{B}{a}[1 + 2at_1 + 2a^2 t_1^2]e^{-2at_1} \tag{232}$$

With

$$B = \frac{b}{4a^2} e^{-a(t_2 - t_1)} \quad , \; b = 2kT\gamma_5 g_{m5} \left(\frac{g_{m3}}{C_L^2} \right)^2 , \text{ and } a = \frac{1}{R_L C_L}$$

this simplifies to

$$\overline{v_{n5}^2}(t_1) = R_{vv}(t_1, t_1) = \frac{kT\gamma_5 g_{m5} R_L}{C_L} \cdot \frac{a_v^2}{2} \cdot \lambda_{b2}(t_1) \tag{233}$$

Where λ_{b2} is the noise evolution factor for this second order system.

$$\lambda_{b2}(t) = [1 + 2at + 2a^2t^2]e^{-2at} \tag{234}$$

The noise evolution factor, λ_{b2}, captures the evolution of the output noise as it decays from its steady state value at the time origin, towards zero. The implications of equation (233) are described in section 4.2.4. As in appendix A, the noise voltage here is proportional to $g_{m5}R_L$, and the substitution

$$g_{m5}R_L = a_v \cdot \sqrt{2\alpha} \tag{235}$$

can be used in (233).

Finally, the system impulse response, h(t), used to determine the output noise due to the current source transistors, assumed that the transconductance of the second stage, which was proportional to G_m, was "on" for all time. A more complete analysis would correct for this assumption. In that case, a slightly different result for $\lambda_{b2}(t)$ can be derived. The expression in (234) is sufficient for our purposes here, however, and is slightly more conservative (pessimistic) than the result we would expect in the other case.

References

[124] W. Beyer, *CRC Standard Mathematical Tables, 26th Edition*, CRC Press, 1981