PROCESS VARIABILITY AND DEVICE MISMATCH

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Abstract

The different types of process variability that cause device mismatch are investigated. A model that relates the variance of mismatch with the area of the devices and the distance between them, presented for MOS transistors by M. Pelgrom et. al.[11] is adopted. It is rederived in order to examine how it could be extended to small dimension devices. Since the mechanisms that cause mismatch are the same for many different kinds of devices, modeling is examined first in general terms and then applied to individual devices. Translation of mismatch into circuit performance degradation is presented for some commonly used simple circuits.

A broad set of test structures was fabricated in the Baseline Process of the Berkeley Microfabrication Laboratory in order to: a) find the coefficients of the model discussed above, b) examine mismatch introduced by different environments around the devices and experimentally find the size and number of dummy devices needed for good matching, c) examine the effect of orientation on mismatch, and d) measure performance degradation in some simple circuits and compare with the predicted by circuit analysis. Results obtained by statistically processing electrical measurements are presented.

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Chapter 1

Introduction

1.1 Overview

The increasing requirement for a higher degree of integration and faster circuits, pushes the semiconductor industry to fabricate devices with ever smaller dimensions. Despite the sophisticated equipment used, we have limited control in processing structures so minute, and large variability in the process characteristics is introduced. The process variability causes circuit performance variability with obvious economic impact. In this thesis we attempt to acquire some insight on process variation and we focus on the variation of the behavior of identically designed devices.

This first chapter provides a short overview of the problem and presents a summary of the methods developed to cope with it. Finally the thesis organization is presented.

1.2 Process Parameter Variability

Integrated circuits consist of a number of interconnected devices (mainly Bipolar and FET transistors, resistors, and capacitors) on a silicon substrate. The devices are formed after a series of processing steps such as oxidation of silicon, deposition of metal or other materials, implantation, selective etching, etc. For the sake of simulation, the behavior of the devices can be modeled as a combination of circuit components such as ideal resistors, capacitors, inductors, and independent and dependent voltage and current sources. The value of each one of these components is a function of a set of variables called *device parameters*. Examples of device parameters are the threshold voltage of FET transistors, the device dimensions, the sheet resistance of a polysilicon line, etc. The value of each device parameter depends on physical quantities called *process parameters*. Examples of

process parameters are the thickness of the silicon oxide, the concentration of doping atoms in the silicon etc. The border between the device parameters and the process parameters is not firmly drawn. For example, the thickness of the oxide and the device dimensions can be considered both device and process parameters. The relation between process and device parameters is not explicit because it depends on factors that cannot be described with a single number, such as doping profiles, and in some cases the mechanism is not very well understood. Some of the models that circuit simulators such as SPICE use to accurately describe the devices are very complex, and some of the device parameters that they use have physical interpretations, while others do not and are empirically introduced. Generally, the device parameters of the accurate models are chosen to better match measurements of the actual device using optimization routines, rather than given as an explicit function of the process parameters [5].

The physical process parameters in a fabrication line are subject to variation. Systematic components of variation can be found across the die, across the wafer and across a whole batch. An attempt to assign different components of the variation to different pieces of the equipment has been presented before [6]. Some of the causes of variation are:

- Nonuniform implantation.
- Nonuniform deposition of a material such as photoresist, polysilicon, oxide and metal.
- Optical effects of the stepper such as diffraction, because the wavelength of the light source used is comparable to the size of the printed geometries.
- Different etching rate because of varying environment.
- Edge roughness because of etching imperfections.
- Polysilicon granularity.
- Variations of temperature, pressure, and concentration of gas in the furnace, which cause nonuniform oxidation and diffusion.
- Variation of the conditions in the plasma etching chamber, which cause non uniform plasma etching.

- Misalignment.
- Recipe modification.
- Interruption of operation of the equipment because of maintenance or cleaning.

Statistical Process Control when properly used can greatly reduce variation and increase the efficiency of the fabrication line [7]. However, it is impossible to eliminate it completely. The unavoidable variation of the physical process parameters causes variation of the device parameters and deviation form the target values. This in turn results in variation of the circuit performance.

1.3 Circuit Performance Variation

Yield is defined as the percentage of the manufactured circuits that are functional and satisfy the performance specifications. There are two factors that determine the yield, the catastrophic failures and the process variation as described in Section 1.2. The part of the yield associated with each one of those is called *catastrophic yield* and *parametric yield* respectively. Catastrophic failures are caused either by random defect spots on the wafer that result in short-circuits and open-circuits, or by failure in the operation of specific structures such as contacts or vias. The catastrophic yield is usually dominant.

It is desirable to design circuits in a way that maximizes the parametric yield. A designer's experience and intuition is needed to find a robust topology that minimizes the effect of the process fluctuation on the performance. The sensitivity of a performance F to a process or device parameter p, defined as

$$S_p^F = \frac{dF/F}{dp/p} \tag{1.1}$$

has been used extensively as a measure of the effect of this parameter to the performance. However, combinations of variations among different parameters are often significant. A direct estimation of the parametric yield using the statistics of the process variation is needed. Furthermore, it is often desirable to optimize the design by changing the nominal values of the device parameters over which the designer has control (i.e., the dimensions

of the devices) in order to maximize the parametric yield. This is referred to as design centering .

Several methods for the estimation of the parametric yield and the optimization of the design have been suggested [1]. Deterministic methods exhaustively explore the process parameter or device parameter space and have the basic disadvantage that the number of simulations needed increases exponentially with the number of the parameters. This is also known as 'the curse of dimensionality' and makes deterministic methods impractical for large circuits. Statistical methods on the other hand are based on the Monte Carlo analysis in which we repeatedly select random values for the device parameters and perform simulation. Using the actual distribution of the device parameters, emulates a pilot run in the production line. The basic advantage of the Monte Carlo analysis is that the number of simulations needed for a stipulated accuracy is independent of the number of the parameters. The accuracy, however, increases only with the square root of the number of the simulations.

Even though Monte Carlo analysis is much more efficient than the deterministic methods, the computational load required for large circuits is still impractical if high yield prediction accuracy is needed. A solution to this problem is to replace the whole circuit or a noncritical part of it with a behavioral model [3], [4]. This greatly diminishes the computational cost since the evaluation of the response of the behavioral model is much faster than the simulation. However, the use of behavioral models limits the generality of the method and reduces the accuracy of the parametric yield estimation. There exists a trade off between the generality and accuracy on the one side and the computational load on the other. The experience and intuition of the circuit designer can identify the weaknesses and the mechanisms of failure of the circuit and facilitate the statistical analysis.

Identically designed devices are often laid out close together. The proper operation of the circuit requires that they behave identically. Often the value of the device parameters is not as important for the performance as the matching among these devices. The difference in the value of a device parameter among identically designed devices is called *mismatch*.

It is related to the relative variation among the devices as opposed to the total variation over a wafer or a whole batch. Examples of circuits that need matched devices are current mirrors, where device mismatch results in current mismatch; the input differential stage of an OPAMP, where mismatch results in input offset; and many kinds of A/D converters, where mismatch introduces nonlinearities; multiplexers, etc. The subject of this thesis is the examination of the device mismatch using a set of test structures.

1.4 Thesis Organization

This thesis is organized as follows. Chapter 2 presents some theoretical background about device mismatch. It includes characterization and modeling of mismatch for MOS transistors, resistors and capacitors. Chapter 3 describes how knowledge of the statistics of mismatch can be translated to knowledge of the performance variation. Chapter 4 describes the test structures that were designed and fabricated in the Berkeley Microfabrication Laboratory in order to measure mismatch. Finally Chapter 5 describes measurement methodology and analysis of the data, and Chapter 6 presents the conclusions.

Chapter 2

Theory of Mismatch

2.1 Introduction

In this chapter we present some theoretical background about mismatch which is based mainly on [11] by Pelgrom et. al., but also on [8], [12] and [13]. While in [11], a mismatch model is derived in the spatial frequency domain, here we work in the distance domain. At the end of the chapter a possible extension of the derived models to small dimension devices is discussed.

2.2 Derivation of the Mismatch Model

Consider a pair of identically designed rectangular devices, with dimensions W by L in distance D, as shown in Figure 2.1. Generally a device parameter P is a function of the local value of n process parameters $q_1, q_2, \ldots q_n$.

$$P = f(q_1, q_2, \ldots q_n) \tag{2.1}$$

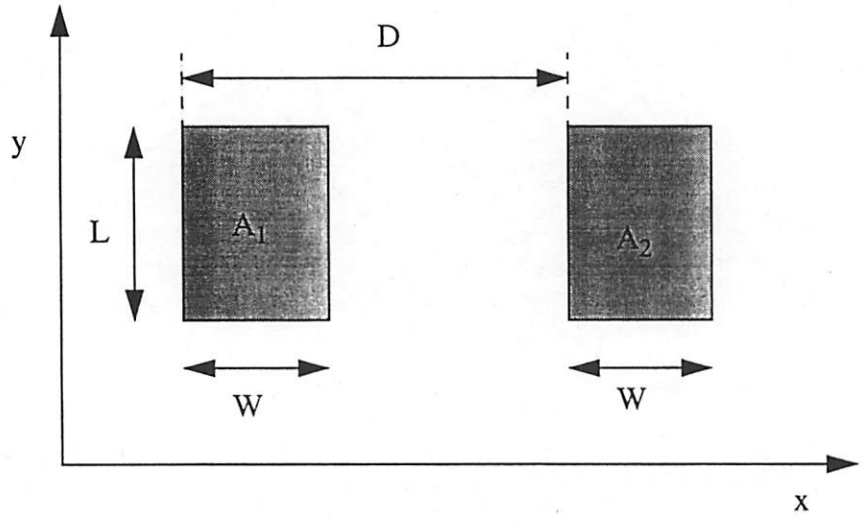


Figure 2.1 A pair of identically designed devices.

The mismatch in the device parameter P between the two devices is given by equation (2.2).

$$\Delta P \cong \frac{\partial f}{\partial q_1}\Delta q_1 + \frac{\partial f}{\partial q_2}\Delta q_2 + ... + \frac{\partial f}{\partial q_n}\Delta q_n \ , \tag{2.2}$$

where Δq_i, represents the mismatch in the local value of the process parameter q_i.

Parameters q_i represent physical quantities such as implanted ion concentration, thickness of the oxide and dimensions of the devices. Because they are introduced by different mechanisms such as implantation, oxide growth, and etching of material, they can usually be considered uncorrelated. The mismatch in the device parameter P is a random variable whose variance can be expressed as

$$\sigma^2_{\Delta P} = \left(\frac{\partial f}{\partial q_1}\right)^2 \sigma^2_{\Delta q_1} + \left(\frac{\partial f}{\partial q_2}\right)^2 \sigma^2_{\Delta q_2} + ... + \left(\frac{\partial f}{\partial q_n}\right)^2 \sigma^2_{\Delta q_n} \ . \tag{2.3}$$

If for some reason some of the q_i are correlated, correlation terms should be introduced in equation (2.3).

2.2.1 "Local value" of a Process Parameter

We referred above to the local value of the process parameter in the device as a single number, but this is actually a function of the position within the device $q_i(x, y)$. It would be more rigorous to refer to the *effective value of* q_i *in the device*, and define this as the constant value of q_i, which would give the same value for P as the function $q_i(x, y)$, when the nominal values are used for the rest of the process parameters. It is reasonable to assume that this effective value is close to the average value of $q_i(x, y)$, in the area of the device, as given by the equation

$$q_{i,eff} \cong \overline{q_i} = \frac{1}{WL}\int_0^W \int_0^L q_i(x, y)\,dx\,dy \ . \tag{2.4}$$

If q_i represents a dimension of the device, for example the length L, it is again reasonable to assume that the effective L is the average of L(x) across the width, as given below:

$$L_{eff} \cong \bar{L} = \frac{1}{W}\int_0^W L_i(x)dx \tag{2.5}$$

In order to support this claim with an example, we examine the effective value of the thickness of the oxide when the device parameter of interest is the capacitance of a poly 1 - poly 2 capacitor. The relation between the effective value of the thickness of the oxide $t_{ox,eff}$ and $t_{ox}(x, y)$, which is the function of position, is

$$\varepsilon_{ox} WL \frac{1}{t_{ox,eff}} = \int_0^{WL}\int \varepsilon_{ox} \frac{1}{t_{ox}(x, y)} dxdy, \tag{2.6}$$

where ε_{ox} is the dielectric constant of the silicon oxide. We express $t_{ox}(x, y)$, as follows

$$t_{ox}(x, y) = \overline{t_{ox}} + \omega(x, y), \tag{2.7}$$

where

$$\overline{t_{ox}} = \frac{1}{WL}\int_0^{WL}\int t_{ox}(x, y)dxdy. \tag{2.8}$$

The value of $\omega(x, y)$, which represents the variation around the average, is a small portion of the average $\overline{t_{ox}}$, and we can write

$$\int_0^{WL}\int \varepsilon_{ox} \frac{1}{\overline{t_{ox}} + \omega(x, y)} dxdy \cong \varepsilon_{ox} \frac{1}{\overline{t_{ox}}} \int_0^{WL}\int \left(1 - \frac{\omega(x, y)}{\overline{t_{ox}}}\right) dxdy = \varepsilon_{ox} WL \frac{1}{\overline{t_{ox}}} . \tag{2.9}$$

From (2.9) and (2.6) follows that

$$t_{ox,eff} \cong \overline{t_{ox}} . \tag{2.10}$$

2.2.2 Local and Global Variation

We are proceeding with an estimation of the quantities $\sigma^2_{\Delta q}$ of the equation (2.3). The difference in the effective value of the process parameter q, as given in (2.4) is

$$\Delta q = \frac{1}{A}\left[\int_{A_1} q(x, y)dxdy - \int_{A_2} q(x, y)dxdy\right], \tag{2.11}$$

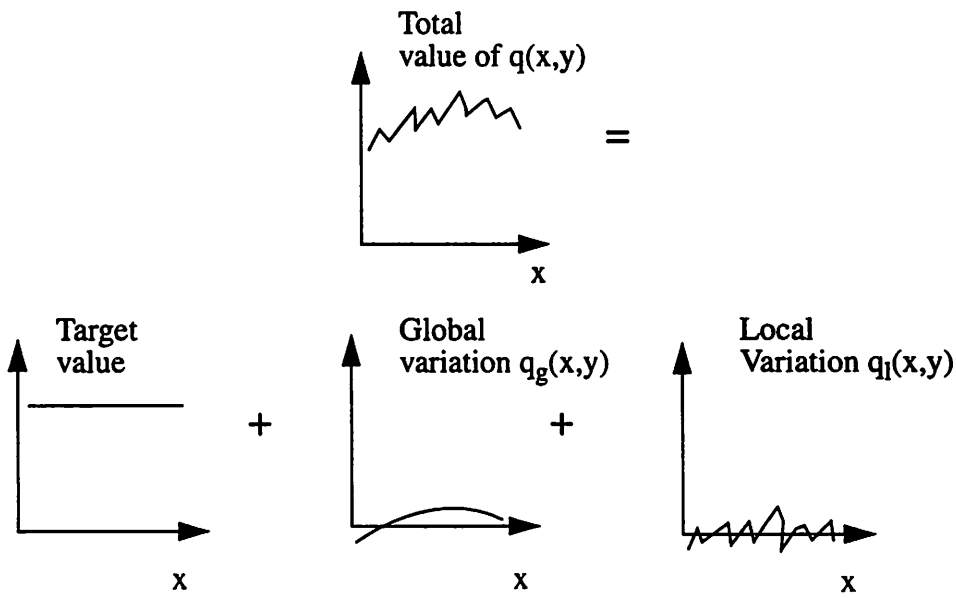


Figure 2.2 Decomposition of value of a process parameter into different components.

where A_1 and A_2 are the areas of the two devices as shown in Figure 2.1 and A=WL is the common magnitude of these areas.

There are two kinds of variation in the process parameters that cause mismatch. The first is *short correlation distance variation,* where the value of the process parameter at one point is uncorrelated with its value at any other point located further than a distance much smaller than the dimensions of the device. This kind will be referred to as *local variation* also. The spatial frequency spectrum of this component covers the whole spectrum and resembles white noise. Examples of mechanisms that cause short correlation distance variation are the grain nature of the polysilicon, the distribution of the oxide charges under the transistor gate, the distribution of ion-implanted, diffused or substrate ions, the local mobility fluctuations and the edge roughness. The second kind of process parameter variation is *large gradients of variation* across the wafer and will also be referred to as *global variation.* The spectrum of this component contains only low spatial frequencies. The two components are caused by different mechanisms and are uncorrelated. For example the global variation in the oxide thickness of poly1-poly2 capacitors is caused by temperature

or gas concentration variation across the surface of the wafer during oxidation, while the local variation is due to the granular nature of the polysilicon. The decomposition of the value of q(x,y) into the nominal (target) value, the global variation and the local variation is depicted in Figure 2.2, where only the x dimension is shown for convenience.

2.2.3 Mismatch Introduced by Local Variation

We will examine first the effect of the short correlation distance variation. $q_l(x,y)$ represents only the local variation part of the whole value of the process parameter. Equation (2.11) gives

$$(\Delta q_l)^2 = \frac{1}{A^2}\left[\left(\int_{A_1} q_l(x,y)dxdy\right)^2 + \left(\int_{A_2} q_l(x,y)dxdy\right)^2 - 2\int_{A_1} q_l(x,y)dxdy \int_{A_2} q_l(x,y)dxdy\right] . \tag{2.12}$$

The first term can be expressed as

$$\frac{1}{(WL)^2}\int_{y_b=0}^{L}\int_{x_b=0}^{W}\int_{y_a=0}^{L}\int_{x_a=0}^{W} q_l(x_a,y_a)q_l(x_b,y_b)dx_a dy_a dx_b dy_b \ . \tag{2.13}$$

We assume now that the spatial random process $q_l(x,y)$ is a wide sense stationary process so that the mean of $q_l(x,y)$ is a constant μ_{q_l} for all points (x,y), and the spatial autocorrelation between two points (x_a,y_a) and (x_b,y_b) depends only on the differences x_a-x_b and y_a-y_b:

$$R((x_a,y_a),(x_b,y_b)) \equiv E(q_l(x_a,y_a)q_l(x_b,y_b)) = R(x_a-x_b, y_a-y_b) \tag{2.14}$$

Here, R( ) is the autocorrelation function and E( ) represents the expectation of a random variable. The physical meaning of this assumption is that the random behavior of $q_l(x,y)$ is constant over the area where the two devices are laid out. We can assume that the mean μ_{q_l} is zero, because if there exists a constant shift in the value of the parameter across the wafer, this can be assigned to the global variation. The expectation of the term in (2.13) is

$$\frac{1}{(WL)^2}\int_{y_b=0}^{L}\int_{x_b=0}^{W}\int_{y_a=0}^{L}\int_{x_a=0}^{W} R(x_a-x_b, y_a-y_b)dx_a dy_a dx_b dy_b . \tag{2.15}$$

Since the correlation distance is much smaller that the device dimensions, we can replace it with an impulse function

$$R(x_a-x_b, y_a-y_b) = \sigma^2\delta(x_a-x_b, y_a-y_b), \tag{2.16}$$

where σ^2 is a positive constant. Using this and the basic property of the impulse function

$$\int_{\text{Area}} \delta(x, y)dxdy = \begin{matrix} 1 & \text{if } (0,0) \in \text{Area} \\ 0 & \text{otherwise} \end{matrix} \tag{2.17}$$

the quantity in (2.15) reduces to

$$\frac{\sigma^2}{WL} \tag{2.18}$$

The first and second terms of (2.12) both evaluate to the expression given in (2.18). Similarly, the third term of (2.12) can be expressed as

$$\frac{2}{(WL)^2}\int_{y_b=0}^{L}\int_{x_b=D}^{D+W}\int_{y_a=0}^{L}\int_{x_a=0}^{W} R(x_a-x_b, y_a-y_b)dx_a dy_a dx_b dy_b \tag{2.19}$$

Since the devices do not overlap, the equation $x_a = x_b$ cannot be satisfied in the area of integration, and, according to equation (2.17), the integral is zero. Combining the above results, the expectation of $(\Delta q_l)^2$ is

$$\sigma^2_{\Delta q_l} = \frac{S^2_{l,q}}{WL} , \tag{2.20}$$

where $S^2_{l,q} = 2\sigma^2$ is a positive constant. This equation shows that the mismatch caused by short correlation distance variation is inversely proportional to the area of the devices.

If the process parameter q is one of the dimensions, W for example, similar analysis in one dimension gives

$$\sigma^2_{\Delta W_l} = \frac{S^2_{l,W}}{L} \quad , \tag{2.21}$$

with $S^2_{l,W}$ a positive constant. This equation shows that the mismatch introduced by edge roughness of the one side is inversely proportional to the length of the other side.

2.2.4 Mismatch Introduced by Global Variation

We proceed by examining the effect of the large gradients of variation. In this section $q_g(x,y)$ represents only the global variation part of the whole value of the process parameter. We assume that the distance D between the two devices and the dimensions W and L are small enough to be able to consider that the variation is linear across the surface and it lies on a plane. Such a variation can be analyzed in two components, one parallel to the x-axis and one parallel to the y-axis, as in Figure 2.1. The y-component has the same effect on both devices and does not contribute to the mismatch. The effect of the x-component of the variation is shown in Figure 2.3. From this figure it is clear that

$$\Delta q_g = \lambda D, \tag{2.22}$$

where λ is the slope of $q_g(x)$. In the absence of knowledge of the shape of the global distribution and the location of the pair of the devices in the die and the wafer, λ can be consid-

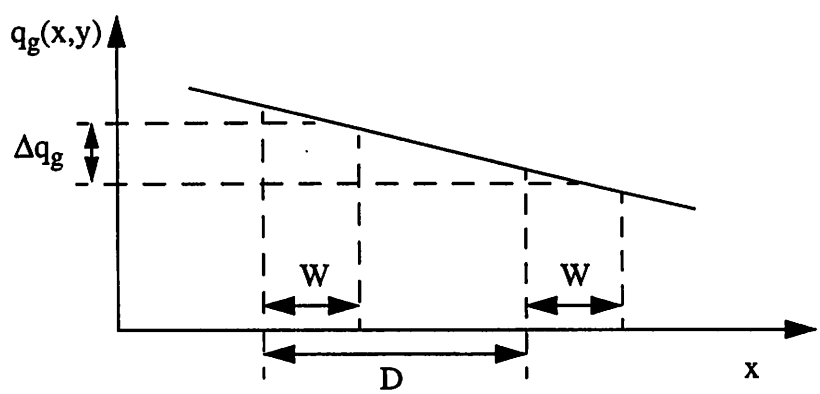


Figure 2.3 Effect of large gradient variation.

ered a zero mean random variable. A non zero mean would give a non zero mean for Δq_g. In this way previous knowledge of systematic behavior of the global variation can be used to predict the systematic part of the mismatch. Assuming that the variance of the slope is $S^2_{g,q}$ the variance of Δq_g is

$$\sigma^2_{\Delta q_g} = D^2 S^2_{g,q} \ . \tag{2.23}$$

Common centroid geometry layout is extensively used to eliminate this part of the mismatch.

2.2.5 Total Mismatch Model

Combining equations (2.20) and (2.23) we obtain the model for the variance of the combined local and global variation

$$\sigma^2_{\Delta q} = \frac{S^2_{l,q}}{WL} + D^2 S^2_{g,q} \ . \tag{2.24}$$

Of particular interest is the case at which a device parameter P does not depend on the dimensions and the process parameters on which it does depend are uncorrelated. Then the partial derivatives of relation (2.3) do not depend on W or L and a relation of the form (2.24), also holds for the device parameter:

$$\sigma^2_{\Delta P} = \frac{S^2_{l,P}}{WL} + D^2 S^2_{g,P} \ . \tag{2.25}$$

If the process parameter q is one of the dimensions, for example W, similar analysis in one dimension gives

$$\sigma^2_{\Delta W} = \frac{S^2_{l,W}}{L} + D^2 S^2_{g,W} \ . \tag{2.26}$$

Switching W and L in the above equation gives the variance for ΔL.

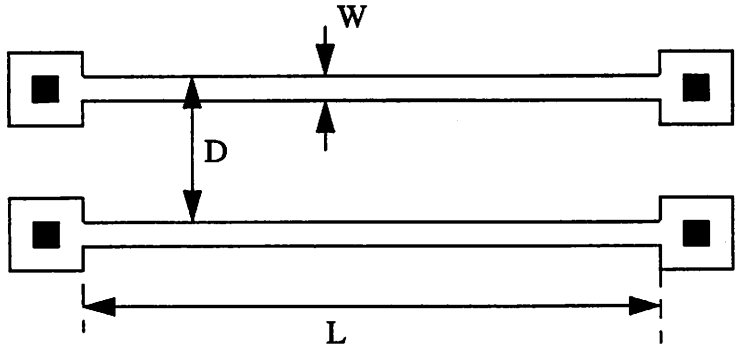


Figure 2.4 A pair of resistors.

2.3 Specific Device Mismatch Models

In this section we will apply the results of Section 2.2 in order to derive mismatch models for specific devices.

2.3.1 Resistors

Consider a pair of resistors made of polysilicon, with dimensions W and L and distance D apart as shown in Figure 2.4.

We examine resistance mismatch of the main body of the resistors, the rectangular region W and L, neglecting the resistance of the contact and the resistance of the square around it. The value of the resistance is given by

$$R = R_s \frac{L}{W}, \tag{2.27}$$

where R_s is the sheet resistance. The mismatch in the value of R is

$$\Delta R = \frac{L}{W}\Delta R_s + \frac{R_s}{W}\Delta L - \frac{R_s L}{W^2}\Delta W \ , \tag{2.28}$$

from which we obtain the relative mismatch

$$\frac{\Delta R}{R} = \frac{\Delta R_s}{R_s} + \frac{\Delta L}{L} - \frac{\Delta W}{W}. \tag{2.29}$$

The mechanism that determines ΔL can vary depending on how the resistor is connected to the rest of the circuit (with contacts, or with wide lines of the same material as the resistor, the configuration around the contact, etc.). Generally ΔL is about the same order of magnitude as ΔW, and L is much longer than W; therefore, the second term of equation (2.29) can be omitted. ΔW and ΔR_S are uncorrelated, so that (2.29) gives

$$\frac{\sigma^2_{\Delta R}}{R^2} = \frac{\sigma^2_{\Delta R_s}}{R_s^{\,2}} + \frac{\sigma^2_{\Delta W}}{W^2}. \tag{2.30}$$

The sheet resistance R_S depends on the thickness of the conducting polysilicon layer and the concentration of the implanted ions in it. These two factors are uncorrelated and do not depend on the dimensions. The variance of ΔR_S has the form of equation (2.25), and the variance of ΔW is given by (2.26). Finally (2.30) can be written as

$$\frac{\sigma^2_{\Delta R}}{R^2} = \left(\frac{S^2_{l,R_s}}{WL} + S^2_{g,R_s}D^2\right) + \frac{1}{W^2}\left(\frac{S^2_{l,W}}{L} + S^2_{g,W}D^2\right), \tag{2.31}$$

where S^2_{l,R_s}, S^2_{g,R_s}, $S^2_{l,W}$ and $S^2_{g,W}$ are positive constants for a specific technology, representing local and global variation in R_S and W. This equation shows that when keeping L and D constant, for very small W, the variation in W dominates. For large W the difference in the sheet resistance dominates. For a specific L, the value of W at which both factors contribute equally to the mismatch depends on the specific technology. By grouping together the terms of the local variation and of the global variation (2.31) becomes

$$\frac{\sigma^2_{\Delta R}}{R^2} = \frac{1}{WL}\left(S^2_{l,R_s} + \frac{S^2_{l,W}}{W}\right) + \left(S^2_{g,R_s} + \frac{S^2_{g,W}}{W^2}\right)D^2, \tag{2.32}$$

and for relatively large values of W we obtain the simplified version

$$\frac{\sigma^2_{\Delta R}}{R^2} = \frac{S^2_{l,R}}{WL} + S^2_{g,R}D^2, \tag{2.33}$$

with $S^2_{l,R}$ and $S^2_{g,R}$ positive constants characteristic of the technology.

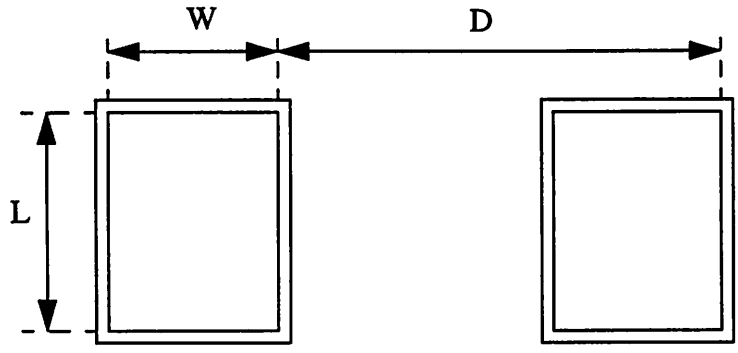


Figure 2.5 A pair of capacitors.

Diffusion resistors are voltage dependent resistors. The width of the depletion region of the reversely biased diode between the resistor and the substrate varies according to the bias of the diode. The width and the thickness vary along the resistor. The effective width and thickness of the resistor depend on the voltage at its terminals. However, for almost zero voltage in both the terminals, similar analysis with the above shows that relations (2.32) and (2.33) hold. These relations should approximately hold also, when the voltage applied to the terminals of the resistors is held constant among different pairs.

2.3.2 Capacitors

Consider a pair of poly 1 - poly 2 capacitors with dimensions W and L and distance D as shown in Figure 2.5. The value of the capacitance is given by

$$C = C_s WL, \tag{2.34}$$

where C_s is the capacitance per unit area. Similar to the case for the resistors, the relative capacitance mismatch is

$$\frac{\Delta C}{C} = \frac{\Delta C_s}{C_s} + \frac{\Delta W}{W} + \frac{\Delta L}{L}. \tag{2.35}$$

In this case W and L are determined during the same processing steps; therefore, ΔW and ΔL cannot be considered uncorrelated. Equation (2.35) gives

$$\frac{\sigma_{\Delta C}^2}{C^2} = \frac{\sigma_{\Delta C_s}^2}{C_s^2} + \frac{\sigma_{\Delta W}^2}{W^2} + \frac{\sigma_{\Delta L}^2}{L^2} + \frac{2}{WL} r_{\Delta W, \Delta L} \ , \tag{2.36}$$

where $r_{\Delta W, \Delta L}$ is the correlation between ΔW and ΔL. This can be estimated as follows. The local part of variation or the edge roughness in ΔW and ΔL is uncorrelated, since the edges with length W and L are far apart compared to the small correlation distance. Only the global variation contributes to the correlation, and its effect can be captured by means of Figure 2.3, where now q is the dimension W or L. Similarly to equation (2.22),

$$\Delta W = \lambda_W D \tag{2.37}$$

and

$$\Delta L = \lambda_L D \ , \tag{2.38}$$

where λ_W and λ_L are the slopes of the global variation of W and L.Therefore,

$$r_{\Delta W, \Delta L} = r_{\lambda_W, \lambda_L} D^2 \ , \tag{2.39}$$

where r_{λ_W, λ_L} is the correlation of λ_W and λ_L, and this correlation is independent of the distance D.

The variance of ΔW and ΔL in (2.36) is given by (2.26). The capacitance per unit area depends on the thickness of the oxide and the value of the dielectric. These factors are uncorrelated, and they do not depend on the dimensions; therefore, ΔC_s has the form of (2.25). Finally (2.36) can be written as

$$\frac{\sigma_{\Delta C}^2}{C^2} = \left(\frac{S_{l, C_s}^2}{WL} + S_{g, C_s}^2 D^2 \right) + \frac{1}{W^2} \left(\frac{S_{l, W}^2}{L} + S_{g, W}^2 D^2 \right) + \frac{1}{L^2} \left(\frac{S_{l, L}^2}{W} + S_{g, L}^2 D^2 \right) + \frac{2}{WL} r_{\lambda_W, \lambda_L} D^2 \tag{2.40}$$

where S^2_{l,C_s}, S^2_{g,C_s}, $S^2_{l,W}$, $S^2_{g,W}$, $S^2_{l,L}$ and $S^2_{g,L}$ are positive constants for a specific technology, representing the local and global variation in C_s, W and L. This equation shows that with D constant, when W is very small, its variation dominates and when L is very small, its variation dominates. For large W and L it is the variation in the capacitance per unit area that dominates. Assuming square capacitors, the common size of W and L at which the variation in the dimensions and the variation in the capacitance per unit area contribute equally to the mismatch is technology specific. By grouping together terms of local and global variation we obtain

$$\frac{\sigma^2_{\Delta C}}{C^2} = \frac{1}{WL}\left(S^2_{l,C_s} + \frac{S^2_{l,W}}{W} + \frac{S^2_{l,L}}{L}\right) + \left(S^2_{g,C_s} + \frac{S^2_{g,W}}{W^2} + \frac{S^2_{g,L}}{L^2}\right)D^2 \qquad (2.41)$$

$$+ \frac{2}{WL} r_{\lambda_W,\lambda_L} D^2 \ .$$

It is not meaningful to make one side extremely short and the reference to it is only academic. Similar analysis, however, could find application in matching the parasitic capacitance of interconnect lines.

For relatively large values of W and L, and for low correlation r_{λ_W,λ_L}, we obtain the simplified form

$$\frac{\sigma^2_{\Delta C}}{C^2} = \frac{S^2_{l,C}}{WL} + S^2_{g,C}D^2, \qquad (2.42)$$

with $S^2_{l,C}$ and $S^2_{g,C}$ positive numbers.

2.3.3 Transistors

Consider now a pair of MOS transistors with channel width W and channel length L at distance D from each other, as shown in Figure 2.6.

Neglecting the channel length modulation, the drain current I of a MOS transistor is given by

$$I = \frac{\mu C_{ox} W}{2 L}(V_{GS} - V_T)^2 \ , \qquad (2.43)$$

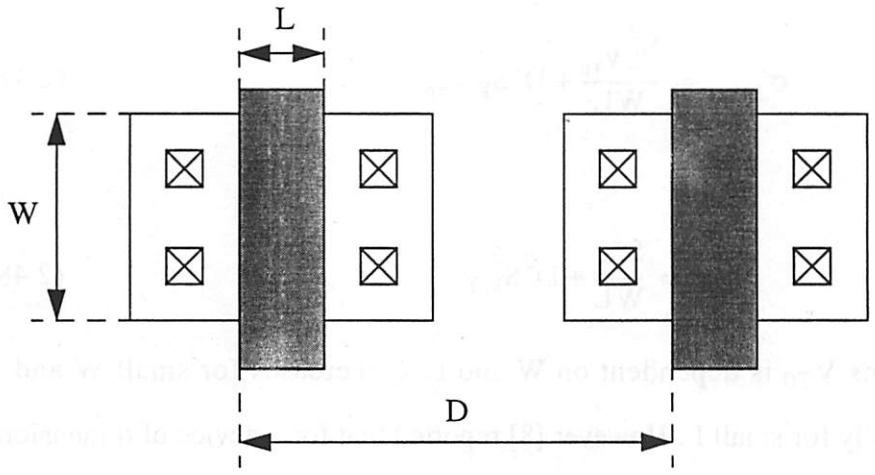


Figure 2.6 A pair of transistors.

where μ is the mobility of the silicon under the gate, C_{ox} is the gate capacitance per unit area and V_{GS} is the gate-source voltage. V_T is the threshold voltage, which is affected by the body effect:

$$V_T = V_{T0} + \gamma(\sqrt{V_{SB} + 2\Phi_P} - \sqrt{2\Phi_P}), \tag{2.44}$$

where V_{T0} is the threshold voltage without body effect, γ is the body effect factor, V_{SB} is the source-substrate voltage and Φ_P is a logarithmic function of the doping concentration of the channel which can be considered constant. Hence the current mismatch is mainly caused by mismatch in V_{T0}, γ and by the current factor

$$\beta = \frac{\mu C_{ox} W}{2 L} \quad . \tag{2.45}$$

The threshold voltage V_{T0} and the body effect factor γ are independent of W and L for relatively large dimensions. They depend on uncorrelated process parameters; therefore, the variances of V_T, V_{T0} and γ are of the form of equation (2.25):

$$\sigma^2_{\Delta V_T} = \frac{S^2_{l,\,V_T}}{WL} + D^2 S^2_{g,\,V_T} \tag{2.46}$$

$$\sigma^2_{\Delta V_{T0}} = \frac{S^2_{l,V_{T0}}}{WL} + D^2 S^2_{g,V_{T0}} \tag{2.47}$$

$$\sigma^2_{\Delta\gamma} = \frac{S^2_{l,\gamma}}{WL} + D^2 S^2_{g,\gamma} \tag{2.48}$$

For small dimensions V_{T0} is dependent on W and L. It increases for small W and it decreases exponentially for small L. However [8] reported that for a device of dimensions 2μm x 2μm the mismatch component introduced by the dimensions variation accounts only for 10% of the total threshold voltage mismatch. Therefore the model of equations (2.47) and (2.48) is valid for this range of dimensions. A discussion of threshold voltage matching of even smaller devices is included in sections 2.4 and 2.5.

The mismatch of μ and C_{ox} has the form of equation (2.25) for the same reasons. The variations in W and L are independent since W is defined when the thick oxide is etched to open the active area and L is defined when the polysilicon is etched to form the gate. Using equations (2.25) and (2.26) we obtain the variance of the relative mismatch for the current factor

$$\frac{\sigma^2_{\Delta\beta}}{\beta^2} = \left(\frac{S^2_{l,\mu C_{ox}}}{WL} + S^2_{g,\mu C_{ox}} D^2\right) + \frac{1}{W^2}\left(\frac{S^2_{l,W}}{L} + S^2_{g,W} D^2\right) + \frac{1}{L^2}\left(\frac{S^2_{l,L}}{W} + S^2_{g,L} D^2\right), \tag{2.49}$$

where $S^2_{l,\mu C_{ox}}$, $S^2_{g,\mu C_{ox}}$, $S^2_{l,W}$, $S^2_{g,W}$, $S^2_{l,L}$ and $S^2_{g,L}$ are positive constants for a specific technology, representing the local and global variation in μC_{ox}, W and L. For large W and L the mismatch in μC_{ox} dominates, while for small W or L the dimensions mismatch dominates. By grouping together terms of local and global variation the above equation becomes

$$\frac{\sigma^2_{\Delta\beta}}{\beta^2} = \frac{1}{WL}\left(S^2_{l,\mu C_{ox}} + \frac{S^2_{l,W}}{W} + \frac{S^2_{l,L}}{L}\right) + \left(S^2_{g,\mu C_{ox}} + \frac{S^2_{g,W}}{W^2} + \frac{S^2_{g,L}}{L^2}\right) D^2 . \tag{2.50}$$

For relatively large values of W and L we obtain the simplified form

$$\frac{\sigma^2_{\Delta\beta}}{\beta^2} = \frac{S^2_{l,\beta}}{WL} + S^2_{g,\beta}D^2, \tag{2.51}$$

with $S^2_{g,\beta}$ and $S^2_{g,\beta}$ positive constants.

In order to find mismatch in the drain current in the saturation region we use (2.43) to obtain

$$\frac{\Delta I}{I} = \frac{\Delta\beta}{\beta} - \frac{2}{(V_{GS}-V_T)}\Delta V_T. \tag{2.52}$$

The threshold voltage and the current factor depend on common factors such as the gate oxide capacitance and the doping concentration of the channel, and we expect the two quantities to be correlated. However, [8] reported that both a theoretical expression and experimental results show that the value of the correlation coefficient is very close to zero. Therefore, (2.52) gives

$$\frac{\sigma^2_{\Delta I}}{I^2} = \frac{\sigma^2_{\Delta\beta}}{\beta^2} + \frac{4}{(V_{GS}-V_T)^2}\sigma^2_{\Delta V_T} \tag{2.53}$$

Using (2.46) and (2.50) we obtain

$$\frac{\sigma^2_{\Delta I}}{I^2} = \frac{1}{WL}\left(S^2_{l,\mu C_{ox}} + \frac{S^2_{l,W}}{W} + \frac{S^2_{l,L}}{L} + \frac{4}{(V_{GS}-V_T)^2}S^2_{l,V_T}\right) \tag{2.54}$$
$$+\left(S^2_{g,\mu C_{ox}} + \frac{S^2_{g,W}}{W^2} + \frac{S^2_{g,L}}{L^2} + \frac{4}{(V_{GS}-V_T)^2}S^2_{g,V_T}\right)D^2.$$

The simplified version for relatively large W and L is

$$\frac{\sigma^2_{\Delta I}}{I^2} = \frac{1}{WL}\left(S^2_{l,\beta} + \frac{4}{(V_{GS}-V_T)^2}S^2_{l,V_T}\right) \tag{2.55}$$
$$+\left(S^2_{g,\beta} + \frac{4}{(V_{GS}-V_T)^2}S^2_{g,V_T}\right)D^2.$$

2.4 Device Parameters of Small Dimension Devices

It is possible that although a device parameter is independent of W and L when these dimensions are relatively large, it becomes a function of them when they are small. A typical example is the threshold voltage of a MOS transistor. In this case, knowledge of the partial derivative of the device parameter with respect to the dimensions - which will be a function of the dimensions - is needed to use (2.3) to predict mismatch of the device parameter. Also the rest of the partial derivatives that appear in (2.3) could be functions of the dimensions now.

For example, in order to predict threshold voltage mismatch behavior of submicron devices we could introduce into (2.3) two new terms, one for each dimension, using the slope of the experimentally obtained curves of the threshold voltage versus W and L. The partial derivatives with respect to the rest of the parameters could be arbitrarily assumed independent of the dimensions as a first approximation, and we could use the model for long dimensions to estimate their effect. Experimental mismatch measurement of threshold voltage of submicron devices are needed to verify the result.

The extension of the mismatch model presented in the next section could be incorporated in the above methodology.

2.5 An Extension of the Mismatch Model of a Process Parameter

The above analysis of effective process parameter mismatch caused by local variation resulting in equations (2.20) and (2.21) is based on the assumption that the autocorrelation distance is small compared to the device dimensions. It is possible that this assumption is not true in the modern submicron technologies. In this section we will investigate how the above equations are modified when we relax this assumption. We preserve the assumption that the process parameter q(x,y) is a wide sense stationary spatial random process, so that the expectation of the first term of (2.12) is given by the quantity in (2.15). We can transform the quadruple intregral

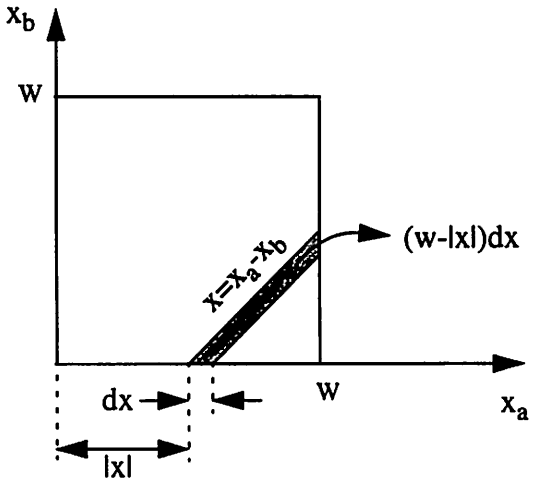


Figure 2.7 Area of integration of the autocorrelation function.

$$\frac{1}{(WL)^2}\int_{y_b=0}^{L}\int_{x_b=0}^{W}\int_{y_a=0}^{L}\int_{x_a=0}^{W} R(x_a-x_b, y_a-y_b)dx_a dy_a dx_b dy_b \tag{2.56}$$

to a double integral by substituting $x=x_a-x_b$ and $y=y_a-y_b$. The area of integration for x_a and x_b is depicted in Figure 2.7 and is the same for y_a and y_b. The new form of the integral is

$$\frac{1}{(WL)^2}\int_{y=-L}^{L}\int_{x=-W}^{W} R(x, y)(W-|x|)(L-|y|)dxdy \ , \tag{2.57}$$

and since the autocorrelation function is even with respect to x and y

$$\frac{4}{WL}\int_{y=0}^{L}\int_{x=0}^{W}\left(1-\frac{x}{W}\right)\left(1-\frac{y}{L}\right)R(x, y)dxdy \quad . \tag{2.58}$$

In order to find an estimation for this quantity we assume that R(x,y) has the rectangular form

$$R_R(x, y) = \begin{cases} \sigma^2 & \text{if } |x|<d_x \text{ and } |y|<d_y \\ 0 & \text{otherwise} \end{cases} \ , \tag{2.59}$$

where we consider different correlation distance for the x and the y direction in order to preserve generality. The quantity in (2.58) now becomes

$$I_R(W)I_R(L), \tag{2.60}$$

where

$$I_R(W) = \frac{2\sigma}{W}\int_0^{\min(W,\,d_x)}\left(1-\frac{x}{W}\right)dx \quad . \tag{2.61}$$

Performing the integration we obtain

$$I_R(W) = \begin{cases} \sigma\left[2\frac{d_x}{W}-\left(\frac{d_x}{W}\right)^2\right] & \text{if } d_x < W \\ \sigma & \text{if } d_x > W \end{cases} \quad . \tag{2.62}$$

As a more realistic example of R(x,y) we consider a two-dimensional Gaussian function

$$R_G(x, y) = \sigma^2\exp\left[-\left(\frac{x^2}{d_x^2}+\frac{y^2}{d_y^2}\right)\right] \quad , \tag{2.63}$$

where again we assumed different correlation distance for the x and the y direction. A two dimensional Gaussian shape as an example of R(x,y) has also been suggested by Shyu, Temes and Kung in [12]. A Gaussian autocorrelation function corresponds to a Gaussian power spectral density, as opposed to the flat power spectral density implied by an impulse autocorrelation function. The quantity in (2.58) now becomes

$$I_G(W)I_G(L), \tag{2.64}$$

where

$$I_G(W) = \frac{2\sigma}{W}\int_0^{W}\left(1-\frac{x}{W}\right)\exp\left(-\frac{x^2}{d_x^2}\right)dx \quad . \tag{2.65}$$

Performing the integration we obtain

$$I_G(W) = \sigma\frac{d_x}{W}\left\{\sqrt{\pi}\cdot\operatorname{erf}\left(\frac{W}{d_x}\right)+\frac{d_x}{W}\left[\exp\left(-\frac{W^2}{d_x^2}\right)-1\right]\right\}, \tag{2.66}$$

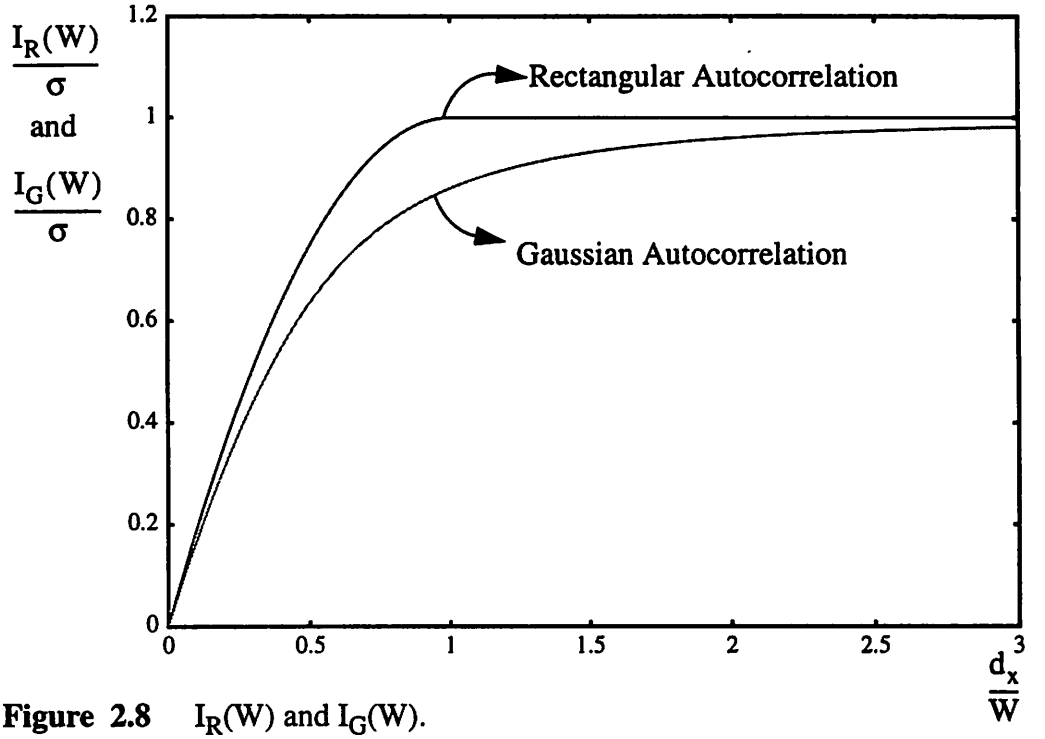


Figure 2.8 $I_R(W)$ and $I_G(W)$.

where erf(x) is the error function

$$\mathrm{erf}(x) = \frac{2}{\sqrt{\pi}}\int_0^x \exp(-\omega^2)d\omega . \tag{2.67}$$

The value of $I_R(W)$ and $I_G(W)$ as a function of d_x/W is depicted in Figure 2.8. $I_R(L)$ and $I_G(L)$ versus d_y/L are similar. The expectation of the second term of (2.12) is equal to that of the first.

We proceed now to calculate the expectation of the third term of (2.12) as given by (2.19), which depends on the distance between the devices and is negative, which means that it improves matching. The quadruple integral

$$\frac{2}{(WL)^2}\int_{y_b=0}^{L}\int_{x_b=D}^{D+W}\int_{y_a=0}^{L}\int_{x_a=0}^{W} R(x_a-x_b, y_a-y_b)dx_a dy_a dx_b dy_b \tag{2.68}$$

can be reduced to a double integral similar to (2.57):

$$\frac{2}{(WL)^2}\int_{y=-L}^{L}\int_{x=-W}^{W} R(x-D, y)(W-|x|)(L-|y|)dxdy \tag{2.69}$$

Since the autocorrelation R(x,y) is an even function of y, we have

$$\frac{4}{WL}\int_{y=0}^{L}\int_{x=-W}^{W} R(x-D,y)\left(1-\frac{|x|}{W}\right)\left(1-\frac{|y|}{L}\right)dxdy\,. \tag{2.70}$$

In order to find an estimation for this term we again use the rectangular autocorrelation function given by (2.59). The quantity in (2.70) now becomes

$$2I_R(L)I_{D,R}(W)\ , \tag{2.71}$$

where $I_R(L)$ is as defined in (2.61) and evaluates to (2.62), and $I_{D,R}(W)$ is given by

$$I_{D,R}(W) = \frac{1}{W}\int_{-W}^{W} R_{R,x}(x-D)\left(1-\frac{|x|}{W}\right)dx\ , \tag{2.72}$$

where

$$R_{R,x}(x) = \begin{cases} \sigma & \text{if } |x|<d_x \\ 0 & \text{otherwise} \end{cases}\ . \tag{2.73}$$

This can be written as.

$$I_{D,R}(W) = \frac{\sigma}{W}\int_{\min(\max(-W,\,D-d_x),\,W)}^{W}\left(1-\frac{|x|}{W}\right)dx \tag{2.74}$$

and is calculated and depicted in Figure 2.9 for different values of distance D.

Using the two-dimensional Gaussian autocorrelation function given by (2.63), the quantity in (2.70) has again the form

$$2I_G(L)I_{D,G}(W)\ , \tag{2.75}$$

where $I_G(L)$ is given by (2.66) and $I_{D,G}(W)$ is given by

$$I_{D,G}(W) = \frac{1}{W}\int_{-W}^{W} R_{G,x}(x-D)\left(1-\frac{|x|}{W}\right)dx\ , \tag{2.76}$$

where $R_{G,x}(x)$ is

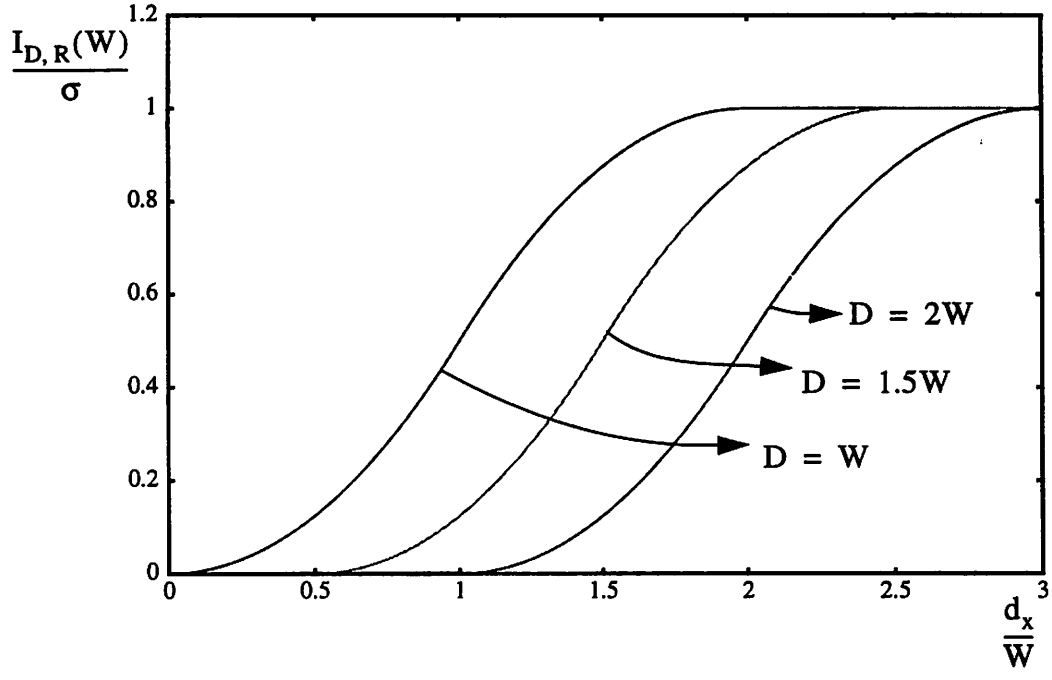


Figure 2.9 $I_{D,R}(W)$, for the rectangular autocorrelation function.

$$R_{G,x}(x) = \sigma \cdot \exp\left(-\frac{x^2}{d_x^2}\right) . \tag{2.77}$$

After some calculations we obtain

$$\begin{aligned} I_{D,G}(W) = \frac{\sigma d_x}{2W}\Bigg\{ & \sqrt{\pi}\left(1+\frac{W}{D}\right)\left[\operatorname{erf}\left(-\frac{D}{d_x}\right)-\operatorname{erf}\left(-\frac{D+W}{d_x}\right)\right] \\ & + \sqrt{\pi}\left(1-\frac{W}{D}\right)\left[\operatorname{erf}\left(-\frac{D-W}{d_x}\right)-\operatorname{erf}\left(-\frac{D}{d_x}\right)\right] \\ & + \frac{d_x}{W}\left[\exp\left(-\frac{(D+W)^2}{d_x^2}\right)-\exp\left(-\frac{D^2}{d_x^2}\right)\right] \\ & + \frac{d_x}{W}\left[\exp\left(-\frac{(D-W)^2}{d_x^2}\right)-\exp\left(-\frac{D^2}{d_x^2}\right)\right]\Bigg\} , \end{aligned} \tag{2.78}$$

which is depicted in Figure 2.10.

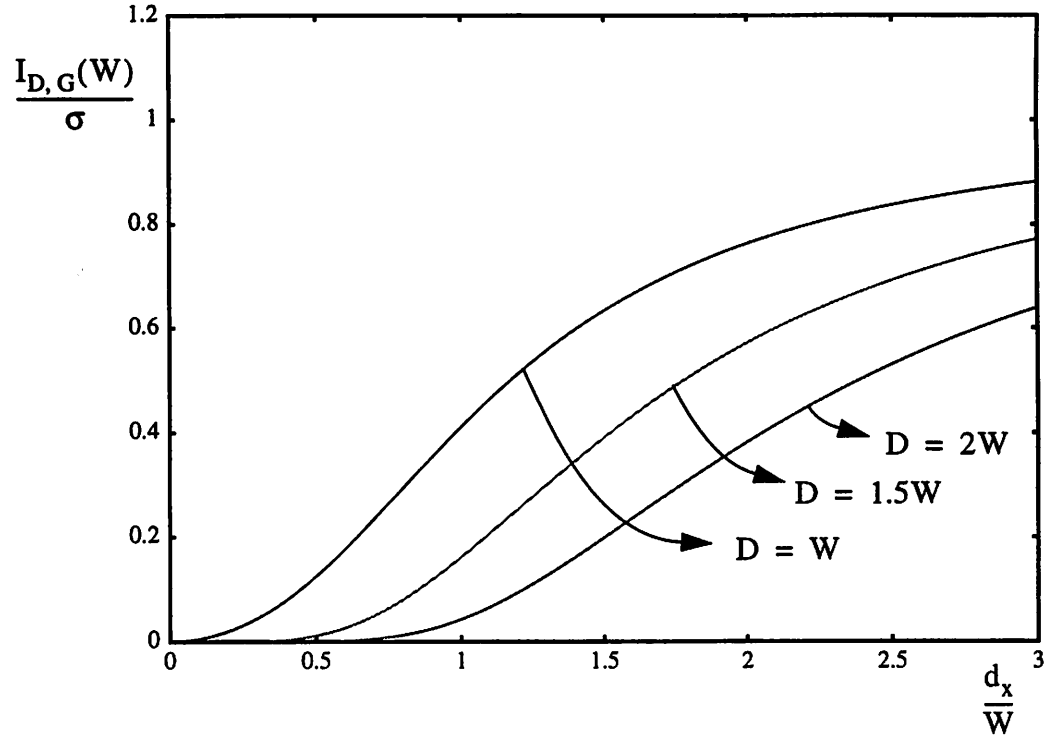


Figure 2.10 $I_{D,G}(W)$ for the two dimensional Gaussian autocorrelation.

Finally the total variance of the local mismatch is

$$\sigma^2_{\Delta q_1} = 2I_R(L)[I_R(W) - I_{D,R}(W)] \tag{2.79}$$

for the rectangular autocorrelation and

$$\sigma^2_{\Delta q_1} = 2I_G(L)[I_G(W) - I_{D,G}(W)] \tag{2.80}$$

for the Gaussian autocorrelation.

When the parameter q is dimension L, similar analysis in one dimension gives

$$\sigma^2_{\Delta L_1} = 2[I_R(W) - I_{R,D}(W)] \tag{2.81}$$

for the rectangular autocorrelation and

$$\sigma^2_{\Delta L_1} = 2[I_G(W) - I_{G,D}(W)] \tag{2.82}$$

for the Gaussian autocorrelation. When parameter q is dimension W

$$\sigma^2_{\Delta W_1} = \begin{cases} 2I_R(L) & \text{if } D > d_x \\ 0 & \text{if } D < d_x \end{cases} \tag{2.83}$$

for the rectangular autocorrelation and

$$\sigma^2_{\Delta W_1} = 2I_G(L)\left[1 - \exp\left(-\frac{D^2}{d_x^2}\right)\right] \tag{2.84}$$

for the Gaussian autocorrelation. It is worth noticing that

$$1 - \exp\left(-\frac{D^2}{d_x^2}\right) \tag{2.85}$$

looks very similar to the step function in (2.83). The estimations of $\sigma^2_{\Delta L}$ in (2.81) and (2.82) have the same step shape too; therefore, the variation in ΔW and ΔL has approximately the same dependence on L and W respectively.

For W and distance D much longer then the autocorrelation distance, $I_{D,R}(W)$ and $I_{D,G}(W)$ are zero. $I_R(W)$ and $I_G(W)$ are proportional to 1/W, and $I_R(L)$ and $I_G(L)$ are proportional to 1/L. Therefore (2.79) and (2.80) of the extended model agree with (2.20) of the model derived for long dimensions in the previous paragraph. The variance of ΔW and ΔL in equations (2.81)-(2.84) is proportional to 1/L and 1/W respectively, and the new model agrees with the previous model that resulted in equation (2.21).

For small dimensions there are two mechanisms through which matching becomes better than what (2.20) and (2.21) predict. First $I_R(W)$ and $I_G(W)$ reach a saturation level that can be observed in Figure 2.9 when W becomes very small, and similarly for L. Second, when D and W are small, $I_D(W)$ becomes significant and reduces mismatch, as equations (2.79) and (2.80) show. Qualitatively, the same behavior is observed for the dimension mismatch in equations (2.81)-(2.84).

2.6 Comments on the Extension of the Model

We expect each process parameter to have its own autocorrelation distance, and saturation of mismatch to become significant at different values of the dimensions W and L for each one of those. The effect on the mismatch on a device parameter P is the weighted sum of the mismatch of many process parameters, as (2.3) implies. If the device parameter does not depend on the dimensions W and L, saturation is expected to appear gradually to its mismatch as W and L become small, and saturation in the mismatch of more process parameters becomes significant.

For the device parameters that are proportional or inversely proportional to W or L, the length or width mismatch term is multiplied by $1/W^2$ or $1/L^2$ respectively as can be seen in equations (2.30), (2.36) and (2.49). Therefore, even if the dimension mismatch itself becomes smaller than what (2.26) predicts, its effect becomes stronger, so we should expect that the matching of the device parameter will be worse than is predicted by the simplified equations (2.33), (2.42) and (2.51).

At this point we do not have sufficient information about the autocorrelation distance of any process parameters, and we are not able to predict if saturation actually appears in the mismatch of the smallest devices that can be fabricated today. Experimental data are needed to support the validity of the model.

Chapter 3

Mismatch and Circuit Performance

3.1 Introduction

In this chapter we examine how device mismatch affects the circuit performance. Examples of performance degradation are input offset in operational amplifiers and differential pairs, current deviation in current mirrors, nonlinearity in A/D converters, etc. Some of the results of this chapter will be used in Chapter 5 to study the behavior of the simple subcircuits that we fabricated.

3.2 Current Mirror

A MOS current mirror is shown in Figure 3.1. The W/L ratio between the two devices is n:m. The output current is ideally $\frac{m}{n}I_{in}$ but because of device mismatch and channel modulation effects it is different in practice. In the following analysis we ignore channel modulation, which can be minimized by using the same V_{DS} for M1 and M2 as in the case of a cascode current mirror. When accuracy is needed we design many identical devices

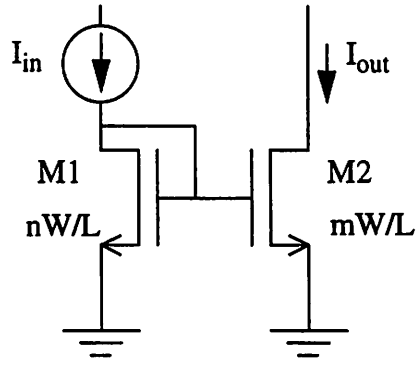


Figure 3.1 A MOS current mirror.

connected in parallel instead of devices of different sizes. Therefore we shall consider that M1 and M2 are not single transistors but n and m, respectively, identically designed transistors connected in parallel. We shall also assume that M1 and M2 are laid out with common centroid geometry with common center of mass, in order to eliminate the effect of the large gradients of variation, as described in Section 2.2.4. The mismatch is assumed to be caused exclusively by the short correlation distance variation with correlation distance much smaller than the device dimensions. For a specific device parameter we assume the same mean and the same variance among all the devices. The square of the deviation of a process parameter from the mean is of the form of (2.13), and the variance of the deviation is of the form (2.15), or equivalently (2.18).

The well known relation that gives the current of a MOS transistor in the saturation region ignoring the finite output resistance is

$$I = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2 = \beta(V_{GS} - V_T)^2 \tag{3.1}$$

where μ is the mobility of the carriers, C_{ox} is the gate capacitance per unit area, V_{GS} is the gate-source voltage, V_T is the threshold voltage and

$$\beta = \frac{\mu C_{ox}}{2}\frac{W}{L} \tag{3.2}$$

is defined as the current factor. In the following analysis the differences in the process parameters β and V_T imply deviations from the common mean. The differences in drain currents and the gate source voltage imply deviations from the value these quantities would have if all the devices behaved identically and the process parameters of all of them were equal to the mean. Since to first order we ignore the large gradient variation, with the aid of equations (2.46) and (2.49) the variance of V_T and β is given by

$$\sigma^2_{V_T} = \frac{S^2_{I,V_T}}{2WL} \tag{3.3}$$

and

$$\frac{\sigma_\beta^2}{\beta^2} = \frac{S_{I,\mu C_{ox}}^2}{2WL} + \frac{1}{W^2}\frac{S_{I,W}^2}{2L} + \frac{1}{L^2}\frac{S_{I,L}^2}{2W} \quad , \tag{3.4}$$

respectively. The coefficients S_{I,V_T}^2, $S_{I,\mu C_{ox}}^2$, $S_{I,W}^2$, $S_{I,L}^2$ have been defined in Chapter 2. The coefficient of 2 in the denominator appears, because here we refer to the variance of a parameter and not the variance of the difference of the parameter between two devices, as was the case equations (2.46) and (2.49).

The variation in the current in terms of the variation in β, V_{GS} and V_T is given by

$$\frac{\Delta I}{I} = \frac{\Delta\beta}{\beta} + \frac{2}{(V_{GS}-V_T)}(\Delta V_T - \Delta V_{GS}) \quad . \tag{3.5}$$

This relation, applied to the i-th of the n devices that comprise M1, gives:

$$\frac{\Delta I_{M1,i}}{I_{in}/n} = \frac{\Delta\beta_{M1,i}}{\beta} + \frac{2}{(V_{GS}-V_T)}((\Delta V_T)_{M1,i} - \Delta V_{GS}) \quad , \tag{3.6}$$

where the index M1,i indicates the specific transistor to which the quantity refers. The total drain current of M1 is I_{in}, so the current variations $\Delta I_{M1,i}$ add up to zero. Summing those relations for i=1 to n gives

$$0 = \frac{1}{\beta}\sum_{i=1}^{n}\Delta\beta_{M1,i} + \frac{2}{(V_{GS}-V_T)}\left(\sum_{i=1}^{n}(\Delta V_T)_{M1,i} - n\Delta V_{GS}\right) \tag{3.7}$$

or

$$\Delta V_{GS} = \frac{1}{n}\sum_{i=1}^{n}(\Delta V_T)_{M1,i} + \frac{(V_{GS}-V_T)}{2}\frac{1}{n\beta}\sum_{i=1}^{n}\Delta\beta_{M1,i} \quad . \tag{3.8}$$

Similarly to (3.6) the variance of the current in each one of the m transistors that comprise M2 is

$$\frac{\Delta I_{M2,i}}{I_{out}/m} = \frac{\Delta\beta_{M2,i}}{\beta} + \frac{2}{(V_{GS}-V_T)}((\Delta V_T)_{M2,i} - \Delta V_{GS}) \quad , \tag{3.9}$$

and the variation in I_{out} is

$$\frac{\Delta I_{out}}{I_{out}} = \frac{1}{m\beta}\sum_{i=1}^{m}\Delta\beta_{M2,i} + \frac{2}{(V_{GS}-V_T)}\left(\frac{1}{m}\sum_{i=1}^{m}(\Delta V_T)_{M2,i} - \Delta V_{GS}\right), \tag{3.10}$$

and by using V_{GS} from (3.8),

$$\frac{\Delta I_{out}}{I_{out}} = \frac{1}{m\beta}\sum_{i=1}^{m}\Delta\beta_{M2,i} - \frac{1}{n\beta}\sum_{i=1}^{n}\Delta\beta_{M1,i} \tag{3.11}$$
$$+ \frac{2}{(V_{GS}-V_T)}\left(\frac{1}{m}\sum_{i=1}^{m}(\Delta V_T)_{M2,i} - \frac{1}{n}\sum_{i=1}^{n}(\Delta V_T)_{M1,i}\right).$$

Assuming that the variance is the same for the process parameters among all the devices and that the threshold voltage is independent of the current factor, as has been referred in Section 2.3.3, we obtain

$$\frac{\sigma^2_{I_{out}}}{I^2_{out}} = \left(\frac{1}{n}+\frac{1}{m}\right)\frac{\sigma^2_\beta}{\beta^2} + \left(\frac{1}{n}+\frac{1}{m}\right)\frac{4\sigma^2_{V_T}}{(V_{GS}-V_T)^2}. \tag{3.12}$$

3.3 Differential Pair

We consider now the differential pair shown in Figure 3.2. We shall estimate the variance of the input offset. As in the case of the current mirror we shall ignore the channel length modulation. The differential pair then has infinite voltage gain, and the offset is the value of the differential input signal which drives all four transistors to saturation. Therefore, the current of all four transistors is given by equation (3.1), and the relative difference in the current between a pair of transistors is given by (3.5). Using the latter we obtain an expression for the offset:

$$V_{off} = \Delta V_{GS}|_{1,2} = \tag{3.13}$$
$$\Delta V_T|_{1,2} + \left.\frac{V_{GS}-V_T}{2}\right|_{1,2}\cdot\left(\left.\frac{\Delta I}{I}\right|_{1,2} - \left.\frac{\Delta\beta}{\beta}\right|_{1,2}\right),$$

where $|_{1,2}$ indicates the M1, M2 device pair. Again, equation (3.5) gives

$$\left.\frac{\Delta I}{I}\right|_{3,4} = \left.\frac{\Delta\beta}{\beta}\right|_{3,4} + \left.\frac{2}{V_{GS}-V_T}\right|_{3,4}\cdot\Delta V_T|_{3,4}. \tag{3.14}$$

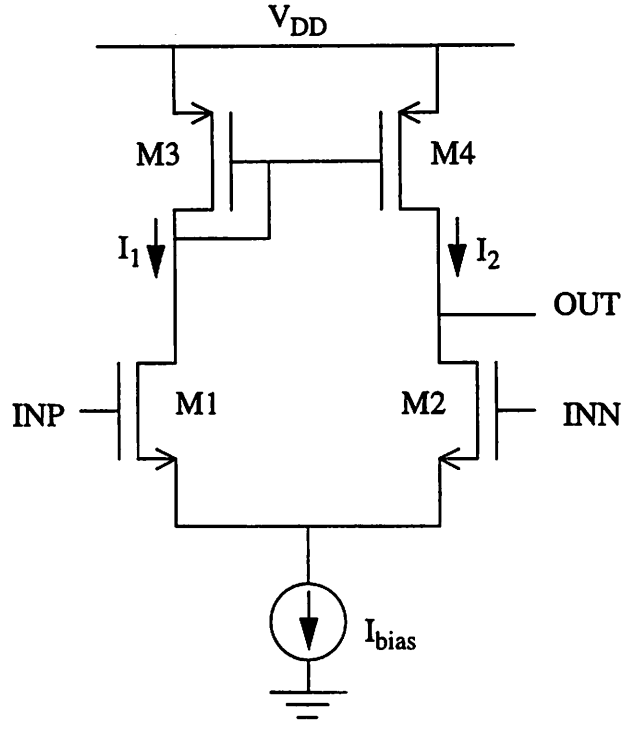


Figure 3.2 A differential pair.

Since

$$\left.\frac{\Delta I}{I}\right|_{1,2} = \left.\frac{\Delta I}{I}\right|_{3,4} , \tag{3.15}$$

we obtain

$$V_{off} = \Delta V_T|_{1,2} \tag{3.16}$$

$$+ \left.\frac{V_{GS}-V_T}{2}\right|_{1,2} \cdot \left(\left.\frac{\Delta\beta}{\beta}\right|_{3,4} - \left.\frac{\Delta\beta}{\beta}\right|_{1,2} + \left.\frac{2}{V_{GS}-V_T}\right|_{3,4} \cdot \Delta V_T|_{3,4} \right) .$$

It is of practical importance to calculate the variance of the input offset. As explained in Section 2.3.3, the current factor and the threshold voltage can be considered uncorrelated. However, we expect some correlation between $\Delta\beta|_{1,2}$ and $\Delta\beta|_{3,4}$, and between $\Delta V_T|_{3,4}$ and $\Delta V_T|_{3,4}$. The local variation components are independent, since we assume short autocorrelation distance. If each one of the transistors M1, M2, M3 and M4 consists of many parallel connected devices and common centroid geometry is used for each pair,

the effect of global variation can be neglected to a first order as discussed above, and the correlation can be considered zero. If M1, M2, M3 and M4 are single devices then similarly to Equation (2.22) we can write

$$\Delta V_T\big|_{1,2} = \lambda_{V_T}\big|_{1,2} D_{1,2} \tag{3.17}$$

and

$$\Delta V_T\big|_{3,4} = \lambda_{V_T}\big|_{3,4} D_{3,4} \ , \tag{3.18}$$

where $\lambda_{V_T}\big|_{1,2}$ and $\lambda_{V_T}\big|_{3,4}$ are the slopes of the large gradients of variation, and $D_{1,2}$ and $D_{3,4}$ are the distances between the two transistors of each pair. The correlation is

$$r_{\Delta V_T} = E\left[\lambda_{V_T}\big|_{1,2} \cdot \lambda_{V_T}\big|_{3,4}\right] D_{1,2} D_{3,4} \ , \tag{3.19}$$

where E[] denotes the expectation of a random variable. It becomes small when the distances $D_{1,2}$ and $D_{3,4}$ are short, when we minimize the total dependence on the global variation, also. Considering relatively large W and L, a similar equation holds for the correlation of $\Delta\beta$. Finally the variance of the offset is

$$\sigma^2_{V_{off}} = \sigma^2_{\Delta V_T|_{1,2}} + \left(\frac{(V_{GS}-V_T)\big|_{1,2}}{(V_{GS}-V_T)\big|_{3,4}}\right)^2 \sigma^2_{\Delta V_T|_{3,4}} + 2\frac{(V_{GS}-V_T)\big|_{1,2}}{(V_{GS}-V_T)\big|_{3,4}} r_{\Delta V_T} \tag{3.20}$$

$$+\left(\frac{V_{GS}-V_T}{2}\bigg|_{1,2}\right)^2\left(\frac{\sigma^2_{\Delta\beta|_{3,4}}}{\beta^2\big|_{3,4}} + \frac{\sigma^2_{\Delta\beta|_{1,2}}}{\beta^2\big|_{1,2}} - 2\frac{r_{\Delta\beta}}{\beta|_{1,2}\beta|_{3,4}}\right)$$

3.4 D/A converter

The operation of a large family of D/A converters is based on arrays of identically designed devices. Depending on the number of devices that are "on", we obtain the several levels of the output signal. An "on" device is defined according to the kind of the converter. If it is a string of resistors with common current flowing through them, a resistor is considered on when the voltage drop across it contributes to the output. If the converter

consists of many transistors with common drain and source, a transistor is on when the gate voltage is such that drives the transistor to saturation, and it contributes to the output current. Finally, if it is a charge redistribution D/A converter, the output is the common terminal of all the capacitors in the array, and a capacitor is on when the voltage on its other terminal changes in the second clock phase, according to a voltage reference.

Assuming that the D/A converter consists of N devices, there are N levels of the output signal corresponding to the situation where 0, 1,... N-1 of the devices are on. The full scale where all N of the devices are on is usually not available as an output. Assuming that k devices are on, the output is

$$A_o = \sum_{i=1}^{k} a_i \qquad k = 0, 1 \ldots N\text{-}1, \tag{3.21}$$

where a_i is the contribution of each device to the output. The nominal values of the a_i are the same and equal to a. When k=0 the output is zero. By turning all the devices on we obtain the full scale output

$$A_{FS} = \sum_{i=1}^{N} a_i = \sum_{i=1}^{k} a_i + \sum_{i=k+1}^{N} a_i, \tag{3.22}$$

and the ratio of the output over the full scale is

$$\frac{A_o}{A_{FS}} = \frac{\sum_{i=1}^{k} a_i}{\sum_{i=1}^{k} a_i + \sum_{i=k+1}^{N} a_i}. \tag{3.23}$$

Integral Nonlinearity at a step k (INL(k)) is defined as the discrepancy of the above quantity form the its expectation -which is also the nominal value - (k/N).

$$INL(k) = \frac{A_o}{A_{FS}} - \frac{k}{N} \tag{3.24}$$

Integral Nonlinearity (INL) of the D/A converter is defined as the maximum INL(k) for all the steps k.

In order to calculate the variance of the quantity in (3.23), we need to calculate the partial derivative with respect to the contribution a_i of the on and the off devices.

$$\left.\frac{\partial}{\partial a_i}\left(\frac{A_o}{A_{FS}}\right)\right|_{a_i \text{ is ON}} = \frac{\sum_{i=k+1}^{N} a_i}{\left(\sum_{i=1}^{k} a_i + \sum_{i=k+1}^{N} a_i\right)^2} = \frac{N-k}{N}\cdot\frac{1}{A_{FS}} \tag{3.25}$$

and

$$\left.\frac{\partial}{\partial a_i}\left(\frac{A_o}{A_{FS}}\right)\right|_{a_i \text{ is OFF}} = -\frac{\sum_{i=1}^{k} a_i}{\left(\sum_{i=1}^{k} a_i + \sum_{i=k+1}^{N} a_i\right)^2} = -\frac{k}{N}\cdot\frac{1}{A_{FS}}, \tag{3.26}$$

where the nominal values of a_i are used for the evaluation.

Under the assumption of a common centroid geometry layout, the effect of the large gradients of variation can be ignored to the first order, and the short correlation distance noise dominates. The a_i can then be considered uncorrelated with equal variance σ_a^2. The variance of the ratio of the output over the full scale is

$$\sigma^2_{\frac{A_o}{A_{FS}}} = \left[k\left(\left.\frac{\partial}{\partial a_i}\left(\frac{A_o}{A_{FS}}\right)\right|_{a_i \text{ is ON}}\right)^2 + (N-k)\left(\left.\frac{\partial}{\partial a_i}\left(\frac{A_o}{A_{FS}}\right)\right|_{a_i \text{ is OFF}}\right)^2\right]\sigma_a^2 \tag{3.27}$$

or

$$\sigma^2_{INL(k)} = \sigma^2_{\frac{A_o}{A_{FS}}} = \frac{k(N-k)}{N}\cdot\frac{\sigma_a^2}{A_{FS}^2}. \tag{3.28}$$

In terms of the nominal step size,

$$a = \frac{A_{FS}}{N}, \tag{3.29}$$

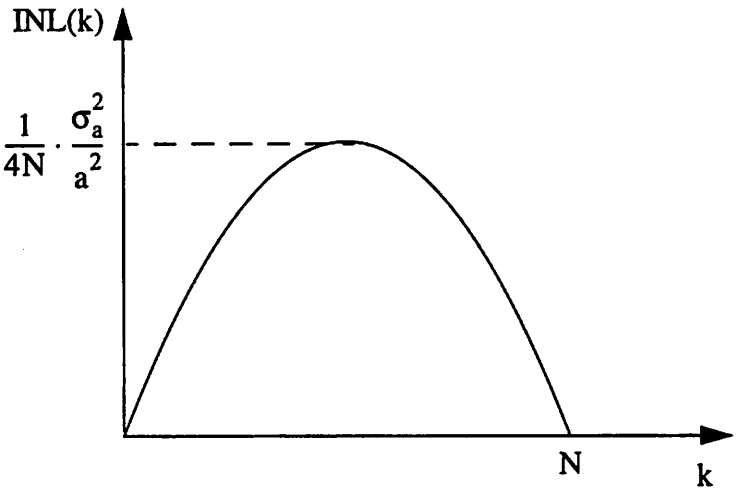


Figure 3.3 Variance of the integral nonlinearity at a step k.

we obtain

$$\sigma^2_{INL(k)} = \frac{k(N-k)}{N^3} \cdot \frac{\sigma_a^2}{a^2} \; . \tag{3.30}$$

This variance as a function of the step k is depicted in Figure 3.3. It is maximized when k=N/2

$$\max(\sigma^2_{INL(k)}) = \sigma^2_{INL\left(\frac{N}{2}\right)} = \frac{1}{4N} \cdot \frac{\sigma_a^2}{a^2} \; . \tag{3.31}$$

Chapter 4

Test Structures

4.1 Introduction

In this chapter we describe the test structures that we designed and fabricated in order to study variability. We used the Baseline Process of the Berkeley Microfabrication Laboratory. The minimum allowed polysilicon linewidth was 2μm.

4.2 General Information

These structures include:

- arrays of resistors and two dimensional arrays of transistors and capacitors to examine neighboring effects,
- arrays of pairs of transistors, resistors and capacitors of various sizes and distances, with which we will verify the validity of the mismatch models presented in chapter 2 and we will measure their coefficients,
- structures with which we will examine the effect of orientation in matching, and
- simple circuits, such as differential pairs and a two stage operational amplifier. We will predict input offset based on the mismatch information of the individual devices using the methodology presented in chapter 3, and we will examine agreement with the measured values.

The area and distance coefficients to which we will refer are the coefficients S_A^2 and S_D^2 respectively of the mismatch model

$$\sigma_P^2 = \frac{S_A^2}{WL} + S_D^2 \cdot D^2 , \tag{4.1}$$

presented in Chapter 2. σ_P^2 is the variance of the mismatch, W and L represent the dimensions of the device, and D the distance between them.

We used structures dedicated to the measurement of each coefficient. Arrays of pairs of small devices with minimum distance between the devices were used for the area coefficient in order to minimize the large gradient variation effect and emphasize the effect of the local variability. Arrays of large devices in long distances were used for the distance coefficient, to minimize the local variability effect and reveal the large gradient dependence.

In the transistor and the resistors structures for the area coefficient, one of the two dimensions is kept constant among the pairs. In this way the graph of mismatch versus area appears identical to the graph of the mismatch versus the varying dimension, and is not affected by discrepancies of the other dimension - which is common - from the nominal value.

In the transistor structures for the area coefficient, while the length L is kept constant, the widths W vary from pair to pair in a way that they are equally spaced on an axis $1/\sqrt{W}$.Graphs of mismatch standard deviation versus the inverse square root of the area and graphs of mismatch standard deviation versus the distance in [11] and [8], motivated us to distribute the widths in the this way. However, it is the mismatch variance, as given in (4.1) that is linearly dependent on the inverse area and the square of the distance. The measurements described in Chapter 5 showed that the error introduced in the estimation of the area coefficient by fitting a line between the mismatch standard deviation and the inverse square root of the area, and the distance coefficient by fitting a line between the mismatch standard deviation and the distance is in some cases significant. Mismatch variance versus inverse area will be used in Chapter 5 for the extraction of the area coefficient, although the points are not evenly distributed on the 1/area axis. The distance coefficient will be extracted from the graph of mismatch variance versus the square of the distance. For resistors, W is kept constant and L varies in a similar way.

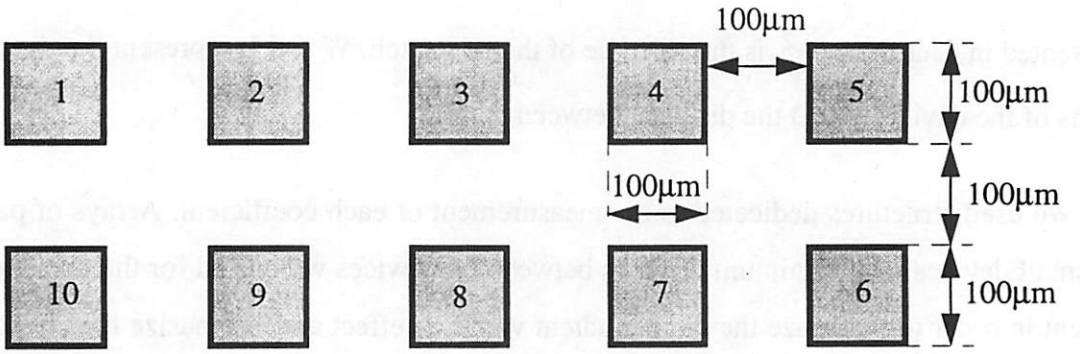


Figure 4.1 The common pad set of all the structures.

From the transistors, we will extract and examine variation in threshold voltage, current factor and body effect coefficient. The resistors with relatively low nominal value are measured with four point measurement while those will relatively high with two point measurement as is described in section 5.3.1.

All the structures are connected to the pad set shown in Figure 4.1. Only the number of the pad to which each wire is connected is shown in the layout of the structures below.The test structures are presented below in groups. For each test structure we present the identifying label printed next to it, its location on the chip, a short description, and a short reference to its use. The coordinates that describe the location are given with the convention that the leftmost bottom padset - that belongs to the scribe lane - has coordinates (0,0), the x-coordinate increases from the left to the right and the y-coordinate increases from the bottom to the top. More information about the organization of the die can be found in [19].

The use of a second metal layer has been avoided where possible, since there have been problems with it in the past in the Baseline Process of the Berkeley Microfabrication Laboratory. It has been used only for the two dimensional transistor arrays, i.e. the structures 23-26 below.

The structures 17 and 18 repeat 2 times in the die. All the rest structures repeat 3 times.

4.3 Resistor Structures

4.3.1 Resistor Arrays for Edge Effects Observation

Structure 1: Array of polysilicon resistors 1.

Label: RAP1

Location: (920, 1280), (2760, 4800), (5520, 320).

Description: Array of 7 poly resistors, width=2μm, length=600μm distance=2mm, depicted in Figure 4.2. Four point measurements.

Use: We will observe if the resistors at the end of the array have different value than those in the middle.

Structure 2: Array of polysilicon resistors 2.

Label: RAP2

Location: (920, 1600), (2760, 5120), (5520, 640).

Description: Array of 7 poly resistors, width=4μm, length=600μm, distance=2μm. The layout is similar to this of structure 1.

Use: The same as for structure 1

Structure 3: Array of N-diffusion resistors.

Label: RAND

Location: (920,1920), (2760, 5440), (5520, 960).

Description: Array of 6 n-diffusion resistors, width=3μm, length=600μm, distance= 3μm, depicted in Figure 4.3.

Use: The same as for structures 1 and 2. We will also observe if the resistor who is closest to the diffusion stripe that biases the substrate has different value than the rest.

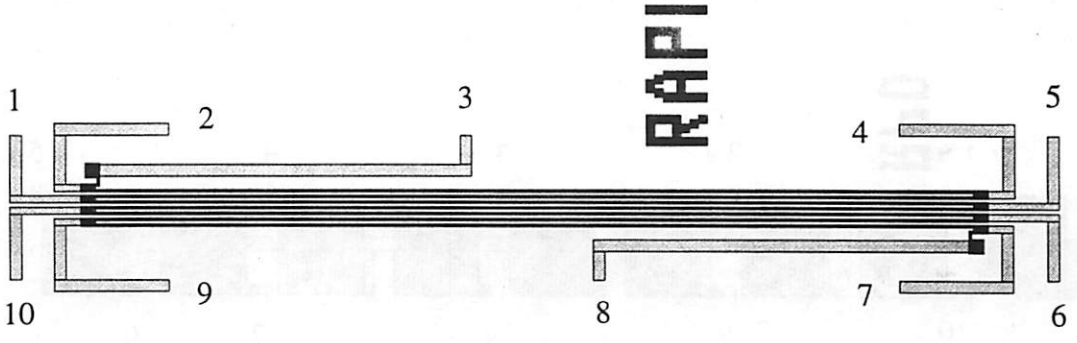


Figure 4.2 Array of Polysilicon Resistors 1.

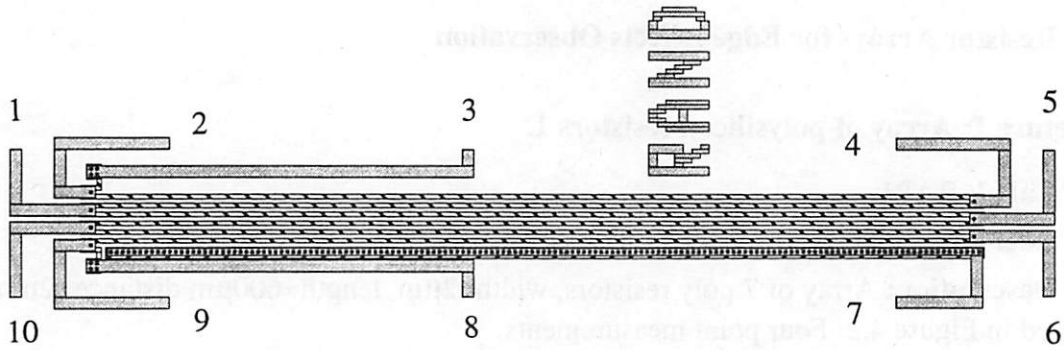


Figure 4.3 Array of N Diffusion Resistors.

Structure 4: Array of P-diffusion resistors.

The information about this structure is the same as for structure 3, but these are p-diffusion resistors. The layout is similar to this of structure 3, also.

Label: RAPD

Location: (920, 2240), (2760, 5760), (5520, 1280).

4.3.2 Polysilicon Resistor Mismatch Model

Structure 5: Polysilicon Resistors for the Distance Coefficient.

Label: RPD

Location: (4600, 3520), (5520, 2560), (6440, 6080).

Description: Array of 9 poly resistors, width=2μm, length=1748μm folded, distance =100μm, depicted in Figure 4.4. Two point measurements.

Use: We will find the distance coefficient of the mismatch model.

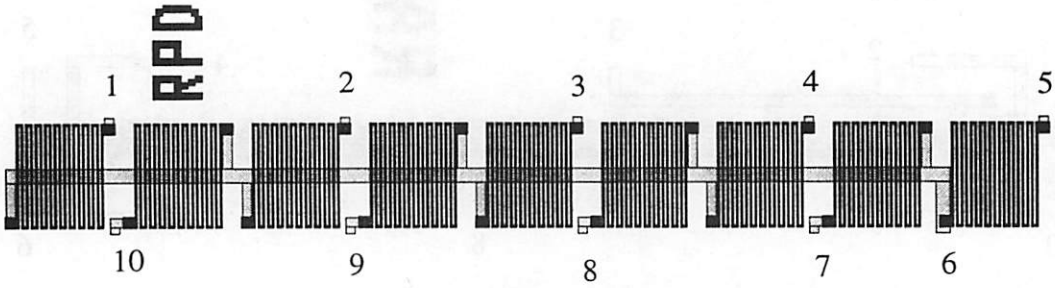


Figure 4.4 Array of Polysilicon Resistors for the Distance Coefficient.

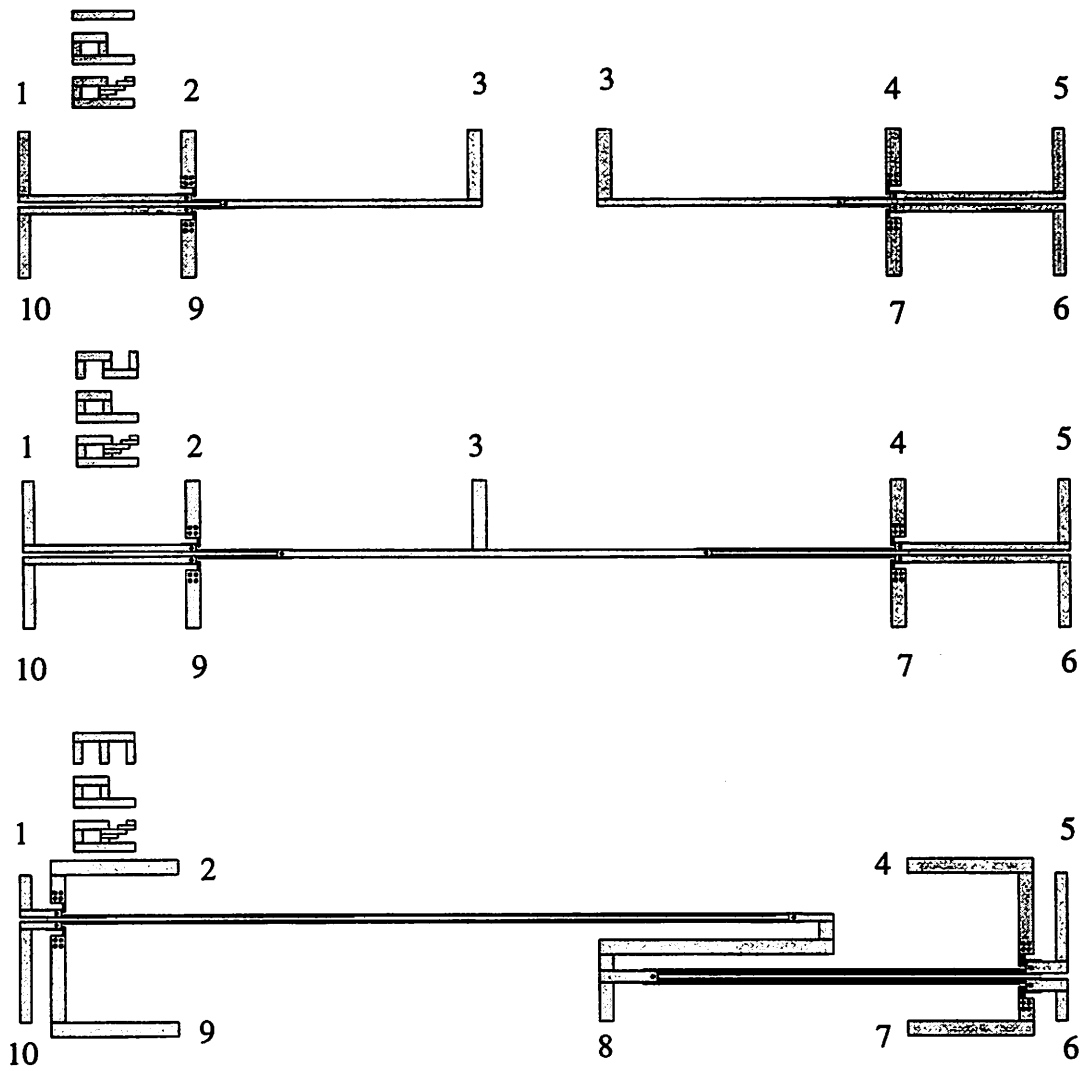


Figure 4.5 Pairs of Polysilicon Resistors 1, 2 and 3 for the Area Coefficient.

Structure 6: Pairs of Polysilicon Resistors 1 for the Area Coefficient.

Label: RP1

Location: (4600, 2560), (5520, 1600), (6440, 5120).

Description: 2 pairs of poly resistors, width=2μm, lengths=20μm and 31.5μm, distance=2μm, depicted in Figure 4.5. Four point measurements.

Use: Together with the structures 7 and 8, we will find the area coefficient of the mismatch model.

Structure 7: Pairs of Polysilicon Resistors 2 for the Area Coefficient.

Label: RP2

Location: (4600, 2880), (5520, 1920), (6440, 5440).

Description: 2 pairs of poly resistors, width=2μm, lengths=55.5μm and 125μm, distance=2μm, depicted in Figure 4.5. Four point measurements.

Use: Described above.

Structure 8: Pairs of Polysilicon Resistors 3 for the Area Coefficient.

Label: RP3

Location: (4600, 3200), (5520, 2240), (6440, 5760).

Description: 2 pairs of poly resistors with equal area, one with length=500μm and width=2μm and one with length=250μm and width=4μm, depicted in Figure 4.5. Four point measurements.

Use: Described above. Theoretically the two pairs should demonstrate the same mismatch since they have the same area. Information about the difference of the actual and the drawn width can be extracted if needed. If R_1 and R_2 are two resistors with dimensions W_1, L_1 and W_2, L_2 respectively, R_S is the sheet resistance, and ΔW is the difference of the drawn and the actual width, the values of the resistors are

$$R_1 = R_S \cdot \frac{L_1}{W_1 - \Delta W} \qquad R_2 = R_S \cdot \frac{L_2}{W_2 - \Delta W}. \tag{4.2}$$

By dividing the two above equations we obtain

$$\Delta W = \frac{W_2(W_1/W_2 - \alpha)}{(1-\alpha)} \qquad \text{where} \qquad \alpha = \frac{R_2}{R_1} \cdot \frac{L_1}{L_2} \tag{4.3}$$

4.3.3 N-Diffusion Resistor Mismatch Model

Structure 9: N-Diffusion Resistors for the Distance Coefficient.

Label: RNDD

Location: (920, 960), (2760, 3200), (4600, 960).

Description: Array of 8 n-diffusion resistors, width=3μm, length=1365μm folded, distance=112.5μm, depicted in Figure 4.6. Two point measurements.

Use: We will find the distance coefficient of the mismatch model.

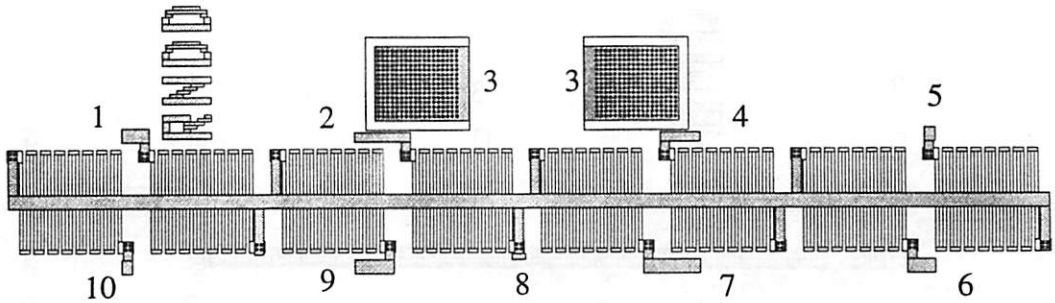


Figure 4.6 Array of N-Diffusion Resistors for the Distance Coefficient.

Structure 10: Pairs of N-Diffusion Resistors 1 for the Area Coefficient.

Label: RND1

Location: (920, 0), (2760, 2240), (4600, 0).

Description: 2 pairs of n-diffusion resistors, width=3µm, lengths=20µm and 31.5µm, distance=3µm, depicted in Figure 4.7. Four point measurements

Use: Together with the structures 11 and 12, we will find the area coefficient of the mismatch model.

Structure 11: Pairs of N-Diffusion Resistors 2 for the Area Coefficient.

Label: RND2

Location: (920, 320), (2760, 2560), (4600,320).

Description: 2 pairs of n-diffusion resistors, width=3µm, lengths=55.5µm and 125µm, distance=3µm, depicted in Figure 4.7. Four point measurements.

Use: Described above.

Structure 12: Pairs of N-Diffusion Resistors 3 for the Area Coefficient.

Label: RND3

Location: (920, 640), (2760, 2880), (4600, 640).

Description: 2 pairs of n-diffusion resistors with equal area, one with width=3µm and length=500µm and one with width=6µm and length=250µm, depicted in Figure 4.7.Four point measurements.

Use: Theoretically the two pairs should demonstrate the same mismatch. Information about the deltaW can be extracted.

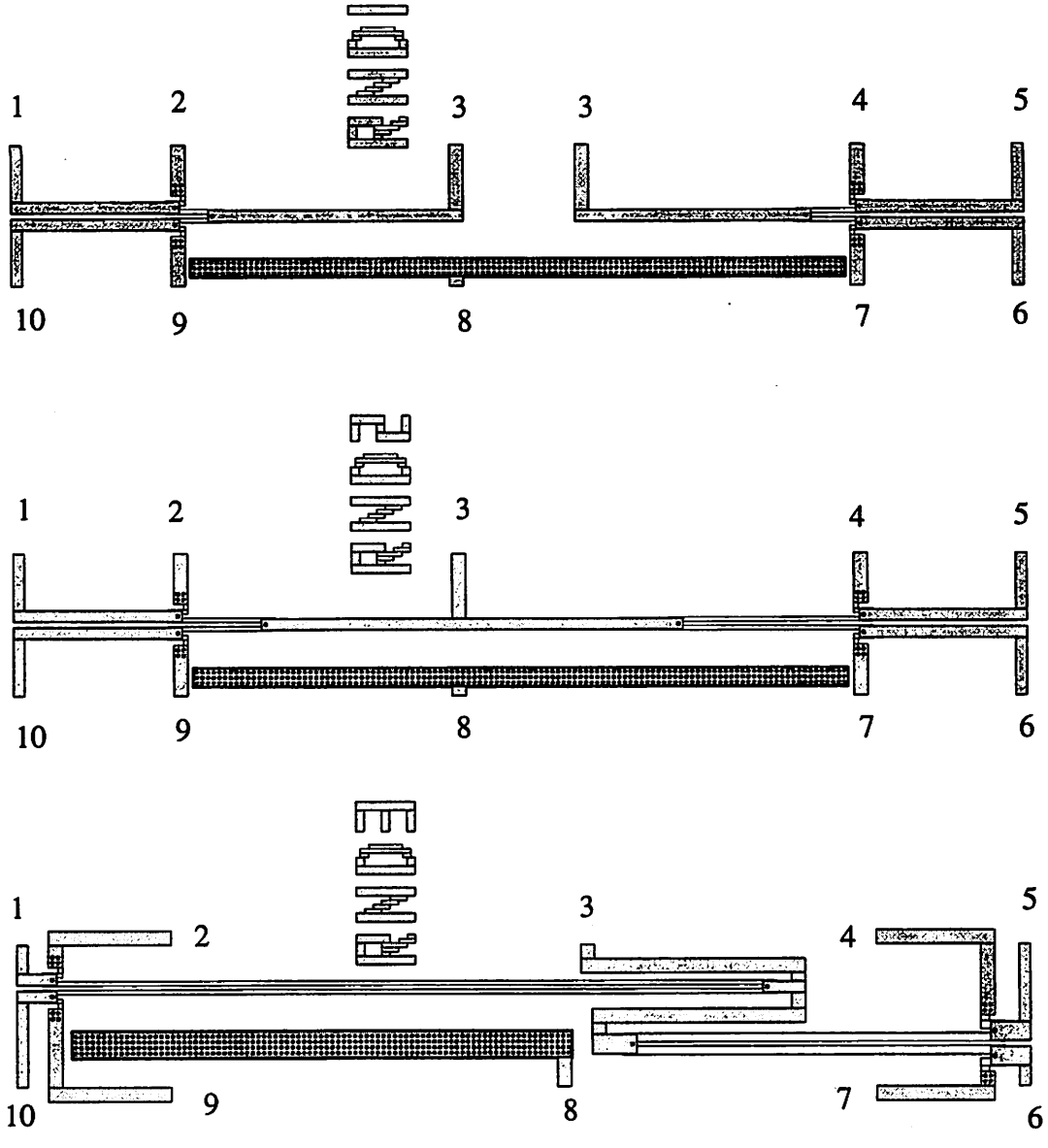


Figure 4.7 Pairs of N-Diffusion Resistors 1, 2 and 3 for the Area Coefficient.

4.3.4 P-Diffusion Resistor Mismatch Model

Information for the structures 13-16 is the same as for the structures 9-12, but here the devices are p-diffusion resistors. Their layout is similar to those of structures 9-12 also.

Structure 13: P-Diffusion Resistors for the Distance Coefficient.

Label: RPDD

Location: (920, 6720), (2760, 4480), (4600, 2240).

Structure 14: Pairs of P-Diffusion Resistors 1 for the Area Coefficient.

Label: RPD1

Location: (920, 5760), (2760, 3520), (4600, 1280).

Structure 15: Pairs of P-Diffusion Resistors 2 for the Area Coefficient.

Label: RPD2

Location: (920, 6080), (2760, 3840), (4600, 1600).

Structure 16: Pairs of P-Diffusion Resistors 3 for the Area Coefficient.

Label: RPD3

Location: (920, 6400), (2760, 4160), (4600, 1920).

4.3.5 Vertical Resistors

Structure 17: Pairs of Vertical Polysilicon and N-Diffusion Resistors.

Label: VN

Location: (1840, 1920), (4600, 6720).

Description: Contains (a) one pair of vertical poly resistors, width=2μm, length=125μm. (b) one pair of vertical n-diffusion resistors, width=3μm, length=125μm. It is depicted in Figure 4.8.

Use: We will examine if orientation is important in resistor matching. Four point measurements

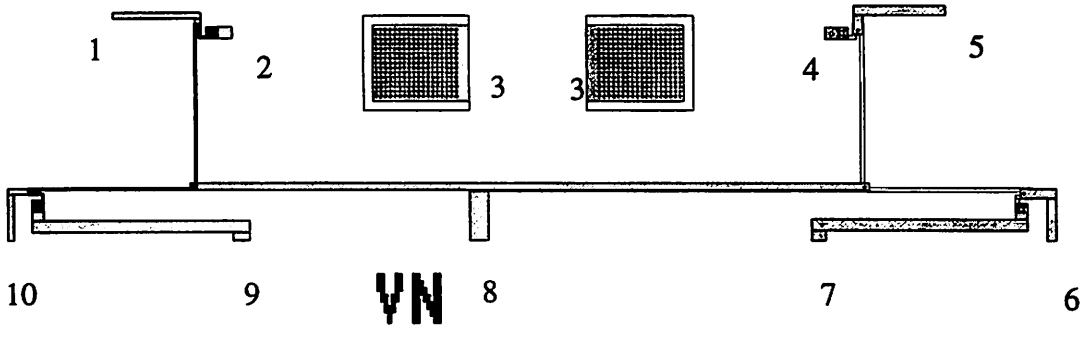


Figure 4.8 Pairs of Vertical Polysilicon and N-Diffusion Resistors.

Structure 18: Pairs of Vertical Polysilicon and P-Diffusion Resistors.

This is the same as structure 17, but the diffusion resistor is p-type here.

Label: VP

Location: (2760, 1280), (5520, 3840).

4.4 Capacitor Structures

4.4.1 Capacitor Arrays for Edge Effect Observation

Structure 19: Two dimensional Capacitor Array 1.

Label: CA1

Location: (920, 4480), (5520, 2880), (5520, 6080).

Description: 5x5 array of poly1-poly2 capacitors, side=15μm. Dummy capacitors with value 1/5, 2/5, 3/5, and 4/5 of the unit are included at the left and right end of the 2nd, 3rd, 4th and 5th from the top row respectively. Every 5 capacitors in a row share common bottom plate and every 5 in a column share common top plate. The values of the capacitors at each row will be compared together. In order to avoid introducing systematic difference in the measured value with interconnections of different length from the top plate to the pads, we introduced parasitic wiring to make the interconnection lengths equal and ensure equal contribution of the interconnection parasitic capacitance to all the capacitors in a row. This parasitic capacitance is important only when it is not eliminated during the measurement. It can be eliminated completely if the substrate is grounded. This structure is depicted in Figure 4.9.

Use: We will observe how large the dummy capacitor should be in order to compensate for the different environment of the capacitors at the end of the array.

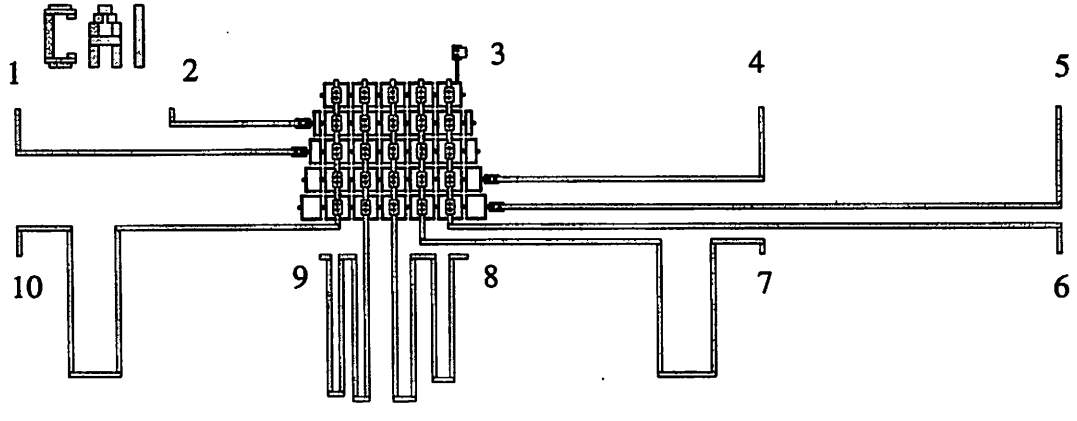


Figure 4.9 Two Dimensional Capacitor Array 1.

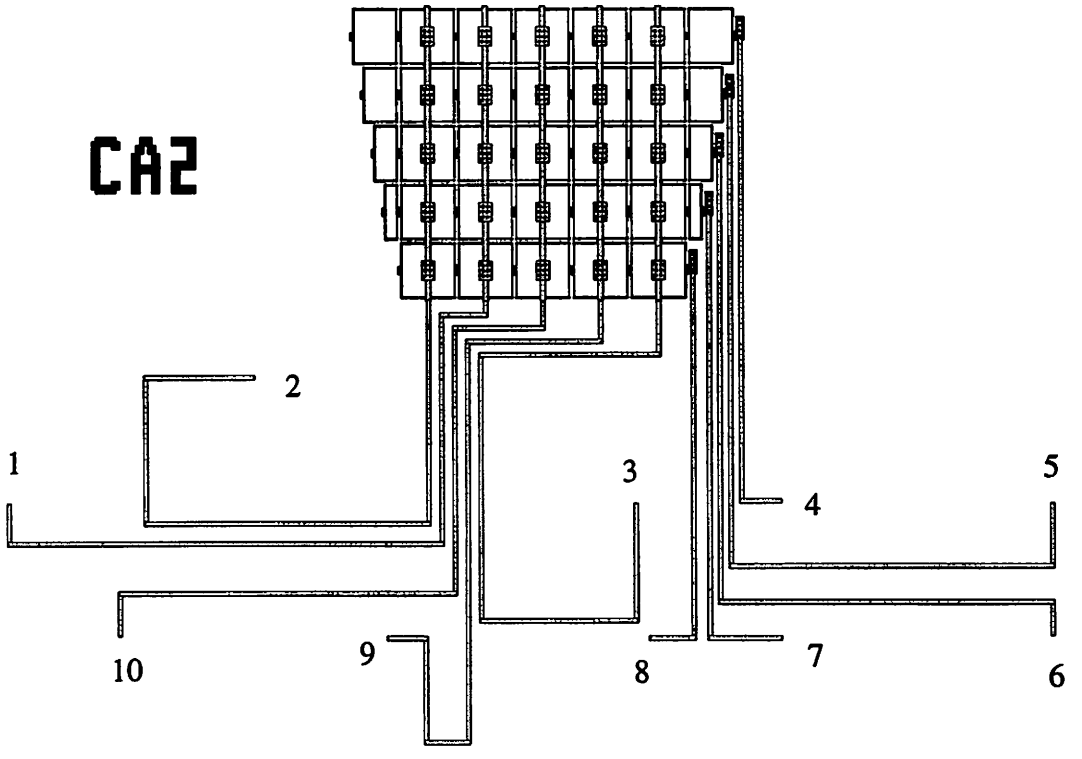


Figure 4.10 Two dimensional Capacitor Array 2.

Structure 20: Two dimensional Capacitor Array 2.

Label: CA2

Location: (920, 4800), (5520, 6400), (5520, 3200).

Description: 5x5 array of poly1-poly2 capacitors, side=40μm. Dummy capacitors with value 1/5, 2/5, 3/5, and 4/5 of the unit are included at the left end right end of the 2nd, 3rd, 4th and 5th row from the bottom are included. Parasitic wiring was introduced as in the capacitor array 1, depicted in Figure 4.10

Use: The same as for structure 19.

4.4.2 Capacitor Mismatch Model

Structure 21: Capacitors for the Distance Coefficient.

Label: CD

Location: (2760, 1920), (4600, 4160), (6440, 6720).

Description: Array of 9 large poly1-poly2 capacitors 78μm x 78μm, distance= 100μm, depicted in Figure 4.11.

Use: We will find the distance coefficient of the mismatch model.

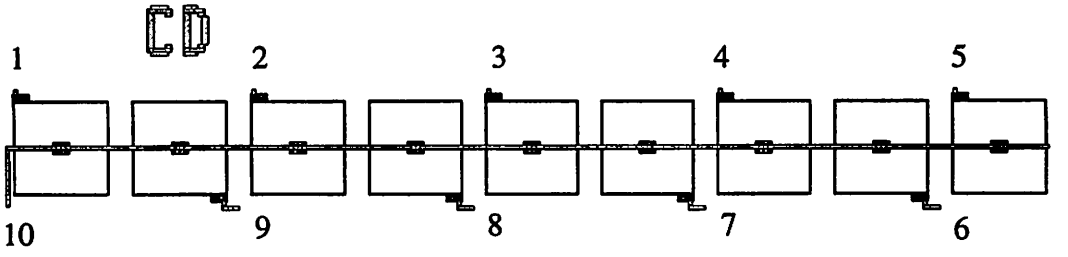


Figure 4.11 Array of Capacitors for the Distance Coefficient.

Structure 22: Pairs of Capacitors for the Area Coefficient.

Label: CS

Location: (2760, 1600), (4600, 3840), (6440, 6400).

Description: 4 pairs of poly1-poly2 capacitors, side= 22μm, 28.5μm, 44μm and 88μm, depicted in Figure 4.12.

Use: We will find the area coefficient of the mismatch model.

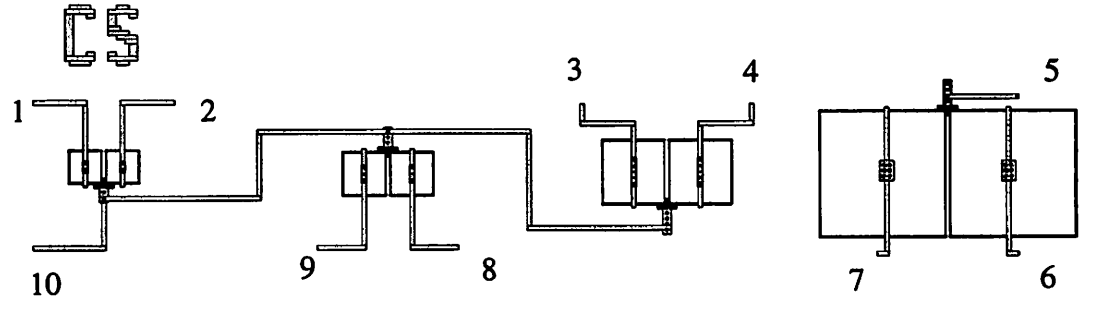


Figure 4.12 Pairs of Capacitors for the Area Coefficient.

4.5 Transistor Structures

4.5.1 Two Dimensional Transistor Arrays

Structure 23: Two Dimensional NMOS Transistor Array 1.

Label: NA

Location: (920, 2560), (3680, 0), (5520, 4160).

Description: 4x4 array of nmos transistors, W/L=20μm/2μm, horizontal distance=23μm, vertical distance=23μm, depicted in Figure 4.13.

Use: Observe neighboring effects.

Structure 24: Two Dimensional NMOS Transistor Array 2.

Label: NA2

Location: (920, 3200), (3680, 640), (5520, 4800).

Description: 4x4 array of nmos transistors, W/L=80μm/10μm, horizontal distance=84μm, vertical distance=31μm, depicted in Figure 4.14.

Use: Observe neighboring effects.

Structure 25: Two Dimensional PMOS Transistor Array 1.

This is the same as structure 23, but the devices are pmos here. The layout is similar also.

Label: PA

Location: (920, 2880), (3680, 320), (5520, 4480).

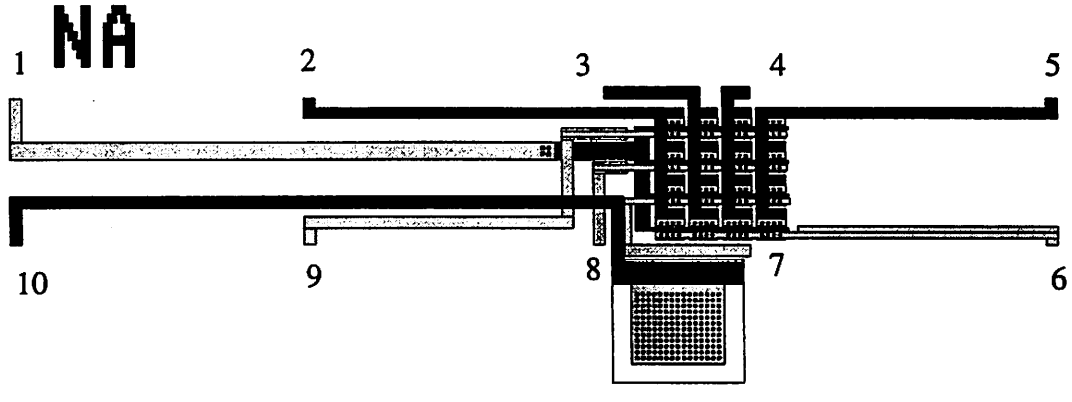


Figure 4.13 Two Dimensional NMOS Transistor Array 1.

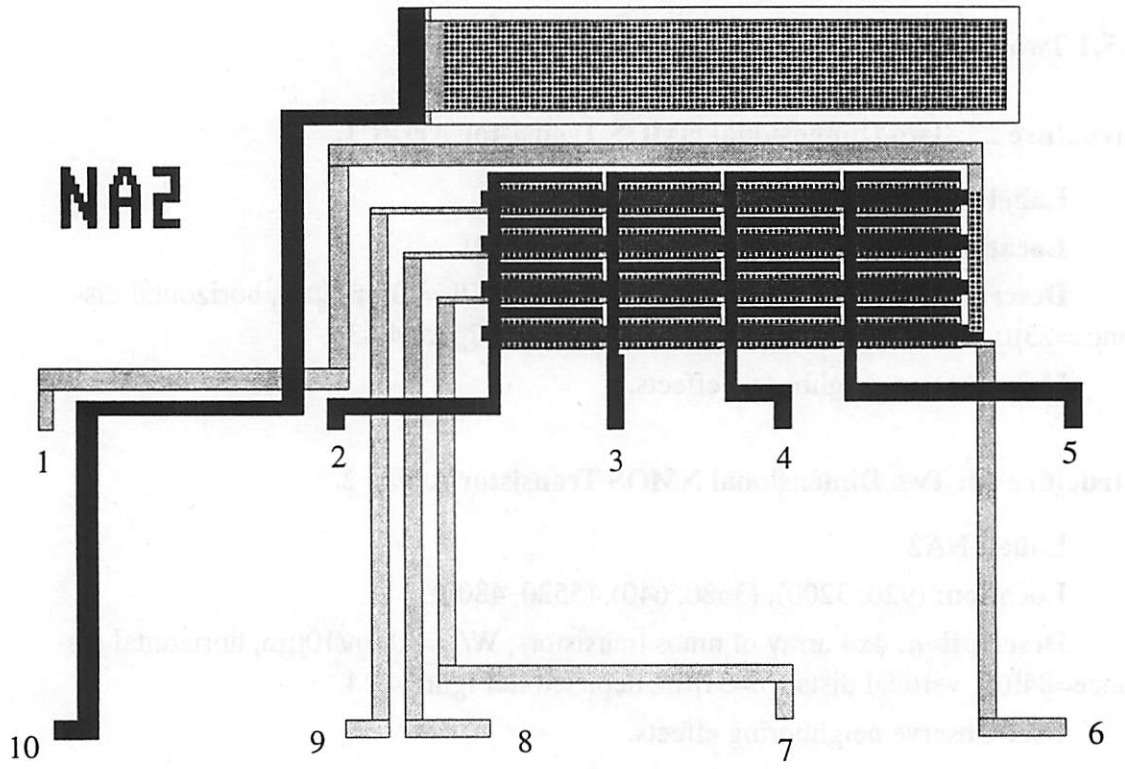


Figure 4.14 Two Dimensional NMOS Transistor Array 2.

Structure 26: Two Dimensional PMOS Transistor Array 2.

This is the same as structure 24, but the devices are pmos here. The layout is similar also.

Label: PA2

Location: (920, 3840), (3680, 1280), (5520, 5440).

4.5.2 NMOS Transistor Mismatch Model (Group A)

Structure 27: NMOS Transistors A for the Distance Coefficient.

Label: NTAD

Location: (1840, 2880), (3680, 2560), (6440, 640).

Description: Array of 7 large nmos transistors, W/L=65μm/10μm, distance= 128.5μm, depicted in Figure 4.15.

Use: We will find the distance coefficient of the mismatch model.

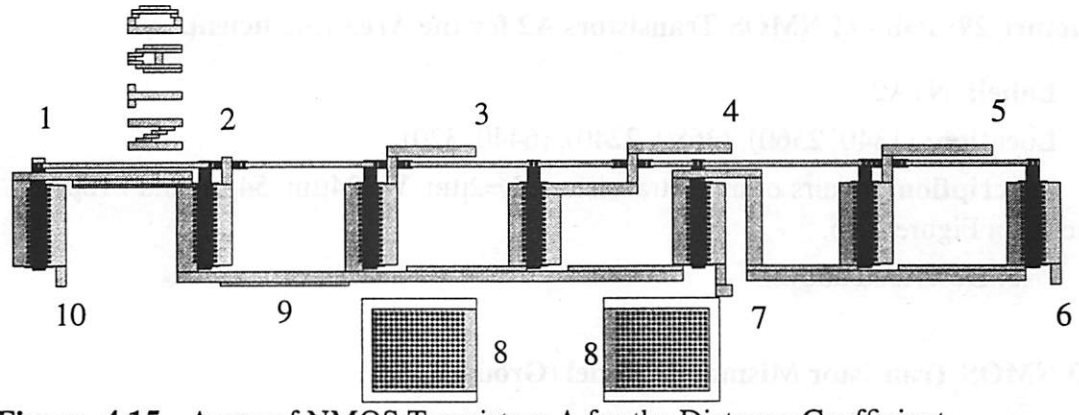


Figure 4.15 Array of NMOS Transistors A for the Distance Coefficient.

Structure 28: Pairs of NMOS Transistors A1 for the Area Coefficient.

Label: NTA1

Location: (1840, 2240), (3680, 1920), (6440, 0).

Description: 3 pairs of nmos transistors, L=2μm, W=6μm, 8.5μm and 13.5μm, depicted in Figure 4.16.

Use: Together with structure 29 we will find the area coefficient of the mismatch model.

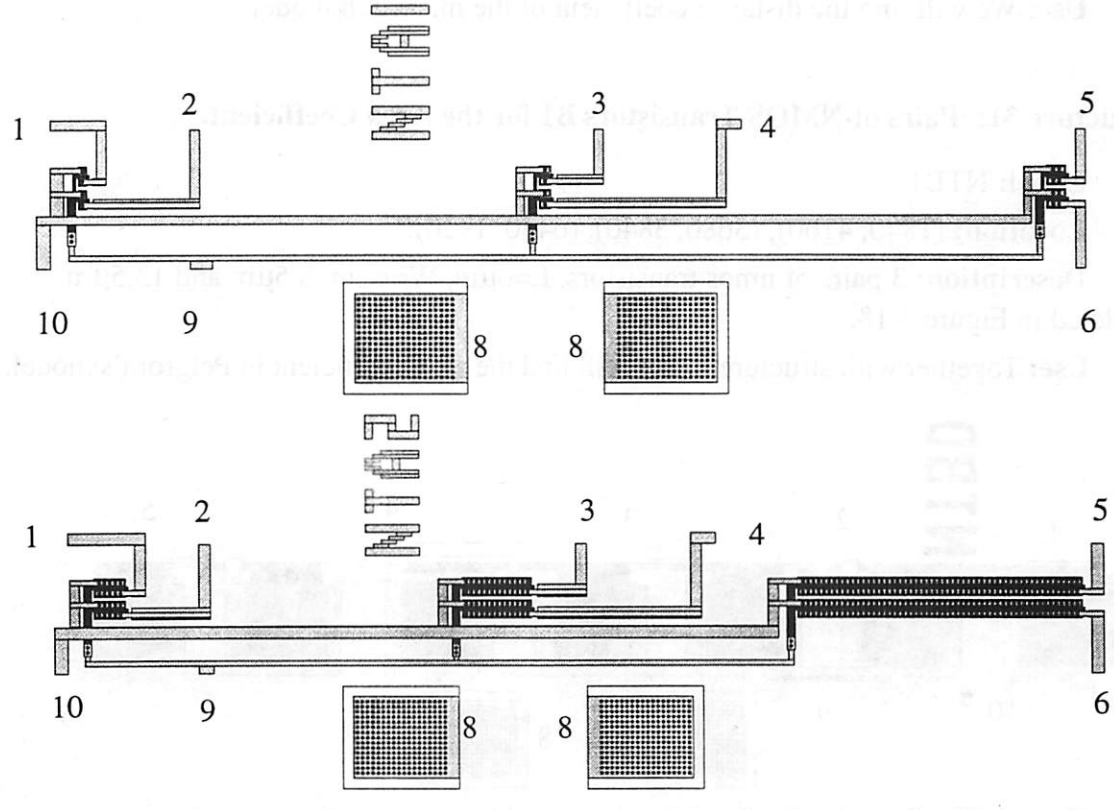


Figure 4.16 Pairs of NMOS Transistors A1 and A2 for the Area Coefficient

Structure 29: Pairs of NMOS Transistors A2 for the Area Coefficient.

Label: NTA2

Location: (1840, 2560), (3680, 2240), (6440, 320).

Description: 3 pairs of nmos transistors, L=2μm, W=24μm, 54μm and 216μm, depicted in Figure 4.16.

Use: Described above.

4.5.3 NMOS Transistor Mismatch Model (Group B)

We will find the coefficients of the mismatch model for nmos transistors again. This is a second group of devices with greater length.

Structure 30: NMOS Transistors B for the Distance Coefficient.

Label: NTBD

Location: (1840, 4800), (3680, 4480), (6440, 2560).

Description: Array of 7 large nmos transistors, W/L=65u/60u, distance= 128.5μm, depicted in Figure 4.17.

Use: We will find the distance coefficient of the mismatch model.

Structure 31: Pairs of NMOS Transistors B1 for the Area Coefficient.

Label: NTB1

Location: (1840, 4160), (3680, 3840), (6440, 1920).

Description: 3 pairs of nmos transistors, L=6μm, W=6μm, 8.5μm and 13.5μm, depicted in Figure 4.18.

Use: Together with structure 32 we will find the area coefficient in Pelgrom's model.

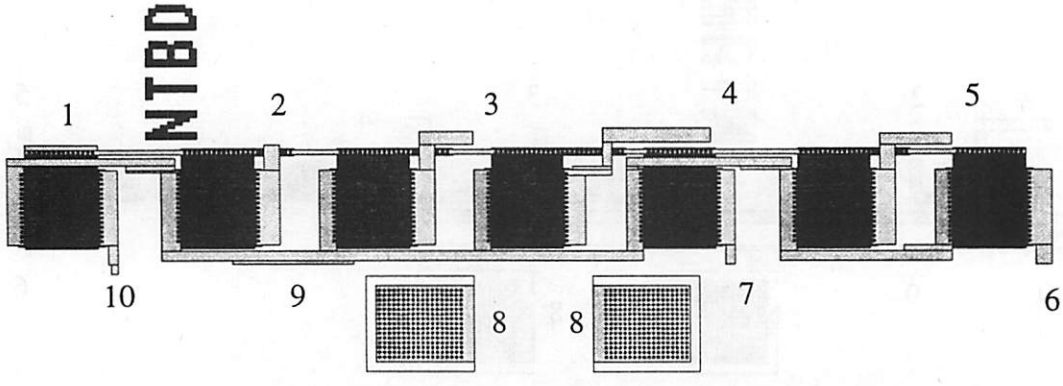


Figure 4.17 Array of NMOS Transistors B for the Distance Coefficient.

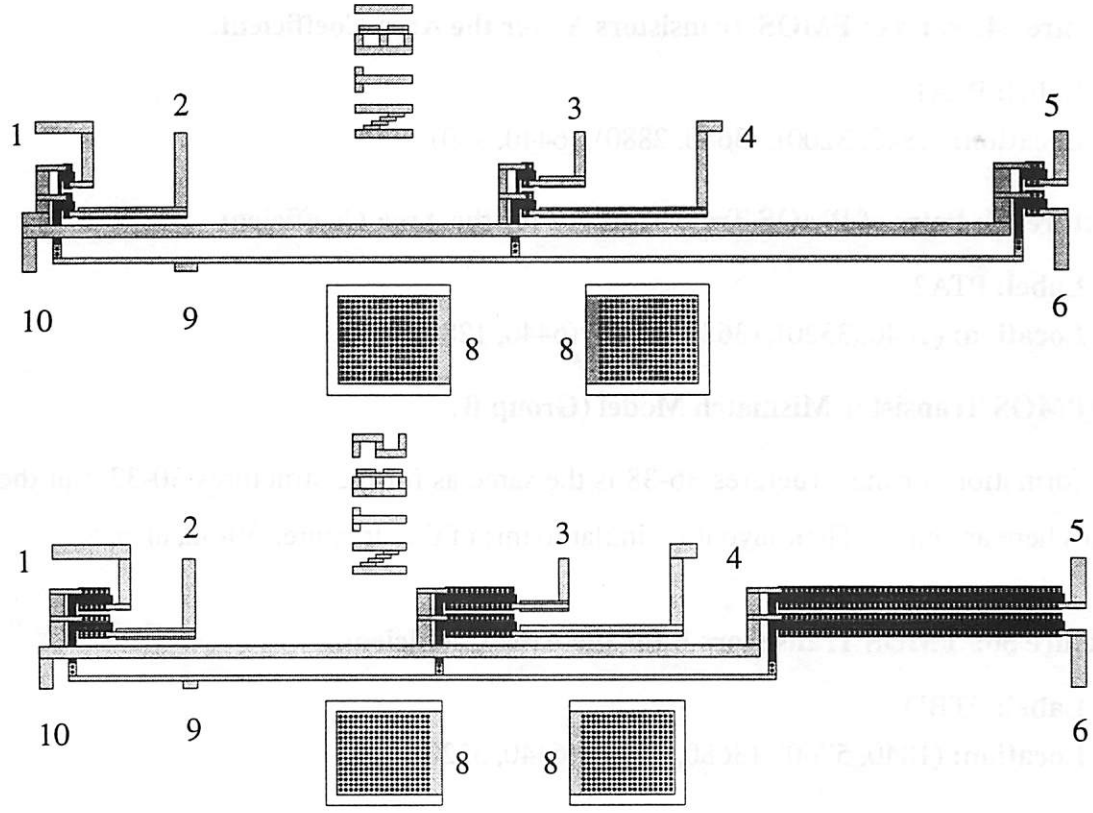


Figure 4.18 Pairs of NMOS Transistors B1 and B2 for the Area Coefficient.

Structure 32: Pairs of NMOS Transistors B2 for the Area Coefficient.

Label: NTB2

Location: (1840, 4480), (3680, 4160), (6440, 2240).

Description: 3 pairs of nmos transistors, L=6μm, W=24μm, 54μm and 216μm, depicted in Figure 4.18.

Use: Described above.

4.5.4 PMOS Transistor Mismatch Model (Group A)

Information for the structures 33-35 is the same as for the structures 27-29, but the devices here are pmos. Their layout is similar to this of the structures 27-29, also.

Structure 33: PMOS Transistors A for the Distance Coefficient.

Label: PTAD

Location: (1840, 3840), (3680, 3520), (6440, 1600).

Structure 34: Pairs of PMOS Transistors A1 for the Area Coefficient.

Label: PTA1
Location: (1840, 3200), (3680, 2880), (6440, 960).

Structure 35: Pairs of PMOS Transistors A2 for the Area Coefficient.

Label: PTA2
Location: (1840, 3520), (3680, 3200), (6440, 1280).

4.5.5 PMOS Transistor Mismatch Model (Group B)

Information for the structures 36-38 is the same as for the structures 30-32, but the devices here are pmos. Their layout is similar to this of the structures 30-32, also.

Structure 36: PMOS Transistors B for the Area Coefficient.

Label: PTBD
Location: (1840, 5760), (3680, 5440), (6440, 3520).

Structure 37: Pairs of PMOS Transistors B1 for the Distance Coefficient.

Label: PTB1
Location: (1840, 5120), (3680, 4800), (6440, 2880).

Structure 38: Pairs of PMOS Transistors B2 for the Distance Coefficient.

Label: PTB2
Location: (1840, 5440), (3680, 5120), (6440, 3200).

4.5.6 Orthogonal Experiment with NMOS Transistors

Orthogonal experiment [22] to observe combined effect of size distance and orientation in the mismatch of pairs of nmos transistors. Size: W/L=6μm/2μm and 60μm/6μm. Distance: 20μm and 200μm. Because of different transistor sizes and different orientation these distances are not exact but approximate.Orientation parallel and vertical. Since the three factors are uncorrelated sources of mismatch, we do not expect to find any significant interaction terms. We will essentially observe the effect of orientation in four different cases.

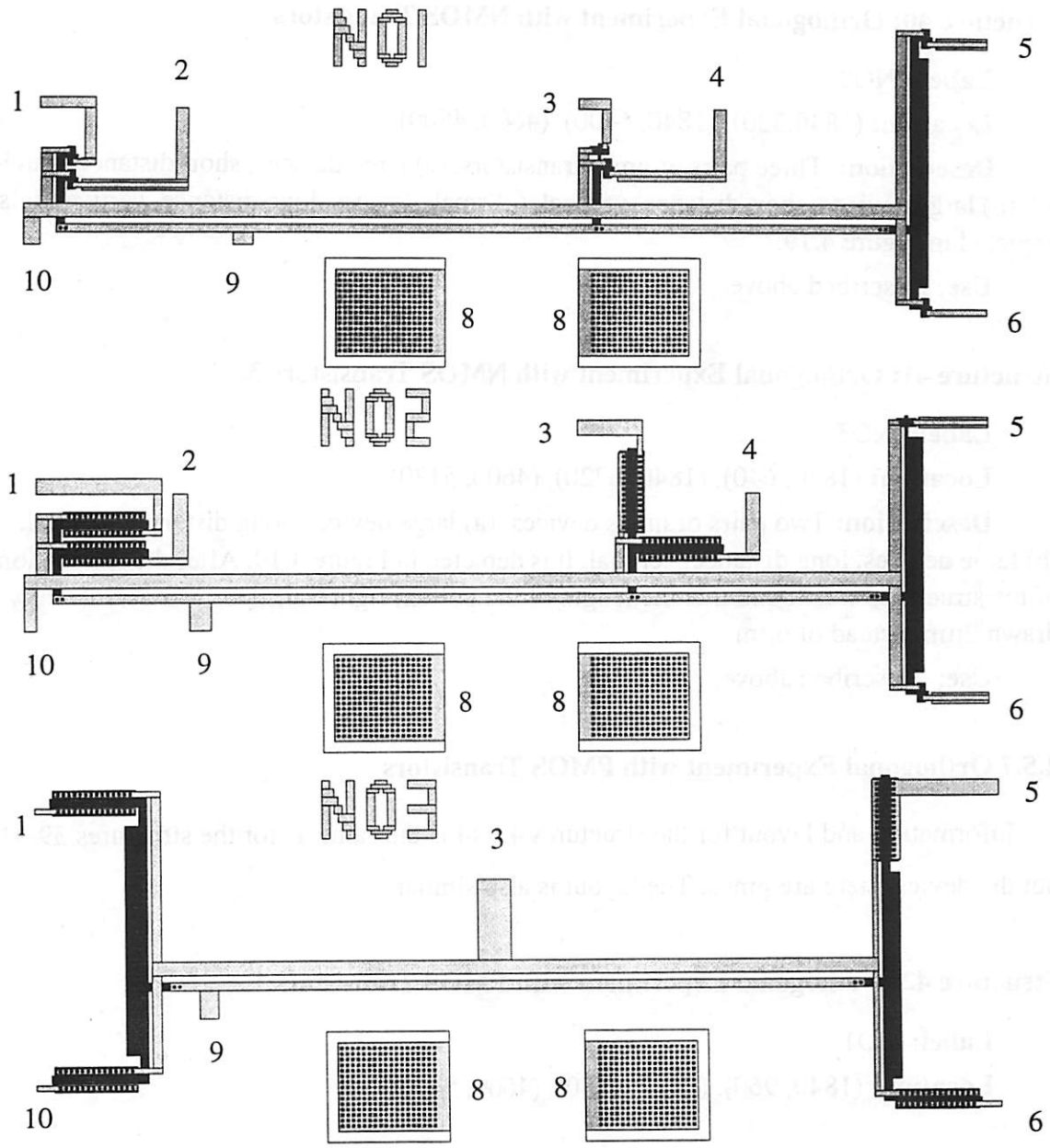


Figure 4.19 Orthogonal Experiment with NMOS Transistors 1, 2 and 3.

Structure 39: Orthogonal Experiment with NMOS Transistors 1.

Label: NO1

Location: (1840, 0), (1840, 6080), (4600, 4480)

Description: Three pairs of nmos transistors. (a) small devices, short distance, parallel, (b) small devices, short distance, vertical, (c) small devices, long distance, parallel. It is depicted in Figure 4.19.

Use: Described above.

Structure 40: Orthogonal Experiment with NMOS Transistors 2.

Label: NO2

Location: (1840,320), (1840, 6400), (4600, 4800).

Description: Three pairs of nmos transistors. (a) large devices, short distance, parallel, (b) large devices, short distance, vertical, (c) small devices, long distance, vertical. It is depicted in Figure 4.19.

Use: Described above.

Structure 41: Orthogonal Experiment with NMOS Transistors 3.

Label: NO3

Location: (1840, 640), (1840, 6720), (4600, 5120).

Description: Two pairs of nmos devices. (a) large devices, long distance, parallel. (b) large devices, long distance, vertical. It is depicted in Figure 4.19. After the fabrication of the structures was found that the length of the bottom right transistor was accidentally drawn 2μm instead of 6μm.

Use: Described above.

4.5.7 Orthogonal Experiment with PMOS Transistors

Information and layout for the structures 42-44 is the same as for the structures 39-41, but the devices here are pmos. The layout is also similar.

Structure 42: Orthogonal Experiment with PMOS Transistors 1.

Label: PO1

Location: (1840, 960), (2760, 6080), (4600, 5440).

Structure 43: Orthogonal Experiment with PMOS Transistors 2.

Label: PO2

Location: (1840, 1280), (2760, 6400), (4600, 5760).

Structure 44: Orthogonal Experiment with PMOS Transistors 3.

Label: PO3

Location: (1840, 1600), (2760, 6720), (4600, 6080).

Description: As for the NMOS case, the length of the bottom right transistor was accidentally drawn 2μm instead of 6μm.

4.6 Simple Circuits

This group includes four differential pairs and one operational amplifier. We use an external current source to bias the circuits. We will predict offset using information from individual transistors and then measure it and compare with the prediction.

4.6.1 Differential Pairs

Structure 45: Differential Pair 1.

Label: DF1

Location: (2760, 0), (3680, 5760), (6440, 3840).

Description: Load devices: 20μm/2μm, Input devices:20μm/2μm. It is depicted in Figure 4.20 together with the differential pairs 2, 3 and 4. The schematic of the all four differential pairs is shown in Figure 4.21. In order to be able to measure device parameters of the transistors, individual transistors identical to the input and load devices have been included in the layout.

Use: Described above.

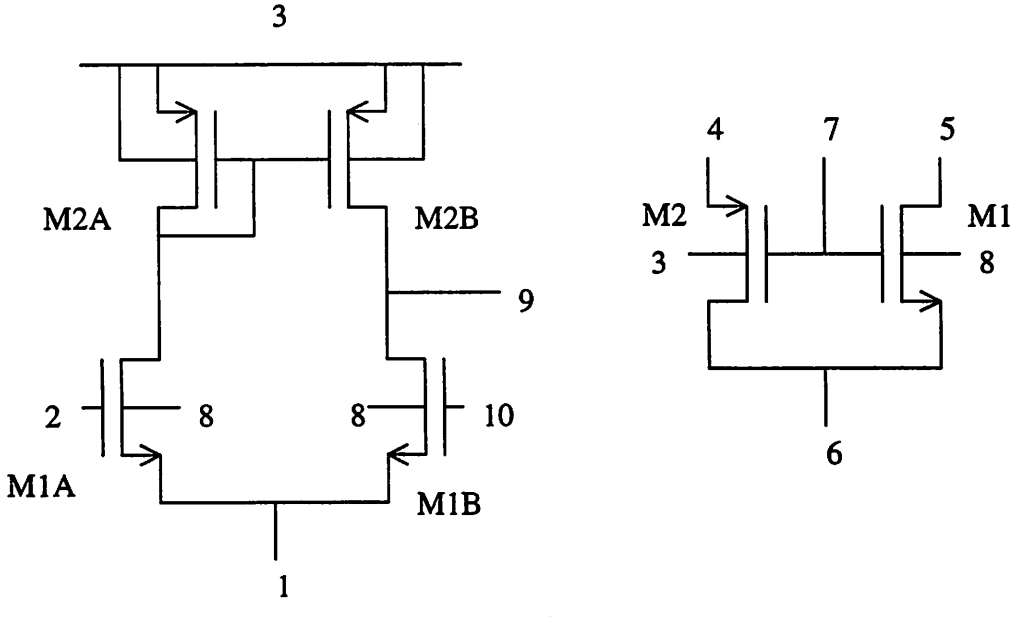


Figure 4.21 Schematic of the differential pairs.

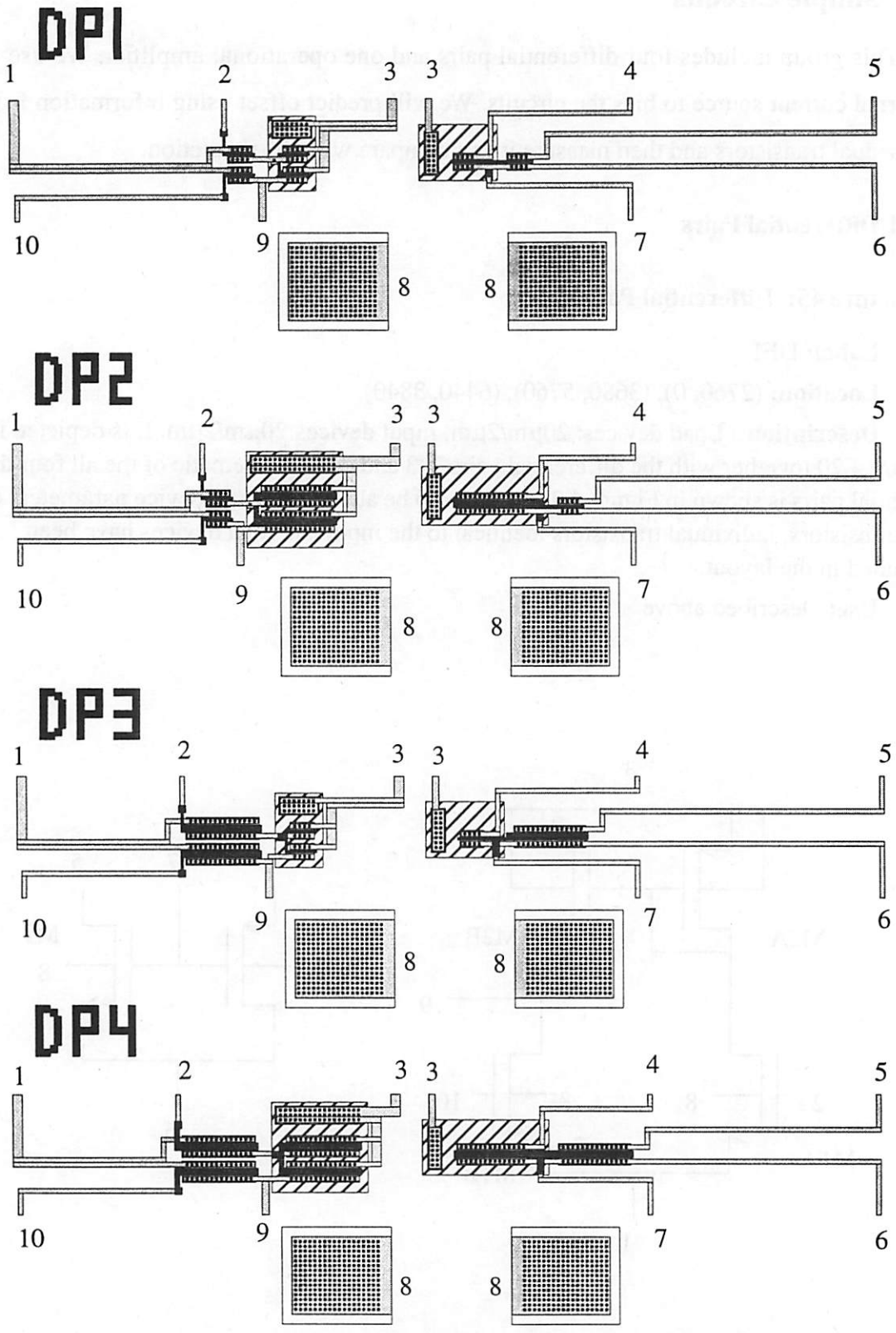


Figure 4.20 Differential Pairs 1, 2, 3, and 4.

Structure 46: Differential Pair 2.

Label: DF2

Location: (2760, 320), (3680, 6080), (6440, 4160).

Description: Similar to this of structure 45. Here Load devices: 60μm/6μm, Input devices:20μm/2μm.

Use: Described above.

Structure 47: Differential Pair 3.

Label: DF3

Location: (2760, 640), (3680, 6400), (6440, 4480).

Description: Similar to this of structure 45. Here Load devices: 20μm/2μm, Input devices:60μm/6μm.

Use: Described above.

Structure 48: Differential Pair 4.

Label: DF4

Location: (2760, 960), (3680, 6720), (6440, 4800).

Description: Similar to this of structure 45. Here Load devices: 60μm/6μm, Input devices:60μm/6μm.

Use: Described above.

4.6.2 Operational Amplifier

Structure 49: OPAMP

Label: OP

Location: (920, 5440), (4600, 6400), (1920, 0).

Description: A simple opamp, depicted in Figure 4.22. Its schematic is shown in Figure 4.23. The device sizes are shown in Table 4.1. Transistors M1C and M3C are copies of the transistors M1A and M3 respectively. These devices are critical for the frequency response. It is possible that measurements from these individual transistors will be desirable in the future.

Use: We will predict offset and then measure it and compare with the prediction.

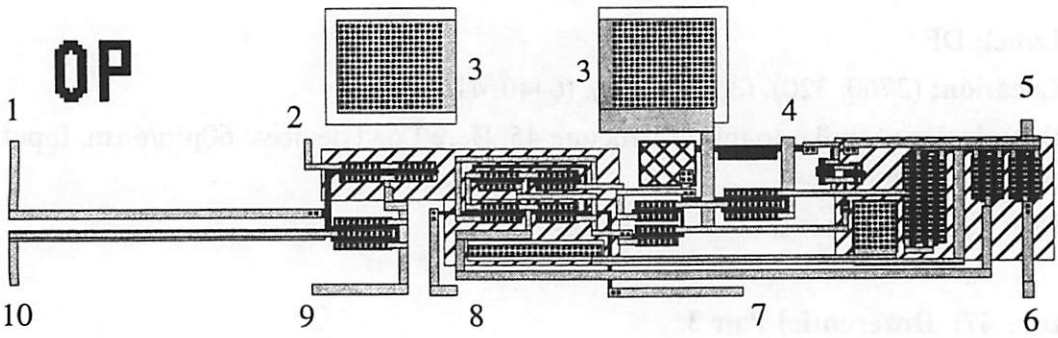


Figure 4.22 Operational Amplifier.

Table 4.1 Device Sizes of the OPAMP (in μm).

Device	Size	Device	Size
M1A	60/2	M5	60/2
M1B	60/2	M6	60/2
M2A	30/2	M7	6/6
M2B	30/2	M8	9/3
M3	80/2	CF	29x38
M4	180/2		

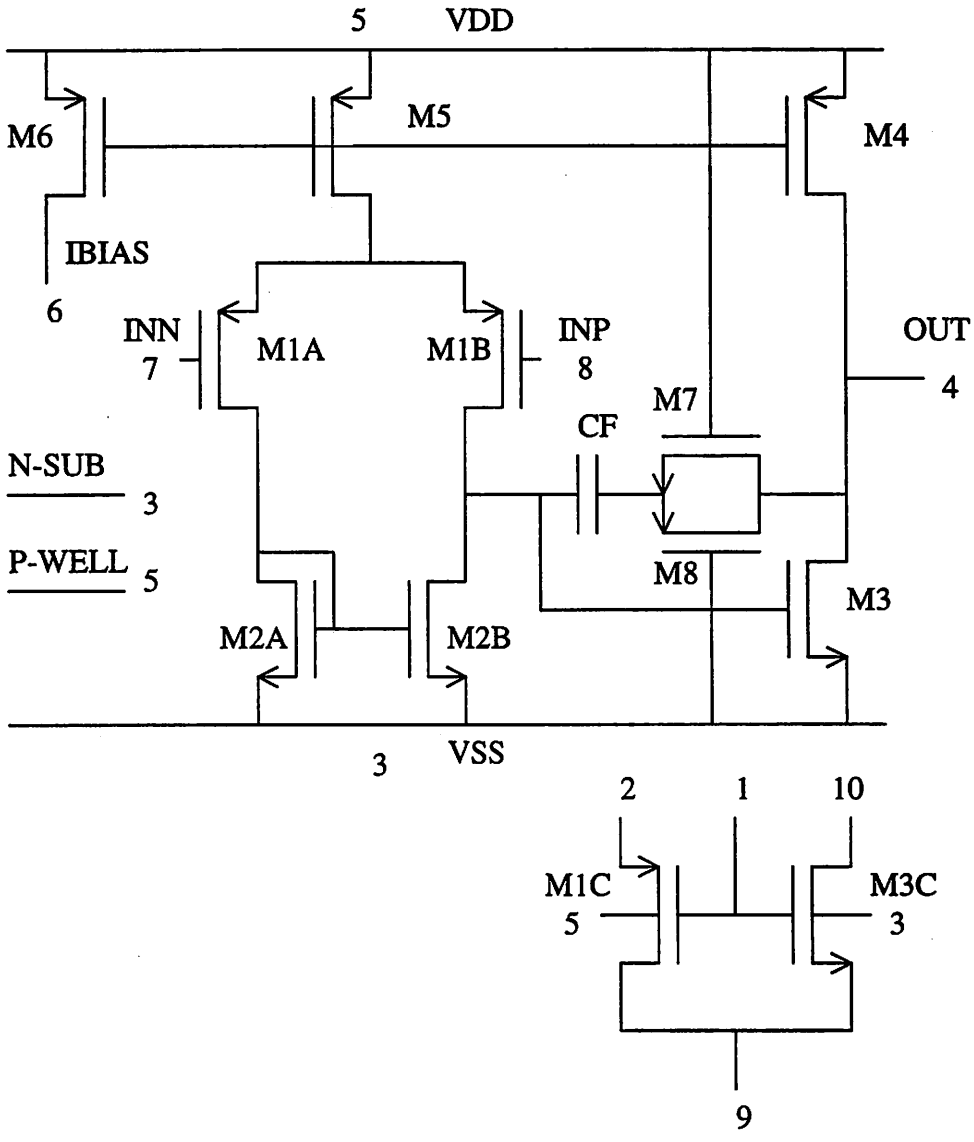


Figure 4.23 Schematic of the Operational Amplifier

Chapter 5

Measurements

5.1 Introduction

Here we describe the measurements taken form the structures presented in the previous chapter. Measurement methodology is presented first. Graphs and tables that summarize the statistical behavior of the measured quantities follow. Below we shall refer to the different structures using the label printed next to each one of them, as given in Chapter 4.

5.2 Equipment

The equipment used for the measurements includes an Electroglass 2001X automatic wafer prober and an HP 4062A Semiconductor Parametric Test System consisting of an HP4085A Switching Matrix, an HP4084A Switching Matrix Controller, an HP4141 DC Source/Monitor unit, and an HP4280A C Meter / C-V plotter.

The structures have been fabricated on 4-inch wafers in the Berkeley Microfabrication Laboratory. There are 52 dice on each wafer. The results presented below represent measurements from one wafer.

5.3 Measurement Methodology

In order to obtain accurate measurements and to check their repeatability we took each measurement 4 times and considered the average. The variance was in almost all cases less than 0.3%, while the advertised equipment resolution for the applied and measured currents and voltages is 0.1%, for the magnitude range used. Therefore, our measurements have an accuracy of 0.15%. The measured variance could have been used for data screening, also. However, we simply removed the outliers from every set of measurements.

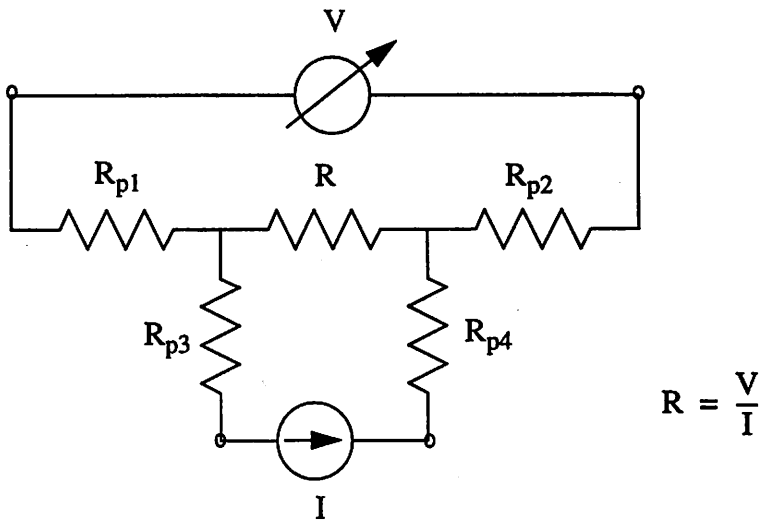


Figure 5.1 Four point resistance measurement.

5.3.1 Resistors

The resistors with relatively low nominal value are measured with four point measurement, as shown in Figure 5.1. The measurement of resistor R is desirable while R_{p1}, R_{p2}, R_{p3}, and R_{p4} are parasitic resistors. We apply a current through resistor R and the parasitic resistors R_{p3} and R_{p4}, and we measure the voltage drop across R using a different pair of terminals. Since the internal resistance of the voltmeter is very high, the current through the parasitic resistors R_{p1} and R_{p2} is almost zero and the voltage drop across them is zero also. In this way the parasitic resistors do not affect the measurement.

Resistors with large nominal value are measured with two point measurement, by applying a current and measuring the voltage on the same pair of terminals, since in this case the parasitic resistances are negligible compared to the high value of the resistor.Equivalent to applying a current, is applying a voltage, so long as we can measure the current through the voltage source. This is actually what we did in practice.

5.3.2 Capacitors

When the substrate is not grounded, the series combination of the top and the bottom plate parasitic capacitances is measured together with the desirable capacitance. This can

be avoided when the substrate is grounded, as shown in Figure 5.2. Indeed, we are able to connect the chuck to the ground and therefore the parasitic capacitances from the top and the bottom plates do not affect the measurements.

An other issue relative to capacitance measurement with an automatic wafer prober is calibration. The cable, switch matrix, and probe pins have stray parasitic capacitances and resistances that affect the measured value. The HP4280A is equipped with error correction which can be performed up to the measurement pins, by disconnecting them from the HP4280A terminals. However parasitic capacitance among the pins remains and is connected in parallel to the capacitance that we want to measure. One solution is to land the pins on oxide or on a pad set with no structures connected to it (such a pad set exists in the scribe lane when second metal layer has not been deposited yet) in order for the pins to obtain the configuration they have during the actual measurement, measure the capacitance between every two pins and keep the measured values in a matrix. During the actual measurement of a capacitor connected between two pins, the corresponding value of the matrix must be subtracted from the measured value. This way of calibration is recommended in the HP4062A manual.

The experiment shows that this way of calibration is not very accurate. For example when we measure the pair of capacitors of the structure for the area coefficient CS, with

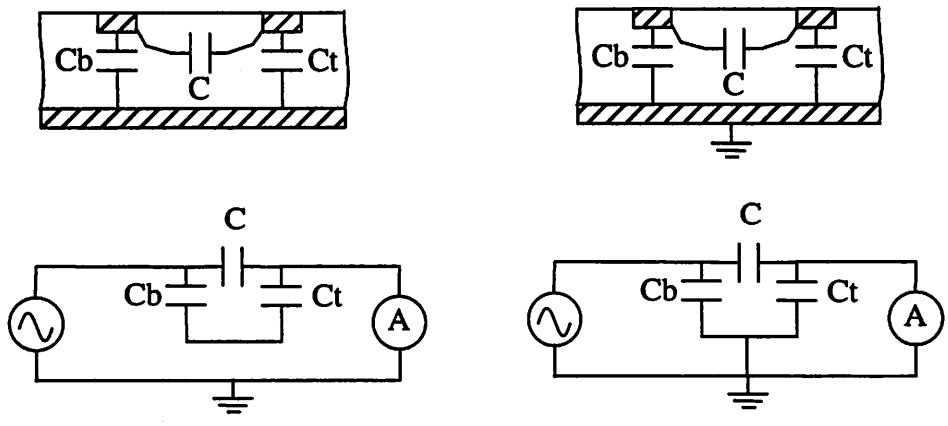


Figure 5.2 Capacitance measurement.

side 22 μm, we obtain a systematic difference approximately equal to 35fF, while there is not physical reason for the two capacitors to be different. The average value for the capacitors of this size is approximately 0.28pF. In this case and in the case of the structure for the distance coefficient CD, the systematic difference can be subtracted with software, since only the variance between the two capacitors of the pair is of interest. Unfortunately this cannot be done for the two dimensional arrays CA1 and CA2, were there is no guarantee that the capacitors are equal, and the difference in their measured values could be because of different environment around the capacitors and also of incomplete calibration.

5.3.3 Transistors

From the transistors we extract threshold voltage, current factor and body effect coefficient. The threshold voltage V_T is extracted from the curve of drain current I_D versus the gate-source voltage V_{GS}, as shown in Figure 5.3. The transistor is kept in the linear region by applying constant drain-source voltage V_{DS} = 50mV. We draw the straight line that is tangent to the curve and has maximum slope. This line intersects the horizontal axis at V_T. The slope of this line is the current factor β. The body effect coefficient γ is found by measuring the threshold voltage for two different values of source-body voltage V_{SB}, 0 and -3V. Then according to (2.44) the coefficient γ is given by:

$$\gamma = \frac{V_T - V_{T0}}{\sqrt{V_{SB} + 2\Phi_B} - \sqrt{2\Phi_B}} \tag{5.1}$$

where V_{T0} is the threshold voltage for V_{SB}=0V, V_T is the threshold voltage for V_{SB}=-3V, and Φ_B is a logarithmic function of the doping concentration of the channel and can be considered constant.

Using the change of the slope of the curve for $V_{GS}>V_T$, information about the equivalent source resistance can be extracted. Such an equivalent resistance represents actual ohmic resistance of the source diffusion, the source contacts and the interconnection path to the measuring instrument, and mobility degradation because of velocity saturation. When the equivalent source resistance is an outlier of the set of measured source resistors of similar transistors, we can use this information to discard the measured values of the

other parameters of a transistor. The equivalent source resistance is actually extracted by our extraction routine, but it was not used for data screening.

5.3.4 Differential Pairs and OPAMP

In order to measure the input offset voltage of the differential pairs and the operational amplifier, we obtain their dc transfer characteristic; i.e., the output voltage as a function of the differential input voltage, as shown in Figure 5.4. Because of the finite output resistance of the transistors, the curve has a finite slope in the transition from the low to the high saturation level and is not infinite as was considered in section 3.3 . The input offset voltage V_{off} is found here as the differential input voltage that drives the output to a predefined output voltage level V_M. The finite output resistance of the transistors creates the systematic component of the input offset. For the differential pairs, this systematic component can be eliminated if we select V_M equal to V_{DD}-V_{GS2}, where V_{DD} is the positive power supply and V_{GS2} is the gate-source voltage of transistors M2A and M2B in Figure 4.21. In this way the drain-source voltages of the transistors in the two branches of the dif-

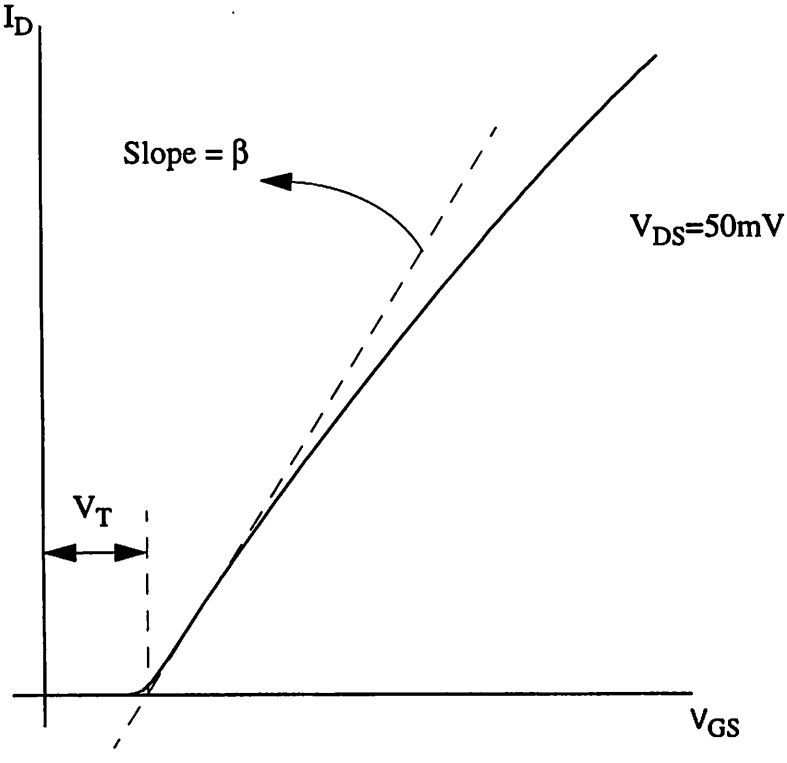


Figure 5.3 Threshold voltage and current factor extraction.

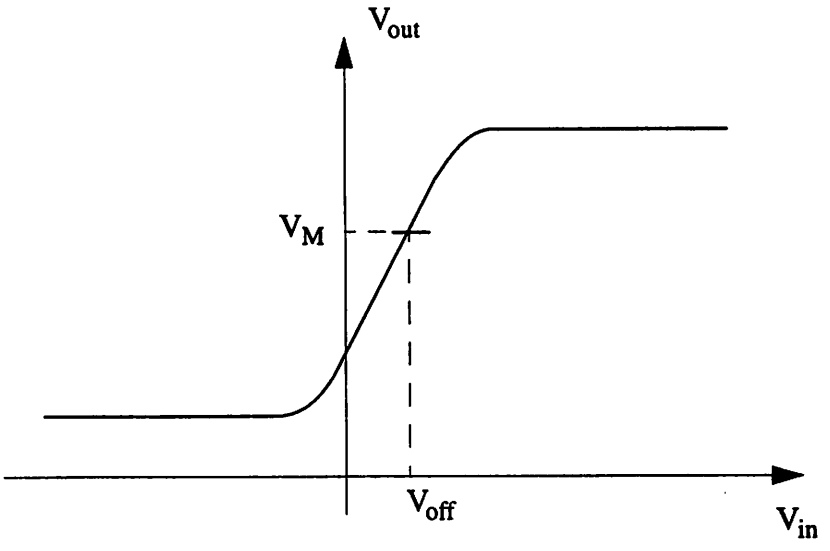


Figure 5.4 Input Offset Voltage for the Differential Pairs and the OPAMP.

ferential pair are identical, and the current difference because of the output resistance of the transistors is eliminated. The operational amplifier has two gain stages, and the dc transfer characteristic curve is very steep, so we could just use the middle of the output range for V_M. A nonzero mean of the input offset voltage could be assigned to the systematic component. In both cases, differential pairs and operational amplifier, we ignore the mismatch in the output resistance between the transistors of each transistor pair, since it is a second order phenomenon, and we can use the formulas derived in Chapter 3.

5.4 Measurement Problems

Because of fabrication problems during the threshold voltage adjustment implantation in the Berkeley Microfabrication Laboratory, the NMOS devices are not functional. Therefore neither the structures that contain single NMOS transistors, nor the differential pairs and the operational amplifier are functional. Because deposition of metal 2 would require longer fabrication time, and experience has shown that it is not reliable in this fabrication line, metal 2 was not used and the transistor arrays of the structures 23-26 (NA, NA2, PA, PA2) are not functional. Finally we encountered serious problems with the auto-

matic wafer prober whose failure interrupted our measurements. However, many of the designed parameters were measured, and the obtained results are given below.

5.5 Resistor Results

5.5.1 Resistor Arrays Edge Effects Observation

We present here the result of the measurements from the structures 1-4 (RAP1, RAP2, RAND, and RAPD). The mean values of the resistors in these structures are shown in Table 5.2. In this table we also show how many of the arrays were fully functional, out of

Table 5.1 Resistors for Edge Effect Observation.

Structure	W(μm)	L(μm)	mean R(Ω)	functional arrays
RAP1	2	600	6,108	153
RAP2	2	600	3,159	153
RAND	3	600	9,474	154
RAPD	3	600	12,630	153

the 52*3=156 that exist on the wafer. An array is considered fully functional if the measured values of all of the resistors in it are not outliers of the set of the similar resistors.

The result is depicted in Figure 5.5. The horizontal axis is distance on an axis perpendicular to the length of the resistors. Each boxplot represents the span of the value of one resistor in the array. Since only the local variation within the array is of interest here, the average within the array has been subtracted from the values of the resistors. The superposition of the remaining quantities for all the arrays of the same kind is depicted in these figures. The distance between the centers of two successive resistors is 4 μm for the structure RAP1, 6 μm for RAP2 and 6 μm for the diffusion structures RAND and RAPD. The black dot represents the median, the box around it shows the upper and the lower quartile, and the whiskers include all the data that are not outliers. The empty dots outside the whiskers represent outliers.

In the polysilicon resistor arrays we observe a clear trend of the leftmost and the rightmost resistor in the array to have higher value than the rest. Even the resistors next to the leftmost and the rightmost tend to have higher values than those in the middle of the array. The phenomenon is more intense for the 2 μm-wide poly lines (RAP1) and less for the 4 μm-wide (RAP2), and indicates that the polysilicon lines next to open area are more narrow. This result can be attributed to optical phenomena of the stepper such as diffraction, as well as to different polysilicon etching rates at the edges and in the middle of the array. The latter is caused by different densities of the etching solution in regions that are close to open area versus regions with dense polysilicon geometry. It is worth noticing in both structures RAP1 and RAP2 that the rightmost resistor has a higher value than the leftmost. Since the environment around the structure is identical on the left and the right side, this

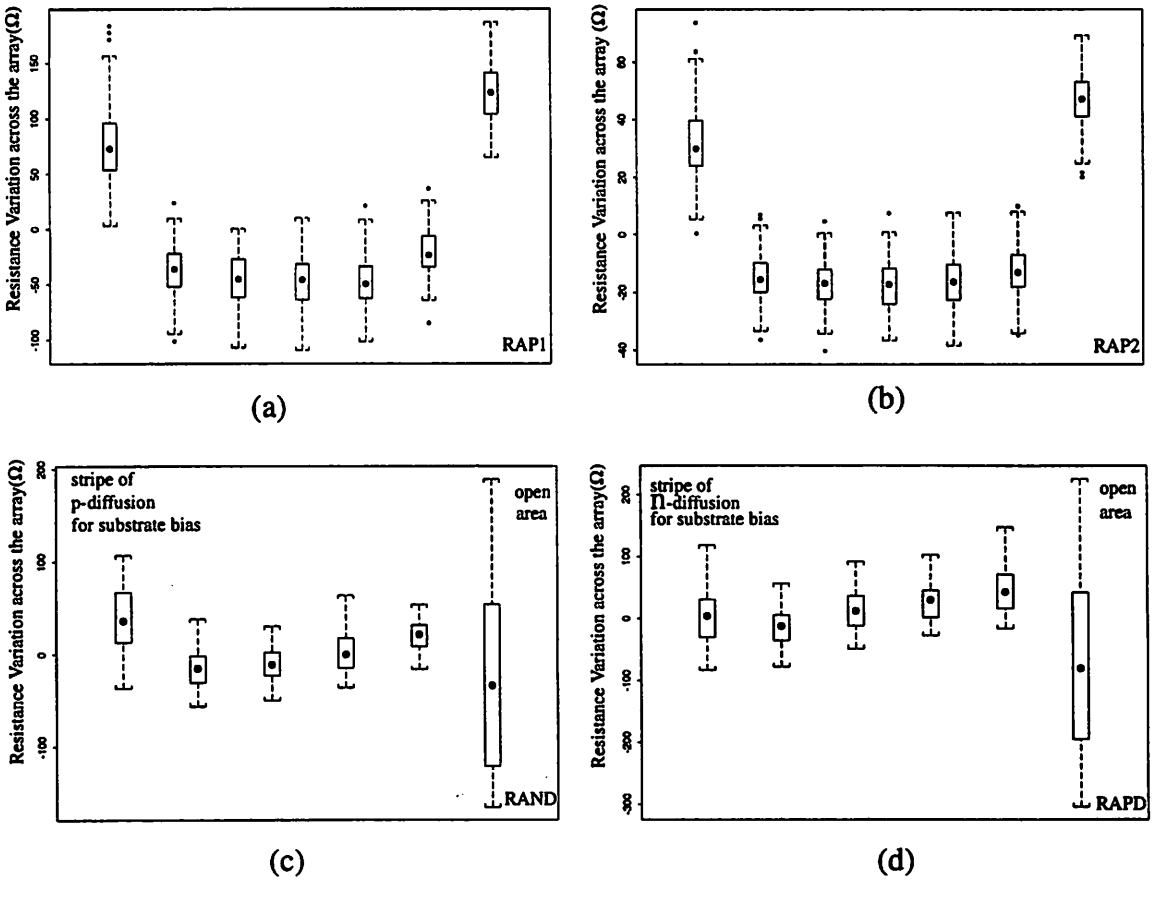


Figure 5.5 Resistance variation in the array of a) polysilicon resistors 1, b) polysilicon resistors 2, c) n-diffusion resistors, and d) p-diffusion resistors.

result can be attributed only to slightly non-vertical polysilicon etching in the plasma chamber.

The structures of the n- and p- diffusion resistors give almost identical profiles. The leftmost resistor corresponds to the one that is next to the diffusion stripe of the opposite kind used to bias the substrate, as is shown in Figure 4.3. The rightmost resistor corresponds to the one that is next to the open area. We observe that the resistor next to open area has lower median value and much higher variance than the rest. Individual boxplot graphs from arrays located in the 3 positions in the die show that the median of the rightmost resistor is not always lower than that of the rest, so we do not have evidence to accept this as a conclusion. However, the variance of the resistor next to open area is consistently higher. This result could also be related to the optical phenomena during the definition of the active area.

5.5.2 Polysilicon Resistor Mismatch Model

Here we present the measurements used for the estimation of the two coefficients of the mismatch model for polysilicon resistors. The measurements refer to structure 5 (RPD) for the distance coefficient, and to structures 6-8 (RP1, RP2 and RP3) for the area coefficient. The measured means for the different resistors of these structures are shown in Table 5.2. In this table is also given the mean of the quantity $\Delta R/R$ for the pairs of resis-

Table 5.2 Poly resistors used for the mismatch model estimation

Structure	W(μm)	L(μm)	mean R(Ω)	mean $\Delta R/R$	Functional Pairs
RPD	2	1748	17251	-	20
RP1	2	20	234.6	0.0109	149
	2	31.5	353.3	0.0110	148
RP2	2	55.5	596.8	0.0094	149
	2	125	1318.8	0.0090	148
RP3	2	500	5206.5	0.0108	145
	4	250	1349.4	0.0051	148

tors. We observe that there is an almost constant shift in the value of ΔR/R from zero for all the pairs with 2 μm-wide resistors, and it is approximately half for the pairs with 4 μm-wide resistors. This is consistent with what we observed in the measurements of the structures RAP1 and RAP2, where the resistor in the one end of the array tends to have higher value than the resistor in the other end and has been assigned to non vertical polysilicon etching in the plasma chamber. Since this is a systematic component of variation, it does not represent random local variation, as the model developed in Chapter 2 assumes. Therefore, the variance of the relative mismatch will be calculated below as the variance of the quantities ΔR/R, and not simply as the sum of their squares. In Table 5.2 is also given the number of the functional pairs of each kind on the wafer. Functional pairs are defined those whose measured mismatch is not an outlier of the set of measured mismatch of all the similar pairs on the wafer. From structure RPD we form 8 different pairs. Each pair consists of the leftmost resistor and one of the other resistors. The minimum number of functional pairs for each one of the 8 different combinations is given in the entry functional pairs for this structure in the table.

Figure 5.6 (a) depicts the mismatch variance of the 5 pairs of resistors with width 2 μm versus the inverse length. It is proportional to the inverse length of the device, and therefore it agrees well with the model developed in Chapter 2. The slope of the fitted line is given on the graph. In order to translate this to the area coefficient we need to multiply by

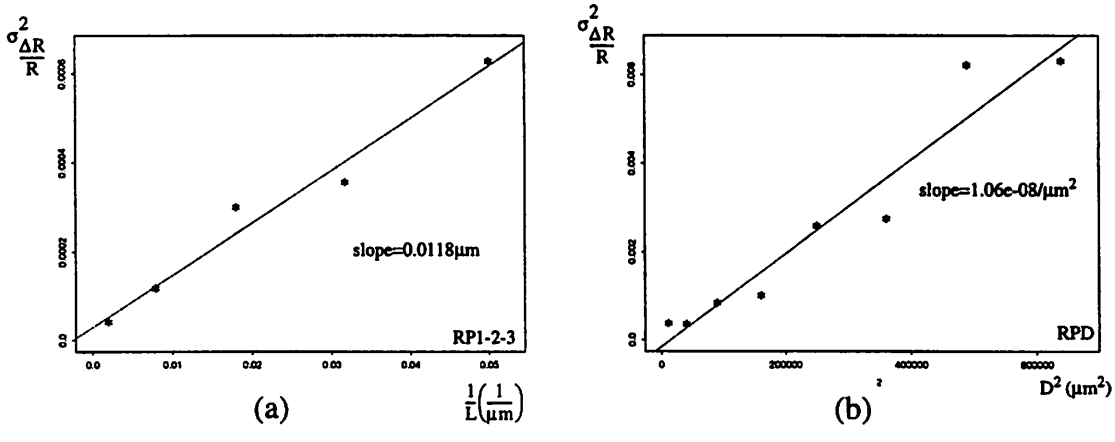


Figure 5.6 Mismatch model determination for polysilicon resistors.

the width. We can easily obtain the mean of the actual width by calculating the difference from the drawn width. Using the mean values from the two last lines of Table 5.2 for the pairs of structure RP3 in equation (4.3), provides the difference of the drawn and the actual width ΔW=-0.1528 μm; therefore, the actual width is Weff=2.1528 μm.

The pairs of 4 μm-wide poly lines with length 250 μm of structure RP3 exhibit a mismatch variance of 3.84e-5, close to that of the 2 μm-wide lines with length 500 μm, with which they have the same nominal area. This is depicted by the leftmost data point in Figure 5.6. Taking into account the difference between the drawn and the actual width, the area ratio is 0.964 with the area of the 4 μm-wide lines smaller, but this is still very close to 1. The agreement of the measured mismatch of the 4 μm-wide lines with the prediction of the model of equation (2.33) derived from the array of pairs of 2 μm-wide lines is some evidence that the more complete model of equation (2.32) is not needed when the width is 2 μm or wider.

Structures RPD had very low yield. Only 20 arrays out of the 156 on the wafer were fully functional, as can be seen in Table 5.2. However, the results from those 20 agree well with the hypothesis that the variance of the mismatch is linear with the square of the distance as shown in Figure 5.6. The y-axis represents the relative mismatch variance for the

Table 5.3 Resistor mismatch model coefficients.

Resistor Type	coef	Value	Units	R^2
poly	area: $S^2_{l,R}$	2.53e-2	$(\mu m)^2$	0.972
	dist: $S^2_{g,R}$	1.06e-8	$(\mu m)^{-2}$	0.934
n-diff	area: $S^2_{l,R}$	2.04e-3	$(\mu m)^2$	0.412
	dist: $S^2_{g,R}$	9.69e-11	$(\mu m)^{-2}$	0.562
p-diff	area: $S^2_{l,R}$	1.60e-3	$(\mu m)^2$	0.033
	dist: $S^2_{g,R}$	3.37e-10	$(\mu m)^{-2}$	0.955

8 pairs that we form between the leftmost and each one of the rest resistors in the array.

The x-axis shows the distance between the two devices of each pair. The distance coefficient of the model is the slope marked on the graph.

The coefficients of the mismatch model are shown in Table 5.3, together with those for diffusion resistors. The last column, the R^2 values, describes how well the data fits the straight line of the model. The closer these values are to 1, the better the fit.

5.5.3 N-Diffusion Resistor Mismatch Model

The measurements here were taken from structure 9 (RNDD) for the distance coefficient, and structures 10-12 (RND1, RND2, and RND3) for the area coefficient.The measured means for the different resistors of these structures are shown in Table 5.4. The

Table 5.4 N-Diffusion resistors used for the mismatch model estimation

Structure	W(μm)	L(μm)	mean R(Ω)	mean ΔR/R	functional pairs
RNDD	3	1748	19,925	-	149
RND1	3	20	383	-3.79e-03	147
	3	31.5	564	2.51e-03	144
RND2	3	55.5	948	-3.89e-04	149
	3	125	2059	1.42-03	146
RND3	3	500	8039	-6.06e-06	148
	6	250	1792	7.61e-04	133

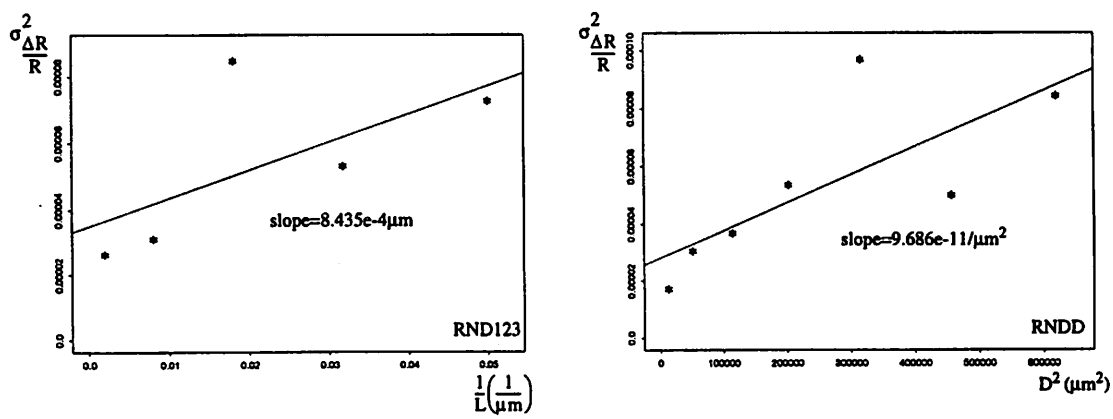
mean of the relative variation and the number of the functional pairs on the wafer is given also. The entry "functional pairs" contains the quantities defined for the polysilicon resistors in Table 5.2. Since the column with the mean ΔR/R values does not show any constant shift from zero, the mismatch variance will be calculated as the sum of squares of the quantities ΔR/R.

The mismatch variance of the 5 pairs of resistors with width 3 μm versus the inverse of the length is depicted in Figure 5.7 (a). We observe that the fitted line has a positive slope,

which means that mismatch increases when the length and the area decrease, but the measured points are not concentrated close to the fitted line. This large variance could be related to the large variation observed in the study of structures RAND and RAPD, for the diffusion resistors next to open area. It could also be a result of the use of different voltage in the measurement of resistors of different length, in order to have substantial, but not too high current. As in the polysilicon resistance case, in order to find the area coefficient we need to know the actual width of the diffusion resistors. Using the mean values of the two resistors of structure RND3, given in Table 5.4, equation (4.3) gives ΔW=0.586 μm; therefore, the actual width of the resistors with nominal width 3 μm, is 2.414 μm.

The pairs of the 6 μm-wide and 250 μm-long resistors of structure RND3 exhibit a mismatch variance of 6.14e-6, less than half of that of the 3 μm-wide and 500 μm-long lines, which have the same nominal area. Taking into account the actual width, the ratio of the two areas is 1.12 with the area of the 3 μm-wide resistor larger, but this does not explain the above result. The explanation could be either that this is a random result since the points of Figure 5.7 (a) are spread away from the fitted line, or that the terms proportional to $1/W^2$ of equation (2.32) become significant for W=2 μm in the case of diffusion resistors.

Figure 5.7 (b) shows the dependence of mismatch on the distance between the devices in a pair of diffusion resistors. Each data point represents one of the 7 pairs of diffusion



(a) (c)

Figure 5.7 Mismatch model determination of n-diffusion resistors.

resistors, formed by the leftmost resistor and each one of the rest resistors in the structure RNDD. The distance on the horizontal axis is the distance between the resistors of each pair. We observe that the mismatch increases with the square of the distance, but the variance around the fitted line is high. The distance coefficient is just the slope marked on the graph.

Both coefficients of the mismatch model are given in Table 5.3.

5.5.4 P-Diffusion Resistor Mismatch Model

As in the previous discussion, the data here are extracted from structure 13 (RPDD) for the distance coefficient, and structures 14-16 (RPD1, RPD2, and RPD3) for the area coefficient. As in the n-diffusion resistor case, Table 5.5 presents the mean value of the resistors contained in these structures, the means of the relative variation and the number of functional pairs.The mismatch variance is calculated again as the sum of squares of the quantities $\Delta R/R$.

Table 5.5 P-diffusion resistors used for the mismatch model estimation

Structure	W(μm)	L(μm)	mean R(Ω)	mean $\Delta R/R$	functional pairs
RPDD	2	1748	25,706	-	146
RPD1	2	20	489	0.0018	147
	2	31.5	727	0.0122	148
RPD2	2	55.5	1229	0.0031	145
	2	125	2665	0.0082	144
RPD3	2	500	10423	0.0043	143
	4	250	2339	-0.0005	122

Figure 5.8 (a) shows the dependence of mismatch on area and Figure 5.8 (b) the dependence on distance. These graphs are similar to those for the n-diffusion case. The measured mismatch values are spread away from the fitted line in the graph for the area coefficient while they follow well the line in the graph for the distance coefficient. Equa-

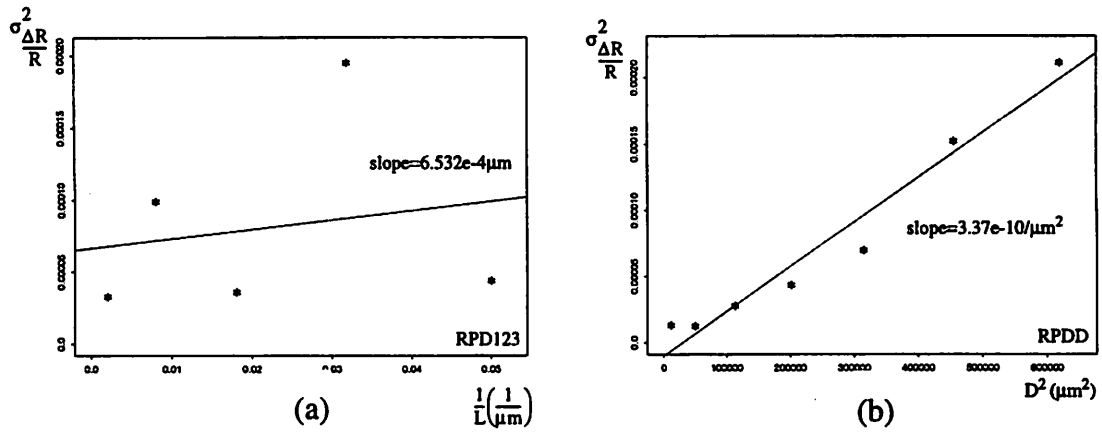


Figure 5.8 Mismatch model determination of p-diffusion resistors.

tion (4.3) gives ΔW=0.557 μm. The coefficients of the model are shown in Table 5.3. The pairs of the 6 μm - wide and 250 μm-long resistors of structure RPD3 exhibit mismatch variance 4.48e-6, again less than half that of the 3 μm-wide and 500 μm-long lines, which have the same nominal area. This is what we observed for the n-diffusion structures also and can be assigned to the same reasons.

5.5.5 Vertical Resistors

In this section we present mismatch measurements from the pairs of vertical resistors of structures 17 (VN) and 18 (VP). Structures VN contain poly and n-diffusion resistors, and structures VP contain poly and p-diffusion resistors. The dimensions of the poly resistors are W=2 μm and L=125 μm, and those of the diffusion resistors W=3 μm and L=125 μm. The results are compared with those obtained from pairs of parallel resistors of the same size contained in structures RP2, RND2, and RPD2. The results are presented in Table 5.6. In all cases the vertical resistors demonstrate higher mismatch, defined as the

Table 5.6 Vertical versus parallel resistors

Material	Structure	Orient.	mean ΔR/R	std.dev ΔR/R	$\sqrt{\Sigma(\Delta R/R)^2}$	functional pairs
Poly	VN & VP	vert.	0.0217	0.0109	0.0244	207
	RP2	paral	0.0106	0.0107	0.0140	148
N-Diff	VN	vert	0.0574	0.0339	0.0669	101

Table 5.6 Vertical versus parallel resistors

Material	Structure	Orient.	mean ΔR/R	std.dev ΔR/R	$\sqrt{\Sigma(\Delta R/R)^2}$	functional pairs
	RND2	paral	0.0014	0.00539	0.00557	146
P-Diff	VP	vert	0.0302	0.0120	0.0327	102
	RPD2	paral	0.0083	0.0055	0.0099	144

sum of squares of the quantities ΔR/R. This is mainly caused by higher mean ΔR/R of the vertical pairs with respect to the parallel and can be attributed to systematic differences in the width of the resistor lines, to directionality of the mobility of the material, and to misalignment. Misalignment affects two parallel placed devices identically and does not cause mismatch.

5.6 Transistor Results

5.6.1 PMOS Transistors Mismatch Model

Since the NMOS devices were not functional, only the PMOS devices were measured. We present here the results from the two groups of structures A and B, for the determination of the PMOS transistor mismatch model. Group A consists of structures 33-35 (PTAD, PTA1 and PTA2), and Group B consists of structures 36-38 (PTBD, PTB1 and PTB2). Table 5.7 shows the means of the measured quantities and the number of the func-

Table 5.7 PMOS transistors for the mismatch model estimation.

Structure	W(μm)	L(μm)	mean V_T (V)	mean β ($\mu A/V^2$)	mean γ ($\sqrt{V}$)	functional pairs
PTAD	65	10	0.683	5.597	0.581	133
PTA1	6	2	0.743	1.787	0.542	143
	8.5	2	0.734	2.811	0.537	142
	13.5	2	0.729	4.835	0.533	144

Table 5.7 PMOS transistors for the mismatch model estimation.

Structure	W(μm)	L(μm)	mean V_T (V)	mean β ($\mu A/V^2$)	mean γ ($\sqrt{V}$)	functional pairs
PTA2	24	2	0.723	9.159	0.531	146
	54	2	0.719	21.00	0.531	145
	216	2	0.715	85.71	0.532	146
PTBD	65	60	0.659	0.969	0.591	137
PTB1	6	6	0.725	0.677	0.585	143
	8.5	6	0.716	1.032	0.578	140
	13.5	6	0.709	1.741	0.573	141
PTB2	24	6	0.703	3.279	0.573	138
	54	6	0.698	7.629	0.570	142
	216	6	0.695	31.10	0.569	142

tional pairs from which we measured mismatch. Functional pairs are considered those whose measured mismatch is not an outlier of the set of measured mismatch of the similar pairs. Since the measurement of mismatch in threshold voltage, current factor and substrate factor gives different number of outliers and functional pairs, in the last column of Table 5.7 we give the minimum number of functional pairs found in the three measurements.

For the structures that determine the distance coefficients (PTAD and PTBD) we form 6 different pairs between the leftmost transistor and each one of the rest. The minimum number of functional pairs for each one of the 6 different combinations and the minimum for the three different measured parameters is given in the entry "functional pairs" for this structure in the table. The variance of mismatch is calculated as the sum of squares of the quantities ΔV_T for the threshold voltage, $\Delta\beta/\beta$ for the current factor and $\Delta\gamma$ for the body effect factor.

The measurement results from Group A are shown in Figure 5.9, and those from Group B in Figure 5.10. In both figures the graphs on the left represent the variance of

mismatch with respect to the inverse of the width of the devices in a pair, and the graphs on the right represent variance of mismatch with respect to the distance between the devices. The row on the top represents mismatch of the threshold voltage, the one in the middle relative mismatch of the current factor, and the one on the bottom mismatch of the body effect factor. In order to calculate the area coefficient from the slopes marked on the

Table 5.8 Mismatch model coefficients for PMOS transistors

parameter	coef.	Value Group A	Value Group B	Units	R^2 Group A	R^2 Group B
V_T	area: S^2_{l,V_T}	9.46e-4	1.16e-3	$V^2(\mu m)^2$	0.946	0.931
	dist: S^2_{g,V_T}	1.30e-11	9.63e-12	$V^2(\mu m)^{-2}$	0.974	0.985
β (relative)	area: $S^2_{l,\beta}$	9.33e-3	5.12e-3	$(\mu m)^2$	0.971	0.957
	dist: $S^2_{g,\beta}$	5.79e-12	6.20e-12	$(\mu m)^{-2}$	0.432	0.454
γ	area: $S^2_{l,\gamma}$	2.32e-4	1.68e-4	$V(\mu m)^2$	0.932	0.944
	dist: $S^2_{g,\gamma}$	3.13e-13	3.07e-13	$V(\mu m)^{-2}$	0.128	0.814

graphs, we need an estimate for the difference between the actual channel length and the drawn transistor length. Since at the time that this information was needed the automatic wafer prober was not functional and we were unable to measure effective length, and since our experiment does not intend to provide a very accurate value of the model coefficients, we will make the approximation that the channel length is equal to the drawn length. This is a reasonable approximation, since we found before that the polysilicon lines are wider than the nominal width, but also there is some overlap of the gate with the source and the drain. The area coefficient is the slope marked on the graph, multiplied by the drawn length. The distance coefficient is just the slope marked on the corresponding graph.The calculated coefficients, together with information about how close the data points fall to the straight line of the model - the R^2 values - are shown in Table 5.8.

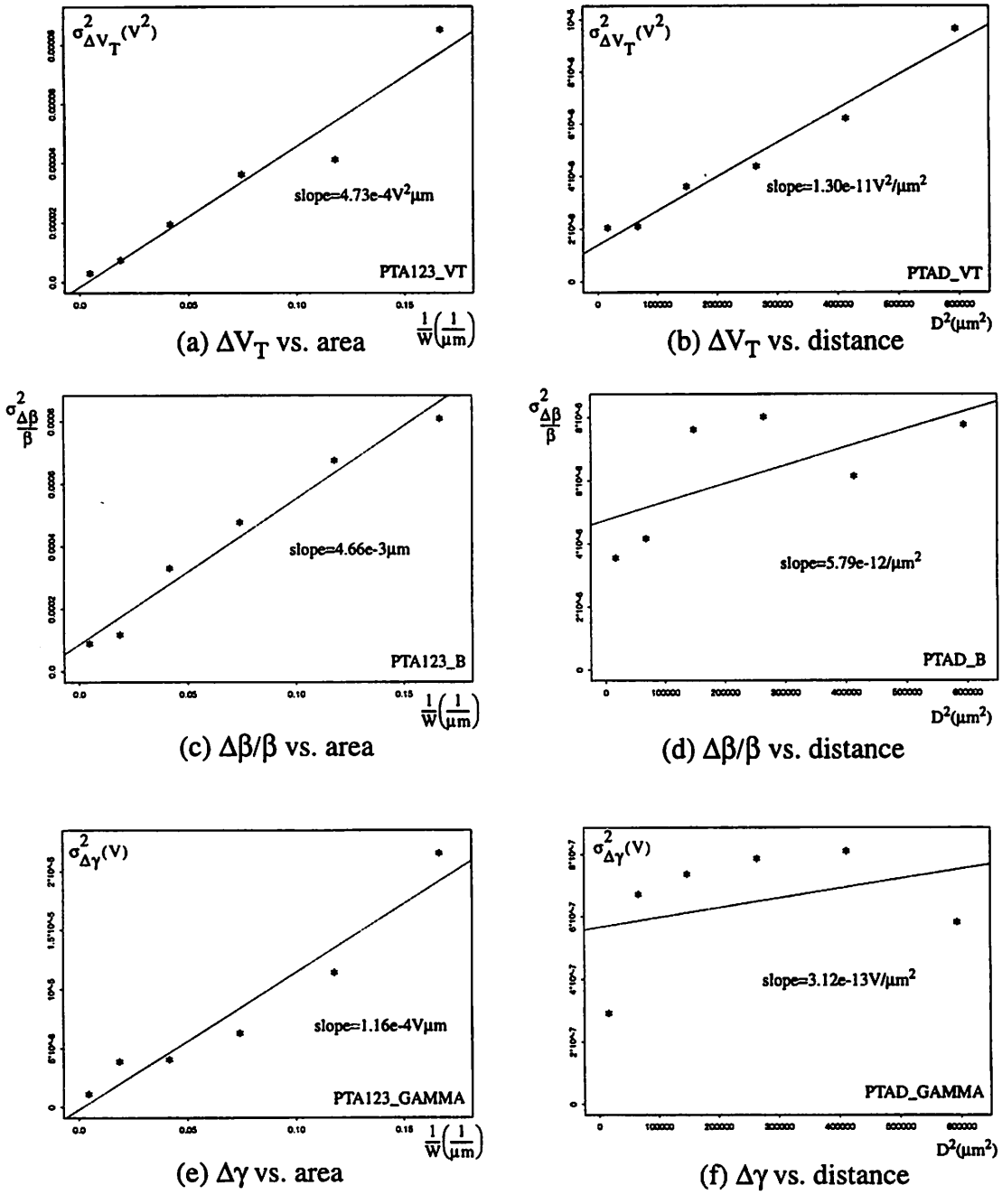


Figure 5.9 Mismatch model determination for threshold voltage, current factor and substrate factor of PMOS transistors. Results from Group A.

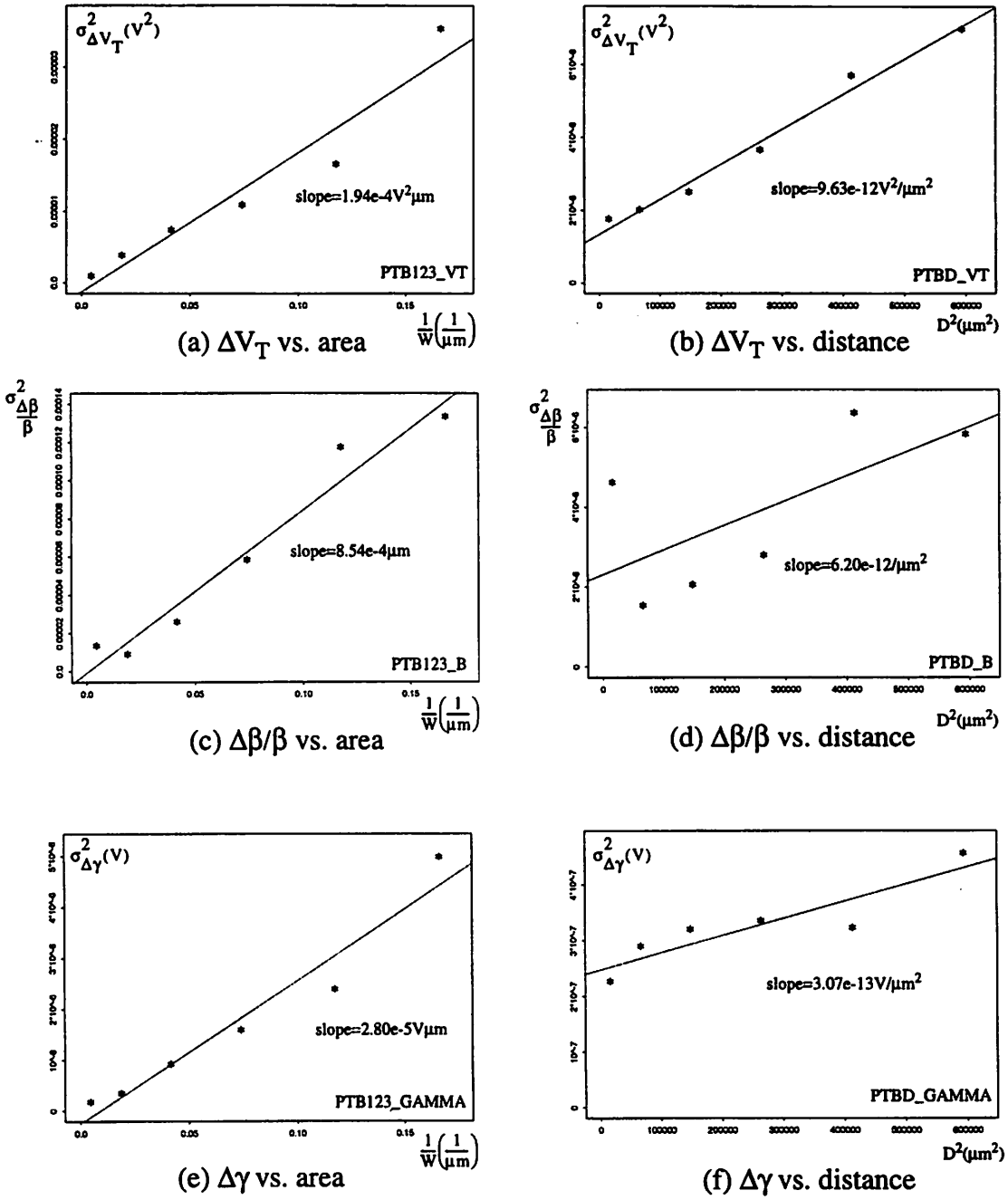


Figure 5.10 Mismatch model determination of the threshold voltage, current factor and substrate factor. Results from Group B.

5.6.2 Orthogonal Experiment with PMOS Transistors

We present in Table 5.9 the results from the orthogonal experiment that examines the combined effect of size, distance, and orientation in transistor mismatch. Since the NMOS devices are not functional, only the results from the PMOS devices are presented. The

Table 5.9 Orthogonal Experiment with PMOS transistors.

Structure	Size (μm/μm)	Dist (μm)	Orientation	std. dev. ΔV_T (V)	std. dev. $\Delta\beta/\beta$	std. dev. $\Delta\gamma(\sqrt{V})$	functional pairs
NO1	6/2	20	paral	0.0107	0.0285	0.00464	141
	6/2	20	vert	0.0099	0.0574	0.00510	144
	6/2	200	paral	0.0105	0.0424	0.00518	145
NO2	6/2	200	vert	0.0104	0.0611	0.00519	143
	60/6	20	paral	0.0017	0.0030	0.00075	147
	60/6	20	vert	0.0018	0.0118	0.00081	145
NO3	60/6	200	paral	-	-	-	0
	60/6	200	vert	-	-	-	0

eight row does not contain results because of the error in the layout of this structures referred in the description of the structures 41 and 44, in Chapter 4. The seventh row does not contain data because of a bug in the measurement code. As in the previous section, the variance of mismatch was calculated as the sum of squares of the quantities ΔV_T for the threshold voltage, $\Delta\beta/\beta$ for the current factor and $\Delta\gamma$ for the body effect factor.

The effect of area and distance has been studied extensively in the previous section. Orientation appears to be an important factor for the current factor but less so for the body effect factor mismatch, while the threshold voltage mismatch appears to be unaffected. The misalignment between the vertical devices is probably the main reason their mismatch is greater than that of the parallel devices.

Chapter 6

Conclusions and Future Work

6.1 Introduction

We presented a study of device mismatch caused by the variability of process parameters. Three different kinds of variation were considered: a) Systematic variation because of the differing environment.b) Local random fluctuations with very small autocorrelation distance. c) Large gradients of variation across the wafer and die. A model that relates the second and the third kinds of mismatch with the area of the devices and the distance between them has been derived before [11]. The variance of mismatch is inversely proportional to the area of the devices and directly proportional to the square of the distance. This model is not device-specific and can be used for the various parameters of the MOS transistors, resistors and capacitors.

6.2 Experiment Overview

We designed a set of test structures in order to study the different causes of mismatch. The first group of structures consists of arrays of resistors, two dimensional arrays of transistors, and two dimensional arrays of capacitors, to study the effect of the environment in variation. The second group contains structures specialized to extract the dependence of mismatch on area and distance, providing the coefficients of the mismatch model. These structures include polysilicon, n and p diffusion resistors, capacitors and NMOS and PMOS transistors. The third group consists of some basic circuits, such as differential pairs and an operational amplifier. In such circuits device mismatch creates input offset. Circuit analysis gives the statistics of the input offset in terms of the statistics of device mismatch. Agreement of the measured input offset statistics with the predicted based on

the mismatch model described above would verify the both the mismatch model extraction and the circuit analysis method.

The test structures were fabricated in the Berkeley Microfabrication Laboratory. The large volume of the measurements of required, fabrication problems and problems with the measuring equipment did not allow the measurement of all the designed structures. However, the neighboring effect in resistor arrays has been observed, the mismatch model coefficients have been extracted for many kinds of devices, and the fit to the model has been discussed. The effect of orientation in mismatch has also been presented. Repetition of the fabrication and new measurements are intended in the future. If the layout is redesigned, the structures for the area coefficients can be designed with the varying dimension such that the areas of the pairs are evenly spaced on a 1/area axis, as discussed in Section 4.2.

6.3 Future Plans

The large number of different structures that we designed did not allow a dense grid of each structure on the die. As a result we were not able to observe the effect of the position in the die and the wafer on mismatch. By concentrating our research on only a few kinds of devices, we will be able to distribute many identical structures in the die. This will allow us for example, to calculate a set of mismatch model coefficients from each die, and then plot wafer maps of the values of the coefficients. Similarly we could calculate a set of mismatch model coefficients from all the structures across the wafer located on the same point in the die and then plot die maps of the coefficients. Analysis of variance can be used to examine the importance of the effect of the position in the die or in the wafer.

Finally, we believe that interesting results can be obtained if the experiment is repeated in a fabrication line capable of creating submicron devices. Theoretical analysis in Chapter 2 showed that for small dimensions, terms proportional to $1/W^2$ and $1/L^2$ are introduced in the model. Also, by relaxing the assumption that the autocorrelation distance of the process variation is much smaller than the dimensions of the devices, theory predicts

that the mismatch becomes better than inversely proportional to the area. A methodology to predict mismatch of the threshold voltage for submicron devices has been discussed in Chapter 2. Therefore actual measurements from devices with one of the dimensions very narrow would illuminate the mismatch behavior. For example, the structures that give the area coefficient for resistors could be redesigned this time, for constant length and variable width, from as narrow as the technology allows, to relatively wide. Since the environment effect has been found to be important for the value of some process parameters, the pairs in the structures from which we will extract the area coefficient can be protected between dummy devices. This could significantly affect the measurements of the diffusion resistors, which have been found to demonstrate large variance when next to open area.

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