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Techniques for Fast Circuit Simulation Applied to Power Estimation of CMOS Circuits†

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Abstract

We present a transistor level power estimator which exploits algorithms for fast circuit simulation to compute the power dissipation of CMOS circuits. The proposed approach uses stepwise equivalent conductance and piecewise linear waveform approximation. The power estimator has been implemented in the SWEC framework. Experimental results indicate that SWEC can obtain a substantial speed-up over HSPICE while maintaining an accuracy of within 10%. Benchmark results on a suite of industry circuits, which include circuits that HSPICE could not handle, are presented.

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1 Introduction

Power minimization is becoming very important for a number of reasons ranging from an increasing demand for portable computing and telecommunication equipment, increasing clock frequencies, to advances in process technology that enables the integration of extremely large number of densely packed devices on a single chip. Minimizing power dissipation of chips has an impact not only on energy savings, but also helps create more reliable chips. Although designers have several techniques at their disposal to minimize power, there is little or no help in terms of tools to assist in analyzing and evaluating the effectiveness of various decisions during the design process.

A challenging problem in this context is how to efficiently obtain power estimates which meet the accuracy and the run-time constraints of the designer. Several approaches have been proposed to compute or estimate power dissipation, each with a different accuracy/run-time trade-off. These approaches can be classified into three broad categories: statistical/empirical techniques [7], probabilistic techniques [6, 9, 10], and circuit simulation based techniques [2, 3, 5].

The main advantages of the probabilistic techniques is their short runtimes and input-independence. The probabilistic techniques use a stochastic model of logic signals of a circuit and propagate the probabilities of logic values through the combinational logic modules in order to compute the average switching rate of the circuit. This measure is in turn, is used to obtain the average power consumption of the circuit. It can potentially be accurate; however, for high accuracy, the spatial and temporal correlation between internal node values must be modeled. As this proves to be expensive, most approaches trade off accuracy for speed, resulting in highly unacceptable estimates at times.

Another approach is to make use of various statistical measures of the circuit. This approach is the most crude of all, despite its advantage in speed. It reads a description of the design, compiles various statistical measures, and calculates the power consumption based on these measures. The main use of this method is to obtain rough estimates of power dissipation at early stages of the design.

Circuit simulators such as HSPICE [4] still provide the most direct and accurate approach for computing power dissipation. While offering good accuracy, HSPICE suffers from a drawback of limited capacity and large run times. This makes HSPICE impractical for all but the smallest of circuits consisting of around a few hundred gates. The popular solution thus is to separately use point tools like Powermill [3] for power estimation and HSPICE for the simulation and verification of the circuit in parts.

In this work we propose the use of a circuit simulation tool SWEC, that alleviates some of the problems faced by tools such as HSPICE, thus making it realistically feasible to perform power estimation along with simulation of the entire design. SWEC uses Stepwise Equivalence Conductance [8] and piecewise linear waveform approximations for fast and accurate circuit simulation. These techniques prove to be very well suited for efficient power estimation as well. In the following sections, we describe the power estimation problem, provide a brief description of SWEC, the power estimator implemented within the SWEC framework and present experimental results on industrial circuits, which show that this tool can be effectively used for power estimation of large CMOS circuits.

2 Problem Description

By power estimation we refer to the problem of estimating the average power dissipation of a circuit. In CMOS circuits, there are two components that contribute to power dissipation [1]: static dissipation (due to leakage current) and dynamic dissipation (due to switching transient current and charging and discharging of load capacitance).

In most CMOS ASICs the contribution due to static dissipation is small compared to dynamic dissipation. The static power dissipation P_s of a circuit is given by the equation:

$$P_s = \sum_{i}^{n} I_l \times V_{dd} \tag{1}$$

where I_l is the leakage current of the device (gate), V_{dd} is the supply voltage and n is the number of devices in the circuits.

The dynamic power dissipation P_{di} for a logic gate is given by the equation:

$$P_{di} = \frac{1}{2} \cdot C_{Li} \cdot V_{dd}^2 \cdot \frac{N_{ti}}{T} \tag{2}$$

where C_{Li} is the output load capacitance on the gate i, V_{dd} is the supply voltage, T is the clock cycle and N_{ti} is the number of switching transitions per clock cycle for gate i. The dynamic power dissipation P_d of a circuit with n gates is given by the summation:

$$P_d = \frac{V_{dd}^2}{2T} \cdot \sum_{i=1}^{n} C_{Li} \cdot N_{ti} \tag{3}$$

The total power dissipated by the circuit is the sum of the two components; static and dynamic dissipation.

$$P_{total} = P_s + P_d \tag{4}$$

The most accurate and straightforward approach to power estimation is by simulation: perform a circuit simulation of the design and monitor the current waveform. While this estimate accounts

for all types of power dissipation, the main drawback of this approach is the very high runtime. At the transistor level, the problem thus reduces to performing efficient transient simulation of the circuits in a *power-estimation friendly* way, i.e. using simulation techniques that are also suited to computing power estimation with minimum overhead.

3 The Circuit Simulation Platform

Stepwise Equivalence Conductance approach was first proposed in [8] to exploit certain characteristics of MOS circuits to speed-up simulation. This approach is based on the use of a stepwise equivalent conductance model of a nonlinear resistive device. The major advantage of this technique is that it eliminates the need of Newton-Raphson iterations for implicit integration. This technique is consistent, absolutely stable and convergent. When applying the integration to digital MOS circuits, an additional speed-up in the simulation is achieved by taking advantage of the fact that the voltage waveforms can be modeled to a good approximation as piecewise linear functions.

Assuming for the sake of simplicity, that there are no inductors and only constant capacitors in the simulated circuit, the KCL nodal equations for the simulated circuit will be of the form

$$\mathcal{F}(V(t)) + C\dot{V}(t) = I_s(t) \tag{5}$$

where $V(t)$ is the node voltage vector, $\mathcal{F}(.)$ is a vector function of $V(t)$ with its i-th entry representing the total current flowing out of node i through resistive devices, C is the constant capacitance matrix, and $I_s(t)$ is a vector of inputs. This nonlinear system of equations can be transformed to a linear time variant system below without any loss of accuracy.

$$G(t)V(t) + C\dot{V}(t) = I_s(t) \tag{6}$$

$G(t)$ represents the instantaneous equivalent conductance matrix for every branch in the circuit at time t, with $G(t)V(t) = \mathcal{F}(V(t))$ at every time instant t. $G(t)$ can be expanded in a Taylor series around $t=t_n$. Retaining only the first two terms, we obtain

$$[G(t_n) + \dot{G}(t_n)(t - t_n)]V(t) + C\dot{V}(t) = I_s(t) \tag{7}$$

This can then be further approximated as,

$$\mathcal{G}V(t) + C\dot{V}(t) = I_s(t) \tag{8}$$

where, for $h_n = t_{n+1} - t_n$,

$$\mathcal{G} = G(t_n) + \dot{G}(t_n)\frac{h_n}{2} \tag{9}$$

We thus obtain a system of linear differential equations, which can be solved directly without any iterations using a standard integration scheme.

SWEC uses an event-driven approach with circuit partitioning to exploit the latency and multi-rate behavior of the circuit.

4 Power Estimation using SWEC

The Stepwise Equivalence Conductance and the piecewise linear waveform approximation are ideally suited for efficient power computation. The power can be measured directly by monitoring the conductance and the voltage waveform during each time-step. Using (5), The power dissipated in each device during a time step h_n (from t_n to t_{n+1}) is given by

$$P_d = \frac{1}{h_n} \int_{t_n}^{t_{n+1}} V(t)\mathcal{F}(V(t))\,dt \tag{10}$$

Recall that, during each time-step, each nonlinear device conductance is approximated by an equivalent conductance $\mathcal{G}$ (Eq. 6-10). Thus, (11) can be simplified as:

$$P_d = \frac{1}{h_n} \int_{t_n}^{t_{n+1}} \mathcal{G} \cdot V^2(t)dt \tag{11}$$

Since the voltage waveforms are piecewise linear, dV/dt is a constant for a given time step. Thus, the power dissipated in each device from t_n to t_{n+1} can be obtained by simply computing the area under the power waveform curve given by:

$$P_d = \frac{\mathcal{G}}{h_n} \int_0^{h_n} \left[V(t_n) + t \cdot \left.\frac{dV}{dt}\right|_{h_n} \right]^2 dt \tag{12}$$

The power in capacitors can be computed similarly. Specifically, one can directly measure the power consumption during simulation using the piece-wise linearity property of the waveforms in SWEC. For each event during the course of a simulation, we perform the following calculations. Suppose an event changes the voltage across a capacitor C_i from v_0 at time t_0 to v_1 at time t_1. Then, the power dissipated from t_0 to t_1 is given by:

$$P_c = \frac{1}{h_n} \cdot C_i \cdot V_{avg} \cdot \frac{dV}{dt} \tag{13}$$

where V_{avg} is the average value of v_0 and v_1. dV/dt is a constant as before. Inductors in the cir-

cuit are handled similarly, with the inductor current (computed for transient simulation using the modified nodal analysis) as the controlling variable.

Then we update the average power up to the time t_1 as follows.

$$P_{t_1} = \frac{P_{t_0} \cdot t_0 + P_{t_1 - t_0} \cdot (t_1 - t_0)}{t_1} \tag{14}$$

where $P_{t_1 - t_0}$ denotes the power consumed from t_0 to t_1 and P_{t_i} denotes the power consumed from $t = 0$ to t_i. We perform this calculation for every event of the simulation, and finally sum up the power dissipated at every node to obtain the power consumption of the circuit.

5 Implementation and Results

The power estimator described in the previous section has been implemented in the SWEC framework. We use HSPICE along with this program to compare benchmark results.

For the purpose of this benchmarking, we used industrial circuits obtained from LSI Logic Corporation. The netlists were extracted from the layout of real designs generated in the design synthesis environment of LSI Logic using their ASIC cell libraries and submicron devices. These circuits range in size from 200 to 6000 cell units in the LSI technology. These netlists were then used along with input stimuli to serve as data for both HSPICE and SWEC. The circuits used in the experiments are listed in Table 1.

Table 2 shows the power measurement results for these circuits. The results were obtained on a DEC 5100/125 platform with a 96 Mbyte memory. The second and third columns in the table correspond to the power dissipation results reported by SWEC and HSPICE respectively. The last column shows the percentage error in the SWEC measurement as compared to HSPICE. It can be seen that for the first 4 circuits the absolute percentage errors range from 1.9% to 10.2%. Note that HSPICE was not able to handle the last two circuits (multp16 - 6344 cell units and mult16 - 5320 cell units) due to memory limitations and/or CPU time constraints. SWEC successfully completed simulation in all examples we ran.

Circuits	Size (cell units)	MOS devices	Capacitors	Description
mux2b16	208	214	134	16 bit 2-to-1 mux
comp16	205	262	137	16 bit comparator
cla16	993	1200	500	16 bit carry look ahead adder
mult8	1276	2691	1008	8 bit wallace tree multiplier
multp16	6344	11314	3922	16 bit pipelined multiplier
mult16	5320	9778	3148	16 bit wallace tree multiplier

Table 1: Circuits used in the experiment

Circuits	SWEC	HSPICE	% Error
mux2b16	0.698	0.685	1.90
comp16	0.862	0.958	-10.20
cla16	1.430	1.54	-7.14
mult8	12.254	11.483	6.71
multp16	40.125	*	-
mult16	54.547	*	-

Table 2: Results of Power Measurements (in mW) (* indicates HSPICE could not complete)

Circuits	SWEC	HSPICE	Speed up
mux2b16	9.12	166.19	18.22
comp16	43.25	1132.65	26.19
cla16	51.75	2017.07	38.98
mult8	229.82	13089.65	56.96
multp16	907.78	*	-
mult16	1076.18	*	-

Table 3: Comparisons of Run Times (in seconds) (* indicates HSPICE could not complete)

.Table 3 shows the speed up achieved by SWEC as compared to HSPICE. For the circuits that HSPICE was able to handle, the speed-up ranged from 18.22 for a 200 cell unit design to 56.96 for a 1276 cell unit design. Note that the speed-up increases as the circuit size grows

6 Conclusions

We have presented an approach to power estimation using SWEC. The proposed method exploits the stepwise equivalent conductance approximation to efficiently compute power dissipation while speeding up the transient simulation process. Based on the results presented, we belie-vethat SWEC can effectively replace HSPICE when a relatively accurate power estimate is desired without the large run times.

In conclusion, SWEC can be effectively used as a tool for power characterization for library elements in system design. It can also be used as a baseline tool for power estimation for reasonably large circuits that HSPICE cannot handle.

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