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A PHYSICAL MODEL FOR MOSFET OUTPUT RESISTANCE

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ABSTRACT

The output resistance (R_{out}) is one of the most important device parameters for analog applications. However, it has been difficult to model R_{out} correctly. In this paper, we present a physical and accurate output resistance model that can be applied to both long-channel and submicrometer MOSFETs. Major short channel effects and hot-carrier effect, such as channel-length modulation (*CLM*) [1], drain-induced-barrier-lowering (*DIBL*) [2] [6] [7] and substrate current induced output resistance reduction [3] [4], are all included in this model, and it is scalable with respect to different channel length L, gate oxide thickness T_{ox} and power supply V_{dd}. This model can be incorporated into any existing MOSFET's model without introducing any discontinuity.

INTRODUCTION

In analog circuit applications, the voltage gain is directly proportional to R_{out}. Existing analytical models for MOSFET R_{out} are not adequate [8], because only channel-length modulation effect is included. The empirical model[4] is more accurate, however it lacks scalibility. To achive high accuracy and scalability, R_{out} model must be analytical and include all the major physical mechanisms that affect R_{out}. The typical MOSFET I-V characteristic and output resistance are shown in Fig. 1. The R_{out} curve can be clearly divided into four regions with each region dominated by a mechanism. The first region is the triode region which is controlled by the carrier mobility. As will be shown, the second region is the near-saturation region dominated by *CLM*. The third region is dominated by *DIBL* and the fourth is the high field region in which R_{out} is greatly reduced by the substrate current induced body effect (*SCBE*). Because most of existing MOSFET models can handle the triode region fairly well, we will concentrate only on the saturation region in this paper.

PHYSICAL OUTPUT RESISTANCE MODEL

To smoothly and easily incorporate the various mechanisms into any drain current equation, the concept of Early voltage V_A which is widely used in BJT models, is adopted. In saturation region, V_A is introduced as follows

$$I_{ds}(V_{gs},V_{ds}) = I_{ds}(V_{gs},V_{dsat}) + \frac{\partial I_{ds}(V_{gs},V_{ds})}{\partial V_{ds}}(V_{ds}-V_{dsat}) \equiv I_{ds}(V_{gs},V_{dsat})(1+(V_{ds}-V_{dsat})/V_A) \quad (1)$$

where V_{dsat} is the saturation voltage and is given by $V_{dsat} = E_{sat}LV_{gst}/(E_{sat}L+V_{gst})$ [1], and $E_{sat} = 2v_{sat}/\mu_{eff}$, v_{sat} and μ_{eff} are saturation velocity and mobility, respectively. V_A has three components, corresponding to *CLM* V_{ACLM}, *DIBL* V_{ADIBL} and *SCBE* V_{ASCBE}. Each component can be evaluateed separately.

$$\frac{1}{V_A} = \frac{1}{I_{dsat}}[(\frac{\partial I_{ds}}{\partial V_{ds}})|_{CLM} + (\frac{\partial I_{ds}}{\partial V_{ds}})|_{DIBL} + (\frac{\partial I_{ds}}{\partial V_{ds}})|_{SCBE}] = \frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBL}} + \frac{1}{V_{ASCBE}} \quad (2)$$

(i) Channel Length Modulation (*CLM*)

As $V_{ds} > V_{dsat}$, the velocity saturation region near the drain extends toward the source, which effectively reduces the effective channel length and in turn increases the drain curren. The channel length reduction ΔL satisfies $V_{ds} = V_{dsat} + l\sinh(\Delta L/l)$ [1], we can get

$$V_{ACLM} = (E_{sat}L + V_{gst})(V_{ds} - V_{dsat})/E_{sat}l \quad (3)$$

where $l = \sqrt{3T_{ox}X_j}$. X_j is the channel depth.

(ii) Drain Induced Barrier Lowering (*DIBL*)

As V_{ds} is applied to the drain, the barrier height between the source and drain will be lowered[2] [7], therefore the threshold voltage V_{th} is reduced and in turn the drain current increases. It has been shown[7] that threshold voltage reduction due to DIBL is given by $-\theta(L)V_{ds}$. $\theta(L)$ is the *DIBL* coefficient which has strong dependence on the channel length and is given by

$$\theta(L) = \exp(-L/2l_t) + 2\exp(-L/l_t) \quad (4)$$

where $l_t = \sqrt{3T_{ox}X_{dep}/\eta}$ and X_{dep} is the depletion width at the source, and X_{dep}/η is the average depletion width along the channel. From the above argument, we obtain

$$V_{ADIBL} = (E_{sat}L + V_{gst})/\theta(L)(1 + 2E_{sat}L/V_{gst}) \quad (5)$$

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(iii) Substrate Current Induced Body Effect (*SCBE*)

At even higher V_{ds}, the electrical field near the drain becomes very high (>0.1MV/cm). some electrons travelling through this region will acquire enough energy to cause impact ionization and result in substrate current. The substrate current will flow through the substrate, produce an ohmic drop across the substrate resistance R_{sub}, and increase the substrate potential. This substrate potential will reduce V_{th} and hence increases the drain current. On the other hand the electrons (in NMOS) created during impact ionization will go into the drain directly. Therefore we have

$$V_{ASCBE} = 1 / [\frac{A_i}{B_i}(1 + g_m \frac{\gamma}{2\sqrt{\phi_s - V_{bs}}} R_{sub}(1 + \frac{B_i l}{V_{ds} - V_{dsat}}))\exp(-\frac{B_i l}{V_{ds} - V_{dsat}})] \quad (6)$$

where A_i and B_i are the parameters associated with the substrate current determined by experimental data [3]. g_m is the transconductance, γ is the coefficient of body effect, ϕ_s is the surface potential. V_{ASCBE} has very strong dependence on V_{ds}, this is because substrate current depends on V_{ds} exponentially [3]. In order to make the drain current and the first order derivative continuous at $V_{ds} = V_{dsat}$. Eq. (2) is modified as

$$V_A = V_{Asat} + 1/(1/V_{ACLM} + 1/V_{ADIBL} + 1/V_{ASCBE}) \quad (7)$$

where V_{Asat} is the Early voltage at $V_{ds} = V_{dsat}$, which can be obtained from the triode region. If the triode region current model in [1] is used, then $V_{Asat} = E_{sat}L + V_{dsat}$. The formulation ensures that R_{out} is continuous throughout all regions, which is an important property for robust circuit simulations. Because the Early voltage approach for modeling R_{out} does not depend on the specific form of the drain current. This methodology is suitable to any MOSFETs model.

DISCUSSION

The individual component of V_A together with the resultant V_A are shown in Fig. 2. The dominant mechanism the one which has smaller Early voltage, in each region can be easily identified. Fig. 3 shows R_{out} the modeling results at different gate voltage. The good agreement between experimental data and modeling results makes the model highly suitable for analog applications. Quantitatively predicting the scaling effects can also be obtained. Figs. 4 and 5 show R_{out} versus V_{ds} for various channel lengths and gate oxide thicknesses, respectively. The most important characteristics of R_{out} in circuit designs are the maximum R_{out} which determines the maximum available gain from the device, and the onsets of drain voltage at which R_{out} starts decreasing on both sides of the peak, which determines the dynamic swing of the drain voltage. Among the three mechanisms stated above, *DIBL* has the greatest impact on the maximum R_{out}, while *SCBE* and V_{dsat} limit the dynamic swing. Fig. 4 shows that maximum R_{out} is reduced as channel length decreases, this is because *CLM* and *DIBL* effects become more severe as channel length is reduced. The channel length sensitivity of maximum R_{out} is mainly due to the exponential dependence on channel length of $\theta(L)$ [7]. $\theta(L)$ and maximum R_{out} versus chnnel length and gate oxide thickness are shown in Fig. 6 and 7, respectively. As gate oxide thickness decreases, short channel effects are suppressed and maximum R_{out} increases, as shown in Fig. 5. However, the substrate current induced body effect (*SCBE*) is also enhanced as indicated by the faster decreasing R_{out} in the high field and thin T_{ox}. It is interesting to note, that in general for a given technology, the hot-carrier effects (e.g. *SCBE*) will be enchanced when the short channel effects (e.g. *CLM & DIBL*) are suppressed. This is because when the short channel effects are suppressed, the high field region has to be suppressed. Therefore the maximum electrical field is increased and hot-carrier effects will be enhanced. If we assume that the minimum R_{out} required in a design is *120 kohms*, a contour of the drain voltage and channel length at which R_{out}=*120 kohms* can be plotted as shown in Fig. 8. The regions enclosed by the contour represent the acceptable design windows. The dynamic swing for any given channel length can be clearly determined from Fig. 8. As expected, devices with thicker gate oxide will provide larger voltage swing but the minimum channel length which can be used is also longer due to worse short-channel effects. With this model, families of plots similar to Fig. 8 at different V_{gst} can be generated and used by analog circuit designer in choosing the optimal device dimensions and bias conditions. Figs. 9 and 10 show that R_{out} model also has capability of modeling PMOS and LDD MOSFET.

CONCLUSIONS

A physical-based analytical model for MOSFET output resistance is presented. Major physical mechanisms important to the output resistance are considered and analysized. Scaling effects of channel length, gate oxide thickness and power supply on the output resistance are also investigated. This model can be incorporated into any exist MOSFET's model without introducing and discontinuity.

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