EECS 143
PROCESSING AND DESIGN OF INTEGRATED CIRCUITS LABORATORY PROJECT

by

Ping K. Ko, Robin R. Rudell, and Katalin Voros

Memorandum No. UCB/ERL M88/50

August 1988
(Revised January 20, 1992)

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
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ABSTRACT

This report describes the laboratory part of the undergraduate course EECS143. An upgraded process has been introduced along with new test structures in the Fall semester of 1987. Process and testing are discussed and characterization examples are included.

July 28, 1988

EECS 143
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Introduction and History

The EECS 143 undergraduate course Processing and Design of Integrated Circuits has been designed to familiarize students with fabrication technology, types of device structures, electrical characterization, modeling of devices, and with the relationships between physical layout and electrical characteristics. The course was first offered in 1972 by Professor D. A. Hodges as a graduate course. It was changed into an undergraduate class the following year and joined with an independent laboratory course (EE134) started several years earlier (1968) by Professors W. G. Oldham and W. Howard. When the two courses were joined, the laboratory section was revised from the fabrication of bipolar devices to PMOS transistors and other test structures (EE147).

In 1980, when the Microfabrication Research Facility was designed, the undergraduate laboratory served as a test site for the modular construction planned for the research lab. As a result, two smaller clean room areas, separated by a service chase, were built into the existing large room and advanced processing equipment was installed. At the same time, a new process was developed and introduced in 1981.[1]

The quarter system allowed only 10 three-hour laboratory sessions to complete the processing and to characterize the devices; thus, a simple, 4-mask aluminum gate NMOS process was designed with spin-on doping for source and drain diffusions and metal definition by lift-off. EECS 143 has been offered every semester since its inception and became a popular course not only for undergraduates, but also for those graduate students who are involved in process technology/integrated circuits design and processing.

When the campus changed from the quarter to the semester system, the number of laboratory sessions increased to 15 and it was possible to carry out a more detailed characterization of the test chip. Advanced test equipment was obtained over the years and by this time, following Berkeley's tradition of constant updating of courses, it was also appropriate to change the process to reflect current industry standards more closely. Thus, both the process and test chip were redesigned, and the new chip was introduced during the Fall semester of 1987.

Course Description

EECS 143 - Processing and Design of Integrated Circuits is a 4-credit undergraduate course, given every semester, with three hours of lecture and three hours of laboratory per week. The course focuses on

- Integrated circuit fabrication
- Monolithic active and passive components
- Device structure and characterization
- Relations between physical layout and electrical characteristics

MOS transistors and circuit elements are fabricated in the laboratory and electrically evaluated. The prerequisite course is EECS 130 - Integrated Circuit Devices, which cannot be bypassed as EECS143 builds heavily on the material presented there.

A typical course outline is shown in Table I with the Laboratory Weekly Schedule in Table II.

Facilities

An independent laboratory with an area of approximately 840 square feet is maintained for EECS143 in 218 Cory Hall. Maintenance of the processing equipment is provided by Microlab staff, and of the characterization instrumentation by the EECS Electronics Support Group.

The equipment is arranged to provide optimum conditions in which a group of 8 students can operate, each pair processing one wafer. There are essentially three working areas, two of which are maintained under clean room conditions for processing: 1) the photoresist clean room, where resist spinning, baking and alignment are done; 2) the diffusion and etching clean room with 3 furnaces, and aluminum evaporator and two wet process stations for the rest of the operations; 3) the characterization area with two probe stations for electrical testing with the aid of two HP 4145 Semiconductor Parameter Analyzers and plotters; a C-V probe station and a miscellaneous measurement station. There are also two computer terminals; class accounts are given out at the beginning of the semester. Students are required to perform process simulations using SUPREM. The laboratory's equipment is listed in Table III.

Test Chip Layout

The test chip was laid out using the KIC graphics editor.[2] Each device was laid out as a separate cell, so that they could be placed as instances once the chip was ready to be "assembled". This facilitated a compact arrangement of devices on the final chip. Devices with repeating structural units, such as the ring oscillator, were also laid out using instances of the basic unit.

Included on the chip were many of the test structures from the original design, along with several new ones. There are three main groups of structures:

1) Resolution test patterns, resistors and capacitors for process characterization (No.'s 1-6);
2) Diode, n-channel MOSFET's and lateral BJT's (No.'s 7-12);
3) Inverter, NOR-gate, ring oscillator for simple circuit measurements (No.'s 13-15).

Figure 1 shows the chip layout and Table IV contains information on device sizes.

Process

The 4 mask NMOS process starts with 2" p-type wafers of 3-5 Ω-cm resistivity, which were blanket-implanted with boron before initial oxidation. This serves as both the field and the device threshold implant, which was moved to the beginning of the process to avoid delays during the semester. After initial oxidation (5000 A) the active (n+ diffusion) area is defined with Mask I (ACTV). This is followed by gate oxidation (800 A) and poly-silicon deposition (3500 A). Mask II (POLY) defines the gate. The poly-Si is wet etched and the active area is BHF dipped clean for n+ diffusion, taking advantage of the self-aligned source/drain feature of poly-Si gates. A spin-on phosphorous-silica film (Emulsitone) is used as the source for n+ diffusion. After drive and oxidation, Mask III (CONT) is aligned and contact openings are etched with BHF. After aluminum evaporation, Mask IV (METL) is printed and Al is defined by wet etching. Sintering is the final step and the process is completed. The process flow is shown in Figure 2. The complete process description and process modules can be found in Appendix I.

Laboratory Operations

Teaching assistants (TA's) for this course are recruited from among those graduate students who are experienced in semiconductor processing and are users of the Microfabrication Facility, the graduate research laboratory on the 4th floor of Cory Hall. This is to ensure that they have the proper background necessary to conduct a processing laboratory on their own. Also, there is a step in the process, polysilicon deposition, for which, due to safety restrictions, there is no provision in the EECS143 lab. The students go to the Microlab for that session where they can see a modern wafer processing facility and, with the aid of the TA, use the LPCVD furnace to deposit polysilicon on their wafers. This works out well.

The maximum number of students that can be accomodated per semester is 64; 8 students/session, with two 3-hour sessions per day with Monday mornings and Friday afternoons left open for maintenance. This requires three full-time TA's. The head TA conducts two sections and takes care of scheduling of laboratory preparation, equipment problems, etc. (see Appendix II). The other two handle three sections each. Office hours are held by each TA separately, also in the lab, one hour per week.

Students are working in pairs throughout the semester and submit joint lab reports: the first one at the end of processing; the second report after characterization, at the end of the semester. Lab report outlines are shown in Appendix III.

To allow sufficient time towards the end of the semester for electrical characterization, students are given a mask set and start with oxidized wafers; thus the first step they become familiarized with in the lab is photolithography. All operations are done by students; TA's are there to guide them. During the waiting periods they are assigned to run SUPREM simulations and are allowed to familiarize themselves with the measurement equipment.

Testing equipment is arranged such that there are four probe stations available; thus all four pairs in a section can work simultaneously. Two stations are connected to HP4145 Semiconductor Parameter Analyzers, on which most of the measurements are done. The C-V probe station is used to measure the capacitors and the 4th station is available to complete the resistor and circuit measurements.

Assignments in the Device Characterization Outline, shown in Appendix IV, describe in detail all the measurements to be done and parameters to be determined. Appendix V contains sample measurement results.

Conclusions

We have introduced a new process and test chip in the laboratory of EECS143 during the Fall Semester of 1987 and further tested it during Spring 1988. This report contains all the corrections found necessary and suggestions for improvement provided by the TA's.

The characterization and parameter extraction part which is the most important experience the students receive from the course, had been extended, requirements described in detail and presented in a systematic manner. With this we hope to increase the students' level of understanding of semiconductor process engineering and to enhance the overall value of the course.

Acknowledgements

Our appreciation and thanks go to Professors D. A. Hodges and W. G. Oldham, who envisioned and created this course, and provided the information about the early days; to those graduate student teaching assistant who, over the years, cared enough to suggest improvements both in the laboratory material and in facilities; and to Professor N. Cheung who arranged for the vast improvement of the testing equipment.

References

1. Deok Jung Kim, "A simplified NMOS process for an instructional laboratory," MS Report, Department of EECS, University of California, Berkeley, December, 1981.
2. G. Billingsley and K. Keller, "KIC: A Graphics Editor for Integrated Circuits," Memorandum No. UCB/ERL M83/62, Electronics Research Laboratory, University of California, Berkeley, October 1983.

EECS 143
Processing and Design of Integrated Circuits

College of Engineering
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley

Course Outline

Week	Topic
1	Overview, Implementation of IC's
2	Process Outline (MOS and Bipolar Technology)
3	Layout, Design Rules, Lithography
4	Oxidation
5	Ion Implantation
6	Diffusion **Midterm Exam I**
7	Diffusion, CVD
8	Thin-Film Deposition and Plasma Etching
9	Process Simulation, Diagnostics and Yield
10	MOS Devices **Midterm Exam II**
11	MOS Process Integration
12	Device Characterization
13	CMOS Processing
14	Bipolar Processing
15	Review
16	**Final Examination**

Table I

EECS 143
Processing and Design of Integrated Circuits

College of Engineering
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley

Laboratory Weekly Schedule
(3-Hour Sessions)

Week	Topic
1	Laboratory Sign-up
2	Orientation (Safety, Cleaning and General Information)
3	Photolithography: Mask I ACTV
4	Gate Oxidation
5	Poly-Si Deposition (Microlab)
6	Photolithography: Mask II POLY
7	N+ Deposition
8	N+ Drive and Oxidation
9	Photolithography: Mask III CONT
10	Metallization
11	Photolithography: Mask IV METL Sintering
12	**First Lab Report Due**
13	Device Characterization
14	Characterization
15	Characterization
16	**Second Lab Report Due**

Table II

EECS 143
Processing and Design of Integrated Circuits

College of Engineering
Department of Electrical Engineering and Computer Sciences
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Laboratory Equipment

Processing

Headway Research Inc. Model EC101 Photoresist Spinner
Two Thermolyne Type 1900 Hot Plates, one with OV-10600 Hot Plate Oven
Kasper Contact Aligner

Three Sola Basic Tempress-Lindberg Furnaces with 10cm diameter tubes
Thermionics Laboratory Inc. TLI-80 Evaporating System

Two Wet Process Stations (one with a hot plate)
Two Mixed-Bed Ion Exchangers for DI water
Polymetrics DI Rinse Station (self containing)
Balsbaugh Series 900 Resistivity Meter
Two Manual Spin-Dryers for 2" Wafers
Two Bausch & Lomb Optical Microscopes

Testing

Baird Atomic 4-Point Probe
Keithley Model 177 uV Digital Multimeter
Current Source

Two Probe Stations with Bausch & Lomb Microscopes
Two HP 4145A Semiconductor Parameter Analyzers
Two HP 7470A Plotters

Probe Station with Bausch & Lomb Microscope
Keithley Model 177 uV Digital Multimeter
HP 3465A Digital Multimeter
Boonton Electronics Model 72BD Capacitance Meter
Boonton Electronics Precision Decade Capacitor
Power Supply with Voltage Sweeper
1 HP 7015A X-Y Recorder

Probe Station with Bausch & Lomb Microscope
Keithley Model 177 uV Digital Multimeter
HP 3438A Digital Multimeter
HP 6235A Triple Output Power Supply
Tektronix Curve Tracer
Tektronix 2215A Oscilloscope

Two Freedom 110 Computer Terminals connected to Cory Hall port selector

Table III

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Device Sizes

(Listed numbers are layout dimensions; all contact holes are 5 μm x 5μm; metal pads are 100 μm x μm)

1) Resolution Test Patterns	Line widths as marked: 2-8 μm Rails: 10 μm
2a) Resistor, Diffused	20 □ (L = 200 μm, W = 10 μm)
2b) Resistor, Poly	20 □ (as above)
2c) Contact Chain, Diffusion	Diffused segments: 50 μm x 150 μm
2d) Contact Chain, Poly	Poly segments: 50 μm x 150 μm
3) Field Oxide Capacitor	Top Metal Plate: 200 μm x 200 μm
4) Gate Oxide Capacitor	Diffused Area: 200 μm x 200 μm Top Plate (poly-Si): 240 μm x 240 μm Contact Pad (outside poly-Si): 100 μm x 100 μm
5) Intermediate Oxide Capacitor	Top Metal Plate: 200 μm x 200 μm
6a) Junction Capacitor	Top Metal Plate: 260 μm x 100 μm Diffused Area: Central Rectangle: 300 μm x 140 μm
6b) Long Periphery Junction Capacitor	Diffused Area and Top Metal Plate: Same as above Fins: 150 μm x 20 μm
7) Diode	Diffused Area: 50 μm x 50 μm
8) MOSFETs (4)	Gate Length (L) = 2 μm, 4 μm, 7 μm, 10 μm Gate Width (W) = 15 μm
9) Long Channel MOSFETS (3)	L = 20 μm W = 20 μm, 15 μm, 10μm
10) Field Oxide MOSFET	L = 100 μm W = 100 μm
11) Large MOSFET	L = 100 μm W = 100 μm
12) Lateral BJT's	Base Widths = 5 μm, 6 μm, 7 μm Emitter Dimensions (Active Area): 50 μm x 50 μm
13) Inverter	Load: L = 10 μm, W = 5 μm Driver: L = 5 μm, W = 40 μm
14) NOR Gate	Load: L = 10 μm, W = 5 μm Driver: L = 5 μm, W = 40 μm
15) Ring Oscillator (21 Stages)	Load: L = 10 μm, W = 5 μm Driver: L = 5 μm, W = 40 μm Buffers: L = 5 μm, W = 60 μm, 80 μm

Table IV

EECS 143 Test Chip Layout

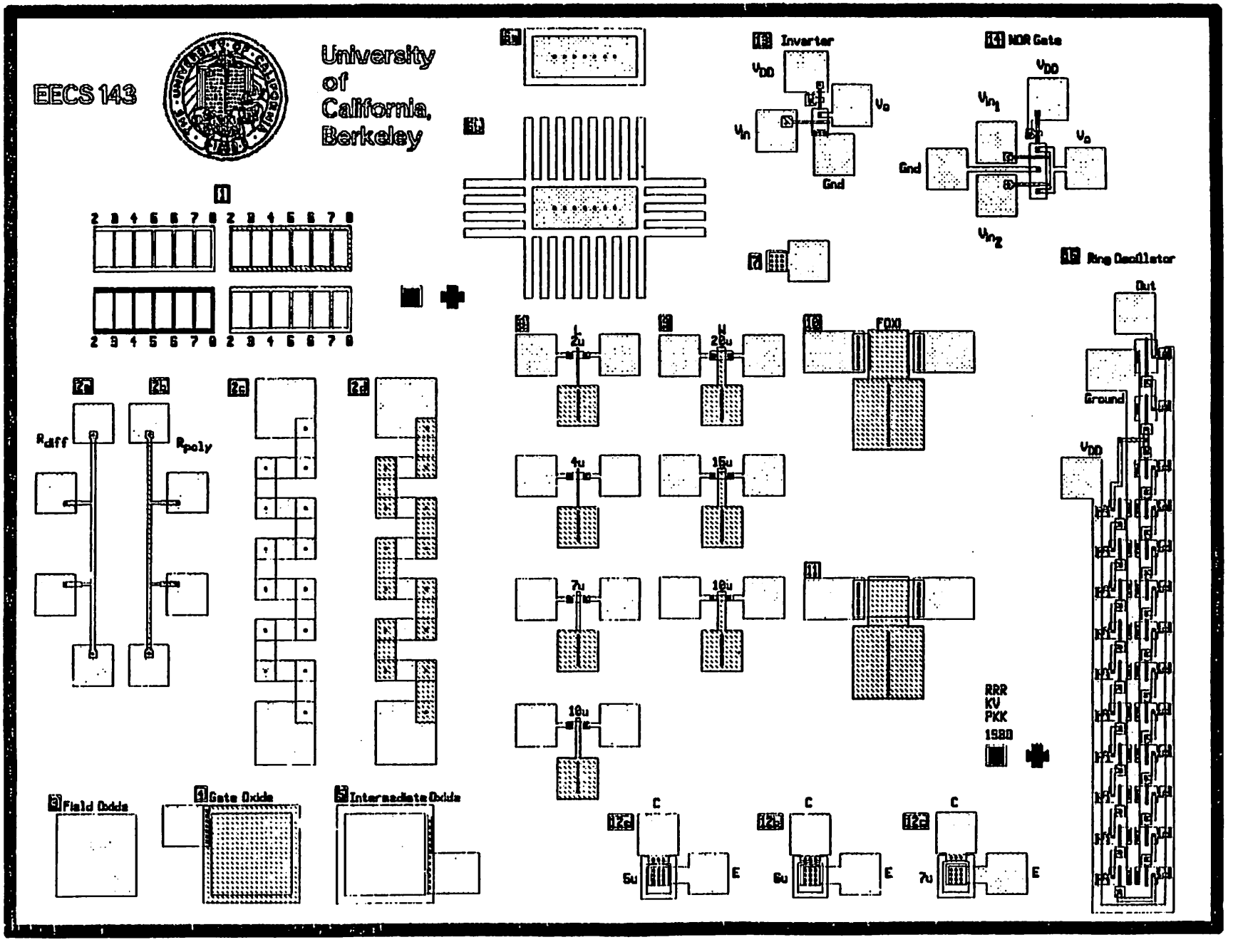
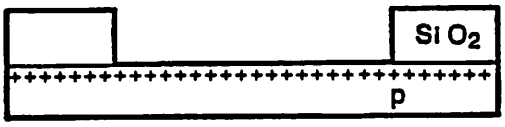
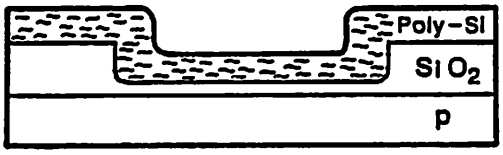


Figure 1

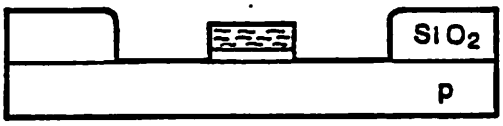
EECS 143
PROCESS FLOW



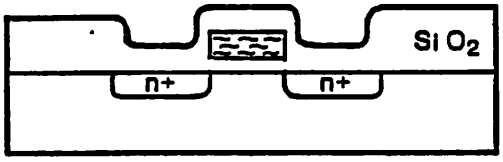
I. Starting wafer: 3-5 Ω-cm p-type
ion implantation: boron.
II. Initial oxidation: 5000Å
III. Mask I: ACTV
Active area definition.



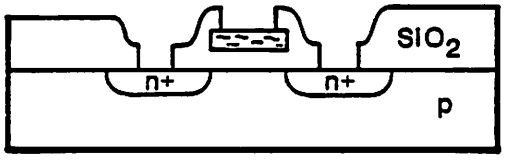
IV. Gate oxidation: 800Å
V. Poly-Si deposition: 3500Å



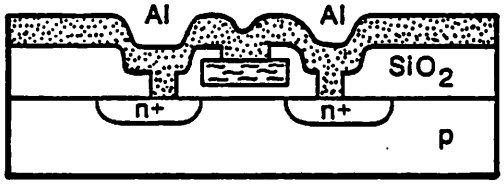
VI. Mask II: POLY
Gate definition.



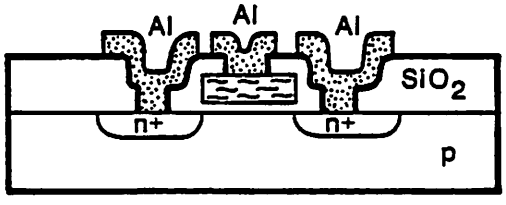
VII. S/D deposition: N+ spin-on glass.
VIII. S/D drive and oxidation: 1000Å



IX. Mask III: CONT
Contact etch



X. Metalization



XI. Mask IV: METL
Metal Etch
Sinter

Figure 2.

Appendix I

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5μm NMOS Process
Poly-Si Gate

Version 3.3

I. Starting Materials

1. Wafers
   - A. 3" p-type silicon wafers with a resistivity of 3-5 Ω-cm and <100> crystal orientation. In addition to work wafers, each section will receive one wafer to be used as a control in step IV.
   - B. Blanket Implant: $3 \times 10^{12}/cm^2$, B^{11}, 60 KeV.
2. Masks

Mask Descriptions
4" x 4" Chrome Plates

Mask Name	Defines	Field
ACTV	Active Area	Dark
POLY	Gate	Clear
CONT	Contact	Dark
METL	Metal	Clear

II. Initial Oxidation - 5000 Å

1. Standard clean your work wafer (Standard Process Module I).
2. Oxidize wafers at 1050°C for 5-70-5 minutes (dry-wet-dry) O_2.
3. Measure oxide thickness. It should be approximately 5200 Å.

III. Active Area Photolithography

1. Standard resist coating (Module II).
2. Standard photomasking: Mask I (ACTV) (Module III).
3. Oxide etching and inspection (Module IV).
4. Do steps 1 and 2 *only* of the standard resist strip (Module VI).
5. Measure line widths of test pattern with filar eyepiece in microscope.

IV. Gate Oxidation - 800 Å

Gate oxidation is done in tube #3 (bottom) at 1100°C following a TCA clean. Gases used are N_2 and O_2. See Furnace Operations in Module VII.

1. Furnace Clean
   a) Do Steps 1 and 2 of the furnace operations procedure (Module VII). Let O_2 flow at maximum rate (15+) for 10 minutes *before* turning on TCA. N_2 is off. **It is critical that this sequence is followed precisely. Failure to do so will result in: black carbon (soot) being deposited throughout the gas lines and tube; or the possibility of an explosion!**
   b) TCA clean for 1 hour at 1050°C before oxidizing wafers. Wafer boat should be in the hot zone during TCA cleaning.
   c) When 1 hour has elapsed, wait 10 minutes after turning off TCA before inserting wafers.
2. Standard Clean (Module I)
   Standard clean wafers including an implanted control wafer from Step I.
3. Wafer Loading and Oxidation
   a) Push wafers into tube as described in Module VII, Steps 4-10. Wafers are inserted in 10% O_2 and 90% N_2: set O_2 to 1.5 cm and N_2 to 4 cm on flowmeter.
   b) When wafers are in the furnace, change flows, maintaining the following sequence: O_2 to 12 cm and N_2 to 0 cm. Start timing.
   c) After 34 minutes of oxidation time at 1100°C have elapsed, turn off O_2 valve and close O_2 flowmeter. Set N_2 flow to 4 cm.
   d) Anneal in N_2 for 10 minutes. Pull wafers out in N_2 as described in Module VII - Steps 12-17.
4. Check oxide thickness on control wafer, then etch off oxide completely in buffered HF. Measure resistivity and use this to estimate channel doping concentration.

V. Poly-Si Deposition - In Microlab

1. Standard clean wafers.
2. Deposit 3500 Å Phosphorus-doped polysilicon. SiH_2 flow = 120 ccm; PH3 flow = 1 ccm. Wafers should be loaded in the center boat for tylan11. Remove the 4" dummies (except for the very first and last slots) and load 3" wafers in their place. Be sure to include a few 3" dummies on either side of the 3" work wafers.
3. Include control wafer with 1000 Å SiO_2; measure poly-Si thickness with Nanospec.

VI. Gate Photolithography

1. Apply standard resist coating (Module II).
2. Standard photomasking: Mask II (POLY) (Module III).
3. Etch poly-Si (Module V).
4. Etch oxide in active area until clear (~1 minute) in BHF.
5. Do Steps 1 and 2 of the standard resist strip, skip the rest (Module VI).

VII. Source-Drain Deposition (N^+)

1. Standard clean wafers without HF dip.

2. Spin Phosphorosilicafilm at 3000 rpm for 20 seconds including p-type test wafer from step IV-4.
3. Bake at 200°C for 15 minutes in bake oven.
4. N^+ pre-diffusion is done at 1050°C in furnace tube #2 (center). Set O_2 flowmeter to 1.5 cm and N_2 to 4 cm. (This corresponds to 10% O_2 and 90% N_2.) The setting is constant during push, deposition and pull.
5. Follow the steps in the furnace operation procedure. Pre-drive time is 5 minutes.
6. Phosphorus glass removal: dip wafers in 10:1 H_2O:HF for 1 minute.
7. Rinse in D.I. water for 10 seconds in each of 3 beakers successively, then spray rinse.
8. Spin dry.
9. Measure resistivity on control wafer.

VIII. Source-Drain (N^+) Drive and Oxidation

1. This step is done at 1050°C in tube #2. Check gas connection to allow for steam oxidation, dry O_2 and N_2 flow. Set dry O_2 to 6.5 cm on flowmeter.
2. Turn on bubbler heater to 98°C. Turn on heater tape.
3. Fill bubbler ~80% with D.I. water. Use a piranha cleaned, well rinsed beaker to fill bubbler.
4. Standard clean wafers, including control wafer used in step VII.
5. When the water is boiling in the bubbler (approximately 20 minutes) push wafers into furnace in dry O_2.
6. Set O_2 flowmeter to 2.5 cm and switch valves to wet O_2. Wet oxidation time is 12 minutes.
7. Turn off wet O_2 and turn on N_2. Set to 4 cm on scale.
8. Anneal for 25 minutes in N_2. Pull wafers out in N_2.
9. After wafers have cooled, immediately apply standard resist coating (Module II).
10. Check oxide thickness on control wafer, then etch oxide completely off in buffered HF and measure resistivity.

IX. Contact Cut

1. Standard photomasking: Mask III (CONT).
2. Do oxide etch for calculated time (Module IV). The back side of the wafer should dewet (metallic in color) indicating no oxide present. Inspect under microscope. You may find it difficult to tell whether the etch is complete, therefore, remove resist (Module VI) and inspect wafer again. If the contacts are not clear, etch for an additional 15 seconds and check again. Contact holes appear white when cleared.

X. Metallization

1. Standard clean wafers. Do the last dip in 10:1 just before wafer is ready to go into evaporator.
2. Aluminum Evaporation (Module VIII).

XI. Metal Definition

1. Standard photomasking: Mask IV (METL) (Modules II and III).

2. Metal Etch:
   a) Pour 300 ml of Al etchant into glass beaker; heat on hot plate to 50°C (sink2).
   b) Immerse wafer in water to wet.
   c) Place wafer in aluminum etchant at 50°C. Bubbles will form on the surface of the wafer as the etchant removes the metal. Be sure to keep your wafer moving to replace chemical at the wafer's surface. Bubbling will subside as etch reaches completion. Etch rate of Al is ~100Å/sec at 50°C.
   d) Rinse wafer very well in DI water. Inspect.
3. Remove resist in acetone, rinse well in DI water, spin dry.
4. Sintering:

   This step is done in furnace tube #1 (top) at 400°C in forming gas (90% N_2, 10% H_2) for 20 minutes. Gas flow is set to 4 cm. Slow push/pull is not necessary.

Process is now completed and the wafers are ready for characterization.

K. Voros
1/16/92

EECS 143
Processing and Design of Integrated Circuits

College of Engineering
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Standard Process Modules

I. Wafer Cleaning

1. Mix piranha solution as follows:
   a) Measure out 5 parts of H_2SO_4 in plastic beaker
   b) Very slowly add 1 part of H_2O_2.
   Note: This mixture is self heating. When cool it may be refreshed by very slowly adding 1 part of H_2O_2.
2. Immerse wafers in piranha solution for 10 minutes.
3. Rinse in DI water for 10 seconds in each of 3 beakers successively, then spray rinse.
4. Dip in 10:1 solution of H_2O:HF for 20 seconds.
5. Rinse in DI water for 10 seconds in each of 3 beakers successively, spray rinse, then place in Polymetrics rinser until resistivity meter indicates 10-15 MΩ or for 10 minutes.
   Note: Clean, bare silicon is hydrophobic and metallic in appearance.
6. Spin dry.

II. Resist Coating

1. Spin wafers immediately after high temperature treatment. If this is impractical, then dehydrate at 120°C for 10 minutes in N_2.
2. Place wafers in HMDS vapor for 2 minutes.
3. Immediately spin on KTI 820 photoresist at 4000 rpm for 30 seconds.
4. Soft bake at 120°C for 1 minute on hot plate.

III. Photomasking

1. Following Kasper Mask Aligner Instructions align wafers to mask and expose.
   Cover wafer box with Al foil when carrying exposed wafer into etching room.
2. Pour 300 ml KTI 934 1:1 developer solution into beaker.
3. Turn off white light in etching room, develop and etch only in yellow light.
4. Dip exposed wafer in the 1:1 developer solution for 30 seconds and agitate slowly.
5. Rinse in DI water for 10 seconds in each of 3 beakers successively, then spray rinse.
6. Spin dry.
7. Inspect under microscope with yellow filter. Measure line widths of test pattern with filar eyepiece. Record data.

8. If not completely developed repeat Step 4 for 15 seconds, then Steps 5-7.
9. Hard bake photoresist for 20 minutes in 120°C oven.

IV. Oxide Etching

1. Fill the 4" deep Pyrex dish with DI water for a water bath. This is to insure more uniform etchant temperature and etch rate.
2. Measure out 300 ml of buffered HF in plastic beaker and place beaker in the water bath. Buffered HF is a mixture of NH_4F (ammonium fluoride) and HF 5:1. Its etch rate of thermal SiO_2 is ~1000A/min. at 25°C.
3. Determine etching time according to the oxide thickness to be etched plus 20% overetch. The overetch is performed for process latitude.
4. Dip wafer in buffered HF for the length of time determined in Step 2. Etching is complete when the liquid "beads" on bare Si; i.e. a hydrophobic surface is detected.
5. Rinse in DI water for 10 seconds in each of 3 beakers successively, then spray rinse only (*no* Polymetrics).
6. Spin dry.
7. Inspect etching for completion under microscope.

V. Polysilicon Etching

1. Fill the 4" deep Pyrex dish with DI water for a water bath. This is to insure more uniform etchant temperature and etch rate.
2. Use premixed silicon etchant obtained from the Microlab. Etch rate: ~50-100 Å/second.
   Composition: 64% HNO_3 / 33% H_2O / 3% NH_4F
3. Determine necessary etch time based on polysilicon thickness and add 10% overetch.
4. Dip in 10:1 solution of H_2O:HF for 20 seconds. Rinse in DI water.
5. Immerse wafers in etchant for determined etch time. Watch the color changes as the silicon is etched.
6. Rinse in DI water for 10 seconds in each of 3 beakers successively.
7. Spin dry or continue to etch.
8. Inspect etching for completion under microscope.

VI. Resist Strip

1. Dip wafer in acetone for 2 minutes.
2. Rinse in DI water for 10 seconds in each of 3 beakers successively, then spray rinse.
3. Piranha clean for 10 minutes.
4. Rinse in DI water for 20 seconds in each of 3 beakers successively, then spray rinse.
5. Dip in 10:1 H_2O:HF for 20 seconds.
6. Rinse in DI water for 10 seconds in each of 3 beakers successively, spray rinse, then place in Polymetrics rinser until resistivity meter indicates 10-15 MΩ or 10 minutes.
7. Spin dry.

VII. Furnace Operations

Furnace temperature should be checked with thermocouple before students start working.

1. Before starting to prepare wafers for a furnace operation check if the furnace controller is set to the required temperature.
2. Check gas inlet connection and set gas flow as required for wafer insertion in the tube.
3. Open sliding exhaust door in the loading vestibule.
4. When wafers are ready for loading remove end cap from tube (holding it with an insulating glove.) Place end cap in furnace vestibule below.
5. Pull out wafer boat with short push rod onto half-shell boat carrier. Place it on the table and let it cool.
6. Load wafers back-to-back on wafer boat.
7. Pull boat into cylindrical carrier.
8. Attach cylindrical carrier to end of tube and push boat into tube with long push rod through end hole of carrier.
9. All high temperature operations are done with slow push and pull as follows: push boat one inch every 10 seconds until mark on push rod lines up with vestibule door, a total of 36 inches. Pulling is accomplished similarly.
10. Timing starts when the boat is pushed in. Remove cylindrical carrier and place end cap on tube.
11. Sequence gas flows as required by process step.
12. After the last step remove end cap, attach cylindrical carrier to end of tube and slowly pull out boat, as described in Step 9, into carrier.
13. Place carrier with boat on table and let it cool.
14. Pull boat into half-shell carrier and unload wafers.
15. Place boat back into end of tube and replace end cap.
16. Place push rods back in appropriate storage tubes.
17. Never mix quartz ware between tubes to avoid cross contamination.

VIII. Aluminum Evaporation

1. Before starting evaporation in the TLI-80 system, fill up cold trap with liquid nitrogen. Push OPERATE button.
2. To load/unload push CHANGE button. Wait 10 seconds and then flip toggle to the 'ON' position. The bell jar will fill with N_2 and can be raised by hand holding the cage support.
3. Lift stainless steel wafer holder out of the inner glass cylinder ("chimney") and place it on the table covered with lint-free paper.
4. a) Place a clean glass slide in stand inside chimney for a clear window.
   b) Hang a clean Al charge in the middle of the tungsten coil.
   c) Turn shutter into COVER position (covering charge).
   d) Place wafer *facing down* on top of wafer holder.
5. Place wafer holder back inside the chimney.
6. Wipe stainless steel base and bottom of bell jar with lint free paper soaked with methanol.

7. Lower bell jar and push OPERATE button. Push bell jar cage down to close it all around until vacuum begins to hold it tight and cannot be lifted.
8. Set pressure gauge to PIRANI and observe increasing vacuum. Switch gauge to lower scales, (DISCHARGE), as pressure begins to drop.
9. Pump down to 2-5x10^{-6} torr. It should take ~30 minutes.
10. Switch electrode power to ON. Increase power by turning powerstat slowly clockwise. At ~40 Amps coil begins to glow, but the Al charge does not melt. This can be observed through the slide window. Let heat @ 40 amps about 20 seconds to drive off water vapor.
11. Increase electrode power to ~60 Amps. The charge will evaporate suddenly and the slide will be coated with Al. As soon as this happens open the shutter and wait for 20 seconds. Slowly turn down powerstat and switch electrode power to OFF.
12. Push CHANGE button, toggle N_2 vent switch on and wait until the bell jar is released. Raise bell jar, unload and load as described in Steps 2-7.
13. When all the wafers are done repeat Steps 5-8. This will pump the system and close the HV valve, leaving the manifold and cold trap continuously pumped on. Always leave the system in CHANGE with toggle valve off.

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1/16/92

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Lab Safety and General Cleaning Procedures

Safety Precautions

I. Using Acids

At many points in the fabrication process strong acids are used as etchants. These cause severe burns if kept in contact with your skin for more than a few seconds, and will cause blindness if splashed in your eyes. Especially dangerous is HF, a component of virtually all oxide etchants. HF burns do not hurt immediately on contact, but by the time they do start to hurt, it is too late. The result is a severe burn which is very painful over prolonged periods and is slow to heal, sometimes taking several weeks. Some precautions to observe are:

a) Always wear protective clothing, including a face mask and rubber gloves, when handling corrosive chemicals. Check gloves for pinholes before putting them on.

b) In preparing a solution involving an acid, *always* add the acid last, except for piranha, in which case you add hydrogen peroxide (H_2O_2) to sulfuric acid (H_2SO_4).

c) Use the chemicals only in the designated area; do not transport chemicals around the room in beakers. Never pour chemicals back into the original container.

Always use **plastic** beakers for etchants containing HF, which eats glass.

Always seek help if you have any questions and make sure you are checked out on every new chemical procedure. *Never* try a new procedure without being checked out on it!

f) Discarding acids:

1) Aspirate buffered HF, 10:1 H_2O:HF, and silicon etchant, or dilute with water and pour them down the drain with "plenum flush" on.

2) Piranha (H_2O_2 & H_2SO_4) is aspirated.

II. Organic Solvents

a) Solvents used in the lab are: methanol, trichloroethane, and acetone. These are harmful when inhaled -- use only in an appropriately vented area.

b) Discarding solvents:

Pour all organic solvents into special container marked "Organic Waste".

Caution: Do **not** mix piranha and organic waste. The resultant mixture is explosive!

III. Photoresist Developer

a) The developer contains potassium hydroxide (KOH). It will blind you if you get it in your eyes and leave it there.

b) Discard developer by aspirating or diluting it with water and pouring it down the drain with "plenum flush" on.

ALWAYS ASK WHEN UNSURE OF PROCEDURE! This is the only way to maintain a safe laboratory for yourself and your fellow students.

Chemical Information

Students should be aware that the Environmental Health and Safety Office has safety information for all chemicals in the lab (and for any other lab on campus). This information is contained in the Material Safety Data Sheets (MSDS) and is available to any student or employee of the University who works with chemicals. Sample MSDS are posted in the lab for your perusal.

General Rules

Never touch semiconductor specimens, the insides of beakers, the business end of the tweezers, or photolithographic masks with your fingers. This also applies to furnace boats (especially) or any other equipment which can transfer particles from your skin to the semiconductor devices. Obviously, contaminating a furnace (for example, by touching the boat and then inserting it into the furnace where any contaminants are vaporized) will ruin not only your attempts at device fabrication, but those of all who follow.

Cleaning Procedures

General cleaning procedures for preparing your sample follow. They fall primarily into three categories: (1) removal of gross contaminants; (2) removal of organic contaminants; and (3) removal of light and heavy metallic ion contaminants. All instruments used, i.e., beakers, tweezers, etc., must be cleaned before being used to clean wafers.

I. Cleaning Tweezers, Wafer Boxes and Plastic Wafer Holders

Scrub parts in liquid detergent, such as "Micro". Rinse well in DI water. Blow dry.

II. Cleaning Glass and Teflon Beakers

a) Scrub parts in liquid detergent, such as "Micro."

b) Rinse in DI water.

c) Soak non-metallic parts for 15 minutes in piranha (H_2O_2:H_2SO_4 1:5). Add the H_2O_2 to the solution just before immersing wafer.

d) Rinse in DI water for 5 minutes.

e) Let dry top down, on lint-free paper.

III. Correct Wafer Handling Technique

To minimize contamination from tweezers, plastic "holders" are available for handling wafers in solutions, and should be used in lieu of tweezers. Wafer drying is accomplished by spinning in special spinner so designated.

IV. Cleaning Furnace Apparatus after Contamination

a) 5% HF:H_2O for 20 seconds.

b) Rinse, blow dry.

c) Bake for 30 minutes.

V. Cleaning Photomask

This procedure should be performed at least 30 minutes before photo step.

a) Dip in acetone for 15 minutes.

b) Rinse.

c) Scrub with cotton ball dipped in dilute microclean.

d) Rinse well.

e) Soak in 1:1 methanol:water for 15 seconds.

f) Soak in 100% methanol for 15 seconds.

g) Blow dry.

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Kasper Mask Aligner

I. Introduction

The Kasper Wafer Alignment System is an integrated optical-mechanical, pneumatic-electrical system which allows accurate alignment of sensitized semiconductor wafers with a mask and exposes them to ultraviolet radiation. It is a high precision piece of equipment and should be treated with care. It is imperative that you understand the machine completely before proceeding.

Keep in mind that a great threat to long life for the Kasper Aligner is dirt. The exposure source is a 200 watt high pressure mercury arc lamp. It is left on at all times. Do NOT turn it off. If the lamp is off, do not turn it on as there is a special procedure for relighting.

II. Operating Procedure

1. You will find the machine in standby mode.
2. Power button, PRESS CONT, MASK CLAMP,and MASK LOAD buttons should be lit.
3. Turn on the vacuum by operating the toggle valve mounted on the table to the right of the machine. A hissing sound indicates that the vacuum is on.
4. Press the VISUAL ALIGN switch. The top portion of the mask aligner will automatically rise.
5. Lif off the mask support plate and place your mask in the vacuum chuck opening with the emulsion or chrome side facing down. Center the mask support plate over the mask and press the MASK CLAMP button to fix mask plate to mask. Center mask and mask plate over the opening and press MASK LOAD to fix assembly to the mask vacuum chuck.
6. Slide the wafer vacuum chuck assembly out all the way towards you. With tweezers, center your wafer on the chuck. Fully push the assembly back under the mask. At this point, you can do gross alignment of the mask to the wafer.
7. Press the VISUAL ALIGN switch to lower the optical head.
8. Press WAFER LOAD switch and the wafer will be raised under the mask and held in place. The SEP button should light, indicating that there is a separation between the wafer and the mask. The instrument goes into separation mode automatically.
9. Press the VISUAL ALIGN switch. It causes the optical head to raise so that you can check whether the wafer is being loaded correctly. If the loading appears to be normal, press VISUAL ALIGN to lower the head and proceed with the alignment.

   There are three positions for the optical turret. A "Row and Column" position allows coarse alignment with a lower power, single field microscope. A "Split Field" position allow fine alignment at a high power by simultaneous viewing of two separate areas of the wafer. The "Expose" position provides a reflector to direct the UV light down to the wafer.

The alignment system consists of a precise X-Y stage which moves the wafer and mask together (scan) and a second X-Y stage which adjusts the wafer position with respect to the mask (align). Incorporated with the "align" stage is a rotating knob for angular alignment. Each stage is controlled by a hand disc. There are two degrees of alignment for the "align" stage. Shifting from 150:1 ratio to 3:1 ratio is done by pressing the button on the right-hand disc control. Rotational alignment is accomplished with either coarse linear actuated motion or a 700:1 rotational fine adjustment.

10. Turn the optical turret to the "Row and Column" position and check that the instrument is in the SEP mode. Turn up the power for the microscope illuminator.
11. Roughly align the wafer pattern to the mask pattern in the desired position by first making the rotation adjustment and then the X-Y adjustment.
12. Turn the optical turret to the "Split Field" position to perform fine alignment of the wafer to the mask. At least one alignment mark should be visible in each half of the split field image. Perform fine rotational and X-Y alignment with the rotation knob and X-Y alignment disc.
13. When alignment is complete, press the CONTACT button which brings the wafer into contact with the mask and actuates the positive pressure. Check to make sure the alignment is correct. If an adjustment is necessary, press the SEP button and realign.
14. Rotate the optical turret to EXPOSURE position, check the timer for correct setting, and press the MANUAL EXPOSE button. You can enter 3 digits on the timer for exposure. Be aware that the last number is in units of .1 seconds (e.g. a setting of 100 is 10.0 seconds!). The maximum timer setting is 99.9 seconds.

    Exposure cannot occur unless the wafer is in contact with the mask. An interlock system ensures the safe, correct exposure.
15. Slide the wafer vacuum chuck assembly out all the way towards you. Remove the wafer with tweezers, and then return the wafer vacuum chuck assembly to the alignment and exposure position.
16. To remove the mask, press the VISUAL ALIGN button which raises the optical head. Press the MASK CLAMP button (light will go on) to release the mask support plate. Press MASK LOAD button (light will go on) to release the mask from the mask vacuum chuck.
17. Return the optical head to the down position by pressing the VISUAL ALIGN button.
18. Turn off the vacuum toggle valve. Decrease the power to the microscope illuminator in order to prolong bulb life.
19. Do not turn off power.

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Description of a Basic Vacuum System

The following is intended for those who have had limited experience in the high vacuum field. The system illustrated (Figure 1) contains the essential elements typically required to obtain high vacuum. The most common and reliable systems utilize three pumping devices: The rotating mechanical pump, the diffusion pump, and the cold trap. Other system components, such as valves and baffles, aid or control the action of these pumps. (For the sake of simplicity, no gauges are shown in Figure 1.)

1. Mechanical Pump

(Capable of reducing pressure to about 10 millitorr.) A typical mechanical pump is shown schematically in Figure 2. Mechanical pumps physically "sweep" the air from the system, usually with a rotary device as shown. The rotor is eccentric to the pump cavity. The rotating vane (or sweep) is kept in contact with the walls of the pump cavity by means of a compression spring.

Rotating vane, positive displacement pumps have large gas handling capacities, but cannot achieve high vacuum. They are used for two purposes: to remove ("rough") the bulk of the air from a system which is initially at atmospheric pressure, and, once this is accomplished, to "back" the diffusion pump, (see below), since a diffusion pump cannot exhaust against atmospheric pressure. Hence, mechanical pumps are often called roughing pumps, backing pumps or forepumps. In our illustration (Figure 1) a single pump serves for both roughing and backing. In some applications, two pumps may be used.

2. Diffusion Pump

(Capable of reducing system pressure to the region of 10^{-7} torr[1]). A diffusion pump has a maximum pressure against which it can exhaust; this is usually in the mtorr region. (The maximum exhaust pressure is also known as the "tolerable forepressure".) The mechanical pump noted above provides and maintains this exhaust pressure for the diffusion pump.

Fast pumping action is achieved through the use of high speed jets of oil vapor which collide with gas molecules and compress them in the direction of the mechanical pump (see Figure 3). (The term "jet"is used to refer to both the vapor stream and to the nozzles from which the vapor issues.)

The oil pool at the bottom of the pump is heated, causing oil vapor to be forced up the jet stack. The vapor strikes the umbrellas, and is projected downward and outward through the nozzles of the jet stack. In passing through the narrow jets, the oil vapor flows at a velocity near that of sound. The high speed vapor jet collides with gas molecules giving them a downward direction toward the foreline. The oil molecules condense on the walls of the pump which are cooled either by an air stream or by water, and flow back to the bottom pool. Thus, a continuous cycle of vaporization, condensation and revaporization takes place. Oil of very low vapor pressure is used in these pumps.

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[1]1 torr = 1 mm Hg

It will be noted that the jet streams are in series; the illustrated pump is a "three-stage" type.

3. **Baffle** (water cooled)

Not all oil is contained and condensed by the diffusion pump. A small amount can escape toward the HiVac area of the system. This "backstreamed" oil is detrimental to the system. To contain it, a water-cooled baffle, shown in Figure 3, is located between the diffusion pump and the cold trap. Most back-streamed diffusion pump oil molecules are condensed on the internal water-cooled baffle disc and returned to the diffusion pump in the form of liquid oil. The baffle helps keep the refrigerated surface of the cold trap operating at maximum efficiency.

4. **Cold Trap**

(Shown with liquid nitrogen as refrigerant in Figure 3). This device reduces pressure by condensing, or freezing out, onto its cold surfaces, condensable vapors that may exist in the system. It also prevents oil vapor from the diffusion pump from diffusing back, or "backstreaming", into the system. By removing "condensables" such as water vapor, a trap actually serves as a pump. The trap is filled after the system has been evacuated to a pressure of less than one mtorr, when most of the condensable vapors have been pumped out of the system by the mechanical and diffusion pumps.

5. **Roughing Line and Valve**

Exposure to atmosphere when at operating temperature will result in decomposition of diffusion pump oil. It is therefore necessary to employ a bypass line around a heated diffusion pump when evacuating a chamber from atmospheric pressure to a "rough" vacuum prior to connecting the chamber to the diffusion pump; hence, the terms "roughing line" and "roughing valve".

Valves 1 and 3 (Figure 1) serve to isolate the diffusion pump, the baffle and cold trap from the object being roughed. During roughing, Valve 2 is open. When roughing has been completed (at ~20 mtorr), Valve 2 is closed before Valves 3 and 1 are opened.

The manifold vent valve admits air to the port manifold to "break" the vacuum and make possible the removal of objects after they have undergone vacuum processing. Valves 1 and 2 must be closed during this operation if the pumps on the vacuum system are still in operation.

The mechanical pump vent valve serves to admit atmosphere to the roughing line, thus bringing the mechanical pump to atmospheric pressure. It is used when shutting down the system; the diffusion pump is turned off and allowed to cool, and then the mechanical pump is turned off. Bring the stopped mechanical pump to atmospheric pressure prevents mechanical pump oil from bring drawn back into the foreline. Valves 1 and 3 are usually closed during the operation, thus maintaining the diffusion pump, cold trap and baffle under high vacuum. This assures a clean system when starting up at some later date.

R. Hamilton
7/25/88

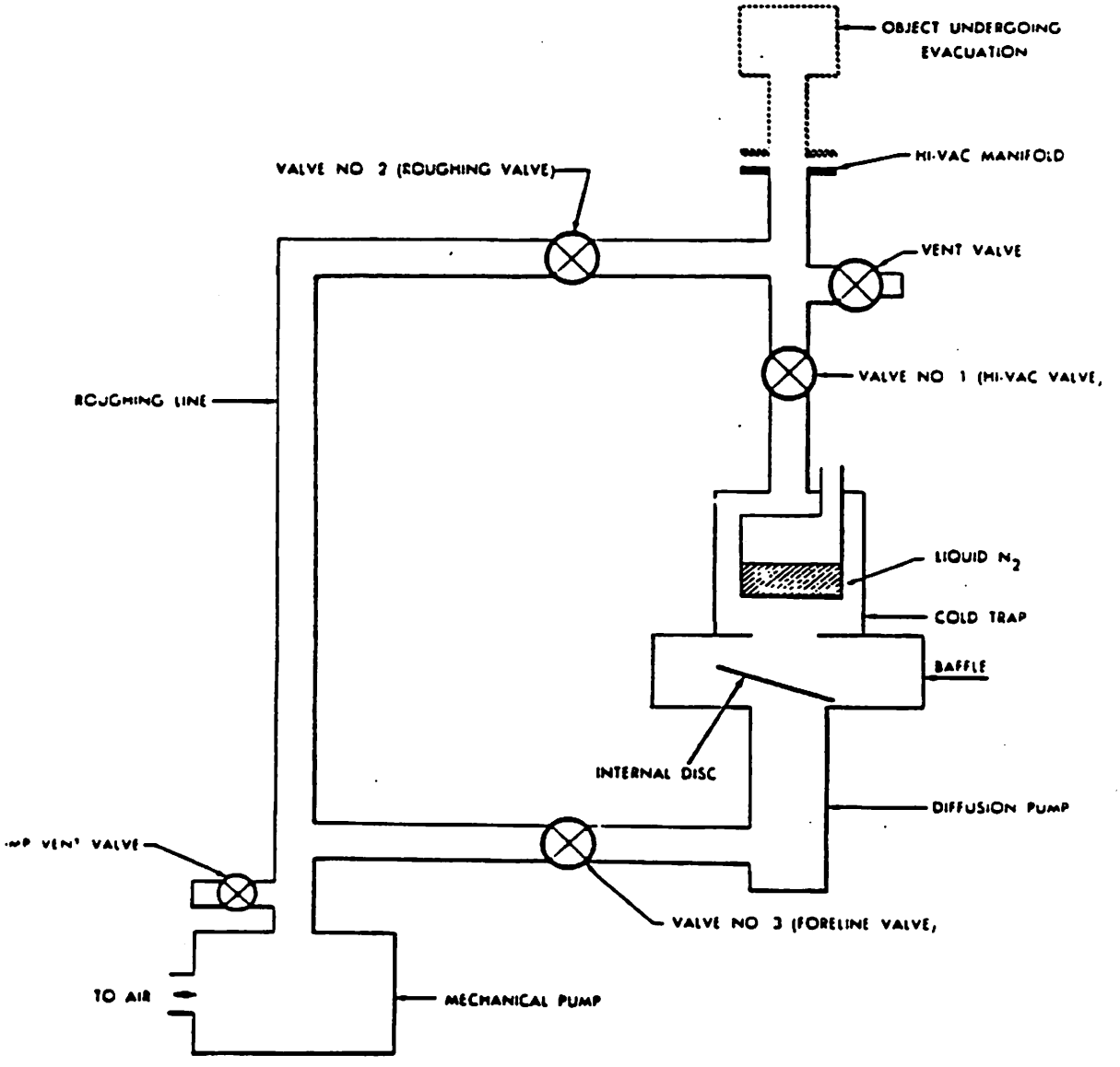

FIGURE 1 - TYPICAL VACUUM SYSTEM

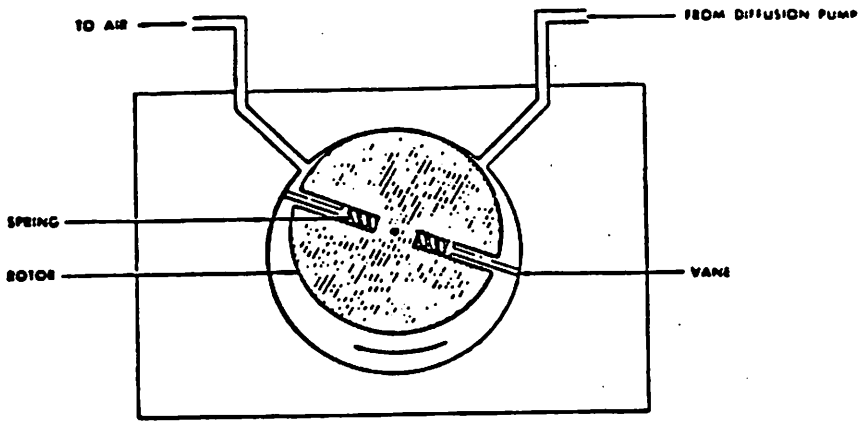

FIGURE 2 - MECHANICAL PUMP

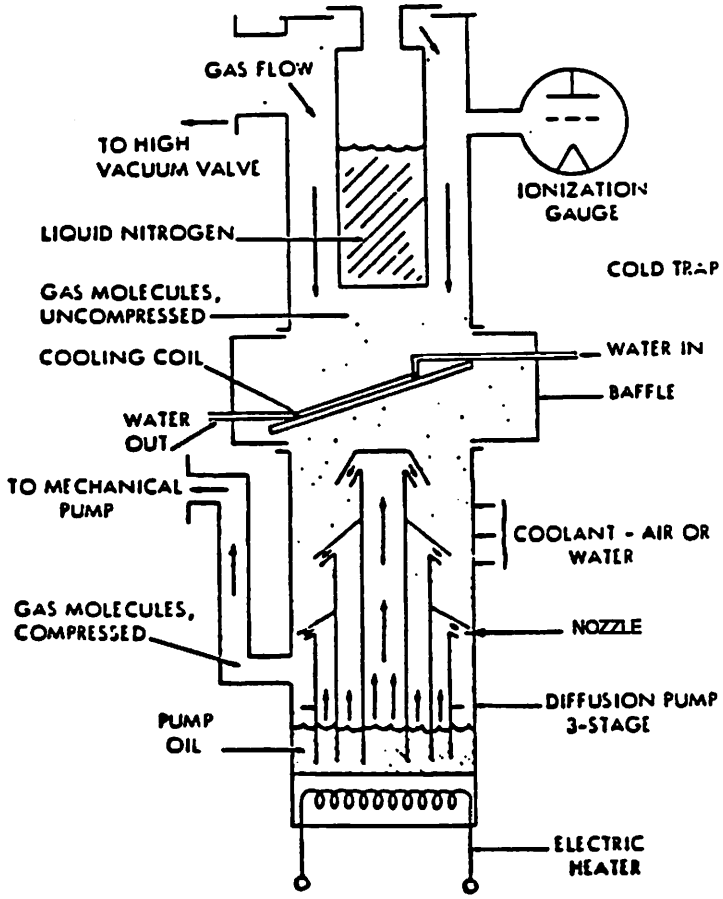

FIGURE 3 - DIFFUSION PUMP, BAFFLE AND COLD TRAP

Appendix II

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Teaching Assistants' Pre-Semester Laboratory Preparation

1. Arrange an interview with Debra Hebert, Microlab Process Supervisor.
2. Piranha clean all beakers, wafer holders, wafer boxes.
3. Degrease stainless steel tweezers: TCA, acetone, methanol.
4. Clean masks as described in the General Cleaning Procedures
5. Clean Polymetrics rinser by draining, wiping clean with lint-free towels, removing every particle, then refilling with D.I. water. Turn on and see if resistivity in cell 2 (outgoing water) will reach ≥15 MΩ. Leave Polymetrics rinser on continuously during the semester.
6. Dismantle and clean water bubbler system with piranha, rinse well.
7. Wipe off every piece of equipment with Microclean; clean off photoresist residues (with acetone) from all knobs, tables, floor, etc. Clean resist spinner thoroughly.
8. Check gas supply; turn on gas flow to check for proper operation.
9. Check waste bottle supply; obtain additional empty bottles from Microlab if necessary.
10. Obtain necessary chemicals and materials from Microlab. Use proper checkout procedure. Account: ee143.
11. Put out new lab coats and disposable booties. Disposable lab coats are worn until they are visibly soiled or torn. Booties are reused and thrown away after two weeks.
12. Check safety shower by holding bucket up to shower head and pulling chain.
13. Check eye wash. Refill with DI water.
14. Turn on fans. Leave them on all semester.
15 Report on computer, in equipment problem log for 'ee143' on argon all work that was done and repairs needed.
16. Report on computer when lab is ready for custodian to strip floor.
17. Use computer "mail ee143@argon" to communicate all problems, questions, etc., with the TA's, the professor and Microlab staff.

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Teaching Assistants' Daily Start-Up and Shut-Down Procedures During Processing

I. Daily Start-Up Procedure

1. Turn on services only to equipment to be used that day.
2. *Always* turn on N_2, using the valve near the top of the tank. This cylinder is located at the front of the service chase. Keep the valve that controls the output around 50 psi.
3. Switch on lights in Diffusion/Etching room and photoresist room.
4. If a furnace is to be used, set temperature controller to indicated number about 30 minutes before use. Turn on gas flow to tube. Check temperature, with TC in the middle of the tube, when furnace has stabilized.

   At the end of the process run, turn down gas flow to 2 cm on flowmeter, and turn down furnace temperature to a setting of 400°C.
5. If needed, turn on the vacuum pump for the Kasper and analytical equipment using the switch on the cord in rear of the service chase. Other vacuum is supplied by a venturi vacuum system mounted on the wall on the right side of the chase. Turn it on by opening the red valve until air flow is heard (both black valves should already be open).
6. If the aligner is to be used, turn on air toggle switch to the Kasper. Aligner power and light remain on at all times.
7. Check that chemicals that will be needed during the lab are there. Check that organic waste bottle is not full.

II. Daily Shut-Down Procedure

1. Close N_2 cylinder in service chase. Turn off vacuum supplies.
2. Turn off light in Photoresist room, leave blower on. Close door.
3. Turn off light in Diffusion/Etching room. Leave on last sink exhaust (where acid waste bottle is stored). Polymetrics rinser stays on all the time. Close door.
4. If a furnace was used, close gas cylinder when tube cools down.
5. Check if equipment used is cleaned and put away, including chemicals. Check condition of each waste bottle; exchange with empty one if more than 3/4 full. Leave lab neat and clean.
6. Send e-mail when waste bottles are full. Put them on the cart in the service chase. Also put empty bottles (e.g. from Si etchant) there.

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Appendix III

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Lab Report 1

Each group of two students will submit one joint report.
The report should be organized as follows:

1. Process Variations (8 Points)

Concisely describe any steps that were done differently from the descriptions in the lab manual. Include any measurements that were done during processing (oxide color and thickness, resistivity, etc.). Why were these steps done differently and how did it affect the outcome of the step? We are looking to see that you understand how the process steps work.

2. Profiles (25 Points)

Draw cross-sectional profiles of a thin-oxide MOSFET (test structure 8) after each of the XI major processing steps. Include all layers and important details (such as pre-deposition layers, the non-planar Si-SiO_2 interface, isotropic etch profiles, etc.) Label each feature and indicate approximate thickness, but you need not to make the drawings to scale.

3. Layout (12 Points)

Draw top views of the same thin-oxide MOSFET after each of the four photolithography steps. These layouts should indicate proper overlaps and alignment information which you observed during processing.

4. Calculations (20 Points)

Theoretically calculate the following, based on times, temperatures, etc.

1. Thicknesses of thick (field), intermediate and gate oxides, (include orientation dependence of oxidation rate but not impurity dependence).
2. Junction depths after pre-deposition and drive-in, (assume only phosphorous doping with surface concentration limited by solid solubility).
3. Final surface concentrations of dopants.
4. Lateral diffusion under the MOSFET gates.

5. Questions (35 Points)

Answer these questions in the most concise manner possible. A few lines should suffice for each.

1. What type of photoresist do we use in the lab, and how does it work?
2. Why do we use HMDS? What happens if we forget to use it? Will it cause any problems if we wait a week after the HMDS treatment to spin photoresist?
3. Photolithography generally involves baking the wafer before spinning resist and again before exposure. What is the purpose of each of these steps? When do we skip the pre-spinning bake step?

What happens if the second bake is too hot (say 150 ° C)?

4. We do lithography steps under yellow light only. What happens if we expose the wafers to fluorescent light before development? After development? If you arrived one morning to find the "yellow" room replaced by a "red" room, would it damage your process to use it?
5. What would happen if we skipped the BHF dip after poly-Si etch? What if we skipped it before metallization?
6. What are the differences between wet and dry oxidation that lead us to use one for the gate oxide and one for the field oxide?
7. Why do we use TCA and how does it work? Why do we only introduce it into the furnace with large amounts of oxygen?
8. After each oxidation we anneal in N_2, after metallization we anneal in N_2/H_2. Could we do either of these anneals equally well in Ar? Dry O_2? A vacuum? Why or why not?
9. Before N+ deposition we clean in piranha but not in HF. Before gate oxidation we clean in both. Why the differences?
10. Why is buffered HF (5:1 NH_4F:HF) used for etching features in the oxide while 10:1 H_2:HF is used for cleaning and p-glass stripping?
11. Why do we use lift-off to define the metal pattern? What processing steps does lift-off save?
12. Why do we first use the roughing pump and then the diffusion pump when pumping down the aluminum deposition system? Why must the foreline pressure be kept below 100 milliTorr? Why must we switch from the roughing pump to the diffusion pump at 200 milliTorr?

6. Extra Credit Questions (2 Point Each)

Explain how you would *measure* the following parameters with simple, inexpensive equipment such as you might find in 218 Cory or in the Microlab. Keep your answers brief.

1. R_s ($\Omega/\square$) and ρ (Ω-cm) of a uniformly doped wafer (such as your original wafer).
   R_s ($\Omega/\square$) of a junction (such as after drive-in).
2. Could you make the second measurement on your own wafer, or would you have to process a separate test pattern?
3. Conductivity type (n or p) and N_A or N_D of a uniformly doped wafer.
4. Oxide thickness and metal thickness.
5. Junction depth and surface concentration (assume a Gaussian profile in a uniformly doped substrate).
6. Extra Extra Credit Question (up to 5 points)
   How do you expect the processing vaariations we saw this term to affect your devices?

7/11/88

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Lab Report 2

This report will summarize characterization of your test structures. The two purposes of characterization are to teach you how to use the equipment and techniques common to semiconductor structure analysis, and to compare the actual behavior of your devices with that predicted theoretically. Each group of two students will submit one joint report. Follow the procedure below.

Before you start taking measurements, study the Device Characterization outline and note that you will need a complete set of plots, as described in the assignments, for parameter extraction. Most of the plots can be done using the HP4145 Semiconductor Parameter Analyzer, which can be programmed to plot algebraic expressions. To expedite this procedure, you should mark off which plots will be done on the HP4545 and which ones by hand. You should also be familiar with the operation of the HP4145; consult the HP manual before you begin.

1. Measurements (10 pts)

You will be making three groups of measurements. Label all plots and indicate corresponding device number.

1. **Transistors**
   Using HP4145 Semiconductor Parameter Analyzer, make plots as described in the Device Characterization Outline, Assignment V, starting with the large geometry MOS transistor, test structure [11] and continuing on to MOSFETS [8], [9], [10]; to the diode [7]; and to the bipolar transistors [12a,b,c].
2. **Capacitors**
   Using the C-V test station, plot capacitance-voltage curves for all capacitors [3], [4], [5], [6a,b] and for the junction capacitance of the diode [7].
3. **Miscellaneous**
   Make the resistor and circuit measurements on the probe station equipped with curve tracer, power supplies and oscilloscope. Make optical measurements with filar eyepiece on microscope.

2. Parameter Extraction (30 pts)

From the data taken above, find the device parameters in the attached table. Show all procedures and calculations.

3. Calculations (30 pts)

Calculate the theoretical values for the MOSFET parameters. Use actual numbers in your theoretical calculations (i.e., use the measured Q_{ss} rather than the expected Q_{ss} when calculating the theoretical V_T). Combined with your earlier calculations of t_{ox}, x_j, $N_{surface}$, and lateral diffusion (from the first lab report), you should be able to determine how well your process worked.

4. Summary (30 pts)

1. (6 pts)
   Draw up a complete set of tables of all measured and/or calculated values;

   - Table I: Line Width Measurements
   - Table II: Resistors
   - Table III: Capacitors
   - Table IV: Diode and Bipolar Transistors
   - Table V: Mosfets
   - Table VI: Circuits

   Show circuit representations requested in each assignment. For clarity, follow the sequence of the assignments.

2. (12 pts)
   Discuss your results. Are the measured values significantly different from what you calculated? Why are the thresholds off? Are they off? Analyze what you have done in the lab. Presentation should be clean and readable.

3. (12 pts)
   Use SUPREM to simulate the dopant profile under the gate, in the S/D area and in the field. Include printouts in your report. Discuss the reasons why SUPREM results are different from your calculations.

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Summary of MOSFET Parameters

Parameter	Measured / Extracted	Theoretical	SUPREM
$t_{ox(Gate)}$			
$C'_{ox(Gate)}$			
x_d			
N_D			
L_D			
C_{FB}			
Q_{ss} (Q_f)			
V_T ($\frac{100}{100}$)			
γ			
N_A			
μ_{eff}			
μ_o			
Θ			
n			
ΔL (in linear region)			
ΔW (in linear region)			
V_T and k for L=2 µm 4 µm 7 µm 10 µm W=10 µm 15 µm 20 µm			
λ for L=2 µm 4 µm 7 µm 10 µm			
Slope			
$V_{T(Field)}$			

Appendix IV

EECS 143
Processing and Design of Integrated Circuits

College of Engineering
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley

Device Characterization

Textbooks

R. S. Muller, T.I. Kamins, *Device Electronics for Integrated Circuits*, Wiley, New York, second ed. 1987.

D. A. Hodges, H. G. Jackson, *Analysis and Design of Digital Integrated Circuits*, McGraw-Hill, New York, second ed. 1988.

I. Line Width Measurements

Test Structure 1 On Layout

The ladder structure has lines of varying width starting at 2 μm, increasing in 1 μm increments to 8 μm. Cross rails are 10 μm.

Assignment I.

Measure line widths with filar eyepiece after photoresist development at each level and at the end of processing. Tabulate measurements.

II. Resistors

Test Structures 2a,b

(a) The n+ diffused resistor is formed during source/drain diffusion. Its resistance is measured by the 4-point probe method: current from a constant current source is passed through the outer probes and the voltage is measured between the inner probes. The resistor value is:

$$R_{diff} = \frac{V}{I} = \frac{L}{W} R_s$$

where R_s is the sheet resistance, L is the length between inner probes and W is the line width. Resistivity in Ω-cm can be calculated if the diffusion depth is known:

$$\rho = R_s x_j$$

(b) The poly-Si resistor is more susceptible to line width variations than the diffused resistor because of the wet etching of poly Si. Since the poly-Si lines are also used as interconnects, the poly resistivity (ρ) is of great importance in circuit design.

$$\rho_{poly} = R_s t_{poly}$$

Test Structures 2c,d

The contact chain is basically a resistor made up of n+ diffused (n+ doped poly-Si) and aluminum sections. The resistance of the aluminum sections is very low compared to the n+ sections and can be neglected. However, contact resistance cannot; thus the value of the total resistance is:

$$R_{total} = 7R_{block}$$

$$R_{block} = \eta R_s + 2R_c$$

where R_c = contact resistance/contact hole and $1 < \eta < 3$. Current density is determined by the geometry of the resistor pattern. The equivalent resistance of the squares containing the contact holes is found to be 0.65 squares; thus η has a value of 2.3 for this configuration.

Assignment II.

1. Measure the value of the diffused resistor, 2a, and compare R_s with the sheet resistance measured on the control wafer after drive-in. Using the x_j value calculated in Lab Report 1, determine doping concentration and electron mobility from standard tables in Muller and Kamins.

2. Measure the line width optically and determine R_s (in Ω/□) from the measured R_{poly}, 2b. Calculate poly-Si resistivity (in Ω-cm).
3. Measure the resistance of the contact chain on both diffused, 2c, and poly-Si, 2d, structures and calculate contact resistance using R_s determined above.

III. Capacitors

There are two types of capacitors used in integrated circuits: MOS capacitors and junction capacitors.

Test Structure 3

The field (thick) oxide MOS capacitance is basically independent of applied voltage because the depletion layer in the substrate is small compared to the thickness of the oxide:

$$C = \frac{A\varepsilon_{ox}}{t_{ox}}$$

When measuring capacitances, care must be taken to account for the parasitic capacitances of the measurement set-up. Parasitic capacitance is measured by lifting the probe until it is just above the top plate of the capacitor without touching. Actual capacitance is then calculated by:

$$C_{actual} = C_{measured} - C_{parasitic}$$

Test Structure 4

The measured value of the gate oxide capacitor, as it is laid out, includes the field oxide capacitance of the contact pad and the ring around the active area:

$$C_{measured} = A_{active}\frac{\varepsilon_{ox}}{t_{gox}} + A_{pad+ring}\frac{\varepsilon_{ox}}{t_{fox}} + C_{parasitic}$$

The gate oxide capacitance varies with applied voltage. As the Si surface is depleted with increasing gate voltage, the capacitance is obtained from the series connection of the oxide capacitance (constant) and the depletion region capacitance. Since the width of the surface depletion layer depends on the bias voltage, the substrate doping and oxide quality, the C-V plot for the gate oxide capacitor can be used to measure/calculate doping concentration, flat band voltage and interface charge density Q_{SS}.

Test Structure 5

The bottom plate of the intermediate oxide capacitor is the N+ diffusion, contacted by the side pad. The oxide is grown during N+ drive-in and it is the same thickness as that over the source/drain areas of devices. Again,

$$C = C_{measured} - C_{parasitic}$$

Test Structures 6a,b

6a) Calculation of junction capacitance:

$$C_j = \frac{C_{jo}}{\left\{1 - \frac{V_a}{\phi_i}\right\}^n}$$

where ϕ_i is the built in potential, C_{jo} is the zero bias junction capacitance and n depends on the type of junction; n = 1/2 for a step junction and n = 1/3 for a linearly graded junction. From a C-V plot of V_a = -5 V to 0 V, C_{jo} can be found.

6b) The long periphery junction capacitor illustrates the effects of junction side wall capacitance:

$$C_{6a} = P_{6a}C_{j_{sidewall}} + A_{6a}C_{j_{bottom}} + C_{parasitic}$$

$$C_{6b} = P_{6b}C_{j_{sidewall}} + A_{6b}C_{j_{bottom}} + C_{parasitic}$$

where P_{6a} and P_{6b} are the lengths of the respective perimeters.

Assignment III.

1. Measure field oxide capacitance at -5 V and calculate field oxide thickness. Plot C-V from -10 V to +10 V to see any effect of bias. Explain.
2. Measure gate oxide capacitance at -5 V and determine gate oxide thickness and C' (capacitance/unit area). From the C-V plot (-5 V to +5 V) determine minimum capacitance and calculate maximum depletion width and substrate doping concentration. Calculate the Debye length (L_D), flat band capacitance(C_{FB}), flat band voltage (V_{FB}) and interface fixed charge density ($Q_{ss} = Q_f$: new nomenclature).
3. Determine intermediate oxide thickness from the capacitance measurement at -5 V. Plot C-V from -5 to 0 and calculate diffusion doping concentration.
4. Determine the value of *n* from the C-V curve and plot log C_j (for C_{6a}) vs. log ({1 - V} over {ϕ_i}).
5. Measuring the capacitances C_{6a}, C_{6b}, and $C_{parasitic}$, calculate junction side wall capacitance, C_{jsw}, in pF/μm and junction bottom capacitance in pF/ μm^2.
6. Plot junction capacitance of diode (test structure [7]) and determine C_{jo}.

IV. Diode and Bipolar Transistors

Test Structure [7] - Diode

The + diffusion forms a diode in the p substrate, which can be contacted through the back of the wafer. (There should be no oxide on the back.) In the forward biased mode, the anode (p) is positive with respect to the cathode (n+). Forward turn-on voltage (V_F) can be estimated from the I_D vs. V_D characteristic; the series resistance, r_s, is the slope of the I_D vs. V_D curve on the high (100 mA) current scale.

Assignment IV - A.

1. Plot the I-V characteristic; read off V_F, reverse breakdown voltage BV_R, and the series resistance r_s.
2. Draw the circuit representation of a diode (including r_s), indicate current direction and voltage polarities.

Test Structure [12a,b,c] - Lateral Bipolar Transistors

The collector and emitter regions of the lateral npn transistors are formed during the n+ source/drain diffusion. The p-type base is the substrate. As drawn, base widths are 5 μm (a), 6 μm (b), and 7 μm (c).

The npn bipolar transistor is normally used as an amplifying device in a common emitter (or grounded emitter) configuration. The collector-to-base current gain, beta, β, (or h_{FE}) is given by

$$\beta = \frac{I_C}{I_B}$$

which can be read off directly from the I_C vs. V_{CE} (with I_B increasing in steps) family of curves.

Assignment IV - B.

1. Plot I_C vs. V_{CE} family of curves for each transistor, determine BV_{CE} and β.
2. Draw the common emitter circuit configuration of the BJT; indicate current directions and voltage polarities.

V. MOSFETs

Test Structures 8-11

These are poly-Si gate, enhancement-mode, n-channel field effect transistors of varying gate lengths and widths. They will be used to completely characterize the process and to extract important parameters for circuit design. A summary of intrinsic device equations (excluding the effects of drain/source series resistances) relevant to this exercise is included in the following:

Threshold voltage:

$$V_T = V_{T0} + \gamma\sqrt{(V_{BS} + 0.7)}$$

$$\gamma = \frac{\sqrt{2\varepsilon_{Si} q N_A}}{C'_{ox}}$$

γ is the body-bias coefficient.

Linear region ($V_{DS} \rightarrow 0$, i.e. $V_{DS} = 50mV$) :

$$I_D = \frac{W_{eff}}{L_{eff}} \mu_{eff} C'_{ox} (V_G - V_T) V_{DS}$$

$$\mu_{eff} = \frac{\mu_0}{1 + \Theta (V_G - V_T)}$$

where Θ is the mobility gate-field degradation coefficient.

Saturation region ($V_{DS} > V_{DSAT}$) :

$$I_D = I_{DSAT} (1 + \lambda V_{DS})$$

where λ is the channel-length modulation parameter;

$$I_{DSAT} = \frac{k}{2} (V_G - V_T)^2$$

where k is the device transconductance parameter and

$$k = \frac{W_{eff}}{L_{eff}} \mu_{effsat} C_{ox}$$

$$k' = u_{effsat} C_{ox}$$

Subthreshold region ($V_G < V_T$) :

$$I_D = I_{D0} \exp\left[\frac{q(V_G - V_T)}{nkT}\right]$$

$n \geq 1$ is the subthreshold slope ideality factor.

Assignment V.

A. Large-geometry transistor, test structure [11]

1. Plot I_D vs. V_{DS}, V_G = 0-7V (1V steps) to show current-voltage characteristics of MOSFET.
2. Plot I_D vs. V_G at V_{DS} = 50 mV for V_{BS} = 0, -1, -2, and -3 V. Determine $V_T(V_{BS})$.
3. From 1 and 2, plot $V_T(V_{BS})$ vs. $\sqrt{(V_{BS} + 0.7)}$ and determine γ and N_A.
4. Plot $\dfrac{I_D}{\frac{W}{L} C'_{ox} (V_G - V_T) V_D}$ vs. V_G at V_{DS} = 50mV, V_{BS} = 0V.

   Determine $\mu_{eff}(V_G)$ for $V_G > V_T$.
5. Plot $\dfrac{1}{\mu_{eff}}$ vs. $(V_G - V_T)$ and determine μ_0 and Θ.
6. Plot log (I_D) vs. V_G at V_{DS} = 50mV and V_B = 0V and determine *n*.

B. Other transistors, test structures [8,9]

1. Plot I_D vs. V_{DS}, V_G = 0-7V (1V steps) to show I-V characteristics of MOSFETs, for
   a) L = 2, 4, 7, 10, 20 μm
      W = 15 μm
   b) W = 10, 15, 20 μm
      L = 20 μm
2. Plot I_D vs. V_G at V_{DS} = 50mV at V_{DS} = 5V, and at V_{BS} = 0V, and determine V_T for each transistor:
   a) in set 8;
   b) in set 9.
3. Determine source/drain resistance and effective channel length (L_{eff}) as follows:

   For each device in set 8, plot $R_{measured} = \dfrac{V_D}{I_D}$ vs. V_G, V_D = 50mV and 5 V on the same plot.

$$L_{drawn} = 2, 4, 7, 10\ \mu m$$

$$R_m = R_{external} + R_{channel}$$

$$R_m = R_{external} + \frac{(L - \Delta L)}{W \mu_{eff} C_o (V_G - V_T)}$$

   Take points from the R_m vs. V_G curves and plot R_m vs. L_{drawn}, one line for each $(V_{GS} - V_T) = 2, 6, 8, 10$ V. These lines should intersect in one point, of which the abscissa = ΔL and the ordinate = $R_{external} = R_{S/D} = R_S + R_D$.

$$L_{eff} = L_{drawn} - \Delta L$$

4. For the channel narrowing effect, ΔW, plot for each device in set 9 $R_m = \dfrac{V_D}{I_D}$ vs.

V_G, V_D = 50mV and 5 V, V_{BS} = 0, on the same plot.

Plot $\frac{1}{R}$ vs. W_{drawn} for $(V_{GS} - V_T) = 2$ V only. Intersection with X axis = Δ W.

Effective channel width:

$$W_{eff} = W_{drawn} - \Delta W$$

5. From 2a) and 3 above, plot V_T vs. L_{eff} at V_D = 50mV;
   and from 2b) and 4 above, plot V_T vs. W_{eff} at V_D = 50 mV
   to observe short-channel and narrow-width effects.
6. Plot $\sqrt{I_D}$ vs. V_G at V_{DS} = 5V and V_{BS} = 0V, and determine V_T and k for each transistor:
   a) in set 8, and
   b) in set 9.
7. Plot I_D vs. V_{DS} at $(V_G - V_T) = 1$V and determine λ by using two values of I_{DSAT} for each device in set 8.
8. From 7 above, plot $\log(\frac{1}{\lambda})$ vs. $\log(L_{eff})$ and determine the slope of the line. (It should be close to -1.)

C. Field oxide MOSFET, test structure 10

The field oxide MOSFET is used to determine the field threshold voltage. A high $V_{Tfield} > V_{DD}$ is needed to ensure proper isolation of the devices.

1. Plot I_D vs. V_{DS} to show I-V characteristics.
2. Plot I_D vs. V_G at V_D = 50mV and V_{BS} = 0, -1, -2, -3 V. Determine field threshold voltage as function of V_{BS}.

VI. Circuits

Test Structure 13

The nmos inverter has a saturated enhancement load. The inverting device has a $\frac{W}{L} = \frac{40}{5}$ and the load device has $\frac{W}{L} = \frac{5}{10}$.

Test Structure 14

The two-input nmos NOR gate is formed by paralleling two inverters. The load is again a saturated enhancement mode transistor.

Test Structure 15

This is a 21-stage ring oscillator; the inverters are of the same size as test structure 13. The two buffers are of L = 5 μm and W = 60 μm and 80 μm. The ring oscillator circuit is used to measure the average propagation delay time, τ_d, of a logic gate. The output is connected to the vertical input of an oscilloscope on which the period (T) of the signal is observed. (V_{DD} = 5V)

$$T = 2n\tau_d$$

Assignment VI.

A. Inverter

1. Plot the voltage transfer characteristics (VTC) for $V_{DD} = 5$ V.
2. Determine V_{OH}, V_{OL}, V_{IH}, V_{IL}, unity gain point ($V_{in} = V_o$) and logic swing.
3. Calculate noise margins, NH_H, NM_L.
4. Construct and check truth table.
5. Draw the inverter circuit (indicate W/L of devices) and logic symbol.
6. Draw layout of inverter.

B. NOR Gate

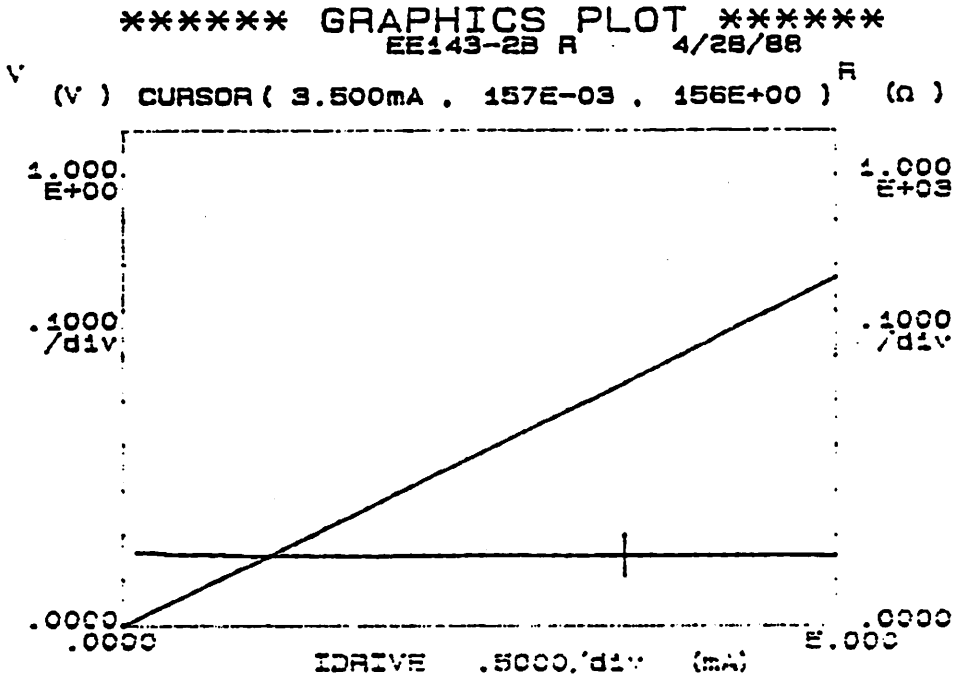
1. Plot VTC for $V_{DD} = 5$ V.
2. Determine V_{OH}, V_{OL}, V_{IH}, V_{IL}, unity gain point ($V_{in} = V_o$) and logic swing.
3. Calculate noise margins, NH_H, NM_L.
4. Construct and check truth table.
5. Draw the inverter circuit (indicate W/L of devices) and logic symbol.
6. Draw layout of inverter.

C. Ring Oscillator

1. Measure propagation delay, τ_d, of one stage.
2. Draw a partial circuit and logic diagram of the ring oscillator. Include each end, skip most of the intermediate stages; label transistor W/L ratios.

P. K. Ko
K. Voros
7/11/88

Appendix V

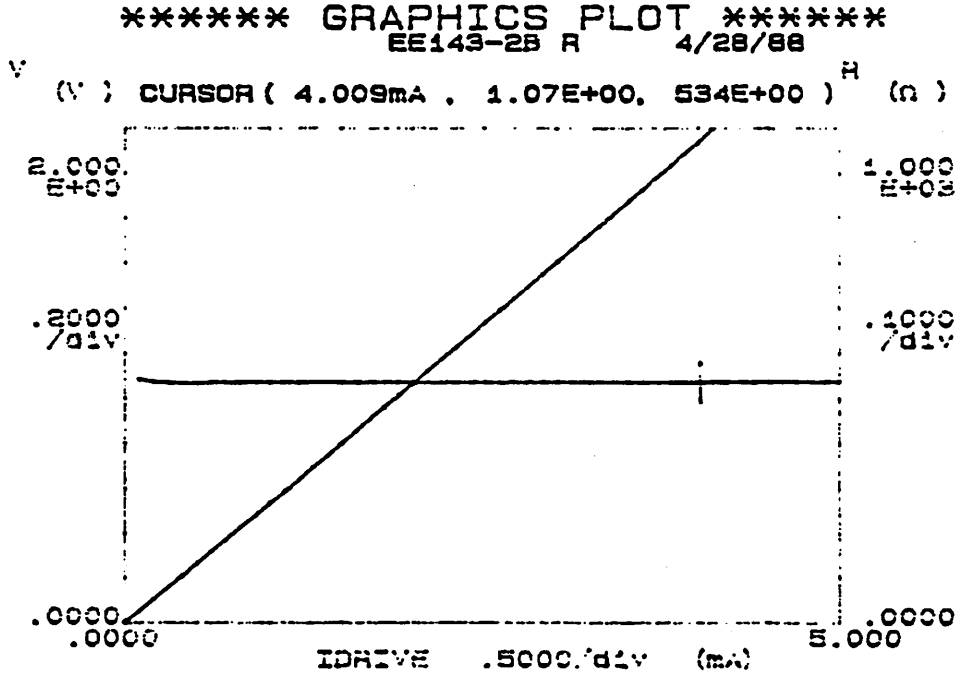


Variable1:
IDRIVE-Ch1
Linear sweep
Start .000 A
Stop 5.000mA
Step 100.0uA

Constants:
I2 -Ch2 10.00pA
I3 -Ch3 10.00pA
V4 -Ch4 .0000V

Figure 1.

Four point probe measurement of diffused resistor

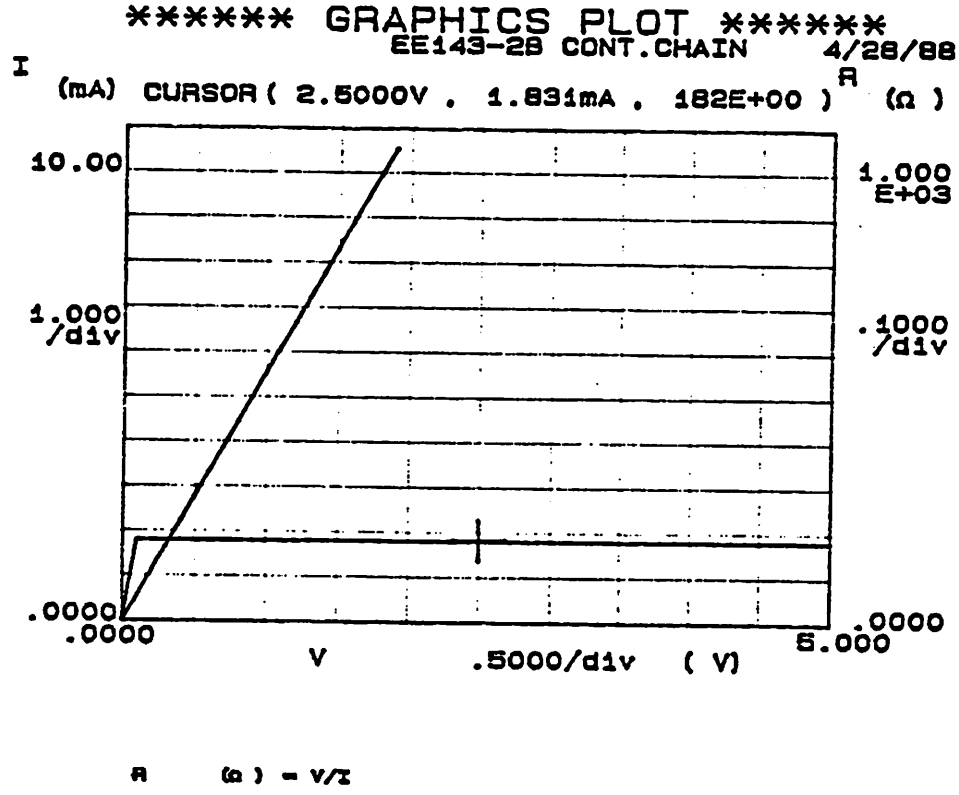


Variable1:
IDRIVE-Ch1
Linear sweep
Start .000 A
Stop 5.000mA
Step 100.0uA

Constants:
I2 -Ch2 10.00pA
I3 -Ch3 10.00pA
V4 -Ch4 .0000V

Figure 2.

Four point probe measurement of polysilicon resistor

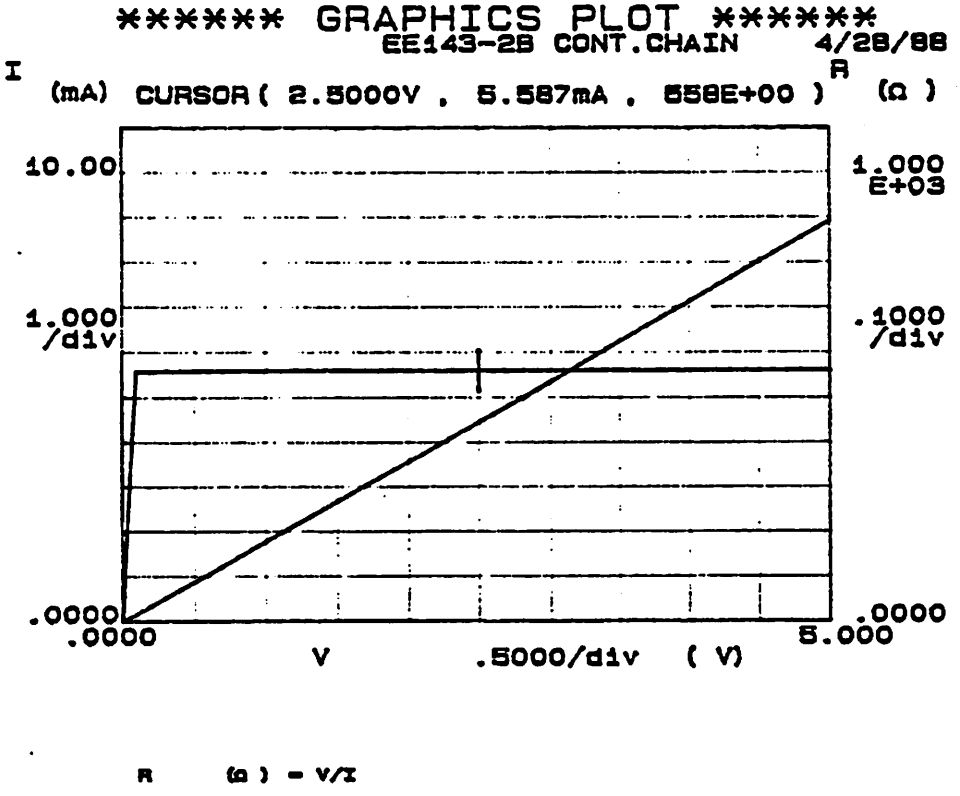



```
Variable:
 V      -Ch1
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .1000V

Constants:
 Vi     -Ch4    .0000V
```

Figure 3.

Resistance measurement of diffused contact chain




```
Variable:
 V      -Ch1
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .1000V

Constants:
 Vi     -Ch4    .0000V
```

Figure 4.

Resistance measurement of polysilicon contact chain

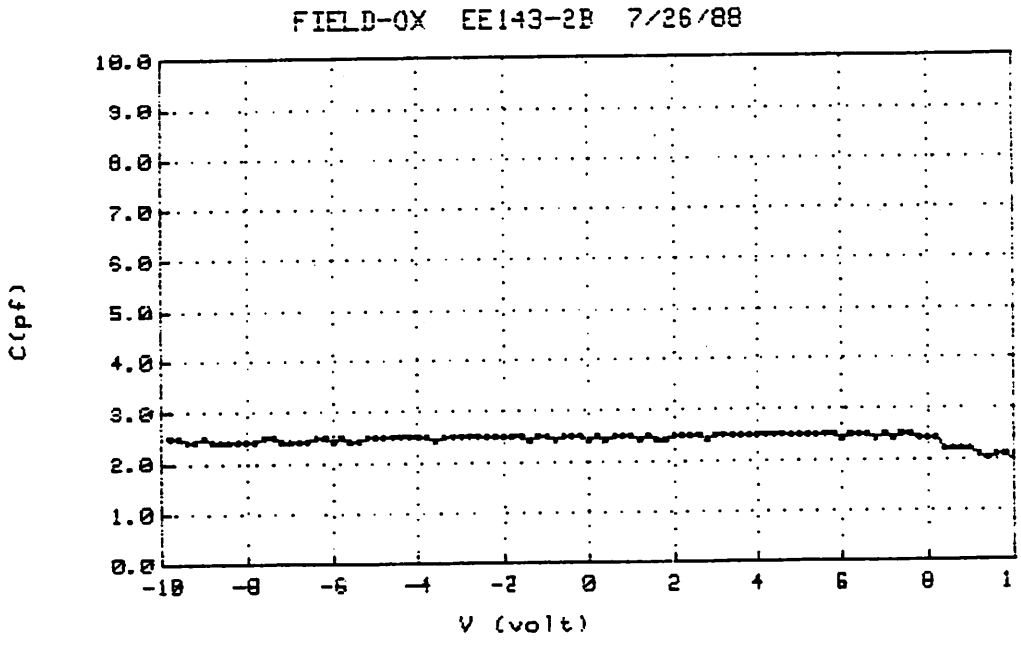


Figure 5.

C-V characteristic of field oxide capacitor

t_{fox} = 5520 Å

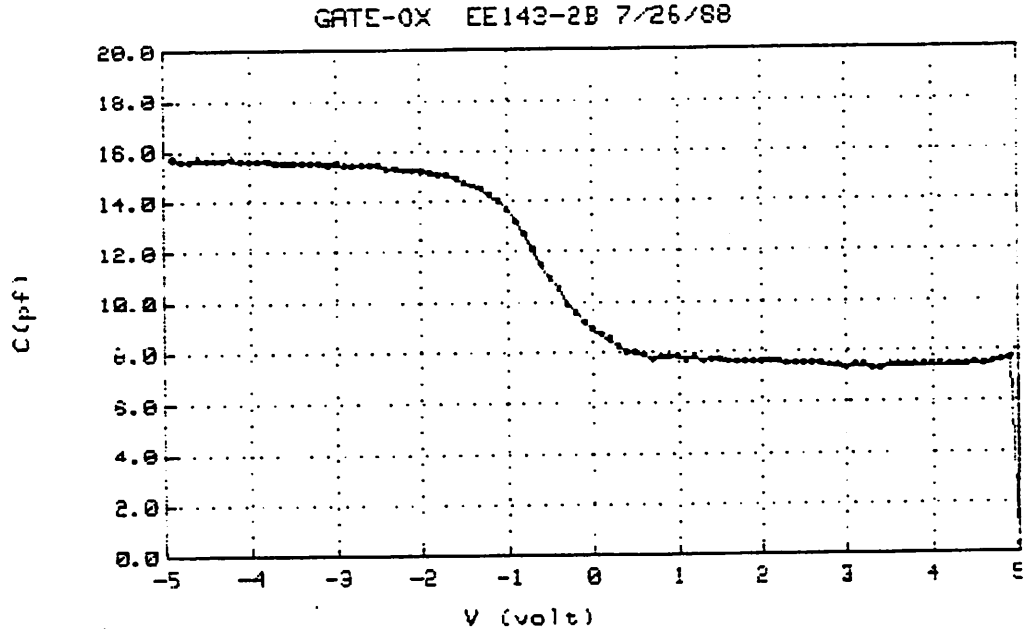


Figure 6.

C-V characteristic of gate oxide capacitor

t_{gox} = 890 Å

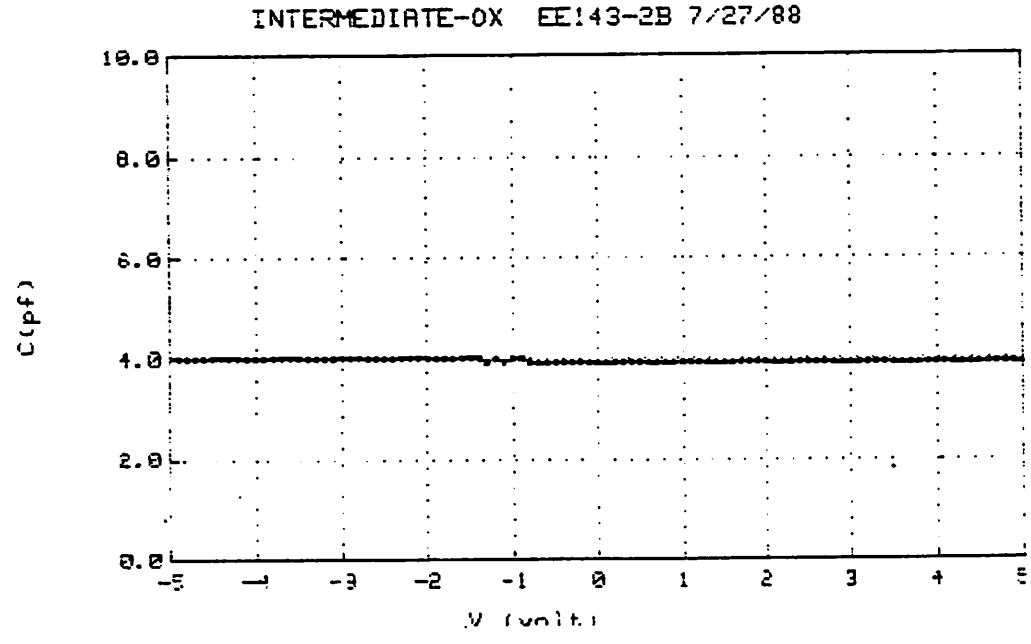


Figure 7.

C-V characteristic of intermediate oxide capacitor

t_{iox} = 3450 Å

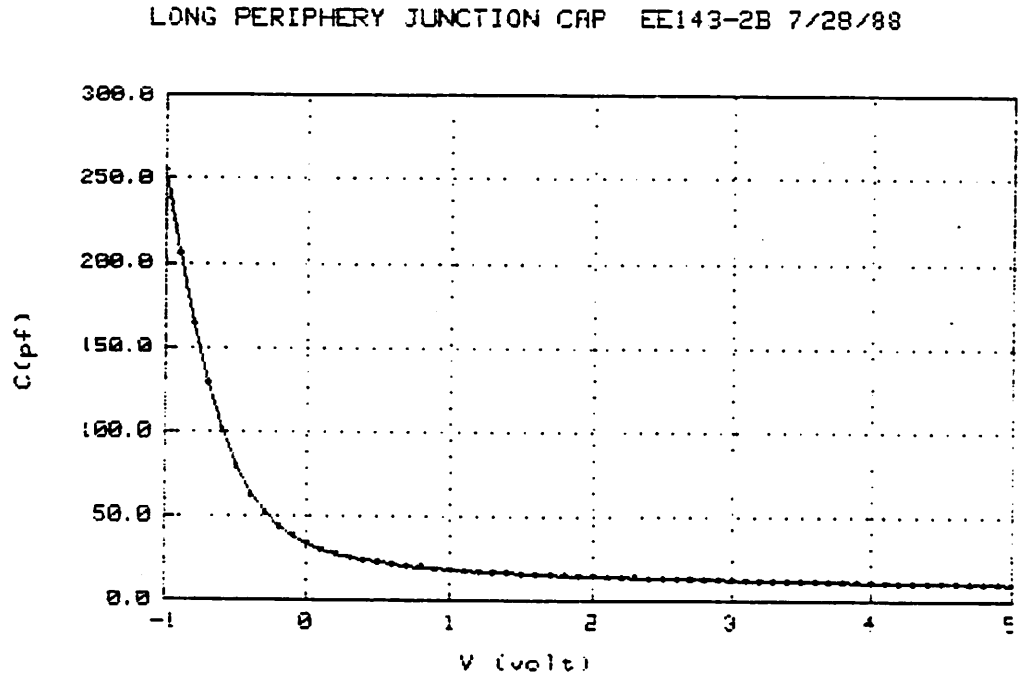


Figure 8.

C-V characteristic of long periphery junction capacitor

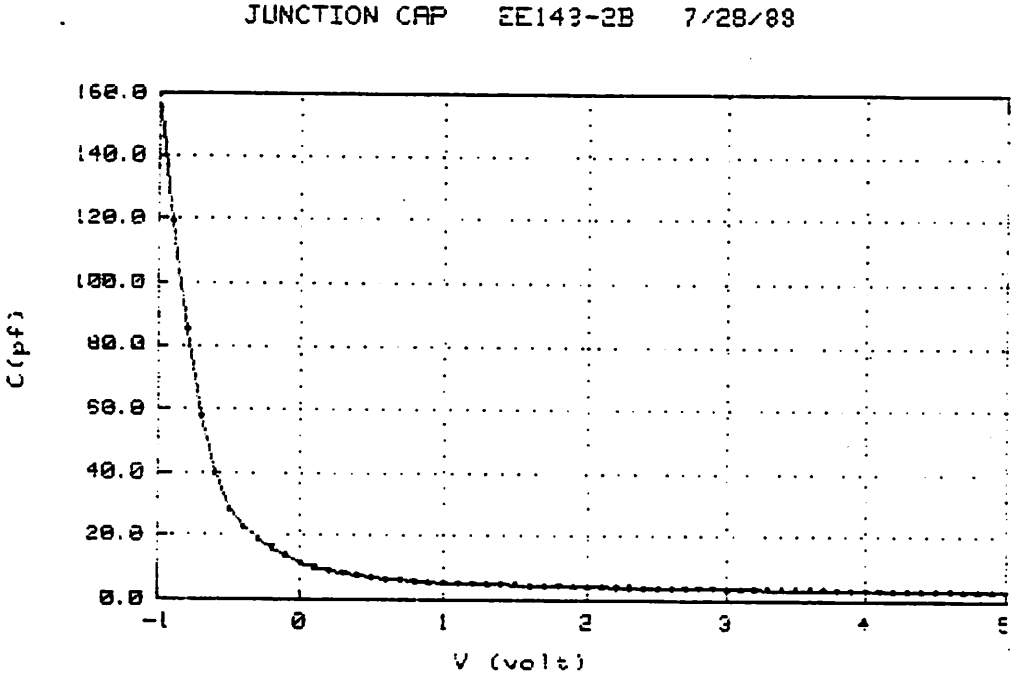


Figure 9.

C-V characteristic of junction capacitor

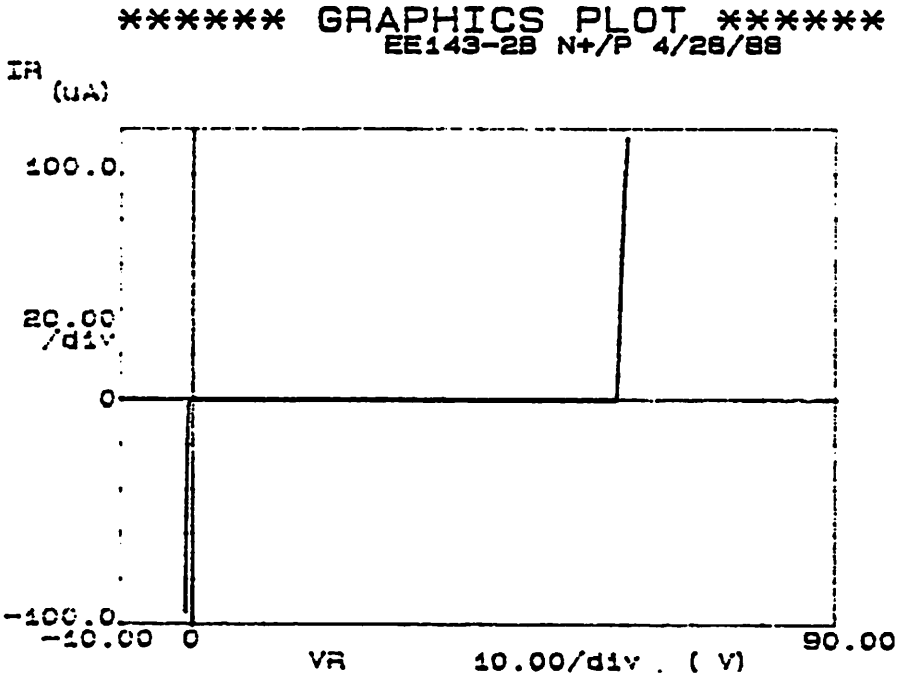
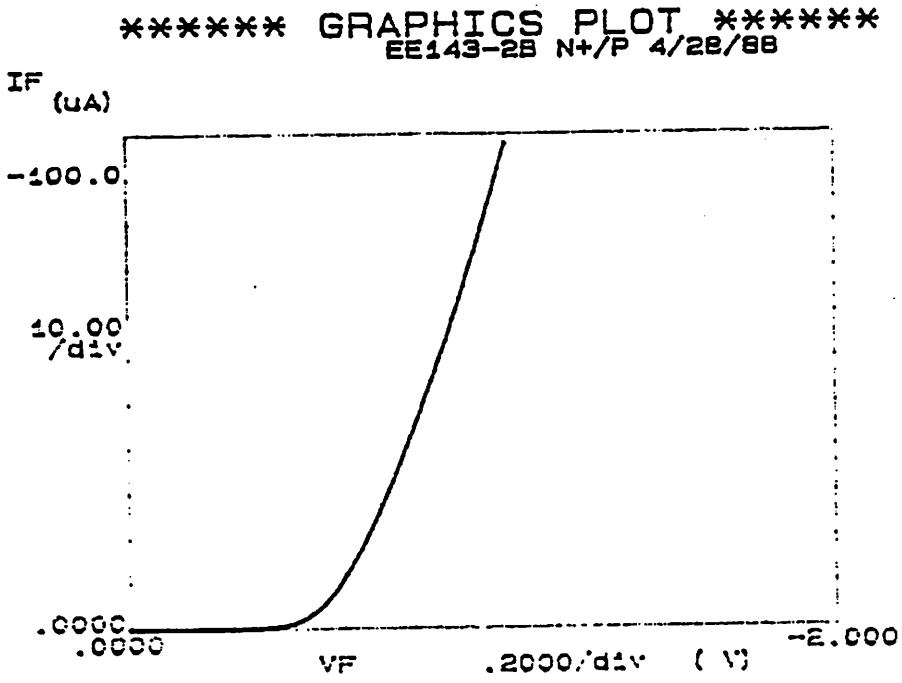


Figure 10.

I-V characteristic of N+/P diode

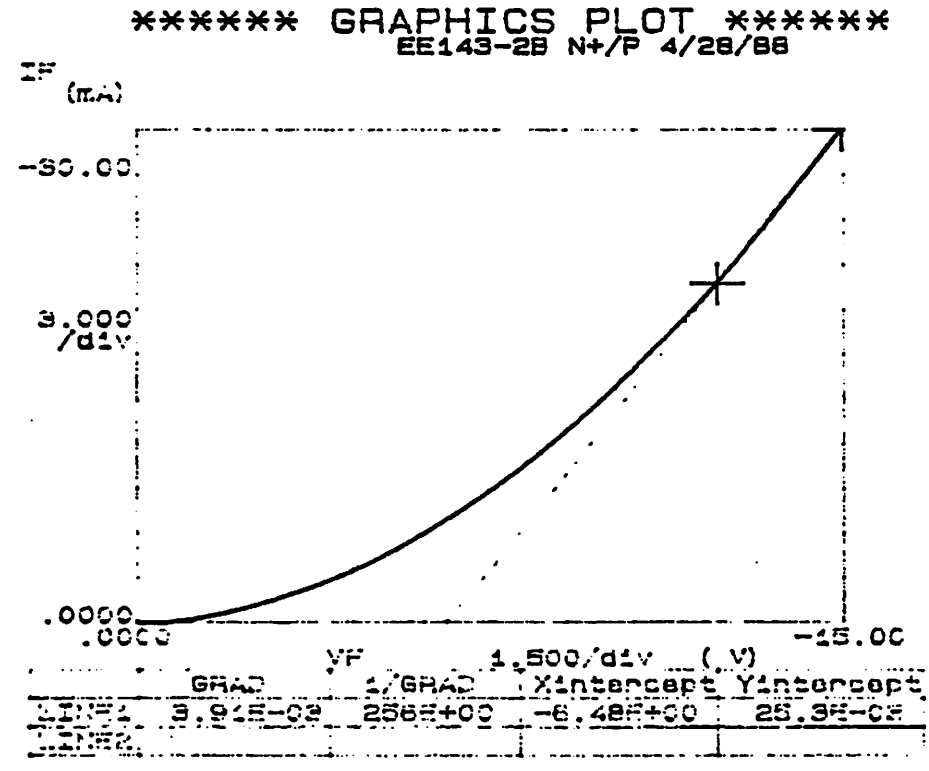


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -2.0000V
Step -.0100V

Constants:
VSUB -Ch3 .0000V

Figure 11.

Forward biased I-V characteristic of N+/P diode



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -15.000V
Step -.0500V

Constants:
VSUB -Ch3 .0000V

Figure 12.

High current forward biased I-V characteristic of N+/P diode to determine series resistance, r_s

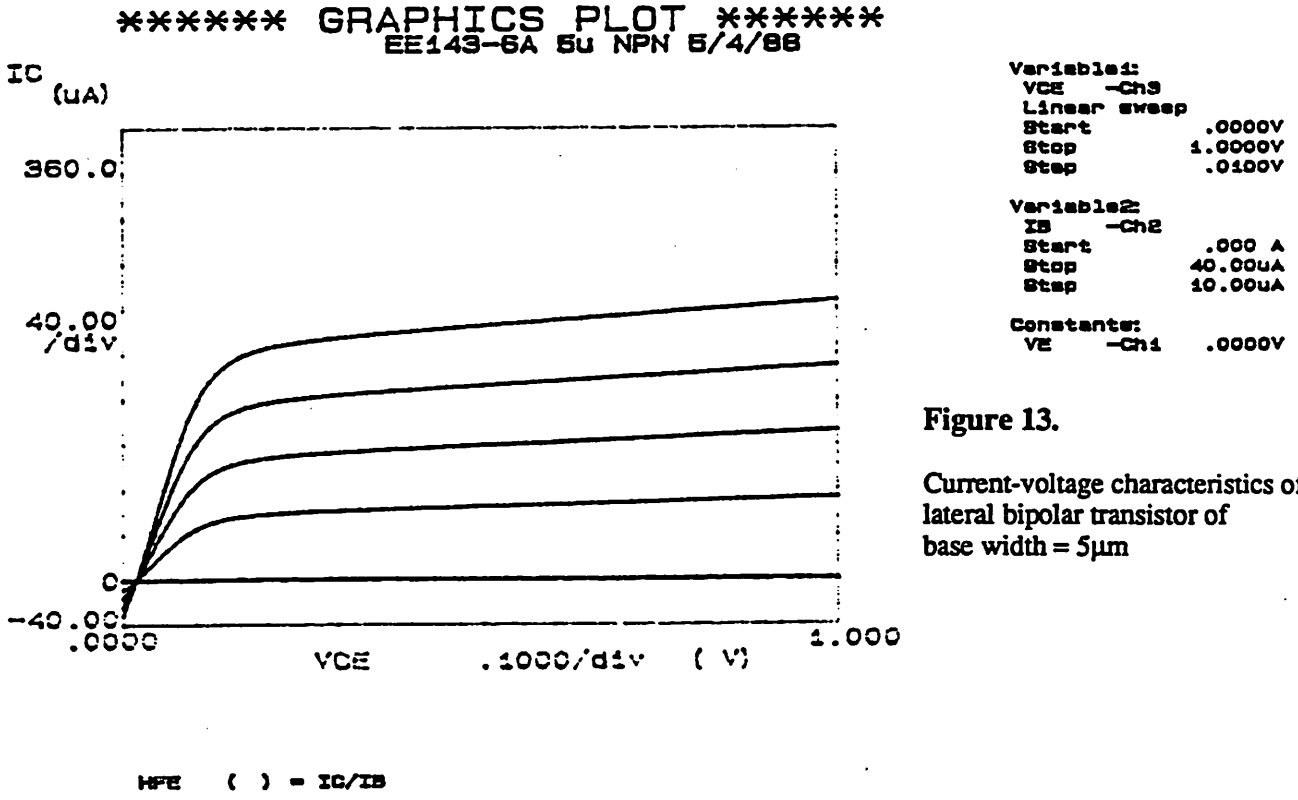


Figure 13.

Current-voltage characteristics of lateral bipolar transistor of base width = 5μm

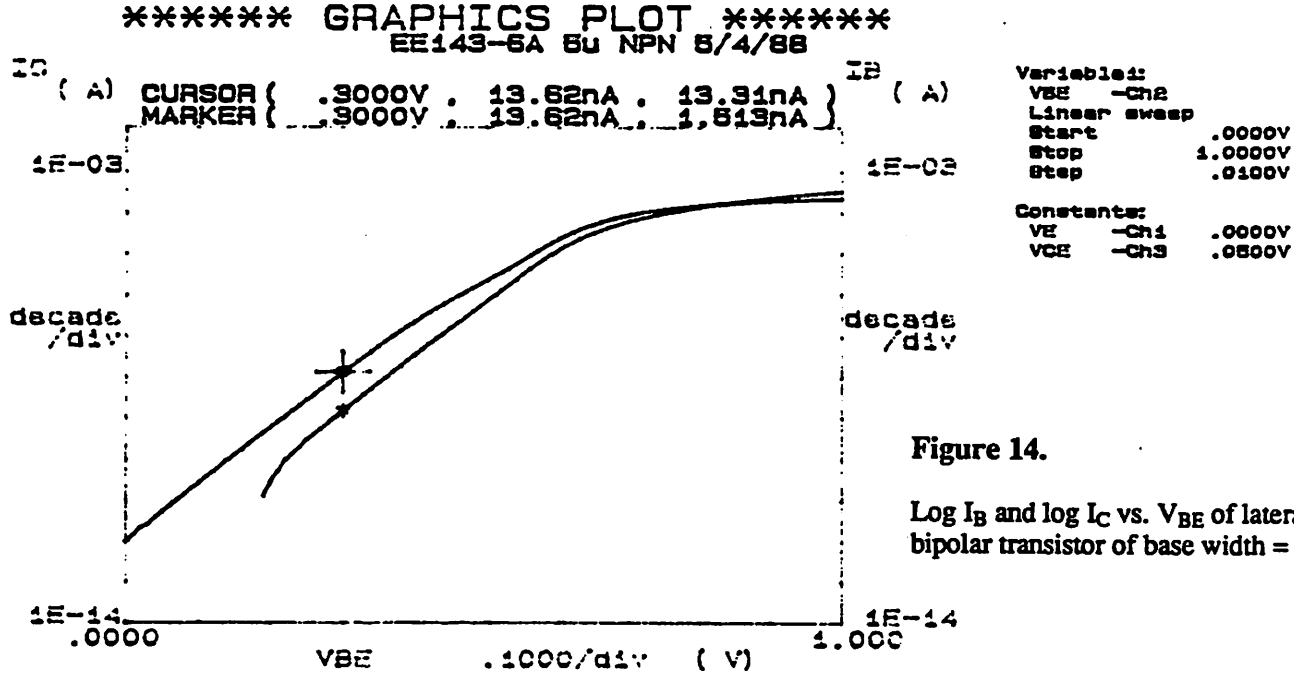


Figure 14.

Log I_B and log I_C vs. V_{BE} of lateral bipolar transistor of base width = 5μm

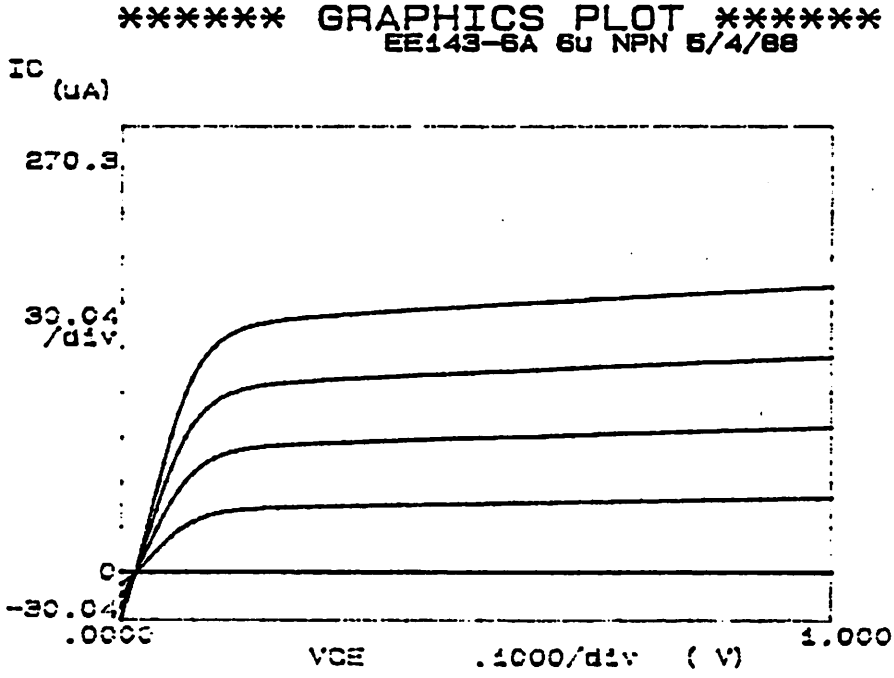


Figure 15.

Current-voltage characteristics of lateral bipolar transistor of base width = 6μm

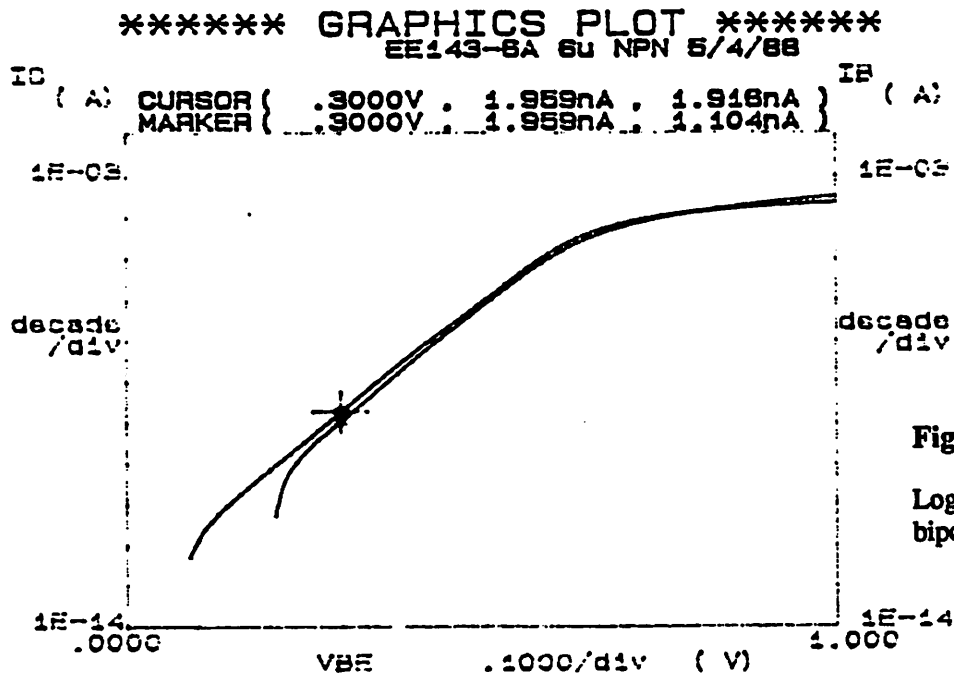


Figure 16.

Log I_B and log I_C vs. V_{BE} of lateral bipolar transistor of base width = 6μm

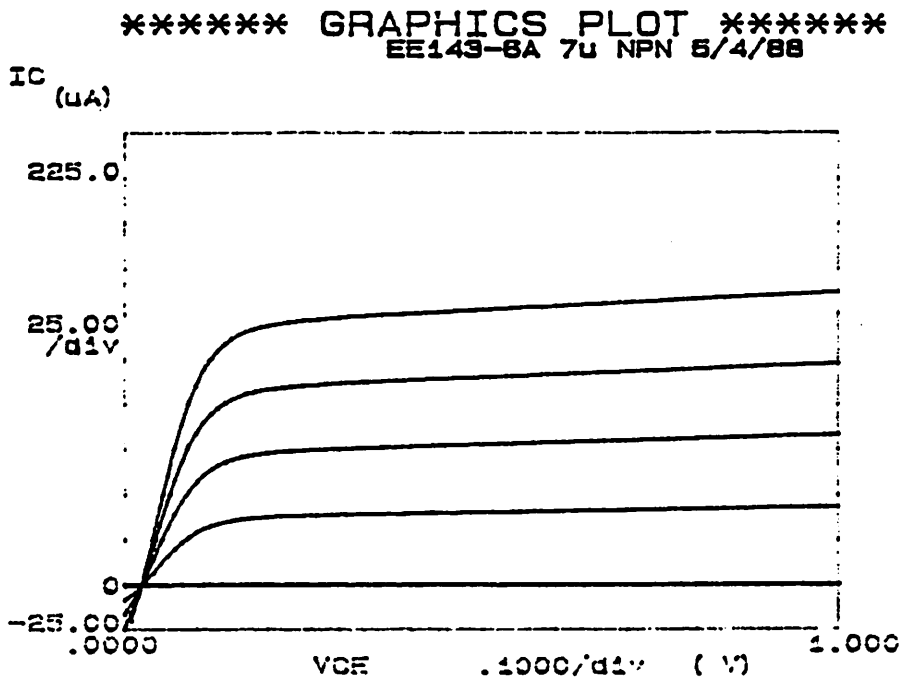


Figure 17.

Current-voltage characteristics of lateral bipolar transistor of base width = 7μm

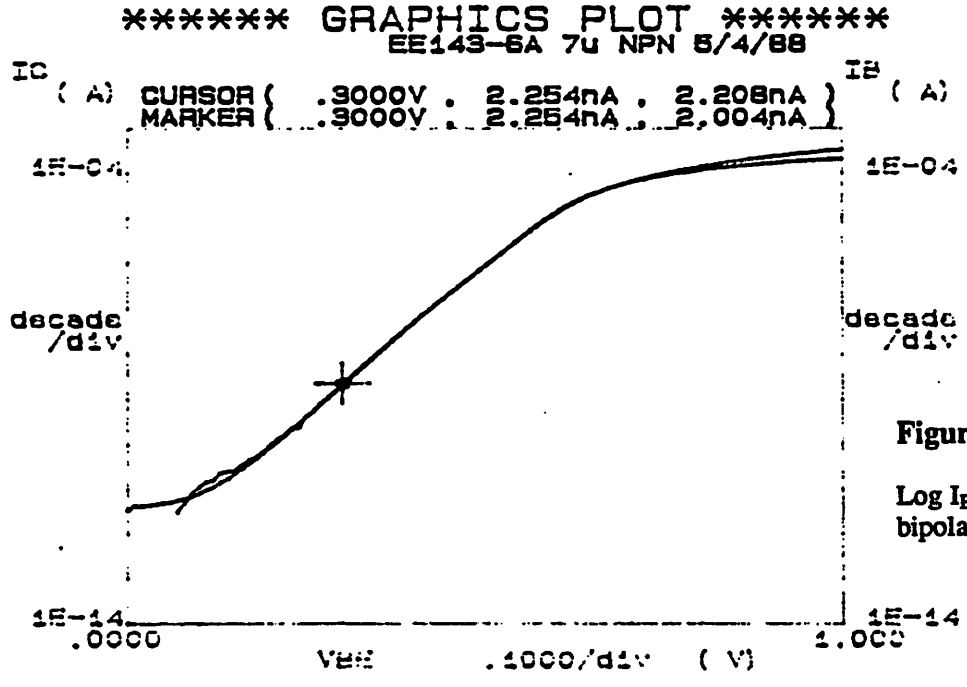
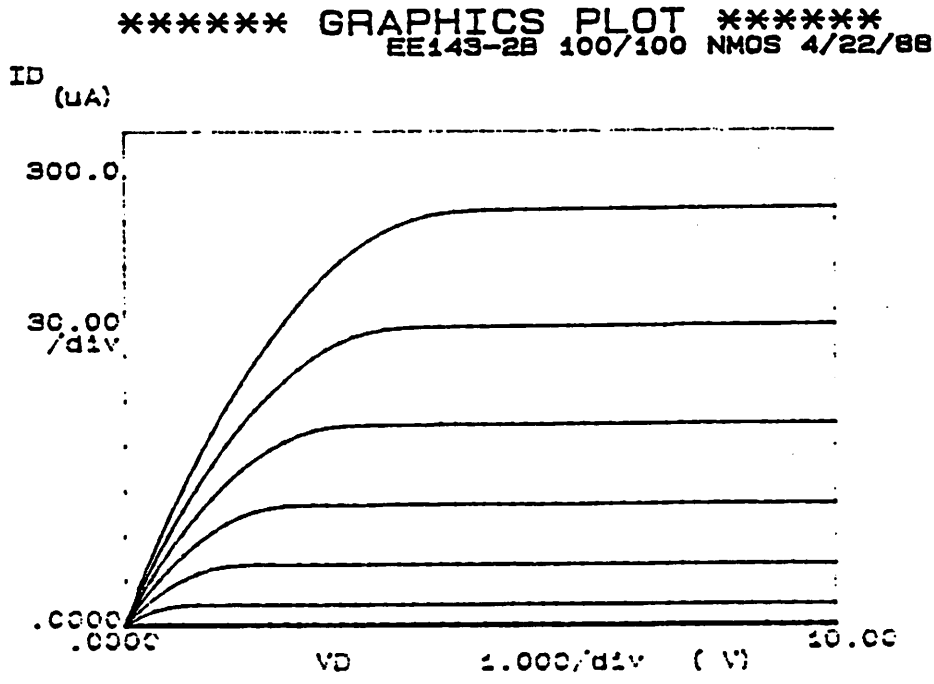


Figure 18.

Log I_B and log I_C vs. V_{BE} of lateral bipolar transistor of base width = 7μm



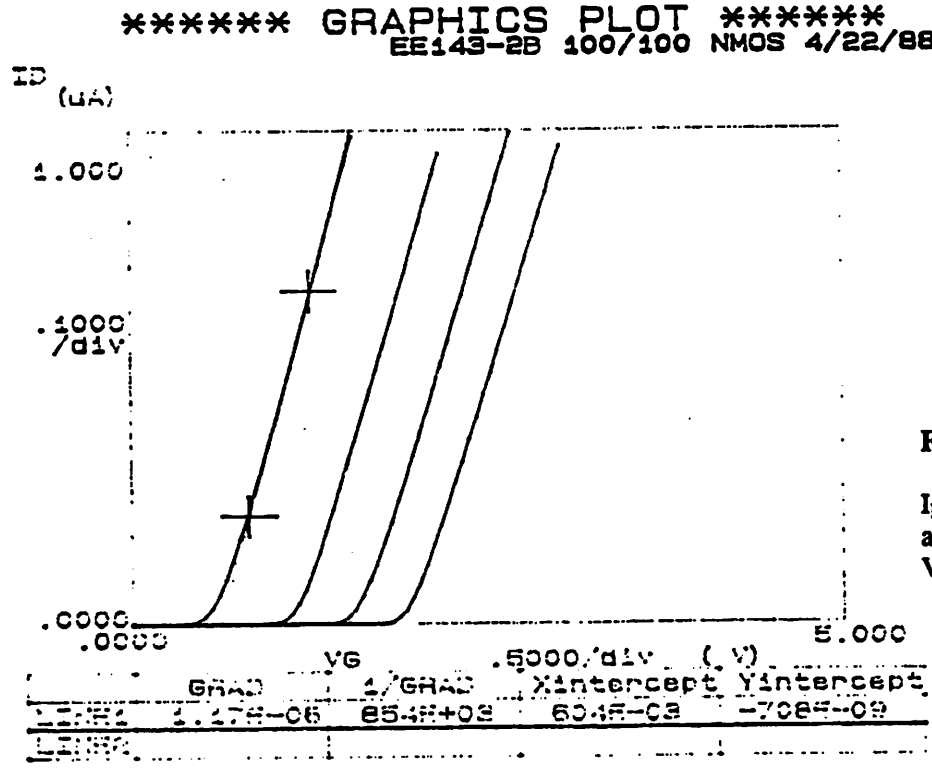

```
Variable1:
 VD     -Ch1
 Linear sweep
 Start          .0000V
 Stop         10.000V
 Step           .2000V

Variable2:
 VG     -Ch4
 Start          .0000V
 Stop          7.0000V
 Step          1.0000V

Constants:
 VS     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 19.

I_D - V_D characteristics of large ($\frac{W}{L} = \frac{100}{100}$) NMOS transistor




```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VSUB   -Ch3
 Start          .0000V
 Stop         -3.0000V
 Step         -1.0000V

Constants:
 VD     -Ch1    .0500V
 VS     -Ch2    .0000V
```

Figure 20.

I_D vs. V_G of large NMOS transistor at varying substrate bias, $V_D = 50mV$

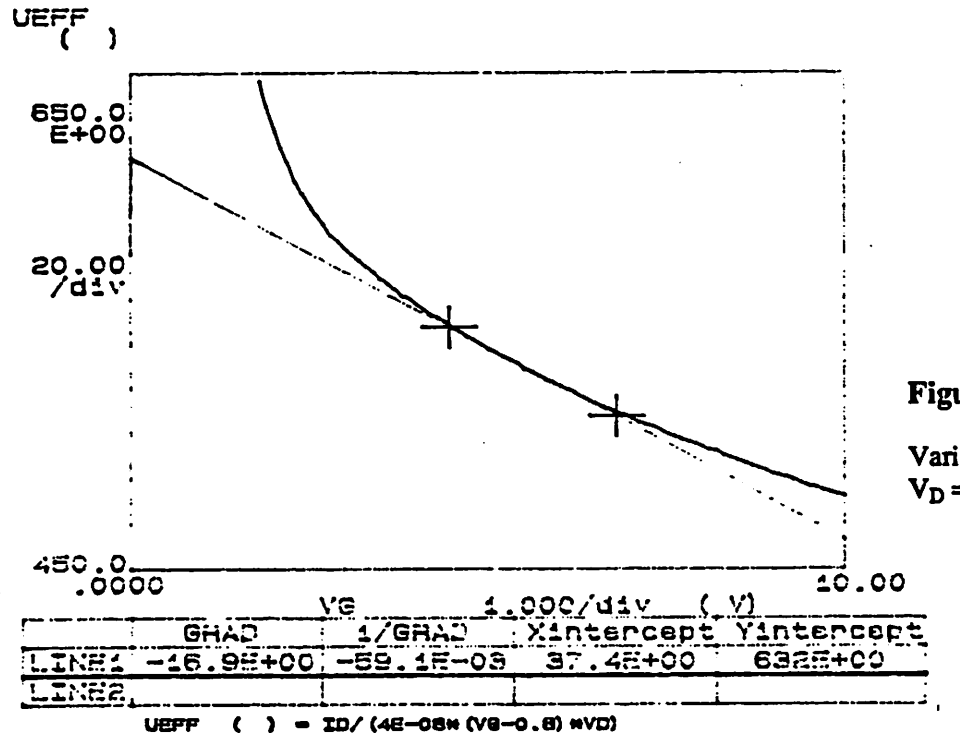


Figure 21.

Variation of μ_{eff} with gate voltage, $V_D = 50$ mV, of large NMOS transistor

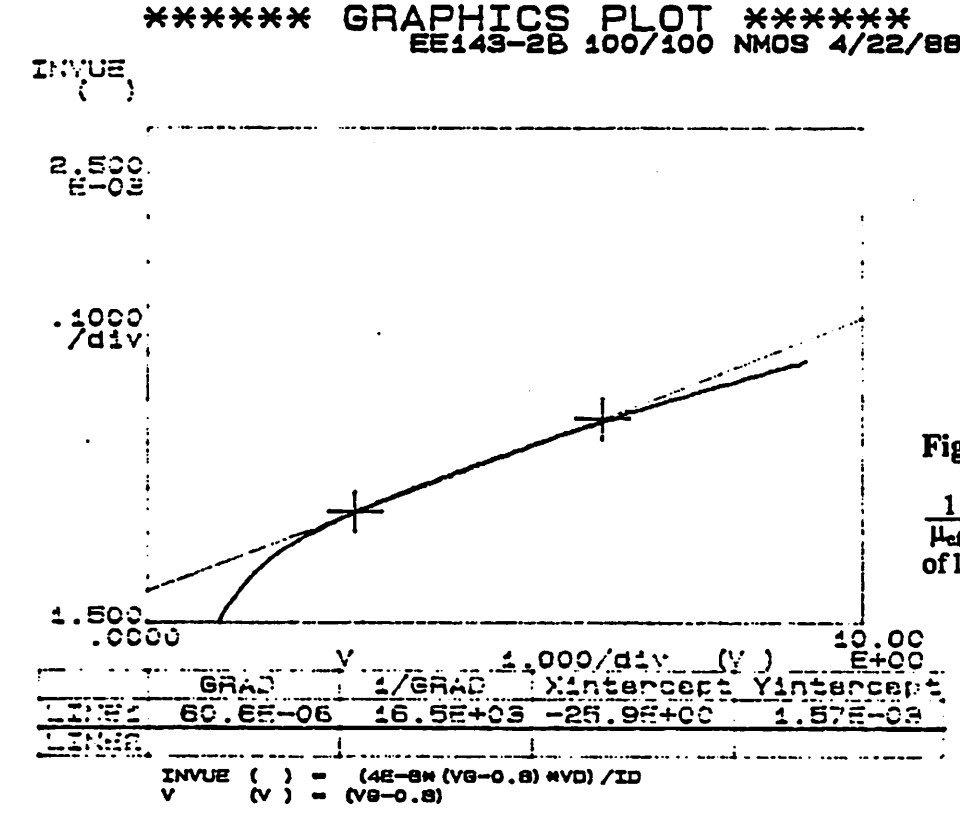
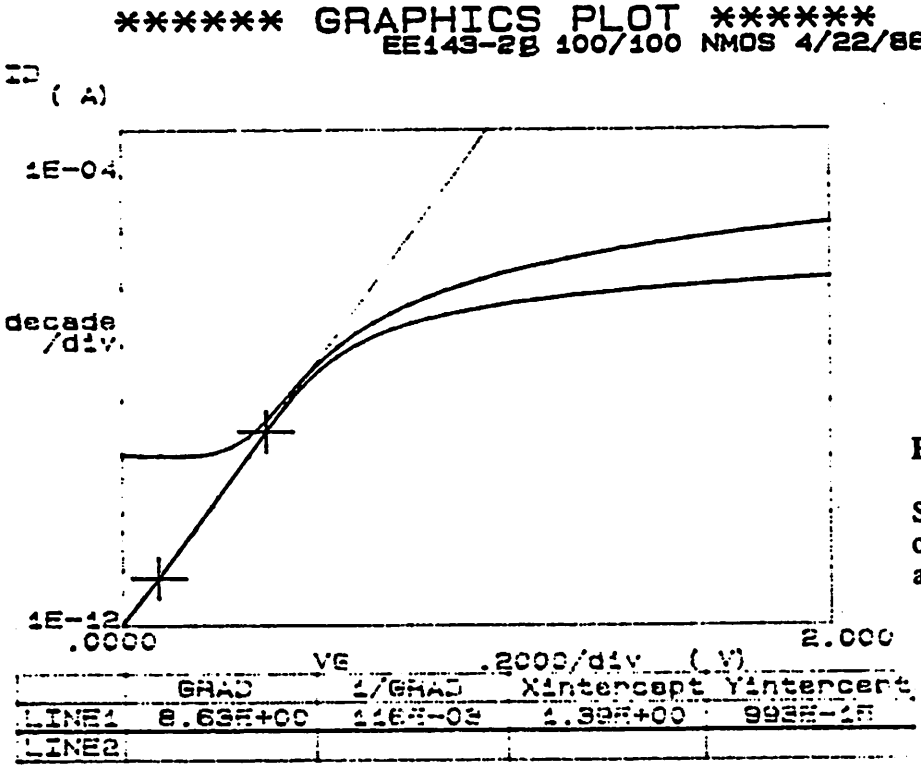


Figure 22.

$\frac{1}{\mu_{eff}}$ vs. $(V_G - V_T)$ at $V_D = 50$mV of large NMOS transistor



Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 2.0000V
Step .0500V

Variable2:
VD -Ch1
Start .0500V
Stop 5.0490V
Step 5.0000V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 23.

Subthreshold current characteristics of large NMOS transistor at $V_D = 50mV$ and 5V

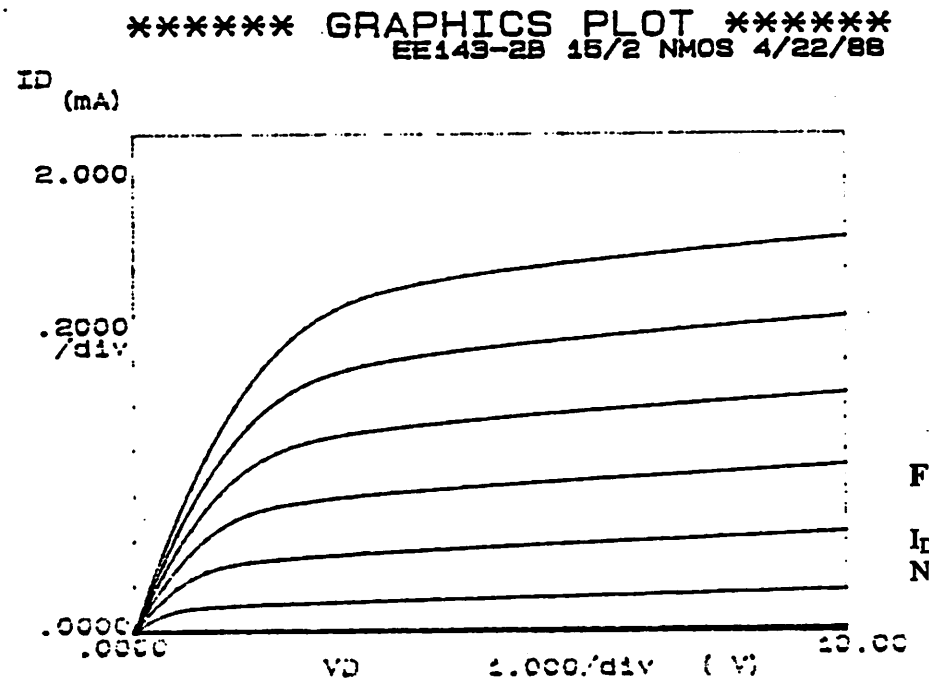


Figure 24.

$I_D - V_D$ characteristics of L = 2μm NMOS transistor (W = 15μm)

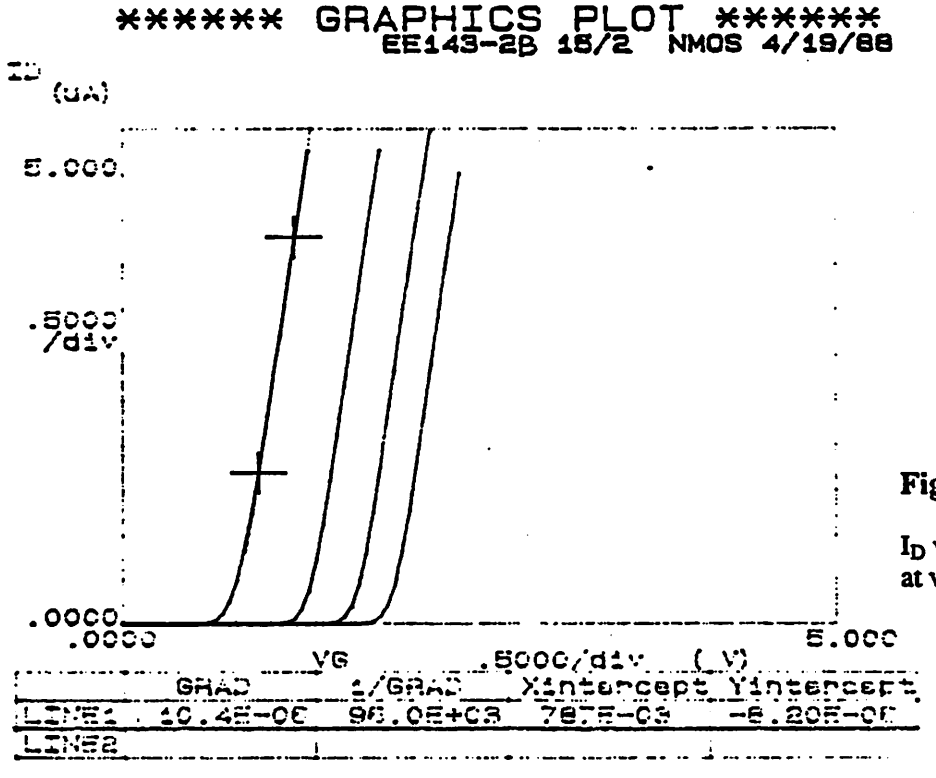
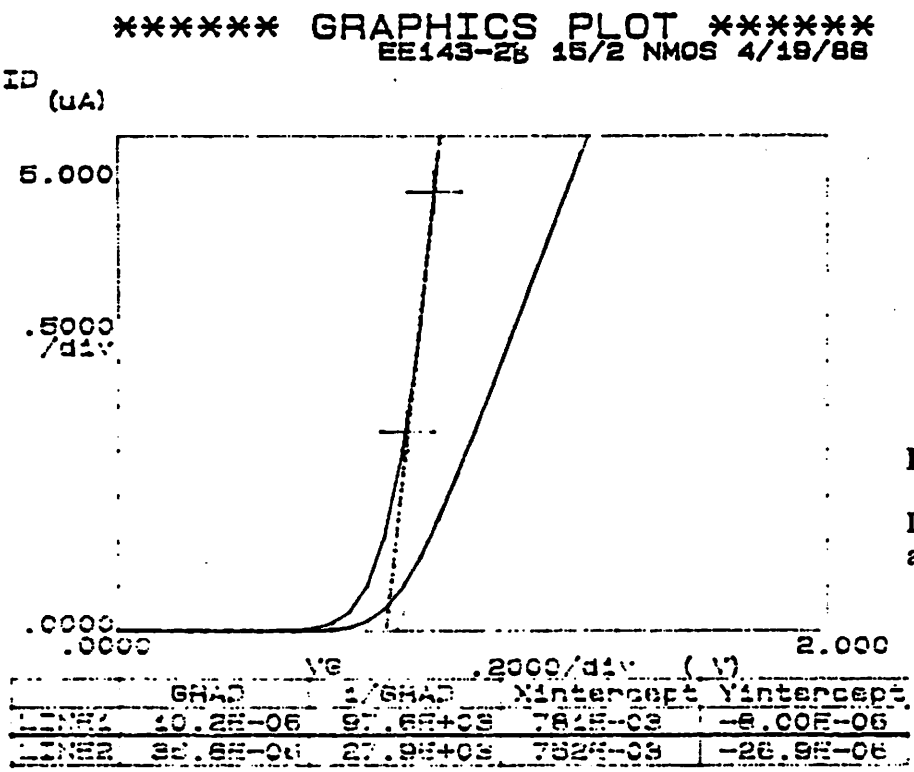


Figure 25.

I_D vs. V_G of L = 2μm NMOS transistor at varying substrate bias, V_D = 50mV



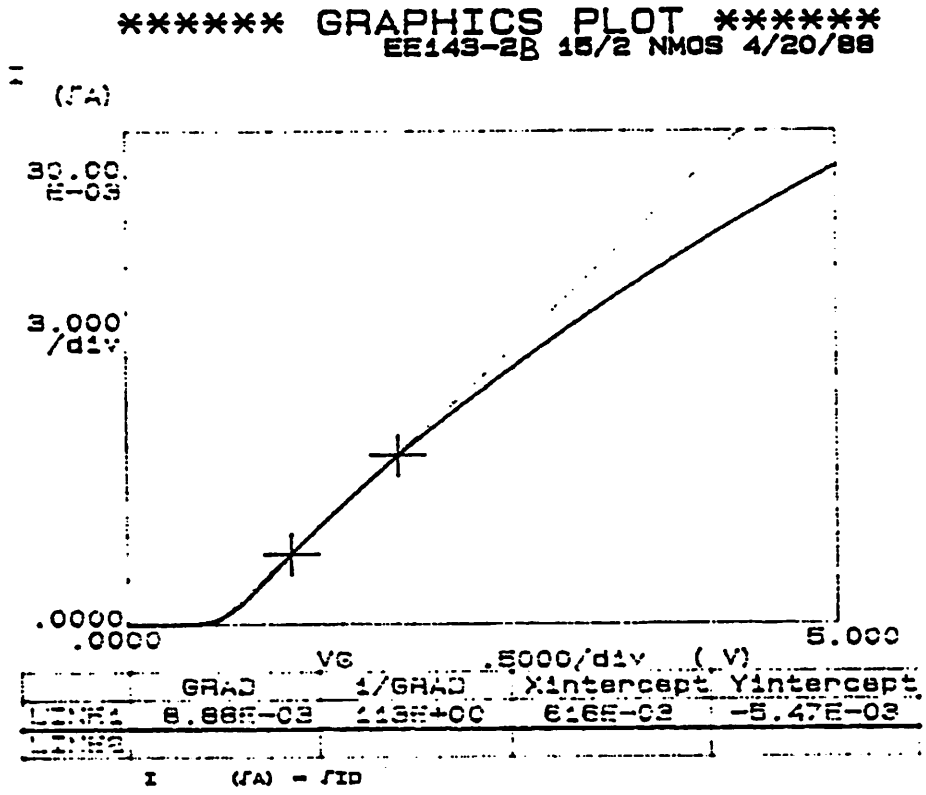

```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VD     -Ch1
 Start          .0500V
 Stop          5.0480V
 Step          5.0000V

Constants:
 VS     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 26.

I_D vs. V_G of L = 2μm NMOS transistor at V_D = 50mV and 5V




```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VSUB   -Ch3
 Start          .0000V
 Stop           .0000V
 Step           .0000V

Constants:
 VD     -Ch1   5.0000V
 VS     -Ch2    .0000V
```

Figure 27.

$\sqrt{I_D}$ vs. V_G of L = 2μm NMOS transistor at V_D = 5V

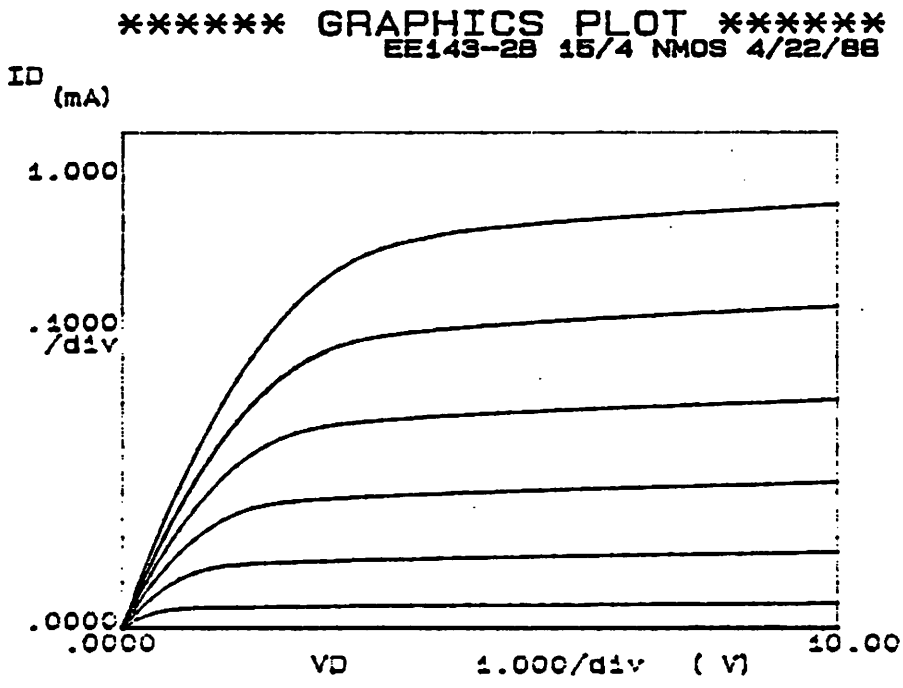


Figure 28.

$I_D - V_D$ characteristics of L = 4μm NMOS transistor (W = 15μm)

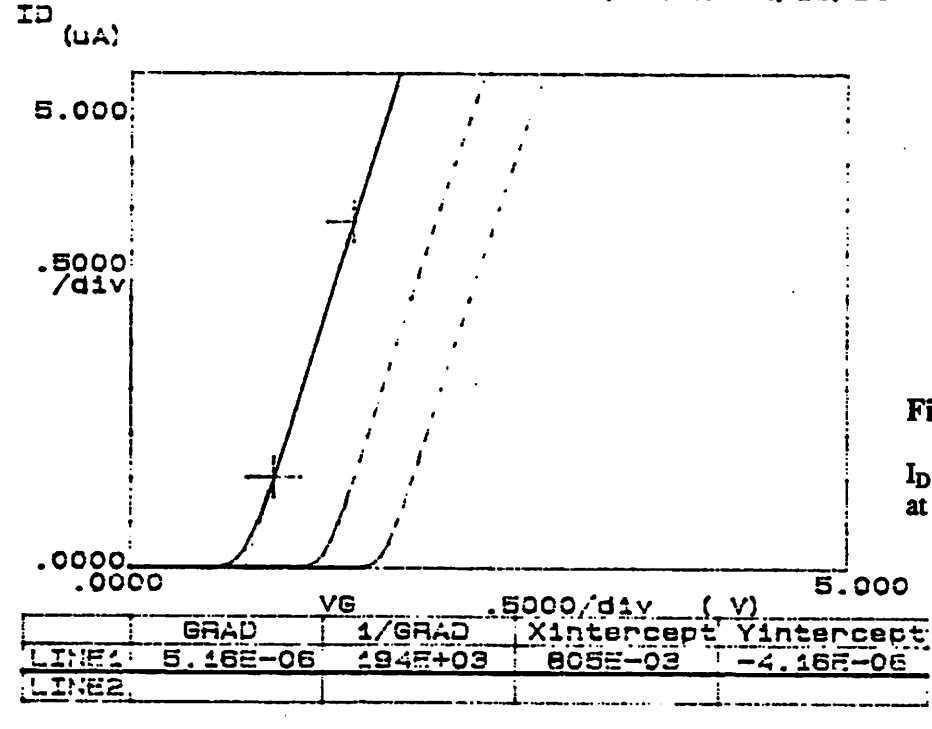
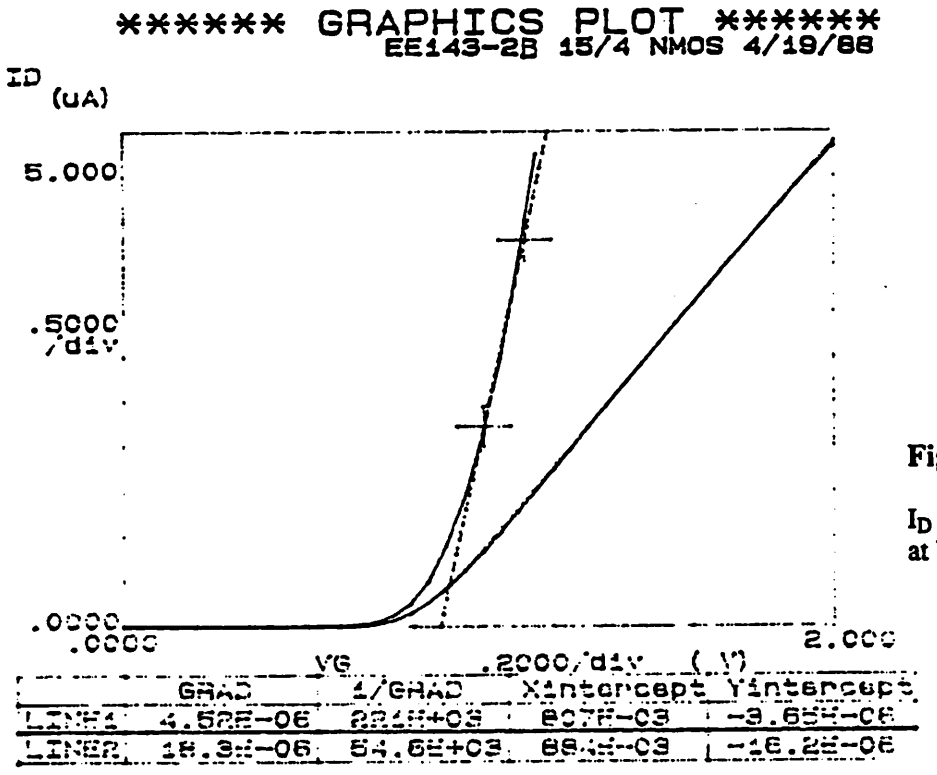


Figure 29.

I_D vs. V_G of L = 4μm NMOS transistor at varying substrate bias, V_D = 50mV



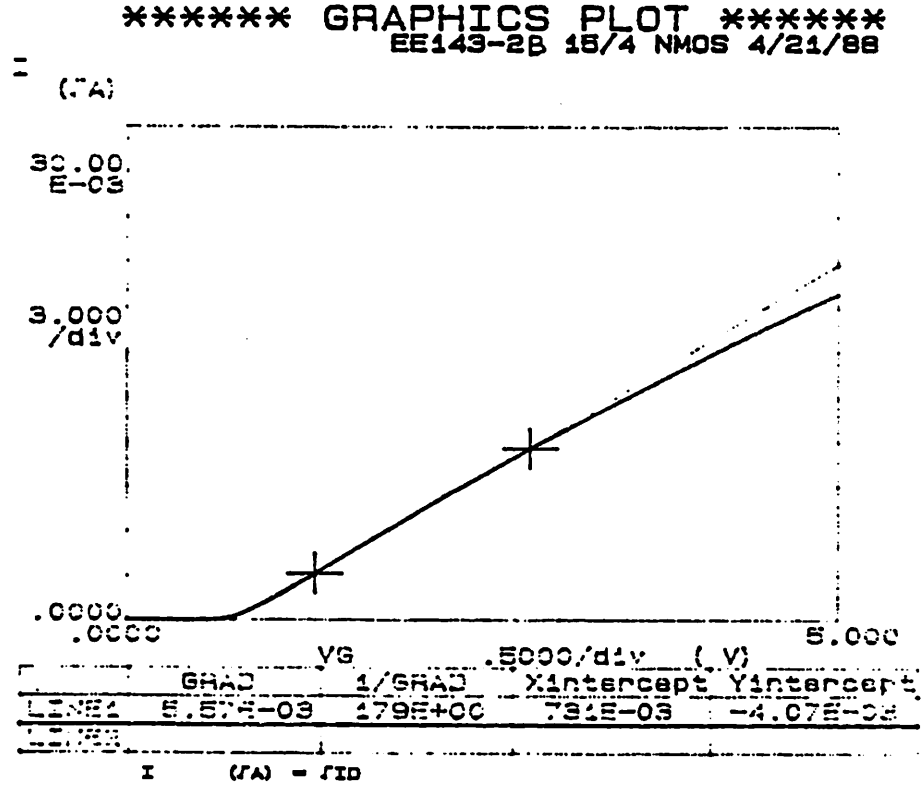

```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VD     -Ch1
 Start          .0500V
 Stop          5.0480V
 Step          5.0000V

Constants:
 VS     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 30.

I_D vs. V_G of L = 4μm NMOS transistor at V_D = 50mV and 5V



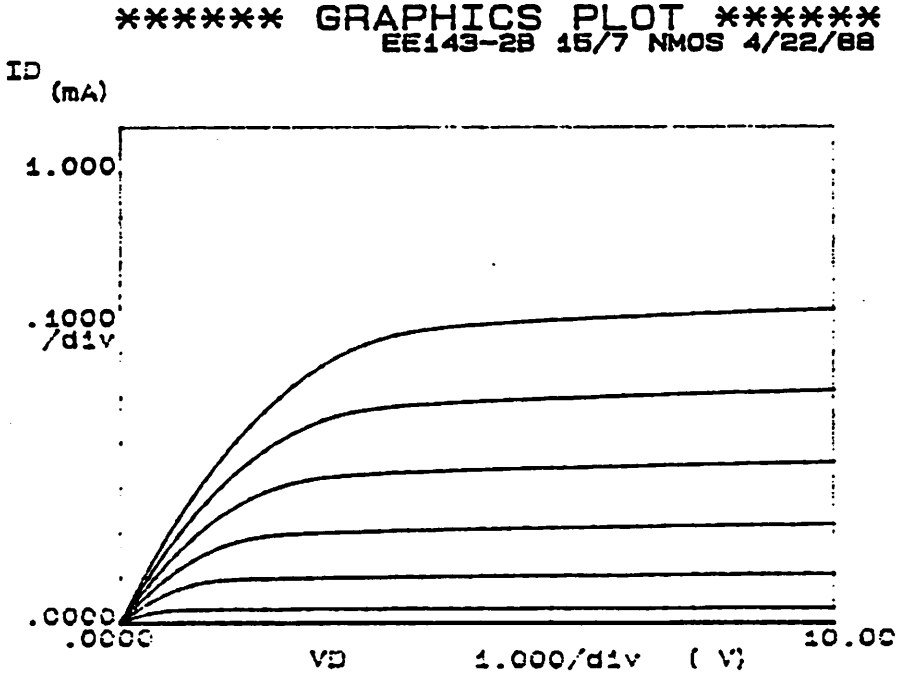

```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VSUB   -Ch3
 Start          .0000V
 Stop           .0000V
 Step           .0000V

Constants:
 VD     -Ch1    5.0000V
 VS     -Ch2     .0000V
```

Figure 31.

$\sqrt{I_D}$ vs. V_G of L = 4μm NMOS transistor at V_D = 5V



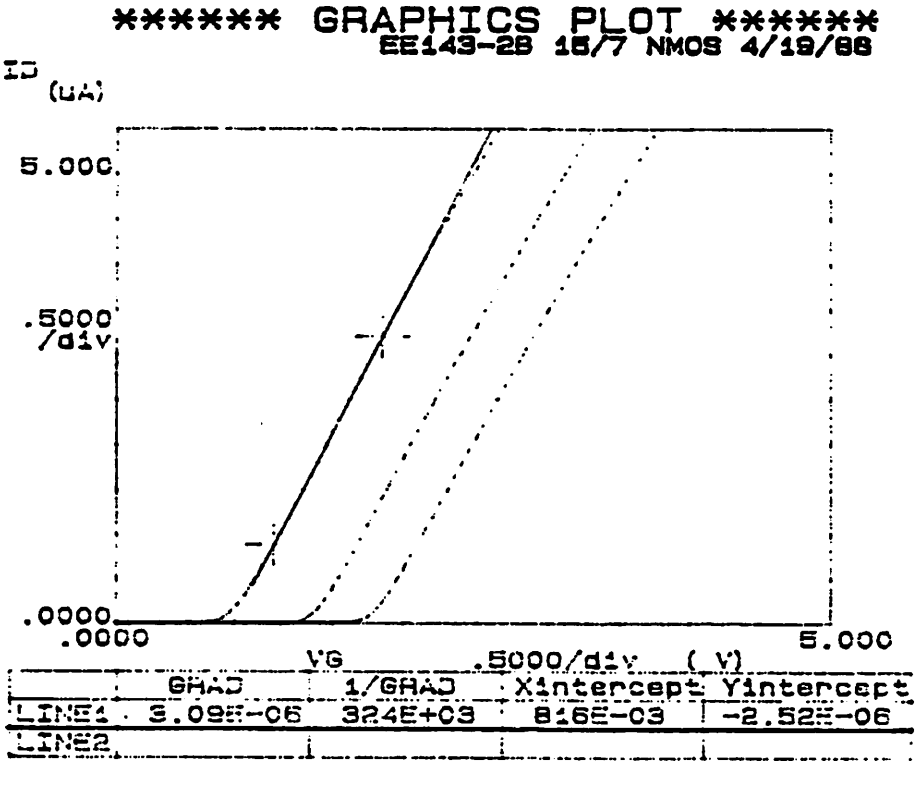

```
Variable1:
 VD     -Ch1
 Linear sweep
 Start          .0000V
 Stop         10.000V
 Step          .2000V

Variable2:
 VG     -Ch4
 Start          .0000V
 Stop          7.0000V
 Step          1.0000V

Constants:
 VS     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 32.

$I_D - V_D$ characteristics of L = 7μm NMOS transistor (W = 15μm)




```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step          .0500V

Variable2:
 VSUB   -Ch3
 Start          .0000V
 Stop         -5.0000V
 Step         -1.0000V

Constants:
 VD     -Ch1    .050V
 VS     -Ch2    .0000V
```

Figure 33.

I_D vs. V_G of L = 7μm NMOS transistor at varying substrate bias, V_D = 50mV

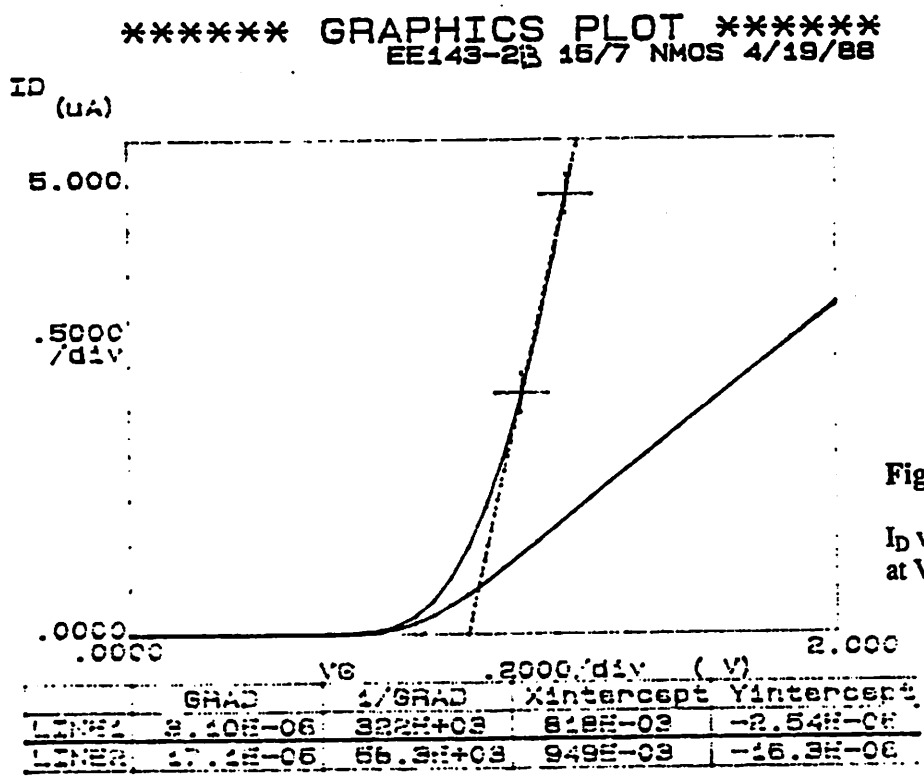


Figure 34.

I_D vs. V_G of L = 7μm NMOS transistor at V_D = 50mV and 5V

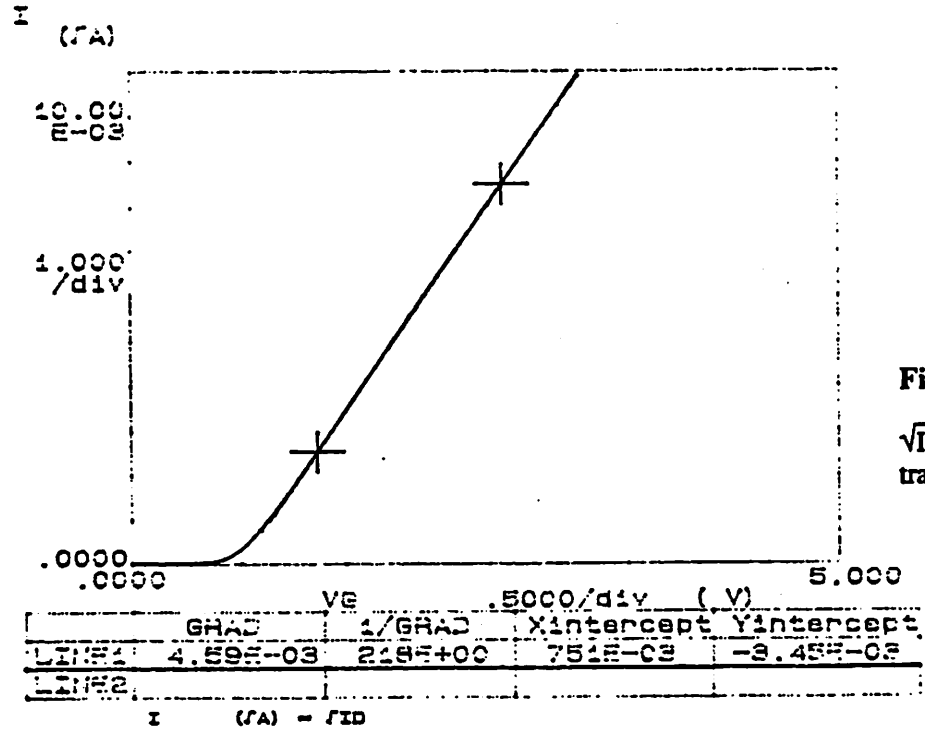


Figure 35.

$\sqrt{I_D}$ vs. V_G of L = 7μm NMOS transistor at V_D = 5V

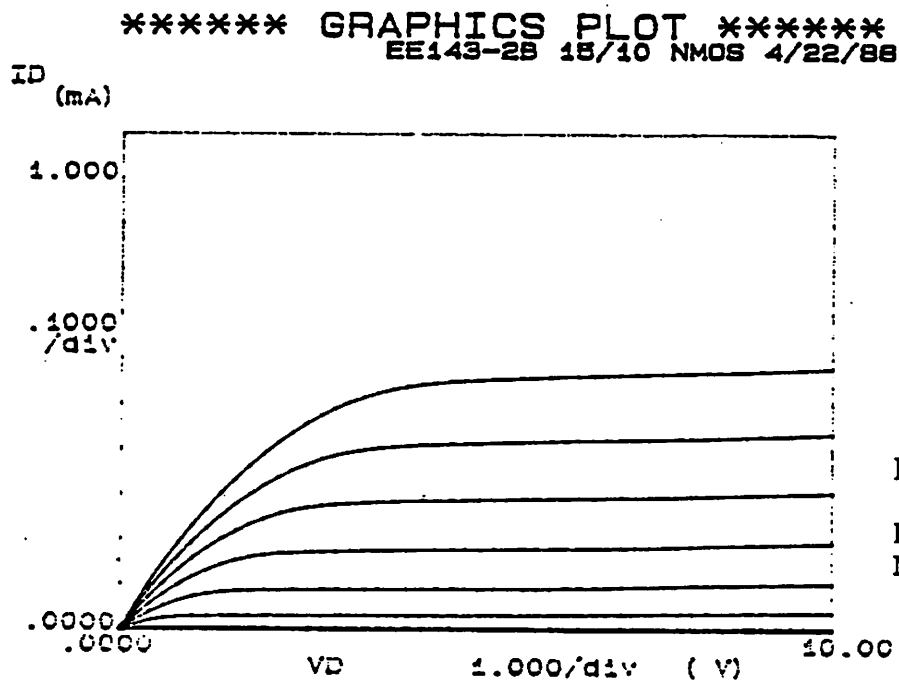


Figure 36.

$I_D - V_D$ characteristics of L = 10μm NMOS transistor (W = 15μm)

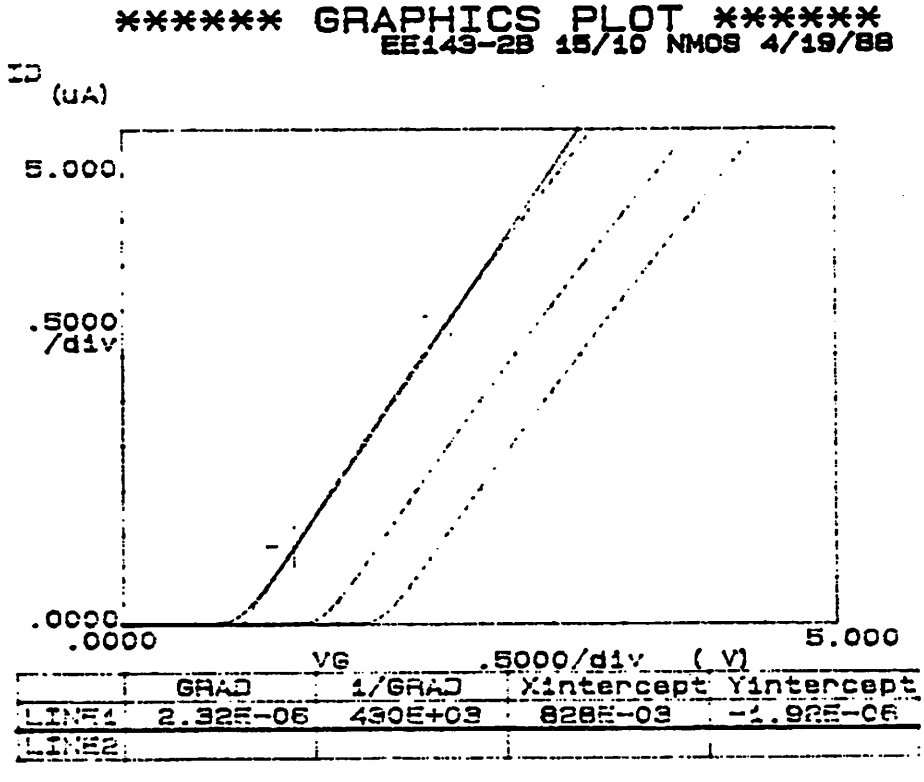


Figure 37.

I_D vs. V_G of L = 10μm NMOS transistor at varying substrate bias, V_D = 50mV

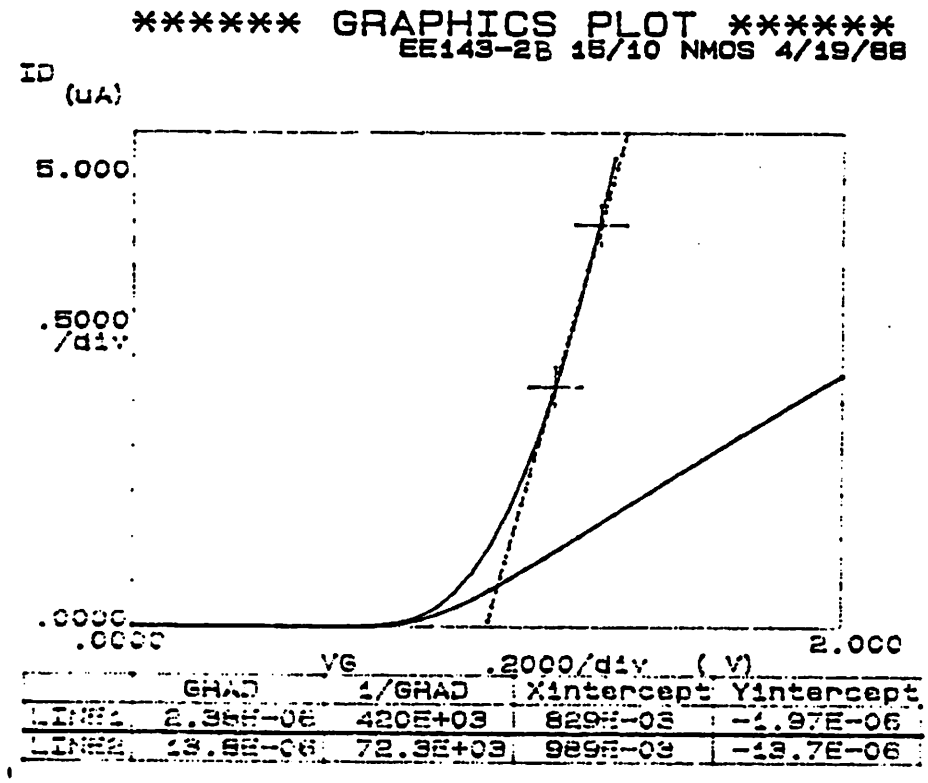


Figure 38.

I_D vs. V_G of L = 10μm NMOS transistor at V_D = 50mV and 5V

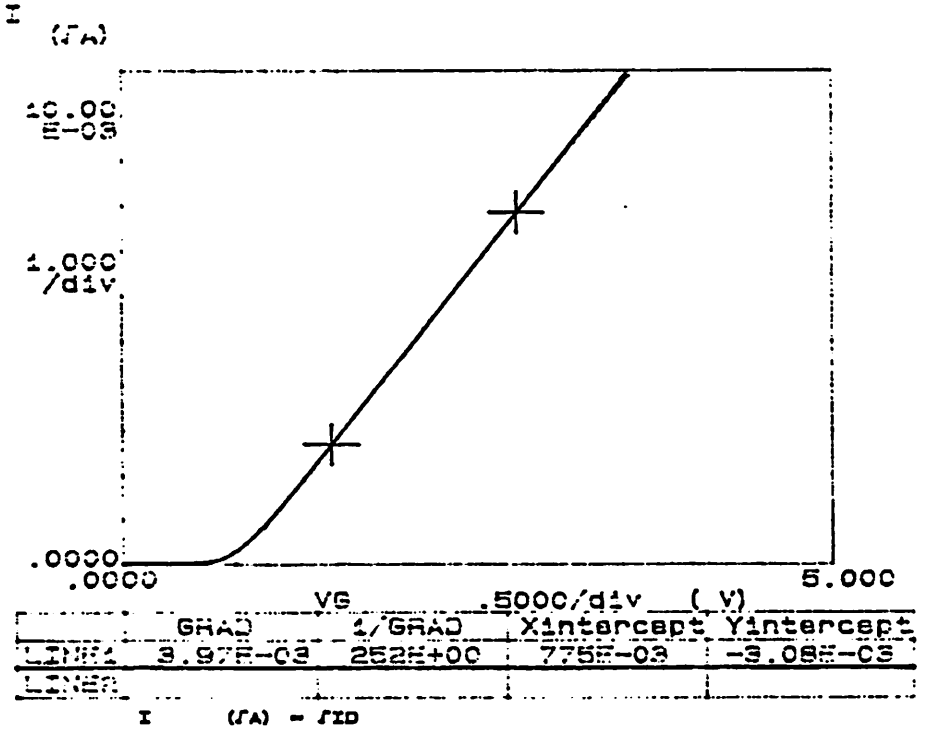
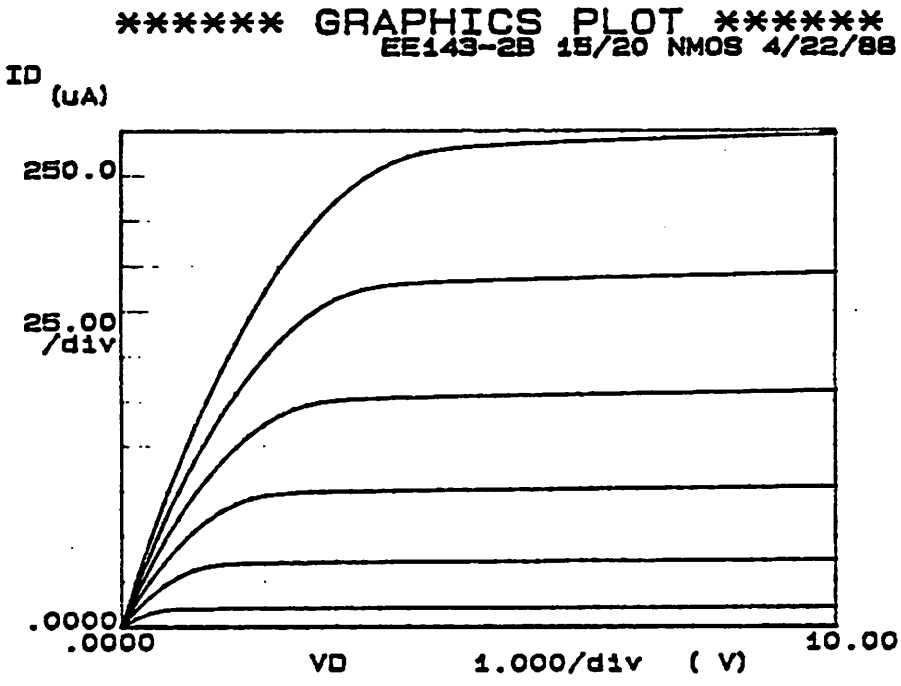


Figure 39.

$\sqrt{I_D}$ vs. V_G of L = 10μm NMOS transistor at V_D = 5V



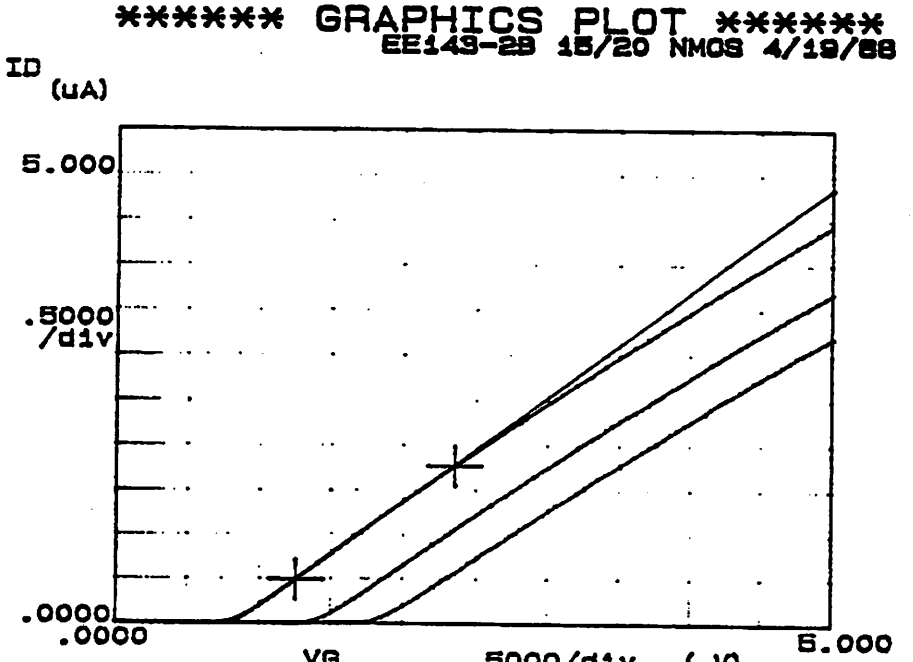

```
Variable1:
 VD     -Ch1
 Linear sweep
 Start          .0000V
 Stop         10.000V
 Step          .2000V

Variable2:
 VG     -Ch4
 Start          .0000V
 Stop          7.0000V
 Step          1.0000V

Constants:
 VB     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 40.

$I_D - V_D$ characteristics of L = 20μm NMOS transistor (W = 15μm)



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	1.16E-06	861E+03	828E-03	-962E-09
LINE2				

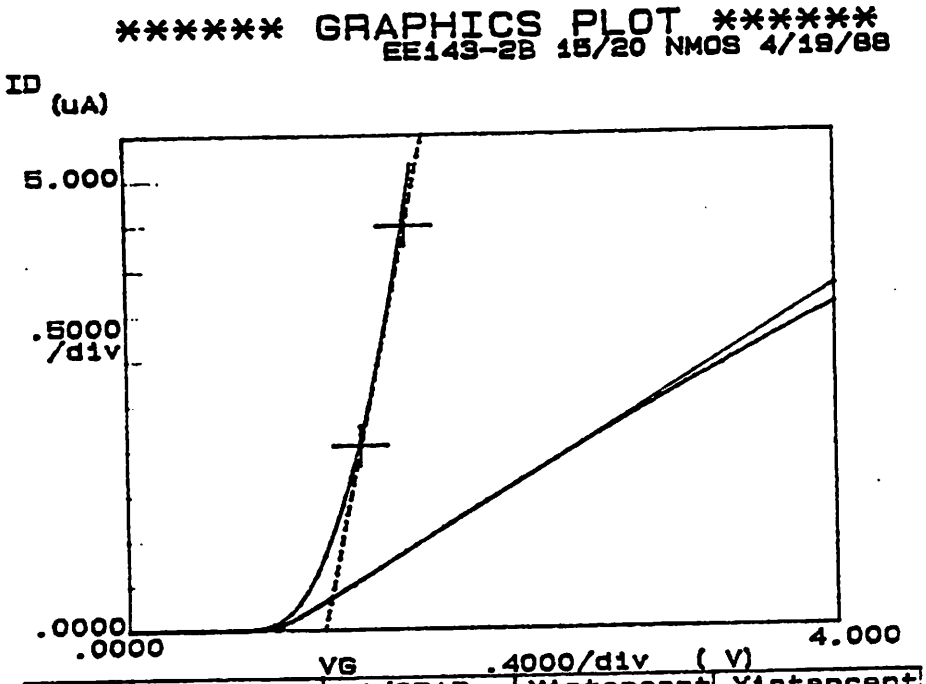
```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VSUB   -Ch3
 Start          .0000V
 Stop         -2.0000V
 Step         -1.0000V

Constants:
 VD     -Ch1    .0500V
 VB     -Ch2    .0000V
```

Figure 41.

I_D vs. V_G of L = 20μm NMOS transistor at varying substrate bias, V_D = 50mV



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	1.19E-06	840E+03	826E-03	-984E-09
LINE2	9.65E-06	104E+03	1.10E+00	-10.6E-06

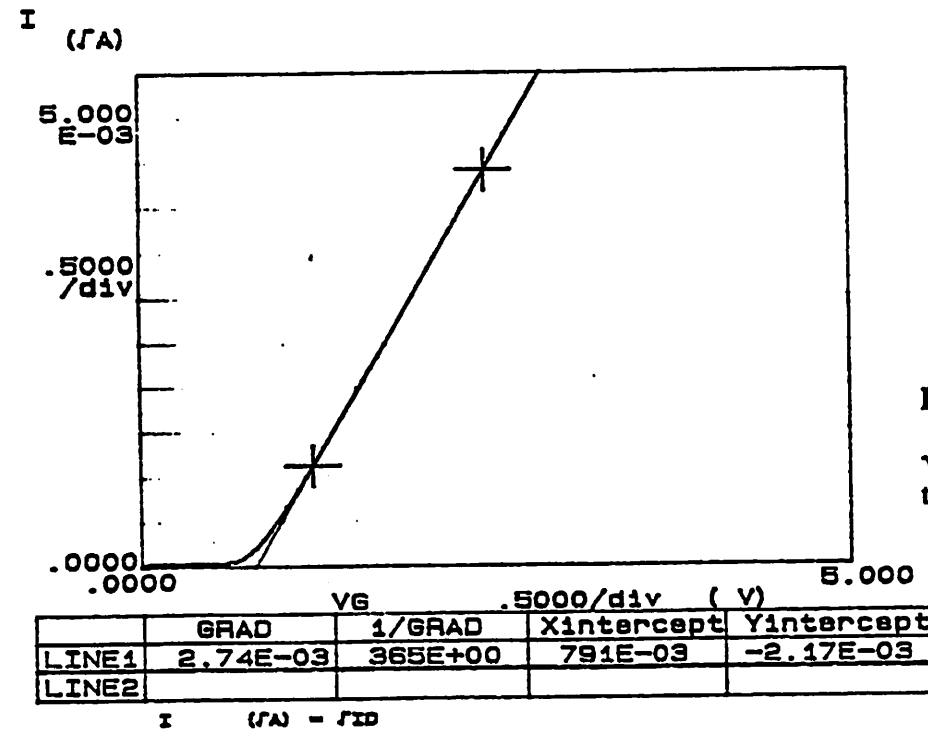
```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VD     -Ch1
 Start          .0500V
 Stop          5.0490V
 Step          5.0000V

Constants:
 VB     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 42.

I_D vs. V_G of L = 20μm NMOS transistor at V_D = 50mV and 5V



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	2.74E-03	365E+00	791E-03	-2.17E-03
LINE2				

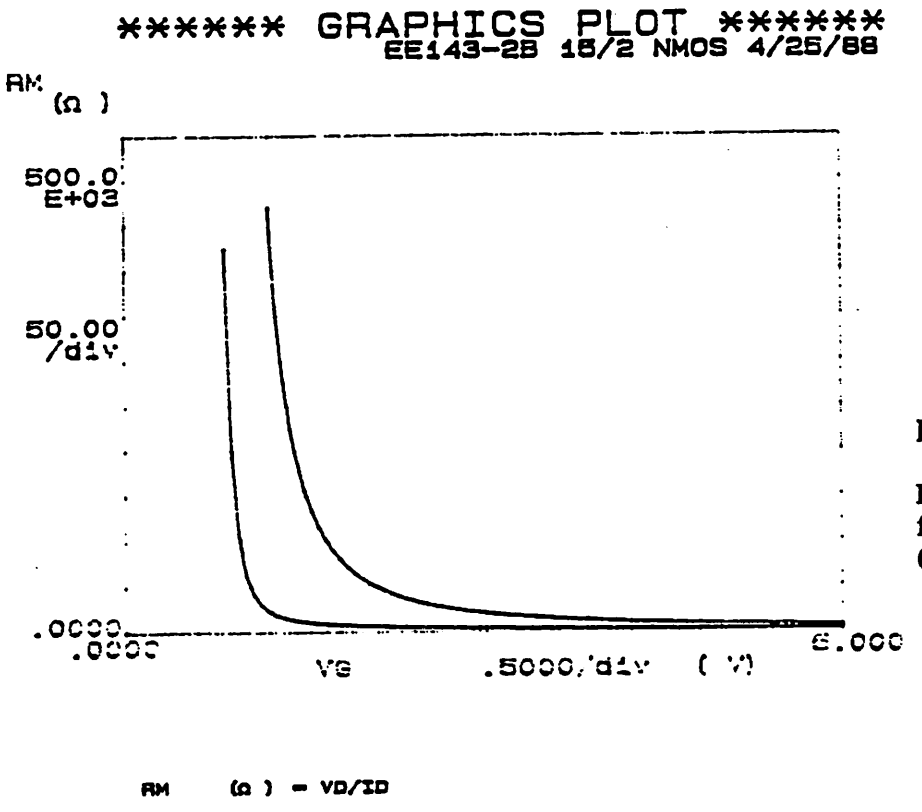
```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VSUB   -Ch3
 Start          .0000V
 Stop           .0000V
 Step           .0000V

Constants:
 VD     -Ch1   5.0000V
 VB     -Ch2    .0000V
```

Figure 43.

$\sqrt{I_D}$ vs. V_G of L = 20μm NMOS transistor at V_D = 5V



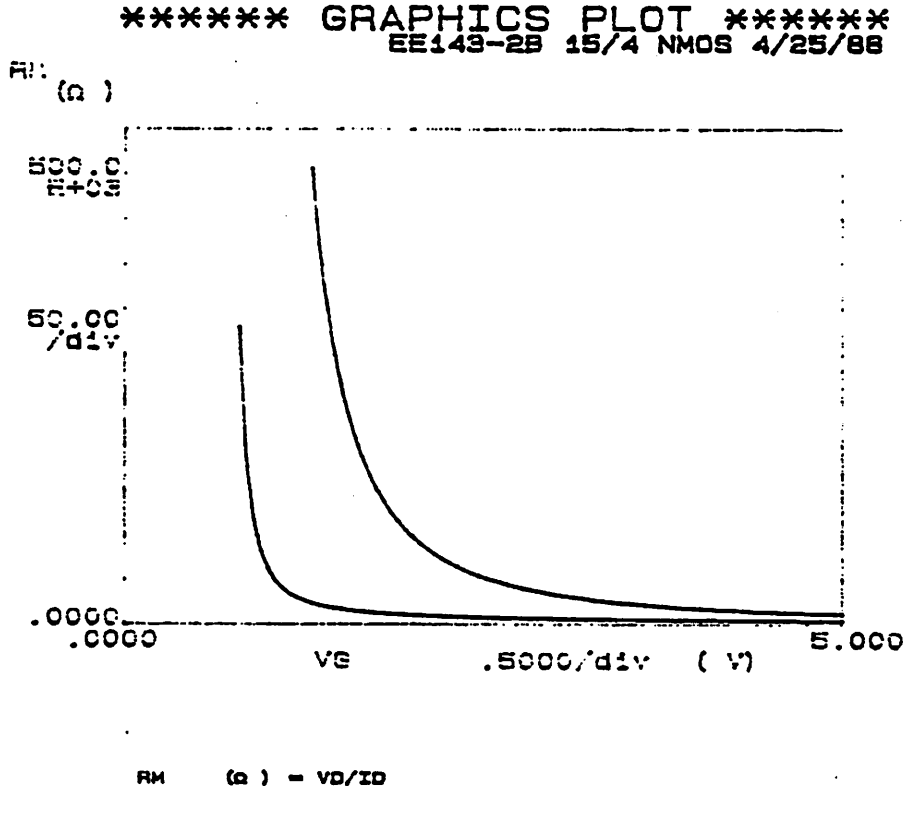

```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VD     -Ch1
 Start          .0500V
 Stop          5.0490V
 Step          5.0000V

Constants:
 VG     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 44.

R_m vs. V_G at V_D = 50mV and 5V for L = 2μm NMOS transistor (W = 15μm)




```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VD     -Ch1
 Start          .0500V
 Stop          5.0490V
 Step          5.0000V

Constants:
 VG     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 45.

R_m vs. V_G at V_D = 50mV and 5V for L = 4μm NMOS transistor (W = 15μm)

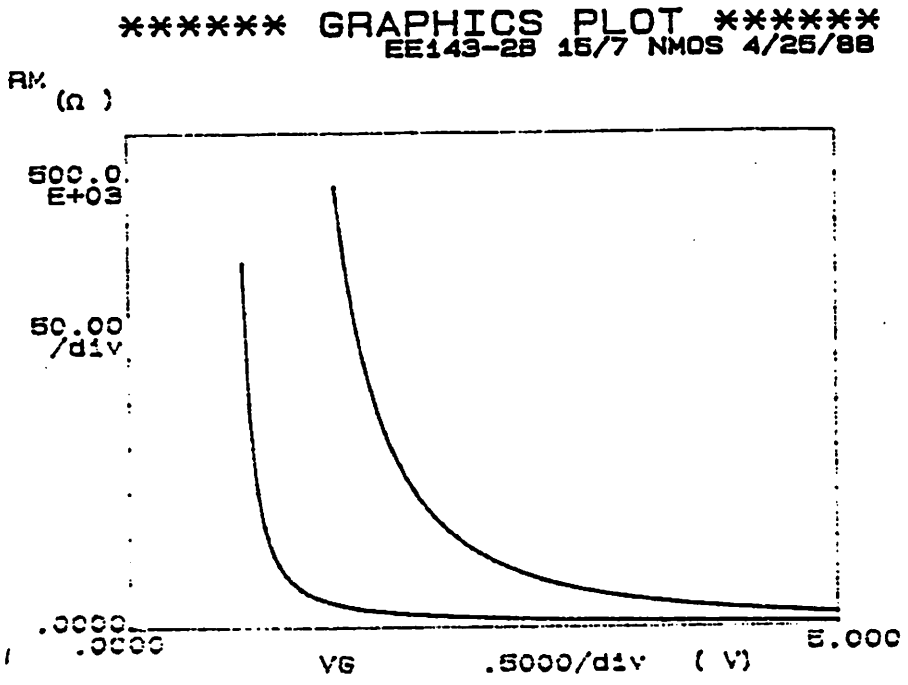


Figure 46.

R_m vs. V_G at V_D = 50mV and 5V for L = 7μm NMOS transistor (W = 15μm)

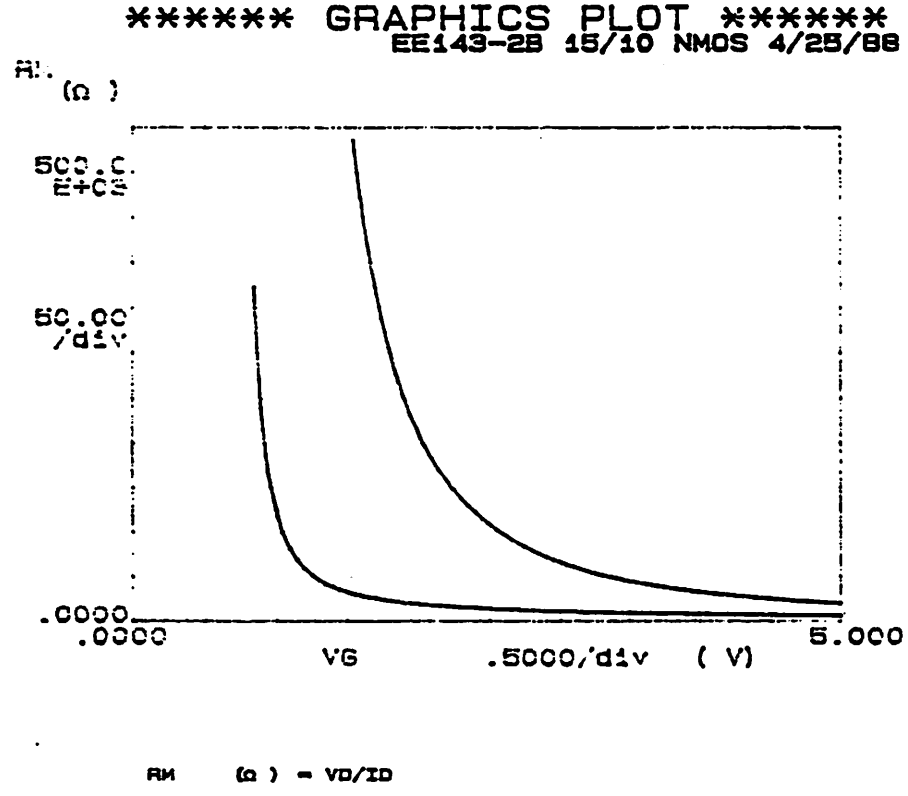
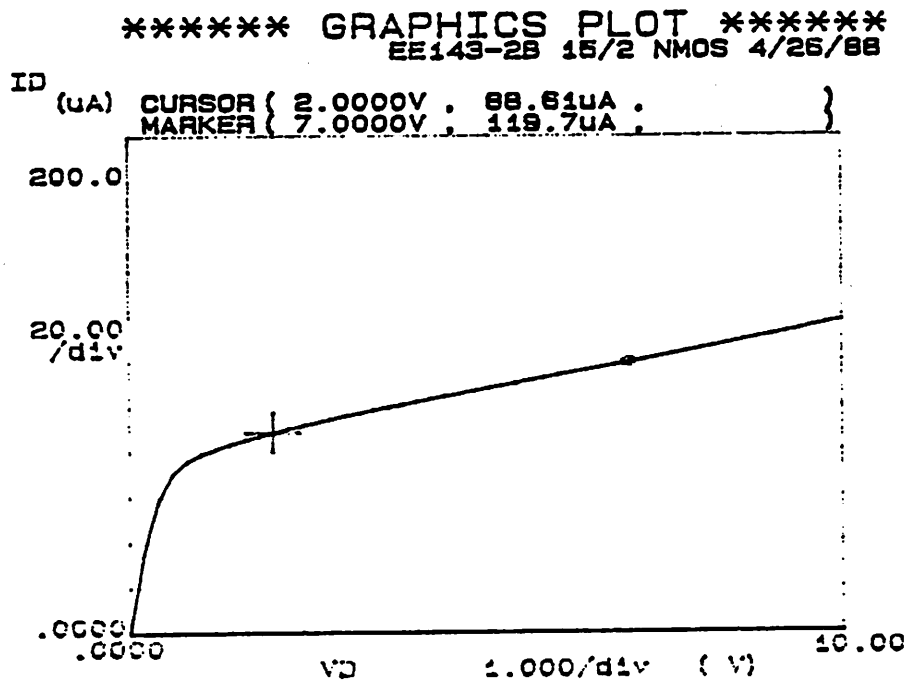


Figure 47.

R_m vs. V_G at V_D = 50mV and 5V for L = 10μm NMOS transistor (W = 15μm)



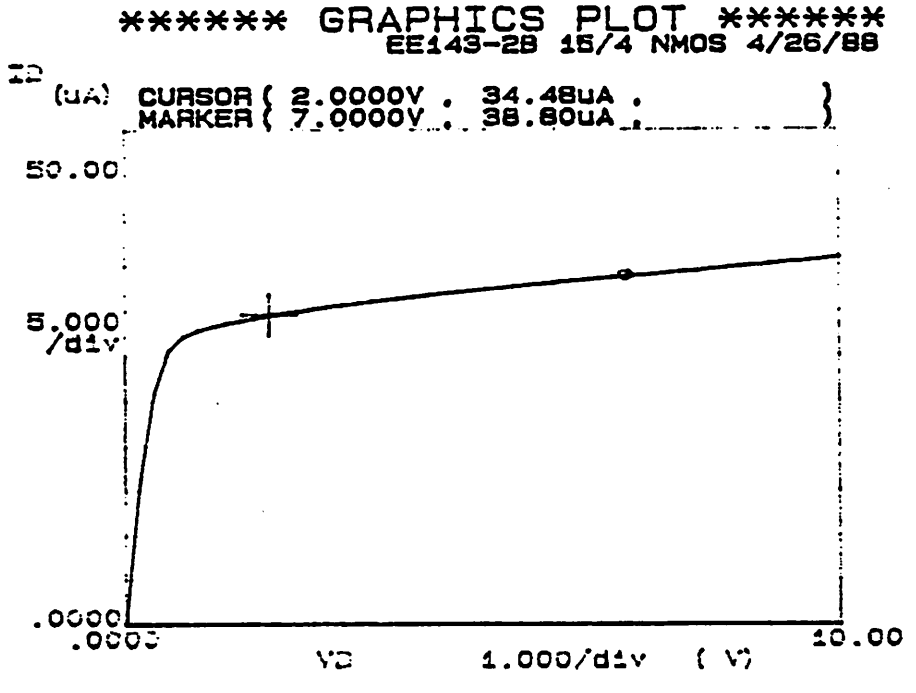

```
Variable1:
 VD     -Ch1
 Linear sweep
 Start          .0000V
 Stop         10.000V
 Step          .2000V

Variable2:
 VG     -Ch4
 Start          .0000V
 Stop         1.7780V
 Step         1.7800V

Constants:
 VB     -Ch2    .0000V
 VBUB   -Ch3    .0000V
```

Figure 48.

I_D vs. V_D at $V_G = V_T + 1$ for $L = 2\mu m$ NMOS transistor



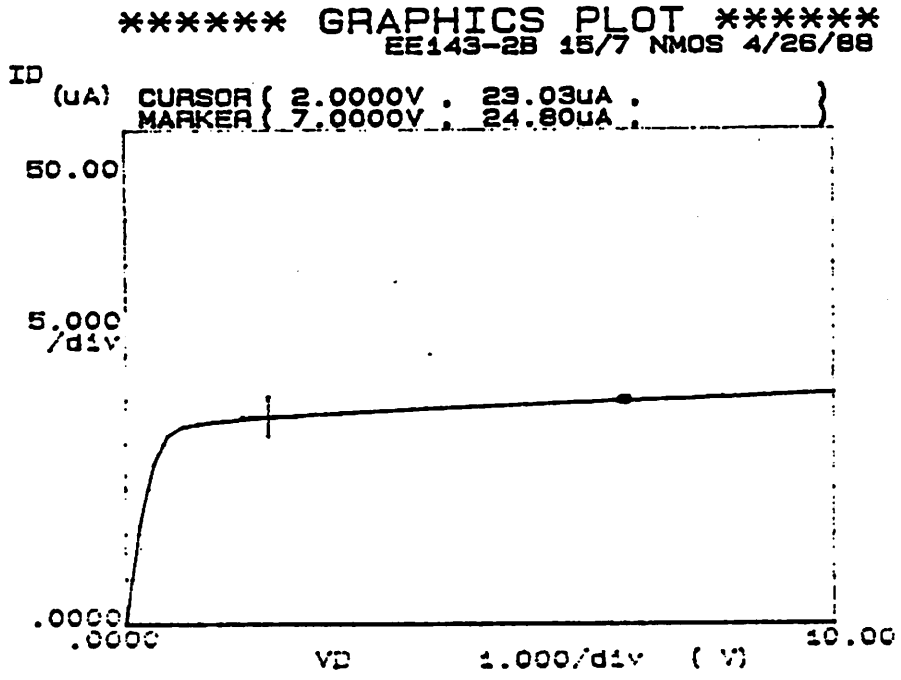

```
Variable1:
 VD     -Ch1
 Linear sweep
 Start          .0000V
 Stop         10.000V
 Step          .2000V

Variable2:
 VG     -Ch4
 Start          .0000V
 Stop         1.8060V
 Step         1.8070V

Constants:
 VB     -Ch2    .0000V
 VBUB   -Ch3    .0000V
```

Figure 49.

I_D vs. V_D at $V_G = V_T + 1$ for $L = 4\mu m$ NMOS transistor



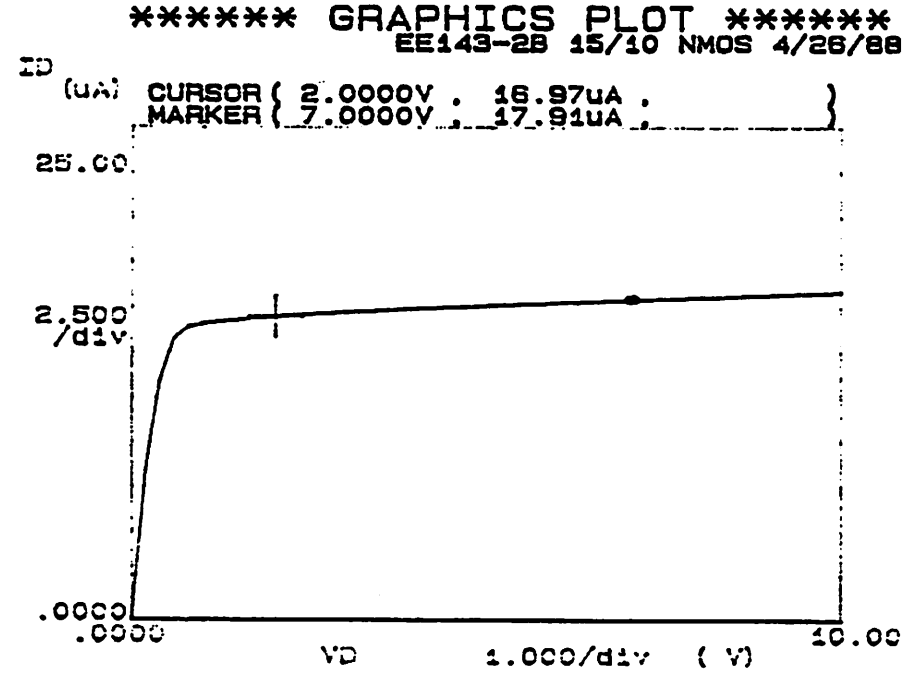

```
Variable1:
 VD     -Ch1
 Linear sweep
 Start          .0000V
 Stop         10.000V
 Step          .2000V

Variable2:
 VG     -Ch4
 Start          .0000V
 Stop         1.8170V
 Step         1.8180V

Constants:
 VS     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 50.

I_D vs. V_D at $V_G = V_T + 1$ for L = 7μm NMOS transistor



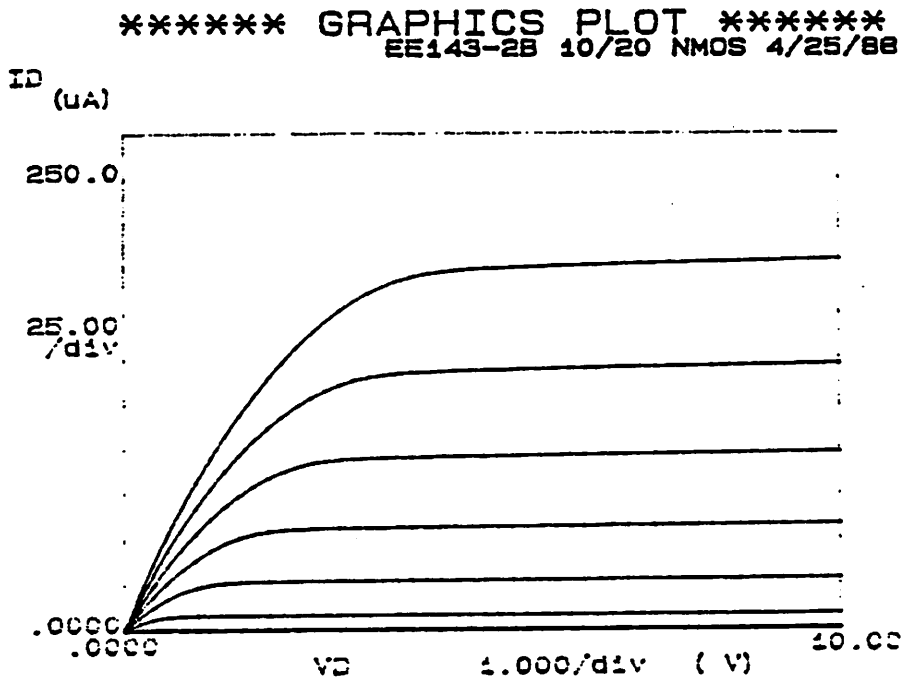

```
Variable1:
 VD     -Ch1
 Linear sweep
 Start          .0000V
 Stop         10.000V
 Step          .2000V

Variable2:
 VG     -Ch4
 Start          .0000V
 Stop         1.8290V
 Step         1.8290V

Constants:
 VS     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 51.

I_D vs. V_D at $V_G = V_T + 1$ for L = 10μm NMOS transistor



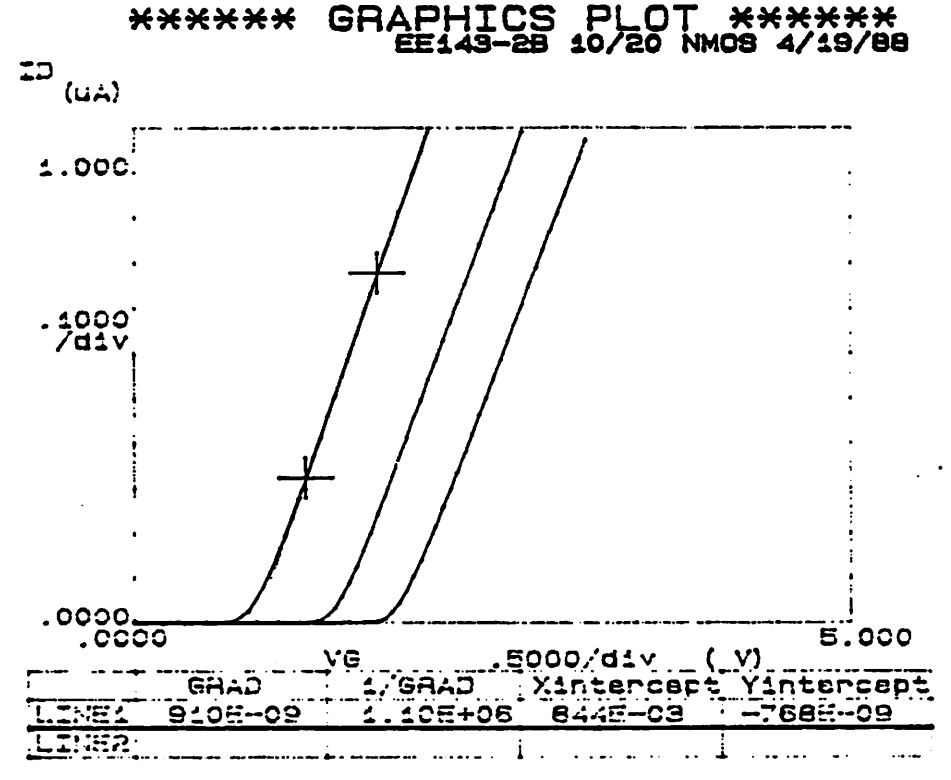

```
Variable1:
 VD     -Ch1
 Linear sweep
 Start          .0000V
 Stop         10.000V
 Step          .2000V

Variable2:
 VG     -Ch4
 Start          .0000V
 Stop          7.0000V
 Step          1.0000V

Constants:
 VS     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 52.

$I_D - V_D$ characteristics of W = 10μm NMOS transistor (L = 20μm)



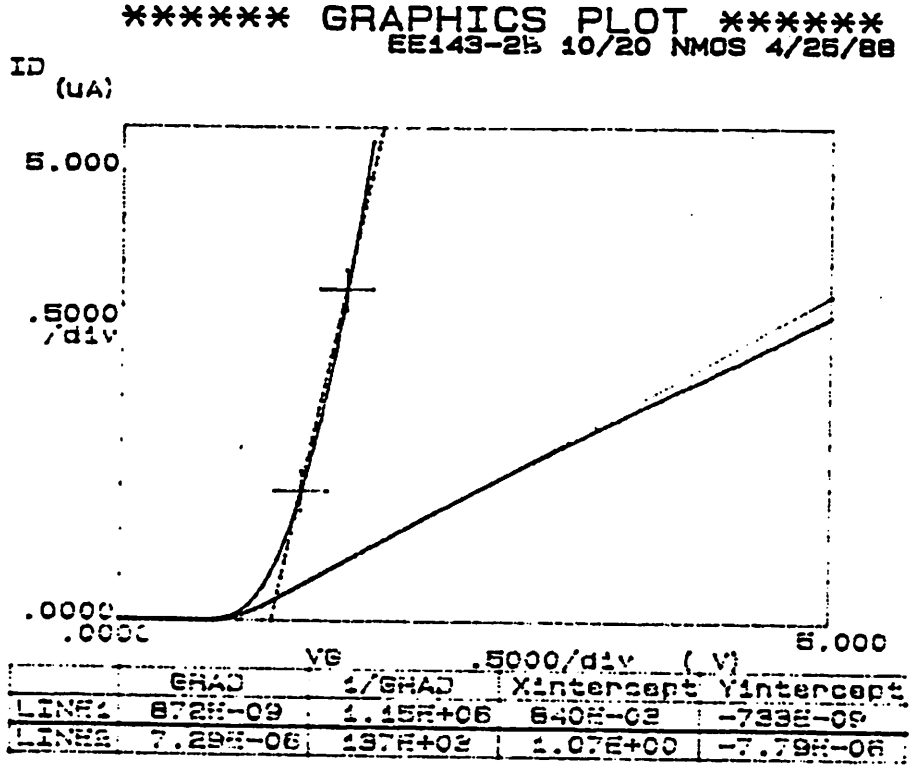

```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step          .0500V

Variable2:
 VSUB   -Ch3
 Start          .0000V
 Stop         -2.0000V
 Step         -1.0000V

Constants:
 VD     -Ch1    .0500V
 VS     -Ch2    .0000V
```

Figure 53.

I_D vs. V_G of W = 10μm NMOS transistor at varying substrate bias, V_D = 50mV



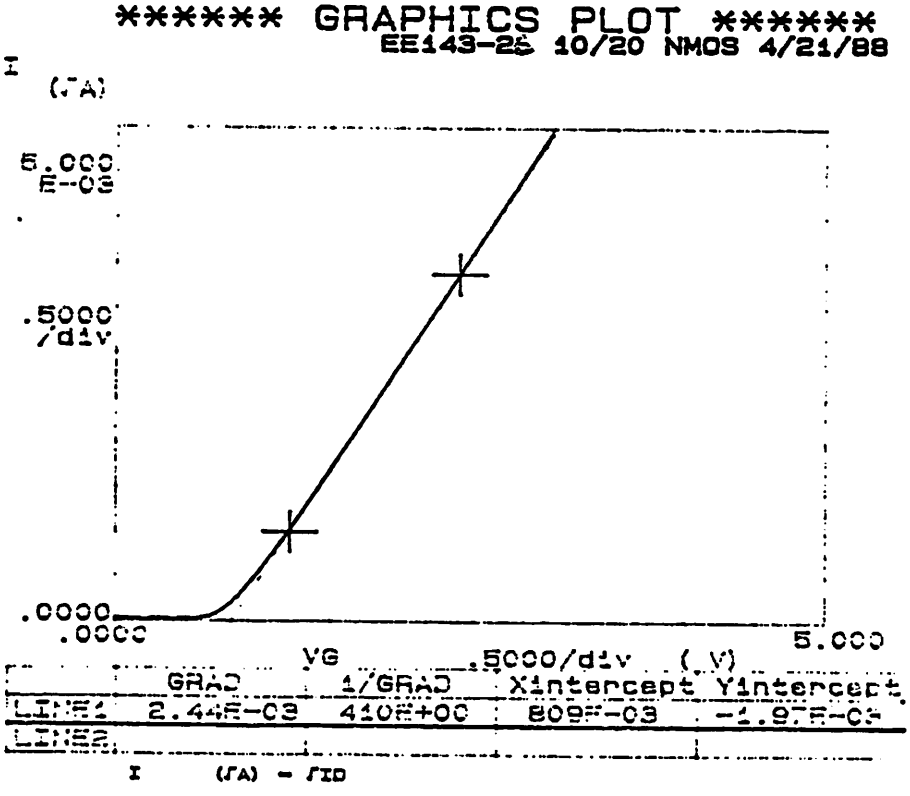

```
Variable1:
 VG      -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VD      -Ch1
 Start          .0500V
 Stop          5.0480V
 Step          5.0000V

Constants:
 VS      -Ch2    .0000V
 VSUB    -Ch3    .0000V
```

Figure 54.

I_D vs. V_G of W = 10μm NMOS transistor at V_D = 50mV and 5V



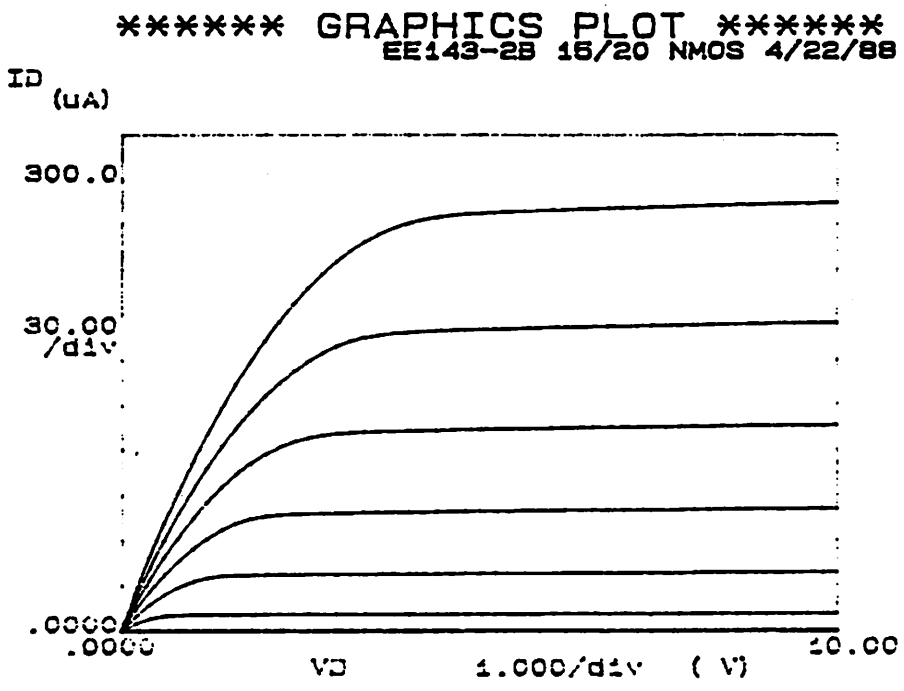

```
Variable1:
 VG      -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VSUB    -Ch3
 Start          .0000V
 Stop           .0000V
 Step           .0000V

Constants:
 VD      -Ch1   5.0000V
 VS      -Ch2    .0000V
```

Figure 55.

$\sqrt{I_D}$ vs. V_G of W = 10μm NMOS transistor at V_D = 5V



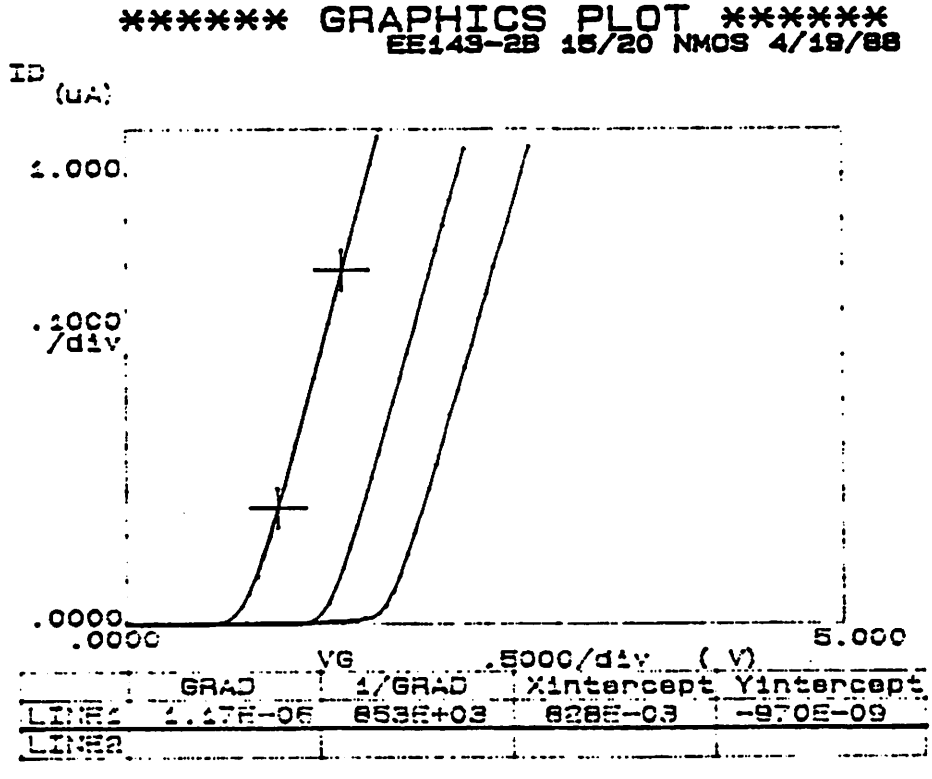

```
Variable1:
 VD     -Ch1
 Linear sweep
 Start          .0000V
 Stop         10.000V
 Step          .2000V

Variable2:
 VG     -Ch4
 Start          .0000V
 Stop          7.0000V
 Step          1.0000V

Constants:
 VS     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 56.

$I_D - V_D$ characteristics of W = 15μm NMOS transistor (L = 20μm)



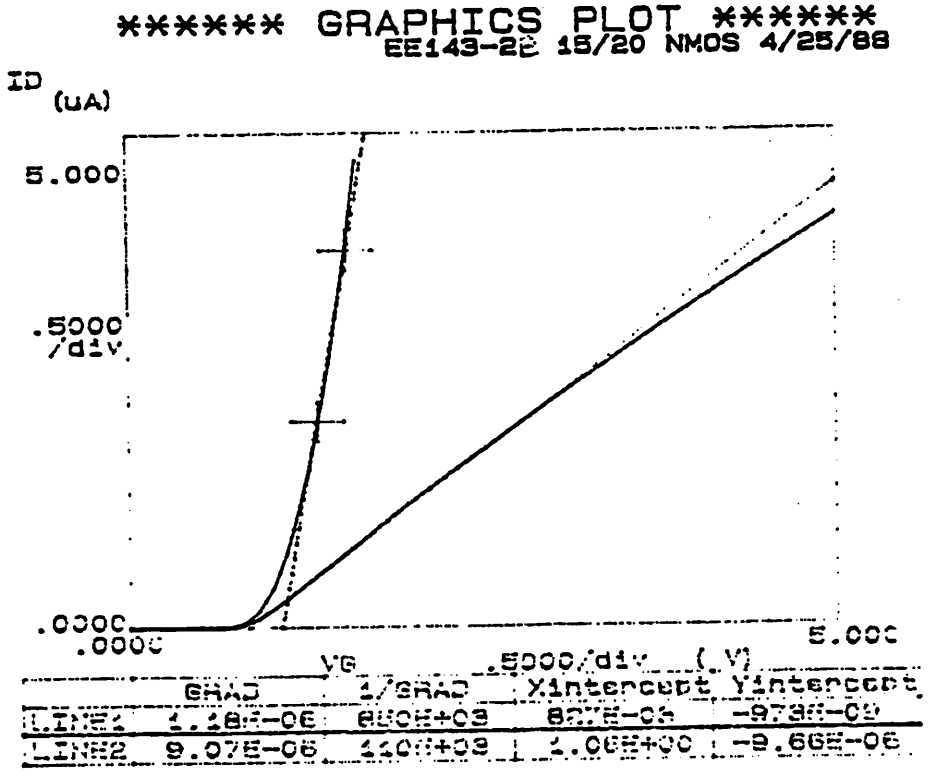

```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VSUB   -Ch3
 Start          .0000V
 Stop         -2.0000V
 Step         -1.0000V

Constants:
 VD     -Ch1    .0500V
 VS     -Ch2    .0000V
```

Figure 57.

I_D vs. V_G of W = 15μm NMOS transistor at varying substrate bias, V_D = 50mV



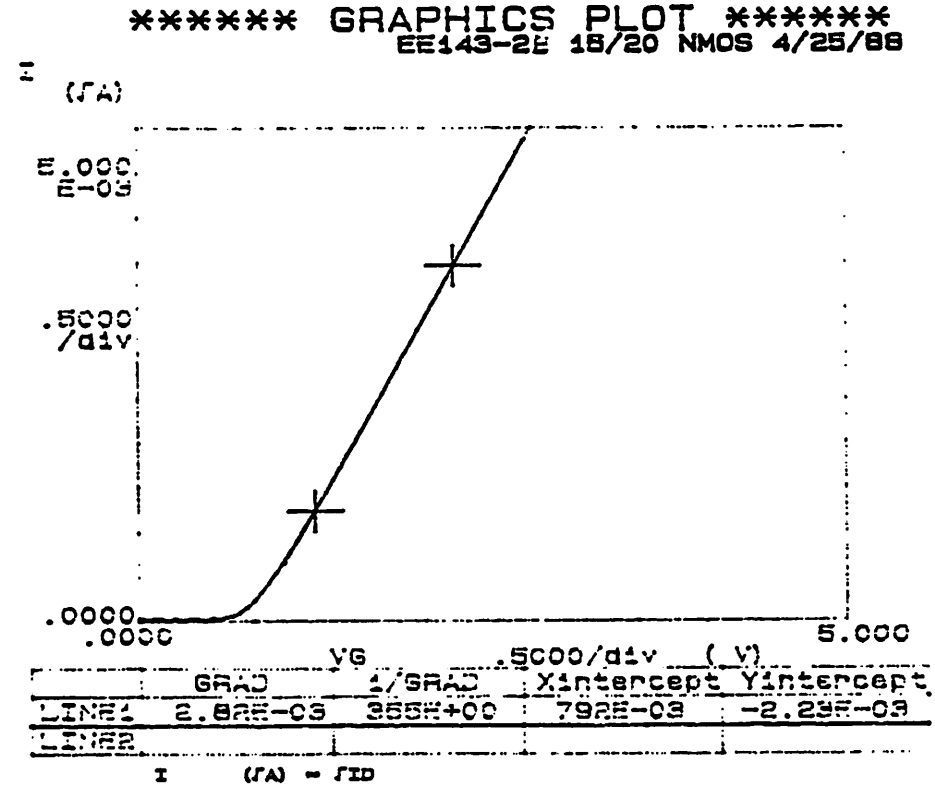
Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VD -Ch1
Start .0500V
Stop 5.0490V
Step 5.0000V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 58.

I_D vs. V_G of W = 15μm NMOS transistor at V_D = 50mV and 5V

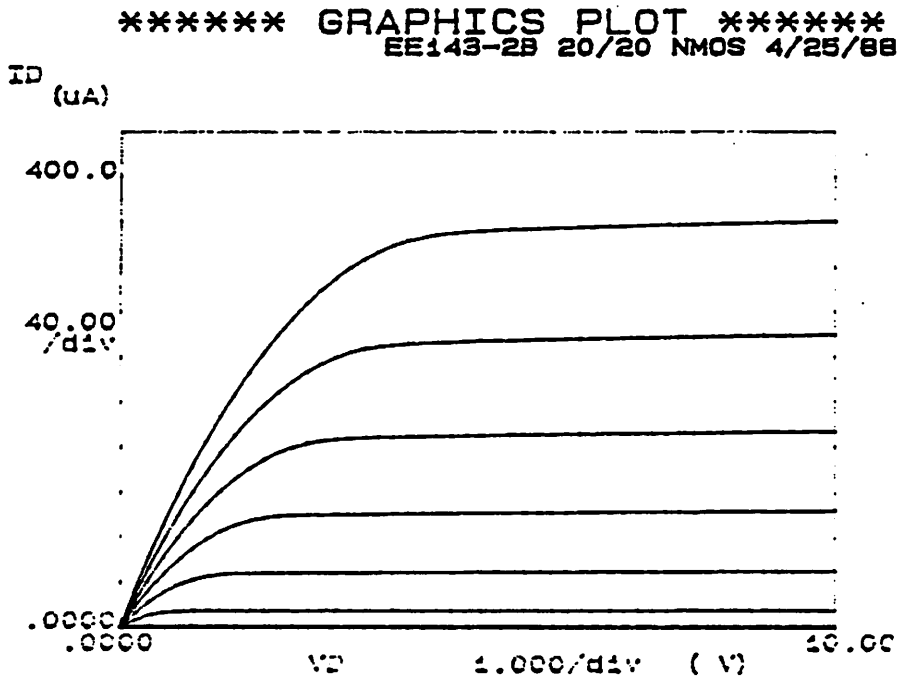


Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Constants:
VD -Ch1 5.0000V
VS -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 59.

$\sqrt{I_D}$ vs. V_G of W = 15μm NMOS transistor at V_D = 5V



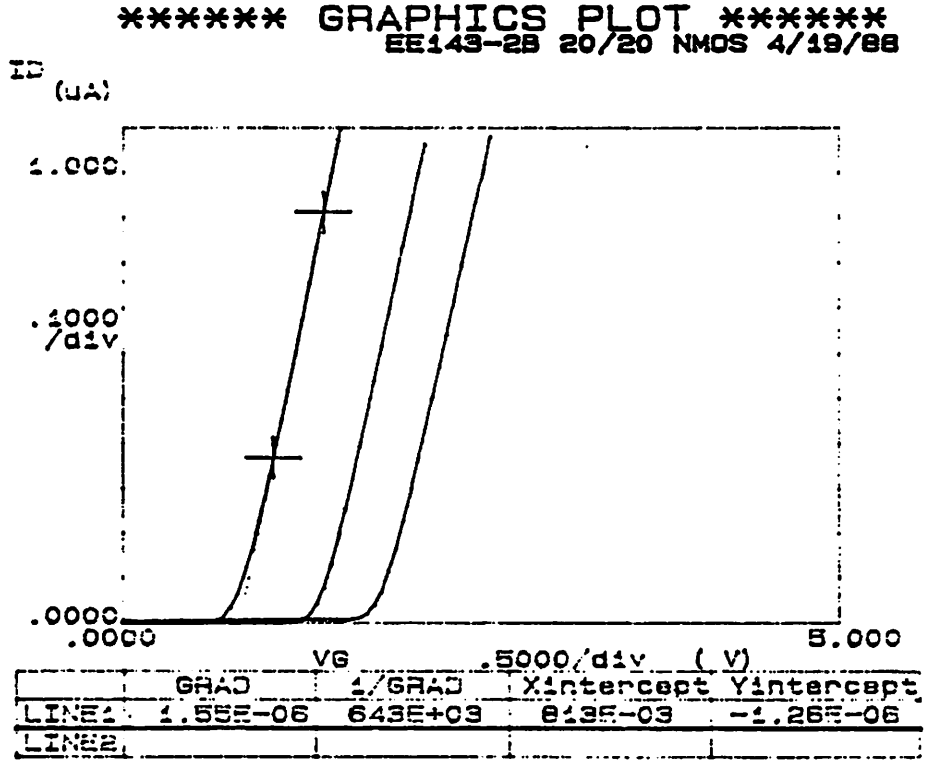

```
Variable1:
 VD     -Ch1
 Linear sweep
 Start          .0000V
 Stop         10.000V
 Step          .2000V

Variable2:
 VG     -Ch4
 Start          .0000V
 Stop          7.0000V
 Step          1.0000V

Constants:
 VS     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 60.

$I_D - V_D$ characteristics of W = 20μm NMOS transistor (L = 20μm)



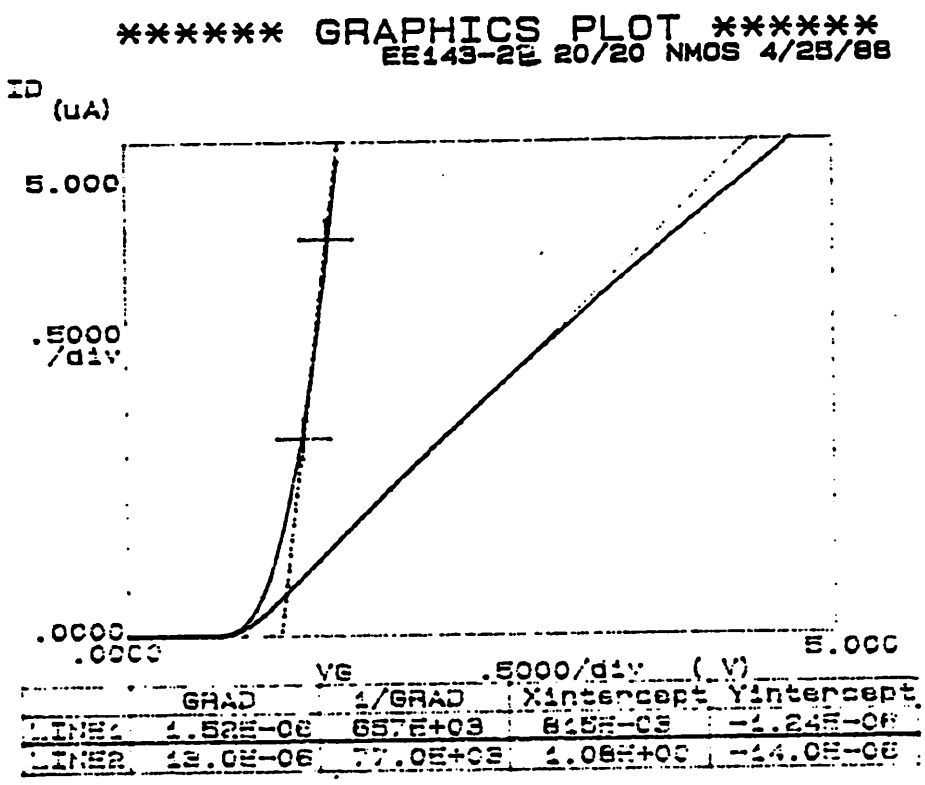

```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step          .0500V

Variable2:
 VSUB   -Ch3
 Start          .0000V
 Stop         -2.0000V
 Step         -1.0000V

Constants:
 VD     -Ch1    .0500V
 VS     -Ch2    .0000V
```

Figure 61.

I_D vs. V_G of W = 20μm NMOS transistor at varying substrate bias, V_D = 50mV



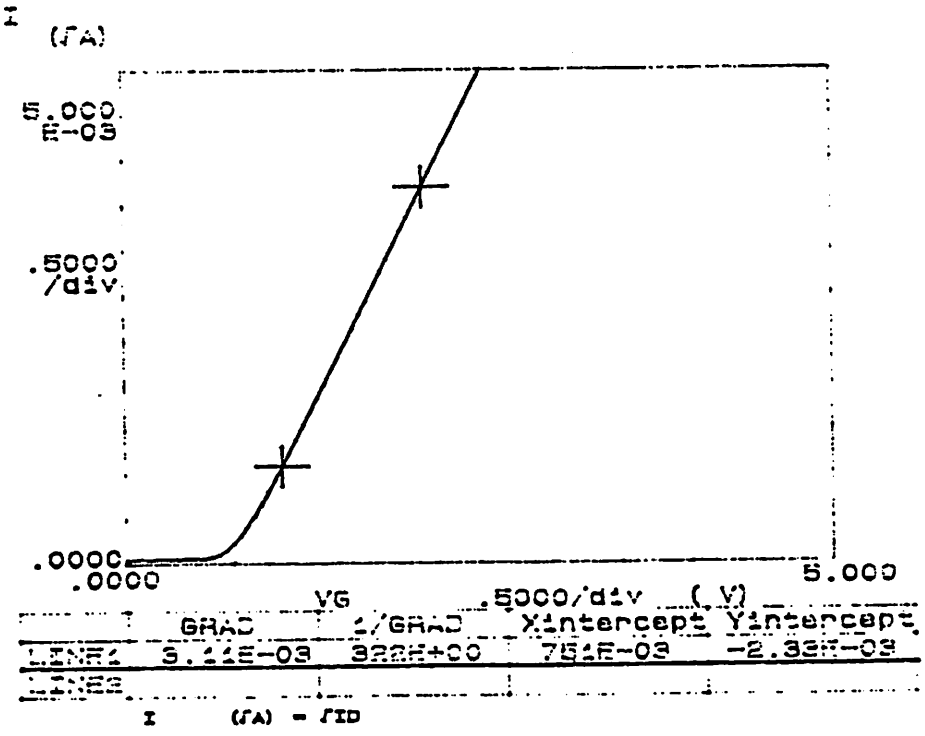

```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VD     -Ch1
 Start          .0500V
 Stop          5.0490V
 Step          5.0000V

Constants:
 VB     -Ch2    .0000V
 VSUB   -Ch3    .0000V
```

Figure 62.

I_D vs. V_G of W = 20μm NMOS transistor at V_D = 50mV and 5V



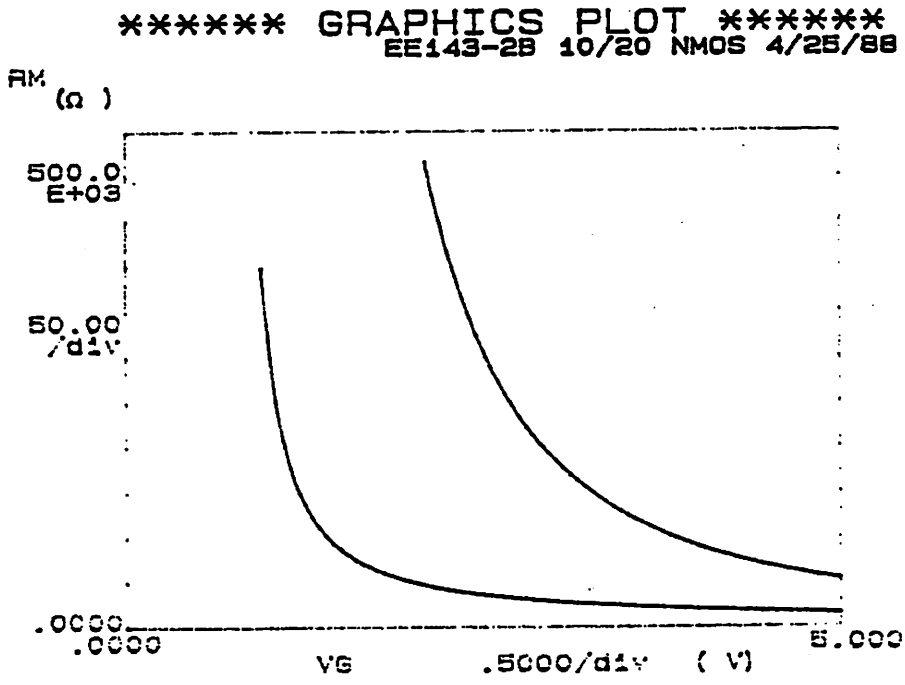

```
Variable1:
 VG     -Ch4
 Linear sweep
 Start          .0000V
 Stop          5.0000V
 Step           .0500V

Variable2:
 VSUB   -Ch3
 Start          .0000V
 Stop           .0000V
 Step           .0000V

Constants:
 VD     -Ch1    5.0000V
 VS     -Ch2    .0000V
```

Figure 63.

$\sqrt{I_D}$ vs. V_G of W = 20μm NMOS transistor at V_D = 5V



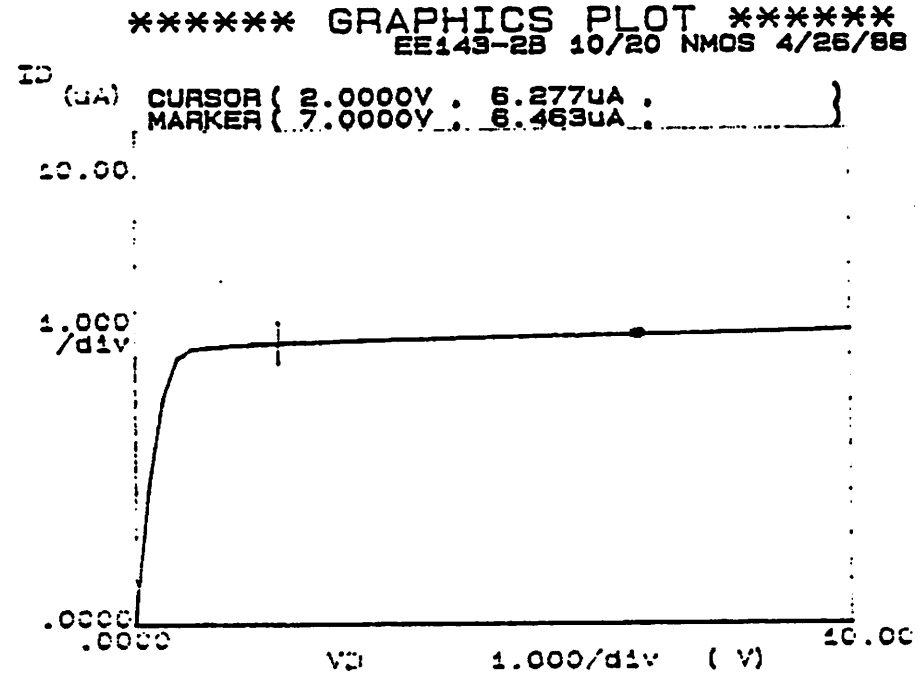
Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VD -Ch1
Start .0500V
Stop 5.0490V
Step 5.0000V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 64.

R_m vs. V_G at V_D = 50mV and 5V for W = 10μm NMOS transistor (W = 15μm)



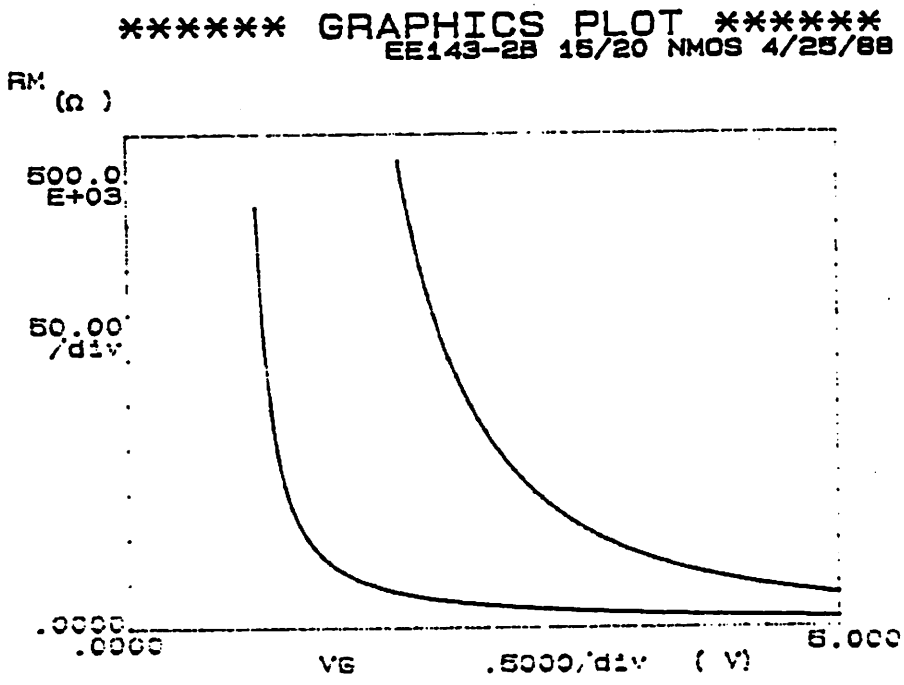
Variable1:
VD -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .2000V

Variable2:
VG -Ch4
Start .0000V
Stop 1.8390V
Step 1.8400V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 65.

I_D vs. V_D at $V_G = V_T + 1$ for W = 10μm NMOS transistor



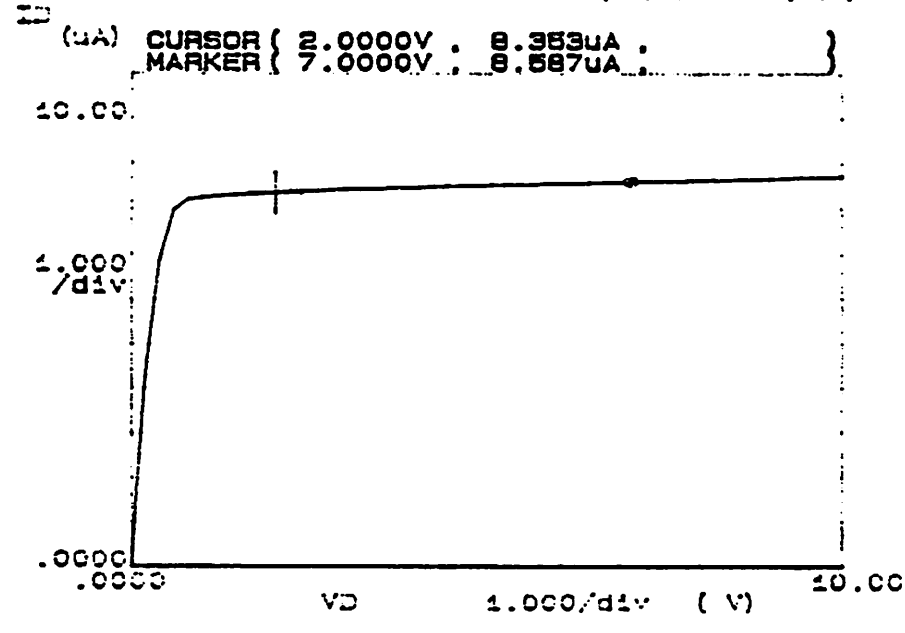
Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VD -Ch1
Start .0500V
Stop 5.0490V
Step 5.0000V

Constants:
VB -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 66.

R_m vs. V_G at V_D = 50mV and 5V for W = 15μm NMOS transistor



Variable1:
VD -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .2000V

Variable2:
VG -Ch4
Start .0000V
Stop 1.8260V
Step 1.8270V

Constants:
VB -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 67.

I_D vs. V_D at $V_G = V_T + 1$ for W = 15μm NMOS transistor

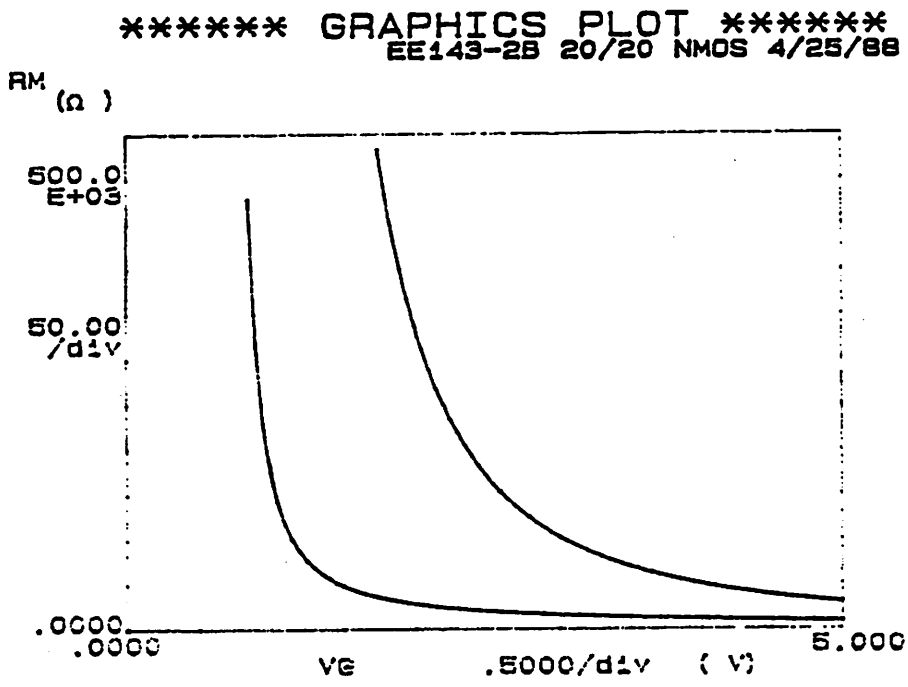


Figure 68.

R_m vs. V_G at V_D = 50mV and 5V for W = 20μm NMOS transistor

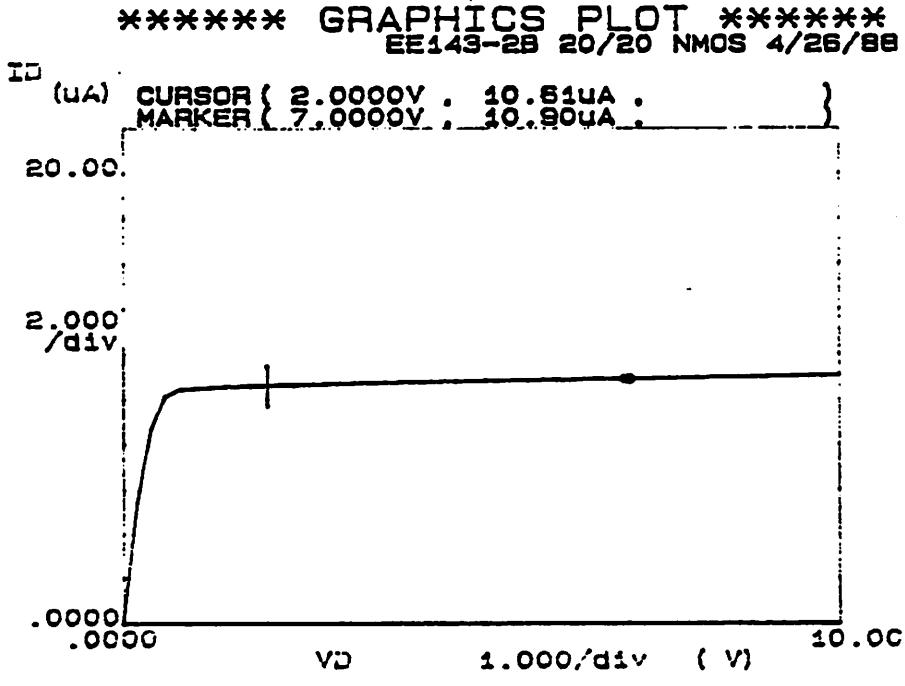


Figure 69.

I_D vs. V_D at $V_G = V_T + 1$ for W = 20μm NMOS transistor

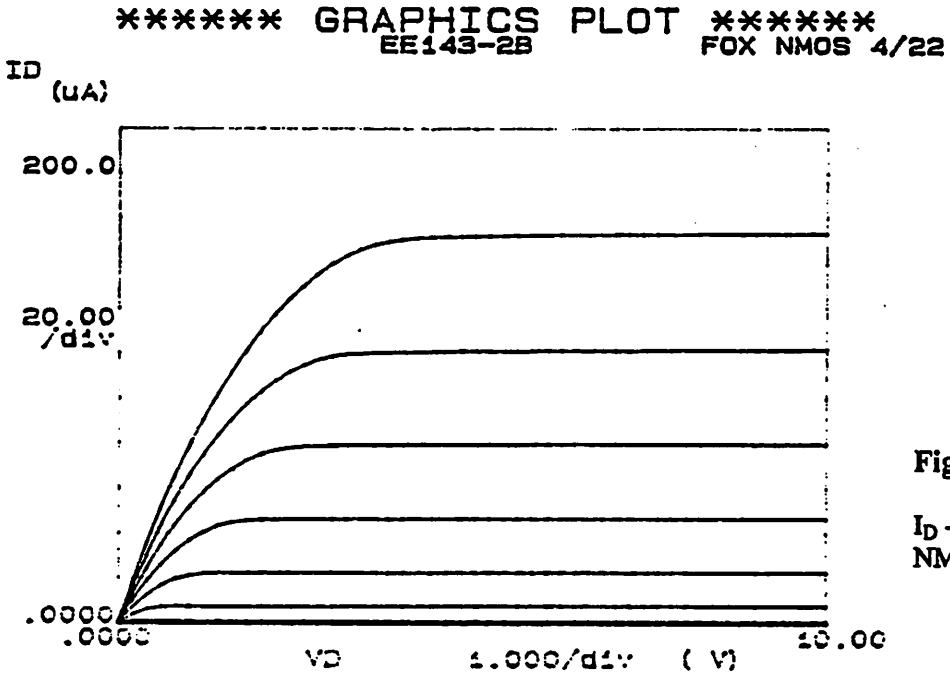


Figure 70.

I_D - V_D characteristics of field oxide NMOS transistor

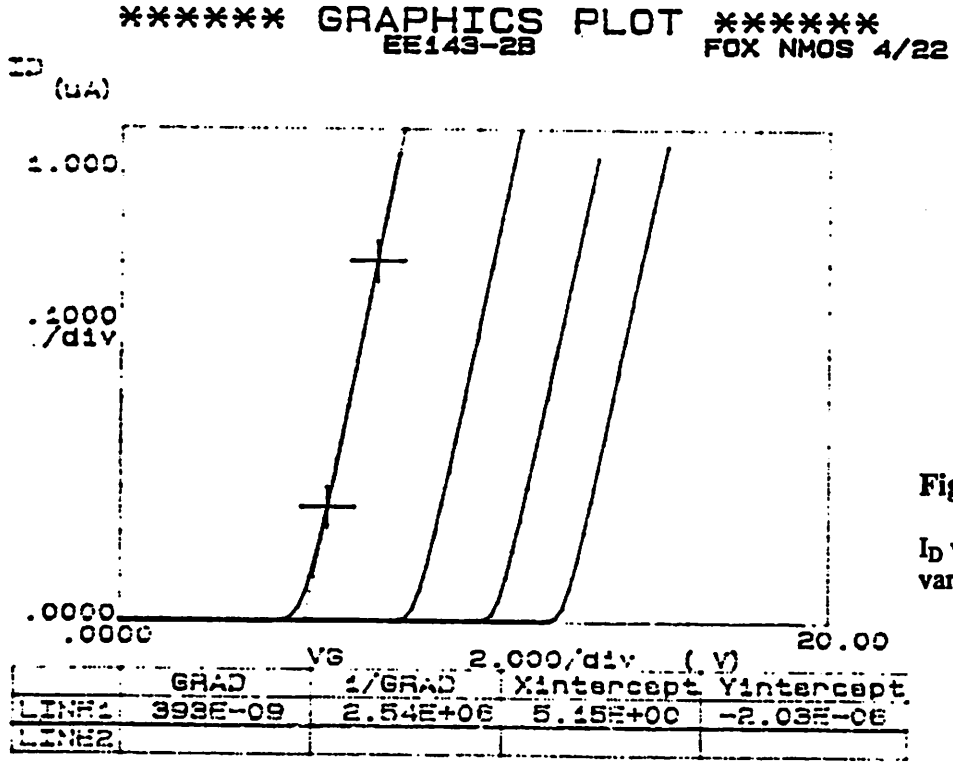


Figure 71.

I_D vs. V_G of field oxide NMOS at varying substrate bias

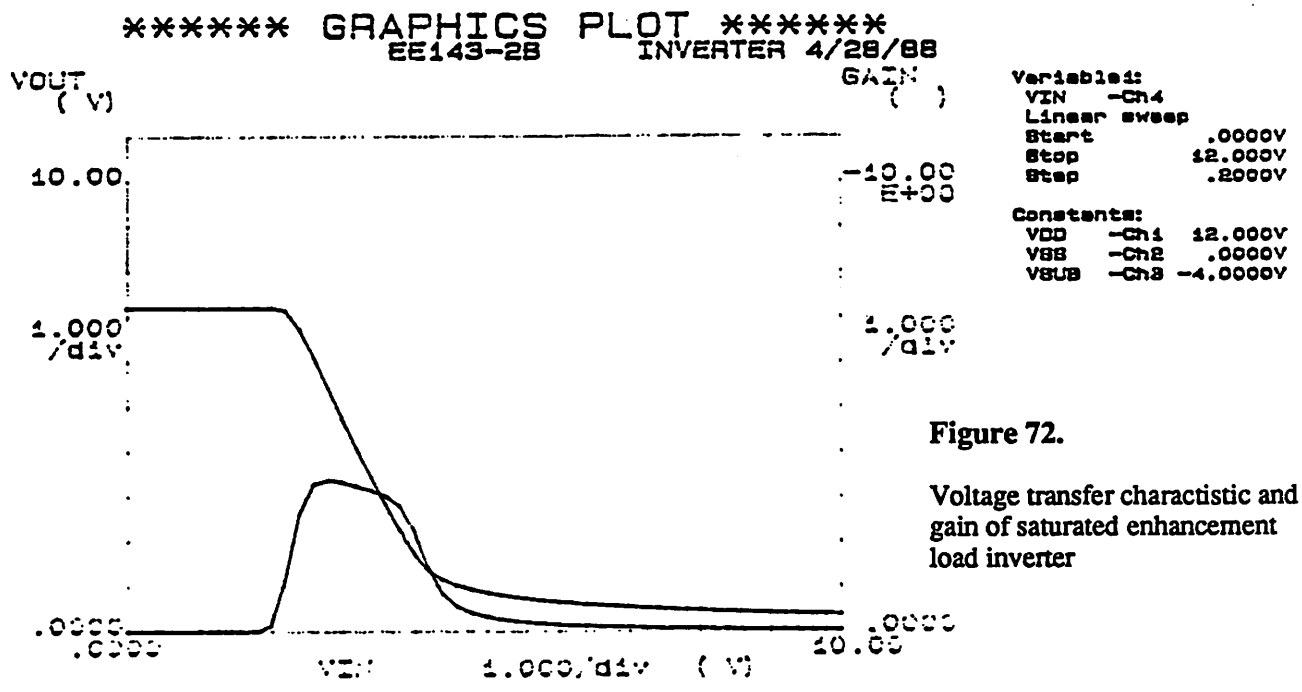


Figure 72.

Voltage transfer charactistic and gain of saturated enhancement load inverter

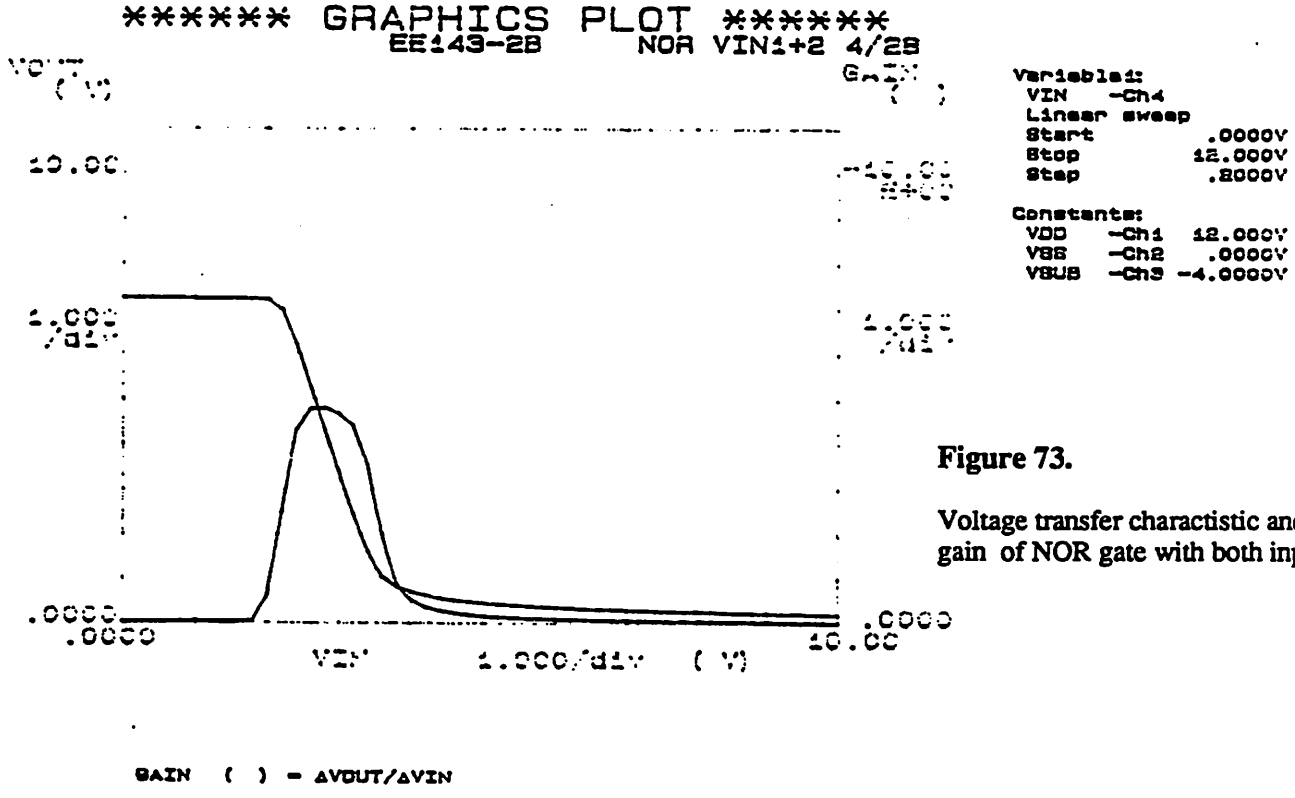


Figure 73.

Voltage transfer charactistic and gain of NOR gate with both inputs on

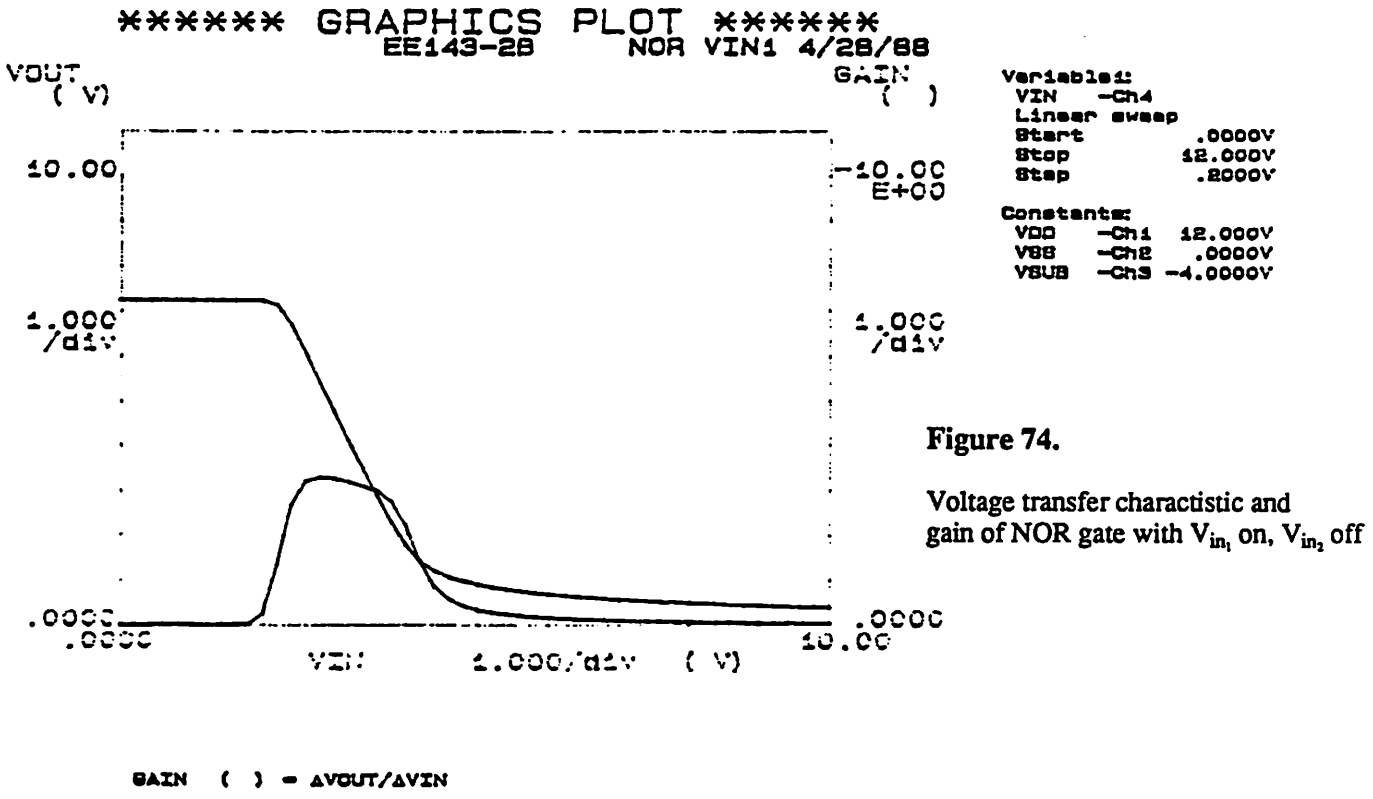


Figure 74.

Voltage transfer charactistic and gain of NOR gate with V_{in_1} on, V_{in_2} off

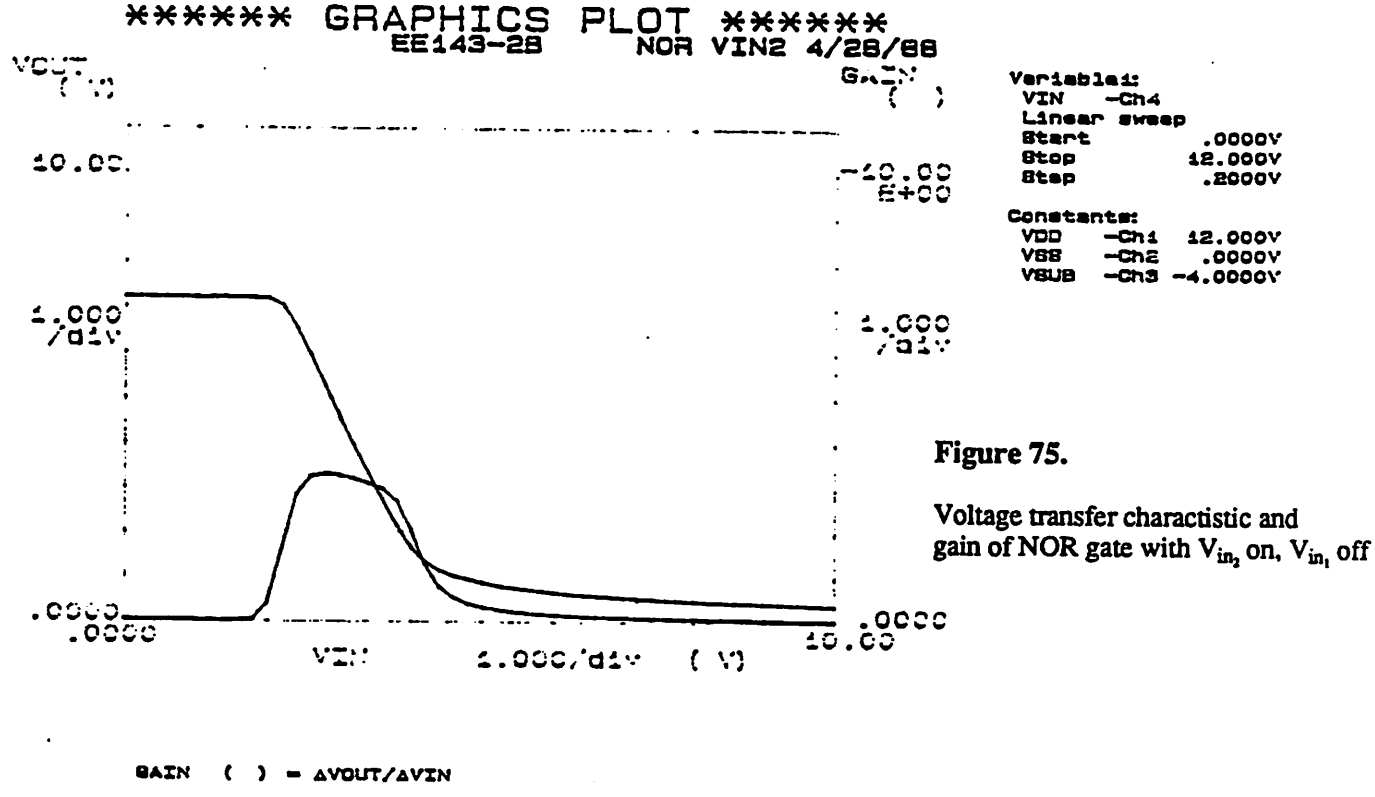


Figure 75.

Voltage transfer charactistic and gain of NOR gate with V_{in_2} on, V_{in_1} off

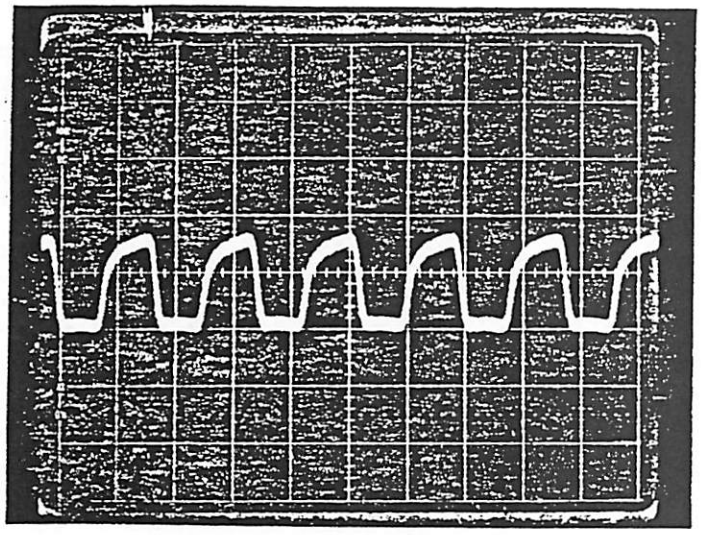


Figure 76.

Transient response of 21 stage ring oscillator at V_{DD} = 12V, V_B = -5V

Vertical scale: 10mV/div
Horizontal scale: 50 nsec/div

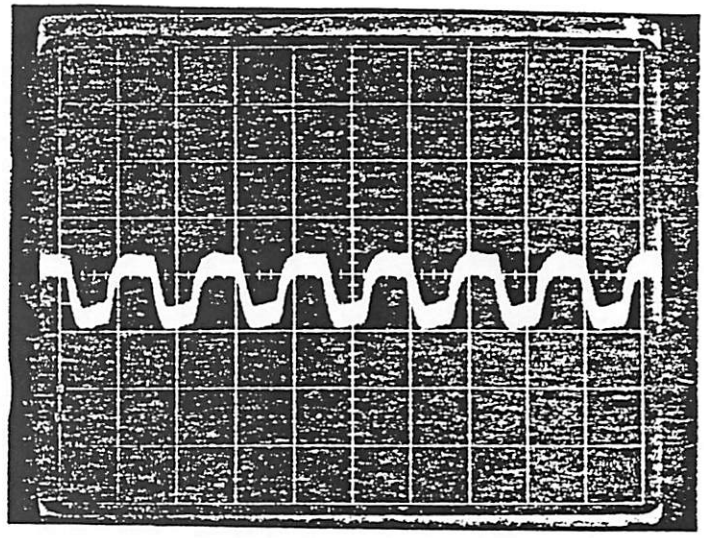


Figure 77.

Transient response of ring oscillator at V_{DD} = 5V, V_B = -1V

Vertical scale: 5mV/div
Horizontal scale: 200 nsec/div

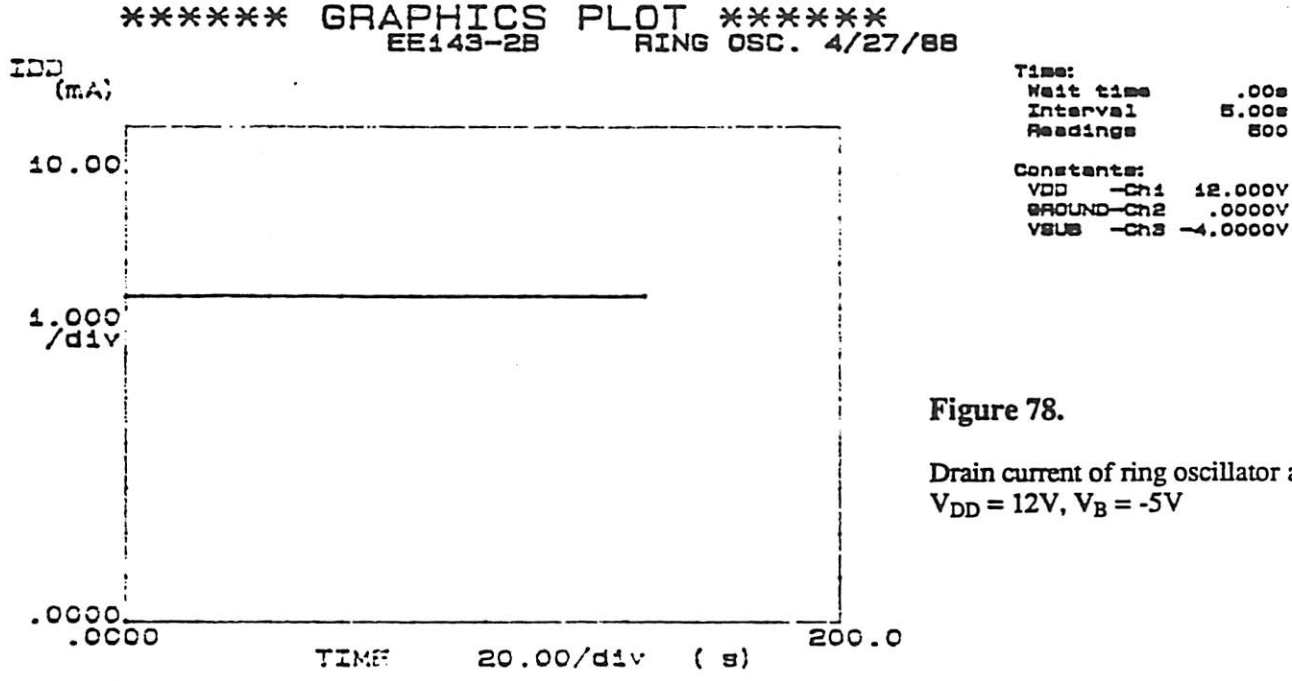


Figure 78.

Drain current of ring oscillator at V_{DD} = 12V, V_B = -5V