BSIM – SUBSTRATE CURRENT MODELING APPENDIX C: IMPLEMENTATION OF THE BSIM SUBSTRATE CURRENT AND DEGRADATION MODELS IN SCALP

by

P. M. Lee, M. M. Kuo, M. Maghsoodnia, P. K. Ko
and C. Hu

Memorandum No. UCB/ERL M87/8

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Degradation model parameters needed for the process file are summarized as follows:

(1) H and n: should be extracted from equation (3) from B's measured at several ΔV_{thf} 's. B is the intercept of the log τ versus log I_{bs} curve (Fig. C1).

(2) m: the ratio of the trap energy and impact ionization energy $\frac{\phi_{it}}{\phi_i}$ which is approximately the slope of the log τ versus log I_{bs} curve (Fig. C1). Typically, m is equal to 2.9 [2].

These parameters should be appended to the process file directly after the substrate current parameters in one row and in the order mentioned above (i.e. H, n, m). Users who do not need any device lifetime information should enter 100, 0.6, and 2.9 for H, n, and m respectively and use the appropriate commands given in section five. Fig. C2 shows the location of all BSIM parameters in the process file for proper SPICE read-in. Fig. C3 shows a sample process file.

4. System Structure and Implementation

This system contains three parts: a pre-processor, the SPICE program, and a post-processor. The two newly developed models are installed in the post-processor and are external to SPICE.

The pre-processor takes an input deck which contains commands given in section four and commands prepared according to the SPICE syntax. SPICE is used in this system to simulate the circuit to determine the transient voltage waveforms at the drain, gate, source, and substrate of all user-selected devices. The post-processor calculates the transient substrate currents by using the node voltages provided by SPICE.

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TITLE PAGE

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1. Introduction

In addition to the substrate current model described in [1], a simple parametric device degradation model has been developed, and these two models have been implemented in SCALP (the Substrate Current And Lifetime Program). SCALP contains a pre- and a post-processor which when used in conjunction with SPICE allows for the simulation of substrate current and device lifetime in analog and digital circuits. No modification to the original SPICE code is necessary for this implementation; consequently the SCALP simulator can be used with minimal setup time and works independently of the specific models implemented in SPICE. Using SCALP and SPICE together as a simulator system, the circuit designer can isolate areas within his circuit susceptible to adverse hot-electron and degradation effects.

The following sections will introduce the degradation model, summarize the basic operation of this new simulator system, describe its internal structures, and offer a guide to users wanting to implement these models in their circuit simulations.

Users who are not interested in using the degradation model in their circuit simulation may skip the following section and go directly to section three.

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2. Degradation Model

2.1 Basic Equations

Device degradation is typically measured by the amount of threshold voltage shift (ΔV_{th}) that occurs. Other parameters, e.g. $\Delta I_d \,/\, I_{do}$, may be used to characterize device degradation. In that case, ΔV_{th} in the equations below should be replaced by, for example, $\Delta I_d \,/\, I_{do}$. In DC static stressing, the device lifetime can be modeled by two basic equations dependent on I_{ds}, I_{bs}, and other parameters [2]:

$$\Delta V_{th} = At^n \qquad (1)$$

$$\tau = WBI_{bs}{}^{-m} I_{ds}{}^{m-1} \qquad (2)$$

$$m = \frac{\phi_{it}}{\phi_i}$$

$$B = H\,\Delta V_{thf}{}^{\frac{1}{n}} \qquad (3)$$

where n , m and H are extracted parameters and H is dependent on device processing technology. ΔV_{thf} is the amount of shift in threshold voltage defined at device failure. W is the device width, τ is the device lifetime, and $q\phi_i$ and $q\phi_{it}$ are the critical energies required for impact ionization and the creation of interface traps, respectively. A typical log - log plot of τ versus I_{bs} is shown in Fig. C1. These equations can then be combined with numerical calculations to find device lifetime.

2.2 Theoretical Analysis

Using a quasi-static analysis, equations (1) and (2) can be extended to model the dynamic stressing behavior in a circuit for which the substrate current of a device is a function of time. Let $\Delta V_{thf} = \Delta V_{th}\,|_{t=\tau}$ be the threshold voltage shift defined at device failure. By solving for A in equation (1) using equation (2), we get:

$$\Delta V_{thf} = A\tau^n = A[WBI_{bs}{}^{-m} I_{ds}{}^{m-1}]^n$$
$$A = \Delta V_{thf}[WBI_{bs}{}^{-m} I_{ds}{}^{m-1}]^{-n}$$

Thus equation (1) becomes

$$\Delta V_{th} = \Delta V_{thf}(WB)^{-n} I_{bs}{}^{mn} I_{ds}{}^{n(1-m)} t^n$$

or

$$\Delta V_{th}{}^{\frac{1}{n}} = \Delta V_{thf}{}^{\frac{1}{n}}(WB)^{-1} I_{bs}{}^m I_{ds}{}^{(1-m)} t$$
$$= (WH)^{-1} I_{bs}{}^m I_{ds}{}^{(1-m)} t \qquad (4)$$

Since $\Delta V_{th}{}^{\frac{1}{n}}$ is a linear function of time, this quantity can simply be summed over the time period of the SPICE analysis. If $t_0, \ldots, t_P$ are the individual time points of SPICE, then

$$[\Delta V_{th(tot)}]^{\frac{1}{n}} = [\Delta V_{th}(t_1 - t_0)]^{\frac{1}{n}} + \cdots + [\Delta V_{th}(t_P - t_{P-1})]^{\frac{1}{n}}$$

Moreover, to find the device lifetime assuming a periodic signal, a simple linear extrapolation in terms of $\Delta V_{th}{}^{\frac{1}{n}}$ is all that is necessary. The number of time intervals of the SPICE analysis needed so that $\Delta V_{th} = \Delta V_{thf}$ is simply

$$N = [\frac{\Delta V_{thf}}{\Delta V_{th(tot)}}]^{\frac{1}{n}}$$

Thus, if the length of the SPICE analysis is $t_P = T$ and is equal to the period of the signal, the lifetime is found from

$$\tau = NT$$
$$= T[\frac{\Delta V_{thf}}{\Delta V_{th(tot)}}]^{\frac{1}{n}}$$

or

$$\tau = \frac{TWH\,\Delta V_{thf}{}^{\frac{1}{n}}}{\sum_{h=1}^{P}[I_{bs}(t_h)]^m[I_{ds}(t_h)]^{1-m}(t_h - t_{h-1})} \qquad (5)$$

3. Process File:

Degradation model parameters needed for the process file are summarized as follows:

(1) H and n: should be extracted from equation (3) from B's measured at several ΔV_{thf}'s. B is the intercept of the log τ versus log I_{bs} curve (Fig. C1).

(2) m: the ratio of the trap energy and impact ionization energy $\frac{\phi_{it}}{\phi_i}$ which is approximately the slope of the log τ versus log I_{bs} curve (Fig. C1). Typically, m is equal to 2.9 [2].

These parameters should be appended to the process file directly after the substrate current parameters in one row and in the order mentioned above (i.e. H, n, m). Users who do not need any device lifetime information should enter 100, 0.6, and 2.9 for H, n, and m respectively and use the appropriate commands given in section five. Fig. C2 shows the location of all BSIM parameters in the process file for proper SPICE read-in. Fig. C3 shows a sample process file.

4. System Structure and Implementation

This system contains three parts: a pre-processor, the SPICE program, and a post-processor. The two newly developed models are installed in the post-processor and are external to SPICE.

The pre-processor takes an input deck which contains commands given in section four and commands prepared according to the SPICE syntax. SPICE is used in this system to simulate the circuit to determine the transient voltage waveforms at the drain, gate, source, and substrate of all user-selected devices. The post-processor calculates the transient substrate currents by using the node voltages provided by SPICE.

For the SPICE analysis, the user is free to choose any one of the models available in SPICE for the circuit simulation. To avoid confusion, from here on we shall refer to the SPICE2 BSIM model as "BSIM2", other SPICE2 models as "SPICE2", the SPICE3 BSIM model as "BSIM3", and other SPICE3 models as "SPICE3". Besides the basic tasks, the operations of the pre- and post- processors differ somewhat for the BSIM2, BSIM3, SPICE2, and SPICE3 users. This was necessary because BSIM2 reads in the process file created by the BSIM extraction program directly whereas BSIM3, SPICE2, and SPICE3 need .MODEL commands with all parameters appended to the input deck. The system configuration was designed to retain as much commonality as possible between the two schemes (see Figs. C4 and C5). The *rawsub* and *RAWMODEL* files are created for communication between the two processors and for storing model parameters. The *RAWPROC* files are the new process files created when BSIM2 is used. All these intermediate files are removed at the end of the simulation. More detailed discussion will be given below.

4.1 Structure of the Pre-Processor:

The program name for the pre-processor is "prescalp.c". All global variables used by this program are declared in "BSIMpredefs.h". Other associated program names needed for compilation are "ACdefs.h", "CKTdefs.h", "FTEconstant.h", "FTEwritedata.h", "GENdefs.h", "INPdefs.h", "NIdefs.h", "OUTinterface.h", "Proc2ModSub.c", "SMPdefs.h", "SPerror.h", "TRCVdefs.h", "prefix.h", "suffix.h", "util.h", and "version.h". The program "prescalp.c" contains six main routines. The functions of these main routines are described below:

(1) *PreFilter*:

This routine scans the entire input file to determine the number of transistors in the circuit, the number of process files given, and the number of transistors given in the .PRINT or .PLOT ISUB commands. This is done in order to allocate the proper amount of memory spaces for data storage.

(2) *FindProc*:

The .PROCESS control line is searched for to obtain the process file name. For each process file given, a corresponding model file is created which contains all the process parameters with the substrate current and degradation parameters commented out. When BSIM2 is used, a new process file is created which is identical to the original process file except the new process parameters are commented out. The filenames for the model file and the new process file are *RAWMODEL* 0 and *RAWPROC* 0 respectively. When more than one process file is given, *RAWPROC* 1, *RAWPROC* 2, etc., will be created.

(3) *FindWidth*, *FindTran*, *FindOption*:

FindWidth and FindTran search for the .ISUBWIDTH and .TRAN control lines and store these information in the rawsub file. The FindOption routine looks for the relevant information (i.e. DEFL, DEFW, NOMOD, etc.) that may appear in the .OPTIONS command.

(4) *CreateInpFile*:

The filtered input deck for SPICE is created in this routine. All non-SPICE-compatible commands are commented out, and the appropriate .PRINT node voltages commands are added to the input deck. Information pertaining to the user-selected transistors are stored in the *rawsub* file. For BSIM2 users, the filename in the .PROCESS control line is changed to *RAWPROC* 0; for BSIM3 users, the *RAWMODEL* file is appended to the input deck, and the .PROCESS command is deleted by the pre-processor; for SPICE2 and SPICE3 users, the .PROCESS command is deleted. All of these are done to maintain compatibility with the different versions of the SPICE codes.

4.2 Structure of the Post-Processor:

The code for the post-processor is stored in "scalp.c", and all global variables are defined in "BSIMpostdefs.h". This program is divided into two main sections. The first part reads in all transistor information from the *rawsub* and the *RAWMODEL* files and stores them. The second part reads in the voltage values from SPICE, calculates the substrate current and device lifetime, and prints the output. Several main functions from this part will be discussed here.

(1) *AddSubParam*:

If either SPICE2 or BSIM2 is being run and the NOMOD option is not present in the .OPTIONS control line as determined by the pre-processor earlier, then the substrate current parameters are appended to the model information section of the SPICE output.

(2) *ReadVoltage*:

This routine is used to search the right set of output voltages from SPICE for the user-selected transistors. This routine is dependent on the SPICE output format in its search and therefore may need modification if SPICE output format is changed.

(3) *BSIMevaluate*:

The BSIM substrate current model is implemented is this routine. Given all the process parameters and specified node voltages, this routine calculates the substrate current.

(4) *BSIMDeltaVth*, *EvaluateLifetime*:

Implementation of the degradation model is done in these two routines. Device lifetime is calculated based on the transient substrate current.

(5) *SubOutput*, *PrintLifetime*:

These two routines are responsible for the printing and plotting of the substrate current and the device lifetime.

5. User's Guide for the Processors

Since the input format for SPICE3, SPICE2, BSIM2 and BSIM3 are all different, the user needs to pay special attention to the command syntax that is applicable to his use. The following new commands have been added for substrate current and degradation analysis:

```
.PRINT  ISUB(MXXX)  <ISUB(MXXX) ... ISUB(MXXX) >
.PRINT  ISUB(SXXX)  <ISUB(SXXX) ... ISUB(SXXX) >
.PLOT  ISUB(MXXX)  <ISUB(MXXX) ... ISUB(MXXX) >  <(MIN,MAX) >
.PLOT  ISUB(SXXX)  <ISUB(SXXX) ... ISUB(SXXX) >  <(MIN,MAX) >
```

Examples:

```
    .PLOT  ISUB(S1)  ISUB(S4)  (0,7E-6)
    .PRINT  ISUB(M1)  ISUB(M4)  ISUB(M5)
```

These control lines are used to either print or plot out the substrate current. The device lifetime is always printed out following the output of the corresponding substrate current unless otherwise specified. The sums of the specified substrate current for the NMOS and PMOS devices are also automatically printed out. This is a good test to determine if the substrate-bias generator will be overloaded by the substrate current. SXXX is a syntax following the BSIM2 convention and should be used for both BSIM2 and SPICE2, while MXXX is used for SPICE3 and BSIM3. MIN and MAX are optional parameters specifying the minimum and maximum substrate current to be plotted.

```
.ISUBALL
```

This command will enable the SCALP simulator to provide the sums of the substrate current for all MOS devices in the circuit regardless of transistors specified in the .PRINT or .PLOT ISUB command.

.ISUBONLY

This command should be used if the user is not interested in the device lifetime calculation. When this command is given, only the substrate current information is provided by the SCALP simulator.

.AGE

When the user wishes to know the lifetimes of all devices in the circuit, this command can be given. This command overrides the .ISUBONLY command and can be used together with the .PRINT or .PLOT ISUB command.

.ISUBWIDTH=COLWIDTH

Examples:

```
.ISUBWIDTH=80

.ISUBWIDTH=100
```

This command controls the width of the substrate current output printout. This is independent of the usual .WIDTH or .OPTIONS WIDTH command used in SPICE. Permissible values for COLWIDTH range from 80 to 200. The default value is 132. In SPICE3 or BSIM3, all non-substrate current analysis printout is outputted in 90 column format, regardless of the .OPTIONS WIDTH command. This was done to insure proper voltage read-in when none of the four nodes of the specified transistor is grounded.

.DELTAVT VALUE

Examples:

```
.DELTAVT 10MV

.DELTAVT 900UV
```

This control line is used for setting the amount of threshold voltage shift defined at device failure. The calculation of device lifetime is based.on this given value.

```
.TRAN TSTEP TSTOP <TSTART>
```

Examples:

```
    .TRAN 1NS 100NS

    .TRAN 5NS 1000NS 2NS
```

Since this simulator system is designed to calculate the transient substrate currents, the SPICE .TRAN command should always be included whenever this system is used. In order for the calculated device lifetime to be meaningful, the difference between TSTOP and TSTART should equal to a multiple of the period of the input signal.

```
.PROCESS PNAME FILENAME=FNAME
```

Examples:

```
    .PROCESS PC1 FILENAME=RUN

    .PROCESS MK1 FILENAME=MMK
```

This control line specifies the process name and the corresponding process file name which contains all the process parameters. The format is identical to that already implemented in BSIM2, but it is new for SPICE2, SPICE3 and BSIM3. It is important to realize that ".MODEL" commands are no longer necessary for BSIM3, but that a ".PROCESS" command is now mandatory.

General form for MOSFETs:

```
SXXXXXXX ND NG NS NB <MNAME> PNAME_MT_DT <L=VAL> <W=VAL> ... etc.

MXXXXXXX ND NG NS NB <MNAME> PNAME_MT_DT <L=VAL> <W=VAL> ... etc.
```

Examples:

```
    S1 1 2 3 4 MODN PC1_NM1_DU1 L=1U W=20U

    S1 1 2 3 4 PC1_NM1_DU1 L=1U W=20U

    M1 1 2 3 4 MODP PC3_PM1_DU2 L=10U W=5U AD=100P AS=100P
```

```
+ PD=40U  PS=40U
```

To describe a MOSFET, the user should use SXXXXXXX for BSIM2 or SPICE2, MXXXXXXX for BSIM3 or SPICE3. MNAME is the model name which should be given only if SPICE2 or SPICE3 is used. PNAME_MT_DT should be given regardless of the type of model used in the SPICE analysis. PNAME is the process name which must be specified in a .PROCESS command. MT is the mos type. The possible choices are NM1 to NM5, and PM1 to PM5. DT is the source/drain junction diffusion type. DU1 to DU3 ar the three available diffusion types with DU1 used as the default value. For users who are not familiar with SPICE commands, please consult the manual for SPICE. For users who wish to learn more about the BSIM model implemented in SPICE or about the BSIM extraction program, please refer to "SPICE IMPLEMENTATION OF BSIM"[3] or "BSIM PARAMETER EXTRACTION - ALGORITHMS AND USER'S GUIDE"[4].

In an UNIX environment, the commands for compilation are:

```
cc -o prescalp prescalp.c -lm
cc -o scalp scalp.c -lm
```

where "prescalp" and "scalp" are the names of the executable files and "prescalp.c" and "scalp.c" are the names of the programs. To execute the programs, the command is:

```
prescalp -x -y deck | spice | scalp > outfile
```

where x is "b" if the BSIM model is used in the SPICE analysis, or "o" if other model is used, y is either "2" or "3" depending on whether SPICE2/BSIM2 or SPICE3/BSIM3 is used, "deck" is the input deck file, "spice" is the name of the executable version of the SPICE program the user is using, and "outfile" is the output file desired. If no "-x" option is specified, the BSIM model is assumed to be used; if no "-y" option is given, the simulator defaults to SPICE2/BSIM2.

Figs. C6 and C7 illustrate sample BSIM2 and BSIM3 input decks respectively for a

CMOS EEPROM sense amplifier shown in Fig. C8. M1 and M7 are EEPROM reference and memory cells, and M3 and M5 are the sense amplifier's NMOS devices of which substrate current simulations are requested. The essential difference between the two input decks is the BSIM transistor designations (SXXX for BSIM2, MXXX for BSIM3). Fig. C9 shows the resulting output for BSIM2 with a 5 volt input pulse of 4ns rise and fall time, and 25ns pulse width applied at $V_{in} = V(6)$ at $t = 0$ns. Output for BSIM3 is virtually identical to the one shown here.

In a VMS environment, the following steps should be executed to assure a proper operation of the simulator.

(1) loading the files :

If the user has the files ready in a Unix or Ultrix environment, he can use the magnetic tape or the DECnet file transfer program (dcp) to transfer the files to a VMS environment. The dcp command is:

```
dcp filename "machine/node/password::[node.directory]filename.extension".
```

Transfer of files from VMS to Unix is done with the same "dcp" command or the "rcp" command. Refer to the help command on VMS for more explanation of the "rcp" command.

(2) compilation and execution :

Two command files have been created to facilitate these processes. The command file for compilation is stored under the name "compile.com", and the one for running the processors is stored under the name "processor.com". To compile the two processors, give this command:

```
@compile
```

To use the SCALP simulator system, the following command should be executed:

```
@processor prescalp -x -y deck spice scalp outfile
```

where "@processor" initiates the execution of the "processor.com" file, and "prescalp -x -y deck spice scalp outfile" is similar to the one used in the UNIX environment with the only difference being that no " | ", " < ", and " > " characters are involved here. Since the explanation for the command "prescalp -x -y deck spice scalp outfile" has been provided earlier, it will be not be given here again.

REFERENCES

[1] P.M. Lee, "BSIM - Substrate Current Modeling," University of California, Berkeley, ERL Memo, UCB/ERL M86/49.

[2] C. Hu, S. Tam, F-C Hsu, P.K. Ko, T.Y. Chan, and K.W. Terrill, "Hot-Electron-Induced MOSFET Degradation - Model, Monitor, Improvement," IEEE Trans. Electron. Devices, Vol. ED-32, pp. 375-385, February 1985.

[3] B.J. Sheu, D.L. Scharfetter, and P.K. Ko, "SPICE2 Implementation of BSIM", University of California, Berkeley, ERL memo, UCB/ERL M85/42.

[4] M.C. Jeng, B.J. Sheu, and P.K. Ko, "BSIM Parameter Extraction - Algorithms and User's Guide", University of California, Berkeley, ERL memo, UCB/ERL M85/79.

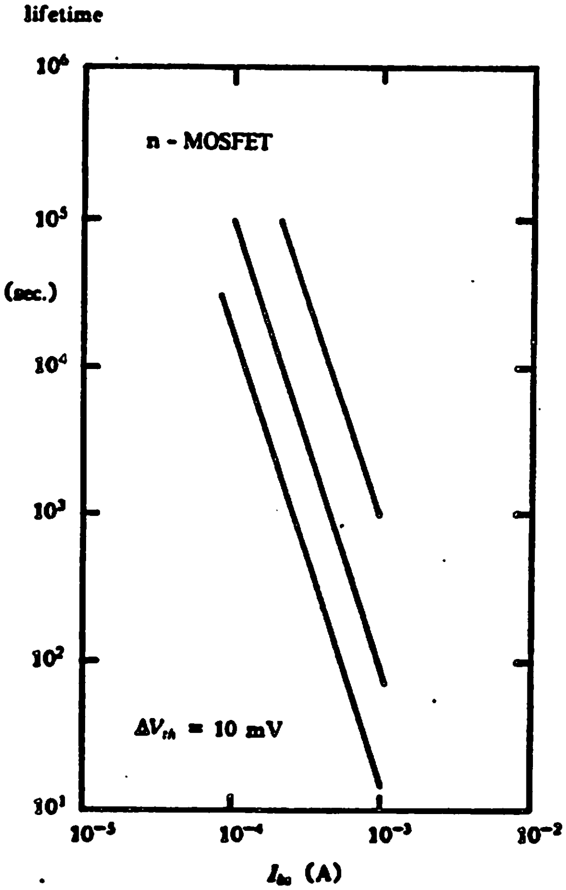
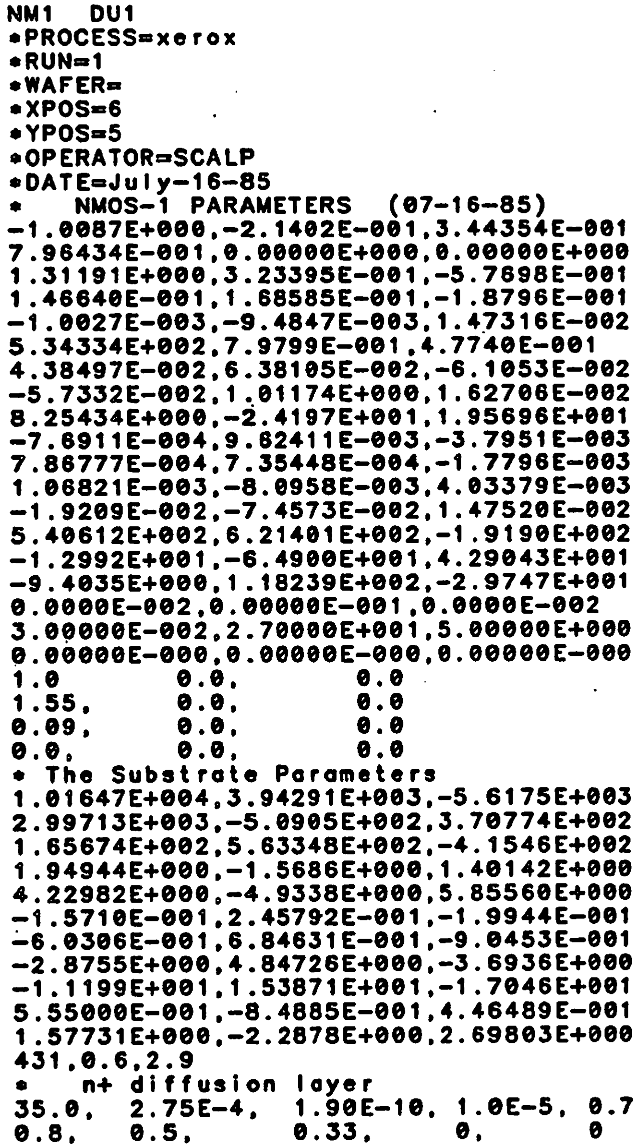


Fig. C1 Typical log - log plots of device lifetime τ versus I_{bs} for various device technologies (from Hu et al [1]).

	Name	L sens. factor	W sens. factor	Units of basic parameter
1	V_{FB} (VFB)	V_{FBl} (LVFB)	V_{FBw} (WVFB)	V
2	ϕ_S (PHI)	ϕ_{Sl} (LPHI)	ϕ_{Sw} (WPHI)	V
3	K_1 (K1)	K_{1l} (LK1)	K_{1w} (WK1)	$V^{1/2}$
4	K_2 (K2)	K_{2l} (LK2)	K_{2w} (WK2)	-
5	$\vec{\eta}_0$ (ETA)	η_{0l} (LETA)	η_{0w} (WETA)	-
6	μ_Z (MUZ)	δ_l (DL)	δ_w (DW)	cm^2/V-s, μm, μm
7	U_{0Z} (U0)	U_{0Zl} (LU0)	U_{0Zw} (WU0)	V^{-1}
8	U_{1Z} (U1)	U_{1Zl} (LU1)	U_{1Zw} (WU1)	μm V^{-1}
9	μ_{ZB} (X2MZ)	μ_{ZBl} (LX2MZ)	μ_{ZBw} (WX2MZ)	cm^2/V^2-s
10	η_B (X2E)	η_{Bl} (LX2E)	η_{Bw} (WX2E)	V^{-1}
11	η_D (X3E)	η_{Dl} (LX3E)	η_{Dw} (WX3E)	V^{-1}
12	U_{0B} (X2U0)	U_{0Bl} (LX2U0)	U_{0Bw} (WX2U0)	V^{-2}
13	U_{1B} (X2U1)	U_{1Bl} (LX2U1)	U_{1Bw} (WX2U1)	μm V^{-2}
14	μ_S (MUS)	μ_{Sl} (LMS)	μ_{Sw} (WMS)	cm^2/V^2-s
15	μ_{SB} (X2MS)	μ_{SBl} (LX2MS)	μ_{SBw} (WX2MS)	cm^2/V^2-s
16	μ_{SD} (X3MS)	μ_{SDl} (LX3MS)	μ_{SDw} (WX3MS)	cm^2/V^2-s
17	U_{1D} (X3U1)	U_{1Dl} (LX3U1)	U_{1Dw} (WX3U1)	μm V^{-2}
18	T_{ox} (TOX)	T_{emp} (TEMP)	V_{dd} (VDD)	μm, °C, V
19	CGDO	CGSO	CGBO	F/m
20	XPART	DUM1	DUM2	-
21	N0	LN0	WN0	-
22	NB	LNB	WNB	-
23	ND	LND	WND	-
24	E_{crit0} (ECRIT0)	E_{crit0l} (LECRIT0)	E_{crit0w} (WECRIT0)	V/cm
25	E_{critg} (ECRITG)	E_{critgl} (LECRITG)	E_{critgw} (WECRITG)	1/cm
26	E_{critb} (ECRITB)	E_{critbl} (LECRITB)	E_{critbw} (WECRITB)	1/cm
27	l_{c0} (LC0)	l_{c0l} (LLC0)	l_{c0w} (WLC0)	$\mu m^{1/2}$
28	l_{c1} (LC1)	l_{c1l} (LLC1)	l_{c1w} (WLC1)	$\mu m^{1/2} - V$
29	l_{c2} (LC2)	l_{c2l} (LLC2)	l_{c2w} (WLC2)	$\mu m^{1/2} - V^{-1}$
30	l_{c3} (LC3)	l_{c3l} (LLC3)	l_{c3w} (WLC3)	$\mu m^{1/2}$
31	l_{c4} (LC4)	l_{c4l} (LLC4)	l_{c4w} (WLC4)	$\mu m^{1/2} - V$
32	l_{c5} (LC5)	l_{c5l} (LLC5)	l_{c5w} (WLC5)	$\mu m^{1/2} - V^2$
33	l_{c6} (LC6)	l_{c6l} (LLC6)	l_{c6w} (WLC6)	$\mu m^{1/2}$
34	l_{c7} (LC7)	l_{c7l} (LLC7)	l_{c7w} (WLC7)	$\mu m^{1/2} - V$
35	H	n	m	-,-,-

Fig. C2 BSIM process file format.



```
NM1  DU1
*PROCESS=xerox
*RUN=1
*WAFER=
*XPOS=6
*YPOS=5
*OPERATOR=SCALP
*DATE=July-16-85
*   NMOS-1 PARAMETERS  (07-16-85)
-1.0087E+000,-2.1402E-001,3.44354E-001
7.96434E-001,0.00000E+000,0.00000E+000
1.31191E+000,3.23395E-001,-5.7698E-001
1.46640E-001,1.68585E-001,-1.8796E-001
-1.0027E-003,-9.4847E-003,1.47316E-002
5.34334E+002,7.9799E-001,4.7740E-001
4.38497E-002,6.38105E-002,-6.1053E-002
-5.7332E-002,1.01174E+000,1.62706E-002
8.25434E+000,-2.4197E+001,1.95696E+001
-7.6911E-004,9.62411E-003,-3.7951E-003
7.86777E-004,7.35448E-004,-1.7796E-003
1.06821E-003,-8.0958E-003,4.03379E-003
-1.9209E-002,-7.4573E-002,1.47520E-002
5.40612E+002,6.21401E+002,-1.9190E+002
-1.2992E+001,-6.4900E+001,4.29043E+001
-9.4035E+000,1.18239E+002,-2.9747E+001
0.0000E-002,0.00000E-001,0.0000E-002
3.00000E-002,2.70000E+001,5.00000E+000
0.00000E-000,0.00000E-000,0.00000E-000
1.0        0.0,        0.0
1.55,      0.0,        0.0
0.09,      0.0,        0.0
0.0,       0.0,        0.0
* The Substrate Parameters
1.01647E+004,3.94291E+003,-5.6175E+003
2.99713E+003,-5.0905E+002,3.70774E+002
1.65674E+002,5.63348E+002,-4.1546E+002
1.94944E+000,-1.5686E+000,1.40142E+000
4.22982E+000,-4.9338E+000,5.85560E+000
-1.5710E-001,2.45792E-001,-1.9944E-001
-6.0306E-001,6.84631E-001,-9.0453E-001
-2.8755E+000,4.84726E+000,-3.6936E+000
-1.1199E+001,1.53871E+001,-1.7046E+001
5.55000E-001,-8.4885E-001,4.46489E-001
1.57731E+000,-2.2878E+000,2.69803E+000
431,0.6,2.9
*   n+ diffusion layer
35.0,  2.75E-4,  1.90E-10, 1.0E-5, 0.7
0.8,   0.5,      0.33,     0,      0
```

Fig. C3 Sample BSIM process file

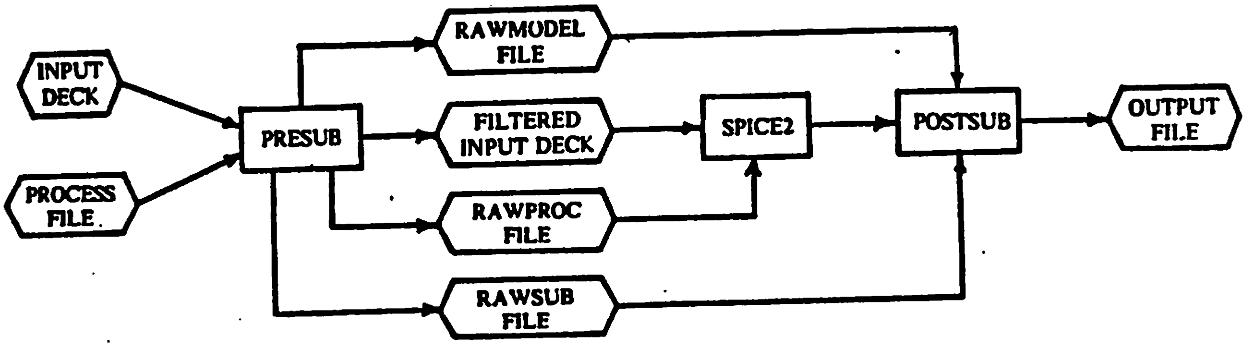


Fig. C4 BSIM2 processor configuration.

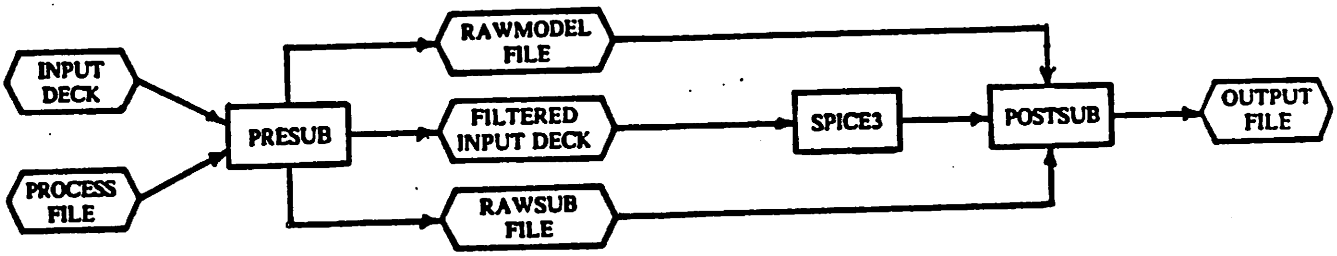


Fig. C5 BSIM3/SPICE2/SPICE3 processor configuration.

```
SIMPLE CMOS SENSE AMPLIFIER
s1 2 5 0 0 PC1_nm1_du1 w=3u l=2u
s2 2 2 5 5 PC1_pm1_du2 w=140u l=2u
s3 3 2 1 0 PC1_nm1_du1 w=20u l=2u
s4 3 2 5 5 PC1_pm1_du2 w=60u l=2u
s5 4 1 0 0 PC1_nm1_du1 w=5u l=2u
s6 4 3 5 5 PC1_pm1_du2 w=10u l=2u
s7 1 6 0 0 PC1_nm1_du1 w=3u l=2u
vdd 5 0 5 dc
vin 6 0 pulse(0,5,0ns,4ns,4ns,25ns,58ns)
.process PC1 filename=PF.SUB
.plot isub(s3) isub(s5)
.deltavt 10mV
c1 1 0 2pf
c2 4 0 0.2pf
.tran 1ns 58ns
.isubwidth=80
.width in=80 out=80
.end
```

Fig. C6 Sample BSIM2 input deck.

```
SIMPLE CMOS SENSE AMPLIFIER
m1 2 5 0 0 PC1_nm1_du1 w=3u l=2u
m2 2 2 5 5 PC1_pm1_du2 w=140u l=2u
m3 3 2 1 0 PC1_nm1_du1 w=20u l=2u
m4 3 2 5 5 PC1_pm1_du2 w=60u l=2u
m5 4 1 0 0 PC1_nm1_du1 w=5u l=2u
m6 4 3 5 5 PC1_pm1_du2 w=10u l=2u
m7 1 6 0 0 PC1_nm1_du1 w=3u l=2u
vdd 5 0 5 dc
vin 6 0 pulse(0,5,0ns,4ns,4ns,25ns,58ns)
.process PC1 filename=PF.SUB
.plot isub(m3) isub(m5)
.deltavt 10mV
c1 1 0 2pf
c2 4 0 0.2pf
.tran 1ns 58ns
.isubwidth=80
.end
```

Fig. C7 Sample BSIM3 input deck.

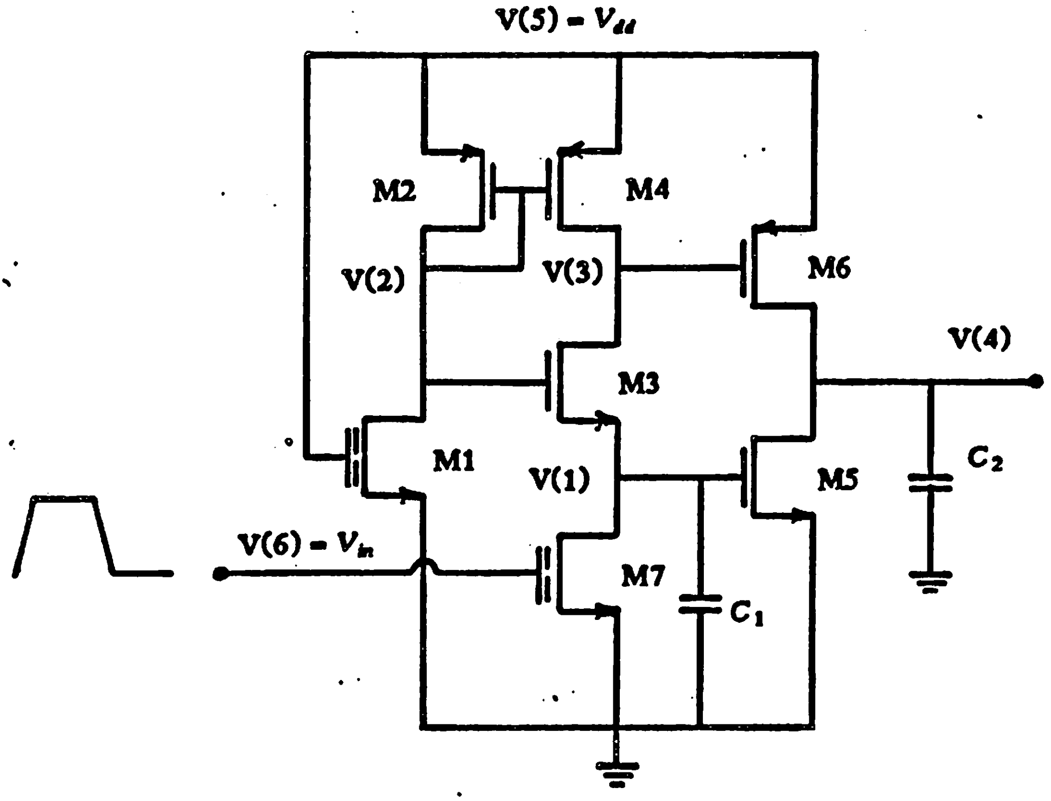
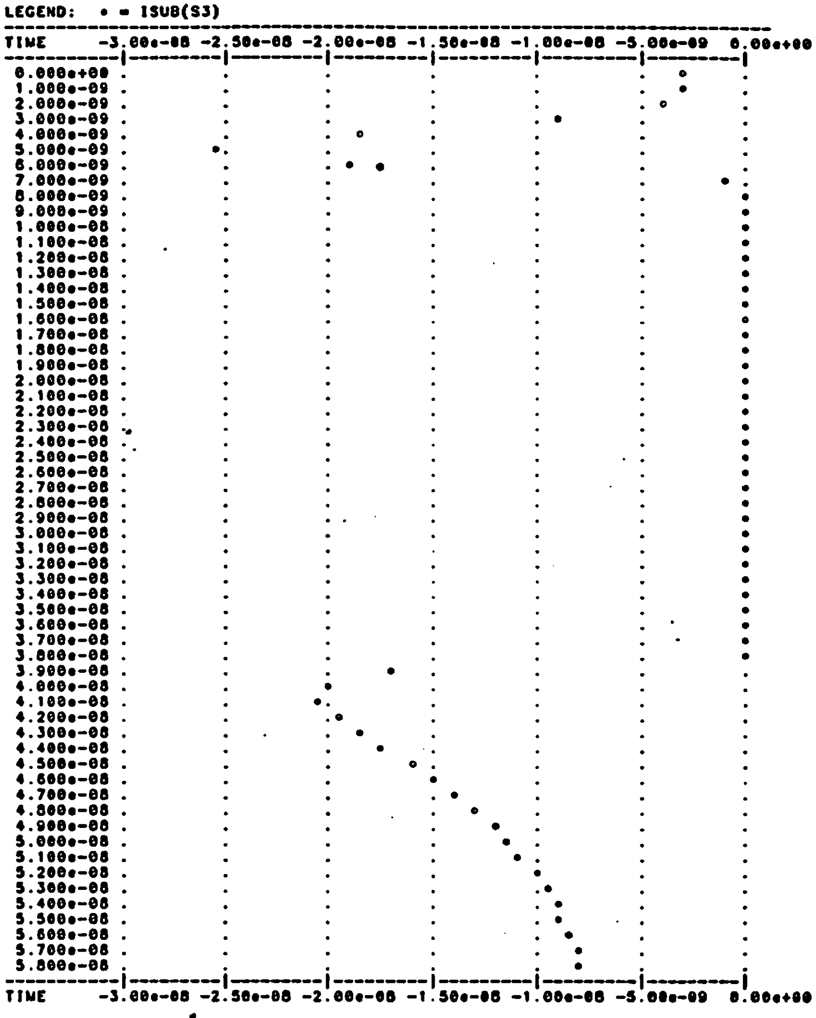


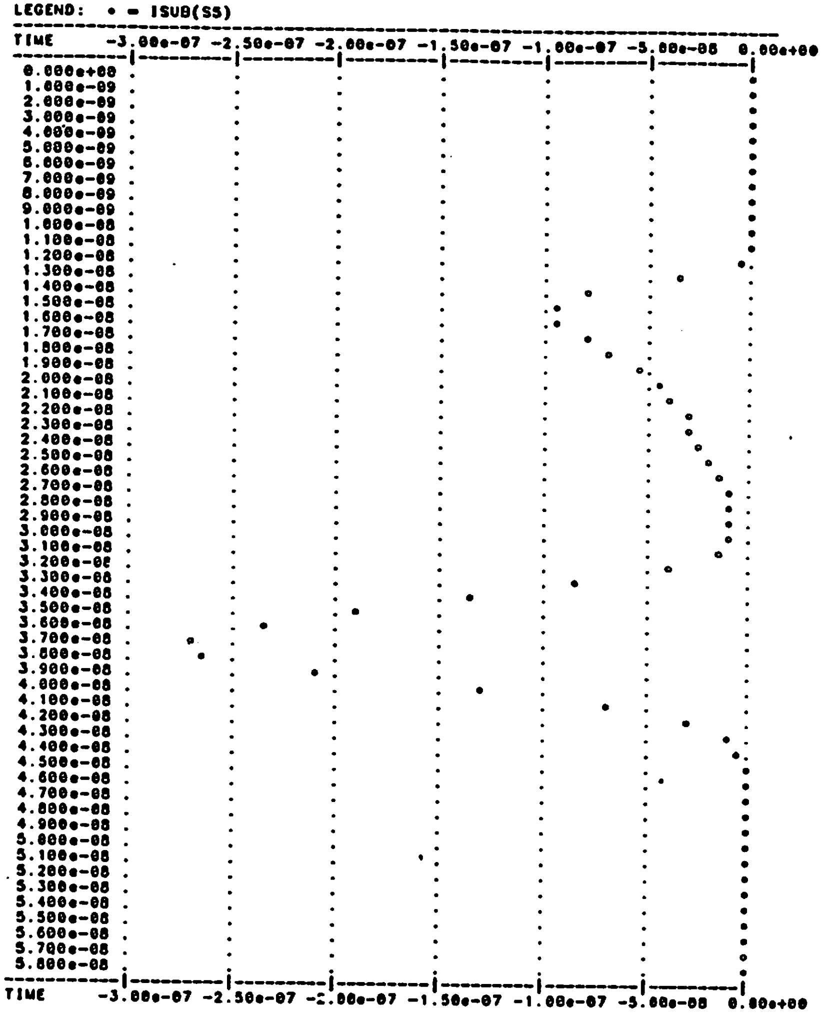
Fig. C8 CMOS sense amplifier circuit used for sample SPICE simulations.

SUBSTRATE CURRENT TRANSIENT ANALYSIS
TRANSISTOR S3



```
   DEVICE LIFETIME AT DELTA VTH = 0.01 VOLTS
-----------------------------------------------------------------------
   >>>>>> TAU(S3) = 1.12627e+12 HRS.  (4.05457e+15 SEC.) <<<<<<
```

SUBSTRATE CURRENT TRANSIENT ANALYSIS
TRANSISTOR S5



```
   DEVICE LIFETIME AT DELTA VTH = 0.01 VOLTS
-----------------------------------------------------------------------
   >>>>>> TAU(S5) = 5.06816e+07 HRS.  (1.82454e+11 SEC.) <<<<<<
```

Fig. C9 BSIM2 output file.

```
                    SUBSTRATE CURRENT TRANSIENT ANALYSIS

LEGEND:  o = IsubNmos(total)
=========================================================================
TIME    -3.00e-07 -2.50e-07 -2.00e-07 -1.50e-07 -1.00e-07 -5.00e-08  0.00e+00
----------|---------|---------|---------|---------|---------|---------|
0.000e+00 .         .         .         .         .         .        o.
1.000e-09 .         .         .         .         .         .        o.
2.000e-09 .         .         .         .         .         .        o.
3.000e-09 .         .         .         .         .         .       o .
4.000e-09 .         .         .         .         .         .     o   .
5.000e-09 .         .         .         .         .         .    o    .
6.000e-09 .         .         .         .         .         .o    o   .
7.000e-09 .         .         .         .         .         .         o
8.000e-09 .         .         .         .         .         .         o
9.000e-09 .         .         .         .         .         .         o
1.000e-08 .         .         .         .         .         .         o
1.100e-08 .         .         .         .         .         .         o
1.200e-08 .         .         .         .         .         .        o.
1.300e-08 .         .         .         .         .         .  o      .
1.400e-08 .         .         .         .         .   o     .         .
1.500e-08 .         .         .         .         .o        .         .
1.600e-08 .         .         .         .         .o        .         .
1.700e-08 .         .         .         .         .   o     .         .
1.800e-08 .         .         .         .         .     o   .         .
1.900e-08 .         .         .         .         .        o.         .
2.000e-08 .         .         .         .         .         .o        .
2.100e-08 .         .         .         .         .         . o       .
2.200e-08 .         .         .         .         .         .   o     .
2.300e-08 .         .         .         .         .         .   o     .
2.400e-08 .         .         .         .         .         .    o    .
2.500e-08 .         .         .         .         .         .     o   .
2.600e-08 .         .         .         .         .         .      o  .
2.700e-08 .         .         .         .         .         .       o .
2.800e-08 .         .         .         .         .         .       o .
2.900e-08 .         .         .         .         .         .       o .
3.000e-08 .         .         .         .         .         .       o .
3.100e-08 .         .         .         .         .         .      o  .
3.200e-08 .         .         .         .         .         . o       .
3.300e-08 .         .         .         .         .  o      .         .
3.400e-08 .         .         .         .  o      .         .         .
3.500e-08 .         .         . o       .         .         .         .
3.600e-08 .         .  o      .         .         .         .         .
3.700e-08 .     o   .         .         .         .         .         .
3.800e-08 .      o  .         .         .         .         .         .
3.900e-08 .         .    o    .         .         .         .         .
4.000e-08 .         .         .         o         .         .         .
4.100e-08 .         .         .         .         . o       .         .
4.200e-08 .         .         .         .         .         o         .
4.300e-08 .         .         .         .         .         .   o     .
4.400e-08 .         .         .         .         .         .     o   .
4.500e-08 .         .         .         .         .         .      o  .
4.600e-08 .         .         .         .         .         .      o  .
4.700e-08 .         .         .         .         .         .      o  .
4.800e-08 .         .         .         .         .         .      o  .
4.900e-08 .         .         .         .         .         .       o .
5.000e-08 .         .         .         .         .         .       o .
5.100e-08 .         .         .         .         .         .       o .
5.200e-08 .         .         .         .         .         .       o .
5.300e-08 .         .         .         .         .         .       o .
5.400e-08 .         .         .         .         .         .       o .
5.500e-08 .         .         .         .         .         .       o .
5.600e-08 .         .         .         .         .         .       o .
5.700e-08 .         .         .         .         .         .       o .
5.800e-08 .         .         .         .         .         .       o .
----------|---------|---------|---------|---------|---------|---------|
TIME    -3.00e-07 -2.50e-07 -2.00e-07 -1.50e-07 -1.00e-07 -5.00e-08  0.00e+00
```

Fig. C9 BSIM2 output file (continued).