BSIM4.0.0 TECHNICAL NOTES

by

Weidong Liu, Kanyu M. Cao, Xiaodong Jin, Chenming Hu
Project Director: Professor Chenming Hu

Memorandum No. UCB/ERL M00/39

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BSIM4.0.0 Technical Notes

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Introduction

BSIM4.0.0 model is developed to explicitly address many issues in modeling sub-0.13 micron CMOS technology and RF high-speed CMOS circuit simulation. The plans and progress of the development were presented and discussed at several Compact Model Council (CMC) meetings in 1998 and 1999 period. Many inputs and several requests from those meetings were incorporated into the model. BSIM4 beta version was tested by CMC member companies and their feedback was incorporated into BSIM4.0.0.

BSIM4.0.0 has the following major improvements and additions over BSIM3v3:

- an accurate new model of the intrinsic input resistance (Rii) for both RF, high-frequency analog and high-speed digital applications;
- flexible substrate resistance network for RF modeling;
- a new accurate channel thermal noise model and a noise partition model for the induced gate noise;
- a non-quasi-static (NQS) model that is consistent with the Rii-based RF model and a consistent AC model that accounts for the NQS effect in both transconductances and capacitances;
- an accurate gate direct tunneling model;
- a comprehensive and versatile geometry-dependent parasitics model for various source/drain connections and multi-finger devices;
- improved model for steep vertical retrograde doping profiles;
- better model for pocket-implanted devices in Vth, bulk charge effect model, and Rout;
- asymmetrical and bias-dependent source/drain resistance, either internal or external to the intrinsic MOSFET at the user's discretion;
- acceptance of either the electrical or physical gate oxide thickness as the model input at the user's choice in a physically accurate manner;
- the quantum mechanical charge-layer-thickness model for both IV and CV;
- a more accurate mobility model for predictive modeling;
- a gate-induced drain leakage (GIDL) current model, available in BSIM for the first time;
- an improved unified flicker (1/f) noise model, which is smooth over all bias regions and considers the bulk charge effect;
- different diode IV and CV characteristics for source and drain junctions;

Threshold Voltage Model

- **General description**

In addition to all the features of the BSIM3v3 model [1], the BSIM4 V_{th} model can more accurately model devices with non-uniform doping profile in both vertical and lateral directions. It also removes a phantom second V_{th} roll-up when $L<L_{min}$ in BSIM3v3. A new long channel DIBL model [2] for pocket devices is also implemented.

- **Vertical non-uniform doping effects**

When the channel doping is not uniform in the vertical direction, there is no single "N_{ch}" available. To clarify its meaning, we define it to be the doping concentration at the depletion edge when $V_{bs}=0$. We also rename the "N_{ch}" in the IV formulation as N_{dep}.

It can be shown [3] that, if we define the zero-th and 1st moment of the vertical doping profile as

$$D_0 = \int_0^{X_{dep}} \left(N(x) - N_{dep}\right) dx$$

$$D_1 = \int_0^{X_{dep}} \left(N(x) - N_{dep}\right) x dx$$

where X_{dep} is the depletion depth and N(x) is the vertical doping profile, then the threshold voltage is

$$V_{th} = V_{th,N_{dep}} + \frac{qD_0}{C_{ox}} + K_{1,N_{dep}}\left(\sqrt{\phi_s - V_{bs} - \frac{qD_1}{\varepsilon_{Si}}} - \sqrt{\phi_s - V_{bs}}\right)$$

where $V_{th,Ndep}$, $K_{1,Ndep}$ and $\phi_s = 0.4 + kT\ln\left(N_{dep}/N_i\right)/q$ can be calculated from conventional models. Since the doping profile is unknown, we split D_0 and D_1 into two parts

$$D_0 = D_{00} + D_{01} = \int_0^{X_{dep0}} \left(N(x) - N_{dep}\right) dx + \int_{X_{dep0}}^{X_{dep}} \left(N(x) - N_{dep}\right) dx$$

$$D_1 = D_{10} + D_{11} = \int_0^{X_{dep0}} \left(N(x) - N_{dep}\right) x dx + \int_{X_{dep0}}^{X_{dep}} \left(N(x) - N_{dep}\right) x dx$$

where X_{dep0} is the depletion depth when $V_{bs}=0$. D_{00} and D_{10} are constants and D_{00} can be merged into V_{th0} in the model. Assuming there is a steep retrograde well below X_{dep0}, It can be shown that D_{01} dominates D_{11} and $D_{01} \approx -C_{01}V_{bs}$. C_{01} depends on the steepness and the depth of the retrograde well. Thus the model for vertical non-uniform doping effect is

$$V_{th} = V_{th0} + K_1\left(\sqrt{\phi_s' - V_{bs}} - \sqrt{\phi_s'}\right) - K_2 V_{bs}$$

where $\phi_s' = \phi_s + \phi_n$, $\phi_s = 0.4 + kT\ln\left(N_{dep}/N_i\right)/q$, $\phi_n = -qD_{10}/\varepsilon_{Si}$ and $K_2 = qC_{01}/C_{ox}$.

- **Lateral non-uniform doping effects**

Reference [2] shows that for long channel devices with pocket implantation, there can be significant drain-induced threshold voltage shift. It can be modeled as

- junction diode breakdown with or without current limiting; and
- dielectric constant of the gate dielectric as a model parameter.

We have been helped by the input from many users, especially the CMC member companies and their representatives. We would particularly like to thank the CMC members for proposing the geometry-dependent parasitics model, which was drafted by Josef Watts and further enhanced by Jon Sanders.

BSIM4.0.0 beta received intensive evaluation by the TI Mixed Signal Products group. Their testing materially and substantially improved the quality of the present production release. We would particularly like to thank Keith Green, Karthik Vasanth, William Liu, Britt Brooks, Doug Weiser, Brian Mounce, Jon Krick, Jim Hellums, Vinod Gupta, and Tom Vrotsos for their invaluable test effort. We would also like to thank Wenliang Zhang and Bob Daniels of Avant!, and John O'Donovan and Kristin Beggs of Cadence for bug reports.

We appreciate these companies providing us with device data during the BSIM4 development: TI, Hitachi, AMD, IBM, and Conexant.

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The BSIM4 model was developed by Professor Chenming Hu, Research Engineer Weidong Liu, and graduate students Xiaodong Jin, Kanyu M. Cao and Jeff Ou.

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$$\Delta V_{th} = -n \cdot V_t \cdot \ln\left(\frac{\left(1 - e^{-V_{ds}/V_t}\right) \cdot L_{eff}}{L_{eff} + dvtp0 \cdot \left(1 + e^{-dvtp1 \cdot Vds}\right)}\right)$$

For V_{ds} of interest, this equation can be simplified as

$$\Delta V_{th} = -n \cdot V_t \cdot \ln\left(\frac{L_{eff}}{L_{eff} + dvtp0 \cdot \left(1 + e^{-dvtp1 \cdot Vds}\right)}\right)$$

For short channel devices, the lateral non-uniform doping profile changes the body bias effect and makes V_{th} roll-up as well. This is modeled by

$$\Delta V_{th} = \sqrt{1 + Lpeb/L_{eff}} \cdot \left(K_{lox} \cdot \sqrt{\phi_s' - V_{bseff}} - K_1 \cdot \sqrt{\phi_s'}\right) + K_{lox} \cdot \left(\sqrt{1 + Lpe0/Leff} - 1\right) \cdot \sqrt{\phi_s'}$$

- **Improved formulation for Short-Channel Effects (SCE)**

  The SCE term used in BSIM3v3 is in the form of $e^{-L/2l} + 2e^{-L/l}$, which is a finite value at L=0 while the V_{th} roll-up term $\sqrt{1 + Nlx/L} - 1$ goes to infinity. So for devices with $L<L_{min}$, modeled V_{th} may have a second roll-up. To eliminate this phantom behavior, we eliminated the approximation used to derive the term $e^{-L/2l} + 2e^{-L/l}$ and model SCE with the more accurate form

$$\frac{0.5}{\cosh\left(D_{VT1} \, L_{eff}/l_t\right) - 1}$$

  When L is small, the function $\propto 1/L^2$ increases faster than $\sqrt{1 + Nlx/L} - 1$. We also expect it to be more accurate even at $L > L_{min}$.

- **Model parameters for V_{th}**

Parameter name	Description	Default value with unit	Binnable ?	Note
VTH0	Long-channel threshold Voltage at V_{bs}=0	0.7V(nmos) -0.7V(pmos)	Yes	-
VFB	Flat-band Voltage	-1.0V	Yes	If not given, calculated from *VTH0*
PHIN	Non-uniform vertical doping effect	0.0V	Yes	-
K1	First body bias coefficient	0.5 $V^{1/2}$	Yes	-
K2	Second body bias coefficient	0.0	Yes	-
K3	Narrow width coefficient	80.0	Yes	-
K3B	Body effect coefficient of K3	0.01/V	Yes	-
W0	Narrow width parameter	2.5e-6m	Yes	-
LPE0	Non-uniform lateral doping parameter at at V_{bs}=0	1.74e-7m	Yes	-
LPEB	Non-uniform lateral doping effect on K1	0.0m	Yes	-
VBM	Maximum applied body bias in V_{th} calculation	-3.0V	Yes	-
DVT0	First coefficient of short channel effect on V_{th}	1.0*	Yes	-

DVT1	Second coefficient of short channel effect on V_{th}	1.0*	Yes	-
DVT2	Body-bias coefficient of short channel effect on V_{th}	-0.0321/V	Yes	-
DVT0W	First coefficient of narrow width effect on V_{th} for small channel length	0.0	Yes	-
DVT1W	Second coefficient of narrow width effect on V_{th} for small channel length	$5.3e6m^{-1}$	Yes	-
DVT2W	Body-bias coefficient of narrow width effect on V_{th} for small channel length	$-0.032V^{-1}$	Yes	-
DVTP0	First coefficient of pocket implant effect on V_{th} for long channel length	0.0m	Yes	-
DVTP1	Second coefficient of pocket implant effect on V_{th} for long channel length	$0.0V^{-1}$	Yes	-

- **Guidelines for parameter extraction**

The parameter extraction procedure is the same as BSIM3v3 except *DVTP0* and *DVTP1*. There are two ways to extract these two parameters.

(1) Measure V_{th} vs. V_{ds} at $V_{bs=0}$ for long and wide channel devices using the constant current method. Fit the V_{th} model to this curve and extract *VTH0*, *DVTP0* and *DVTP1*. In the constant current method V_{th} can be defined as V_{gs} at which $I_{ds}=I_{crit}W/L$, where I_{crit} can be 1e-7A for NMOS and 5e-8A for PMOS.
(2) Extract *VTH0*, *DVTP0* and *DVTP1*directly by fitting V_{th} vs. L at $V_{ds}=0$ and $V_{ds}=V_{dd}$ using long devices (eg: devices with L>1um).

Improved V_{gsteff}

- **General description**

In Bsim3V3, there is no parameter dedicated to the moderate inversion region. To improve the model accuracy in this region, two parameters, *VOFFL* and *MINV*, are introduced.

- ***VOFFL* parameter**

For non-uniform channel doping profiles, *VOFF* parameter varies with L. We propose the following length dependence

$$V_{off}' = V_{off} + \frac{V_{offl}}{L_{eff}}$$

- ***MINV* parameter**

MINV is incorporated to improve the accuracy of g_m, g_m/Id, and g_m^2/I_d in the moderate inversion region. The expressions are:

$$m^* = 0.5 + \arctan(minv)/\pi$$

$$V_{gsteff} = \frac{n \cdot v_t \cdot \ln\left[1 + e^{m^* \cdot V_{gs} / n \cdot v_t}\right]}{m^* + n \cdot Cox\sqrt{2\Phi_s / q\varepsilon_{si} N_{ch}}\, e^{-(1-m^*)V_{gs} - V_{off} / n \cdot v_t}}$$

An *arctan* function is used to limit m* between 0 and 1 to improve parameter optimization process.

- **Parameters for V_{gsteff}**

Parameter name	Description	Default value with unit	Binnable ?	Note
VOFF	Offset voltage in moderate inversion region for large W and L	-0.08V	Yes	-
VOFFL	Coefficient for gate length dependence of *VOFF*	0.0m-V	No	-
MINV	Coefficient of moderate inversion	0.0	Yes	-

- **Guideline for parameter extraction**

In general, the threshold voltage extracted by "linear extrapolation" (peak *gm*) method based on the strong inversion IV equations may be considered the threshold voltage for moderate-to-strong inversion. V_{th} extracted by "constant current" method that extracts V_{th} from sub-threshold IV can be considered the threshold voltage for weak-to-moderate inversion. The difference of these two voltages is *VOFF*. *VOFFL* can be extracted from the gate length dependence of the difference. We suggest *VOFF, VOFFL,* and *MINV* be used to minimize the fitting errors of the target curves such as g_m/I_d and g_m^2/I_d.

Improved Bulk Charge Model

Bulk charge effect has a strong dependence on the channel doping profile. The equation for A_{bulk} is:

$$F\_doping = \frac{\sqrt{1 + L_{peb}/L_{eff}}\, K_{1ox}}{2\sqrt{\phi_s - V_{bseff}}} + K_{2ox} - K_{3b}\frac{T_{ox}}{W_{eff}' + W_0}\phi_s$$

$$A_{bulk} = \left(1 + F\_doping\left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}}\left(1 - A_{gs} V_{gsteff}\left(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}}\right)^2\right) + \frac{B_0}{W_{eff}' + B_1}\right)\right)\frac{1}{1 + KetaV_{bs}}$$

Mobility Models

- **General**

BSIM4 provides three different mobility models. The mobMod=0 and 1 models are from BSIM3v3.2.2; the new mobMod=2, a universal mobility model, is more accurate and suitable for predictive modeling.

- **Parameter set for the mobility models**

Parameter name	Description	Default value with unit	Binnable ?	Note
U0	Low-field mobility	NMOS: 0.067m^2/Vs; PMOS: 0.025m^2/Vs	Yes	-
UA	Coefficient of first-order mobility degradation due to vertical field	1.0e-9m/V for mobMod=0 and 1; 1.0e-15m/V for mobMod=2	Yes	-
UB	Coefficient of second-order mobility degradation due to vertical field	1.0e-19m^2/V^2	Yes	-
UC	Coefficient of mobility degradation due to body-bias effect	-0.0465V^{-1} for mobMod=1; -0.0465e-9m/V^2 for mobMod=0 and 2	Yes	-
EU	Exponent for mobility degradation of mobMod=2	NMOS: 1.67; PMOS: 1.0	Yes	Note-1

Note-1: if *EU* is negative, *EU* is set to zero.

- **Model equations**

MobMod=0:

$$\mu_{eff} = \frac{\mu 0}{1+\left(UA+UCV_{bseff}\right)\left(\frac{V_{gsteff}+2V_{th}}{T_{oxe}}\right)+UB\left(\frac{V_{gsteff}+2V_{th}}{T_{oxe}}\right)^2}$$

MobMod=1:

$$\mu_{eff} = \frac{\mu 0}{1+\left[UA\left(\frac{V_{gsteff}+2V_{th}}{T_{oxe}}\right)+UB\left(\frac{V_{gsteff}+2V_{th}}{T_{oxe}}\right)^2\right]\left(1+UCV_{bseff}\right)}$$

MobMod=2:

$$\mu_{eff} = \frac{\mu 0}{1+\left(UA+UCV_{bseff}\right)\left[\frac{V_{gsteff}+C_0\cdot\left(Vth0-Vfb-\varphi_s\right)}{T_{oxe}}\right]^{EU}}$$

where the constant C_0 = 2 for NMOS and 2.5 for PMOS.

Output Resistance Model

- **General description**

The output resistance model of BSIM4 has significant improvements over that of BSIM3v3 especially for long-channel devices and pocket-implanted devices. The channel length modulation (CLM) model has been improved over L. Four new parameters *FPOUT*, *PDITS*, PDITSL, and *PDITSD* to model the output resistance of long-channel devices and pocket-implanted devices. For non-pocket devices, use of these parameters are also encouraged because these devices may have non-uniform lateral doping profile due to defect-enhanced diffusion even without pocket implant.

- **Degradation factor**

It can be shown [2] that a long channel device with a drain pocket-implant has lower output resistance than that without it. The degradation ratio can be modeled as

$$F = \frac{1}{1 + fprout \cdot \frac{\sqrt{L_{eff}}}{V_{gsteff} + 2v_t}}$$

- **Channel-Length-Modulation model**

It has been shown [4] that the CLM model of BSIM3v3 does not scale accuragely with L correctly because V_{ACLM} is assumed to be constant with respect to Vds when deriving I_{ds}. We correct this by removing this approximation and derive the I_{ds} formula from integration. Let

$$C_{clm} = \frac{1}{P_{clm}} \cdot F \cdot \left(1 + P_{vag} \frac{V_{gsteff}}{E_{sat} L_{eff}}\right)\left(1 + \frac{R_{ds} \cdot I_{dso}}{V_{dseff}}\right)\left(L + \frac{V_{dsat}}{E_{sat}}\right) \cdot \frac{1}{litl}$$

$$V_{ACLM} = C_{clm} \cdot (V_{ds} - V_{dseff})$$

$$V_A = V_{asat} + V_{ACLM}$$

Then omitting other effects gives

$$I_{ds} = I_{dsat}\left(1 + \int_{V_{dsat}}^{V_{ds}} \frac{1}{V_A} dV_{ds}\right) = I_{dsat}\left(1 + \frac{1}{C_{clm}} \ln\left(\frac{V_A}{V_{asat}}\right)\right)$$

- **Effect of drain induced threshold voltage shift on the output resistance**

Pocket implants introduce a potential barrier at the drain end of the channel. This barrier can be lowered by the drain voltage even in long-channel devices. The output resistance of this effect can be modeled as [2]

$$V_{ADITS} = \frac{1}{P_{dits}} \cdot F \cdot \left[1 + \left(1 + P_{ditsl} L_{eff}\right) e^{P_{ditsd} \cdot V_{ds}}\right]$$

- **Change in V_{ADIBL}**

  V_{ADIBL} is separated from V_{ACLM}, and changed to

$$V_{ADIBL} = V_{ADIBL,BSIM3} \cdot \left(1 + P_{VAG} \frac{V_{gsteff}}{E_{sat} L_{eff}}\right)$$

  Note that the degradation factor, F, is not applied to V_{ADIBL}. The reason is that F is derived for long-channel device while DIBL is a short channel effect.

- **Drain current equation**

  Ids is formulated as

$$I_{ds} = \frac{I_{ds0} \cdot N_f}{1 + \frac{R_{ds} I_{ds0}}{V_{dseff}}} \left[1 + \frac{1}{C_{clm}} \ln\left(\frac{V_A}{V_{Asat}}\right)\right] \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}}\right) \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADITS}}\right) \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)$$

  where I_{ds0}, V_{Asat}, V_{ASCBE}, and other terms have the same definitions as in BSIM3v3. N_f is the number of device fingers.

- **Parameters for the Rout model**

Parameter name	Description	Default value with unit	Binnable ?	Note
PCLM	Channel length modulation parameter	1.0	Yes	-
PDIBLC1	First output resistance DIBL effect correction parameter	0.39	Yes	-
PDIBLC2	Second output resistance DIBL effect correction parameter	0.0001	Yes	-
PDIBLCB	Body effect coefficient of DIBL correction parameters	$0.0V^{-1}$	Yes	-
DROUT	L dependence coefficient of the DIBL correction parameter in Rout	1.0	Yes	-
PSCBE1	First substrate current body-effect parameter	4.24e8V/m	Yes	-
PSCBE2	Second substrate current body-effect parameter	1.0e-5m/V	Yes	-
PVAG	Gate dependence of early voltage	0.0	Yes	-
DELTA	Effective V_{ds} parameter	0.01V	Yes	-
FPROUT	Pocket degradation parameter in Rout	$0.0V/m^{0.5}$	Yes	Typical ~500
PDITS	Magnitude of DITS on Rout	$0.0V^{-1}$	Yes	Typical ~0.5
PDITSL	L dependence of DITS on Rout	$0.0m^{-1}$	No	Typical ~1e6
PDITSD	V_{ds} dependence of DITS on Rout	$0.0V^{-1}$	Yes	Typical ~0.3

- **Guidelines for parameter extraction**

Parameters for long channel device fitting: *FPOUT, PDITS, PDITSL,* and *PDITSD.*
Parameters for short channel device fitting: Other parameters.

- **References**

[1] Weidong Liu *et al.*, BSIM3v3.2 MOSFET Model - User's Manual (1998). pp. 3-10. http://www-device.eecs.berkeley.edu/~bsim3.
[2] Kanyu Mark Cao *et al.*, "Modeling of Pocket Implanted MOSFETs for Anomalous Analog Behavior." *Tech. Dig.* of *IEDM*, Washington DC, Dec. pp. 171-174, 1999.
[3] John R. Brews, Physics of the MOS Transistor. Silicon Integrated Circuits, Chap. 1, Academic Press 1981.
[4] Karti Mayaram, modeling CLM-Rout in BSIM3. Personal communication.

Asymmetric and Bias-Dependent R_{ds} Model

- **General**

  Accurate modeling of the bias-dependent LDD source/drain resistance R_{ds}(V) is very important for deep-submicron CMOS technologies. In BSIM3, R_{ds}(V) is modeled internally through the I_{ds} equation and R_s(V)=R_d(V) is assumed. BSIM4 keeps this option for the sake of simulation efficiency. In addition, BSIM4 allows R_{ds}(V) to be external and asymmetrical (i.e. like the source/drain diffusion resistance, the LDD resistances R_d(V) and R_s(V) are connected between the external and internal source (drain) nodes. This feature makes accurate RF CMOS simulation possible. The internal R_{ds}(V) option can be invoked by setting the model selector ***rdsMod*** = 0 **(internal)** and the external one by setting ***rdsMod*** =1 **(external).**

- **Model parameters**

Parameter nme	Description	Default value with unit	Binnable ?	Note
rdsMod	Bias-dependent S/D resistance model selector	0	NA	-
RDSW	Zero bias LDD resistance per unit width for ***rdsMod***=0	200.0ohm·(μm)^{WR}	Yes	Note-1
RDSWMIN	LDD resistance per unit width at high Vgs and zero Vbs for ***rdsMod***=0	0.0ohm·(μm)^{WR}	No	Note-1
RDW	Zero bias lightly-doped drain resistance R_d(V)per unit width for ***rdsMod***=1	100.0ohm·(μm)^{WR}	Yes	Note-1
RDWMIN	Lightly-doped drain resistance per unit width at high V_{gs} and zero V_{bs} for ***rdsMod***=1	0.0ohm·(μm)^{WR}	No	Note-1
RSW	Zero bias lightly-doped source resistance R_s(V)per unit width for ***rdsMod***=1	100.0ohm·(μm)^{WR}	Yes	Note-1
RSWMIN	Lightly-doped source resistance per unit width at high V_{gs} and zero V_{bs} for ***rdsMod***=1	0.0ohm·(μm)^{WR}	No	Note-1
PRWG	Gate bias dependence of LDD resistance	1.0V^{-1}	Yes	Note-1
PRWB	Body bias dependence of LDD resistance	0.0V$^{-0.5}$	Yes	-
WR	Width dependence parameter of LDD resistance	1.0	Yes	-

Note-1: if negative, a warning message will be issued and the parameter is set to 0.0.

- **Model equations**

***rdsMod*==0 (internal R_{ds}(V)):**

$$R_{ds}(V)=\left\{RDSWMIN+RDSW\cdot\left[PRWB\cdot\left(\sqrt{\Phi_s-V_{bseff}}-\sqrt{\Phi_s}\right)+\frac{1}{1+PRWG\cdot V_{gsteff}}\right]\right\}\Big/(1e6\cdot WeffCJ)^{WR}$$

***rdsMod*==1 (External R_d(V) and R_s(V)):**

R_d(V) is expressed as

$$R_d(V)=\left\{RDWMIN+RDW\cdot\left[-PRWB\cdot V_{bd}+\frac{1}{1+PRWG\cdot(V_{gd}-V_{fbsd})}\right]\right\}\Big/\left[(1e6\cdot WeffCJ)^{WR}\cdot N_f\right]$$

R_s(V) is expressed as

$$R_s(V)=\left\{RSWMIN+RSW\cdot\left[-PRWB\cdot V_{bs}+\frac{1}{1+PRWG\cdot(V_{gs}-V_{fbsd})}\right]\right\}\Big/\left[(1e6\cdot WeffCJ)^{WR}\cdot N_f\right]$$

In the above equations, *WeffCJ* is the effective width of the source/drain diffusion regions, *NF* is the number of finger, and V_{fbsd} is the flat-band voltage between the gate and the source/drain. V_{fbsd} is given by

If *NGATE* > 0.0,

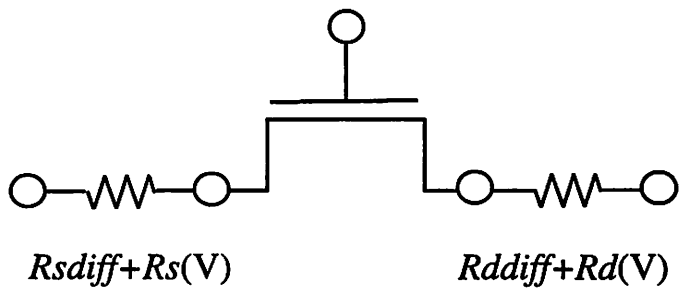
$$V_{fbsd}=\frac{kT}{q}\log\left(\frac{N_{gate}}{N_{sd}}\right)$$

Else

$$V_{fbsd}=0.0$$

where *NGATE* and *NSD* are the doping concentrations in the poly-silicon gate and the source/drain regions, respectively. *NSD* defaults to 1.0e20cm^{-3} and can be binned.

The following figure shows the schematic for ***rdsMod***=1.



Modeling Quantum-Mechanical Inversion-Layer Thickness and High-*k* Gate Dielectrics

- **General**

As the gate oxide thickness is vigorously scaled down, the finite charge-layer thickness can not be ignored [1]. BSIM4 models this effect in both IV and CV. For this purpose, BSM4 accepts the electrical gate oxide thickness *TOXE* and/or the physical gate oxide thickness *TOXP*, or their difference *DTOX* = *TOXE* – *TOXP*, as the model inputs, based on which the effect of effective gate oxide capacitance C_{oxeff} on IV and CV is modeled [2].

High-*k* gate dielectric can be modeled as an "equivalent oxide" with thickness adjusted for SiO_2 (3.9). For example, 3nm gate dielectric with a dielectric constant of 7.8 would have an equivalent oxide thickness of 1.5nm.

BSIM4 also allows to specify a gate dielectric constant (*EPSROX*) different from 3.9 (SiO_2) as an alternative approach to modeling high-*k* dielectrics.

- **Model parameters**

Parameter name	Description	Default value with unit	Binnable ?	Note
EPSROX	Gate dielectric constant relative to vacuum	3.9 (SiO_2)	No	*EPSOX* typically should be ≥ 3.9
TOXE	Electrical gate equivalent oxide thickness	3.0e-9m	No	Note-1
TOXP	Physical gate equivalent oxide thickness	*TOXE*	No	Note-1
TOXM	*TOXE* at which the other BSIM4 parameters are extracted	*TOXE*	No	Note-1
DTOX	Defined as (*TOXE* – *TOXP*)	0.0m	No	-

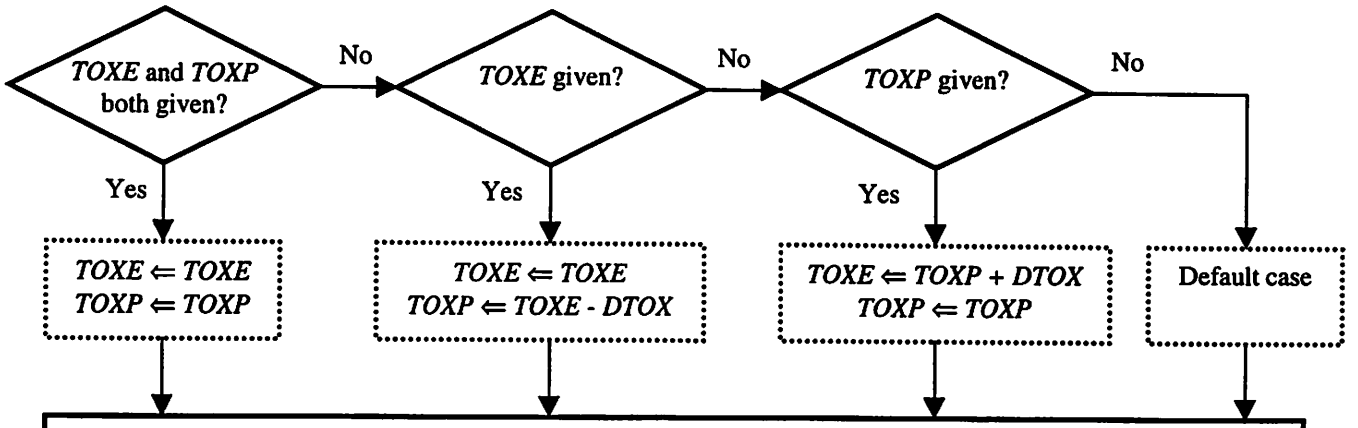
Note-1: if value <= 0.0, fatal errors will be issued.

- **References:**

[1] Y.C. King, H. Fujioka, S. Kamohara, K. Chen, and C. Hu, "DC electrical oxide thickness model for quantization of the inversion layer in MOSFET's," *Semicond. Sci. Technol.*, vol. 13, pp. 963-966, 1998.

[2] Weidong Liu, Xiaodong Jin, Yachin King, and Chenming Hu, "An efficient and accurate compact model for thin-oxide-MOSFET intrinsic capacitance considering the finite charge layer thickness," *IEEE Trans Electron Devices*, vol. 46(5), pp. 1070-1072, 1999.

- **Algorithm and model equations**



- *TOXE* is used to compute: *Vth*, subthreshold swing, *Vgsteff*, *Abulk*, mobiliy, *Vdsat*, *K1OX = K1 * TOXE / TOXM*, *K2OX = K2 * TOXE / TOXM*, capMod=0 and 1, and so on; and
- *TOXP* is used to compute C_{oxeff} for drain current and capMod=2 through X_{DC}

$$X_{DC} = \frac{1.9\times10^{-9}}{1+\left(\frac{V_{gsteff}+4(VTH0-VFB-\Phi_s)}{2TOXP}\right)^{0.7}}$$

Model of Gate-Induced Drain Leakage (GIDL) Current

- **General**
  The gate-induced-drain leakage (GIDL) current [1-2] and its body bias effect are modeled in BSIM4.

- **New model parameters**

Parameter Name	Description	Default value with unit	Binnable ?	Note
AGIDL	Pre-exponential coefficient for GIDL	0.0mho	Yes	Note-1
BGIDL	Exponential coefficient for GIDL	2.3e9V/m	Yes	Note-1
CGIDL	Parameter for the body bias effect on GIDL	$0.5V^3$	Yes	-
EGIDL	Fitting parameter for band bending	0.8V	Yes	-

Note-1: if the binned value is less than or equal to zero, *Igidl* will be zero.

- **GIDL equations**

$$I_{gidl} = AGIDL\, W_{effCJ} \cdot Nf \cdot \frac{V_{ds} - V_{gs\_eff} - EGIDL}{3 \cdot T_{oxe}} \cdot \exp\left(-\frac{3 \cdot T_{oxe} \cdot BGIDL}{V_{ds} - V_{gs\_eff} - EGIDL}\right) \cdot \frac{V_{db}^3}{CGIDL + V_{db}^3}$$

where W_{effCJ} is the width of the drain diffusion region.

- **References**

[1] T.Y. Chan, J. Chen, P.K. Ko, C. Hu, "The Impact of Gate-Induced Drain Leakage Current on MOSFET Scaling," *Tech. Digest of International Electron Devices Meeting (IEDM),* Washington, D.C., Dec. 1987, pp. 718-721.

[2] S.A. Parke, E. Moon, H-J. Wenn, P.K. Ko, C. Hu, "Design for Suppression of Gate-Induced Drain Leakage in LDD MOSFET's Using a Qusasi-Two Dimensional Analytical Model," *IEEE Trans. Electron Devices,* Vol. 39, No. 7, July 1992, pp. 1694-1703.

Gate Direct Tunneling Current Model

- **General description**

As the gate oxide thickness is scaled down to 3 nm and below, gate leakage current due to carrier direct tunneling becomes important. This tunneling happens between the (polysilicon) gate and the silicon beneath the gate oxide. The tunneling carriers can be either electrons or holes, or both, either from the conduction band or valence band, depending on (the type of the polysilicon gate and) the bias regime.

In BSIM4, the gate tunneling current of n^+-poly NMOS and p^+-poly PMOS are modeled. Its components include the tunneling current between gate and substrate/body (Igb), and the current between gate and channel region (Igc), which is partitioned between the source and drain terminals by Igc = Igcs + Igcd. Yet another type of tunneling component is the tunneling current between gate and source/drain diffusion regions (Igs and Igd). As an example, Fig. 1 shows schematically the modeled current flows for an NMOST in the inversion region.

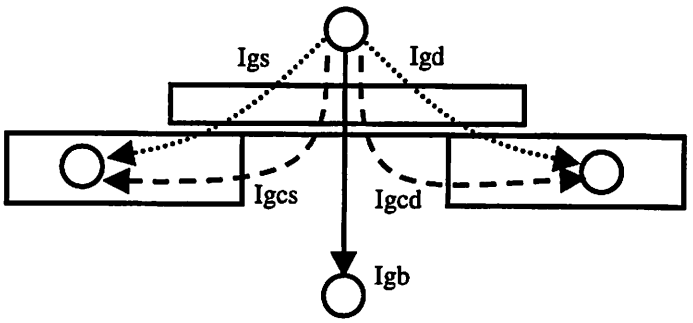


Fig. 1. Schematic gate current components flowing between NMOST terminals in inversion.

- **Model selectors**

Two global selectors are provided to turn on/off the tunneling components. igcmod=1 turns on Igc, Igs and Igd; igbmod=1 turns on Igb. When both are set to 0, no gate tunneling current components are modeled.

- **Equation for V_{ox}**

The gate tunneling current is a strong function of the voltage drop across the gate oxide (V_{ox}). V_{ox} is derived as

$$V_{ox} = V_{fbzb} - V_{fbeff} + k_{1ox}\sqrt{\varphi_s} + V_{gsteff}$$

where V_{fbzb} is calculated from V_{th} under zero bias conditions, V_{gsteff} is the effective (V_{gs_eff} – V_{th}) with poly-depletion effects considered by V_{gs_eff}, V_{fbeff} is expressed by

$$V_{fbeff} = V_{fbzb} - \frac{1}{2}\left[(V_{fbzb} - V_{gb} - \delta) + \sqrt{(V_{fbzb} - V_{gb} - \delta)^2 + 4V_{fbzb}\delta}\right]; \delta = 0.02$$

$\sqrt{\varphi_s}$ is given by

$$\sqrt{\varphi_s} = \frac{k_{1ox}}{2}\cdot\left[-1+\sqrt{1+\frac{4}{k_{1ox}{}^2}\left(V_{gs\_eff}-V_{fbeff}-V_{gsteff}-V_{bseff}\right)}\right]$$

As will be shown later on, it is convenient to transform V_{ox} into

$$V_{ox} = V_{oxacc} + V_{oxdepinv}$$

where $V_{oxacc} = V_{fbzb} - V_{fbeff}$ for the accumulation region and $V_{oxdepinv} = k_{1ox}\sqrt{\varphi_s} + V_{gsteff}$ for the depletion and inversion regions. Note that V_{ox} and its derivatives are continuous over all bias regions.

- **Equations for the tunneling currents**

(1) Gate-to-substrate/body current (Igb = Igbacc + Igbinv)

Igbacc -- determined by ECB (Electron tunneling from Conduction Band):

Igbacc, which is significant in the accumulation region, is given by

$$Igbacc = W_{eff}L_{eff}\cdot A\cdot T_{oxRatio}\cdot V_{gb}\cdot V_{aux} \cdot\exp\left[-B\cdot T_{oxe}\left(aigbacc - bigbacc\cdot V_{oxacc}\right)\cdot\left(1+cigbacc\cdot V_{oxacc}\right)\right]$$

where the physical constant A = 4.97232e-7 A/V^2, B = 7.45669e11 (g/F-s^2)$^{0.5}$ is another physical constant, $T_{oxRatio} = \left(\frac{T_{oxref}}{T_{oxe}}\right)^{ntox}\cdot\frac{1}{T_{oxe}{}^2}$, and

$$V_{aux} = nigbacc\cdot V_{tm}\cdot\log\left(1+\exp\left(-\frac{V_{gb}-V_{fbzb}}{nigbacc\cdot V_{tm}}\right)\right).$$

Igbinv -- determined by EVB (Electron tunneling from Valence Band):

Igbinv, which is significant in the inversion region, is given by

$$Igbinv = W_{eff}L_{eff}\cdot A\cdot T_{oxRatio}\cdot V_{gb}\cdot V_{aux} \cdot\exp\left[-B\cdot T_{oxe}\left(aigbinv - bigbinv\cdot V_{oxdepinv}\right)\cdot\left(1+cigbinv\cdot V_{oxdepinv}\right)\right]$$

where A = 3.75956e-7 A/V^2, B = 9.82222e11 (g/F-s^2)$^{0.5}$, and

$$V_{aux} = nigbinv\cdot V_{tm}\cdot\log\left(1+\exp\left(\frac{V_{oxdepinv}-eigbinv}{nigbinv\cdot V_{tm}}\right)\right).$$

(2) Gate-to-channel current (Igc) and gate-to-S/D current (Igs and Igd)

Igc -- determined by ECB for NMOS and HVB for PMOS (Hole tunneling from Valence Band), respectively.

$$Igc = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gs\_eff} \cdot V_{aux} \cdot \exp\left[-B \cdot T_{oxe}\left(aigc - bigc \cdot V_{oxdepinv}\right) \cdot \left(1 + cigc \cdot V_{oxdepinv}\right)\right]$$

where A = 4.97232e-7 A/V^2 for NMOS and 3.42537e-7 A/V^2 for PMOS, B = 7.45669e11 (g/F-s^2)$^{0.5}$ for NMOS and 1.16645e12 (g/F-s^2)$^{0.5}$ for PMOS, and

$$V_{aux} = nigc \cdot V_{tm} \cdot \log\left(1 + \exp\left(\frac{V_{gs\_eff} - V_{th0}}{nigc \cdot V_{tm}}\right)\right).$$

Igs and Igd -- Igs represents the gate tunneling current between the gate and the source diffusion region, while Igd represents the gate tunneling current between the gate and the drain diffusion region. Igs and Igd are determined by ECB for NMOS and by HVB for PMOS, respectively.

$$Igs = W_{eff} Dlcig \cdot A \cdot T_{oxRatioEdg} \cdot V_{gs}' \cdot V_{gs}' \cdot \exp\left[-B \cdot T_{oxe} \cdot Poxedge \left(aigsd - bigsd \cdot V_{gs}'\right) \cdot \left(1 + cigsd \cdot V_{gs}'\right)\right]$$

and

$$Igd = W_{eff} Dlcig \cdot A \cdot T_{oxRatioEdg} \cdot V_{gd}' \cdot V_{gd}' \cdot \exp\left[-B \cdot T_{oxe} \cdot Poxedge \left(aigsd - bigsd \cdot V_{gd}'\right) \cdot \left(1 + cigsd \cdot V_{gd}'\right)\right]$$

where A = 4.97232e-7 A/V^2 for NMOS and 3.42537e-7 A/V^2 for PMOS, B = 7.45669e11 (g/F-s^2)$^{0.5}$ for NMOS and 1.16645e12 (g/F-s^2)$^{0.5}$ for PMOS,

$T_{oxRatioEdge} = \left(\frac{T_{oxref}}{T_{oxe} \cdot Poxedge}\right)^{ntox} \cdot \frac{1}{\left(T_{oxe} \cdot Poxedge\right)^2}$, $V_{gs}' = \sqrt{\left(V_{gs} - Vfbsd\right)^2 + 1.0e-4}$, and

$V_{gd}' = \sqrt{\left(V_{gd} - Vfbsd\right)^2 + 1.0e-4}$.

- **Partition of Igc**

To consider the drain bias effects, Igc is split into two components, Igcs and Igcd, that is Igc = Igcs + Igcd.

$$Igcs = Igc \cdot \frac{pigcd \cdot V_{ds} + \exp\left(-pigcd \cdot V_{ds}\right) - 1 + 1.0e-4}{pigcd^2 \cdot V_{ds}^{\ 2} + 2.0e-4}$$

and

$$Igcd = Igc \cdot \frac{1 - \left(pigcd \cdot V_{ds} + 1\right) \cdot \exp\left(-pigcd \cdot V_{ds}\right) + 1.0e-4}{pigcd^2 \cdot V_{ds}^{\ 2} + 2.0e-4}.$$

- **Table of parameters for the gate tunneling current model**

Parameter Name	Description	Default value with unit	Binnable ?	Note
igcmod	Global model selector for Igs, Igd, Igcs and Igcd current components	0	N/A	igcmod==1 turns on Igs, Igd, Igcs and Igcd.
igbmod	Global model selector for Igb current	0	N/A	igbmod==1 turns on Igb.
aigbacc	Parameter for Igb in accumulation	0.43 $(Fs^2/g)^{0.5} m^{-1}$	Yes	-
bigbacc	Parameter for Igb in accumulation	0.054 $(Fs^2/g)^{0.5} (mV)^{-1}$	Yes	-
cigbacc	Parameter for Igb in accumulation	0.075 V^{-1}	Yes	-
nigbacc	Parameter for Igb in accumulation	1.0	Yes	Note-1
aigbinv	Parameter for Igb in inversion	0.35 $(Fs^2/g)^{0.5} m^{-1}$	Yes	-
bigbinv	Parameter for Igb in inversion	0.03 $(Fs^2/g)^{0.5} (mV)^{-1}$	Yes	-
cigbinv	Parameter for Igb in inversion	0.006 V^{-1}	Yes	-
eigbinv	Parameter for Igb in inversion	1.1V	Yes	-
nigbinv	Parameter for Igb in inversion	3.0	Yes	Note-1
aigc	Parameter for Igcs and Igcd	NMOS: 0.43 PMOS: 0.31 $(Fs^2/g)^{0.5} m^{-1}$	Yes	-
bigc	Parameter for Igcs and Igcd	NMOS: 0.054 PMOS: 0.024 $(Fs^2/g)^{0.5} (mV)^{-1}$	Yes	-
cigc	Parameter for Igcs and Igcd	NMOS: 0.075 V^{-1} PMOS: 0.03 V^{-1}	Yes	-
aigsd	Parameter for Igs and Igd	NMOS: 0.43 PMOS: 0.31 $(Fs^2/g)^{0.5} m^{-1}$	Yes	-
bigsd	Parameter for Igs and Igd	NMOS: 0.054 PMOS: 0.024 $(Fs^2/g)^{0.5} (mV)^{-1}$	Yes	-
cigsd	Parameter for Igs and Igd	NMOS: 0.075 V^{-1} PMOS: 0.03 V^{-1}	Yes	-

dlcig	S/D overlap length for Igs/Igd	Lint	No	-
nigc	Parameter for Igs, Igd, Igcs, and Igcd	1.0	Yes	Note-1
poxedge	Factor for the gate oxide thickness in the S/D overlap regions	1.0	Yes	Note-1
pigcd	Vds dependence of Igcs and Igcd	1.0	Yes	Note-1
ntox	Exponent for the tox ratio	1.0	Yes	-
toxref	Nominal gate oxide thickness	30.0A	No	Note-1

Note-1: if the value is less than or equal to zero, fatal errors are issued.

Charge-Voltage (CV) Model

- **General**

  BSIM4 provides three options for selecting intrinsic and overlap/fringing capacitance models. Those three capacitance models come from BSIM3v3.2.2, and the BSIM3v3.2.2 CV model parameters are used without change in BSIM4 except that separate *CKAPPA* parameters, *CKAPPAS* (binnable, defaulting to 0.6) and *CKAPPAD* (binnable, defaulting to *CKAPPAS*), are introduced for the source-side and drain-side diodes, respectively. The following table maps the BSIM4 capacitance models to those in BSIM3v3.2.2.

- **BSIM4 capacitance model options**

BSIM4 capacitance models	Matched capMod in BSIM3v3.2.2
capMod=0	Intrinsic capMod=0 + Overlap/fringing capMod=0
capMod=1	Intrinsic capMod=2 + Overlap/fringing capMod=2
capMod=2 (**default model**)	Intrinsic capMod=3 + Overlap/fringing capMod=2

The BSIM3v3.2.2 capMod=1 is no longer supported in BSIM4.

Electrode Gate and Intrinsic-Input Resistance Model

- **General**

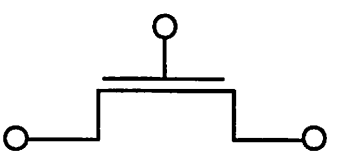
BSIM4 provides four options for modeling electrode gate (bias-independent) and bias-dependent gate (intrinsic input) resistances. This model also works with multi-finger devices.

- **Model parameters**

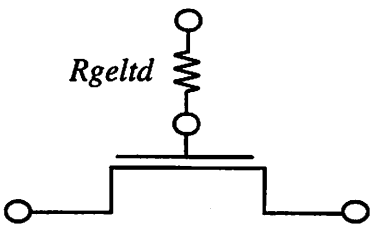
Parameter name	Description	Default	Binnnable ?	Note
RgateMod (instance and global)	Gate-resistance model selector	0 – no gate resistance	NA	-
RSHG	Gate-electrode sheet resistance	0.1 ohm/square	No	Warning message if *RSHG* <= 0.0
XGW	Distance from the gate contact to the channel edge	0.0m	No	-
XGL	Difference between *Ldrawn* and physical gate length	0.0m	No	-
NGCON	Number of gate contacts for each finger, 1 or 2	1.0	No	Fatal error if <1.0
XRCRG1	Parameter for distributed channel-resistance effect	12.0	Yes	Warning message if *XRCRG1* <= 0.0
XRCRG2	Parameter to account for the excess channel diffusion resistance	1.0	Yes	-

- **Options and schematic**

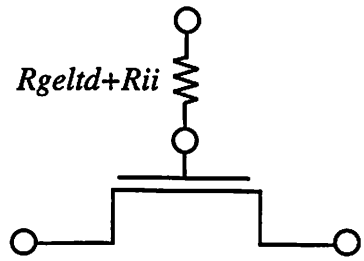
rgateMod = 0 (zero-resistance):
No gate resistance is generated.



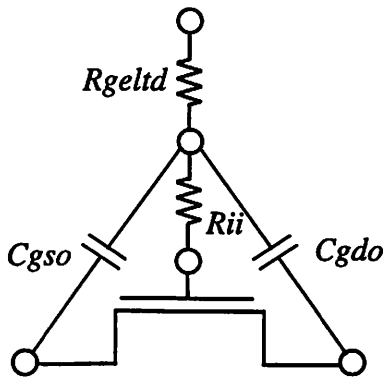
rgateMod = 1 (constant-resistance):
Only the electrode gate resistance (bias-independent) is generated by adding an internal gate node.



rgateMod = 2(variable-resistance):
The gate resistance is the sum of the electrode gate resistance and the intrinsic-input resistance *Rii* (bias-dependent) [1]. An internal gate node is introduced.



rgateMod = 3 (two-node):
The electrode gate resistance is in series with the intrinsic-input resistance through two internal gate nodes, so that the overlap capacitance current will not pass through the intrinsic-input resistance.



- **Equations**

Electrode gate resistance:

$$Reltd = \frac{rshg \cdot \left(xgw + \frac{Weffcj}{3ngcon} \right)}{ngcon \cdot (Ldrawn - xgl) \cdot NF}$$

Please refer to "Modeling Series/Parallel Devices" for the layout parameters in the above equation.

Intrinsic-input resistance:

$$\frac{1}{Rii} = xrcrg1 \cdot \left(\frac{1}{Rdrif} + \frac{1}{Rdiff} \right) = xrcrg1 \cdot \left(\frac{I_{ds}}{V_{dseff}} + xrcrg2 \cdot \frac{Weff \mu_{eff} C_{oxeff} kT}{qLeff} \right)$$

- **References**

[1] Xiaodong Jin, Jia-Jiunn Ou, Chih-Hung Chen, Weidong Liu, Paul Gray, and Chenming Hu, "An effective gate resistance model for CMOS RF and noise modeling," *Tech. Dig.* of *IEDM*, San Francisco, CA, pp. 961-964, Dec. 1998.

Substrate Resistance Network

- **General**

For CMOS RF circuit simulation, it is essential to consider the high frequency coupling through the substrate. BSIM4 offers a flexible built-in substrate resistance network. This network is constructed such that little simulation efficiency penalty will result. Note that the substrate resistance parameters listed below should be extracted for the total device, not on a per-finger basis.

- **Model selector and parameters**

Parameter name	Description	Default value with unit	Binnable ?	Note
rbodyMod (instance and global parameter)	Model selector for distributed substrate resistance network	0 – network is turned off	NA	-
GBMIN (instance and global parameter)	Minimum conductance in parallel with each of the five substrate resistances	1.0e-12mho	No	Note-1
RBPB (instance and global parameter)	Resistance connected between bNodePrime and bNode	50.0ohm	No	Note-2
RBPD (instance and global parameter)	Resistance connected between bNodePrime and dbNode	50.0ohm	No	Note-2
RBPS (instance and global parameter)	Resistance connected between bNodePrime and sbNode	50.0ohm	No	Note-2
RBDB (instance and global parameter)	Resistance connected between dbNode and bNode	50.0ohm	No	Note-2
RBSB (instance and global parameter)	Resistance connected between sbNode and bNode	50.0ohm	No	Note-2

Note-1: if *GBMIN* < 1.0e-20, warning message will be issued since it is too small. Each substrate resistance listed above is connected in parallel with *GBMIN* to prevent too large resistance values, which would otherwise cause poor convergence.

Note-2: if value < 1.0e-3, it is set to 1.0e-3ohm.

- **Topology**

***rbodyMod* = 0 (Off):**

No substrate network is generated at all.

***rbodyMod* = 1 (On):**

All five resistances in the substrate network as shown schematically below are present simultaneously. *GBMIN* is in parallel with each resistance in the network. To simplify the representation of the model topology, *GBMIN* is merged into each resistance. Note that the intrinsic model substrate reference point is the internal body node **bNodePrime**, into which the impact ionization current I_{SUB} and the GIDL current I_{GDIL} flow.

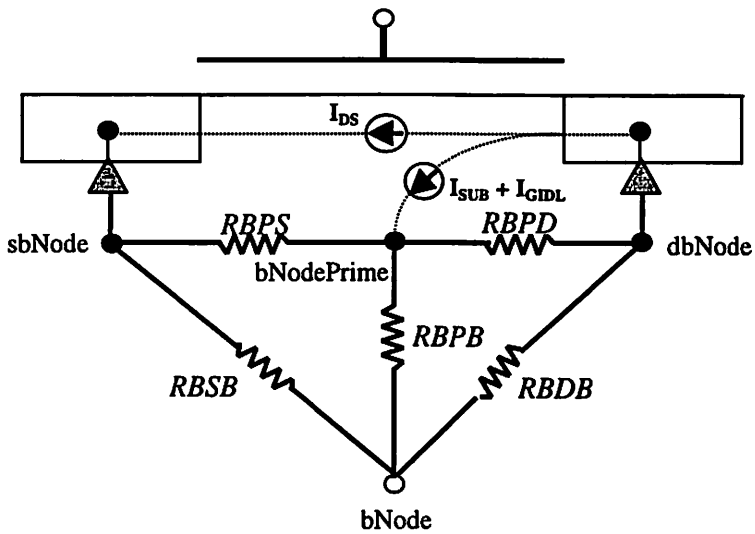


Fig. 1 Topology with the substrate resistance network turned on.

Non-Quasi-Static Model

- **General**

BSIM4 uses two different NQS model selectors to turn on the charge-deficit NQS model in transient simulation (using ***trnqsMod***=1) and AC simulation (using ***acnqsMod***=1). The AC NQS model does not require the internal NQS charge node that is required by the transient NQS model. Both the transient NQS and AC NQS models are developed from the same fundamental physical basis: the channel/gate charge response to the external signal are relaxation-time (τ) dependent and the transcapacitances and transconductances (such as g_m) for AC analysis can therefore be expressed as functions of $j\omega\tau$.

- **Model parameters**

Parameter name	Description	Default value with unit	Binnable ?	Note
trnqsMod (instance and global)	Transient NQS model selector	0 – off	NA	-
acnqsMod (instance and global)	AC NQS model selector	0 - off	NA	-
XRCRG1	Parameter for distributed channel-resistance effect	12.0	Yes	Warning message if *XRCRG1* <= 0.0
XRCRG2	Parameter to account for the excess channel diffusion conductance	1.0	Yes	-

Warning: these models should not be turned on when rgateMod is set to 2 or 3.

- **Model equation**

In time domain, the charging current at time t due to channel charge $Q_{ch}(t)$ is expressed as

$$\frac{\partial Q_{ch}(t)}{\partial t} = \frac{Q_{def}(t)}{\tau} \qquad (1)$$

Therefore the charging current at the gate, source, and drain terminals for the transient NQS model is obtained from

$$\frac{\partial Q_{g,d,s}(t)}{\partial t} = XPART_{G,D,S}\frac{Q_{def}(t)}{\tau} \qquad (2)$$

where $XPART_{G,D,S}$ are the charge partition number, and $Q_{def}(t)$ is the difference between the channel charge density $Q_{ch,qs}(t)$ under quasi-static approximation and $Q_{ch}(t)$. Thus,

$$Q_{def}(t) \equiv Q_{ch,qs}(t) - Q_{ch}(t) \qquad (3)$$

By substituting (3) into (1), it can be shown that in the frequency domain $Q_{ch}(t)$ can be written as

$$\Delta Q_{ch}(t) = \frac{\Delta Q_{ch,qs}(t)}{1 + j\omega\tau} \qquad (4)$$

where the transit time τ is equal to the product of R_{ii} and WLC_{ox}, where R_{ii} is given by

$$\frac{1}{Rii} = xrcrg1 \cdot \left(\frac{1}{Rdrif} + \frac{1}{Rdiff} \right) = xrcrg1 \cdot \left(\frac{I_{ds}}{V_{dseff}} + xrcrg2 \cdot \frac{Weff\mu_{eff} C_{oxeff} kT}{qLeff} \right)$$

Based on (4), it can be proved that the transcapacitances C_{gi}, C_{si}, *and* C_{di} (*i* stands for any of the *d*, *g*, *s*, and *b* terminals of the device) and the channel transconductances g_m, g_{ds}, and g_{mb} all become complex quantities. For example, g_m and C_{dg} now become

$$g_m = \frac{g_{m0}}{1+\omega^2\tau^2} + j\left(-\frac{g_{m0} \cdot \omega\tau}{1+\omega^2\tau^2} \right)$$

$$C_{dg} = \frac{C_{dg0}}{1+\omega^2\tau^2} + j\left(-\frac{C_{dg0} \cdot \omega\tau}{1+\omega^2\tau^2} \right)$$

The quantities in the above two equations with sub "0" are known from the OP analysis.

Flicker Noise Model

- **General**

  BSIM4 provides two flicker noise models. When the model selector ***fnoiMod*** is set to 0, a simple flicker noise model which is convenient for hand calculations is invoked. A unified physical flicker noise model, which is the default model, will be used if ***fnoiMod*** == 1. These two flicker noise models come from BSIM3v3, but the unified model has many improvements. For instance, it is now smooth over all bias regions and considers the bulk charge effect.

- **Model parameters**

Parameter name	Description	Default value with unit	Binnable ?	Note
fnoiMod	Flicker noise model selector	1	NA	-
AF	Flicker noise exponent	1.0	No	-
EF	Flicker noise frequency exponent	1.0	No	-
KF	Flicker noise coefficient	0.0 A^{2-AF} $\cdot s^{1-EF} \cdot F$	No	-
NOIA	Flicker noise parameter A	NMOS: 6.25e41 $(eV)^{-1} \cdot s^{1-EF} \cdot m^{-3}$ PMOS: 6.188e40 $(eV)^{-1} \cdot s^{1-EF} \cdot m^{-3}$	No	-
NOIB	Flicker noise parameter B	NMOS: 3.125e26 $(eV)^{-1} \cdot s^{1-EF} \cdot m^{-1}$ PMOS: 1.5e25 $(eV)^{-1} \cdot s^{1-EF} \cdot m^{-1}$	No	-
NOIC	Flicker noise parameter C	8.75e9$(eV)^{-1} \cdot s^{1-EF} \cdot m$	No	-
EM	Saturation field	4.1e7V/m	No	-

- **Equations**

fnoiMod==0 (simple model):

Noise density is $S_{id}(f) = \dfrac{KF \cdot I_{ds}^{\ AF}}{C_{oxe} L_{eff}^{\ 2} f^{EF}}$

fnoiMod==1 (unified physical model):

In the inversion region, the noise density is expressed as

$$S_{id,inv}(f) = \frac{kTq^2 \mu_{eff} I_{ds}}{C_{oxe} L_{eff}^{\ 2} A_{bulk} f^{ef} \cdot 10^{10}} \left(NOIA \cdot \log\left(\frac{N_0 + N^*}{N_t + N^*}\right) + NOIB \cdot (N_0 - N_t) + \frac{NOIC}{2}\left(N_0^{\ 2} - N_t^{\ 2}\right)\right)$$
$$+ \frac{kTI_{ds} \Delta L_{clm}}{W_{eff} \cdot L_{eff}^{\ 2} f^{ef} \cdot 10^{10}} \cdot \frac{NOIA + NOIB \cdot N_t + NOIC \cdot N_t^{\ 2}}{\left(N_t + N^*\right)^2}$$

where N^*, N_0, N_l, and ΔL_{clm} are given as

$$N^* = kT \cdot (C_{oxe} + C_d + C_{it}) / q^2 \text{ , } (C_{it} \text{ is a model parameter from DC})$$

$$N_0 = C_{oxe} \cdot V_{gsteff} / q$$

$$N_l = C_{oxe} \cdot V_{gsteff} \cdot \left(1 - \frac{A_{bulk} V_{dseff}}{V_{gsteff} + 2v_t}\right) / q \text{ , and}$$

$$\Delta L_{clm} = Litl \cdot \log\left(\frac{\frac{V_{ds} - V_{dseff}}{Litl} + E_m}{E_{sat}}\right)$$

$$E_{sat} = \frac{2v_{sat}}{\mu_{eff}}, \quad and \; Litl = \sqrt{3X_j T_{oxe}}$$

In the subthreshold region, the noise density is written as

$$S_{id,subVt}(f) = \frac{NOIA \cdot kT \cdot I_{ds}^{\ 2}}{W_{eff} L_{eff} f^{EF} N^{*2} \cdot 10^{10}}$$

The total flicker noise density is expressed by

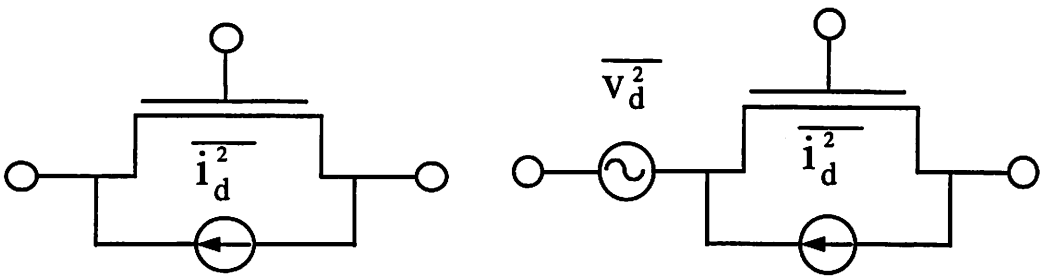
$$S_{id}(f) = \frac{S_{Id,inv}(f) \times S_{id,subvt}(f)}{S_{id,subvt}(f) + S_{Id,inv}(f)}$$

(Holistic) Thermal Noise Model

- **General**

There are two thermal noise models in BSIM4 as shown in the following figures:
(1) ***tnoiMod***=0 (charge-based): thermal noise model used in BSIM3v3.2.2;
(2) ***tnoiMod***=1(holistic): new holistic thermal noise model .

tnoiMod=0 ***tnoiMod***=1



In the new thermal noise model, all the short-channel effects and velocity saturation effect incorporated in the IV model are automatically included in the thermal noise model, hence the name "holistic thermal noise model". In addition, the amplification of the channel thermal noise through *gm* and *gmbs* as well as the induced-gate noise with partial correlation to the channel thermal noise are all captured in the new "noise-partition" model.

- **Thermal noise equations**

tnoiMod=0:

$$\overline{i_d^2} = \frac{4kT\Delta f}{R_{ds}(V) + \dfrac{L_{eff}^{\ 2}}{\mu_{eff}\left|Q_{inv}\right|}} \cdot ntnoi$$

tnoiMod=1:

$$\overline{v_d^{\ 2}} = 4kT \cdot theta^2 \cdot \frac{V_{dseff}\Delta f}{I_{ds}}$$

$$\overline{i_d^2} = 4kT\frac{V_{dseff}\Delta f}{I_{ds}}\left[g_{ds} + beta^*(g_m + g_{mbs})\right]^2 - \overline{v_d^{\ 2}}(g_m + g_{ds} + g_{mbs})^2$$

where

$$theta = 0.37 \cdot \left[1 + tnoib \cdot L_{eff} \cdot \left(\frac{V_{gsteff}}{E_{sat} L_{eff}} \right)^2 \right]$$

$$beta = 0.577 \cdot \left[1 + tnoia \cdot L_{eff} \cdot \left(\frac{V_{gsteff}}{E_{sat} Le_{ff}} \right)^2 \right]$$

- **Model Parameters**

Parameter name	Description	Default value with unit	Binnable?	Note
tnoiMod	Thermal noise model selector	0	NA	-
NTNOI	Noise factor for short channel devices for tnoiMod=0	1.0	No	-
TNOIA	L-dependence parameter for channel thermal noise partitioning	1.5	No	-
TNOIB	L-dependence parameter for channel thermal noise partitioning	3.5	No	-

- **Other noise sources modeled in BSIM4**

BSIM4 also models the thermal noise contributions from the substrate, electrode gate, and source/drain resistances. Shot noise due to various gate tunneling current components is modeled as well.

Asymmetric Source/Drain Junction Diode Model with Breakdown

- **Diode IV model selector**

  In BSIM4, there are three junction diode IV models. When the model selector ***dioMod*** is set to 0 ("resistance-free"), the diode IV is modeled as resistance-free with or without breakdown depending on the parameter values of *XJBVS* or *XJBVD*. When ***dioMod*** is set to 1 ("breakdown-free"), the diode is modeled exactly the same way as in BSIM3v3.2.2 with current-limiting feature in the forward-bias region through the limiting current *IJTHSFWD* or *IJTHDFWD*; diode breakdown is not modeled for ***dioMod***=1 and *XJBVS, XJBVD, BVS*, and *BVD* parameters all have no effect. When ***dioMod*** is set to 2 ("resistance-and-breakdown"), BSIM4 models the diode breakdown with current limiting in both forward and reverse operations. In general, setting ***dioMod*** to 1 produces fast convergence.

- **Model parameters (separate IV and CV parameters for the drain-side and source-side junctions)**

Parameter Name		Description	Default with unit	Binnable ?	Note
Source side	Drain side				
NJS	*NJD*	Junction emission coefficient	*NJS*=1.0; *NJD=NJS*	No	-
XTIS	*XTID*	Junction current temperature exponent	*XTIS*=3.0; *XTID=XTIS*	No	-
IJTHSREV	*IJTHDREV*	Limiting current in reverse bias region	*IJTHSREV*=0.1A; *IJTHDREV= IJTHSREV*	No	Note-1
IJTHSFWD	*IJTHDFWD*	Limiting current in forward bias region	*IJTHSFWD*=0.1A; *IJTHDFWD= IJTHSFWD*	No	Note-2
XJBVS	*XJBVD*	Fitting parameter for diode breakdown	*XJBVS*=1.0; *XJBVD=XJBVS*	No	Note-3
BVS	*BVD*	Breakdown voltage	*BVS*=10.0V; *BVD=BVS*	No	Note-4
JSS	*JSD*	Bottom junction reverse saturation current density	*JSS*=1.0e-4A/m^2; *JSD=JSS*	No	-
JSWS	*JSWD*	Isolation-edge sidewall reverse saturation current density	*JSWS*=0.0A/m; *JSWD=JSWS*	No	-
JSWGS	*JSWGD*	Gate-edge sidewall reverse saturation current density	*JSWGS*=0.0A/m; *JSWGD=JSWGS*	No	-
CJS	*CJD*	Bottom junction capacitance per unit area	*CJS*=5.0e-4F/m^2; *CJD=CJS*	No	-
PBS	*PBD*	Bottom junction built-in potential	*PBS*=1.0V; *PBD=PBS*	No	-
MJS	*MJD*	Bottom junction grading coefficient	*MJS*=0.5; *MJD=MJS*	No	-

CJSWS	*CJSWD*	Isolation-edge sidewall junction capacitance per unit length	*CJSWS*=5.0e-10F/m; *CJSWD=CJSWS*	No	-
PBSWS	*PBSWD*	Isolation-edge sidewall junction built-in potential	*PBSWS*=1.0V; *PBSWD=PBSWS*	No	-
MJSWS	*MJSWD*	Isolation-edge sidewall junction grading coefficient	*MJSWS*=0.33; *MJSWD=MJSWS*	No	-
CJSWGS	*CJSWGD*	Gate-edge sidewall junction capacitance per unit length	*CJSWGS=CJSWS*; *CJSWGD=CJSWS*	No	-
PBSWGS	*PBSWGD*	Gate-edge sidewall junction built-in potential	*PBSWGS=PBSWS*; *PBSWGD=PBSWS*	No	-
MJSWGS	*MJSWGD*	Gate-edge sidewall junction grading coefficient	*MJSWGS=MJSWS*; *MJSWGD= MJSWS*	No	-

Note-1: if *IJTHSREV* <= 0.0, *IJTHSREV* is set to 0.1.
if *IJTHDREV* <= 0.0, *IJTHDREV* is set to 0.1.
Note-2: if *IJTHSFWD* <= 0.0, *IJTHSFWD* is set to 0.1.
if *IJTHDFWD* <= 0.0, *IJTHDFWD* is set to 0.1.
Note-3: For dioMod=0, if *XJBVS* < 0.0, *XJBVS* is set to 1.0.
For dioMod=2, if *XJBVS* <= 0.0, *XJBVS* is set to 1.0.
For dioMod=0, if *XJBVD* < 0.0, *XJBVD* is set to 1.0.
For dioMod=2, if *XJBVD* <= 0.0, *XJBVD* is set to 1.0.
Note-4: if *BVS* <= 0.0, *BVS* is set to 10.0.
if *BVD* <= 0.0, *BVD* is set to 10.0.

- **IV and breakdown equations**

In the following, the equations will be given only for the source-side diode. The drain-side diode has an analogous set of equations.

diomod == 0 (resistance-free):

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{qV_{bs}}{NJS \cdot kT}\right) - 1\right] \cdot f_{breakdown} + V_{bs} \cdot G_{\min}$$

where I_{sbs} is the total saturation current consisting of the components through the gate-edge and isolation-edge sidewalls and the bottom junction, and

$$f_{breakdown} = 1 + XJBVS \cdot \exp\left(-\frac{q \cdot (BVS + V_{bs})}{NJS \cdot kT}\right)$$

In the above equation, when *XJBVS* = 0, no breakdown will be modeled.

diomod == 1 (breakdown-free):

The exponential IV term is linearized at *IJTHSFWD* in the forward-bias mode only.

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{qV_{bs}}{NJS \cdot kT}\right) - 1\right] + V_{bs} \cdot G_{\min}$$

diomod == 2 (resistance-and-breakdown):
The exponential term is linearized at both *IJTHSFWD* in the forward-bias mode and *IJTHSREV* in the reverse-bias mode.

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{qV_{bs}}{NJS \cdot kT}\right) - 1\right] \cdot \left[1 + XJBVS \cdot \exp\left(-\frac{q(BVS + V_{bs})}{NJS \cdot kT}\right)\right] + V_{bs} \cdot G_{\min}$$

- **Diode CV model**

  The BSIM4 junction diode CV models use equations similar to those of BSIM3v3.2.2, but with separate model parameters used (listed above) for S/D junctions.

Note: The impact of device layout/geometry on the diode IV and CV modeling is given in the section on layout-dependent parasitics model.

Modeling Series/Parallel Devices

- **General**

BSIM4 provides a comprehensive and versatile geometry (layout)-dependent parasitics model. This model supports series (such as isolated, shared, or merged S/D) and multi-finger device layout, or a combination of these two configurations.

- **Model parameter and selector**

Parameter name	Specified on	Description	Default value with unit	Binnable ?	Note
perMod	Model card	Whether Ps/Pd (when given) includes the gate-edge perimeter	1 -including the gate-edge perimeter	NA	-
geoMod	Model card Instance	Specify how the end S/D diffusions are connected	0 (isolated)	NA	-
rgeoMod	instance	Specify the end S/D contact type: point, wide or merged, and how S/D parasitic resistance is computed	0 – no S/D diffusion resistance	NA	-
rgateMod	Model card instance	Select different gate resistance models	0 – no gate resistance	NA	-
DMCG	Model card	Distance from the contact center to the gate edge	0m	No	-
DMCI	Model card	Distance in the channel length direction from the contact center to the isolation edge	*DMCG*	No	-
DMDG	Model card	Same as *DMCG* but for merged devices only	0m	No	-
DMCGT	Model card	*DMCG* in test structures	0m	No	-
NF	instance	Number of device fingers	1	No	Note-1
DWJ	Model card	Offset of the S/D junction width due to variations	*DWC* – used in CV model	No	-
MIN	instance	Whether to minimize the number of drain or source diffusions for even-number finger only	0 – minimize the drain diffusion numbers	No	-
RSHG	Model card	Gate electrode sheet resistance per square	0 ohm/square	No	-
XGW	Model card	Distance from the gate contact to the channel edge	0m	No	-
XGL	Model card	Offset of the gate length due to variations in patterning	0m	no	-
NGCON	Model card	Number of gate contacts	1	no	Note-2

Note-1: if less than 1, fatal error;
if greater than 500, a warning message is given and reset to 20.
Note-2: if less than 1, fatal error;
if not equal to 1 or 2, a warning message is given and reset to 1.

- **Details**

In the following, only the source-side case is illustrated. The same approach is used for the drain side.

Calculation of Pseff and Aseff

If (Ps is given)
  If (permod=0)
    Pseff=PS
  Else
    Pseff=PS – Weffcj * NF
Else
  Pseff computed from NF, DWJ, GEOMOD, DMCG, DMCI, DMDG, DMCGT, and MIN.

If (As is given)
  Aseff=AS
Else
  Aseff computed by NF, DWJ, GEOMOD, DMCG, DMCI, DMDG, DMCGT, and MIN.

NOTE: Pseff and Aseff will be used in junction diode IV and CV evaluations. Pseff itself does not include the gate-edge perimeter. In other words, the total source junction perimeter is equal to (Pseff + Weffcj * NF).

Calculation of S/D resistance

If (***rgeoMod*** == 0)
  The diffusion resistance Rs and internal source node sNodePrime are not generated
Else if (the number of source squares NRS is given)
  Rs=NRS * Rsheet
Else
  Rs computed from NF, DWJ, GEOMOD, DMCG, DMCI, DMDG, DMCGT, and MIM.

Calculation of Weffcj

Weffcj, per-finger device junction width, is used in computation of parasitics, GIDL and bias-dependent *Rds*(V), not used to compute Ids, intrinsic CV and overlap CV. Weffcj is defined as

$$Weffcj = \frac{W_{drawn}}{NF} - 2\cdot\left(DWJ + \frac{Wlc}{L^{Wln}} + \frac{Wwc}{W^{Wwn}} + \frac{Wwlc}{L^{Wln}W^{Wwn}}\right)$$

Definition for Wdrawn, PS, PD, AS and AD in the instance line

These instance parameters are defined as the total values for a multi-finger device, not the values for each finger.

- ***geoMod* option**

geoMod	End source	End drain	Note
0	isolated	isolated	*NF=Odd*
1	isolated	shared	*NF=Odd, Even*
2	shared	isolated	*NF=Odd, Even*
3	shared	shared	*NF=Odd, Even*
4	isolated	merged	*NF=Odd*
5	shared	merged	*NF=Odd, Even*
6	merged	isolated	*NF=Odd*
7	merged	shared	*NF=Odd, Even*
8	merged	merged	*NF=Odd*
9	sha/iso	shared	*NF=Even*
10	shared	sha/iso	*NF=Even*

NOTE: All inside S/D are assumed shared. For end S/D, Pseff, Pdeff, Aseff, Adeff are all ***geoMod*** dependent.

- ***rgeoMod* option**

rgeoMod	End-source contact	End-drain contact
0	No *Rs*	No *Rd*
1	wide	wide
2	wide	point
3	point	wide
4	point	point
5	wide	merged
6	point	merged
7	merged	wide
8	merged	point

NOTE: Wide contacts are assumed for all inside S/D. The computation of *Rs* and *Rd* also depends on the setting of ***geoMod***.

- **Diode saturation current and capacitances**

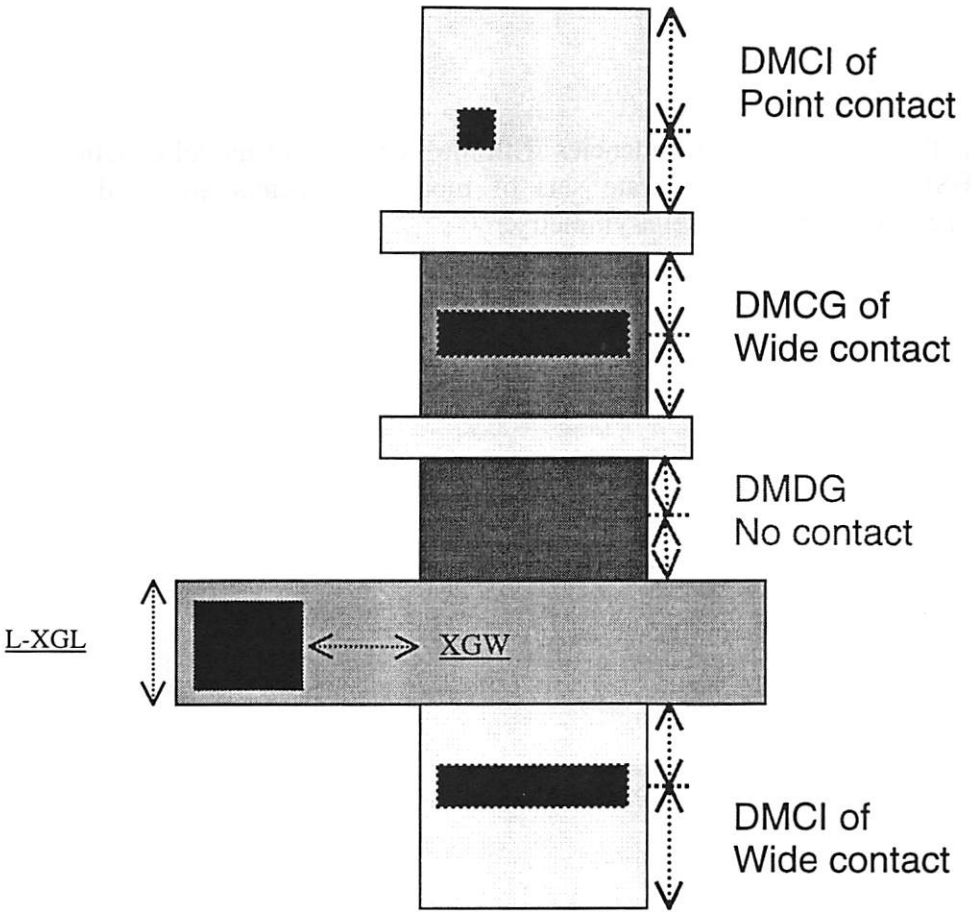
Saturation current is computed as
if ((Aseff <= 0.0) and (Pseff <= 0.0))
  Isbs = 1.0e-14;
Otherwise
  Isbs = Aseff * unitAreaIsbs + Pseff * unitLengthSidewallIsbs + Weffcj * NF
    * unitLengthGateSidewallIsbs;

Zero-bias junction capacitances are calculated by
Bottom junction: czbs = unitAreaJctCap * Aseff;
Isolation-edge sidewall: czbssw = unitLengthSidewallJctCap * Pseff;
Gate-edge sidewall: czbdswg = unitLengthGateSidewallJctCap * Weffcj * NF;
Total zero-bias Source junction capacitance: czbs = czbs + czbssw + czbsswg.

- ***rgateMod* options**

Please refer to the section on "Electrode and intrinsic input resistance model".

- **Definition for layout parameters**



Modeling Temperature Dependence

- **General**

  BSIM4 models the temperature dependencies with the same sets of model equations as those in BSIM3v3.2.2. But separate sets of model parameters are used for source/drain junction diodes to model asymmetry.