High-Q Strong Coupling Capacitive-Gap Transduced RF Micromechanical Resonators

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By

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Abstract

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This dissertation presents a hierarchical, intuitive, and technology agnostic procedure for designing RF channel-select filters, followed by an actual demonstration solidly confirming the validity of the design method. Two distinct methods then follow that aim to increase the resonator electromechanical coupling coefficient, which substantially improves the functionality of the demonstrated filter for future applications, e.g., ones that require higher-order with sharper roll-off characteristics and less passband ripple. To increase functionality even further, the remaining chapters of this thesis introduce a fabrication and post-processing method using CMOS-compatible ruthenium metal that allows integration of micromechanical devices, such as the aforementioned RF filters, atop CMOS.

Chapter 2 introduces design, fabrication, and experimental demonstration of a differential input/output RF channel-select micromechanical disk filter consisting of 96 mechanically coupled capacitive-gap-transduced polysilicon disk resonators, centered at 224MHz with only 0.1% (9kHz) bandwidth, all while attaining 2.7dB insertion loss and more than 50dB out-of-channel stopband rejection. Combined with inherent high-*Q*'s of capacitive-gap disk resonators, sub-40nm transduction gaps enabled by the sidewall sacrificial layer fabrication technology and defensive design strategies employing buffer disks against fabrication residual stress were instrumental in obtaining this impressive performance with decent yield and RF-compatible 590Ω filter termination impedance. Perhaps most encouraging, the equivalent circuit model developed for this complicated structure based on mechanical and electrical parameters was spot on in capturing not only the ideal filter response, but also the parasitic nonidealities that might distort the filter performance.

Having presented an initial RF channel-select filter demonstration, Chapters 3-5 then focus on design methods and fabrication techniques that could raise the filter performance one step further by substantially increasing the electromechanical coupling coefficient of its constituent resonators. Specifically, Chapter 3 introduces a new type of a resonator formed via hollowing out a capacitive-gap transduced radial mode disk resonator that achieved a measured electromechanical coupling strength (C_x/C_o) of 0.75% at 123 MHz without the need to scale the device's meager 40-nm electrode-to-resonator gap. This is almost 7× improvement in C_x/C_o compared with a conventional radial contour-mode disk at the same frequency, same dc bias, and same gap. C_x/C_o increases like this should improve the passbands of channel-select filters targeted for low power wireless transceivers, as well as lower the power consumption of MEMS-based oscillators.

Considering the dependence of the electromechanical coupling on the actuation gap is inverse cubic compared to the linear dependence on mass, Chapters 4-5 attempt to obtain strong coupling by reducing the actuation gaps to below 10nm from their current 37nm. To realize this, one must first overcome fabrication-related hurdles such as precise thin film residual stress control, smooth post-etch sidewalls free of asperities, and sub-10nm sacrificial layer conformal deposition. Chapter 4 attacks the first hurdle by introducing an on-chip strain measurement device that harnesses precision frequency measurement to precisely extract sub-nm displacements, allowing it to determine the residual strain in a given structural film with best-in-class accuracy, where stress as small as 15MPa corresponds to 2.9nm of displacement. The importance of attaining such accuracy manifests in the fact that knowledge of residual strain might be the single most important constraint on the complexity of large mechanical circuits, such as RF channel-select filters.

Chapter 5 then addresses the remaining hurdles for achieving sub-10nm gaps by using a modified polysilicon etch recipe that generates considerably smoother sidewalls and an atomic layer deposited (ALD) 8nm-thick conformal SiO_2 sidewall sacrificial layer. The single-digit-nanometer electrode-to-resonator gaps demonstrated in this chapter have enabled 200-MHz radial-contour mode polysilicon disk resonators with motional resistance R_x as low as 144Ω while still posting Q's exceeding 10,000, all with only 2.5V dc-bias. The tiny motional resistance, together with (C_x/C_o)'s up to 1% at 4.7V dc-bias and (C_x/C_o)-Q products exceeding 100, propel polysilicon capacitive-gap transduced resonator technology to the forefront of MEMS resonator applications that put a premium on noise performance, such as radar oscillators. Simultaneous high-Q and strong electromechanical coupling (C_x/C_o) makes this technology attractive for future sharp roll-off, flat passband RF channel-select filters targeted for low power receivers as well as wide band filters targeted for the LTE bands.

The decent resonator performance offered by polysilicon structural material with Q's exceeding 10,000 at 200MHz comes with a drawback that LPCVD polysilicon with deposition temperatures of 590-615°C is not directly integrable atop CMOS due to thermal budget constraints. Pursuant to mitigating this issue, Chapter 6 introduces a fabrication and post-processing method using CMOS-compatible ruthenium metal that allows integration of micromechanical devices atop CMOS. Specifically, introduction of tensile stress via localized Joule heating has yielded some of the highest metal MEMS resonator Q's measured to date, as high as 48,919 for a 12-MHz ruthenium micromechanical clamped-clamped beam. The low-temperature ruthenium metal process, with highest temperature of 450°C and paths to an even lower ceiling of 200°C, further allows for MEMS processing over CMOS wafers offering a promising route towards monolithic realization of CMOS-MEMS circuits needed in communication transceivers.

Finally, Chapter 7 fulfills the promise of this dissertation in metals, i.e., *simultaneous* high-Q and strong coupling, by employing a 20-nm-gap CMOS-compatible flexural-mode square-plate resonator constructed in thermal-annealed ruthenium metal that posts quality factors (Q's) exceeding 5,000 and an impressive transducer strength C_x/C_o (equivalent to k_t^2) of up to 71% intrinsic and 36% with 55fF of bond capacitance loading, which in turn permits more than 46% voltage-controlled resonance frequency tuning (from 18.005 to 9.713MHz) with a voltage excursion from 0.5 to 2.8V. The 36% C_x/C_o is 75 times larger than the 0.48% of published AlN piezoelectric material in this HF frequency range. With processing temperatures potentially below 350°C (using localized annealing), this metal resonator is amenable to integration directly over even advanced node CMOS, making this technology attractive for single-chip widely tunable filter and oscillator applications, e.g., for wireless communications.

Dedicated to my parents.

None of this would have been possible without their unconditional love and support.

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Chapter 1
Introduction

Wireless communications with applications touching upon wide-ranging areas such as from the most complicated military and defense needs to our simplest daily routines has become an indispensable part of the contemporary society. Especially, the rapid proliferation of smartphones in the last decade has substantially increased the number of wireless users creating an ever-growing demand for faster data rates with minimal power consumption much needed for longer battery life. Such a need of course has attracted significant research and investment in both university and industry level to achieve the most efficient wireless communication scheme in an already congested electromagnetic spectrum by employing novel hardware solutions as well as utilizing optimization in the software level for the upcoming 5G networks. Recent multi-billion dollar company acquisitions between technology companies working in this field further hint that research and development on wireless communication systems will continue as the worldwide user demand keeps growing.

Although smartphones and cellular communication serve as ideal vehicles to explain the impact of wireless communications in our lives, military applications have always become the main driver behind the advances in this field starting from the World War I and II days. It is no surprise than that today almost all military gadgets, aircrafts, naval ships, and missiles etc. heavily depend on reliable wireless communication links able to survive and correctly function in harsh environments such as extreme temperature, force, acceleration, and impact. For this reason, most nations allocate significant resource supporting wireless research and development not to fall behind in this technological competition.

Internet of Things (IoT) envisioning massive connected sensor networks, i.e., trillions of sensors, has recently emerged as another driver behind wireless communications research both in hardware and software level. Operating on a set-and-forget type scheme with battery, these wireless motes put a premium on power consumption at the expense of reduced data rate. Potential applications for such a connected sensor network are enormous, ranging from smart cities and industrial process control to wearables and environmental monitoring.

1.1. Brief History

After James C. Maxwell's theoretical prediction of electromagnetic waves in 1864 [1], Heinrich Hertz was the first to generate these waves through a set of experiments and prove their existence in 1887 [2]. Fig. 1.1 depicts a simplified schematic of Hertz's original experiment. Here, a dc voltage source connected to the primary of an induction coil through an electrical switch supplies the input power. Two capacitor plates large enough to hold substantial amount of charge are connected to each end of the secondary coil and separated by a tiny air gap. Similar to the automobile ignition system, periodically opening and closing the electrical switch creates a back-emf in the circuit creating a huge alternating electrical field across the tiny gap between the two straight metal roads attached to the capacitor plates and causing a spark discharge in the air gap. Placed at a

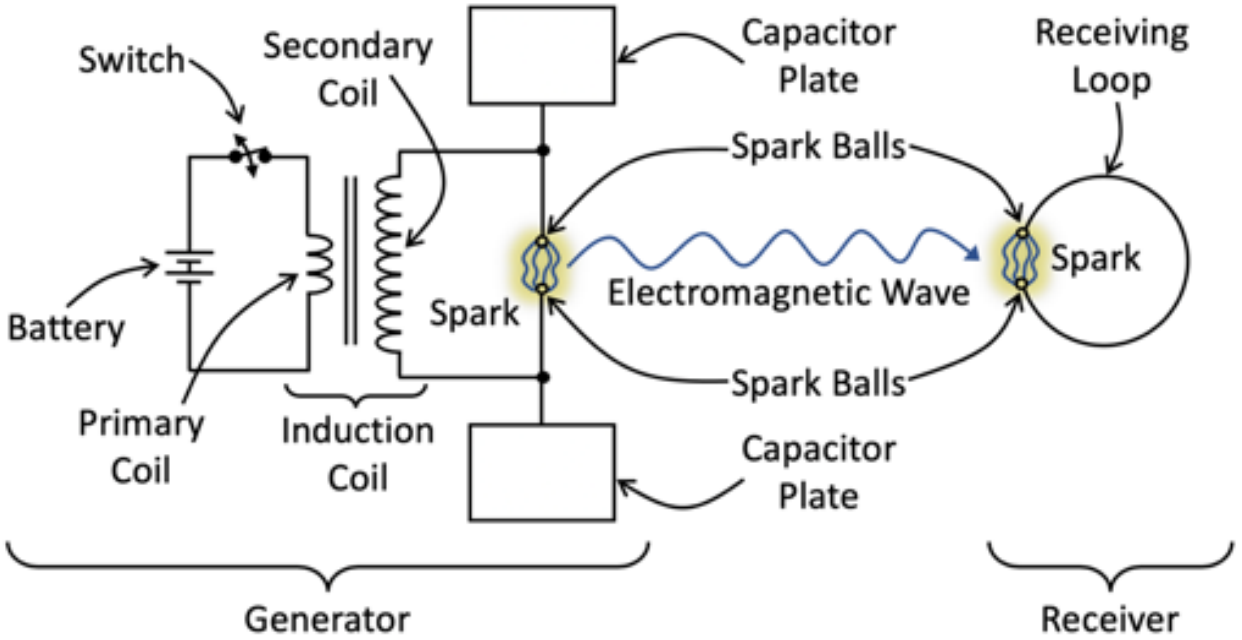


Fig. 1.1: Hertz's original experimental setup to prove the existence of electromagnetic waves first theoretically predicted by Maxwell.

certain distance from the transmitting circuitry, a ring-shaped conductor with two spark balls at each end separated with a tiny air gap acts as a receiver for picking up any electromagnetic wave generated by the spark discharge. Using this simple experimental setup, Hertz showed that any spark discharge in the generator circuit also triggers a resulting spark in the ring receiver proving the existence of electromagnetic waves travelling in free space.

However, it wasn't until Guglielmo Marconi that the spark gap transmission had been employed for wireless communication. Marconi firstly replaced the spark gap in the receiving end with a more sensitive coherer which is basically an iron powder-filled vacuum tube with electrical connections on both ends [3]. The electrical resistance of the iron filings inside the tube dramatically reduces when there is an incident electromagnetic wave making it a very sensitive wireless detector. Marconi also replaced the huge capacitor plates of the Fig. 1.1 spark generator with wires — one directly connected to the earth and the other as elevated as possible in the air literally using kites both in the transmitting and receiving ends as Fig. 1.2 shows. Other than increasing the transmit/receive efficiency, such an elevated antenna concept enabled this very first wireless radio to avoid geographical barriers yielding a much enhanced transmission distance. From 1897-1899, Marconi demonstrated the first wireless telegraphy both in England and the United States [4].

A major issue with the early wireless receivers was their vulnerability to strong blocker signals radiated by other nearby transmitters masking the desired weak signal of interest. Inspired by Sir Oliver Lodge's notion of tuning, Marconi solved this problem by placing a tapped inductor and a tunable Leyden jar capacitor in series with the aerial antenna to limit the range of frequencies radiated by the spark gap generator and received by the coherer. By tuning the Leyden jar capacitor on the receiving end to match the transmission frequency, i.e., tuning the transmitter and receiver into resonance, the receiver only detects the desired signal and filters out all the other interferers radiated by the other transmitters.

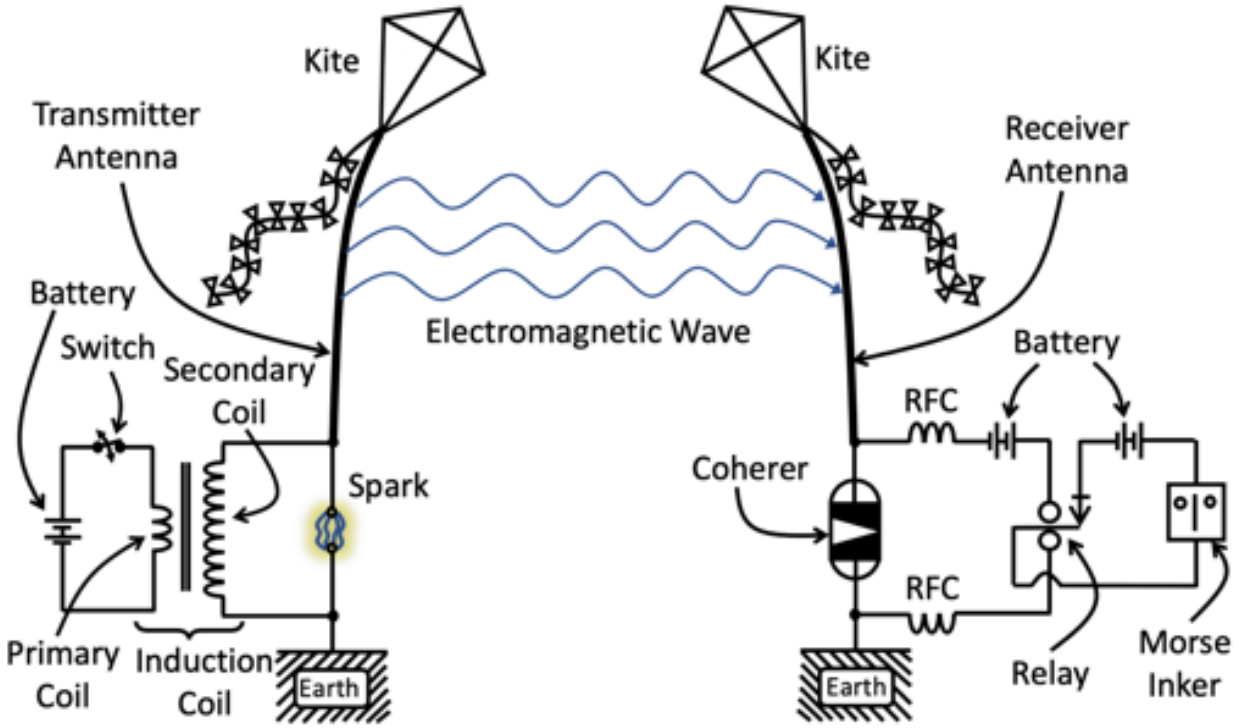


Fig. 1.2: Marconi's transmitter and receiver circuit diagrams employed in the early demonstration of the wireless telegraphy [4].

Finally, after all these improvements, Marconi achieved the first long wave transatlantic transmission in 1901, i.e., the Morse code for letter 'S', from the coast of England to the coast of Canada by using a 25kW transmitter and antennas comprised of fifty 50-meter-high copper wires [4].

1.2. Conventional Transceivers

A. Super-Heterodyne Receiver

Since its invention by Edwin Armstrong in 1918 to further improve the receiver sensitivity to transmitted spark signals [5], the super-heterodyne structure has been the most widely used receiver architecture in extremely high sensitivity radios. Although the full super-heterodyne receiver operation looks fairly complicated as Fig. 1.3 shows, the main idea behind it is quite simple consisting of two separate frequency down-conversion steps:

i) RF-to-IF conversion in Fig. 1.3(a): converts the high frequency RF carrier signal picked up by the antenna to an intermediate frequency (IF)
ii) IF-to-baseband conversion in Fig. 1.3(b): demodulates the intermediate frequency (IF) signal to the baseband frequency for further processing by the subsequent electronic stages

As mentioned previously, today's wireless communication systems transmit baseband information signals through a modulated high frequency carrier signal in a pre-assigned RF channel consisting of certain bandwidth due to difficulties imposed by antenna size limitations at low baseband frequencies. Considering that the desired receive signal is usually pretty weak due to transmission path losses and there might be another user transmitting a much stronger signal in an

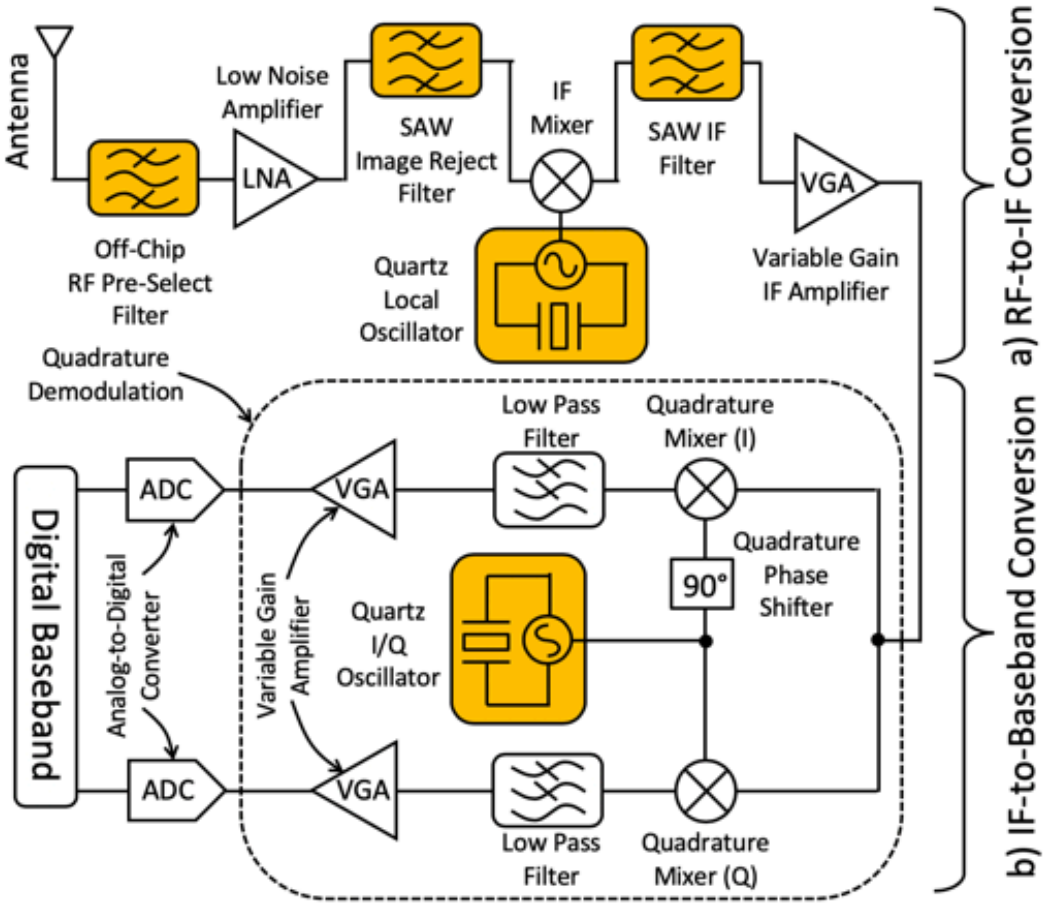


Fig. 1.3: Super-heterodyne receiver architecture a) RF-to-IF conversion. b) IF-to-baseband conversion.

adjacent RF channel, i.e., as much as 60dB for LTE [6] and 80dB for GSM [7], the receiver circuitry must be extremely linear to handle such a huge dynamic range to function properly. Otherwise, the strong out-of-channel interferers might mix and fall into the operating channel through receiver nonlinearity by generating intermodulation products stronger than the desired signal as depicted in Fig. 1.4. Attaining such a linearity at high RF carrier frequencies to accommodate the large dynamic range, however, comes with a highly undesirable power consumption penalty, especially in today's handheld and battery-powered devices.

To relax the dynamic range requirements for the demodulating circuitry, the top portion of the super-heterodyne architecture of Fig. 1.3, i.e., RF-to-IF conversion, filters out the out-of-channel interferers in two distinct steps by employing off-chip mechanical filters and down-converts the carrier signal to a lower intermediate frequency (IF). Specifically, an off-chip wideband RF pre-select filter immediately after the antenna considerably attenuates out-of-band signals residing in the adjacent bands as shown in Fig. 1.4(b). Here, the lack of low insertion loss RF channel-select filters consisting of extremely high-Q resonators forces designers to only employ band selection without introducing too much insertion loss to the already weak receive signal. It is also important to note that the filter insertion loss directly contributes to the noise figure of the receive electronics chain degrading the overall signal-to-ratio (SNR). In addition to keeping the RF pre-select filter insertion loss at a minimum, a low-noise amplifier (LNA) that follows amplifies the weak receive

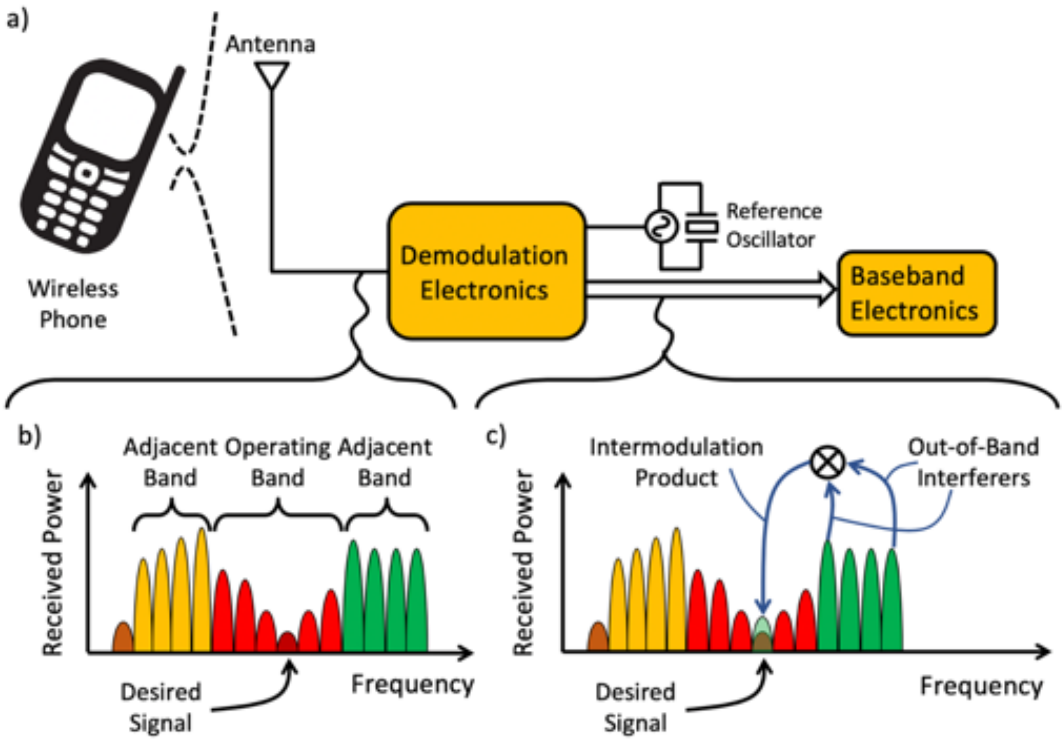


Fig. 1.4: (a) A hypothetical communication receiver without filtering before demodulation electronics. (b) Typical frequency spectrum of power received by antenna showing out-of-band and out-of-channel interferers much stronger than the desired signal. (c) Formation of an intermodulation product masking the desired signal due to nonlinearities in the demodulation electronics circuitry.

signal to prevent subsequent stages from deteriorating the noise figure per the Friis' equation below [8]

$$F_{total} = IL_{RF} + F_{LNA} + \frac{F_2 - 1}{G_{LNA}} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \tag{1.1}$$

where IL_{RF} is the insertion loss (or noise figure) of the RF pre-select filter, F_{LNA} is the noise figure of the LNA, G_{LNA} is the gain of the LNA, F_i and G_i are noise factor and power gain of the i^{th} stage in an n-stage system, respectively, the noise figures of the RF pre-select filter and subsequent low-noise amplifier (LNA). With high enough LNA gain, the stages that follow the LNA do not significantly contribute to the receive chain noise figure.

Next, a mixer stage using a local oscillator (LO) signal provided by a tunable voltage controlled oscillator (VCO) phase locked to a highly stable lower frequency off-chip quartz crystal oscillator down-converts the filtered and amplified RF signal to an intermediate frequency where selecting a channel is much easier since the required filter percent bandwidth significantly reduces. To prevent the mixer from converting the image of the actual RF signal around the LO frequency, however, a mechanical off-chip surface acoustic wave (SAW) image reject filter first filters out the image frequency component before feeding the signal to the IF mixer that follows. Once the down conversion is complete, another off-chip SAW filter this time performs the channel selection at IF as mentioned, followed by another amplification stage. As not readily obvious from Fig. 1.3, it is important to note that the LO signal fed to the IF mixer must be tunable to keep the IF frequency

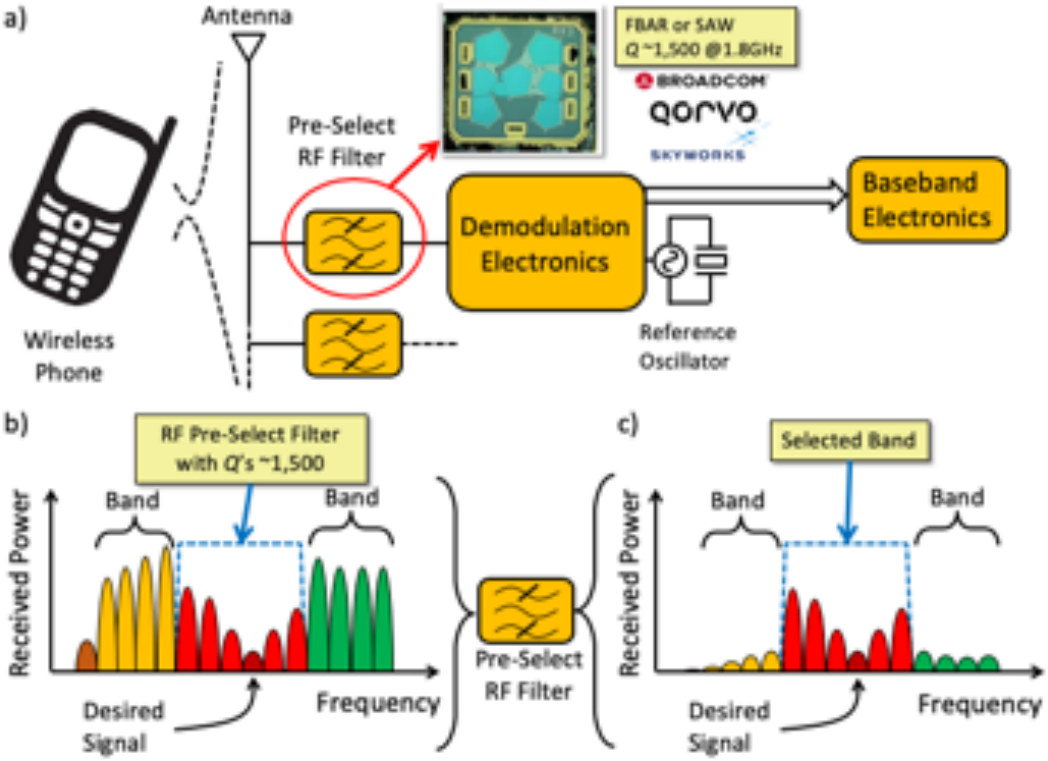


Fig. 1.5: a) A revised receiver architecture with RF pre-select filters included. b) Typical frequency spectrum of power received by antenna. c) Same frequency spectrum of (b) after wideband filtering through an RF pre-select filter with resonator Q's of 1,500.

constant since the RF carrier frequency is always subject to change depending on the current RF channel assignment. Making the LO frequency tunable allows for using a constant frequency channel-select filter at IF without requiring tunability, which is usually not an easy task for narrowband filters, at the expense of increased power consumption and complexity introduced by the phase-locked loop (PLL) in the VCO circuit.

The rest of the super-heterodyne circuit presented in Fig. 1.3(b) simply demodulates the signal at IF frequency to the baseband by employing quadrature modulation. Quadrature modulation entails mixing the IF signal with an LO signal at IF frequency provided by an off-chip highly stable crystal oscillator at two different phases with 90° apart to generate I/Q amplitudes proportional to the original signal's real and imaginary components by removing the need to synchronize phases between the transmitter and receiver. A low pass filter (LPF) that follows then only selects the baseband component filtering out the higher frequency mixing component. After another stage of amplification, an analog-to-digital converter (ADC) digitizes the signal and baseband processing starts.

Although the super-heterodyne architecture is the choice for sensitive radios, several off-chip components that must interface with the receiver circuit significantly increases power consumption as well cost. As the RF pre-select filter can only achieve band selection, rather than channel selection, the VCO-generated IF mixer LO signal must have a decent phase noise performance necessitating an off-chip crystal reference and power-hungry PLL circuit. If RF channel selection directly after antenna were possible, even a noisy VCO would be sufficient for IF mixing leading to a lower power operation.

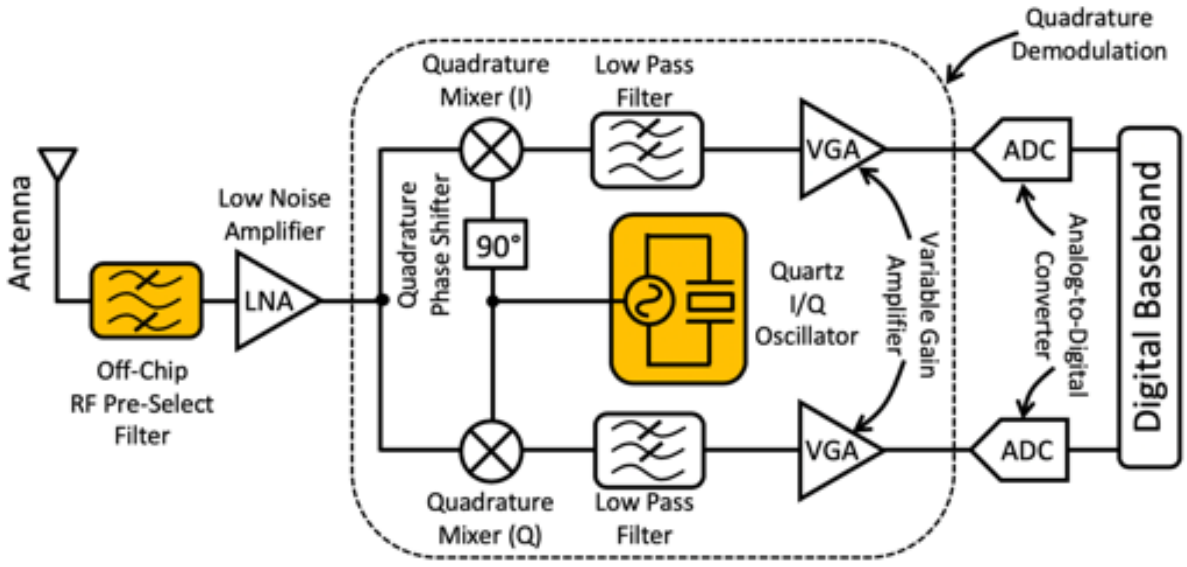


Fig. 1.6: The direct conversion receiver architecture.

B. Direct Conversion Receiver

Compared to super-heterodyne receiver, direct conversion receiver completely skips the IF stage by demodulating the signal right after the LNA as shown in Fig. 1.6. Such an approach eliminates the need for image reject and IF SAW filters in the IF stage reducing the number of off-chip filters from three to one, which provides significant savings. In addition, the removal of the power-hungry PLL circuit and the off-chip crystal reference in the IF mixer VCO circuit reduces the complexity and saves even more power. Also, as the LNA now directly interfaces with the quadrature mixers with fairly high input impedance, the LNA design requirements becomes more relaxed.

Although direct conversion receiver reduces the design complexity quite a bit by eliminating some off-chip components, it also significantly increases the dynamic range that the demodulation circuit must handle as there is no channel selection filtering strong out-of-channel interferers whatsoever. Such an increase in the dynamic range manifests itself with a tighter linearity specification for the demodulation circuit, hence increased power consumption.

As the previous discussion so far hinted several times, the most important bottleneck preventing low power receiver operation is the presence of strong interferers in adjacent channels necessitating multiple off-chip filters, off-chip crystal reference clocks, and additional circuit complexity to obtain low phase noise LO signals. Therefore, a filter technology that could achieve RF channel selection eliminating all out-of-channel interferers right after the antenna hence removing the need for any additional IF filters and relaxing the demodulation circuit dynamic range for low power wireless communication is much needed.

1.3. RF Channel Selection

The power consumption of a radio generally goes as the number and strength of the RF signals it must process [9], [10], [11]. In particular, a radio receiver would consume much less power if the signal presented to its electronics contained only the desired signal in a tiny percent bandwidth frequency channel and no interferers. A recent MEMS-based RF channel-selecting super-regenerative receiver demonstrates this [12], even if only for small bit rates. At higher bit rates, however,

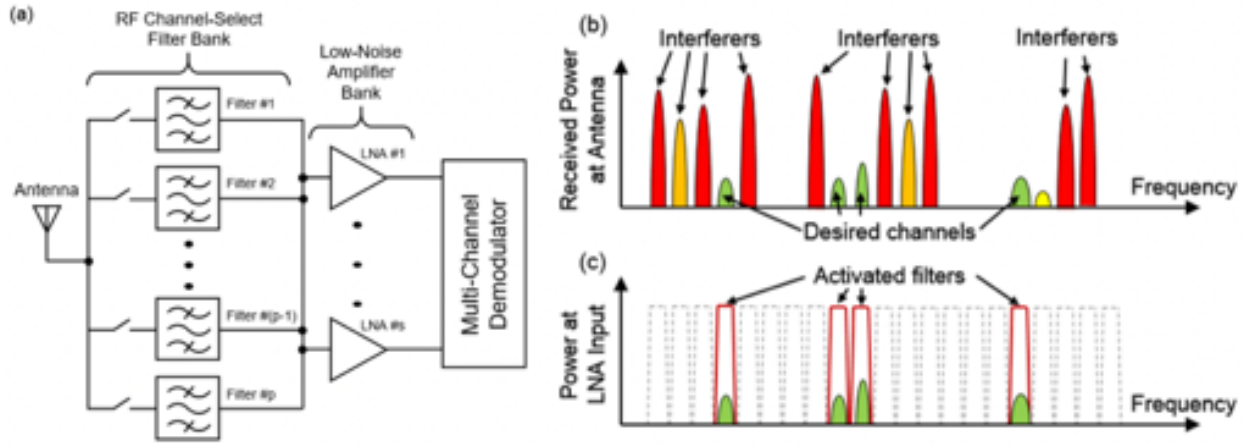


Fig. 1.7: (a) Direct conversion receiver architecture combined with an RF-channel select filter bank capable of eliminating in-band blockers directly at the RF front-end. (b) Cartoon description of a possible multi-carrier power spectrum that might appear at the antenna of an advanced multi-carrier communication system. (c) On/off configuration of the filters in the RF channelizing filter bank that selects only the desired channels.

RF channel-selection is rare. Instead, the typical mix of signals includes unwanted energy outside the desired channel that may be much stronger than the desired signal, by as much as 60dB for LTE [6] and 80dB for GSM [7]. The more unwanted energy present, the higher the dynamic range required of the electronics, hence, the larger the power consumption. Unfortunately, a lack of filters capable of selecting single channel bandwidths at RF forces the front-ends of contemporary receivers to accept unwanted signals, and thus, to operate with sub-optimal efficiency. Indeed, FBAR or SAW filters, while adept at RF *band*-selection, do not possess sufficient quality factor Q to manage practical RF *channel*-selection without undue insertion loss.

It is no surprise, then, that attempts to realize RF filters with percent bandwidths in the range of 0.1% sufficient to remove all interfering signals, leaving only energy in the desired RF channel, are abundant in the literature [13]. Because the bandwidths of such RF channel-selecting filters are so small, and technologies capable of attaining the needed Q's are generally not widely tunable, much of the research has focused on micro-scale filters that can assemble into banks of weakly tunable filters, *cf.* Fig. 1.7, to cover a target communication band.

1.4. Need for Simultaneous High-Q and Strong Electromechanical Coupling

Because it offers tiny size and very high Q, many research approaches to RF channel-selection focus on MEMS technology. These studies employ various resonator technologies using piezoelectric [14], [15], [16], [17], internal dielectric [18], [19], and capacitive-gap [20], [21], [22], [23], [24] actuation. Unfortunately, so far none of the explored approaches truly achieves the needed performance, which demands not only small percent bandwidth, but also low passband insertion loss and high stop-band rejection. Several approaches explored thus far use resonators, e.g., based on piezoelectric materials [14], [15], that lack the needed Q to achieve low insertion loss in so small a percent bandwidth. For example, one attempt to use conventional attached-electrode piezoelectric resonators does achieve the needed 0.1% bandwidth, but only with excessive passband loss on the order of 15dB [14], which is clearly not permissible immediately after the antenna.

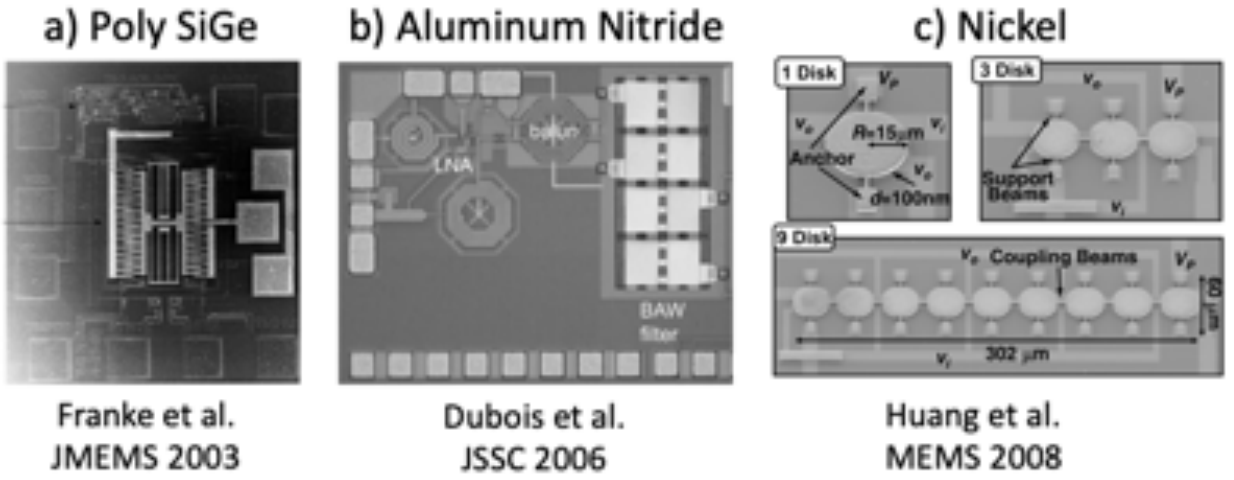


Fig. 1.8: Previous CMOS-MEMS integration attempts using MEMS-last approach with a) Poly-crystalline silicon germanium (Poly SiGe) b) Aluminum nitride (AlN) c) Nickel MEMS resonator materials.

On the other hand, approaches that attain sufficient *Q*'s on the order of 10,000, e.g., capacitive-gap transduced resonators, so far do not possess enough electromechanical coupling to attain 50dB stop-band rejection at UHF. In particular, although the design of [25] achieves the needed 0.06% bandwidth with an insertion loss of only 2.5dB, it does so with only 27dB of stop-band rejection. It also requires rather large termination impedances on the order of 1.5kΩ that necessitate the use of inductors to resonate out shunt input and output capacitance. Finally, its yield of devices with adequately small passband ripple is quite low.

More recent work using a "capacitive-piezoelectric" transducer that combines capacitive and piezoelectric transduction to realize a resonator with simultaneous high *Q* and coupling [26], [27] seems poised to eventually achieve RF channel-select filters with appropriate insertion loss and stop-band rejection characteristics. The work of [26], however, demonstrates only a single-resonator that provides only a 2-pole frequency shaping transfer function. Most RF front-ends require at least 4-pole shaping characteristics, i.e., two resonators. Perhaps most importantly, if one transducer technology alone—e.g., one of capacitive-gap or piezoelectric, but not both—can be shown sufficient to achieve the needed filter characteristic, then this would likely be the more cost-effective approach.

1.5. Monolithic CMOS Integration

CMOS-MEMS integration has always enticed MEMS researchers since such a monolithic approach, if realized without significant performance degradation, would drastically reduce the power consumption of MEMS oscillators and filters by eliminating all undue parasitics originating from bond-wired two-chip approach as well as increase the overall functionality by allowing seamless and complex coexistence of mechanical and electrical components on a single chip, leading to a true electro-mechanical circuit on chip.

Previous attempts to achieve monolithic integration have mostly employed two different approaches: MEMS-first and MEMS-last — each having its own advantages and drawbacks. In the former, transistor circuit fabrication follows atop the MEMS devices putting no constraint on the thermal budget of the MEMS fabrication process, however creating concerns over contamination in the CMOS fabrication line caused by pre-processed MEMS wafers. For this reason, MEMS-last

approach entailing MEMS device fabrication atop a finished CMOS wafer has recently gained more popularity as it allows for a wide-range of CMOS foundry options. However, such an approach places an upper temperature threshold of 500°C (even lower for the advanced node CMOS) during MEMS processing to avoid destroying the underlying transistor circuits, hence limiting the MEMS interconnect and structural layer material choices to only low-temperature deposited materials. To this end, polycrystalline silicon germanium material shown in Fig. 1.8(a) possess the required low deposition temperature of 450°C and inherent high-Q behavior, however its large interconnect resistance incurs additional parasitic losses preventing the MEMS resonator from achieving its true potential [28]. As Fig. 1.8(b) depicts, low-temperature sputtered aluminum nitride (AlN) with its strong electromechanical coupling in resonator applications is another candidate for monolithic integration [29]. However, the large parallel capacitance inherent to piezoelectric resonator technology unfortunately does not allow substantial power reduction especially for oscillator applications. Another material group that deposit at low temperatures through evaporation, sputtering, or electroplating but usually not considered for high-Q resonator applications is metals. As shown in Fig. 1.8(c), fabricating nickel disk resonators via electroplating atop CMOS circuits resolves the large interconnect resistance and shunt device capacitance issues associated with polycrystalline and aluminum nitride, respectively, however nickel disk resonators in this study suffer from low-Q and frequency stability problems. This dissertation continues to investigate metals as a potential candidate for CMOS-MEMS monolithic integration by dispensing with nickel and introduces ruthenium as a viable choice with performance comparable to or better than its other micromachinable counterparts once properly post-processed.

1.6. Dissertation Overview

This dissertation presents a hierarchical, intuitive, and technology agnostic procedure for designing RF channel-select filters, followed by an actual demonstration solidly confirming the validity of the design method. Two distinct methods that followed aimed at increasing the resonator electromechanical coupling coefficient to substantially improve the functionality of the demonstrated filter for future applications that require higher-order filters with sharper roll-off characteristics and less passband ripple as well as wider bandwidth. To increase the device functionality even further, the last part of this thesis introduces a fabrication and post-processing method using CMOS-compatible ruthenium metal that allows integration of micromechanical devices such as aforementioned RF filters atop CMOS.

Chapter 2 introduces design, fabrication, and experimental demonstration of a differential input/output RF channel-select micromechanical disk filter consisting of 96 mechanically coupled capacitive-gap-transduced polysilicon disk resonators, centered at 224MHz with only 0.1% (9kHz) bandwidth all while attaining 2.7dB insertion loss and more than 50dB out-of-channel stopband rejection. Combined with inherent high-Q's of capacitive-gap disk resonators, sub-40nm transduction gaps enabled by the sidewall sacrificial layer fabrication technology and defensive design strategies employing buffer disks against fabrication residual stress were instrumental in obtaining this impressive performance with decent yield and RF-compatible 590Ω filter termination impedance. It is also worth noting that the spurious-free filter spectrum achieved in this work with more than 50dB out-of-channel stopband rejection is a direct result of the differential input/output scheme utilized in the design and granted by the flexibility of all-mechanical design. The equivalent circuit model developed for this complicated structure based on mechanical and electrical

parameters was spot on in capturing not only the ideal filter response, but also the parasitic nonidealities that might distort the filter performance.

Having presented an initial RF channel-select filter demonstration, Chapters 3-5 then focus on design methods and fabrication techniques that could take the filter performance one step further by substantially increasing the electromechanical coupling coefficient of the resonators constituting such a filter. Specifically, Chapter 3 dispenses with conventional resonator designs and introduces a new type of a capacitive gap transduced resonator formed by hollowing out a regular solid disk device ("hollow disk resonator") to achieve 0.75% electromechanical coupling strength at 123MHz in the radial contour mode with an actuation gap of 37nm , i.e., almost 7 times increase compared to its solid disk counterpart, with almost negligible change to the conventional disk resonator fabrication process. Although the hollow disk quality factor in the radial contour mode is somewhat lower than what a solid disk could achieve at the same frequency due to transverse component of the mode shape motion radiating energy to the substrate via center stem, i.e., compare 3,512 vs. 20,000, this work also experimentally shows that the wine glass mode shape of the exact same hollow disk device does not have such a shortcoming by posting measured Q's greater than 10,000 in the same frequency range.

Considering the dependence of the electromechanical coupling on the actuation gap is inverse cubic compared to the linear dependence on the mass, Chapters 4-5 attempt to obtain strong coupling by reducing the actuation gaps to levels below 10nm from their current 37nm. To realize such an endeavor, one must first overcome fabrication-related hurdles such as precise thin film residual stress control, smooth post-etch sidewalls free of asperities, and sub-10nm sacrificial layer conformal deposition. Considering compressive stresses as low as 50MPa are sufficient to cause shorts with a sub-10nm-gap 200-MHz upper-VHF polysilicon disk resonator, Chapter 4 attacks the first hurdle by demonstrating an on-chip electrical stiffness-based resonant strain sensor comprised of a spoke-supported ring resonator that could reliably measure residual strains as low as 9.19nε (corresponding to 1.45kPa in a polysilicon thin film layer) to enable process optimization. The dependence is strong enough and frequency measurement precision good enough that even sub-nm gap changes, hence MPa-level stresses, are precisely measurable.

Having optimized the deposition parameters to achieve minimal post-fabrication residual stress by employing such a strain diagnostic presented in Chapter 4 and fabricated alongside real devices, Chapter 5 then addresses the remaining hurdles for achieving sub-10nm gaps by using a modified polysilicon etch recipe that generates considerably smoother sidewalls to reduce the asperities that might otherwise intensify electric fields causing breakdown and an atomic layer deposited (ALD) 8nm-thick SiO_2 sidewall sacrificial layer defining the record narrow transduction gap achieves perfect conformality. Single-digit-nanometer electrode-to-resonator gaps successfully presented in this chapter have enabled 200-MHz radial-contour mode polysilicon disk resonators with motional resistance R_x as low as 144Ω while still posting Q's exceeding 10,000, all with only 2.5V dc-bias. The demonstrated gap spacings down to 7.98nm are the smallest to date for upper-VHF micromechanical resonators and fully capitalize on the fourth power dependence of motional resistance on gap spacing. High device yield and ease of measurement debunk popular prognosticated pitfalls often associated with tiny gaps, e.g., tunneling, Casimir forces, low yield, none of which appear. The tiny motional resistance, together with k_t^2's up to 1% at 4.7V dc-bias and $k_t^2 \cdot Q$ products exceeding 100 render polysilicon capacitive-gap transduced resonator technology suitable for high order RF channel-select filter applications that offers better roll off and less passband ripple —

both become increasingly critical as the wireless spectrum becomes more congested as the number of users constantly increases.

The decent resonator performance offered by polysilicon structural material in previous chapters with Q's exceeding 10,000 at 200MHz comes with a drawback that LPCVD polysilicon with deposition temperatures of 590-615°C is not directly integrable atop CMOS due to thermal budget constraints. For this reason, the adopted two-chip approach to interface micromechanical resonators and filters with the transistor circuits incurs inevitable parasitics causing undue power consumption, performance degradation, and cost increase. In search of materials amenable to direct CMOS-MEMS integration, SiGe meeting the temperature ceiling for previous generation CMOS has emerged as a promising candidate but its high interconnect and structural parasitic resistance significantly compromise the attainable oscillator performance [28]. Sputter-deposited or evaporated nominally at room temperature, metals meet the temperature ceiling requirement even for advanced node CMOS without introducing undue parasitic resistances that could otherwise degrade the performance. Unfortunately, however, to date metals post much lower Q's than their polysilicon, AlN, or diamond counterparts hindering their use as a resonator structural material [30]. To alleviate this, some method without requiring transistor-damaging temperatures is necessary to enhance metal Q if metal is to replace these materials.

Pursuant to this, Chapter 6 introduces one such method that effectively employs tensile stress in ruthenium metal clamped-clamped beam ("CC-beam") resonators for raising their Q to levels significantly better than achievable by their polysilicon counterparts at the same frequency range with very low thermal exposure to underlying transistors. In contrary to previous demonstrations of this technique in silicon nitride strings which necessitate either a very high post-fabrication residual tensile stress in the structural material, i.e., around 1GPa, [31] causing adhesion issues and film delamination later in the process or the use of impractical macroscopic mechanical means involving substrate bending [32], we have shown that a simple device-level localized rapid thermal annealing (RTA) process conveniently induces the required high tension, i.e., on the order of 1GPa, in ruthenium CC-beam resonators by allowing the metal atoms to re-crystallize and become more compact, hence generate tensile stress. Because the needed RTA temperatures exceeding 1000°C are CMOS incompatible and hence a furnace anneal would damage underlying transistor circuits, this work rather utilized a very short current pulse, i.e., on the order of milli seconds, flowing through the CC-beam resonator that locally anneals only the resonator through Joule heating (a.k.a., localized annealing), leaving rest of the chip intact hence minimizing thermal exposure to the transistors beneath. The introduction of tensile stress via this method has yielded some of the highest metal MEMS resonator Q's measured to date, as high as 48,919 for a 11.8-MHz ruthenium micromechanical CC-beam resonator with an actuation gap of 120nm. Compared to its unannealed counterpart with a Q of 180 at 1.2MHz this corresponds to a 270 times increase in Q at a 10 times higher frequency. The high Q's continue into the very high frequency (VHF) range, with Q's of 7,202 and 4,904 at 61 and 70MHz, respectively. These marks are substantially higher than the 6,000 at 10 MHz and 300 at 70MHz previously measured for polysilicon CC-beams, defying the common belief that metal Q cannot compete with conventional micromachinable materials.

Finally, Chapter 7 fulfills the promise of this dissertation in metals, i.e., *simultaneous* high-Q and strong coupling, by demonstrating the Q-boosting concept and thermal annealing method presented in Chapter 6 by employing a 20-nm-gap CMOS-compatible ruthenium metal square-plate resonator. Combining a thermal-anneal-boosted Q of 5,000 at 18MHz with electromechanical coupling coefficients k_t^2's of 71% afforded by 20nm transduction gaps, the ruthenium square plate

resonator introduced in this chapter achieves an impressive $k_t^2 \cdot Q$ figure of merit (FOM) of 274 with only 2.1V dc-bias. Aside from having impressive measured values of Q, k_t^2, and FOM besting even some of the common micromachinable materials, its extremely high transducer efficiency permits more than 46% voltage-controlled tuning range (from 18.005 to 9.713MHz), challenging the common assumption that high-Q resonators are simply not tunable.

Chapter 2
RF Channel-Select Micromechanical Disk Filters

This chapter presents a detailed analysis and advanced equivalent circuit model based on mechanical and electrical parameters that accurately predict the measured behavior, including parasitics and second-order effects, of RF channel-select micromechanical filters, such as designed, fabricated, and experimentally demonstrated in [33]- [34]. The demonstrated differential input/output RF channel-select micromechanical disk filter is centered at 224MHz with only 0.1% (9kHz) bandwidth all while attaining 2.7dB insertion loss and more than 50dB out-of-channel stopband rejection. Combined with inherent high-*Q*'s of capacitive-gap disk resonators, sub-40nm transduction gaps enabled by the sidewall sacrificial layer fabrication technology and defensive design strategies employing buffer disks against fabrication residual stress were instrumental in obtaining this impressive performance with decent yield and RF-compatible 590Ω filter termination impedance. Perhaps most encouraging, the equivalent circuit model developed for this complicated structure based on mechanical and electrical parameters was spot on in capturing not only the ideal filter response, but also the parasitic nonidealities that might distort the filter performance. This implies that the GHz-filters with sub-200-Ω impedances enabled by sub-20-nm transduction gaps predicted by the same model might soon come true, bringing this technology even closer to realizing the ultra-low-power channel-selecting RF front-ends.

2.1. Introduction

This work focuses on the degree to which capacitive-gap transduced micromechanical resonators can achieve the aforementioned RF channel-selecting filters. It aims to first show theoretically that with appropriate scaling capacitive-gap transducers are strong enough to meet the needed coupling requirements; and second, to fully detail an architecture and design procedure needed to realize said filters. It then provides an actual experimentally demonstrated RF channel-select filter designed using the above procedures and confirming theoretical predictions.

The overall micromechanical circuit design hierarchy used here builds upon micromechanical vibrating disk resonators [35] and uses a combination of capacitive actuation gap scaling [36], coupled array-composites [37], electrical stiffness tuning [38], [39], and fabrication process improvements to attain unprecedented RF channel-select performance [34]. It specifically modifies the design of [25] to that of Fig. 2.1, which points out the major design changes [33]. Now, smaller electrode-to-resonator gaps on the order of 39nm amplify the input/output electromechanical coupling by more than 8.6×, which directly contributes to larger stop-band rejection. The new design also introduces additional electrodes around disks specifically tasked for frequency tuning towards higher circuit yields; as well as carefully designed electrode-less buffer devices that alleviate post-fabrication stress, thereby also contributing to higher yield. Combined, these design changes yield

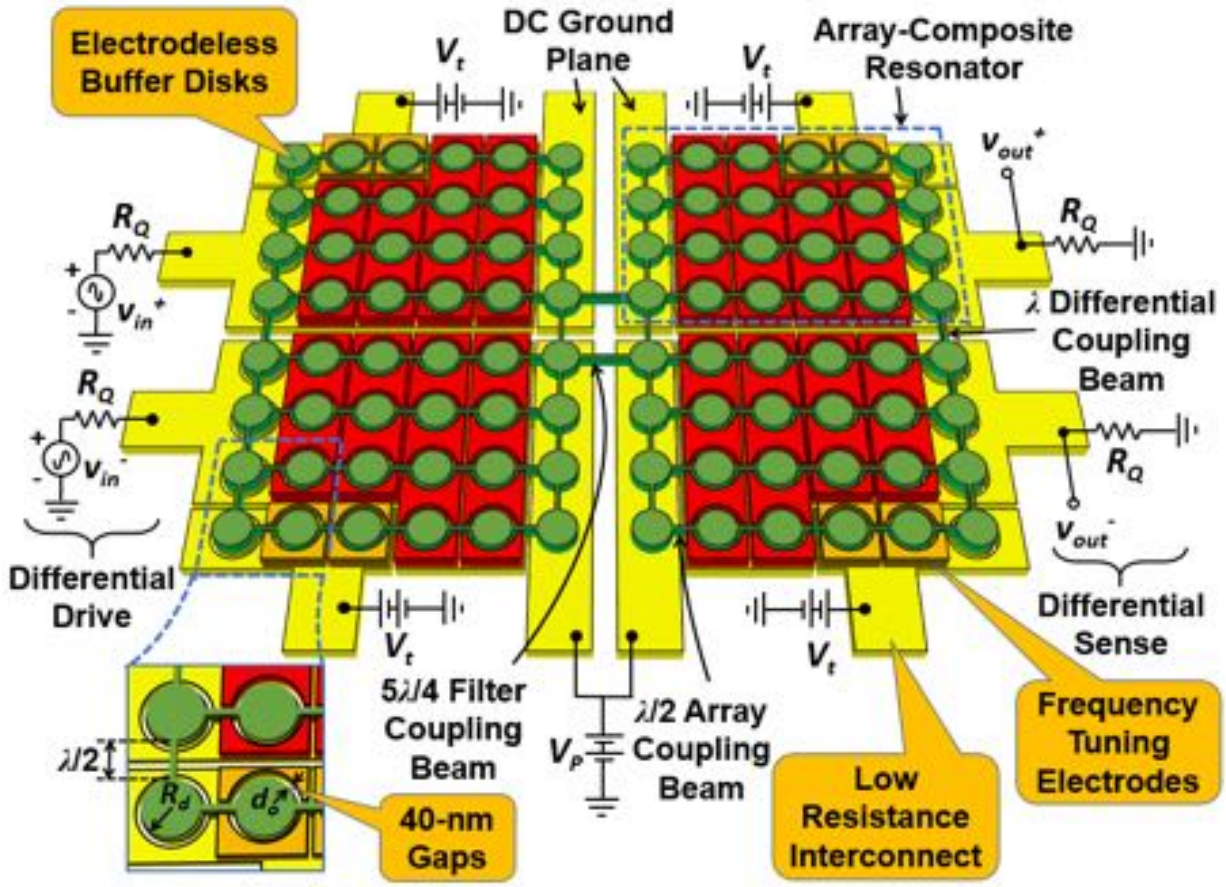


Fig. 2.1: The improved filter design of this work in a preferred bias and excitation configuration used to evaluate filter performance with indicated improvements over to the filter design of [25] [33].

a 223.4-MHz two-resonator filter that employs 206 resonant micromechanical elements to realize a channel-selecting 0.1%-bandwidth while achieving only 2.7dB of in-band insertion loss together with 50dB of out-of-channel stop-band rejection. This amount of rejection is more than 23dB better than that of [25] and comes in tandem with a 20dB shape factor of 2.7 commensurate with its use of two array-composite resonators.

2.2. Filter Design Specifications

Fig. 2.2 presents the transmission response, i.e., S_{21} with reference impedance R_Q, of a third-order bandpass filter (BPF) and identifies important performance metrics [40], including insertion loss, stopband rejection, passband ripple, group delay ripple, and 20dB shape factor. A common way to achieve filter characteristics as in Fig. 2.2 is to link multiple two-pole resonators together by coupling elements of some form, as shown in Fig. 2.2(a) [40], [41]. Fig. 2.2(b) presents one possible implementation that employs series *LCR* resonator tanks coupled by shunt capacitors to mimic the structure of Fig. 2.2(a). Here, the resonators realize bandpass biquad transfer functions that when coupled by the shunt capacitors assemble into a frequency response as shown in Fig. 2.2(c), where three mode peaks ensue, separated by frequency spans governed by coupling strength. Termination of the filter by resistors R_Q then effectively loads the resonators, loading their Q's and widening their responses so that they add constructively in the passband to form the

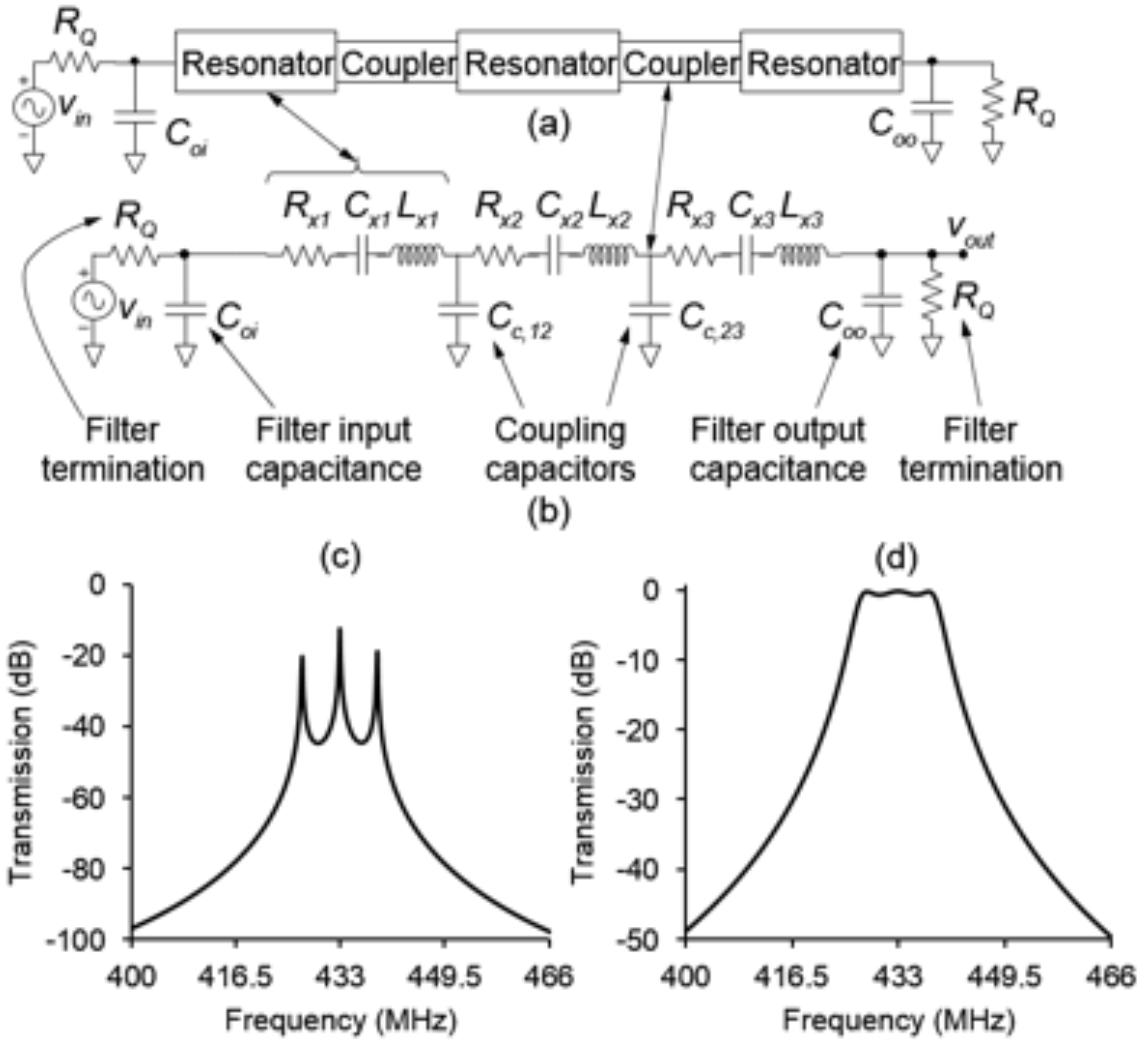


Fig. 2.2: (a) Schematic description of a popular topology for a resonator-based band-pass filter, comprising a chain of discrete resonator tanks linked with coupling elements. (b) One electrical implementation of (a) using series LCR tanks and shunt capacitor couplers. (c) Unterminated (i.e., $R_Q = 0\Omega$) frequency response of the circuit in (b), showing three distinct peaks denoting the resonance modes of the coupled circuit. (d) Terminated filter response after Q-control via termination resistors R_Q.

flat response of Fig. 2.2(d). Phasing of resonator currents also induces subtraction of their responses outside the passband, thereby providing rejection in the stopband.

The desired filter amplitude response, *cf*. Fig. 2.2(a)-(b), minimizes the passband insertion loss, ripple, and the filter 20dB shape factor, the latter defined here by the ratio of the 20dB bandwidth to the 3dB bandwidth; and maximizes the stopband rejection. The group delay characteristic [41] illustrated in Fig. 2.2(c) is a measure of the degree to which the filter phase response deviates from the ideal linear-phase response. Not only must the group delay be below a certain threshold, its ripple must also be small. In many cases, the ripple or variation is most important. As a result, in the plot of Fig. 2.2(c), often only the region of filter bandwidth indicated between the large group delay peaks is actually usable. Note that Chebyshev and Elliptic type filters display a rippled group

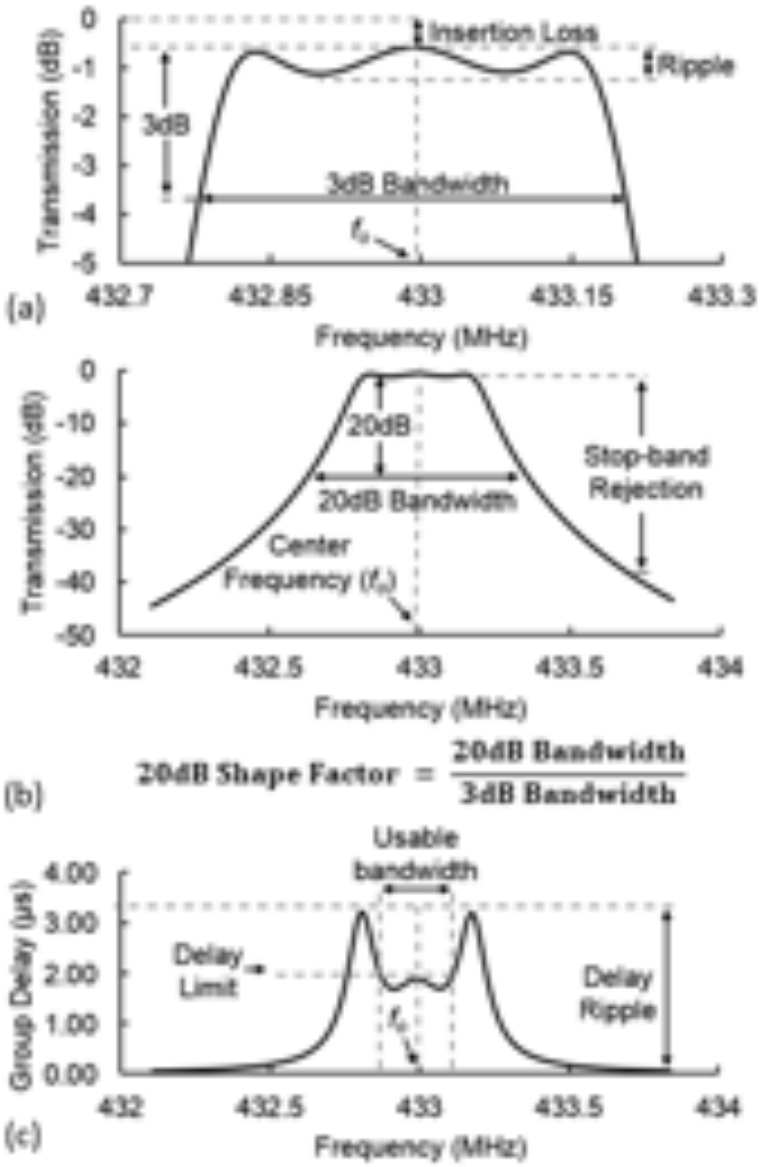


Fig. 2.3: Graphs defining metrics that gauge bandpass filter performance. (a) Zoom-in on the 3dB passband. (b) Wide-span frequency response. (c) Group delay response.

delay over the passband as shown in Fig. 2.2, whereas Bessel type filters achieve maximally flat group delay at the expense of increased shape factor [41].

It should be noted that the smaller the percent bandwidth of the filter, the larger the group delay in the usable bandwidth region. Thus, at first glance, it might seem that the 0.1%-bandwidth RF channel-select filters targeted by this work are not usable in a practical application, since they will have larger group delay than the 3%-bandwidth filters typically used in wireless handsets. Such worries, however, are mostly unfounded, since smaller bandwidth signals can withstand larger group delay variations. In other words, slower bit rates can generally tolerate larger delay variations. The important thing is that the bit period-to-group delay variation ratio be above a certain threshold. The smaller the bandwidth of a signal, the larger its bit period, hence the larger the permissible group delay variation.

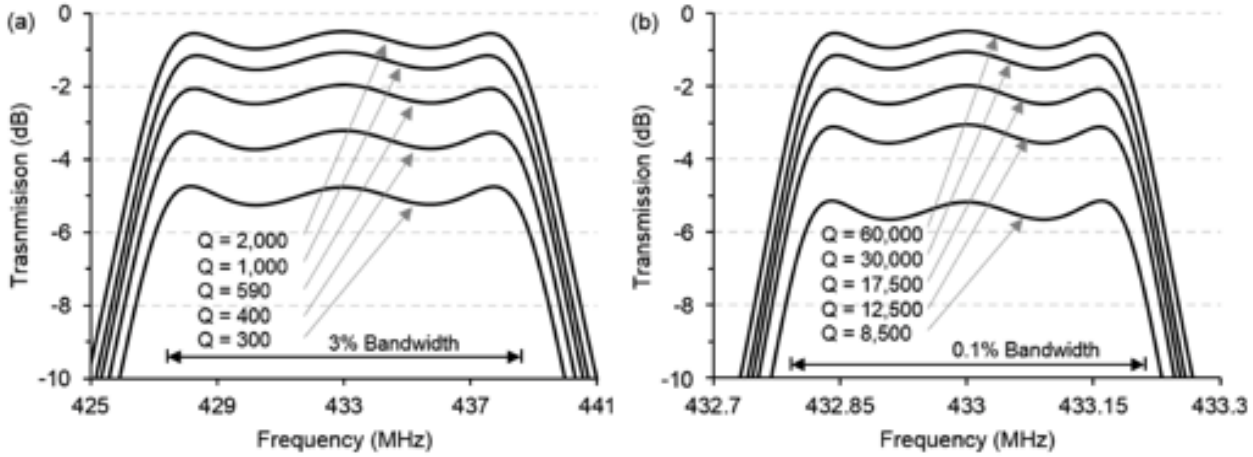


Fig. 2.4: Simulated frequency characteristics for a 433-MHz three-resonator filter with varying constituent resonator Q's, illustrating how resonator Q governs the insertion loss of a filter. (b) For an insertion loss less than 2dB, resonator Q's must be larger than 590Ω for a 3% bandwidth filter. (c) When the filter bandwidth shrinks to 0.1%, even higher resonator Q >17,500, is needed.

Group delay is determined primarily by the filter type, i.e., Chebyshev, Butterworth, etc., and bandwidth. Although filter type also governs passband insertion loss *IL* and stopband rejection, these very important metrics also depend heavily on the performance of the resonators constituting the filter, particularly their quality factor *Q* and their input/output transducer coupling, the latter gauged by the (C_x/C_o) ratios of the end resonators in Fig. 2.2(a). In brief, low filter insertion loss requires sufficient *Q*; while proper termination with minimal passband distortion and large stop-band rejection requires sufficient electromechanical coupling.

2.3. Needed *Q* and Coupling

Whether or not high resonator *Q*, strong transducer coupling (C_x/C_o), or a simultaneous combination of both, are needed, depends largely on the percent bandwidth of the filter to be realized. In particular, the small percent bandwidth filters needed for the aforementioned RF channel-selection application require resonators with large *Q* to avoid excessive insertion loss, but do not require large (C_x/C_o).

A. Needed Quality Factor

The insertion loss of a front-end filter is perhaps its most important performance metric. Indeed, the positioning of this filter directly after the antenna and before the low noise amplifier, *cf.* Fig. 1.7, means that its loss cannot be attenuated by amplifier gain. As a result, the filter insertion loss ends up adding directly to the receiver noise figure, so often has the greatest impact on overall receiver sensitivity.

The insertion loss of any coupled-resonator filter is primarily determined by the ratio of constituent resonator *Q* to overall filter quality factor Q_f [40], or

$$q_o = \frac{Q}{Q_f} \tag{2.1}$$

where Q_f takes the form

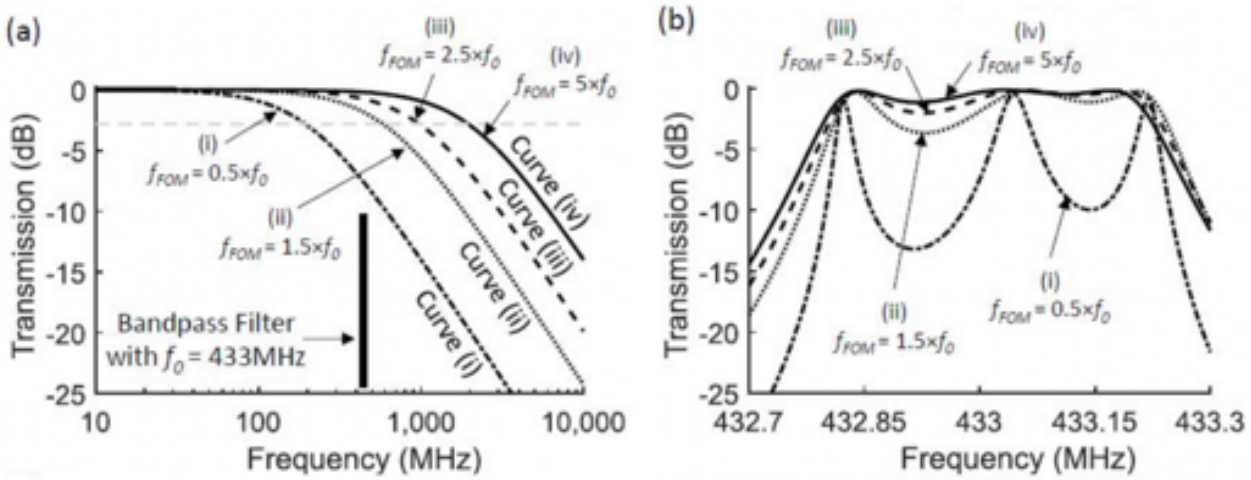


Fig. 2.5: Simulations illustrating the degree to which low-pass filtering by shunt parasitic capacitance impacts passband flatness for a three-resonator filter, cf. Fig. 2.3, operating at center frequency f_o = 433MHz. Here, the filter response curves in (b) correspond to the parasitic low-pass filter cases in (a), for which (i) $f_{FOM} = 0.5\ f_o$. (ii) $f_{FOM} = 1.5\ f_o$. (iii) $f_{FOM} = 2.5\ f_o$. and (iv) $f_{FOM} = 5\ f_o$.

$$Q_f = \frac{f_o}{B} \tag{2.2}$$

where f_o and B are the filter center frequency and 3dB bandwidth, respectively. The filter type and order set the minimum q_o required to achieve a desired insertion loss. Here, filter cookbooks [40] readily provide q_o values for various filter types and insertion losses. For example, the minimum q_o required for less than 2dB insertion loss for a 2nd order Chebyshev filter is 9.7; it increases to 18.6 and 31.1 for third and fourth order filters, respectively [40]. Note that the relation between the quantity set by (2.1) and the filter insertion loss is independent of the resonator technology used to implement the filter.

Equation (2.1) implies that the higher the filter Q_f, i.e., the narrower the fractional bandwidth, the higher the constituent resonator Q needed to maintain low insertion loss. Thus, high resonator Q becomes especially important for the small percent bandwidth RF channel-selecting filter targeted, here—much more so than a conventional 3% band-select filter used in today's wireless handsets.

Fig. 2.4 illustrates the Q dependency by comparing simulated frequency responses of a three-resonator, 0.5dB-ripple, Chebyshev filter operating at 433MHz for band-select and channel-select cases with 3% and 0.1% fractional bandwidths, respectively, with varying constituent resonator Q's. For these simulations, $C_o = 0$ in order to isolate the effect of Q. Here, large resonator Q clearly minimizes insertion loss, regardless of the percent bandwidth. However, to achieve the same insertion loss, a filter with a smaller percent bandwidth requires resonators with larger Q than one with a large percent bandwidth. For example, the filter with 3% 3dB-bandwidth shown in Fig. 2.4(a) requires resonator Q's of 590 to achieve an insertion loss of 2dB. However, when the bandwidth shrinks to the 0.1% required for RF channel-selection (at 433MHz with a 433kHz bandwidth), the required Q for 2dB insertion loss increases to 17,500 as shown in Fig. 2.4(b). The requirement becomes more stringent as frequencies increase or bandwidths decrease. For example, a 30-kHz bandwidth at 433MHz corresponds to a percent bandwidth of 0.007%, for which the Q

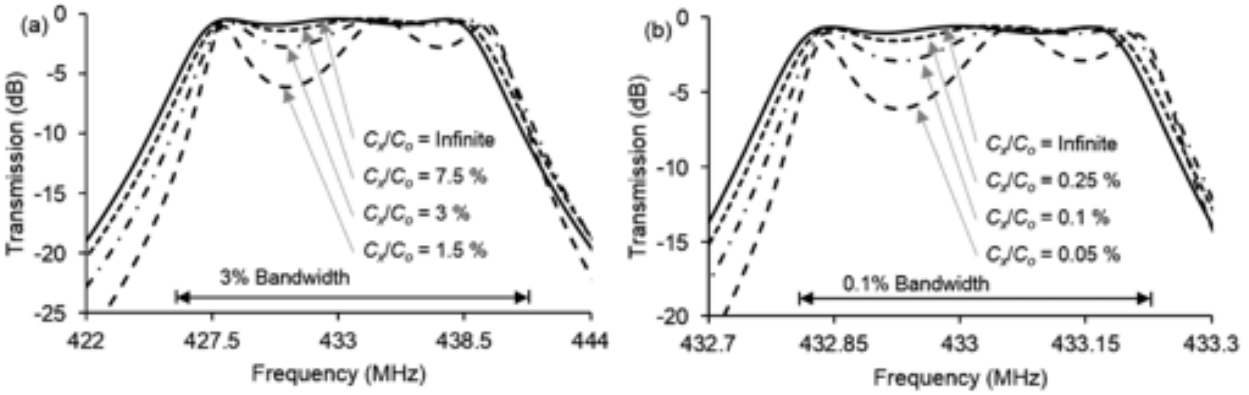


Fig. 2.6: Simulated plots of responses for (a) a 3% bandwidth and (b) a 0.1% bandwidth 3-resonator Chebyshev filter with 0.5dB designed ripple for varying values of transducer (C_x/C_o). Here, the simulations use resonator Q's of 2,500 in (a), and 50,000 in (b).

required for less than 2dB insertion loss rises to 240,000. The need for Q becomes less stringent as the filter order reduces. For example, a second order version of the 0.1%-bandwidth, 433-MHz filter requires resonator Q's of only 9,600 to achieve less than 2dB of insertion loss.

B. Needed Electromechanical Coupling Strength

The electromechanical coupling requirement governs proper impedance termination of a given filter. In particular, the flat passbands shown in Fig. 2.2(d) and Fig. 2.3(b) are achieved via termination resistors R_Q's that load the input and output ports, as shown in Fig. 2.2(a). Here, the R_Q's essentially load the Q's of the filter end resonators, smoothing out the passband ripple in the process.

The 50Ω convention for many discrete parts, e.g., antenna, often stipulates that the R_Q for filters at an RF front-end match to this value. Once past the antenna, however, impedances larger than 50Ω, in the range of 200-400Ω, can offer performance enhancements for active circuits. At the intermediate frequency (IF) of super-heterodyne receivers (still used in military applications), impedances in the kilo-ohm range are common. Low power applications also benefit from impedances this high. In summary, the wide variance in application needs calls for a wide range of desirable R_Q's, and in turn a filter design methodology poised to accommodate.

If the filter had no shunt capacitance C_o at its input and output, then the value of R_Q can be as large or small as needed, with no limit. The presence of C_o, however, places an upper limit on the value of R_Q. In an actual physical realization, load capacitance C_L from leads or other electrically connected structures to the substrate joins C_o to further limit R_Q. In particular, R_Q and (C_o+C_L) combine to form a low pass filter (LPF) that greatly attenuates and distorts the filter response if its cut-off frequency is below the filter center frequency f_o, such as depicted by curve (i) in Fig. 2.5(a), which distorts the filter passband as shown in Fig. 2.5(b). Here, the low pass cut-off frequency is labeled f_{FOM} to emphasize its role as a figure of merit for a given resonator/filter design, where the higher its value, the less passband distortion incurred. Even if f_{FOM} is higher than the filter's center frequency, *cf.* curve (ii) with simulated response in Fig. 2.5(b), phase shift from the LPF can still generate significant passband distortion that may or may not be acceptable, depending upon the application. Thus, it is not enough for f_{FOM} to just be higher than f_o. As a rule of thumb, for the case of a three-resonator Chebyshev BPF, the amount of passband distortion introduced by the

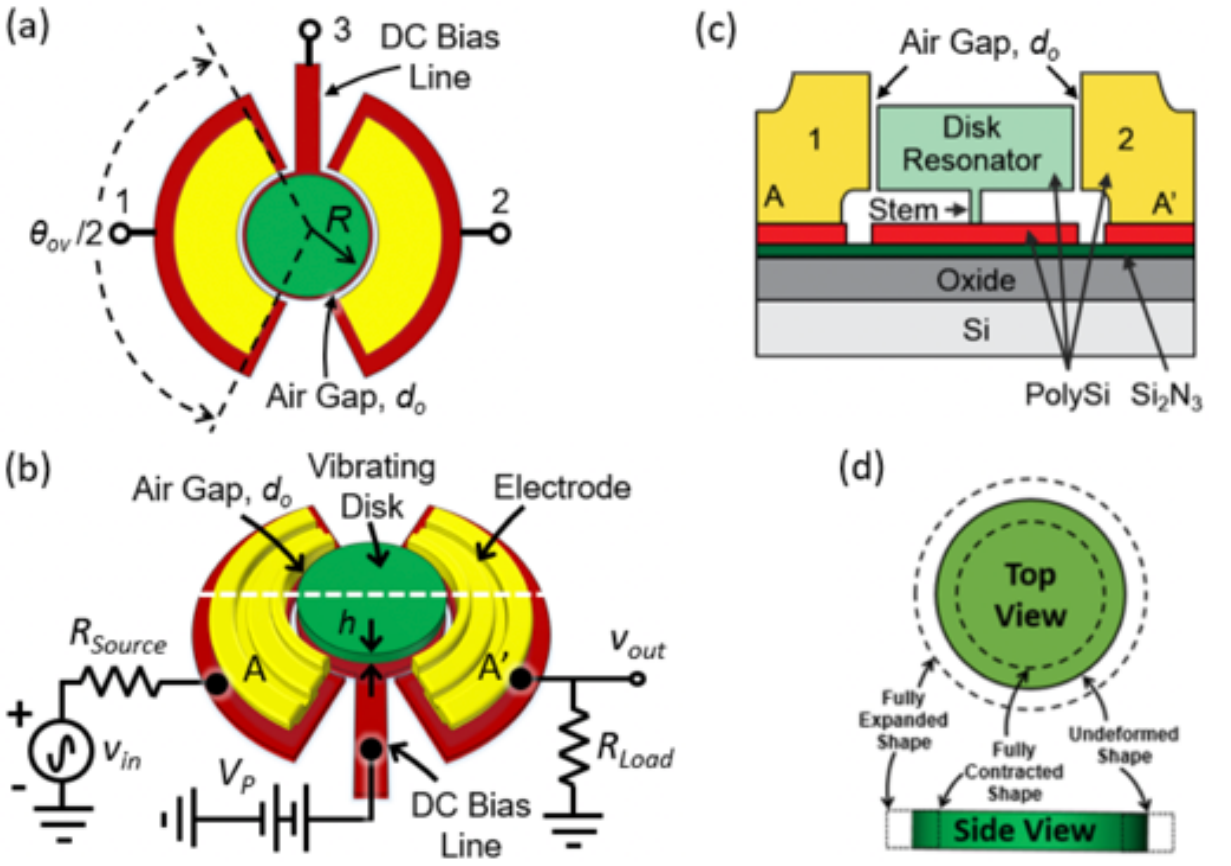


Fig. 2.7: Pictorial summary for a micromechanical disk resonator with two input/output ports and a resonator body port. (a) Layout view. (b) Perspective view in a typical drive and sense configuration. (c) Cross-section view. (d) Radial-contour vibration mode shape.

parasitic LPF is generally acceptable when f_{FOM} is more than 2.5 times the BPF center frequency, as shown by curves (iii) and (iv).

For the case where C_o dominates over C_L, the quantity (C_x/C_o) becomes a very convenient figure of merit for comparison of electromechanically transduced resonators used in a filter. In this case, a rule of thumb to avoid passband distortion upon proper termination stipulates that the transducer coupling at the input and output resonators of a given filter should satisfy

$$\frac{C_x}{C_o} > \gamma P_{BW} \tag{2.3}$$

where P_{BW} is the percent bandwidth of the filter given as B/f_o; and γ is 2.5 for a low insertion loss 3-resonator Chebyshev filter, and ~6 for a 3-resonator linear phase filter.

Fig. 2.6 illustrates the dependence of passband distortion on (C_x/C_o) by plotting simulated responses for (a) a 3% bandwidth and (b) a 0.1% bandwidth 3-resonator Chebyshev filter with 0.5dB designed ripple for varying values of transducer (C_x/C_o). As shown, the passband of the filter in Fig. 2.6(a) remains relatively undistorted until the transducer (C_x/C_o) drops to below 7.5%, at which point an amount of extra ripple equal to the original 0.5dB ripple appears in the passband for a total of 1dB ripple. On the other hand, the passband ripple of the 0.1% bandwidth filter of Fig. 2.6(b) worsens to 1dB when (C_x/C_o) drops to a much smaller 0.25%. Note that the passband

TABLE 2.I: MINIMUM f_{FOM} / f_O AND C_X /C_O RATIOS THAT ADD LESS THAN 0.5dB RIPPLE TO THE DESIGNED NOMINAL RIPPLE VALUE FOR 0.1% BANDWIDTH FILTERS OF DIFFERENT ORDERS

Filter Type	Filter Order											
	2			3			4			5		
	f_{FOM}/f_o	C_x/C_o	γ	f_{FOM}/f_o	C_x/C_o	γ	f_{FOM}/f_o	C_x/C_o	γ	f_{FOM}/f_o	C_x/C_o	γ
Chebyshev (0.5dB Ripple)	2.36	0.12%	1.2	4.70	0.25%	2.5	5.90	0.32%	3.2	6.75	0.37%	3.7
Chebyshev (0.1dB Ripple)	1.82	0.13%	1.3	3.75	0.26%	2.6	4.47	0.33%	3.3	4.98	0.38%	3.8
Legendre	-	-	-	2.95	0.25%	2.5	4.79	0.44%	4.4	5.54	0.58%	5.8

distortions for both filters conform to the guideline of (2.3). Table 2.I presents more information on what values of f_{FOM} and (C_x/C_o) maintain ripple to acceptable values.

From Fig. 2.6, the smaller the percent bandwidth, the smaller the needed (C_x/C_o). In particular, for a 0.1% bandwidth suitable for RF channel-selection, (C_x/C_o) need only be ~0.25%. It is important to note that the needs of a 0.1% RF channel-select filter differ significantly from those of conventional 3% band-select filters used in today's handsets. In particular, conventional 3% filters put a premium on strong coupling, where (C_x/C_o) ~7% is common, and not so much on Q, for which 600 is often acceptable as in Fig. 2.4(a). On the other hand, a 0.1% RF channel-select filter places a high premium on Q, which must often be greater than 10,000, and not so much on (C_x/C_o), for which values of only 0.25% are often acceptable.

2.4. Simplified Description of Vibrating Disk Filter Operation

The mechanical filter of this work is much like the filter of Fig. 2.3(b), except that instead of *LCR* tanks constrained to Q's below 100, it uses mechanically coupled arrays of vibrating micromechanical resonators [35] capable of achieving Q's exceeding 10,000. As shown in Fig. 2.7, each such resonator comprises an electrically conductive disk surrounded by electrodes spaced by small gap spacing d_o from its perimeter, and supported at its center by a stem post, as described in Fig. 2.7(c).

To operate the disk, a dc-bias voltage V_P is applied to its conductive structure (via terminal 3) and ac voltages $v_i = V_i \cos(2\pi ft)$ are applied at one or both of its electrodes. The combinations of DC and AC voltages applied across each affected electrode-to-resonator gap generate forces on the disk structure at frequency f that then actuate the disk into vibration with amplitude governed by its high Q force-to-velocity bandpass biquad transfer function. In particular, when f matches the disk resonance frequency f_o, the disk responds by vibrating with a large (e.g., several nanometers) resonance amplitude in the radial-contour mode shape depicted in Fig. 2.7(d), where the disk expands and contracts radially around its circumference in a motion reminiscent of breathing. Vibration of the disk gives rise to time-varying capacitors at each electrode-to-resonator interface. Since these capacitors have dc-bias voltages across them, they generate currents given by that can then serve as outputs at selected electrodes.

As shown in Fig. 2.1 and detailed later in Section 2.8, the actual filter uses arrays of many disk resonators that combine currents and add stiffnesses to reduce impedance and tailor bandwidth, respectively. Ignoring the arraying for now (for simplicity), Fig. 2.8(a) presents a two-disk version

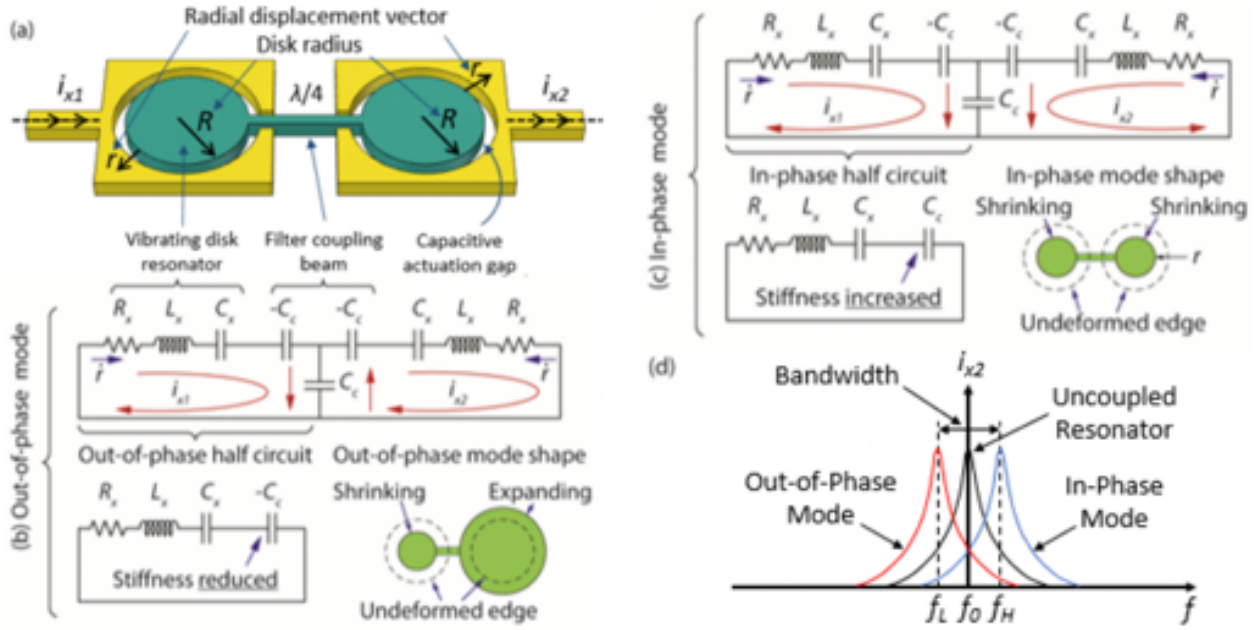


Fig. 2.8: (a) Schematic description of a mechanically coupled two-disk-resonator filter. Equivalent circuit models for (b) the lower frequency out-of-phase and (c) the higher frequency in-phase filter mode shapes. (d) Motional current spectra for the uncoupled vibrating disk and the lower and higher frequency filter modes.

of a micromechanical filter for the purposes of explaining its operation. Here, the two disks coupled by a single quarter-wavelength extensional mode beam are identical in all respects, i.e., they have the same resonance frequency. From a mechanical perspective, mechanical coupling of the two resonators creates a two-degree-of-freedom mechanical system that effectively splits the originally identical resonance frequencies of the disks apart into two mode frequencies, i.e., eigenstates, which now define the passband of the filter response. The two modes can be characterized as *out-of-phase*, where the two resonators vibrate with opposite phase, i.e., one expanding while the other contracts at a given instant, *cf.* Fig. 2.8(b); and *in-phase*, where the disks expand and contract in unison, *cf.* Fig. 2.8(c).

The mechanism by which the quarter-wavelength coupling beam splits frequencies follows from study of the electrical equivalent circuit for this system, shown in Fig. 2.8 [20]. Here, *LCR* tanks model each disk resonator, while a *T*-network of capacitors models the quarter-wavelength coupling beam, essentially treating it as an acoustic transmission line. As shown in [20] [21], the values of the L_x, C_x, and R_x elements in the *LCR*'s are derived directly from the values of mass, stiffness, and damping of the actual resonators.

In the lower frequency *out-of-phase* mode described in Fig. 2.8(b), the coupling spring experiences no strain, since the adjacent disk edges displace in opposite radial directions. In this mode, the coupling spring contributes no stiffness, only mass, to the total system, which lowers the frequency relative to the original resonators. This means the current into the leftmost (input) disk at resonance, given by

$$i_{x1} = \frac{v_i}{R_x} \tag{2.4}$$

is positive; and the current going into the rightmost (output) disk is negative, i.e., current flows out of the disk into the output electrode. Thus, current flows through the device, from input to output. This means the motional currents indicated as i_{x1} and i_{x2} in the electrical equivalent circuit flow in the same clockwise directions around their respective meshes. They thus cancel in the shunt capacitor C_c, which means the voltage drop across the shunt arm of the coupling beam T-network equals zero. This then yields the half circuit for the system shown in (b), where a capacitor of value $-C_c$ adds in series to the motional C_x of the mechanical resonator, lowering the mesh frequency from that of the original resonator down to the lower mode frequency f_L given by

$$f_L = \frac{1}{2\pi}\sqrt{\frac{1}{L_x}\left(\frac{1}{C_x} - \frac{1}{C_c}\right)} \tag{2.5}$$

In the higher frequency *in-phase* mode, where both disks vibrate in unison, the coupling spring now experiences strain. This adds stiffness to the system, raising its frequency over that of the original resonators. From the electrical equivalent circuit perspective, the motional currents i_{x1} and i_{x2} in each resonator tank now flow in opposite directions around their respective meshes, which means they add in the shunt C_c arm of the T-network. Each mesh thus absorbs half of the shunt C_c to yield the overall half circuit shown in Fig. 2.8(c), where now a positive C_c adds in series to the motional capacitance C_x. This raises the mesh frequency to

$$f_H = \frac{1}{2\pi}\sqrt{\frac{1}{L_x}\left(\frac{1}{C_x} + \frac{1}{C_c}\right)} \tag{2.6}$$

Fig. 2.8(d) plots the motional current amplitude spectrum for an uncoupled individual constituent disk resonating at frequency f_o alongside the coupled out-of- and in-phase mode frequencies at f_o-B_{sep}/2 and f_o+B_{sep}/2, respectively, where $B_{sep} = f_H - f_L$ is the frequency span that separates the modes. The out-of-phase and in-phase resonance transfer functions illustrated in Fig. 2.8(d) correspond to the orthogonal eigenvectors of the coupled two-resonator system shown in Fig. 2.8(a).

The sum of these transfer functions generates the overall filter transfer function, as illustrated in Fig. 2.9(c). Note that the relative phase between these modes plays a crucial role in shaping the overall filter response. In particular, the out-of-phase and in-phase modes have the same phase between the mode peaks, so add constructively within the filter passband to form a flatter response in this region. Outside the peaks, their phases differ by 180°, which means they subtract outside the passband, yielding a steeper roll-off to the stopband and a higher overall stopband rejection.

However, as shown in Fig. 2.9(b), addition in the passband will not yield a flat passband if the Q's of the constituent resonators are too high. Indeed, to permit a flat passband, the signal power of each mode spectrum at the frequency directly between the peaks must be approximately equal to half that at the peaks themselves. This is where the termination impedances shown in Fig. 2.3 and again in Fig. 2.9(a) become important. These termination resistors R_Q load the Q's of the resonators, broadening their peaks and effectively raising their power levels at frequencies away from resonance. To attain half power between the peaks, the resonator Q's must be reduced to approximately that of the filter, or

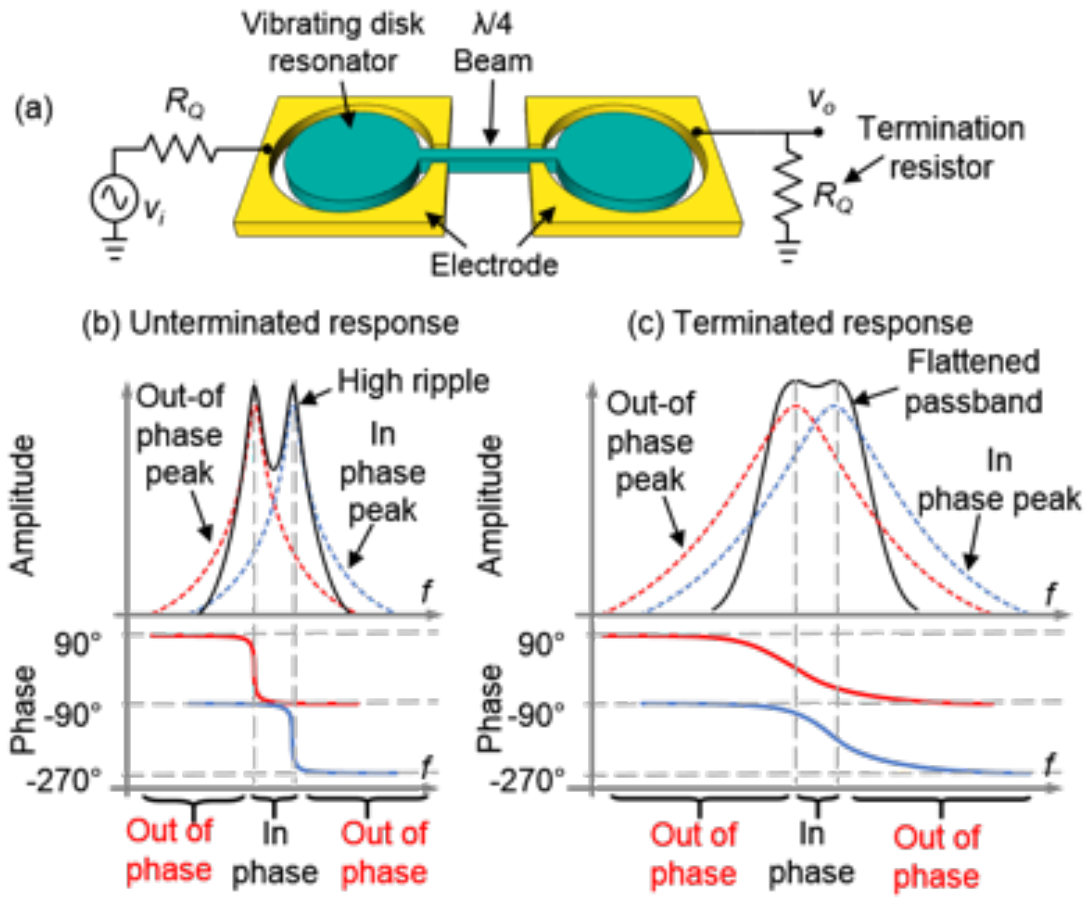


Fig. 2.9: (a) Mechanically coupled two-resonator filter with termination resistors R_Q added for Q-control. (b) Illustration showing addition of in-phase and out-of-phase resonator frequency responses to create the unterminated filter response. (c) Illustration showing the mechanism for filter response formation after Q-control with appropriate termination resistors R_Q. Note that the plots are not to scale, as the unterminated response would normally be several dB below the terminated response, as depicted in Fig. 2.3 and described in [20].

$$q_n Q_f = Q\left(\frac{R_x}{R_x + R_Q}\right) \rightarrow R_Q = R_x\left(\frac{Q}{q_n Q_f} - 1\right) \tag{2.7}$$

where q_n is a modification factor that depends upon the filter order and type, i.e. Chebyshev, Butterworth, and that can be found in filter cookbooks [40]. Upon inclusion of termination resistors R_Q, the flattened passband response in Fig. 2.9(c) ensues.

From (2.7), note that for a properly designed filter, R_Q tracks R_x. In other words, a filter designed for a large R_Q uses resonators with large R_x; and if designed for a small R_Q, the resonators have small R_x. Because of this, the insertion loss of a properly designed filter using (2.7) is ultimately independent of R_Q. To elaborate using equations, the insertion loss for this two-resonator filter takes the form

$$IL = \frac{R_Q + R_x}{R_Q} = \frac{Q}{Q - q_n Q_f} \tag{2.8}$$

where tracking of R_Q and R_x effectively cancels them, leaving a rightmost expression that depends only on Q parameters. Thus, insertion loss depends primarily on the resonator Q and the filter Q_f.

From Fig. 2.9(c), it is clear that with quarter-wavelength coupling the center frequency of the Fig. 2.9 filter equals the (common) frequency of its constituent resonators; and its 3dB bandwidth is a bit more than the total separation B_{sep} afforded by the coupler strength, captured by the value of C_c. Using (2.5) and (2.6), the mode peak separation takes the form

$$B_{sep} = \frac{C_x}{C_c} f_o = \frac{k_c}{k_m} f_o \tag{2.9}$$

where the last form recognizes that C_x and C_c are proportional to the inverse dynamic stiffnesses k_m and k_c of the resonators and coupler, respectively [20]. Since filter bandwidth is generally the 3dB bandwidth, a modification factor k_{ij} applied to (2.9) yields the more common form

$$B = \frac{k_c}{k_m k_{ij}} f_o \tag{2.10}$$

where B is the 3dB bandwidth, and k_{ij} refers to the modification factor needed for the coupler between the i^{th} and j^{th} resonators in a multi-resonator filter. k_{ij} values are widely tabulated in filter cookbooks [40] for a variety of filter types and orders.

It is worth mentioning here that for this electrically driven and sensed filter the R_Q's serve as source and load impedances. While the R_Q's do effectively load the Q's of the resonators, the resonators themselves must have high Q to start with in order to have motional resistances R_x's sufficiently smaller than R_Q to preserve low insertion loss. In other words, one cannot start with low Q resonators and expect low insertion loss; the resonator Q's must be high to start with.

2.5. Actual Filter Structure and Operation

Although the actual demonstrated filter essentially operates as described in the previous section, its overall structure is substantially more complicated, all in the interest of maximizing performance. Again, Fig. 2.1 presents the perspective-view schematic of the entire mechanical filter circuit in a preferred differential input/output configuration, showing all applied voltages and termination impedances, and pointing out key differences with the previous one of [25] that allow the present design to achieve much improved performance. As shown, the filter comprises 96 disks mechanically coupled by 110 beams. Many of the disks are surrounded by electrodes spaced only 39nm from their edge sidewalls to serve as either input/output or mechanisms for frequency tuning. Array composite resonators are clearly discernable, and their use represents a second level of hierarchy in an overall hierarchical design reminiscent of those used in complex VLSI transistor circuits, but here used to achieve a complex MSI mechanical filter circuit. Fig. 2.10 illustrates the four main levels of hierarchy that include:

1st Level: Radial-Contour Mode Disk Resonator

The polysilicon contour mode disk resonator depicted in Fig. 2.7 and described in Section 2.7 comprises the unit element and 1st level of hierarchy in the mechanical circuit. In Fig. 2.1, all disks are h=3μm-thick with R=12.1μm radii, so share a common radial-contour mode resonance frequency that sets the center frequency of the overall filter.

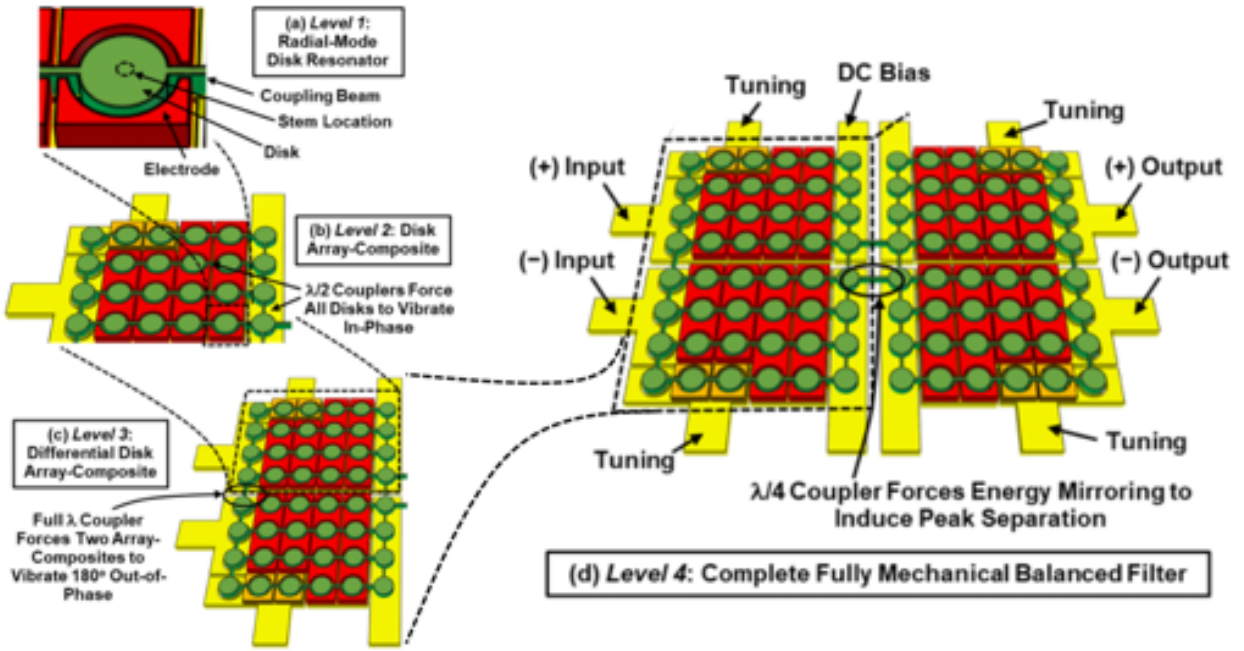


Fig. 2.10: Pictorial breakdown of the four levels of hierarchy in the disk-array micromechanical filter design. (a) Level 1: Radial-mode capacitive-gap transduced disk resonator. (b) Level 2: Half-wavelength beam-coupled array-composite of disks making up an "array quadrant". (c) Level 3: Full-wavelength beam-coupled pair of quadrant array-composites for which coupling forces the array-composites to vibrate 180^o out-of-phase. (d) Level 4: Quarter-wavelength beam-coupled differential array-composites that finally make up the total filter.

2nd Level: Disk Array-Composite

To reduce termination impedance and raise stiffness to facilitate small bandwidth, four array-composites of half-wavelength coupled disks make up the 2nd level of hierarchy. Each combines and raises currents, thereby reducing motional resistance, hence, filter termination impedance.

3rd Level: Differential Array-Composite

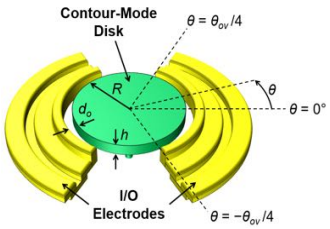
To enable differential I/O, a 3rd level of hierarchy couples pairs of array-composites via full-wavelength beams. This forces them to vibrate 180° out-of-phase, thereby enabling differential mode balanced operation that cancels feedthrough to enable large stopband rejection.

4th Level: Coupled Resonator Filter

A 4th level of hierarchy couples the differential blocks via quarter-wavelength beams that split their resonances, generating the desired passband and promoting signal subtraction in the stopband that increases rejection.

Operation of the filter requires the application of a DC voltage V_P to the conductive suspended structure to amplify forces and electrical outputs; and differential electrical inputs through termination impedances (governed by design) to the left-hand terminals. These electrical signals convert to mechanical (e.g., velocity) signals that process mechanically through the frequency response of the structure and then convert back to electrical signals at the outputs.

TABLE 2.II: RADIAL-CONTOUR MODE DESIGN EQUATIONS AND PROCEDURE SUMMARY

Objective/Procedure	Parameter	Relevant Design Equations for a Given Parameter	Eq.
	Resonance Frequency	$f_{nom} = \frac{K_{(R,m),mat}}{2R}\sqrt{\frac{E}{\rho}}$ where $K_{(R,m),mat} = \frac{\zeta_{(R,m),mat}}{\pi\sqrt{2(1+\sigma)}}$ where R denotes the disk radius, E and σ are the Young's modulus and Poisson ratio, and m = mode number.	(2.11)
	Solve For ζ	$\frac{\zeta}{\xi}\frac{J_0(\zeta/\xi)}{J_1(\zeta/\xi)} = 1-\sigma, \quad \zeta = 2\pi f_{nom} R\sqrt{\frac{2\rho(1+\sigma)}{E}}, \quad \xi = \sqrt{\frac{2}{1-\sigma}}$	(2.12)
Given: f_{nom}, V_P, R_x Find: radius R, electrode-to-resonator gap spacing d_o 1. Choose E, ρ, and σ by choice of structural material. 2. Choose thickness h. 3. Use (2.11) to find the R needed to achieve f_{nom}. Use (2.12) to get ζ in the process. 4. Use (2.13) to find the d_o needed to achieve R_x. 5. (2.14)-(2.16) yield all needed values in the transformer-based negative C_o equivalent circuit.	Motional Resistance, Capacitance, and Inductance	$R_x = \frac{r_x}{\eta_e^2}, \quad C_x = c_x\eta_e^2, \quad L_x = \frac{l_x}{\eta_e^2}$	(2.13)
	Core Equiv. Circuit Elements	$l_x = m_m(R) = \frac{2\pi\rho h\int_0^R rJ_1^2(\phi r)dr}{J_1^2(\phi r)}, \ \phi = \omega_0\sqrt{\frac{\rho}{E}(1-\sigma^2)}$ $c_x = \frac{1}{k_m(R)} = \frac{1}{\omega_{nom}^2 m_m}, \ r_x = b_m(R) = \frac{\sqrt{k_m m_m}}{Q} = \frac{\omega_{nom} m_m}{Q}$	(2.14)
	Static Overlap Capacitor	$C_o = \frac{\varepsilon_o\theta_{ov}Rh}{d_o}$	(2.15)
	Electromechanical Turns Ratio	$\eta_e = V_P\frac{C_o}{d_o}$	(2.16)

2.6. Detailed Filter Design

Given the design hierarchy from the previous section, a sensible design procedure now emerges:

1) Design the fundamental micromechanical radial-contour mode disk building block to resonate at the filter center frequency f_o with the needed Q and coupling strength (C_x/C_o) with given values of dc-bias V_P and electrode-to-resonator gap spacing d_o.
2) Assemble disks into array-composites to achieve a specific termination resistance R_Q, linearity spec, and bandwidth. Here, the array size N_{tot} is key to maintaining practically realizable filter coupling beam dimensions for the chosen filter bandwidth B.
3) Design quarter-wavelength filter coupling beams that yield the desired filter passband.
4) Convert the design from single-ended to differential.

TABLE 2.III: FILTER DESIGN PROCEDURE WITH EQUATIONS

Given the following parameters:

Design Goals: f_o, B, R_Q

Filter Constants: q_n, k_{ij}, γ

Resonator & Material Constants: Q, E, ρ, κ_{mat}, θ_{ov}, χ, σ_{single}*

Dimension Constraints: $w_{c,min}$, d_o, h

Voltage Constraints: V_{max}‡

Find: R, N_{tot}, N_{io}, N_t, V_P, λ, w_c.

1. Find the disk radius R using (2.17).
2. Solve (2.18) for V_p to achieve sufficient C_x/C_o with corresponding γ value from Table 2.I.
3. Pick the number of rows N_{row} in a quadrant.
4. Use (2.19) to determine the number of I/O electrodes needed for R_Q. Assume $N_t = 0$ for now.
5. Use (2.20) to determine the number of columns N_{col}.
6. If σ_{single} is known, use (2.21) and (2.22) to determine the minimum number of tuning electrodes for the desired yield. If needed, increment V_P or N_{col}.
7. Determine R_Q using (2.23). Adjust V_P or N_{col} to match the spec, if needed.
8. Use (2.24) to confirm correct center frequency after arraying.
9. Determine the acoustic wavelength λ by (2.25) for the $\lambda/4$ filter, $\lambda/2$ array-composite, and λ differential couplers.
10. Determine the coupling beam dimension w_c that meets the desired filter bandwidth B specification using (2.26).
11. Assemble the fully balanced structure of Fig. 2.1.
12. Use (2.27)-(2.30) to generate the equivalent circuit of Fig. 2.24, then simulate to confirm the correct filter response.

Mechanical Design Variables	Disk Radius	$R = \frac{K_{mat}}{2f_o}\sqrt{\frac{E}{\rho}}$	(2.17)
	Approx. Required Bias Voltage for Sufficient Array C_x/C_o	$V_P^2 \geq 1.5\gamma\frac{P_{BW}k_m d_o^3}{\varepsilon_o A_o} = 1.5\gamma d_o^3\frac{2B\pi^3\chi K_{mat}\sqrt{E\rho}}{\varepsilon_o\theta_{ov}}$	(2.18)
	Total No. of Disks to Attain Spec'ed Termination Impedance R_Q	$N_{io} = \frac{\Gamma}{2} + \sqrt{\left(\frac{\Gamma}{2}\right)^2 + \Gamma N_b}$ where $\Gamma = \frac{2\pi B m_m}{q_n\eta_e^2 R_Q} = \frac{\pi\chi\rho\omega_o}{Q_f q_n h\varepsilon_o^2\theta_{ov}^2}\frac{d_o^4}{R_Q V_P^2}$, $N_b = 2N_{row}$	(2.19)
	No. of Columns Needed	$N_{col} > \frac{N_{io}+N_b}{N_{row}}$	(2.20)
	No. of Tuning Electrodes	$N_t = N_{col}N_{row} - N_{io} - N_b$	(2.21)
	No. of Tuning Electrodes Needed for % Perfect-Tuned Yield⁘	$N_t \geq i\sigma_{single}\frac{\sqrt{2N_{tot}}k_m d_o^3}{\varepsilon_o A_o V_T(2V_P - V_T)} = i\sigma_{single}\frac{\sqrt{2N_{tot}}\pi^3 K_{mat}^2\chi E d_o^3}{\varepsilon_o\theta_{ov}RV_T(2V_P - V_T)}$ where $i = 1\,(68.3\%), 2\,(95.4\%), 3\,(99.7\%), \ldots$	(2.22)
	Termination Impedance R_Q	$R_Q = \left(\frac{Q}{q_n Q_f} - 1\right)\frac{N_{tot}}{N_{io}^2}\frac{r_x}{\eta_e^2} = \left(\frac{Q}{q_n Q_f} - 1\right)\frac{\omega_o}{Q}\frac{N_{tot}}{N_{io}^2}\frac{d_o^4}{V_P^2}\frac{\pi\chi\rho}{h\varepsilon_o^2\theta_{ov}^2}$	(2.23)
	Array Quadrant Center Frequency	$f_o = \frac{1}{2\pi}\sqrt{\frac{k_m}{m_m}}\sqrt{1 - \frac{\varepsilon_o A_o}{d_o^3 k_m}\left\{\frac{N_{io}}{N_{tot}}V_P^2 - \frac{N_t}{N_{tot}}(V_P - V_T)^2\right\}}$	(2.24)
	Wavelength for Coupling Beam Designs	$\lambda = \frac{1}{f_o}\sqrt{\frac{E}{\rho}}$	(2.25)
	$\lambda/4$ Coupling Beam Width to Attain Filter Bandwidth B	$w_c = N_{tot}\frac{Bm_m}{h}\frac{2\pi\xi k_{ij}}{\sqrt{E\rho}} = \frac{\xi N_{tot}\pi^2 K_{mat}^2\chi k_{ij}P_{BW}}{2f_o}\sqrt{\frac{E}{\rho}}$ where $\xi = 1, 3, 5, \ldots$	(2.26)
Filter Electrical Equivalent Circuit Elements	$\lambda/4$ Coupling Beam Lumped Element	$c_c = \frac{2(\xi\lambda/4)}{\pi E h w_c} = \frac{\xi}{h w_c\omega_o\sqrt{E\rho}}$ where $\xi = 1, 3, 5, \ldots$	(2.27)
	Array-Composite Core-LCR Elements	$r_{xA} = N_{tot}\frac{m_m\omega_o}{Q} = N_{tot}\frac{\chi h K_{mat}\sqrt{E\rho}\pi^2 R}{Q}$ $l_{xA} = N_{tot}m_m = N_{tot}\chi\rho\pi R^2 h$ $c_{xA} = \frac{1}{N_{tot}m_m\omega_o^2} = \frac{1}{N_{tot}\pi^3 K_{mat}^2\chi E h}$	(2.28)
	I/O Electrode Elements	$\eta_{eA} = N_{io}V_P\frac{\varepsilon_o\theta_{ov}Rh}{d_o^2}$ $C_{oA} = N_{io}\frac{\varepsilon_o\theta_{ov}Rh}{d_o}$	(2.29)
	Tuning Electrode Elements	$\eta_{tA} = N_t(V_P - V_T)\frac{\varepsilon_o\theta_{ov}Rh}{d_o^2}$ $C_{tA} = N_t\frac{\varepsilon_o\theta_{ov}Rh}{d_o}$	(2.30)

* σ_{single} is the single disk resonator's frequency standard deviation.
‡ V_{max} is the maximum voltage allowed in the technology.
⁘ Assumes $V_T = V_P$ for maximum tuning.

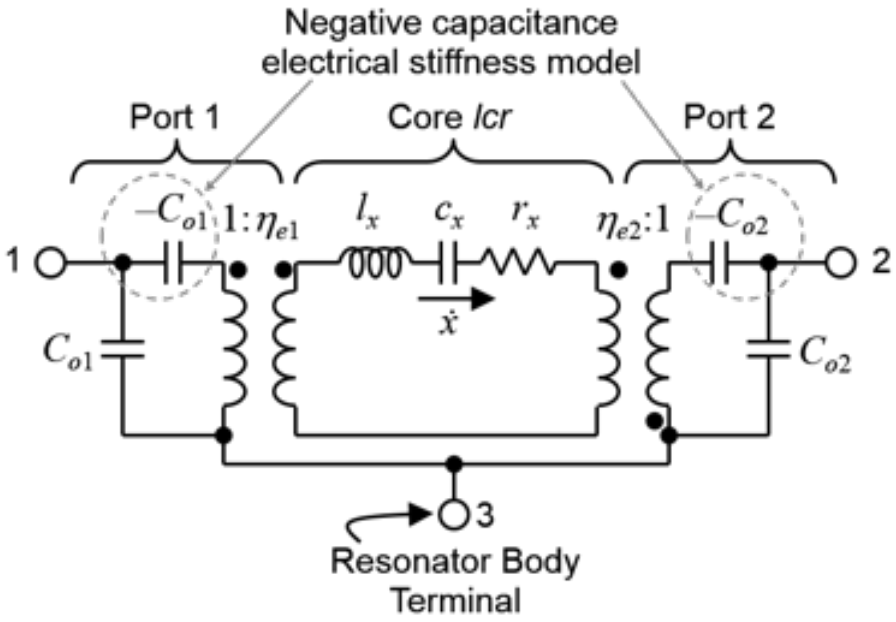


Fig. 2.11: Negative capacitance small-signal AC equivalent circuit for a two-port capacitive gap transduced micromechanical resonator, such as that of Fig. 2.7, when operating in the radial-contour mode

5) Simulate the filter electrical equivalent circuit and verify satisfactory operation in the electrical domain.

Table 2.II and Table 2.III capture this design procedure and provide a preview of the relevant governing equations. Sections 2.7 - 2.13 now expand on the detailed steps and formulations needed to execute each stage of the design process.

2.7. Radial-Contour Mode Disk Design

The radial-contour mode disk used in this work offers an excellent combination of high Q, reasonable electromechanical coupling (when small gaps are used), and perhaps equally important, mechanical circuit design flexibility. The last of these derives from the fact that a lateral mode disk like that summarized in Fig. 2.7 is isotropic around its circumference, i.e., it ideally presents the same loading or response at any point on its outside edges. This means that radial beams can attach and couple to a given disk at any angle and still elicit the same response. Such coupling flexibility is quite welcome when complex coupling geometries are required, like the arrays of Fig. 2.1.

The literature is abundant with capacitive-gap-transduced radial-contour mode disk resonators capable of Q's greater than 29,300 at 153.9MHz in polysilicon structural material [42], and greater than 55,000 at 497.6MHz in polydiamond [43]. Thus, from the perspective of achievable frequency and Q, the chosen disk resonator design seems adequate for RF channel-selection, at least for the example shown in Fig. 2.4.

From the perspective of electromechanical transducer coupling strength, however, the disk resonators so far reported in the literature have been lacking. For example, the 153.9-MHz polysilicon disk of [42] posted a (C_x/C_o) of only 0.00048%, while a higher frequency 497.6-MHz diamond one was even poorer, on the order of only 0.00005% [43]. Section 2.3-B mentioned that (C_x/C_o)

need not be large for RF channel-selection, but these values are abysmal. If disk resonators are to be useful, their design must allow several orders of magnitude improvement in these numbers.

Fortunately, the literature provides comprehensive and experimentally confirmed models for radial-contour mode disk resonators that allow accurate prediction of design-driven performance improvements. Fig. 2.11 and Table 2.II summarize the equivalent circuit and expressions for elements from [44], respectively, which details the most recent radial-contour mode disk model using a negative capacitance concept. Using formulations from [44], the electromechanical coupling factor for a radial-contour mode disk takes the form

$$\frac{C_x}{C_o} = \frac{V_P^2}{d_o^3} \frac{\varepsilon_o R \theta_{ov}}{\pi^3 \chi K_{mat}^2 E} \tag{2.31}$$

where V_P is the dc-bias applied between the disk resonator and the surrounding electrodes, d_o is the electrode-to-resonator gap spacing, ε_o is the permittivity of vacuum, R is the disk radius, θ_{ov} is the angular overlap between the electrode and the disk in radians, and E is the Young's modulus of the resonator structural material. Fig. 2.7 schematically illustrates these design variables. χ is a constant that relates the static mass M_{tot} of the disk to its dynamic mass m_m as

$$m_m = \chi M_{tot} = \chi \rho \pi R^2 h \tag{2.32}$$

where ρ is the resonator structural material density. χ can be derived by consideration of the total kinetic energy of the resonant disk structure and its radial velocity at the disk edges and equals χ=0.763, 0.967, 0.987 for a disk operating in its first, second, and third radial-contour modes, respectively [44].

Since (2.32) depends on disk radius R, it is a function of disk resonance frequency f_{nom} that derives from the simultaneous solution of [44]

$$\frac{\zeta}{\xi} \frac{J_0(\zeta/\xi)}{J_1(\zeta/\xi)} = 1 - \sigma, \;\; \xi = \sqrt{\frac{2}{1-\sigma}} \tag{2.33}$$

and

$$\zeta = 2\pi f_{nom} R \sqrt{\frac{\rho(2+2\sigma)}{E}} \tag{2.34}$$

where σ is the Poisson ratio of the structural material, and J_0 and J_1 are Bessel functions of the first kind of order zero and one, respectively. Although the solution of (2.33)-(2.34) as described provides an accurate value for the contour-mode resonance frequency, it does not readily impart design insight. To provide better insight to variable dependencies, rearrangement and simplification of (2.33)-(2.34) yields the closed form

$$f_{nom} = \frac{\alpha K_{mat}}{2R} \sqrt{\frac{E}{\rho}} \tag{2.35}$$

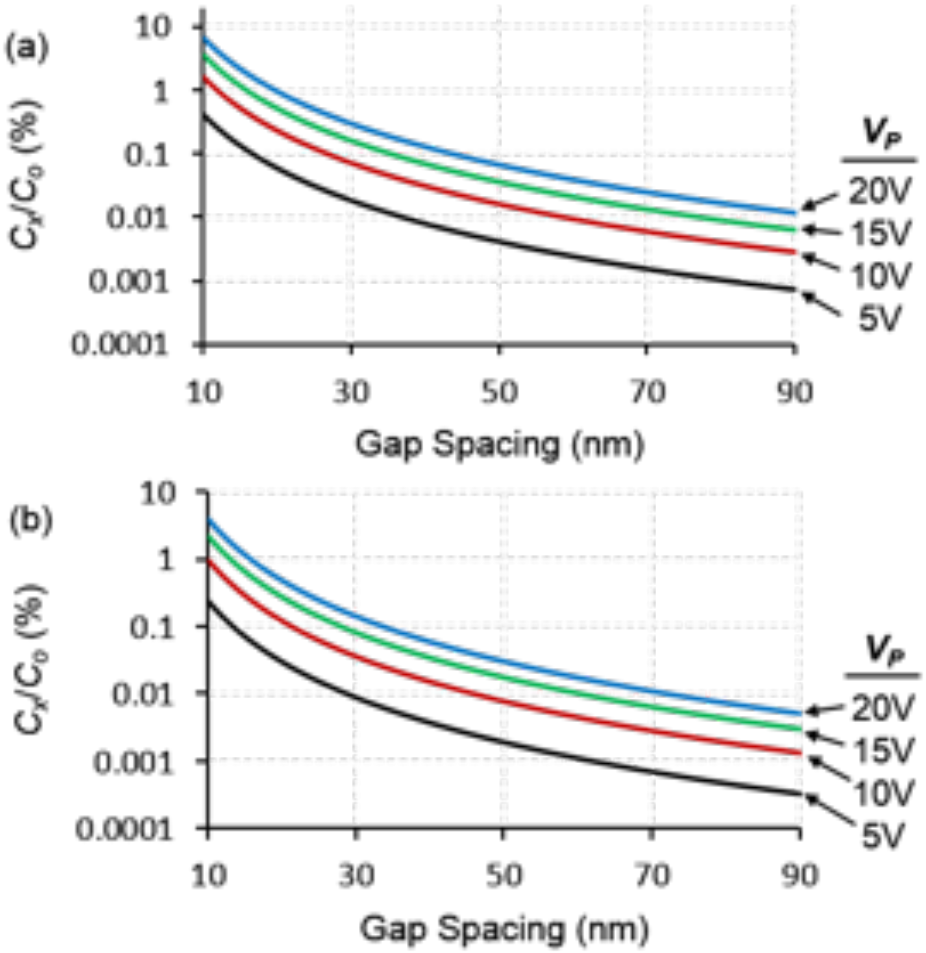


Fig. 2.12: Simulated plot of C_x/C_o for a polysilicon contour mode disk resonator with fully surrounding electrodes plotted as a function of the electrode-to-resonator gap spacing for four different bias voltages operating at (a) 433MHz, and (b) 1.2GHz.

where α is a mode-dependent scaling factor that accounts for higher order modes, i.e., 1, 2.64, and 4.61 for the 1st, 2nd, and 3rd radial-contour mode, respectively, and K_{mat} is a dimensionless frequency parameter that depends upon the structural material and is independent of radius [44]. For polysilicon K_{mat}=0.654. Solving for R and then inserting into (2.31) yields the expression for electromechanical coupling as a function of resonance frequency

$$\frac{C_x}{C_o} = \frac{V_P^2}{d_o^3} \frac{\alpha}{f_{nom}} \frac{\varepsilon_o \theta_{ov}}{2\pi^3 \chi K_{mat} \sqrt{E\rho}} \tag{2.36}$$

From (2.36), a reduction in electrode-to-resonator gap spacing d_o is clearly the most effective approach to raising (C_x/C_o), given the third power dependence. In fact, reducing d_o from the 80nm used for the 163-MHz disk of [25] to 40nm would increase (C_x/C_o) from 0.022% to 0.177% for a 14V dc-bias voltage—an 8× increase that makes possible a 0.177%-bandwidth two-resonator filter at this frequency. At higher frequency, the dependence on radius shown in (2.31) reduces the efficacy of gap scaling. In particular, for the fundamental mode 1.156-GHz disk of [35] the same 40nm gap and 14V yield a (C_x/C_o) of only 0.024%. An even smaller gap remedies this, where use

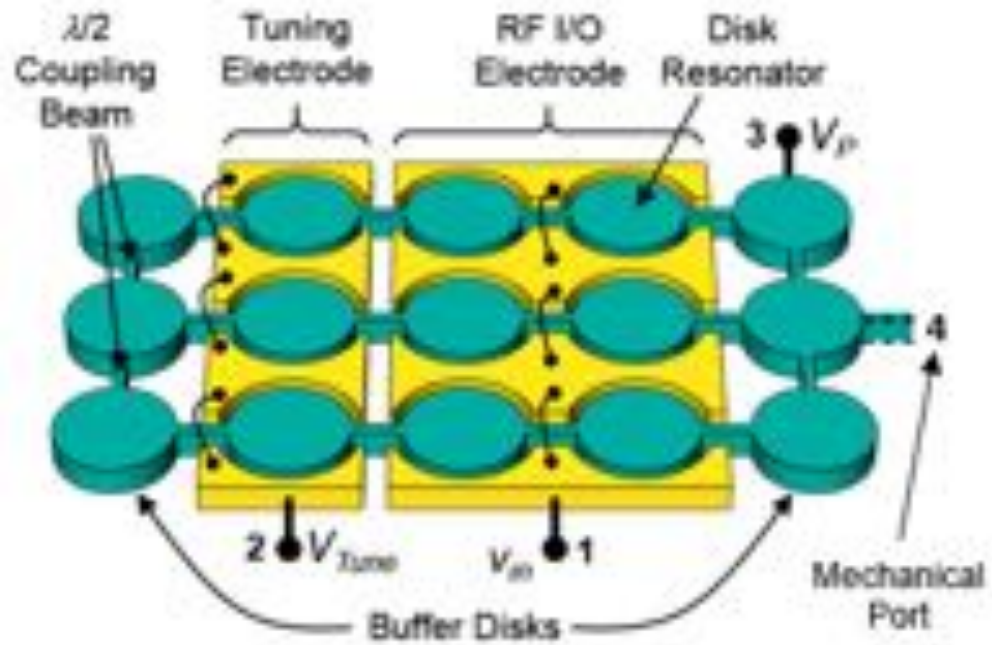


Fig. 2.13: Illustration of a λ/2 coupled array-composite resonator with dedicated tuning electrodes and outer buffer disk-resonators for defensive design against in-plane structural film stress.

of the fundamental mode together with 20.6nm and 14V recapture the (C_x/C_o) of 0.177%. This gap sounds small and was indeed once considered impractical, but no longer in light of recent 13-nm gap polysilicon wine-glass disk resonators, which at 60-MHz with 5.5V dc-bias posted a (C_x/C_o) of 1.62% with a Q of 29,640 [45]. Gaps like this should extend the frequency range of disk-array filters well beyond the 223.4 MHz of this work

Fig. 2.12 plots (C_x/C_o) versus gap spacings below 100nm for radial-contour mode disks at various frequencies and dc-bias voltages. The chosen V_P voltages are all well below the pull-in voltage for the devices determined both via the classic electrical stiffness pull-in expression and by FEM simulation. Still, other factors might also limit the permissible V_P, e.g., weak stem anchor or electrical breakdown, so the higher voltage plots of Fig. 2.12 do require validation. Assuming for now that they hold, the plots predict that capacitive-gap transducers with gaps approaching 10nm have potential to achieve (C_x/C_o) ~10% at usable RF frequencies. Electromechanical coupling this high is actually not unheard of for capacitive-gap transducers. For example, the clamped-clamped beam resonators used in the HF filter of [21] posted (C_x/C_o)'s on the order of 14.8% at V_P=35V.

It should be mentioned that adequate (C_x/C_o) does not guarantee an impedance match with the stages before and after the eventual filter using a given disk resonator. Unfortunately, the tiny size of a single disk relegates it to high impedance. Taking the example of a two-resonator 0.5dB-ripple Chebyshev filter with q_n=1.9497 [40] and Q/Q_f=9.5 for less than 2dB insertion loss, (2.7) predicts that a match to a 50Ω R_Q termination requires a motional resistance R_x of 12.9Ω; and a match to 200Ω requires that R_x be 51.6Ω. Using (2.13) in Table 2.II with a gap of d_o = 20nm, the 163-MHz disk reported in [25] with Q = 10,500, h = 3μm, and V_P = 14V, has a (C_x/C_o) of 1.3% (much larger than the 0.06% needed by the filter of [25]) and an R_x of 48Ω. So with the 20-nm gap, the motional resistance of the 163-MHz case is sufficient to permit a filter with 200Ω terminations. It, however, is larger than the needed 12.9Ω for a 50Ω termination even though its (C_x/C_o) is more than sufficient.

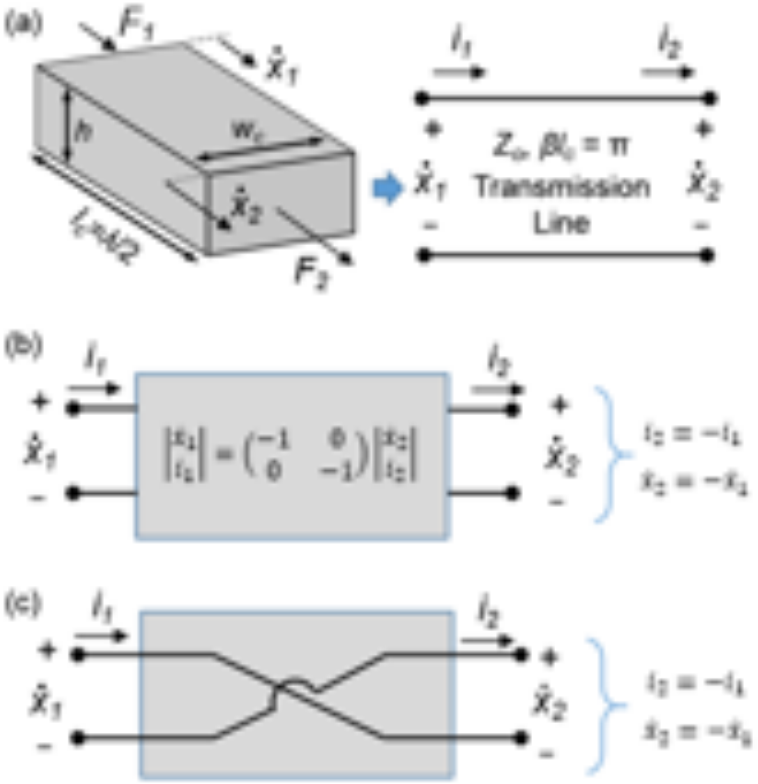


Fig. 2.14: (a) Schematic view of a λ/2 array extensional mode coupling beam and its acoustic transmission equivalent representation with acoustic impedance Z_o and electrical length $\beta l_c = \pi$. (b) ABCD matrix representation for the acoustic transmission line formed by the λ/2 beam. (c) Electrical equivalent circuit representation of the λ/2 beam.

The solution: Arraying to further lower R_x without affecting (C_x/C_o).

2.8. Disk Array-Composite Design

Section 2.5 and Fig. 2.1 briefly introduced the strategy of arraying N_{io} disk resonators to attain a combined output current N_{io} times larger than that of a single resonator for the same input voltage, i.e., a motional resistance N_{io} times smaller. Of course, the currents of the devices in an array sum constructively only if all devices vibrate in phase and at the same frequency. To insure this, as depicted in Fig. 2.13, the disks in the array are mechanically strong-coupled by half-wavelength beams that effectively transform the array into a single multi-resonator composite device in which all constituent disks vibrate in unison at one mode frequency. Here, the use of half-wavelength coupling links ideally selects one desired mode and rejects other modes [46]. Its strong coupling also avoids motional resistance reductions predicted for weakly coupled resonator arrays [47]. The result: An array-composite resonator with substantially lower impedance and greater power handling than a single one of its constituents.

The action of the half-wavelength extensional-mode coupling beams is perhaps best understood by closer inspection of the beam itself, depicted in Fig. 2.14, and its defining chain matrix, which relates the force F and the velocity $\dot{x}$ on both ends of the beam (*cf.* Fig. 2.14(a)), taking the form

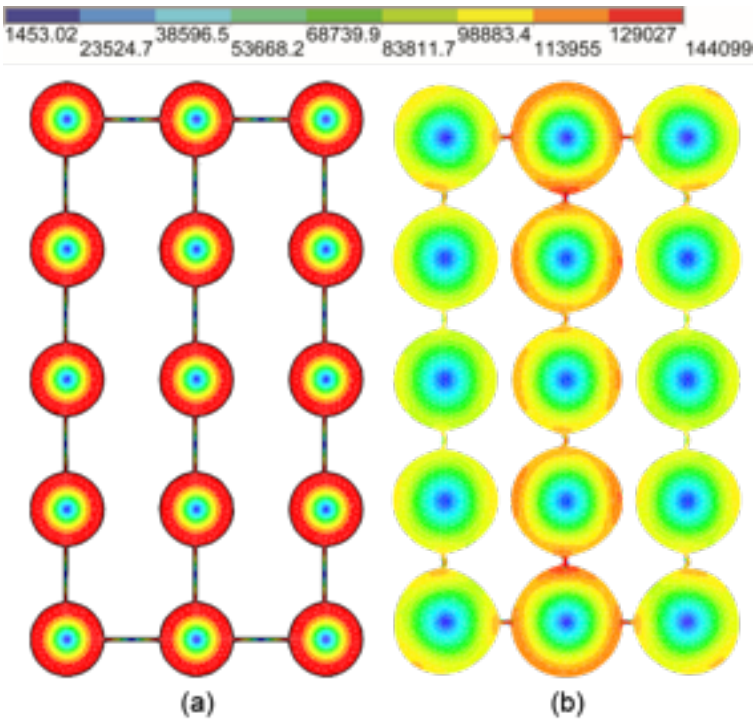


Fig. 2.15: Finite element modal analysis result for a 5×3 disk resonator array coupled by (a) ideal λ/2 length beams, and (b) non-ideal 0.6λ length beams with process variations. The color map legend indicates local mode shape displacement with arbitrary units.

$$\begin{bmatrix} F_1 \\ \dot{x}_1 \end{bmatrix} = \begin{bmatrix} \cos(\beta l_c) & jY_o \sin(\beta l_c) \\ jZ_o \sin(\beta l_c) & \cos(\beta l_c) \end{bmatrix} \begin{bmatrix} F_2 \\ \dot{x}_2 \end{bmatrix} \tag{2.37}$$

where Z_o and β, are the characteristic acoustic impedance and propagation constant, respectively, defined in terms of beam thickness h, beam width w_c, beam length l_c, and material properties E and ρ as

$$Y_o = \frac{1}{Z_o} = hw_c\sqrt{\rho E}, \qquad \beta = \frac{\omega}{v_p}, \qquad v_p = \sqrt{\frac{E}{\rho}} \tag{2.38}$$

where v_p is the acoustic velocity.

Considering the beam as a mechanical transmission line with acoustic wavelength λ at the desired vibration mode frequency defined as

$$\lambda = \frac{1}{f_0}\sqrt{\frac{E}{\rho}} \tag{2.39}$$

and setting the coupling beam length $l_{c,\lambda/2}$ to half-wavelength, given by

$$l_{c,\lambda/2} = \frac{1}{2f_0}\sqrt{\frac{E}{\rho}} \tag{2.40}$$

$\beta l_{c,\lambda/2} = \beta\lambda/2 = \pi$ in (2.37), which then yields

$$\begin{bmatrix} F_1 \\ \dot{x}_1 \end{bmatrix} = \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} F_2 \\ \dot{x}_2 \end{bmatrix}, \quad \begin{matrix} F_1 = -F_2 \\ \dot{x}_1 = -\dot{x}_2 \end{matrix} \tag{2.41}$$

states that half-wavelength coupling enforces equal force and displacement amplitudes with opposite phases at the coupling beam-ends. In other words, it forces the disks attached at the ends of the extensional coupling to vibrate in unison, i.e., with the same phase. From Fig. 2.8 and the discussion of Section 2.4, this means it forces the highest frequency mode and rejects all other modes. Ideally, the in-phase mode would be the only one permissible under half-wavelength coupling. Fig. 2.15(a) presents the finite element analysis (FEA)-simulated mode shape for a 5×3 half-wavelength-coupled array showing identical contour-mode shapes for all resonators. With non-ideal 0.6λ coupling beams, however, apparent mode shape and phase variation occur between the disks in the coupled array as shown in Fig. 2.15(b).

To lend more insight into the action of the half-wavelength beams, Fig. 2.14(a) presents alongside the schematic view of a $\lambda/2$ coupling beam its acoustic transmission line equivalent model for which (2.41) governs the force-to-velocity transfer function at the beam ends. Here, the direct electromechanical analogy [48] [49] models the force and velocity applied on the ends of the beam as the voltages and currents, respectively, across the ports of the transmission line. It is important to note that the width of the $\lambda/2$ beam does not affect its network properties defined by (2.41). Thus, the width of the $\lambda/2$ couplers typically equals the minimum achievable critical dimension of the fabrication technology. A wider beam width would still mathematically satisfy (2.41), but would risk perturbing the vibration mode shape of the adjacent connected disks.

To provide a more visual circuit model, Fig. 2.14(b) equates the $\lambda/2$ beam to a two-port network using the ABCD matrix of (2.41), which then further simplifies to the electrical equivalent circuit of Fig. 2.14(c). This cross-coupled circuit clearly shows that the $\lambda/2$ beam acts to invert the phase of the motions at its ends, consistent with the previous discussion.

A. Non-I/O Disks

Upon closer inspection, the Fig. 2.13 array-composite contains additional disks in the array-composite beyond those used for input/output (I/O). These include disks whose electrodes accept frequency tuning voltages rather than I/O inputs in order to correct for practical issues caused by finite fabrication tolerances that introduce device mismatch; as well as electrodeless buffer disks that alleviate fabrication stress that otherwise could debilitate a large mechanical circuit like that of Fig. 2.1. These non-I/O disks add to the total disk count in an array-composite, so further raise the impedance seen into each individual disk (either electrically or mechanically). As will be seen, they also lower the effective electromechanical coupling of a disk array-composite. Later sections paper will further detail the need for these extra disks, but for now, any array-composite model must include them.

B. Array-Composite Equivalent Circuit

The electrical equivalent circuit for the simple λ/2-coupled two-disk array-composite of Fig. 2.16(a) results via simple combination of the electrical equivalent circuit representations of the λ/2 beam presented in Fig. 2.14(c) and the circuit model of a single disk resonator presented in Fig. 2.11. Fig. 2.16(b) does just this. Redrawing the circuit then yields the visually simpler version of

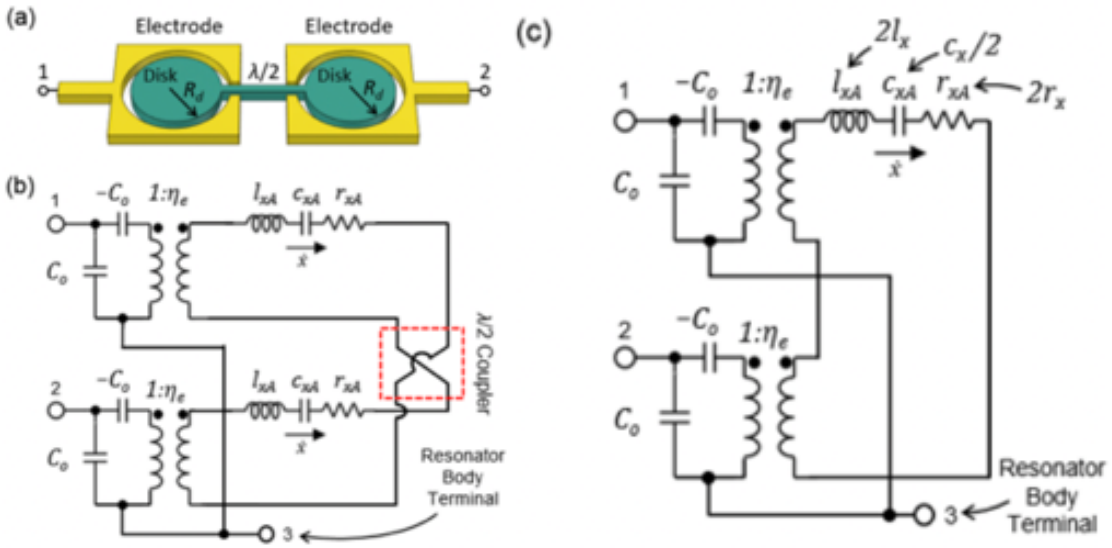


Fig. 2.16: (a) Schematic view a two-resonator network coupled with a half-wavelength beam. (b) Electrical equivalent circuit representation of the two-resonator array-composite that combines the circuits presented in Fig. 2.11 and Fig. 2.14(c); and (c) the same circuit after combining series elements.

Fig. 2.16(c) that better elucidates the series and parallel connected components. Here, it is no surprise that the core LCR elements modeling the vibrating disks cascade in series, since λ/2-coupling forces the disks to vibrate in-phase with identical mode shapes. The result: Their dynamic stiffnesses, masses, and damping losses add linearly. Similarly, since the electrodes modeled by the transformers are in parallel, the forces exerted by the electrodes add cumulatively to generate a total combined force N_{io} times larger than that of a single electrode, where N_{io} is the number of driven input/output (I/O) electrodes, each fully surrounding a disk to the extent possible.

Fig. 2.13 presents a more complex scenario, since some disks contribute to I/O, while others do not, as they might serve frequency tuning or other purposes; and any resonator may be used to mechanically couple to another mechanical structure, as indicated by the dashed beam on the right. The total effective equivalent circuit for an N_{tot}-resonator $\lambda/2$-coupled array-composite with N_{io} I/O disks, N_t tuning disks, and N_b buffer disks becomes that presented in Fig. 2.17, where expressions for the elements and turns ratios now take on the following forms:

$$\begin{aligned} \eta_{eA} &= N_{io} \times \eta_e \\ \eta_{tA} &= N_t \times \eta_e \\ r_{xA} &= N_{tot} \times r_x \\ l_{xA} &= N_{tot} \times l_x \\ c_{xA} &= \frac{1}{N_{tot}} \times c_x \end{aligned} \tag{2.42}$$

where η_{eA} and η_{tA} are the electromechanical coupling coefficients at the array-composite's input-output and tuning electrodes, respectively. Similarly, r_{xA}, l_{xA}, and c_{xA} represent the core-*LCR* values that model the equivalent damping, dynamic mass, and inverse dynamic stiffness of the array-composite, respectively. The mechanical coupler turns ratio η_c is 1 for the present case where mechanical couplers attach only at the edges of disks, but can be different from 1 when the velocity

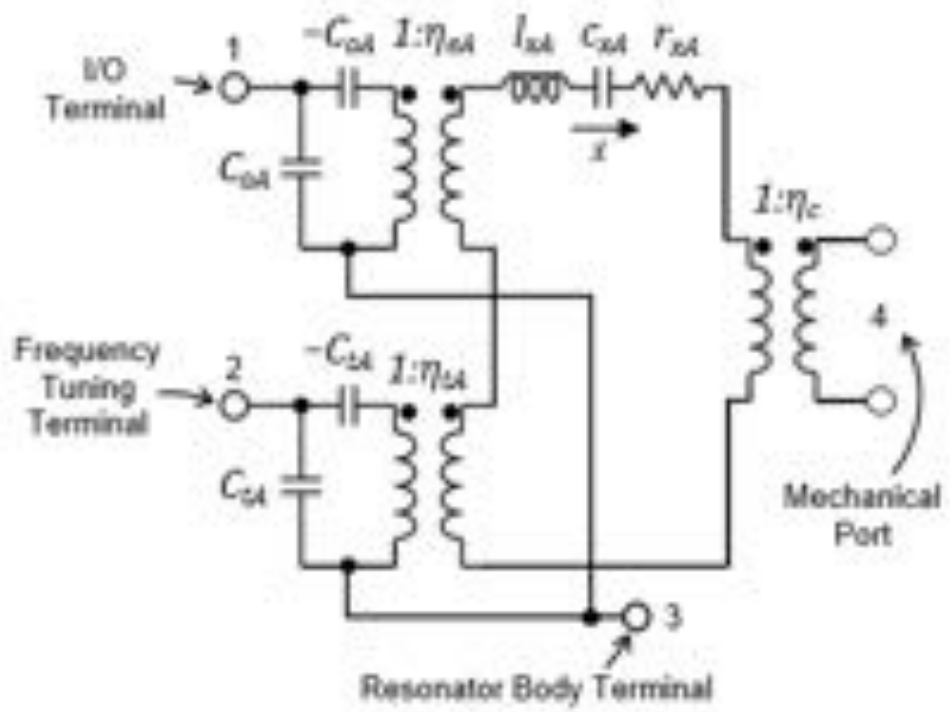


Fig. 2.17: General electrical equivalent circuit for the structure of Fig. 2.13.

at the core or reference point for the *LCR* circuit differs from that at the coupling location [20], [21].

The Fig. 2.17 circuit shows four terminals: one that goes to the electrodes of all disks involved with I/O; one that goes to the electrodes of all disks intended for frequency tuning; one that goes to a mechanically coupled next stage; and one that goes to the movable structure. The circuit, of course, is general enough that many of the electrodes are re-assignable to other purposes at will.

C. Array-Composite Motional Resistance

With I/O electrodes in parallel and all disks vibrating in unison, the currents flowing into the I/O electrodes now add in phase, allowing for a total current N_{io} times that of a single electrode fully surrounding a single disk. Since the current increases for the same input voltage, the motional resistance of the structure decreases to

$$R_{xA} = \frac{N_{tot}}{N_{io}^2} R_x \tag{2.43}$$

where R_{xA} and R_x represent the motional resistance of the array-composite and a single disk resonator, respectively. The corresponding expression for the filter termination resistance follows from inserting (2.43) in (2.7) as

$$R_Q = \left(\frac{Q}{q_n Q_f} - 1\right)\frac{N_{tot}}{N_{io}^2} R_x \cong \frac{Q}{q_n Q_f}\frac{N_{tot}}{N_{io}^2}\frac{r_x}{\eta_e^2} \tag{2.44}$$

where rewriting the single resonator's damping term r_x in terms of the resonator Q, dynamic mass m_m, and electromechanical coupling coefficient η_e leads to

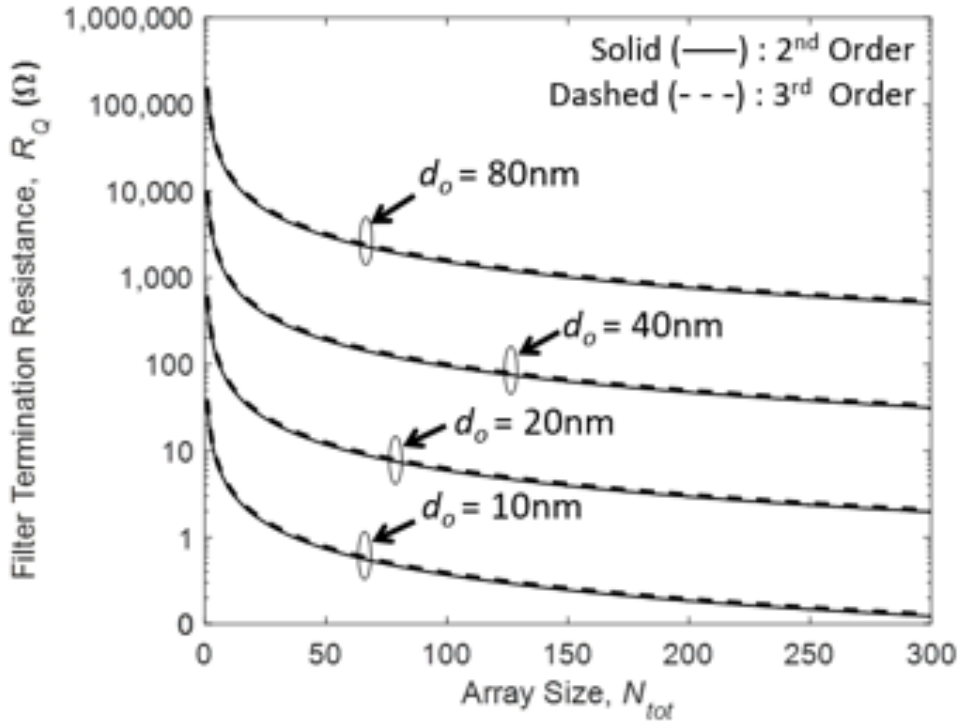


Fig. 2.18: Simulated plots of filter termination resistance vs. number of 433-MHz disk resonators in a half-wavelength-coupled array-composite calculated for three different gap spacing cases assuming two- and three-resonator 0.5dB-ripple Chebyshev filter designs. For these simulations, V_P = 15V, h = 3μm, P_{BW} = 0.1%, $N_{tot} = N_{io}$, ρ = 2300kg/m^3, χ = 0.763 (1st mode), θ_{ov} = 2π, q_n (2nd order) = 1.9497, q_n (3rd order) = 1.8638. The curves show only small differences between 2nd and 3rd order.

$$R_Q = \frac{1}{Q_f}\frac{N_{tot}}{N_{io}^2}\frac{2\pi f_o m_m}{q_n \eta_e^2} \tag{2.45}$$

Rewriting m_m and η_e of (2.45) in terms of the fundamental design variables yields

$$R_Q = \frac{f_o}{Q_f}\frac{N_{tot}}{N_{io}^2}\frac{d_o^4}{V_P^2}\frac{2\pi^2 \chi \rho}{q_n h \varepsilon_o^2 \theta_{ov}^2} \tag{2.46}$$

The right-hand-most form of (2.44) addresses the specific case where the filter insertion loss is low, i.e., the resonator is Q much larger than the filter Q_f. In this case, the value of R_Q is independent of the unloaded resonator Q, and the knobs that best specify its value become the electrode-to-resonator gap spacing d_o (with a 4th power dependence) and the dc-bias voltage V_P (with a square-law dependence).

A single polysilicon disk resonating at 433 MHz with a Q of 20,000, 40-nm gaps, 26V dc-bias, thickness h of 3μm, and fully surrounding electrodes, i.e. θ_{ov}=2π, would exhibit a motional resistance R_x of 364Ω, which after assembly into a filter circuit is much too high to match to adjacent stages in a conventional receiver. In contrast, combination of 20 of these same resonators into a disk array-composite (with 12 I/O resonators, 8 buffers) with all I/O resonators hooked in parallel allows summation of output currents to reduce the motional resistance down to 50Ω. According to (2.46), a two-resonator 0.1% bandwidth 0.5-dB-ripple Chebyshev filter using this array-composite

requires a termination resistance of 470Ω. Reducing gaps to 20-nm and dropping the dc-bias voltage to 9V reduces the needed number of array-composite resonators to 10 (with 6 I/O) to achieve the same filter response, but with an R_Q of 49Ω.

Fig. 2.18 plots termination resistance R_Q versus number of 433-MHz based resonators in the array-composite for three different gap spacing examples of 80nm, 40nm, 20nm, and 10nm used in two- and three-resonator 0.5dB-ripple Chebyshev filters, showing the large range over which gap spacing and array size choices specify the filter termination resistance. Note that 10-nm gaps are not unreasonable, given recent demonstrations of 13-nm gaps [45].

D. Array-Composite Power Handling

In addition to motional resistance, the power handling of an array-composite improves over that of a single constituent resonator. This is obvious, given that the current now distributes among N_{io} devices, so any detrimental effects, e.g., heating, lessen by approximately the factor N_{io}.

Third-order intermodulation distortion is often a good gauge for the largest input power acceptable to a given circuit element or system block. For practical applications, the third-order intermodulation intercept point IIP_3, defined as the input power at which the output powers due to an input at the carrier frequency and at two frequencies equally spaced from it, i.e. $f_1 = f_0 - \Delta f$ and $f_2 = f_0 - 2\Delta f$, are equal, is a good metric for device or circuit linearity. [50] already developed an expression governing the IIP_3 of a radial-contour mode disk resonator, repeated here for convenience as follows [51], [37]:

$$P_{IIP_3} = P_{V^2X} \parallel P_{VX^2} \parallel P_{X^3} \tag{2.47}$$

This compact IIP_3 power expression comprises the parallel connection of three resonator nonlinearity sources given by

$$\begin{aligned} P_{V^2X} &= \frac{4\pi\varepsilon_o f_o Q V_P^2 A_o}{d_o(2\Theta_1 + \Theta_2^*)} = \frac{4\pi\varepsilon_o f_o Q V_P^2 Rh\theta_{ov}}{d_o(2\Theta_1 + \Theta_2^*)} \\ P_{VX^2} &= \frac{4\pi f_o Q d_o^2 k_{re}}{3\Theta_1(\Theta_1 + 2\Theta_2^*)} = \frac{16\pi^4 f_o^3 Q d_o^2 R^2 h\chi\rho}{3\Theta_1(\Theta_1 + 2\Theta_2^*)} \\ P_{X^3} &= \frac{2\pi f_o Q d_o^5 k_{re}^2}{3\varepsilon_o A_o V_P^2 \Theta_1^2 \Theta_2^*} = \frac{32\pi^7 f_o^5 Q d_o^5 R^3 h\chi^2\rho^2}{3\varepsilon_o \theta_{ov} V_P^2 \Theta_1^2 \Theta_2^*} \end{aligned} \tag{2.48}$$

where starred variables indicate complex conjugates, A_o is the overlap area between the electrode and the disk, k_{re} is the effective stiffness of a single disk at the edge, Θ_1 and Θ_2 model the degree to which the resonator's amplitude transfer function attenuates the blocker input tones and take the form

$$\begin{aligned} \Theta_1 &= \frac{1}{1 - (f_1/f_0)^2 + j(f_1/Qf_0)} \\ \Theta_2 &= \frac{1}{1 - (f_2/f_0)^2 + j(f_2/Qf_0)} \end{aligned} \tag{2.49}$$

Here, the P_{V^2X} and P_{VX^2} terms derive from nonlinear interactions between voltage and displacement, while the P_{X^3} term is purely displacement-derived.

For an array-composite like that of Fig. 2.13 with N_{io} I/O electrodes and N_{tot} electrodes, the expression for IIP_3 becomes

$$P_{IIP_3} = N_{tot}\left[\beta P_{V^2X} \parallel P_{VX^2} \parallel \frac{P_{X^3}}{\beta}\right] \tag{2.50}$$

where $\beta = N_{io}/N_{tot}$. If all disks are I/O disks, then the improvement in IIP_3 becomes linear with N_{tot}.

E. Array-Based Mechanical Impedance Tailoring

Equation (2.43) already showed how the number of resonators N_{tot} used in a mechanically coupled array-composite acts as a knob to control the electrical resistance presented by any one (or group) of its resonators. Note further that coupling all resonators in this way does more than merely add together currents to lower electrical motional impedance and raise power handling. In fact, one of the most useful characteristics of an array-composite for filter design is the degree to which it can tailor the mechanical impedance, i.e., as governed by the effective stiffness and mass, presented to a mechanical input/output port.

The amount of stiffness tailoring available is readily apparent when determining the impedance seen into the mechanical port in the array-composite equivalent circuit of Fig. 2.17 with the other ports grounded. In particular, grounding terminals 1, 2, and 3 of this circuit leaves port 4 essentially coupled to an effective resonator with mass, stiffness, and damping values all N_{tot} times as large as that of a single resonator. This means the stiffness presented to a mechanical structure, e.g., a coupling beam, attached to a disk's edge, is N_{tot} times as large as that of a single disk resonator. Thus, N_{tot} acts as a knob to control the mechanical impedance presented by any one of its resonators.

As will be seen, the dynamic stiffness presented at a coupling location very much controls the bandwidth of a given filter design. The ability to raise the presented stiffness by arraying equates to an ability to decrease the percent bandwidth of a given filter, such as needed for RF channel-selection.

2.9. Minimum Electromechanical Coupling Strength Required for the Chosen Bandwidth

Although array size strongly influences the impedance presented by the combined array-composite input terminal, it does not raise the electromechanical coupling strength gauged by the ratio of motional-to-static input capacitance (C_{xA}/C_{oA}). For the case where all disks possess I/O electrodes and all electrodes are hooked in parallel, i.e. $N_{tot} = N_{io}$, (C_{xA}/C_{oA}) follows readily by simply taking the ratio of

$$C_{xA} = N_{tot}\eta_e^2 c_x = N_{tot}\frac{V_P^2}{d_o^4}\frac{h(\varepsilon_o R\theta_{ov})^2}{\pi^3 \chi K_{mat}^2 E} \tag{2.51}$$

and

$$C_{oA} = N_{tot}C_o = N_{tot}\frac{\varepsilon_o R\theta_{ov} h}{d_o} \tag{2.52}$$

which yields

$$\frac{C_{xA}}{C_{oA}} = \frac{V_P^2}{d_o^3}\frac{\varepsilon_o R\theta_{ov}}{\pi^3 \chi K_{mat}^2 E} \tag{2.53}$$

Here, (C_{xA}/C_{oA}) does not change with the number of I/O disks.

If, on the other hand, non-I/O disks are included, as described in Section 0, the expression for electromechanical coupling strength becomes

$$\frac{C_{xA}}{C_{oA}} = \frac{N_{io}}{N_{tot}}\frac{V_P^2}{d_o^3}\frac{\varepsilon_o R\theta_{ov}}{\pi^3 \chi K_{mat}^2 E} \tag{2.54}$$

where N_{tot} is the total number of mechanically coupled disks that include both the I/O and non-I/O disks, which means the N_{io}/N_{tot} term in (2.54) is always less than one. In (2.54), the only other adjustable variables are V_P and d_o, as the rest are fixed by the chosen center frequency f_o. In most practical cases, it is up to the dc-bias V_P and electrode-to-resonator gap d_o scaling to insure adequate electromechanical coupling (C_{xA}/C_{oA}) to meet the requirement of (2.3) [36].

To gauge how the minimum C_{xA}/C_{oA} that avoids passband distortion for a given filter bandwidth B scales with frequency, one can use (2.35) and (2.54) to rewrite (2.3) as

$$\frac{1}{B}\left(\frac{V_P^2}{d_o^3}\right)\left(\frac{\varepsilon_o \theta_{ov} N_{io}}{2\pi^3 \chi K_{mat} N_{tot}\sqrt{E\rho}}\right) > \gamma \tag{2.55}$$

The terms in the rightmost parentheses in (2.55) comprise material, resonator, and filter design constants that are fixed for a given filter response and technology choice. This again leaves the bias voltage V_P and electrode-to-resonator gap spacing d_o as the primary design knobs to satisfy (2.55) for a given desired bandwidth B. It is important to observe that (2.55) is independent of disk radius, and thus, of the filter center frequency f_o. Thus, if the needed bandwidth stays constant for a bank of filters over a range of frequencies—which is often the case for RF channel-selection—then so do the needed gap d_o and bias voltage V_P for each filter in the bank.

2.10. Filter Passband Specification

Section 2.4 described how mechanical coupling of two identical single disk resonators—or more preferably identical array-composites that behave as single disks with reduced R_x—creates a two degree of freedom system with two closely spaced modes that define a filter passband, as described in Fig. 2.8. A more explicit expression for the bandwidth of the filter follows from (2.10), which accounting for the stiffness transformation afforded by arraying described by (2.42), yields

$$B = \frac{k_{c,ij}}{k_{reA}}\frac{f_o}{k_{ij}} = \frac{k_{c,ij}}{k_{re}}\frac{f_o}{N_{tot}k_{ij}} \tag{2.56}$$

where k_{reA} is the effective stiffness of a disk array-composite, and $k_{c,ij}$ is the stiffness of the filter coupling beam between i^{th} and j^{th} resonators in a multi-resonator filter. While any coupling beam length can be chosen to provide the dynamic stiffnesses $k_{c,ij}$ for the required filter bandwidth in(2.56), beams with lengths matching odd multiples of the quarter-wavelength, i.e. $\lambda/4$, form a special case that minimizes the sensitivity of the filter response to variations in beam dimensions, e.g., caused by finite fabrication tolerances. This resilience against process variations arises from

the fact that $\lambda/4$ dimensions zero out the derivative of the dynamic beam stiffness with respect to the beam length [49].

A. Electrical Equivalent Circuit for a λ/4 Coupling Beam

Like other components of a mechanical filter, the behavior of a $\lambda/4$ coupling beam follows the prediction of its equivalent electrical circuit. As described in Section 2.8, the characteristics of a small cross-section coupling beam vibrating in its extensional mode are similar to the behavior of an electrical transmission line, and in *ABCD* matrix form conform to (2.37). The special case of a quarter-wavelength coupling beam with $l_c = \lambda/4$ sets the electrical length of the transmission line equivalent representation of the beam to $\beta l_c = \pi/2$ in (2.37), which then yields the *ABCD* matrix expression for a $\lambda/4$ coupling beam

$$\begin{bmatrix} F_1 \\ \dot{x}_1 \end{bmatrix} = \begin{bmatrix} 0 & jY_o \\ jZ_o & 0 \end{bmatrix} \begin{bmatrix} F_2 \\ \dot{x}_2 \end{bmatrix} \tag{2.57}$$

Here, the $\lambda/4$ coupling beam behaves as an impedance inverter commonly used in ladder filter design [52].

As introduced in Section 2.4, a *T*-network of capacitors (*cf.* Fig. 2.8) aptly captures the electrical equivalent lumped circuit model of the $\lambda/4$ coupling beam. Fig. 2.19 presents the transmission line representation of this circuit, where Z_A, Z_B, and Z_C model the series and shunt arm impedances. Equating the *ABCD* matrices of the circuit presented in Fig. 2.19 [52] with that of (2.57) leads to

$$\frac{1}{Z_c} = jZ_o \rightarrow j\omega_o c_c = \frac{j}{hw_c\sqrt{\rho E}} \tag{2.58}$$

which then yields the expression for the dynamic stiffness of a $\lambda/4$ coupling beam in terms of beam dimensions:

$$k_c = \frac{1}{c_c} = \frac{\pi E}{2}\frac{hw_c}{l_{\lambda/4}} \tag{2.59}$$

where w_c is the width of the coupling beam, and $l_{\lambda/4}$ is the beam length equal to

$$l_{\lambda/4} = \frac{\xi}{4f_o}\sqrt{\frac{E}{\rho}}, \qquad \xi = 1, 3, 5, \ldots \tag{2.60}$$

where the presence of ξ indicates that any odd multiple of the quarter-wavelength also provides the desired variance resilience.

B. λ/4 Coupling Beam Width & Array Size

Inserting (2.39) and (2.59) in (2.56) provides the filter bandwidth expression in terms of fundamental device geometry and material properties:

$$B = \frac{w_c}{N_{tot}}\left(f_o^2 \frac{2}{\xi\pi^2 K_{mat}^2 \chi k_{ij}}\sqrt{\frac{\rho}{E}}\right) \tag{2.61}$$

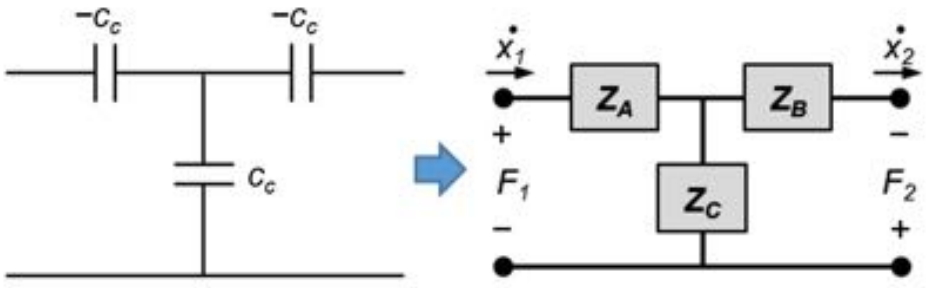


Fig. 2.19: Transmission line model equivalent of the λ/4 beam electrical equivalent circuit

The only free variables to set the filter bandwidth B in (2.61) are the $\lambda/4$ beam width w_c and the array size N_{tot}, where the remaining terms given in the parentheses are fixed by other filter specifications.

It is important to observe from (2.61) that very small bandwidths may require excessively narrow beam widths. This becomes especially true if the array-composite design approach is not used, i.e. if N_{tot}=1. Interestingly, use of array-composites with large enough N_{tot} becomes critical to maintaining w_c wider than the critical dimension $w_{c,min}$ that can be reliably manufactured, as governed by

$$w_c = N_{tot}\left(\frac{B}{f_o}\right)\frac{\xi\pi^2 K_{mat}^2 \chi k_{ij}}{2f_o}\sqrt{\frac{E}{\rho}} > w_{c,min} \tag{2.62}$$

Taking as an example the 433-MHz disk resonator of Section 2.8-C, the use of stand-alone polysilicon disk resonators to form a second order Chebyshev filter with 0.5dB ripple not only demands an impractically high termination resistance (exceeding 10kΩ), but also requires a very narrow $\lambda/4$ coupling beam width of 22nm with k_{ij} =0.7225 and N_{tot}=1 in (2.62). Here, increasing the array size to N=24 adjusts the beam width to w_c = 534nm that can now be reliably patterned and etched into 3μm-thick polysilicon using DRIE, with the added benefit of low sub-1kΩ filter termination resistances. So arraying is critical to successful filter realization.

Equation (2.62) further indicates that filters with very small fractional bandwidth $P_{BW} = B/f_o$, such as needed for RF channel-selection [13], must use resonator array-composites with size N_{tot} greater than a minimum number N_{min} set by $w_{c,min}$ according to

$$N_{tot} \geq N_{min} = \frac{w_{c,min}}{P_{BW}}\frac{2f_o}{\xi\pi^2 K_{mat}^2 \chi k_{ij}}\sqrt{\frac{\rho}{E}} \tag{2.63}$$

regardless of other filter specifications such as filter termination resistance or layout area. Fig. 2.20 uses (2.63) to plot the minimum achievable fractional bandwidth P_{BW} for a 2nd order polysilicon Chebyshev filter operating at 1GHz for different minimum filter coupling beam widths. These curves demonstrate the wide fractional filter bandwidth range achievable by mechanically coupled disk filters, where larger array sizes enable smaller fractional bandwidths desired for channel-select applications.

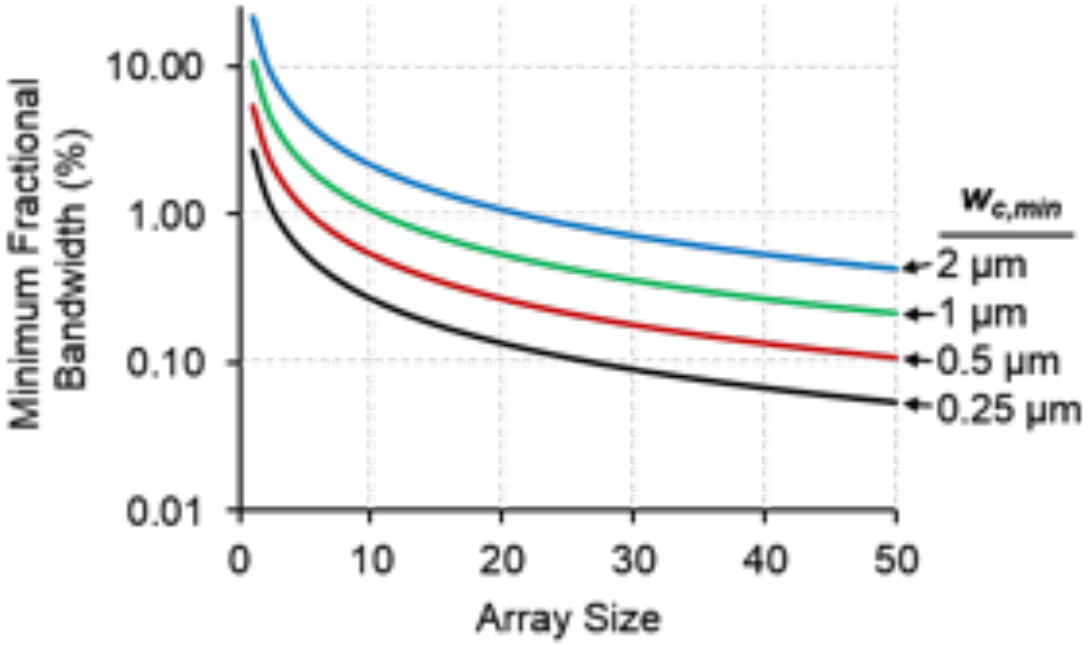


Fig. 2.20: Simulated curves of minimum achievable fractional bandwidth as a function of array size for different minimum coupling beam widths for a 2nd order polysilicon Chebyshev filter operating at 1GHz.

The large number of $\lambda/2$ coupled disks indicated in Fig. 2.20 may at first glance raise area and cost concerns; however, the disks that form the array have tiny dimensions that scale inversely proportional to frequency. For example, a 0.1% fractional bandwidth 2nd order polysilicon filter operating at 1GHz with 0.25μm wide coupling beams requires N_{tot}=25 $\lambda/2$ coupled resonators per array-composite. As illustrated in Fig. 2.1, a second order differential filter comprises four array-composites, which in this case leads to N_{tot}=25 resonators in each quadrant. This 100-coupled disk resonator circuit would consume only 110μm × 110μm die area (assuming electrode routing is done in another layer as in CMOS), where each disk has a diameter of only 5.4μm. To put this tiny footprint in perspective, one could amass 2,025 similar filters on a 5mm×5mm chip, perhaps towards devising a low cost, programmable mode-selectable RF channelizing filter bank for a very flexible receiver front-end capable of satisfying nearly any communication standard.

Thought this paper focuses on channel-selecting filters, note that larger bandwidth filters, e.g., 3% for band-selection, can employ multiple wider coupling beams to raise the spring-to-resonator array-composite ratio.

2.11. Differential Mechanical Design

A differential filter with electrically and mechanically symmetric drive and sense has two advantages over a single-ended one:

1) Symmetric (i.e., differential) design suppresses spurious modes close to the filter center frequency generated by complex mechanical circuit non-idealities [25].
2) Common-mode feedthrough currents flowing through parasitic elements, e.g., capacitors formed by electrode-disk overlaps and substrate couplings, cancel.

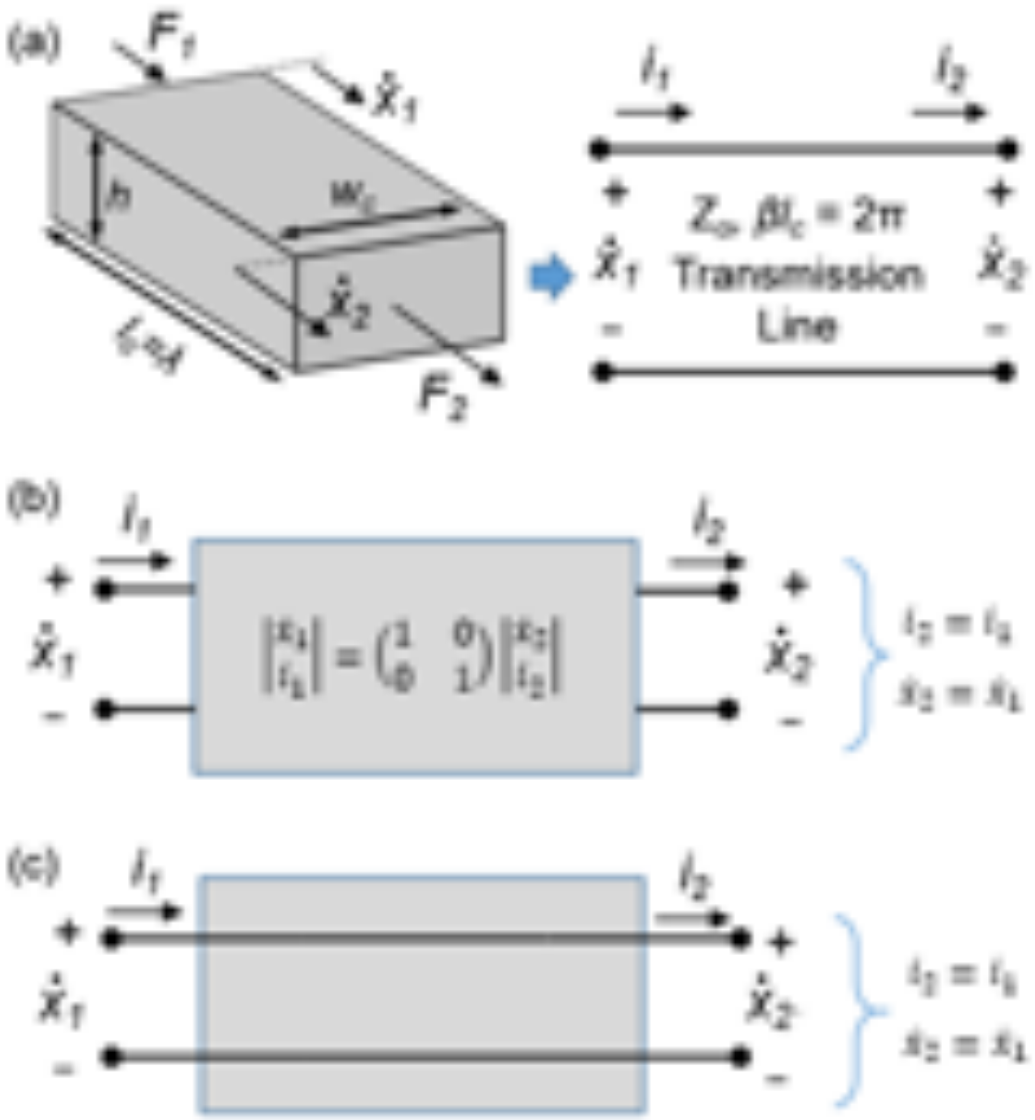


Fig. 2.21: (a) Schematic view of a λ extensional-mode coupling beam and its acoustic transmission equivalent representation with acoustic impedance Z_o and electrical length $\beta l_c = 2\pi$. (b) ABCD matrix representation for the acoustic transmission line formed by the λ beam. (c) Electrical equivalent circuit representation of the λ beam.

Much like differential transistor pair design, if the micromechanical resonator circuit could encompass two symmetric halves forced to resonate at the same vibration frequency but 180° out of phase, this would yield the desired differential operation with the stated benefits. Similar to the analysis presented in Section 2.8 for λ/2 beams that enforce in-phase vibration, the electrical transmission line analogy outlined by (2.37) also reveals the coupling beam design needed to enforce differential vibration. Here, setting the beam length l_c to the full wavelength λ so that the electrical length becomes $\beta l_c = \beta\lambda = 2\pi$ yields the ABCD matrix

$$\begin{bmatrix} F_1 \\ \dot{x}_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} F_2 \\ \dot{x}_2 \end{bmatrix}, \quad \begin{matrix} F_1 = F_2 \\ \dot{x}_1 = \dot{x}_2 \end{matrix} \tag{2.64}$$

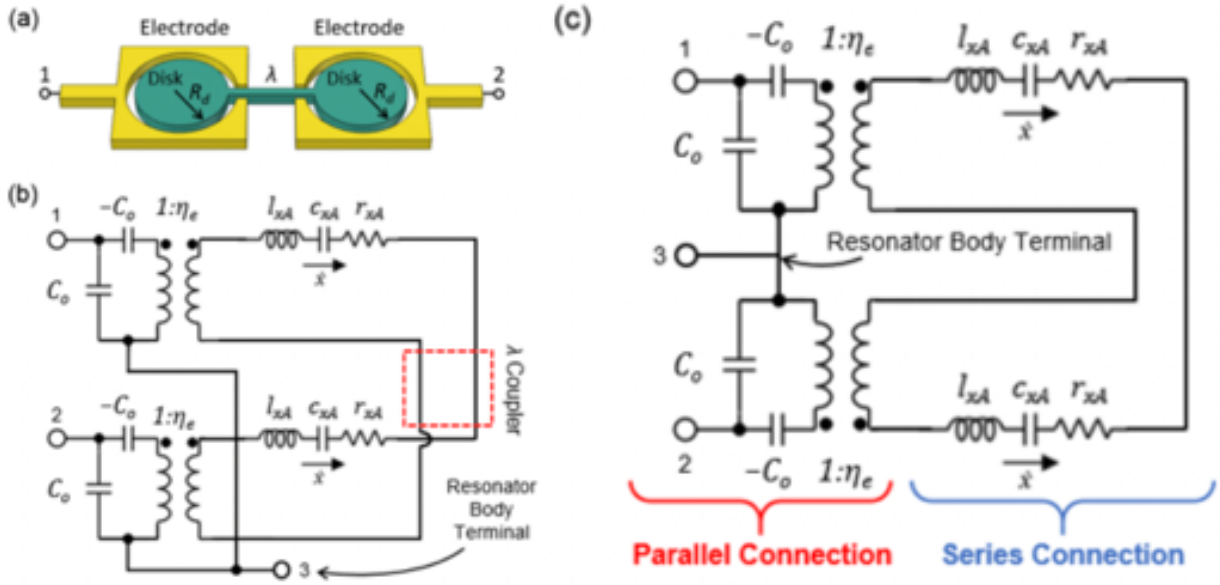


Fig. 2.22: (a) Schematic view of a two-resonator network coupled by a full-wavelength beam. (b) Electrical equivalent circuit representation of the two-resonator differential array-composite that combines the circuits presented in Fig. 2.11 and Fig. 2.21(c); and (c) the same circuit after combining series elements.

With reference to Fig. 2.21(a), the $\dot{x}_1 = \dot{x}_2$ condition in (2.64) is only possible when one of the coupled disks contracts while the other expands to keep the displacement magnitude and direction on both ends of the coupling beam identical. As a result, λ-coupled disks assume the same vibration frequency but out-of-phase displacement.

Similar to Fig. 2.14 that explains the in-phase $\lambda/2$ coupler model, Fig. 2.21 illustrates the equivalent circuit model for the full-wavelength differential coupler. Here, the width of the λ differential coupler does not change its network properties at resonance, much like the $\lambda/2$ coupler, and typically equals the minimum critical dimension to avoid loading the disk resonators by unnecessarily wide coupling beams.

Fig. 2.22 illustrates the electrical equivalent circuit for a λ-coupled differential disk pair, which combines the equivalent circuit of a single disk resonator given by Fig. 2.11 and the circuit model for the λ coupler given by Fig. 2.21(c). Similar to the $\lambda/2$ coupled case presented in Fig. 2.16(c), the core-*LCR* circuits of the λ-coupled disks add in series. However, in contrast to the $\lambda/2$ coupled case, the electrodes of the λ-coupled pair combine in parallel with differential polarity. Therefore, the electrodes must drive differentially, i.e. with 180° phase difference relative to each other, to avoid cancelling the motional currents generated by the individual disks.

A. Differential Filter Topology

To convey how the overall differential filter structure functions, Fig. 2.23 presents the expected properly terminated filter frequency response for a simplified 4-disk-array version of this design, with dotted lines to show its unterminated response, and with FEA-simulated vibration mode shapes corresponding to each peak of the response. Here, the $\lambda/2$ beams combine four disk resonators in each quadrant to create four array-composites that act like four single disks, but with 4× less R_x. Note how all disks in a given array-composite vibrate with the same phase and mode shape—a result of $\lambda/2$-coupling.

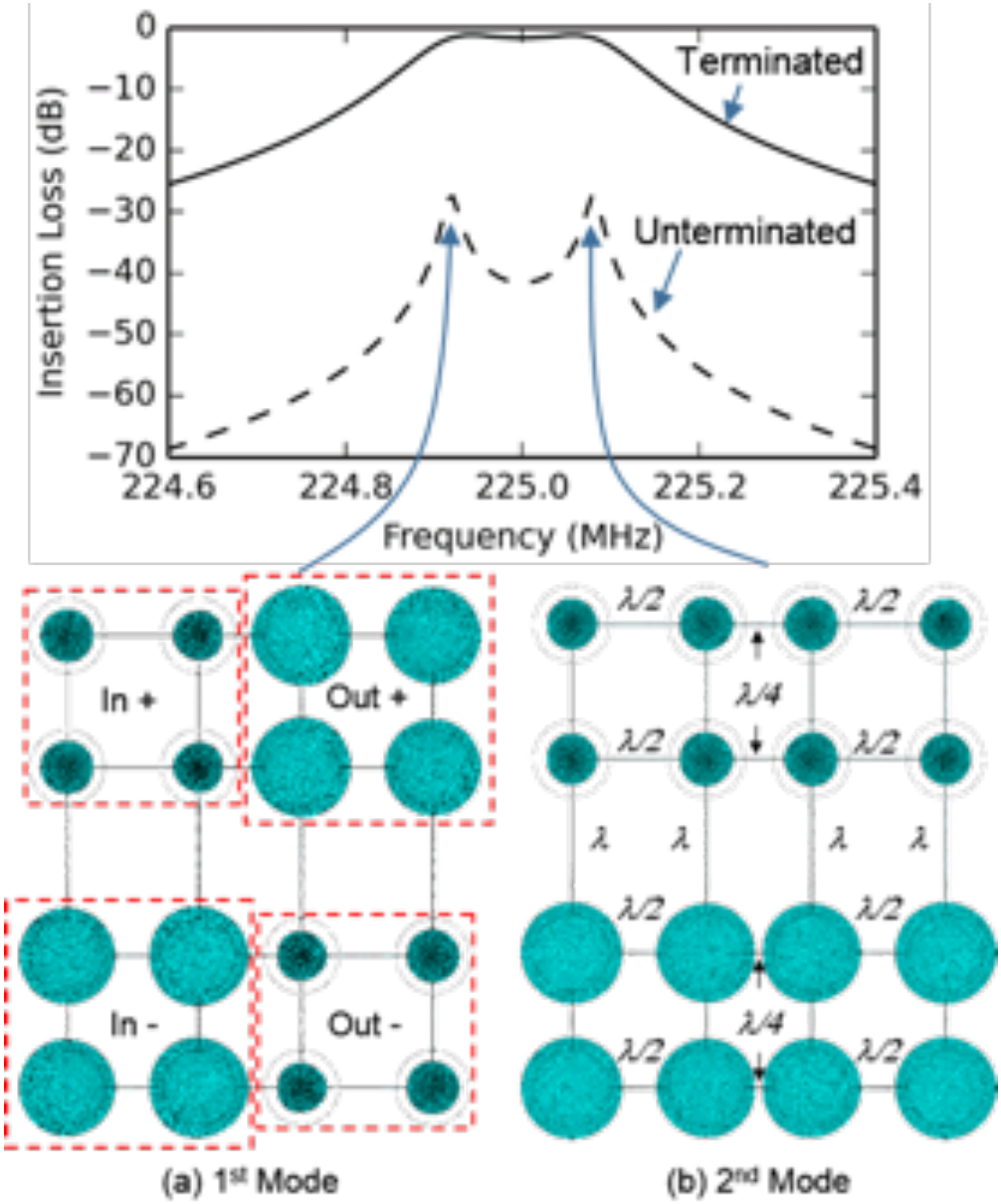


Fig. 2.23: FEA simulation of mode shapes of disk resonators coupled by various wavelength optimized beams, where λ-coupling enforces differential vibration of upper and lower halves, and λ/4 beams realize (a) out-of-phase (lower frequency 1st mode) and (b) in-phase (higher frequency 2nd mode) filter modes. Here, the terminated filter plot simulation used R_Q = 600Ω (i.e., the design value of the actual demonstrated filter of this work), while the unterminated plot used R_Q = 10Ω.

To induce differential operation, λ-coupling of the array-composites in the upper and lower halves of the mechanical circuit enforces out-of-phase motion between left-half top and bottom array-composites (which comprise the input devices) and right-half ones (comprising the output devices). Fig. 2.23 clearly shows how the upper and lower array-composites in the left and right halves move with opposite phase when the whole structure vibrates, no matter the mode. A consequence of this is that (ideally) common-mode input forces cannot excite this filter; only differential ones within the passband can, which means only differential signals can pass through the structure.

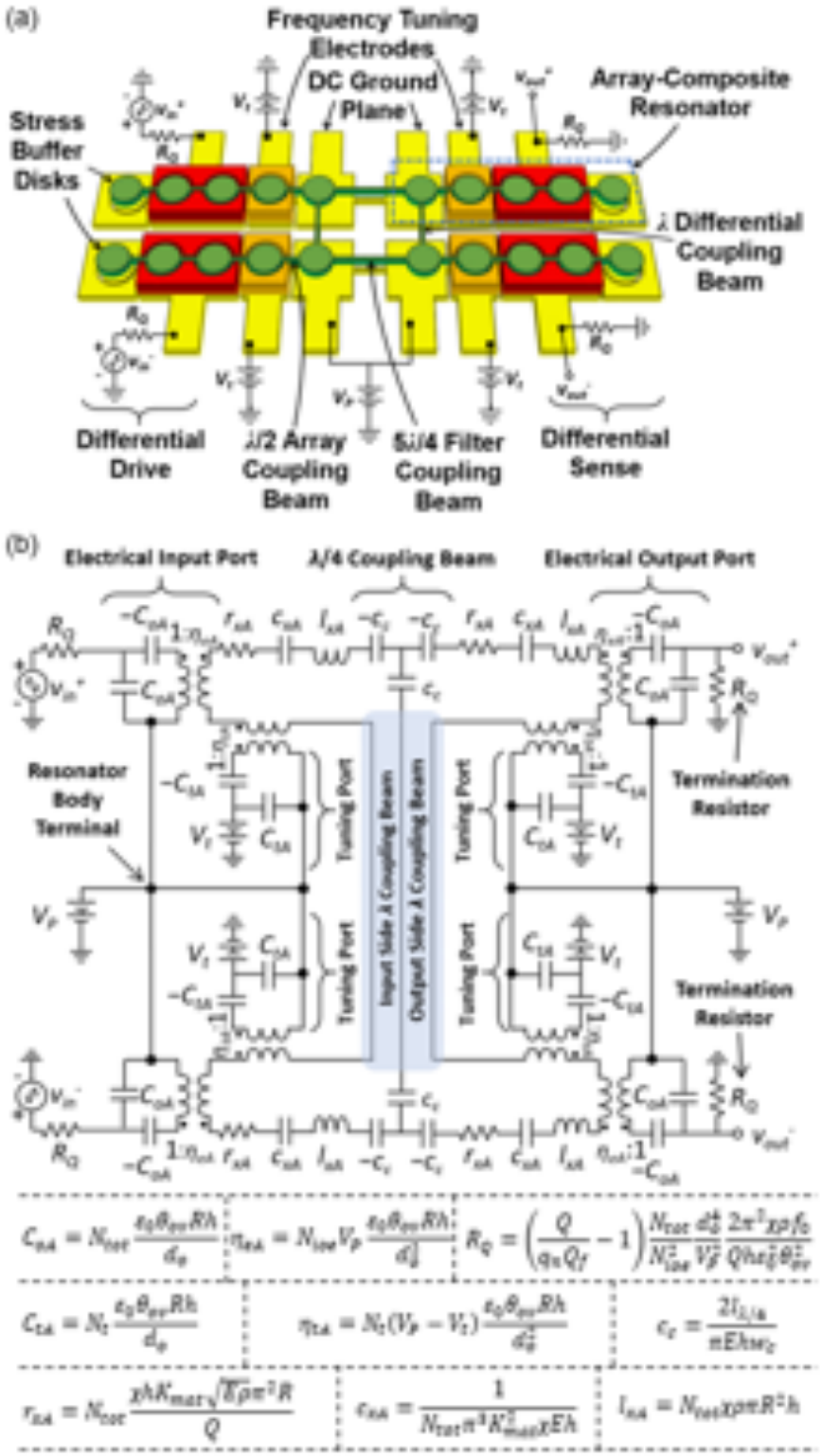


Fig. 2.24: (a) Schematic description of a 2nd order differential filter. (b) Electrical equivalent circuit for a 2nd order differential filter.

The filter response simulations in Fig. 2.23 are not only consistent with Fig. 2.9's depiction of passband flattening via termination, it further more accurately depicts the reduction of insertion

loss expected when one properly terminates a filter [20]. In essence, the termination resistors R_Q serve as source and load resistors. The bigger they are, the less attenuation by the finite filter resistance, so the smaller the insertion loss. Of course, they should not be larger than the filter design value, since this would introduce undue peaking in the passband, compromising its flatness.

2.12. Filter Electrical Equivalent Circuit Model

Much like their transistor circuit counterparts, the design of micromechanical circuits benefits immensely from behavioral models that capture their electrical response in circuit simulators, such as SPICE [53]. It is to this end that previous sections employed electromechanical analogies to capture the functionality added by each level of hierarchy. The overall filter equivalent circuit combines these sub-circuits as modules and accurately captures the filter electrical behavior for arbitrary terminations.

Fig. 2.24 (b) presents the electrical equivalent circuit for the 2nd order differential filter of Fig. 2.24(a), which is simpler than that of Fig. 2.1 for illustrative purposes. Here, each five-resonator $\lambda/2$-coupled array-composite equates to a circuit similar to that of Fig. 2.17(b). Here, N_{io}=2 in (2.42), since only two electrodes in each array-composite bear I/O electrodes, the third reserved for frequency tuning. Buffer devices to alleviate stress-related issues mentioned earlier in Section 0 and detailed more extensively in Section 2.15, also book-end each array. The $\lambda/4$ filter coupling beams that adjoin the upper and lower array-composites equate to *T*-networks like that of Fig. 2.19. Finally, the differential operation imposed by the λ coupling beams between upper and lower array-composites is captured by the electrically balanced differential drive and sense for the symmetric upper and lower half-circuits presented in Fig. 2.24.

Note that the corresponding circuit for the design of Fig. 2.1 is identical to that for Fig. 2.24(a), except that N_{io} is 14, and N_{tot} is 24.

2.13. Filter Design Procedure

Table 2.III presents a procedure for designing a complete filter in the topology of Fig. 2.1 alongside example design values that illustrate the design of the actual filter demonstrated in this work. As is often the case with complex circuit designs, there is no one solution that achieves a given filter specification, but rather several valid solutions, where which one ensues depends upon choices made during the design process. The design process thus becomes an exercise in making choices that optimize a given desired outcome, e.g., smallest size, most tunable, etc. Thus, this section focuses on guidelines for choosing appropriate initial values. The design procedure of Table 2.III does just this.

Any design of course begins with a specification. For a filter, this includes the center frequency f_o, bandwidth B, type (e.g., Chebyshev, Butterworth, etc., essentially specified by k and q values [40]), order, desired termination resistance R_Q, and the structural material set that specifies material constants and Q. Table 2.VI includes these specifications for the demonstrated 224-MHz filter.

Given the hierarchical nature of the Fig. 2.1 circuit, it makes sense to start with the base device, i.e., the disk resonator, then work to build the larger circuit. Design of the disk essentially boils down to determining its radius assuming (for now) no applied voltages, which simplifies things by removing consideration of electrical stiffness. Once known, the disk radius yields its dynamic mass and stiffness. For the demonstrated 224-MHz design, the radius, mass, and stiffness are 12.1μm, 2.42×10^{-12}kg, and 4.79MN/m, respectively.

At this point, one must start making choices. The first things to choose are the electrode-to-resonator gap spacing d_o and the dc-bias voltage V_P. Each of these variables comes with constraints: manufacturing constraints for the former and breakdown or pull-in constraints for the latter. One good approach is to just choose a gap spacing, e.g., 40nm, and then let the (C_x/C_o) spec govern the dc-bias voltage. A good rule of thumb here is to choose a d_o and V_P combination that yields a (C_x/C_o) about 1.5γ times the filter fractional bandwidth (γ from (2.3)). For the demonstrated filter of this work, the intended d_o of 40nm leads to an initial V_P choice of 16V. If the needed V_P ends up too high, then reductions in d_o can help to lower V_P.

The next most logical design parameter to choose is the number of resonators in each of the four $\lambda/2$-coupled array-composite quadrants. Assuming a symmetric design like that of Fig. 2.1, this comes down to choosing the number of rows N_{row} and columns N_{col} of disks and ultimately the number of disks used for I/O, tuning, and stress buffering in each quadrant. Here, one should start by simply choosing the number of rows. Since each row associates with two buffers in the Fig. 2.1 design, i.e., $N_b = 2N_{row}$, the smaller the number of rows chosen, the smaller the array. Choosing only one row per quadrant, however, makes for a long and thin filter for which long distances between disks might worsen fabrication mismatch issues. Choosing a larger number of rows makes for a more compact square-like quadrant, leading to a filter shape like Fig. 2.1, while also providing more points at which $\lambda/4$ coupling beams might be placed (in parallel) for larger bandwidth designs. But at the cost of more resonators. The chosen number of rows is 4 for the demonstrated filter of this work, which Fig. 2.1 in this part depicts in an illustration.

Determination of the number of columns requires first the number of I/O resonators needed to insure the termination resistance value R_Q. The number of I/O resonators needed follows from Fig. 2.18, which derives from (2.46) using the previously chosen values of d_o and V_P and assumes $N_{tot} = N_{io}+2N_{row}$. This equation essentially insures that there are enough I/O resonators N_{io} to satisfy the termination resistance R_Q requirement. Once known, the number of columns must be such that the row-column product (which equals N_{tot}) exceeds $N_{io}+N_b$. For the current design, the number of needed I/O resonators is 15, making the combined I/O and buffer count 23. This requires at least 6 columns, making for a total of 24 resonators per quadrant.

The remaining $N_{tot} - (N_{io}+N_b) = 1$ can then serve as a tuning electrode. If the single disk resonator manufacturing resonance frequency standard deviation is known, then (2.21) computes the number of tuning resonators needed to attain perfectly tuned filter fabrication yields of 68.3%, 95.4%, and 99.7% for i equal to 1, 2, and 3, respectively. The designer can merely increase the dc-bias and/or add a column if yield requirements call for more tuning resonators. For the demonstrated filter in this work, the addition of 1V to the design-flow dc-bias to make $V_P = 17$V allows reduction of the needed I/O resonator number to 14, allowing for 2 tuning resonators while retaining 24 resonators total in a quadrant. This is still less than the 3 recommended by (2.22) for 68.3% perfect-tuned yield, but is sufficient for the demonstrated research prototype.

This quadrant design yields an R_Q of 445Ω close to the desired 450Ω. Further massaging of dc-bias and row-column choices can get even closer to this target, if needed.

From here, the dimensions of the coupling beams come readily from the indicated expressions. These then permit assembly of the fully balanced structure of Fig. 2.1, which in turn yields the complete equivalent circuit of the filter for SPICE verification shown in Fig. 2.24. Table 2.VI includes all dimensions and geometry considerations to allow for the complete layout of a filter satisfying the stated specification.

A. Filter Design Examples

To give a sense of what types of filters might be desirable in an RF front-end bank, Table 2.IV presents example designs for various 2nd order Chebyshev differential filters requiring R_Q=50Ω and with center frequencies ranging from 50MHz to 3GHz assuming 3μm-thick polysilicon structural material. The columns grouped under the 'filter specifications' section of Table 2.IV specify the filter center frequency, bandwidth, and insertion loss as design objectives. The filter design procedure summarized in Table 2.III then yields the values listed under the 'Calculated Design Variables' section of Table 2.IV that satisfy the corresponding filter specifications. All designs assume a fabrication process using 3-μm-thick polysilicon structural material and 20-nm electrode-to-resonator gaps. Here, three different values of dc-bias that increase with increasing center frequency help to maintain the needed (C_x/C_o)'s. In addition, each design assumes the minimum required single-resonator Q value indicated in the table.

Table 2.IV illustrates the one-to-one relation between example RF channel-select communication standard requirements, i.e., filter spectral masks, and the geometric dimensions of the final on-silicon filter product. The fact that lateral dimensions (instead of the thickness) specify each filter constitutes a key advantage of this design approach, since it means the whole filter bank is amenable to automatic generation by a computer-aided design (CAD) program [9]. Such a program could very quickly generate the layouts required to achieve all filter responses, making realization of a VLSI circuit of such filters as convenient as already the case for transistor IC design.

Note that several of the lower frequency designs in the table use already achievable resonator performance, as evidenced this work and by the summary of achieved (C_x/C_o) and Q combinations in Fig. 2.20 of [26]. However, this table is perhaps most useful in identifying needed resonator attributes and challenges at the higher frequencies. In particular, it predicts that application of already achieved gap spacings (e.g., from [45]) to disk resonators should allow channel-select filters at the prescribed high frequencies, as long as 12V dc-biases are permissible, and as long as the indicated Q minima are attainable. The jury is still out on polysilicon Q, but CVD diamond material readily provides the needed Q [54].

It is worth noting that some of the coupling beam widths in Table 2.IV for filters past 1.8 GHz become quite small. If too small, then one solution is to use coupling beams that are multiples of a quarter-wavelength. For example, use of 5λ/4 beams instead of λ/4 takes the needed 1.8-GHz filter coupling beam width from 208nm to 1.04μm.

Table 2.V summarizes the Fig. 2.24 equivalent circuit element values for each of the Table 2.IV filter designs. To demonstrate the utility of the equivalent circuit, Fig. 2.25 plots SPICE simulated frequency responses for three of the filters within the 50MHz to 3GHz frequency range, each properly terminated with 50Ω.

As Table 2.IV demonstrates, capacitive transduced vibrating disk filter technology can adapt to challenging channel-select filter specifications over a wide frequency range by merely adjusting numerous design knobs, such as voltage, electrode-to-resonator gap spacing, and array size. Table 2.IV makes it clear that the combination of capacitive transducer gap scaling and array-composite scaling is key to achieving RF channel-selection at 1GHz and beyond with a small area footprint. While the need for 70 resonators in each array-composite in the 3-GHz design of the last row might seem daunting, note that the total filter quadrant area can be as small as 0.00064mm^2, so a 4-

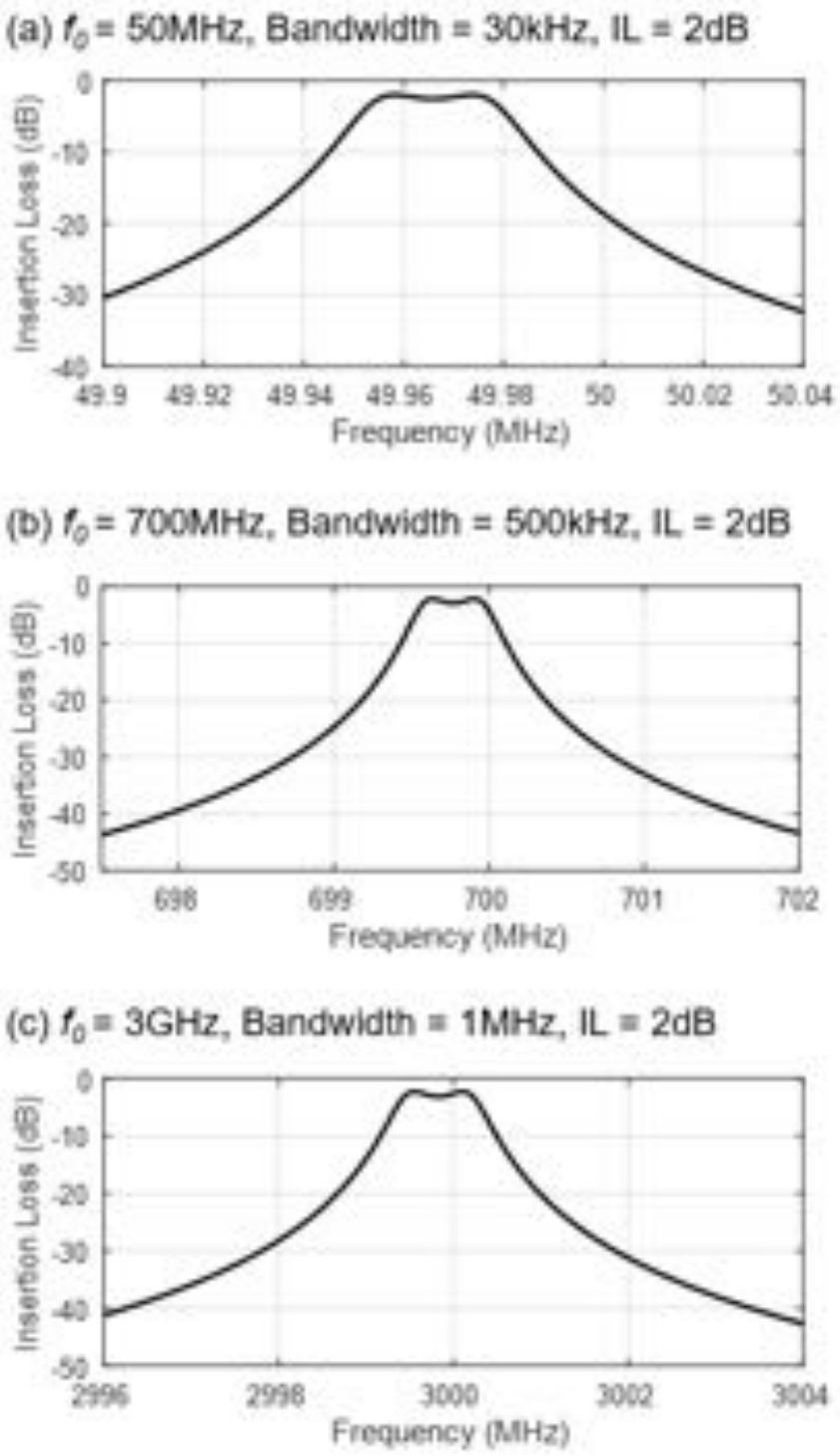


Fig. 2.25: SPICE simulated frequency responses for a 2nd order 50Ω terminated 0.5dB ripple 2dB insertion loss Chebyshev filter with (a) 30kHz bandwidth at 50MHz. (b) 500kHz bandwidth at 700MHz. (c) 1MHz bandwidth at 3GHz.

quadrant filter consumes 0.00256mm^2. Indeed, 9765 of such filters (without bond pads) could fit in a 5mm×5mm chip.

Table 2.IV: 2ND ORDER DIFFERENTIAL CHEBYSHEV POLYSILICON DISK FILTER BANK DESIGN EXAMPLE†

Filter Specifications				**Computed Quadrant Design Variables**												
f_o (MHz)	B (kHz)	PBW (%)	IL (dB)	*Min. Req. Q*	V_P (V)	C_x/C_o (%)	d_o (nm)	R_Q (Ω)	R (μm)	$l_{\lambda/4}$ (μm)	w_c (nm)	N_{tot}	N_{io}	N_t	Array Size (row x col)	Area (μm×μm)
50	30	0.060	2	15,957	5	0.372	20	46	54.2	41.4	1850	16	11	1	2×8	300×1450
100	30	0.030	2	31,915	5	0.186	20	46	27.1	20.7	463	16	11	1	2×8	150×724
250	500	0.200	2	4,787	9	0.275	20	49	10.8	8.29	4630	60	47	1	6×10	213×366
433	500	0.115	2	8,291	9	0.143	20	50	6.26	4.79	1852	72	51	3	9×8	189×167
700	500	0.071	2	13,404	9	0.089	20	50	3.87	2.96	708	72	51	5	8×9	103×117
900	500	0.056	2	17,234	9	0.071	20	48	3.01	2.30	416	70	51	5	7×10	69×102
1200	1000	0.083	2	11,489	12	0.104	20	48	2.26	1.73	435	65	52	3	5×13	36×100
1800	1000	0.056	2	17,234	12	0.067	20	48	1.51	1.15	208	70	54	2	7×10	35 x 51
2400	1000	0.042	2	22,978	12	0.050	20	48	1.13	0.86	117	70	54	2	7×10	26×38
3000	1000	0.033	2	28,723	12	0.035	20	49	0.90	0.69	75	70	52	4	7×10	21×30

† Assumes h=3μm, θ_{ov}=330º, and fundamental mode resonance.

TABLE 2.V: 2ND ORDER DIFFERENTIAL CHEBYSHEV POLYSILICON DISK FILTER BANK EQUIVALENT CIRCUITS

Filter Specifications				**Equivalent Circuit Element Values**								
f_o (MHz)	B (kHz)	PBW (%)	IL (dB)	R_Q (Ω)	C_{oA} (pF)	η_{eA} (μC/m)	r_{xA} (μΩ)	c_{xA} (nF)	l_{xA} (pH)	c_c (μF)	C_{tA} (pF)	η_{tA} (C/m)
50	30	0.060	2	46	4.56	1,140	15.30	13.049	777.27	30.10	0.414	0
100	30	0.030	2	46	2.28	567	3.82	13.049	194.32	60.20	0.207	0
250	500	0.200	2	49	3.90	1753	38.24	3.480	116.59	2.408	0.00829	0
433	500	0.115	2	50	2.44	1098	15.30	2.900	46.64	3.475	0.144	0
700	500	0.071	2	50	1.51	679	5.85	2.900	17.84	5.619	0.148	0
900	500	0.056	2	48	1.17	528	3.44	2.983	10.50	7.431	0.115	0
1200	1000	0.083	2	48	0.90	539	3.60	3.212	5.482	5.335	0.00518	0
1800	1000	0.056	2	48	0.62	373	1.72	2.983	2.624	7.431	0.00230	0
2400	1000	0.042	2	48	0.47	280	0.968	2.983	1.476	9.908	0.00173	0
3000	1000	0.033	2	49	0.35	216	0.774	2.983	0.9446	12.384	0.00276	0

Still, filters at GHz frequencies will be challenging. Fortunately, there is no need to ponder feasibility at VHF, as the demonstrated filter of this work demonstrates.

2.14. Nonidealities

Having presented a complete design procedure for filters utilizing capacitive-gap transduced micromechanical disk resonators, the rest of this chapter now turns to practical implementation issues. In particular, unlike the ideal filter covered so far, a real filter suffers non-idealities that if not circumvented can significantly compromise performance. Among the most important practical considerations for the present design are:

1) Structural film stress, especially in-plane stress that might push resonators into their substrate-anchored electrodes.
2) Parasitic trace resistance that might contribute significant insertion loss and increase input to output feedthrough.
3) Finite fabrication tolerances that introduce frequency variations, most importantly frequency mismatches between identically designed resonators.

Pursuant to elucidating, understanding, and alleviating the impact of these and other non-idealities, the rest of this chapter demonstrates an actual polysilicon surface-micromachined filter designed using the previously outlined methods. The demonstrated 223.4-MHz second order Chebyshev filter, *cf*. Fig. 2.1, employs 206 resonant micromechanical elements to realize a channel-selecting 0.1%-bandwidth while achieving only 2.7dB of in-band insertion loss together with 50dB of out-of-channel stop-band rejection [33]. This amount of rejection is 23dB better than that of previous capacitive-gap transduced channel-select filter efforts [25], and comes in tandem with a 20dB shape factor of 2.7 commensurate with its use of two array-composite resonators. Capacitive transducer gaps scaled down to 39nm and a bias voltage of 14V achieve sufficient single-resonator transducer coupling strengths of C_x/C_o = 0.1% and a low filter termination impedance of only 590Ω. As shown in Fig. 2.1, the filter comprises 96 disks mechanically coupled by 110 beams. The clearly discernable mechanically coupled resonator arrays implement a design hierarchy reminiscent of complex VLSI transistor circuits, but here used to achieve a complex MSI mechanical filter circuit [34].

The following sections begin by addressing each of the three practical considerations enumerated above and describing defensive design solutions. These include electrodeless buffer devices that alleviate post-fabrication stress to prevent undue disk-to-electrode contact in Section 2.15; thick conductive interconnect layers that greatly reduce parasitic resistance, thereby reducing insertion loss and increasing isolation, in Sections 2.16 and 2.17; and non-input/output (I/O) devices specifically tasked to provide voltage-controlled electrical stiffness frequency tuning to compensate for finite fabrication tolerances in Section 2.18.

2.15. Defensive Design Against Film Stress

The previous sections of this study emphasized the importance of small electrode-to-resonator gaps that amplify the input/output electromechanical coupling and directly contribute to large stop-band rejection. Indeed, small gaps have greatly enhanced the electromechanical coupling coefficients of the single disks of [36] and [45].

Unfortunately, going from a single resonator to an ensemble of mechanically linked ones introduces a yield loss mechanism that intensifies as gaps become smaller. In particular, differences in substrate and structural material thermal expansion coefficients generate strains when the temper-

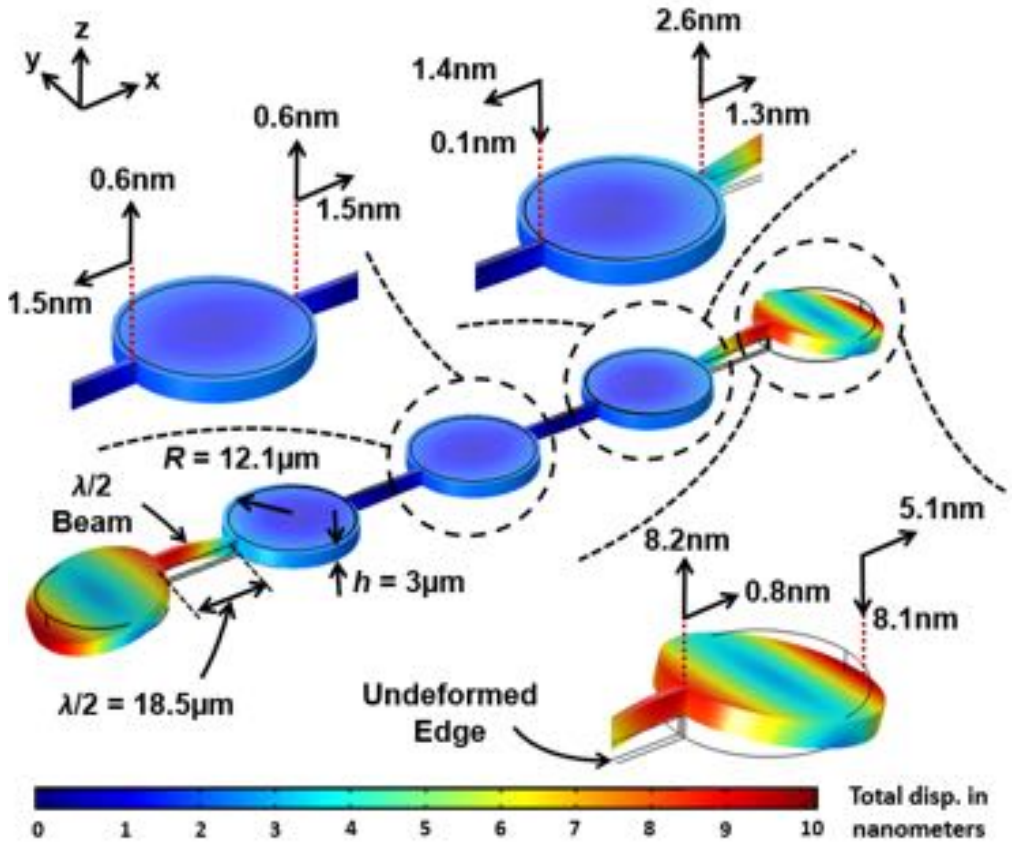


Fig. 2.26: Finite element stationary analysis result for a 1×5 polysilicon disk resonator array-composite under 50 MPa compressive stress. Each disk is substrate-anchored at the center by a stem post 2μm in diameter and connected to the adjacent disk with λ/2 long beams. The color-map legend indicates displacement in nanometers.

ature drops from the structural material deposition temperature to room temperature that effectively move certain resonators in the network relative to their electrodes. If strains are large enough, resonators can actually push into their electrodes, shorting the two in a way that would debilitate the whole filter. Clearly, the problem becomes worse as electrode-to-resonator gap spacing shrinks.

Fig. 2.26 illustrates the problem for the case of a linear array of five identical 224-MHz polysilicon contour mode disk resonators, each 3μm-thick with 12.1μm-radius, all coupled via half-wavelength extensional-mode beams. 2μm-diameter center stem anchors suspend each disk 0.5μm above the substrate. Here, a stationary finite element analysis (FEA) reveals that the strain in a string of half-wavelength coupled disks under the typical (for polysilicon over silicon) 50MPa of in-plane compressive stress translates to the end disks, leaving the inner disks relatively strain free. For the specific case of Fig. 2.26, the outer edges of the end disks move 5.1 nm along the string axis, which is 2× larger than the maximum 2.6 nm experienced by the inner disks. This is fortuitous, indeed, and suggests that gap-closing strains alleviate by merely employing electrodeless buffer disks at the ends of any string of coupled disks that absorb most of the strain, allowing the inner disks to sport electrodes spaced very close to them with reasonable resilience against stress.

To further quantify the permissible set of array lengths as a function of residual stress, Fig. 2.27 plots the maximum displacement experienced by each disk in the Fig. 2.26 5-disk linear array

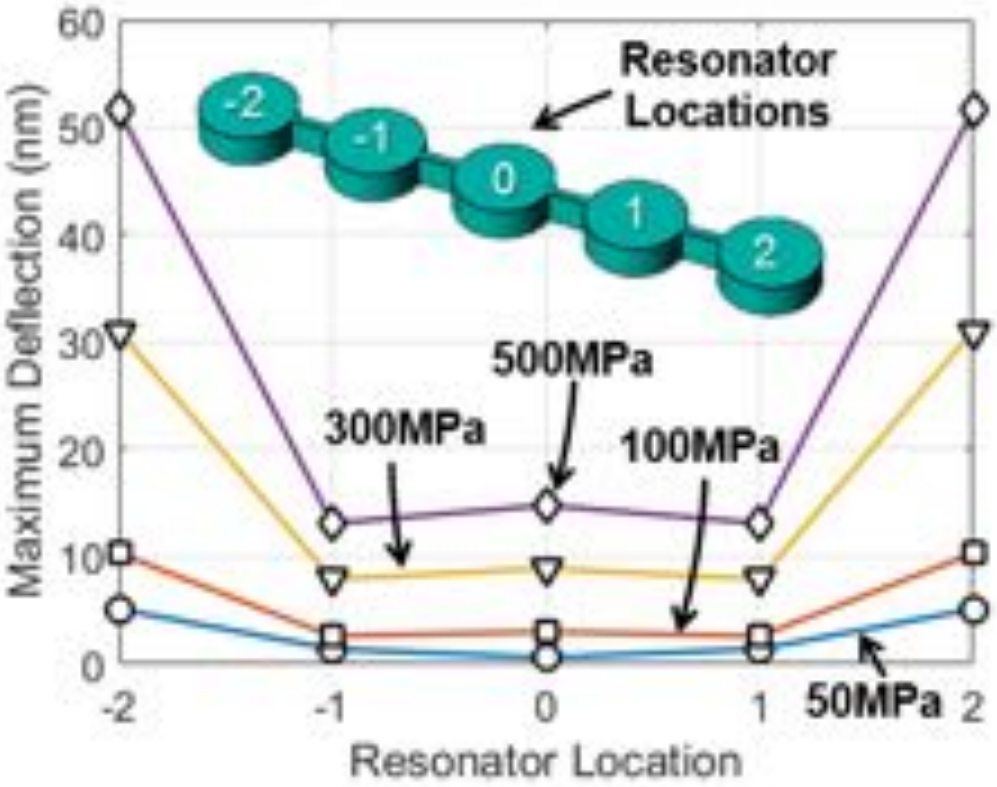


Fig. 2.27: Plot of FEA static analysis results for maximum static displacement under four different structural film stress scenarios for the structure of Fig. 2.26.

under four different residual stress conditions, with some much larger than normal. The plot more clearly illustrates how the inner disks experience very similar displacements that gradually increase with stress, while displacements at the end disk increase much more abruptly with increasing stress. An important takeaway from Fig. 2.27 is that a 5-disk linear array (such as used in the demonstrated filter) cannot safely support 40nm electrode-to-disk gaps if post fabrication residual stress values rise above 1.5GPa. Interestingly, according to FEA simulation, the use of just two buffer devices as in Fig. 2.27 is just as effective for much larger arrays, as well. For example, a 9-disk array with two buffer devices incurs less than 1-nm increase in inner disk movement over a 5-disk one.

The area penalty incurred when employing stress-relieving electrodeless buffer disks at the boundaries of each of the four arrays is clear from Fig. 2.1, where the penalty amounts to a 50% increase in disk footprint over the electroded 4×4 array. The penalty for doing this manifests in not only area, but also electromechanical coupling, which reduces from the 0.128% it would have been without the buffer disks, to 0.074% with the buffer disks, as predicted by (2.54) for the filter design presented in Table 2.I. As will be seen in Section 2.21, these encumbrances are well worth the yield enhancement afforded via these buffer disks.

2.16. Impact of Parasites

As with any micro-scale on-chip device, parasitic resistance and capacitance can impact the performance of a micromechanical filter, and their influence increases as frequency increases. Of

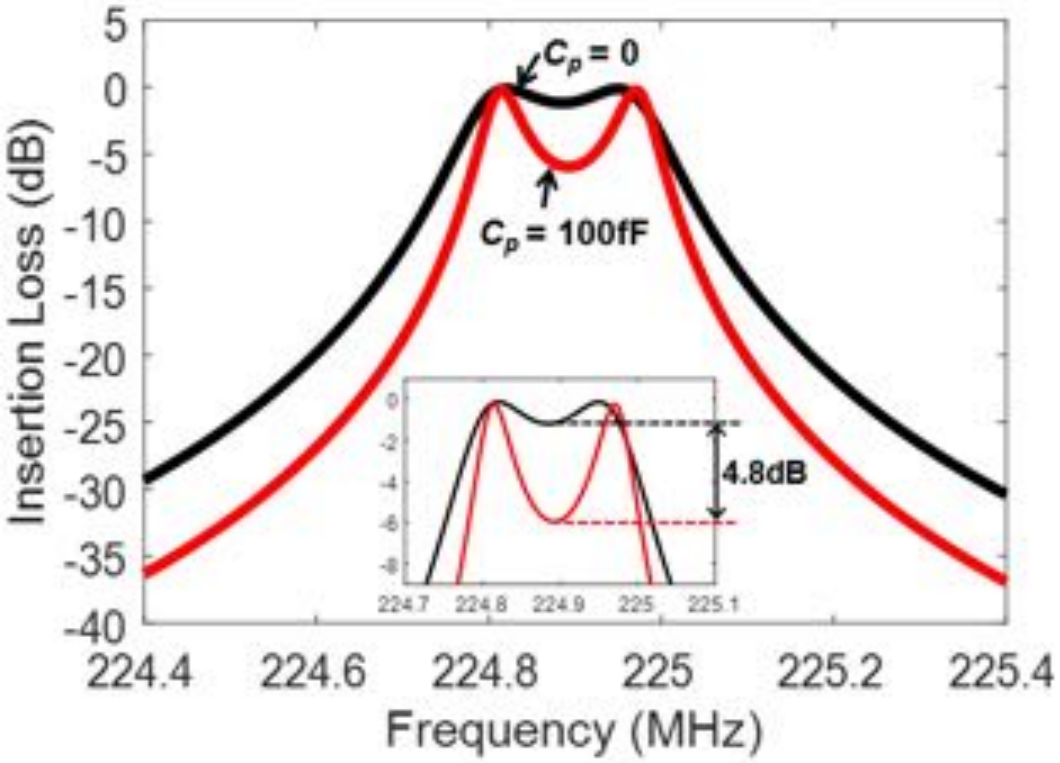


Fig. 2.28: Simulated frequency response spectra for a 225-MHz two-pole, i.e. two-resonator, 0.5dB-ripple, Chebyshev filter with 0.1% bandwidth, for small and large values of pad capacitance.

the two, resistance is perhaps the most controllable, which is fortunate, since resistance can often serve as an effective knob with which to control capacitive parasites.

The capacitive parasites that most impact filter performance are shunt capacitance at the input and output terminals; and feedthrough capacitors that offer an alternative signal path for input signals thereby competing with the filter path.

A. Shunt Parasitic Capacitance

Previous sections described the importance of electromechanical coupling (C_x/C_o) to avoid passband distortion, where (C_x/C_o) should be greater than the intended percent bandwidth by a factor governed by the filter order, which in turn depends upon the number of resonators used. Note that (2.53) for (C_x/C_o) accounts for only the intrinsic electrode-to-resonator overlap C_o and not any parasitic capacitance. If additional capacitance C_p from parasitic sources adds to the intrinsic value, the value of (C_x/C_o) changes by the factor

$$\left(\frac{C_x}{C_o}\right)_{eff} = \frac{1}{1 + C_p/C_o}\left(\frac{C_x}{C_o}\right) \tag{2.65}$$

which could entail a significant reduction if C_o is small compared with C_p. For example, the 12.1μm-radius disks used in the prototype of this work have shunt C_o's of 47.4fF. If a single resonator were used as an input device, biased as in Table 2.I, then an 80μm × 80μm bond pad that alone adds 97.7fF of shunt capacitance through the 500nm nitride and 2μm oxide layers would

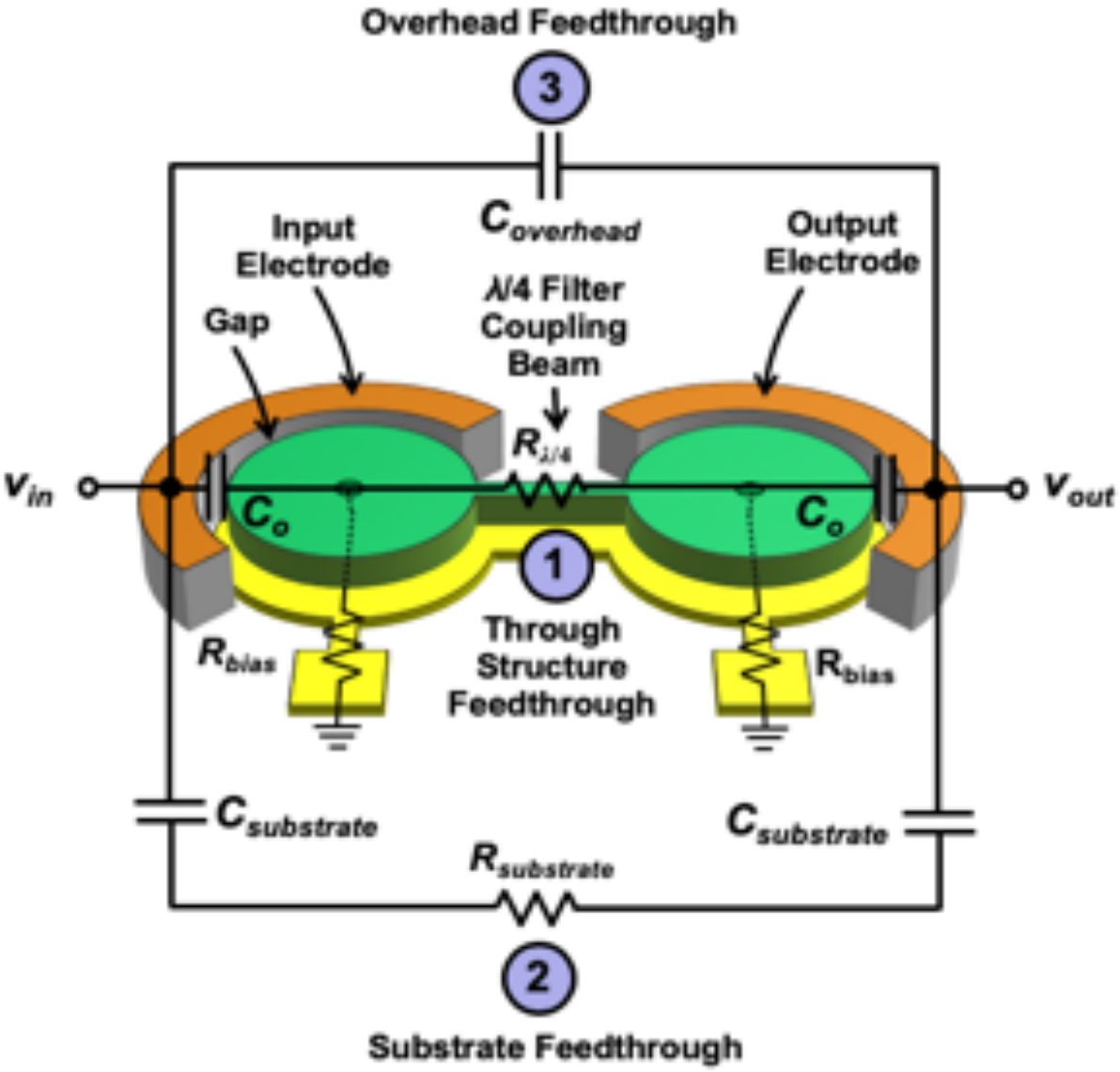


Fig. 2.29: Schematic description of dominant electrical feedthrough paths in a simple two-resonator filter.

reduce (C_x/C_o) by 3×, from 0.1% to 0.034%. Fig. 2.28 illustrates via simulation the 4.8dB of additional passband distortion imposed by this bond pad capacitance. This much distortion is generally not acceptable.

One method to obviate shunt capacitance, whether parasitic or intrinsic, is to resonate it out via an inductor. The obvious issue here is the need for an inductor, which whether on or off chip, incurs undesirable cost increase. Still, this solution makes good sense if that one inductor can resonate the shunt capacitance of many filters all at once, such as would be possible for an RF channel-selecting bank of filters [55]. If only one filter, however, the use of an inductor to resonate out shunt capacitance is not cost effective.

Equation (2.65) suggests that an alternative solution that avoids the need for an inductor is simply to increase the intrinsic C_o of the resonator relative to C_p. Perhaps the most effective way

to do this is to decrease the electrode-to-resonator gap spacing, since this raises C_x faster than C_o, raising the overall (C_x/C_o) while increasing immunity against C_p.

If reducing gap spacing is not an option, however, then the next best solution is as shown in Fig. 2.1, where the use of disk array-composites increases the intrinsic C_o and the C_x at the same rate, keeping (C_x/C_o) constant, while attenuating the effect of C_p via (2.65). In the specific prototype demonstrated here, ignoring for now the effect of buffer disks, the use of 16 I/O disks in each quadrant array generates 800fF of intrinsic C_o, which now limits the reduction in (C_x/C_o) to only 1.1×, yielding a $(C_x/C_o)_{eff}$ of 0.089%.

Finally, another reasonable strategy to reduce C_p is to float the substrate, which would work best if the substrate were non-conductive. The prototype filter demonstrated here actually takes this approach, i.e., does not ground the substrate, but its substrate is not un-doped, but rather lightly-doped with a resistivity of 8-12Ω-cm. Although this does reduce shunt capacitance, it also introduces additional feedthrough, which can both distort the passband and reduce the stopband rejection.

B. Feedthrough Parasites

Fig. 2.29 depicts the parasitic resistors and capacitors that most impact the performance of a simple two-resonator filter. These include:

1) the physical resistors R_{bias} from the actual dc-bias voltage supply to the disk-to-electrode interfaces;
2) the resistance $R_{\lambda/4}$ between the disks, mainly through the coupling beam;
3) the electrode-to-resonator overlap capacitors, C_o; and
4) the feedthrough path from input electrode to output electrode, which comprises the series combination of substrate capacitors C_{sub}'s, plus series resistance, as well as direct overhead capacitance C_f between the electrodes.

Of particular concern are parasitic elements that permit electrical feedthrough of signals from input to output that effectively bypass the filter transfer function. Here, electrical feedthrough can generate significant passband distortion and reduce out-of-band rejection, thereby compromising the filter's ability to eliminate out-of-channel blockers.

Of the paths available for feedthrough in Fig. 2.29, three stand out as most troublesome:

1) Through-Structure Feedthrough (Path 1) starting at the input electrode, going through the input electrode-to-disk capacitor, through the structure resistance (dominated by the coupling beam's $R_{\lambda/4}$), and finally through the disk-to-output electrode overlap capacitor to the output electrode.

2) Through-Substrate External Feedthrough (Path 2) going through the input electrode-to-substrate capacitor, through the substrate resistance, and finally out the substrate-to-output electrode capacitor to the output electrode. Note that in a practical research design that allows interrogation via probe, or in a situation where MEMS and other function dies connect via wire-bonds, bond pads can greatly increase the electrode-to-substrate capacitance.

3) Overhead External Feedthrough (Path 3) going from input to output through direct parasitic feedthrough capacitance, perhaps going over the structure itself. This component can be particularly important in situations where probe station probe tips or bond wires access the filter.

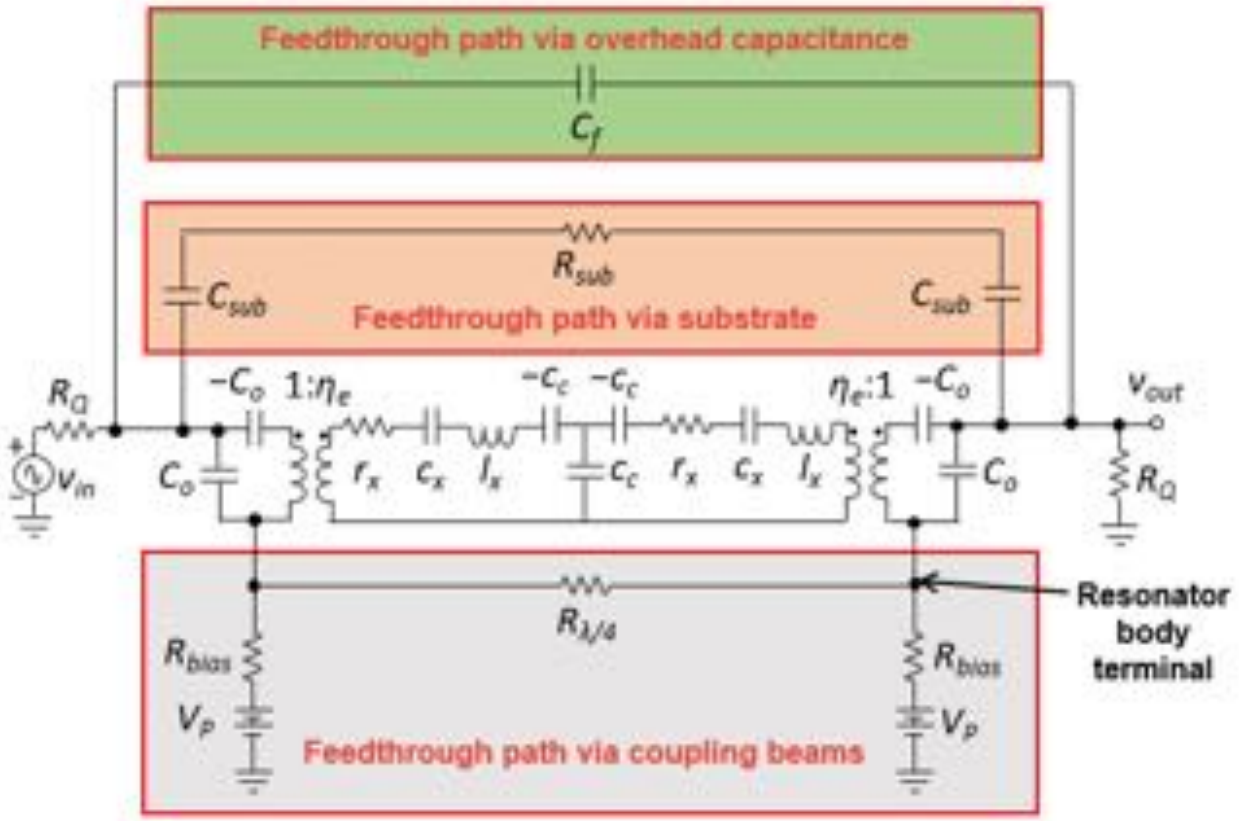


Fig. 2.30: Circuits for the parasitic paths Fig. 2.29 hooked around the circuit for a properly terminated two-resonator filter with input source v_{in} and output v_{out}.

Insight on methods to suppress these feedthrough paths follows most readily from inspection and simulation of the equivalent circuit modeling the filter and its parasitic elements.

2.17. Filter Electrical Equivalent Circuit with Parasitic Elements

Of course, the entire filter is more complex than the simple two-resonator illustration of Fig. 2.29, as it contains arrays of disks and a fully differential structure. Unfortunately, complexity like this can hide significant insight. In the interest of gleaning maximum insight, it is instructive to tackle first the much simpler equivalent circuit of the two-resonator filter in Fig. 2.29.

A. Case: Single-Ended Filter

Pursuant to this, Fig. 2.30 inserts the simple parasitic path circuit of Fig. 2.29 into a properly terminated drive and sense circuit with input source v_{in} and output v_{out}. From this circuit, depending on the values of internal parasitic resistors R_{bias} and $R_{\lambda/4}$, the amount of source signal v_{in} traversing the feedthrough path and appearing at the output becomes a strong function of the value of R_Q.

i. Suppressing Series External Feedthrough (Paths 2 and 3)

Simple inspection of the Fig. 2.30 circuit reveals that the purely series feedthrough paths, i.e., paths 2 and 3, experience greater attenuation with smaller values of R_Q. In particular, the transfer function for the overhead feedthrough path from v_{in} to v_{out} takes the form

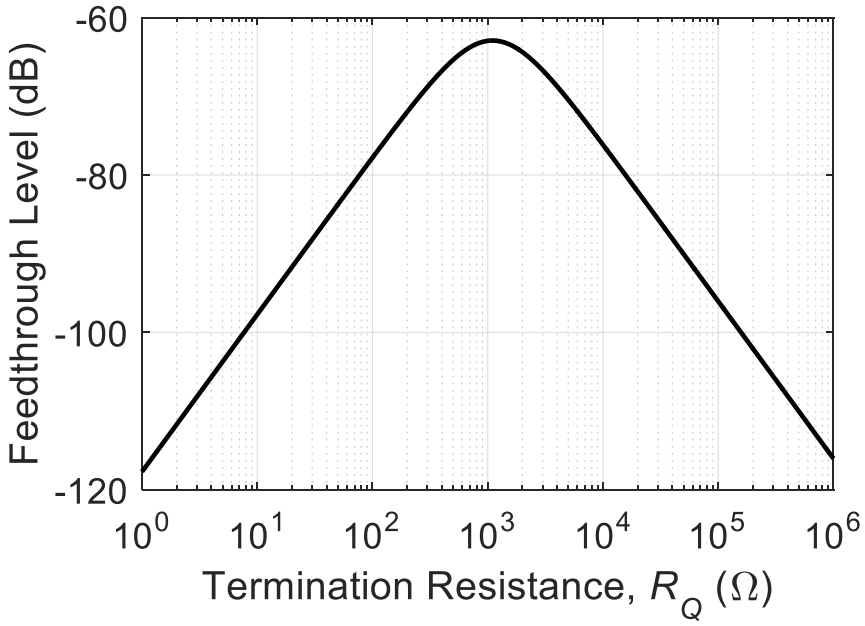


Fig. 2.31: Through structure feedthrough at 223 MHz versus the value of R_Q for typical values of structural parasitic elements: R_{bias} = 5.85Ω, $R_{\lambda/4}$ = 10Ω, and C_o = 648fF (for a disk array).

$$\frac{v_{out}}{v_{in}} = \frac{j\omega R_Q C_f}{1 + j2\omega R_Q C_f} \tag{2.66}$$

Here, reducing R_Q from 5kΩ to 50Ω would decrease the feedthrough level by 39.9dB at 223MHz for a C_f value of 10fF.

For the through substrate feedthrough path, the expression relating the voltage seen at v_{out} to that at v_{in} takes the form

$$\frac{v_{out}}{v_{in}} = \frac{j\omega R_Q C_{sub}}{2 + j\omega(2R_Q + R_{sub})C_{sub}} \tag{2.67}$$

Again, a need to reduce R_Q manifests, where reducing R_Q from 5kΩ to 50Ω would decrease the feedthrough level by 33.12dB at 223MHz for typical C_{sub} and R_{sub} values of 530.5fF and 374.98Ω, respectively.

Beyond this, consideration of the external feedthrough path 2 suggests that the magnitude of unwanted current in an asymmetric structure is best suppressed by shrinking bond pads and increasing the isolation dielectric layer thickness (*cf.* Fig. 2.37) to reduce capacitance from the I/O ports to the substrate; and by raising the substrate resistance, perhaps by using an undoped silicon substrate.

ii. Suppressing Through-Structure Feedthrough (Path 1)

In Fig. 2.30 signals feeding through the structure itself first proceed through the input capacitance, then through a resistive voltage divider comprised of the R_Q, R_{bias}, and $R_{\lambda/4}$ resistors. The element values of the resistors in this voltage divider largely determine how much signal shunts to ac ground (realized by dc-bias sources) and how much makes it to the output. Assuming R_Q is much larger than R_{bias} and $R_{\lambda/4}$, the expression relating the voltage seen at v_{out} to that at v_{in} is

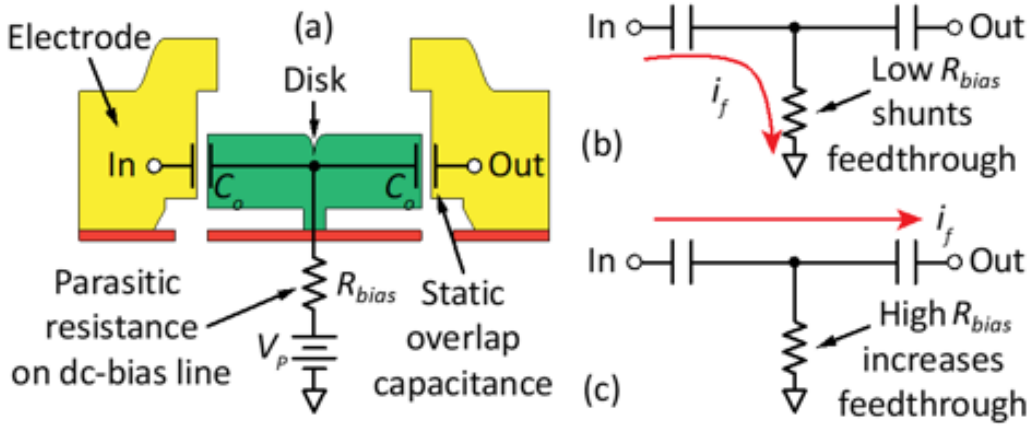


Fig. 2.32: (a) Schematic describing the current divider formed by dc-bias trace parasitic resistance and static electrode-disk overlap capacitors, where (b) very low trace resistance creates a sink for parasitic feedthrough current i_f and increases filter rejection as desired. In contrast, (c) high trace resistance cannot effectively shunt electrical feedthrough, allowing it to leak to the output.

$$\frac{v_{out}}{v_{in}} \approx \left\{ \frac{j\omega R_{bias} C_o}{1 + j\omega R_Q C_o} \frac{1 + \frac{R_{\lambda/4}}{R_{bias}}}{2 + \frac{R_{\lambda/4}}{R_{bias}}} \right\} \left\{ \frac{1}{1 + \frac{R_{\lambda/4}}{R_{bias}}} \right\} \left\{ \frac{j\omega R_Q C_o}{1 + j\omega R_Q C_o} \right\} \tag{2.68}$$

Equation (2.68) reveals that for cases where through-structure feedthrough dominates over external paths, there is a worst case value of R_Q where the transfer function of (2.68) peaks (which of course is bad). Fig. 2.31 plots (2.68) at 223 MHz versus the value of R_Q for typical values of structural parasitic elements: R_{bias} = 5.85Ω, $R_{\lambda/4}$ = 10Ω, and C_o = 648fF (for the demonstrated disk array). Here, the worst case value of R_Q is 1,101Ω at which the feedthrough level peaks to −62.9 dB at 223 MHz. From the plot, when through-structure feedthrough dominates over other paths, it is best to pick either small or large values of R_Q. This is fortuitous given that most practical IF and RF applications prefer impedances on the smaller side, in the 50- to 500- Ω range.

Equation (2.68) further suggests that feedthrough plummets when interconnect resistance, e.g, R_{bias}, is minimized while structure resistance, e.g., $R_{\lambda/4}$, is maximized. As shown in Fig. 2.32(b), the R_{bias} resistors associated with dc-bias interconnects effectively shunt to ground currents that would otherwise feedthrough to the output. The smaller the value of R_{bias}, the larger the amount of current that takes the path towards the dc-bias pads, and the less parasitic current that reaches the output. In contrast, a high R_{bias} resistance between the dc-bias source and the disk resonator effectively repels current, directing it towards the output port instead of the dc-bias sink, *cf.* Fig. 2.32(c), where it can mask the desired motional current of the device and limit the ultimate filter stopband rejection. This justifies the added fabrication process complexity to achieve 3μm-thick phosphorus doped polysilicon interconnect traces in this study, which are considerably thicker than the 300nm of [25], so much more conductive. The 3μm-thick interconnect of this work provides a sheet resistance on the order of 0.8Ω/□, which is considerably smaller than the 21.3Ω/□ of previous 300nm-thick traces. As will be seen, this greatly improves the stopband rejection of the demonstrated filter.

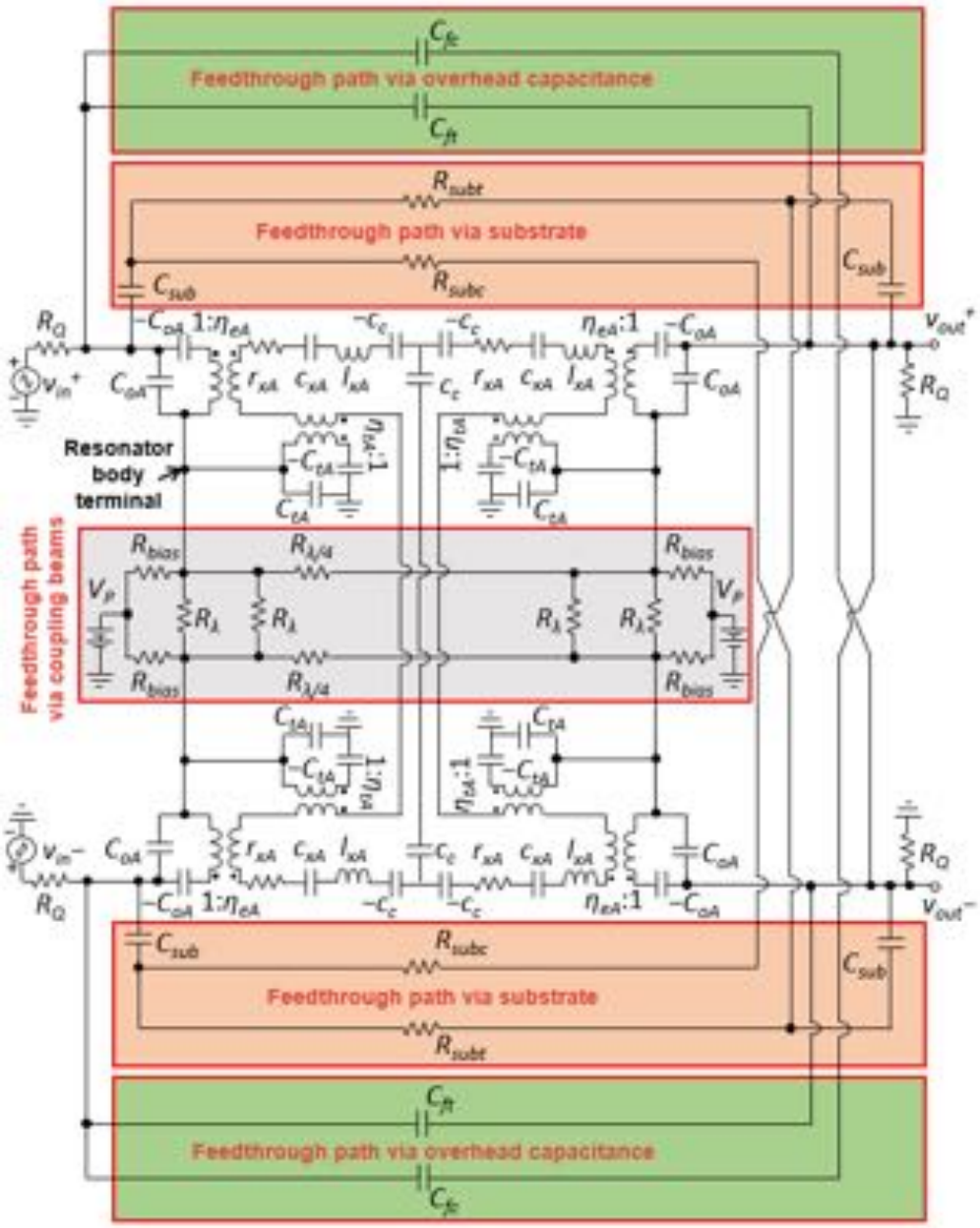


Fig. 2.33: Electrical equivalent circuit for a 2nd order differential micromechanical disk filter. This circuit improves upon the version presented in Fig. 2.24(b) by introducing parasitic electrical feedthrough models as marked in the highlighted rectangular areas. Here, the three dominant feedthrough paths comprise feedthrough via coupling beams, via the substrate parasitic capacitances, and via overhead capacitance. The "t" and "c" added to certain feedthrough element subscripts stand for "through" and "cross", respectively.

Low parasitic trace resistance not only minimizes parasitic feedthrough, but also minimizes parasitic Q loading of constituent resonators by resistive traces, thereby reducing insertion loss. Low interconnect resistance becomes especially important as electrode-to-resonator gaps shrink to yield correspondingly small resonator motional resistances that are more easily loaded by the interconnect resistance. Disks operating in radial contour modes further derive more benefit than

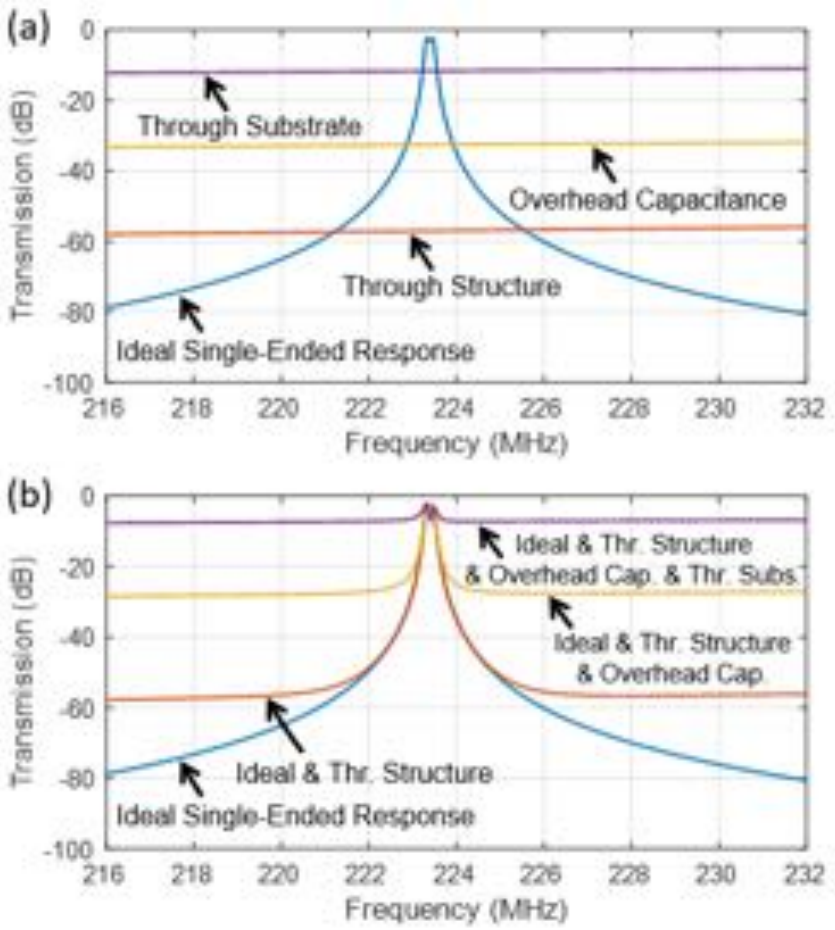


Fig. 2.34: Single-ended filter response alongside various feedthrough components. (a) Ideal single-ended filter response with individual parasitic feedthrough components. (b) Full filter responses as a function of the different feedthrough mechanisms.

wine-glass counterparts from reduced parasitic trace resistances, since the resonant motional currents to resistive loading from dc-bias lines, as well as from input/output lines, both of which degrade the resonator *Q*, with detrimental impact to filter insertion loss.

As mentioned, raising the structure resistance also reduces parasitic current feeding through the structure. In fact, making the coupling beams non-conductive, as done in [56], would greatly suppress parasitic feedthrough. The benefits of doing this, however, need to outweigh its added process complexity.

B. Case: Balanced Differential Filter

Interestingly, the parasitic feedthrough that plagues the single-ended filter example of the previous sub-section attenuates dramatically when the filter takes on a balanced topology with differential input/output, as in Fig. 2.1. Here, balanced differential operation generates largely offsetting feedthrough currents at each output node that result in orders of magnitude reduction in feedthrough versus the single-ended case.

The degree of improvement is very clear upon simulation of the equivalent circuit for the entire filter. To this end, Fig. 2.33 modifies the equivalent circuit of Fig. 2.24(b) to explicitly include the

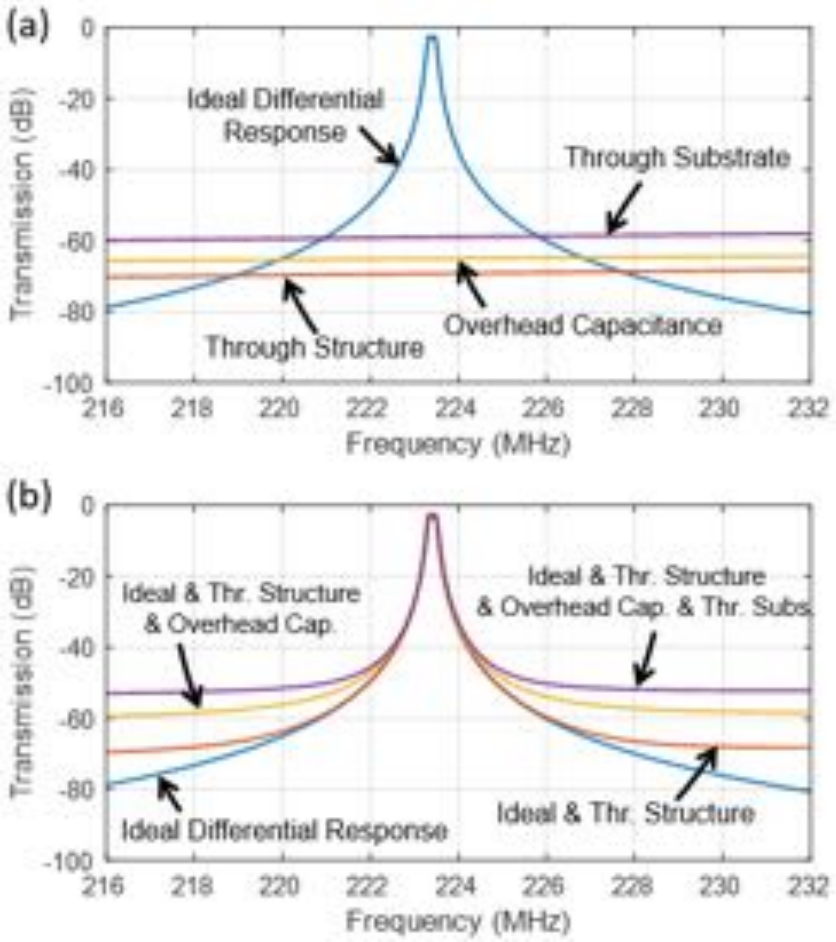


Fig. 2.35: Differential filter response alongside various feedthrough components. (a) Ideal differential filter response with individual parasitic feedthrough components. (b) Full filter responses as a function of different feedthrough mechanisms, showing superior performance relative to the single-ended case of Fig. 2.34(b).

most problematic parasitic paths, shown boxed in the figure. Here, resistors $R_{\lambda/4}$ model the resistance across each of the quarter-wavelength coupling beams connecting left and right disk array-composites in the top and bottom halves of the hierarchical structure. Meanwhile, resistors R_{λ} model resistive paths across the full-wavelength beams coupling top and bottom array-composites. Finally, resistors R_{bias} model the equivalent interconnect resistance from the stems to the bias bond pads of the combined resonators in each of the four half-wavelength-coupled array-composites.

Due to their complex structure, parasitic contributions from the disk array-composites are distributed in nature, so are most correctly modeled via circuit networks that mimic the interconnection of all resistors and capacitors in their structures. Doing so reveals that use of a 3μm-thick doped polysilicon structure together with 3μm-thick doped polysilicon interconnect, such as demonstrated here, yields total parasitic resistance contributions from each array-composite that are negligible compared with the resistance of the $\lambda/4$ and λ beams that couple them. To unclutter the visual circuit, the model of Fig. 2.33 ignores the distributed parasitic resistance of the disk array-composites and condenses their equivalent circuits to that used for single resonators, but with element values augmented by the number of resonators used per the theory introduced previously.

The efficacy by which balanced differential operation suppresses feedthrough is perhaps best gauged by comparison with the single-ended case. To this end, Fig. 2.34 uses the top half of the Fig. 2.33 circuit to simulate the resulting single-ended filter response alongside the various feedthrough components described in the last sub-section. Fig. 2.34(a) specifically compares the ideal single-ended filter response with individual parasitic feedthrough components, while Fig. 2.34(b) plots full filter responses as a function of the different feedthrough mechanisms. The plot in Fig. 2.34(b) for the case where all feedthrough paths are present post a rather meager stopband rejection of only -7.5dB.

For comparison, Fig. 2.35 presents similar simulations, but for the entire balanced differential filter circuit of Fig. 2.33, applying a differential input and taking a differential output. The difference is night and day, where cancellation of parasitic feedthrough now permits a stopband rejection of -52.2dB, which is 44.7dB better than the single-ended case.

Clearly, the degree to which the Fig. 2.33 filter structure is truly symmetric dictates the achievable stopband rejection. Ultimately, despite layout symmetry, practical fabrication mismatch limits the degree of symmetry attainable. With stopband rejection as the gauge, Section 2.21 will show that the fabrication process herein, together with voltage-controlled frequency tuning, allows for excellent symmetry.

2.18. Electrical Stiffness Tuning of Frequency Mismatches

Small percent bandwidth filters present challenges in not only insertion loss, but also yield and repeatability. Indeed, the smaller the percent bandwidth, the smaller the allowable mismatch between resonators. For example, as illustrated by the simulations of Fig. 2.36, 0.1% bandwidth requires resonator-to-resonator frequency matching better than 50ppm to limit mismatch-derived pass-band ripple to less than 0.5dB over the designed 0.5dB. So far, single disk resonators (such as used in the arrays of this work) post frequency standard deviations on the order of $\sigma_{f,Single}$ = 316ppm [57], which is clearly short of the requirement. For this reason, only a small number of the mechanical filters fabricated in [25] actually exhibited acceptable passband distortion. Yields of course must be much higher for high volume production.

Reference [57] showed that mechanically-coupled array-composites of resonators attain better matching than any one of their constituents by a factor equal to $\sqrt{N_{tot}}$, where N_{tot} is the total number of resonators in the array. Thus, the 48 resonators (including non-I/O ones) used in each differential array-composite pair of Fig. 2.1 should improve the 316ppm standard deviation by 6.9× to 45.7ppm. This means that about 73% of fabricated filters using the design of Fig. 2.1 should exhibit acceptable passband distortion (defined here as < 0.5dB), with no need for tuning. However, for the more desirable 95% yield, the standard deviation would need to be about 25ppm.

Ultimately, achieving 95% of 0.1% channel-select filters with less than 0.5dB passband distortion requires tuning. The filter of Fig. 2.1 achieves this by dedicating some of the resonators in each of its mechanically-coupled arrays exclusively for frequency tuning via voltage-controlled electrical stiffness [38]. In this approach, application of a voltage across an electrode-to-resonator gap generates an electric field that varies as gap spacing changes, i.e., as the resonator displaces, in turn, causing the electric force between electrode and resonator to vary in-phase with the change in gap spacing. Any force proportional to and in phase with displacement is, of course, a stiffness, in this case taking the form

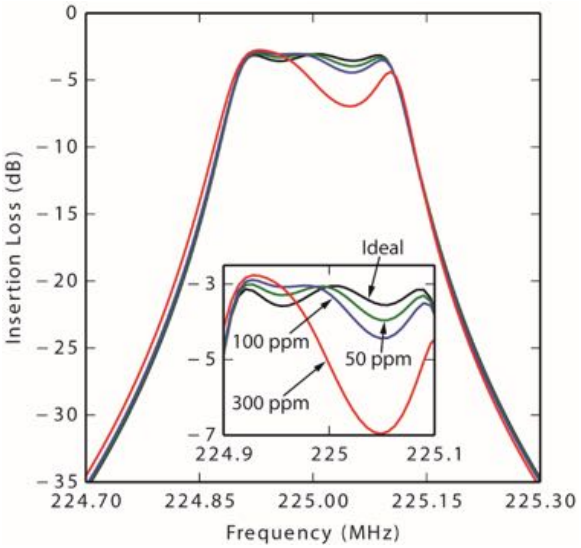


Fig. 2.36: Simulated frequency response spectra for a 225-MHz three-pole, i.e. three-resonator, 0.5dB-ripple, Chebyshev filter with 0.1% bandwidth, for different amounts of resonator-to-resonator mismatching. For each mismatch case, adjacent resonators experience the indicated frequency deviation in opposite directions to simulate the worst-case mismatch scenario.

$$k_{ej} = \frac{\eta_{ej}^2}{C_{oj}} = \frac{V_{Pj}^2 \left(\frac{\partial C}{\partial x}\right)_j^2}{C_{oj}} = \frac{\varepsilon_o A_{oj} V_{Pj}^2}{d_{oj}^3} \tag{2.69}$$

where k_{ej} is the electrical stiffness generated at port j, and η_{ej}, C_{oj}, A_{oj}, $V_{Pj} = V_P - V_j$, and d_{oj} are the electromechanical coupling factor, overlap capacitance, overlap area, voltage drop, and spacing, respectively, across the electrode-to-resonator gap of that port.

Although in the demonstrated design of Fig. 2.1 only 4 resonators out of the 48 in each differential array-composite possess tuning electrodes, any resonator with a voltage across its electrode-to-resonator gap contributes to the total effective electrical stiffness. This includes the 28 I/O resonators in each differential array-composite. Taking this into consideration, the total frequency-pulling strength of the electrical stiffness imposed on the i^{th} differential array-composite of Fig. 2.1 using identical disks and electrodes takes the form

$$\omega_{oi} = \sqrt{\frac{N_{tot}k_m - k_{e1} - k_{e2} - \cdots - k_{ej}}{N_{tot}m_m}} = \omega_{oim}\sqrt{1 - \frac{\sum_{j=0}^{Ne} k_{ej}}{N_{tot}k_m}} \tag{2.70}$$

where ω_{oi} is the radian resonance frequency of the i^{th} differential array-composite including electrical effects; N_{tot} is the total number of disk resonators in the differential array-composite; N_e is the total number of electrode-equipped resonators; k_m and m_m are the purely mechanical stiffness and mass, respectively, of each single disk in the array, and ω_{oim} is the purely mechanical radian resonance frequency, i.e., with no voltages applied, given by

$$\omega_{oim} = \sqrt{\frac{N_{tot}k_m}{N_{tot}m_m}} = \sqrt{\frac{k_m}{m_m}} \tag{2.71}$$

Again, only a subset of the electrodes serve as frequency tuners; the rest connect to the input/output ports. Assuming an applied voltage scheme as in Fig. 2.1, where the movable structure holds a voltage V_P, all I/O electrodes are at dc ground, and all tuning electrodes at V_t, and further assuming that all disks and electrodes are identical (so dropping the *j* subscripts), whether they be I/O or tuning, (2.70) becomes

$$\omega_{oi} = \omega_{oim}\sqrt{1 - \frac{N_{io}V_P^2\left(\frac{\partial C}{\partial x}\right)^2}{N_{tot}k_m C_o} - \frac{N_t(V_P - V_t)^2\left(\frac{\partial C}{\partial x}\right)^2}{N_{tot}k_m C_o}} = \\ = \omega_{oim}\sqrt{1 - \frac{N_e}{N_{tot}}\frac{\varepsilon_o A_o}{d_o^3 k_m}V_P^2 - \frac{N_t}{N_{tot}}\frac{\varepsilon_o A_o}{d_o^3 k_m}V_t(V_t - 2V_P)} \tag{2.72}$$

where N_{io} is the number of I/O electrodes, and N_t is the number of tuning electrodes. To better isolate the influence of the tuning voltage V_t, it is often useful to define a nominal resonance frequency equal to the frequency of a differential array without the influence of tuning electrodes. For the case of Fig. 2.1, where without V_t's all electrode-to-resonator gaps sustain V_P, the nominal resonance frequency of array-composite *i* is

$$\omega_{oinom} \approx \omega_{oim}\left(1 - \frac{N_e}{N_{tot}}\frac{\varepsilon_o A_o}{2d_o^3 k_m}V_P^2\right) \tag{2.73}$$

which holds when the electrical stiffness due to V_P is much smaller than the pure mechanical stiffness of the array $N_{tot}k_m$. The tuned resonance frequency then takes the form

$$\omega_{oi} \approx \omega_{oinom}\left\{1 - \frac{N_t}{N_{tot}}\frac{\varepsilon_o A_o}{2d_o^3 k_m}V_t(V_t - 2V_P)\right\} \tag{2.74}$$

which again holds when the amount of frequency tuning is very small, e.g., less than 1%, which will be the case, here. From (2.74), provided $V_t > 0$, a positive $V_t - 2V_P$ reduces the array-composite frequency from ω_{oinom}, while a negative one raises its frequency. In other words, the bias and tuning scheme of Fig. 2.1 provides both upward and downward tuning.

In addition to standard deviation advantages already mentioned, the use of disk array-composites provides a flexibility in electrode usage not available with single resonators. In particular, the ability to dedicate some disks for tuning and others for I/O effectively allows frequency tuning without simultaneously affecting I/O transducer efficiency, i.e., without affecting device impedance. This decoupling of tuning and I/O impedance is an important advantage that allows translation of a bandpass filter's center frequency while maintaining a constant bandwidth—something not easily achievable by the majority of tunable *LC* and piezoelectric resonator filters that employ varactors for tuning [58] [59].

The main drawback to separation of tuning and I/O resonators is the compromise in transducer strength. Specifically, the impact of converting an I/O resonator to a tuning one is not just the loss of an I/O electrode, but also the addition of the stiffness of a non-I/O resonator to the total array-composite stiffness, which then further degrades the electromechanical coupling (C_x/C_o). When also factoring in the need for stress buffering devices, the $(C_x/C_o)_{prac}$ of a practical array-composite

equipped with buffer and tuning reduces from that of an ideal array (where all resonators participate in I/O) by the factor

$$\frac{(C_x/C_o)_{prac}}{(C_x/C_o)_{ideal}} = \frac{N_{io}}{N_{io} + N_b + N_t} \tag{2.75}$$

where N_b is the number of buffer resonators used. Clearly, to retain maximum electromechanical coupling, one should limit the number of tuning electrodes to as few as needed to overcome the absolute and mismatch frequency tolerances of the prescribed manufacturing process.

To this end, the normalized frequency excursion Δf provided by reasonably sized tuning voltages is important. The expression for this follows readily from algebraic manipulation of (2.73) and takes the form

$$\Delta f = \frac{\omega_{oinom} - \omega_{oi}}{\omega_{oinom}} \approx \frac{N_t}{N_{tot}} \frac{\varepsilon_o A_o}{2 d_o^3 k_m} V_t (V_t - 2V_P) \tag{2.76}$$

To ensure sufficient tuning range to correct for worst-case fabrication mismatch scenarios, a filter designer should choose variables in Table 2.VI to satisfy

$$\Delta f \geq \frac{\sigma_{single}}{\sqrt{2N_{tot}}} \tag{2.77}$$

where σ_{single} is the frequency standard deviation for single constituent resonators in the given manufacturing process, and where the $\sqrt{2N_{tot}}$ term accounts for the reduction in resonance frequency standard deviation when arraying [57].

As illustrated in Fig. 2.1, each differential array-composite in the filter demonstrated herein dedicates $N_t = 2$ of its $N_{tot} = 24$ resonators for frequency tuning and $N_b = 8$ for stress buffering. Using (2.76), this resonator utilization scheme with values from Table 2.VI yields a frequency pull of 30.2ppm for a 4V change in V_t, This is sufficient to reduce the 45.7ppm frequency standard deviation expected for a 48-resonator array-composite down to the 25ppm needed to constrain mismatch-induced ripple to less than 0.5dB over a designed 0.5dB for 95% of fabricated 0.1% bandwidth filters.

2.19. Design Parameters for the Fabricated 224 MHz, 0.1% Bandwidth Channel-Select Filter

The 'Design' columns of Table 2.VI and Table 2.VII present the result of applying the step-by-step filter design procedure and equations derived so far towards realization of a 224-MHz differential coupled disk resonator filter using the topology of Fig. 2.1 with a bandwidth B = 224kHz (i.e., 0.1%) and sub-1-kΩ termination resistors. The resulting mechanical circuit employs 96 resonators among 206 resonant elements. The design assumes fabrication via the polysilicon surface-micromachining process flow described in Section 2.20 with a minimum resolvable critical dimension of $w_{c,min}$ = 1μm. The design assumes material properties from past experience, specifically E = 158GPa, ρ = 2300kg/m^3, and σ = 0.226, for the Young's modulus, density, and Poisson ratio, respectively.

TABLE 2.VI: FILTER PHYSICAL DESIGN AND PERFORMANCE SUMMARY

	Parameter	Design Source	Design	Meas.	Adjusted / Simulated	Unit
Filter Specifications	Center Frequency, f_o	Spec.	224	223.4	223.4	MHz
	Bandwidth, B	Spec.	224	229	229	kHz
	Percent Bandwidth, P_{BW}	Spec.	0.10	0.10	0.10	%
	Insertion loss, IL	Spec.	2	2.73	2.73	dB
	Minimum Beam Width, $w_{c,min}$	Process	1	1	1	μm
	Out-of-Band Rejection @ Δf = 5MHz	Fig. 2.35	69.6	50.2	49.7	dB
	Filter Termination Resistance, R_Q	(2.23)	445	590	**637**	Ω
Filter Design & Material Constants	Normalized q_0	Spec.	10	-	9.0513	-
	Normalized q_n	Spec.	1.9497	-	1.9497	-
	Normalized k_{ij}	Spec.	0.7225	-	0.7225	-
	Young's Modulus, E	Process	158	-	158	GPa
	Density, ρ	Process	2300	-	2300	kg/m^3
	Frequency Material Constant, K_{mat}	(2.31)	0.654	-	0.654	-
	Disk Mass Adj. Factor, χ	[44]	0.763	-	0.763	-
Single Disk Resonator	Disk Radius, R	(2.17)	12.1	12.12	12.127	μm
	Structural Material Thickness, h	Process	3	3	3	μm
	Electrode-to-Resonator Gap, d_o	Process	40	39.1	39.1	nm
	Electrode Span Angle, θ_{ov}	Layout	330	330	330	°
	DC bias voltage, V_P	(2.18)	17	14	**14**	V
	Resonator Quality Factor, Q	Process	10,000	8,830	**8,830**	-
	Res. Electromech. Coup. Coeff., (C_x/C_o)	(2.31)	0.17	0.13	0.13	%
	Disk Dynamic Mass at Perimeter, m_m	(2.16)	2.4213	-	2.43	ng
	Disk Dynamic Stiffness at Perimeter, k_m	(2.16)	4.7963	-	4.79	MN/m
	Disk Damping at Perimeter, b_m	(2.16)	0.3408	-	**0.39**	μkg/s
Array-Composite Quadrant	Total No. of Disks, N_{tot}	(2.19)-(2.22)	24	24	24	-
	Rows × Columns, $N_{row} \times N_{col}$	Layout	4×6	4×6	4×6	-
	Number of Input/Output Resonators, N_{io}	(2.19)	14	14	14	-
	Number of Buffer Resonators, N_b	Layout	8	8	8	-
	Number of Tuning Resonators, N_t	(2.22)	2	2	2	-
	Acoustic Quarter-Wavelength, $\lambda/4$⁜	(2.25)	9.2503	9.27	9.27	μm
	Filter $5\lambda/4$ Coupling Beam Width, w_c	(2.26)	5.1664	-	5.3	μm
	Array-Composite $\lambda/2$ and λ Coup. Beam Width	Layout	1	1	1	μm
	Array Electromech. Coup. Coeff., (C_{xA}/C_{oA})	(2.54)	0.10	0.076	0.076	%

* Boldface value indicates a change from design value needed to curve fit the simulation to actual measured data.

⁜ The actual quarter wavelength coupler length used is $5\lambda/4$.

TABLE 2.VII: FILTER CIRCUIT DESIGN SUMMARY

	Parameter		Source	Design	Meas.	Adjusted/ Simulated	Unit
Core Equivalent Circuit Variables	Inductance at Disk-Composite Array Perimeter, l_{xA}		(2.28)	58.112	-	58.380	pH
	Capacitance at Disk-Composite Array Perimeter, c_{xA}		(2.28)	8.6872	-	8.6863	nF
	Resistance at disk-composite array perimeter, r_{xA}		(2.28)	8.1788	-	**9.2855**	μΩ
	$\lambda/4$ Coupling Beam Lumped Element, c_c		(2.27)	12.024	-	**11.748**	μF
	RF input port static overlap capacitance, C_{oA}		(2.29)	647.57	-	**664.08**	fF
	RF input port coupling coefficient, η_{eA}		(2.29)	275.22	-	**237.78**	μC/m
Tuning Port	Tuning port static overlap capacitance, C_{tA}		(2.30)	92.510	-	**94.869**	fF
	DC tuning voltage, V_t		Measured	17	12.1	**12.1**	V
	Tuning port coupling coefficient, η_{tA}		(2.30)	0	-	**4.61**	μC/m
Parasitic Elements	DC bias line resistance, R_{bias}		Measured	0	-	**5.85**	Ω
	λ coupling beam resistance, R_λ		Measured	0	-	**8**	Ω
	Overhead parasitic capacitances	C_{ft}	Measured	0	-	**27.50**	fF
		C_{fc}	Measured	0	-	**26.86**	fF
	Substrate parasitic resistances	R_{subt}	Measured	0	-	**378.98**	Ω
		R_{subc}	Measured	0	-	**388.76**	Ω
	Bond pad capacitance, C_{sub}		Measured	0	-	**530.5**	fF
	Agilent E5071C I/O Plane Eff. Tuning Inductor, L_{tune}		Measured	0	-	**423**	nH

* Boldface value indicates a change from design value needed to curve fit the simulation to actual measured data.

The end result of the design procedure comprises not only all relevant geometric dimensions, but also the resulting element values for the electrical equivalent model of Fig. 2.33 summarized in Table 2.VII. In each table, the variables under the column labeled 'Design' indicate the initial design goals assumed during device layout, while values under the column labeled 'Measured' provide the actual measured data obtained either directly from measured plots or curve-fitted to data sets from the fabricated filter structure. The 'Adjusted/Simulated' column provides values used in simulation and shows in boldface parameters introduced or adjusted to match simulated curves using the Fig. 2.33 circuit to the measured ones (more on this in Section 2.21).

2.20. Disk Filter Fabrication Process

Pursuant to verifying the overall design strategy detailed so far, the polysilicon vibrating disk filters of this work were fabricated using a five mask process similar to that of [35] with the cross-sections of major process steps presented in Fig. 2.37. Given the degrading impact of stress and electrical parasites outlined in Sections 2.14 - 2.16, the fabrication process employs modifications to the conventional polysilicon surface-micromachining process of [35] to mitigate these effects. In particular, it

1) increases the thickness of the doped polysilicon interconnect to reduce interconnect resistance from 21.3Ω/□ at the conventional 300nm-thick to 0.8Ω/□, at the new 3μm-thick; and
2) employs a generous amount of chemical mechanical polishing (CMP) to eliminate topography during alignment and lithography steps to reduce variance.

A. Fabrication Process Flow Description

The process starts on 6″ blank Si wafers with successive LPCVD depositions of 2μm LTO and 500nm low-stress silicon nitride at 450ºC and 835ºC, respectively, to serve as electrical isolation layers; followed by 3μm of LPCVD polysilicon deposited at 590ºC for 8 hours, then dopes via $POCl_3$ at 1000ºC. Lithography via a first mask and subsequent deep-reactive ion etching (DRIE) using an SF_6 chemistry then delineates the interconnect layer, which again due to its much greater thickness than previous processes, offers 0.8Ω/□ sheet resistance. A3.5μm-thick HTO layer is then blanket deposited via LPCVD at 920ºC to not only cover the polysilicon, but also to uniformly fill spaces between polysilicon interconnect traces. The CMP step that follows grinds away oxide until it selectively stops on the polysilicon traces, leaving a flat surface composed of oxide and polysilicon interconnect regions. This CMP step eliminates the high topography created by the 3μm-thick interconnect routing, and in doing so, facilitates subsequent lithography and etch steps, as well as prevents ripples in the structural resonator film to follow. Next, a blanket 500nm-thick LTO film deposited via LPCVD at 450ºC serves as a bottom sacrificial oxide layer (underlying eventual disks) with a uniform thickness over the flattened wafer surface, as depicted in Fig. 2.37(a). Circular stem openings with 2μm diameter are then lithographically defined and etched into the oxide film with the polysilicon interconnect serving as the etch stop.

LPCVD deposition of 3μm-thick structural polysilicon at 590ºC (followed by $POCl_3$ doping at 1000ºC) then covers the wafer and refills the stem openings etched in the previous step to form the anchor posts of the disk resonators. These mechanical anchors support the disk resonators at their very centers, which correspond to the contour mode vibration nodal points, while also connecting the electrically conductive disk structures to the underlying interconnect layer. A following LPCVD deposition at 450ºC of 1.2μm-thick oxide then establishes a hard mask layer to be used when etching the thick structural polysilicon. Following a lithography step to delineate the disk structures and coupling beams that form the mechanical filter, RIE using an Ar:CHF_3:CF_4 chemistry transfers the filter structure pattern into the oxide hard mask. Any photoresist remaining above the oxide is then removed to avoid polymer formation and photoresist re-deposition on the etch sidewall during the following structural polysilicon etch step.

The next step—etching the structural material—is vital to many aspects of device performance, from its resonance frequency to its *Q* to its repeatability. Indeed, etch undercut and smoothness both impact the resonance frequency and its repeatability. The smoothness and straightness of etched structural sidewalls further determine whether or not the desired mode shape ensues, which if not, degrades the achievable *Q*, especially if the resulting mode shape exhibits vertical motion that pumps energy through the anchor to the substrate. To ensure adequate smoothness and a sidewall angle as close to 90º as possible, exhaustive etch recipe characterization yielded an optimal Lam TCP 9400SE polysilicon RIE etch recipe using gas flow rates of 140sccm of HBr, 14sccm of Cl_2, and 5sccm of O_2 at 12mTorr pressure with 250W and 75W RF and wafer bias powers, respectively. This recipe etches polysilicon at a rate of 220nm/min with a polysilicon to oxide etch selectivity of 16:1 and reduces the sidewall roughness compared with higher Cl_2 flow rate recipes.

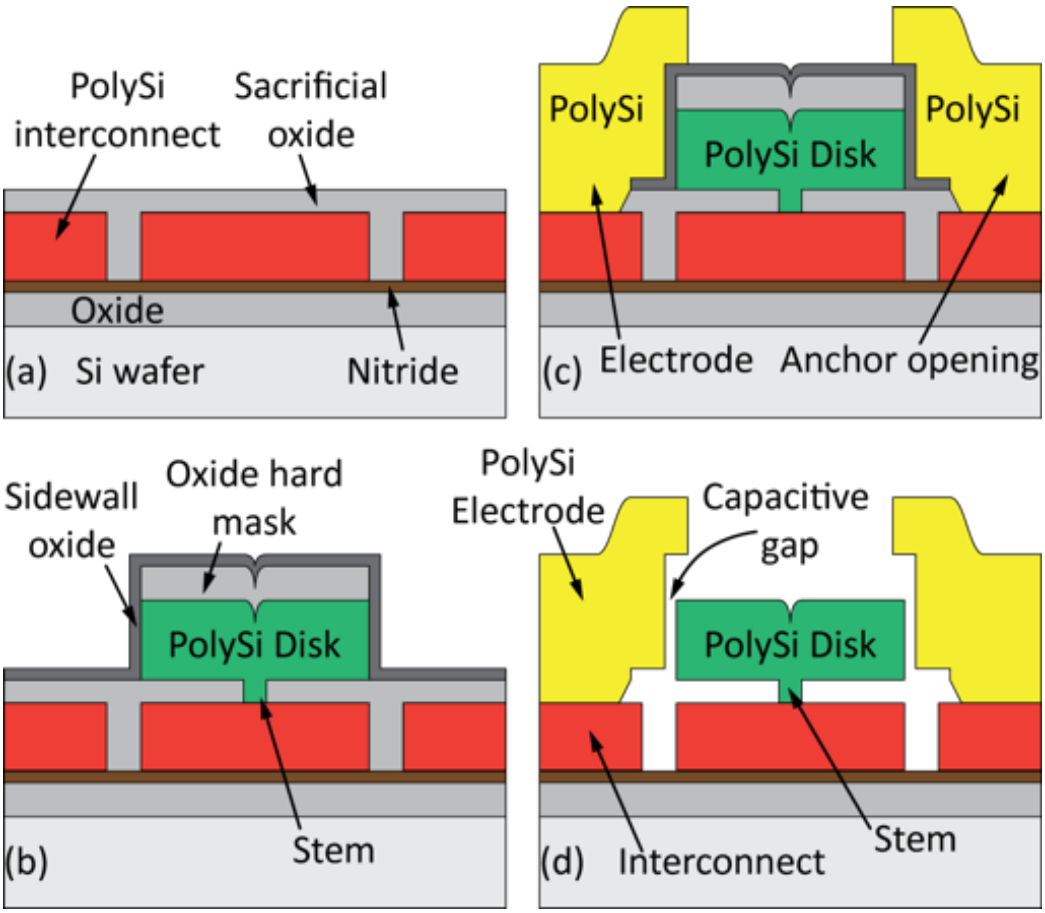


Fig. 2.37: Cross sections describing disk filter fabrication process flow after (a) patterning interconnect and depositing bottom sacrificial oxide, (b) depositing structural polysilicon over the stem opening followed by structural layer etch using an oxide hard mask and sidewall sacrificial oxide deposition, (c) opening electrode anchors then filling with doped polysilicon and patterning to form electrodes, and (d) fully released resonator.

The high selectivity between the oxide hard mask and the structural polysilicon film further enables the desired vertical sidewalls and transfers the layout lateral dimensions to the structural polysilicon film with reduced uncertainty. The efficacy of this recipe derives in part from the tendency of an HBr/Cl_2 based etch chemistry to form sidewall polymer residues containing halogens and silicon oxide [60] that protect sidewalls during etching. This barrier, however, should not be present during subsequent high temperature deposition steps. Removal of sidewall polymer residue entails immersion of wafers into a 50:1 hydrofluoric acid bath for 30 seconds, followed by rinsing in DI water, and finally immersion for 10 minutes in DuPont EKC-270 post-etch residue remover heated to 70°C.

After structural polysilicon patterning comes arguably the most critical step of the fabrication process: Deposition of the sidewall sacrificial oxide layer that defines the 39nm capacitive actuation gap between the disk and the surrounding electrodes. Here, LPCVD deposition of high temperature oxide (HTO) using 40sccm of DCS and 100sccm of N_2O flow with 600mTorr process pressure at 920°C coats a uniform, conformal, and pinhole free layer of HTO over the vertical disk sidewalls, as illustrated in Fig. 2.37(b). Electrode anchor openings are then etched into the bottom oxide sacrificial layer, followed by a blanket LPCVD deposition of 3μm-thick polysilicon and

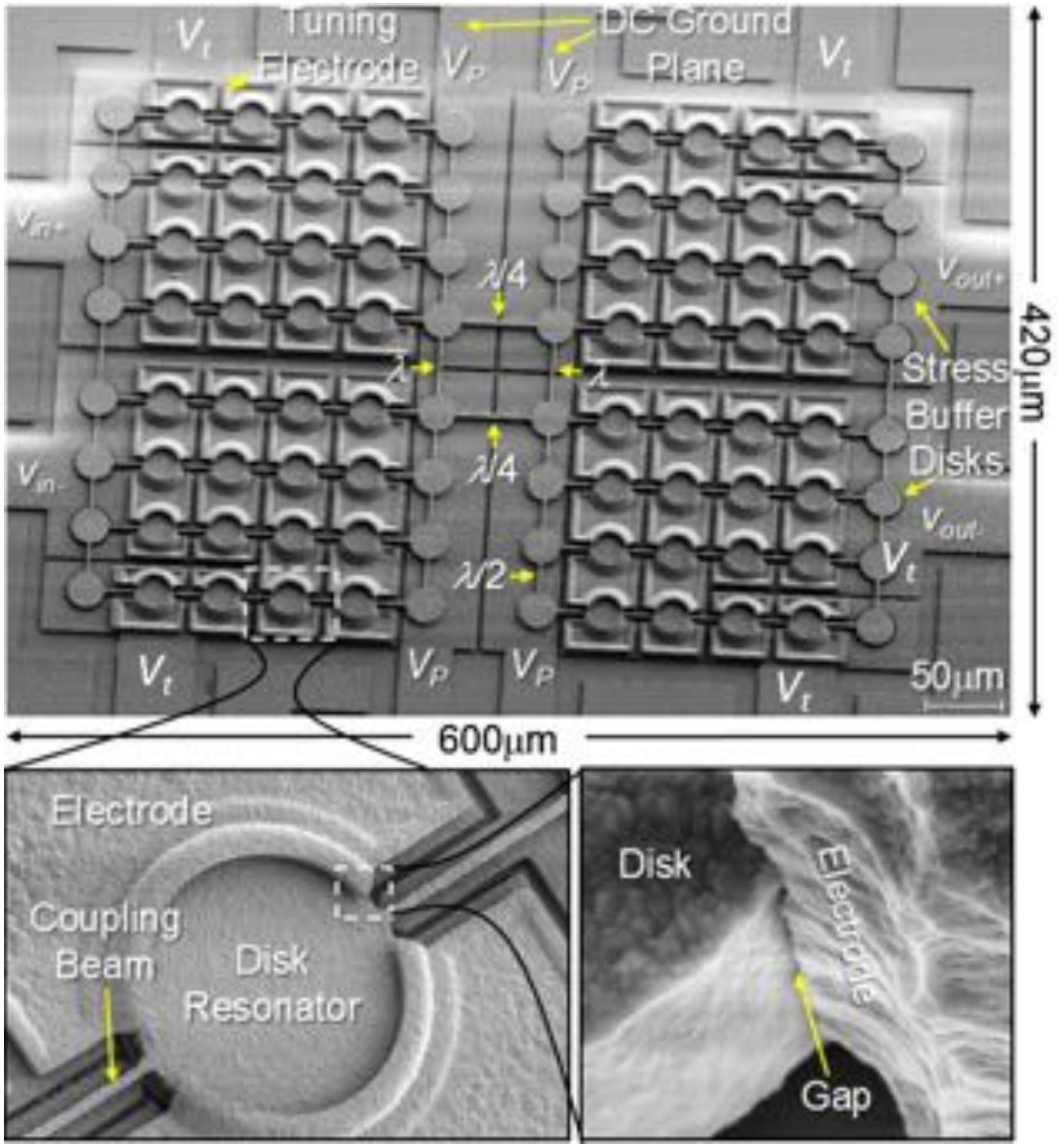


Fig. 2.38: SEM image of a fabricated and released second-order differential filter described schematically in Fig. 1. Zoomed-in view of one of the constituent disk resonator building blocks (left inset). Tiny (39 nm) capacitive actuation gap between the disk resonator and its electrode (right inset).

subsequent $POCl_3$ doping at 1000°C. The final lithography and dry etch steps then define the electrodes, as shown in Fig. 2.37(c).

Completed wafers are diced and the resulting dies released (when needed) in 49 wt. % liquid HF that frees the filter structure with the final resonator cross-section presented in Fig. 2.37(d). Fig. 2.38 presents the SEM image of a fabricated and released 2nd order differential filter that physically realizes the mechanical circuit schematically illustrated in Fig. 2.1. The insets in Fig. 2.38 focus in on a constituent disk resonator and coupling beams linking it to other devices in the filter network; and on the tiny capacitive actuation gap formed between the disk resonator and the electrode.

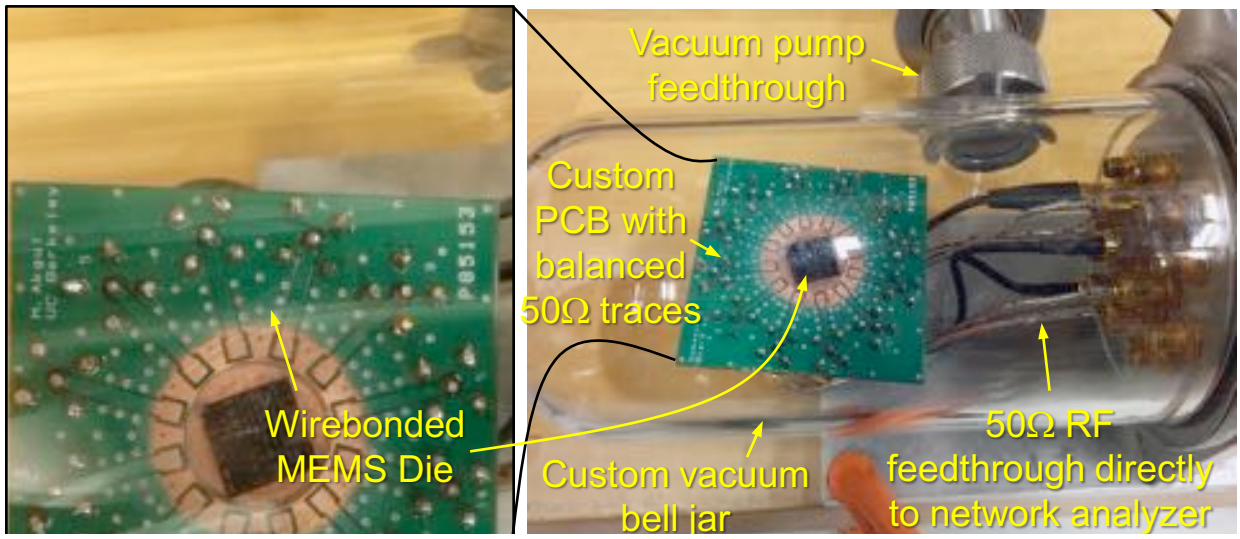


Fig. 2.39: Vacuum measurement setup using 50Ω RF feedthroughs with matching electrical lengths that connect the network analyzer directly to the wire-bonded micromechanical filter for balanced differential measurement.

2.21. Measurement Results

Immediately after fabrication, filters without buffer disks were shorted to their electrodes, and thus, non-functional. The fact that only filters with buffer disks worked, whether single-ended or differential, confirms the importance and efficacy of the buffer-based stress-relief strategy of Section 2.15.

Fabricated differential filters were tested via a four-port direct measurement setup mimicking the circuit of Fig. 2.1 using an Agilent E5071C network analyzer with the measurement plane moved to the I/O bond pads using standard SOLT calibration, i.e., the instrument compensates out parasitic elements up to the pads. (Since I/O shunt capacitance dominates among parasitics, this essentially amounts to applying an E5071C-simulated tuning inductance.) All measurements used 0dBm, i.e. $0.225V_{rms}$ signal amplitude, source power settings on all four ports of the network analyzer. During testing, the released MEMS die resides on a board emplaced into in a custom-made vacuum bell jar that provides a 30μTorr vacuum environment as well as ports to allow wired connection to outside measurement instrumentation. Inside the bell jar, wire bonds connect the MEMS die to balanced 50Ω pc-board traces that lead to 50Ω coaxial cable fixtures. These fixtures then permit direct coaxial cable connection to the network analyzer's 50Ω inputs, as shown in Fig. 2.39.

Again, the mechanical filter requires a 590Ω termination, so the 50Ω measurement system impedance must be transformed to 590Ω for correct filter operation. Here, the network analyzer's fixture simulator functionality comes in handy, where the network analyzer simulates 590Ω ports from signals measured at its 50Ω ports without the need for any external processing.

In addition to source power applied differentially to the I/O ports with instrument-simulated 590Ω source impedances, Fig. 2.1 indicates other electrical inputs to the device under test. These include a dc-bias voltage of $V_P = 14V$ applied to the conductive filter structure through the underlying dc-ground plane; as well as DC voltages applied to the indicated frequency tuning pads that connect to non-I/O electrodes purposed for voltage-controlled electrical stiffness tuning, such as described in Section 2.18.

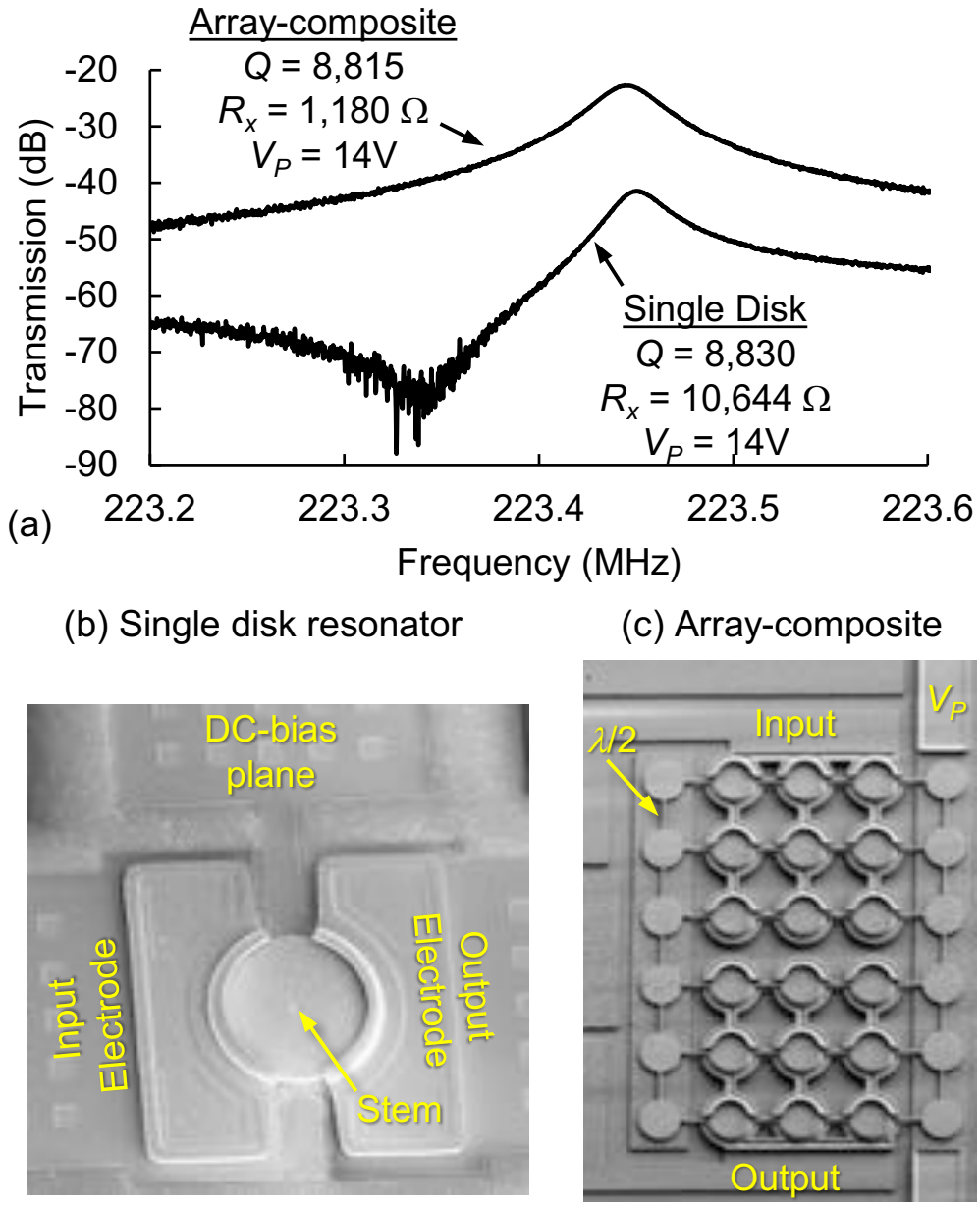


Fig. 2.40: (a) Comparison of two-port measured frequency spectra for a single disk resonator and a 30-resonator array-composite, with SEM images in (b) and (c).

A. Verification of λ/2 Coupled Array-Composite Operation

To demonstrate the benefits accrued by elevating the design hierarchy from single disk resonators to λ/2 coupled array-composites, Fig. 2.40(a) compares the measured two-port frequency spectrum obtained from a single disk resonator shown in Fig. 2.40(b) with that of a 30-resonator array-composite device shown in Fig. 2.40(c). Here, both the single disk resonator and those used in the 5×6 array have radii of 12.1μm, which sets their center frequencies at 223.4MHz. As shown, the array composite retains the high Q>8,000 of the single disk resonator while reducing its motional resistance by 9× from 10,644Ω to 1,180Ω for the same bias voltage of V_P = 14V. Note that these are two-port measurements where the dc-bias goes to the suspended structure while one electrode

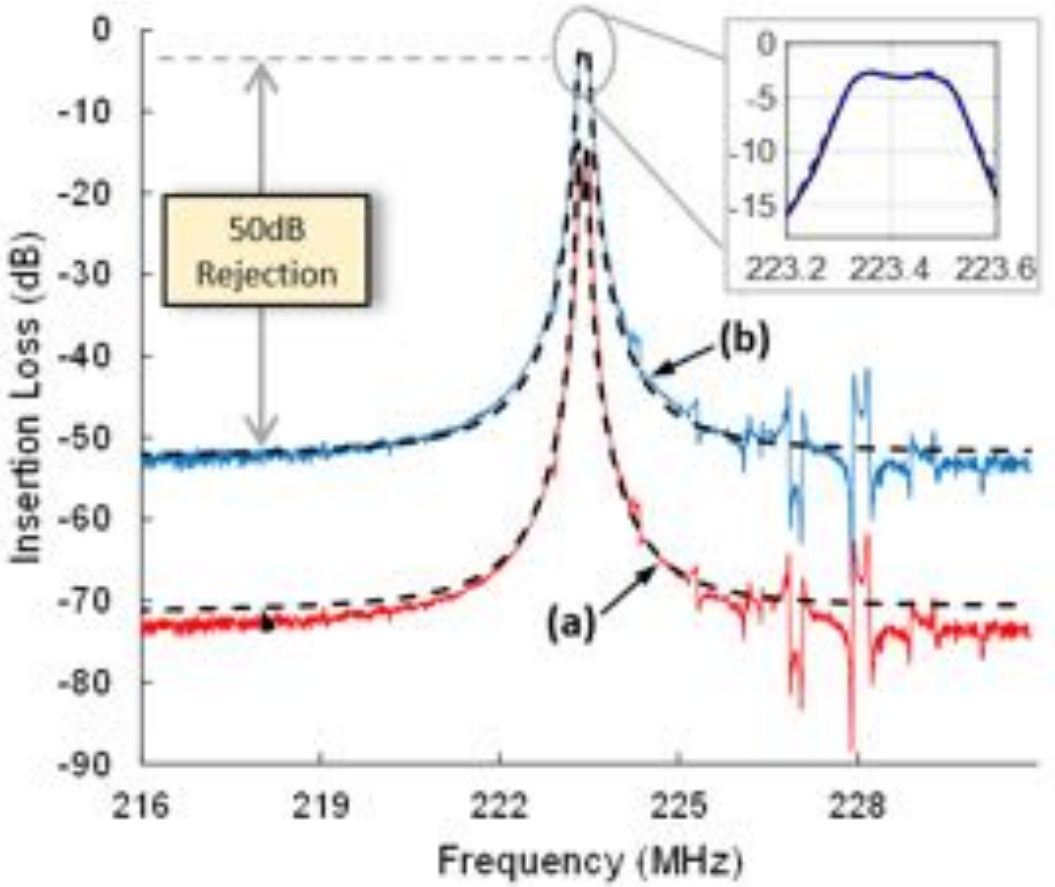


Fig. 2.41: Comparison of (a) unterminated (i.e., with 50Ω termination) and (b) 590Ω terminated measured filter spectra (solid lines) together with electrical equivalent circuit simulation results for both cases shown as dashed lines.

receives the input signal and the other the output signal [61]. The array in this case has the capacitive transduction area of 9 devices, which is smaller than the 14 for each array-composite quadrant of the Fig. 2.38 filter, so its motional resistance is significantly higher.

Nevertheless, the measured improvement in R_x agrees well with the theoretical expectation derived in (2.46) that the improvement factor should be proportional to N_{tot} / N_{io}^2. Here, $N_{tot} = 30$ is the total number disks used in the array-composite, including stress-buffer devices in the array perimeter; and $N_{io} = 18$ is the number of resonators with surrounding input/output electrodes. These numbers predict a 10.8× R_x reduction. The slight difference between the measured 9× R_x improvement and the theoretical expectation likely derives from phase mismatches between arrayed resonators that prevent the total summed motional current from attaining the ideal value that would otherwise be delivered to the output node if all resonators vibrated in perfect phase [39].

Phase deviations notwithstanding, the presented disk array-composite mechanical circuit serves as a good example of enhanced functionality via a building block approach, where the array-composite displays strong agreement between the measurement results and the predicted reduction in R_x while maintaining the high Q and single vibration frequency of a single disk device.

B. Terminated & Electrically Tuned Filter Spectrum

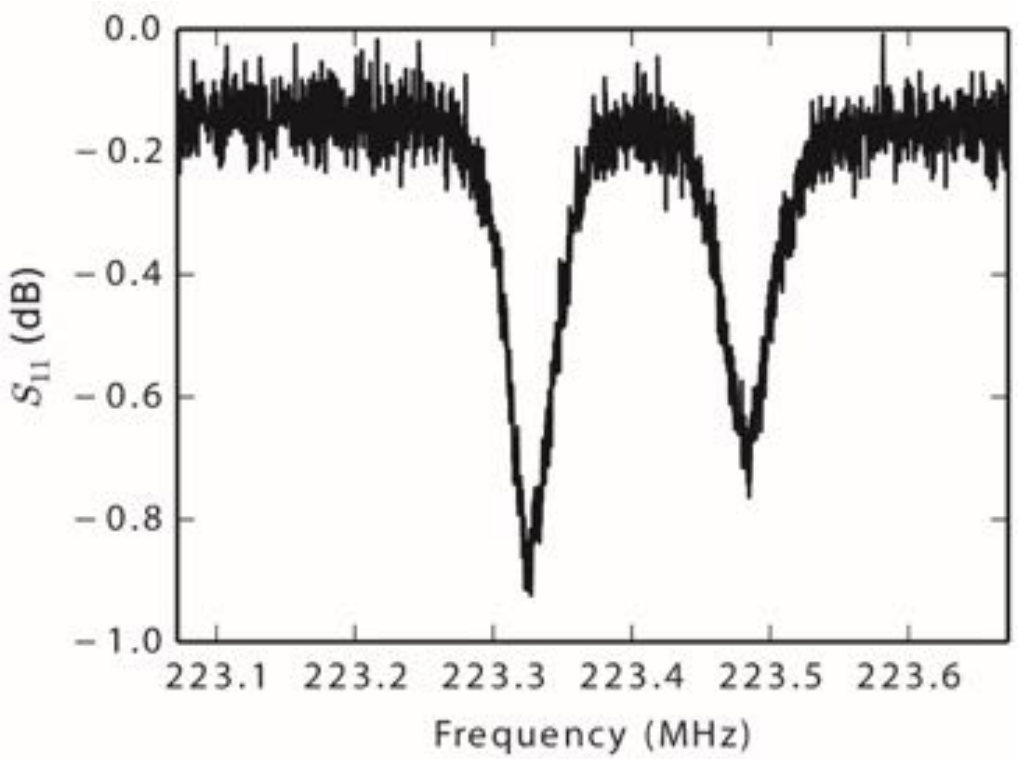


Fig. 2.42: Measured return loss, i.e. S_{11}, data from the positive-input electrode of the differential filter under identical measurement conditions to those of

Fig. 2.41(a) presents the measured filter spectrum as driven and sensed directly by the 50Ω ports of the network analyzer without using its impedance simulation capability. Without the designed 590Ω termination, the measured spectrum is not one expected for a properly designed filter, but rather one with the jagged passband and small stopband rejection shown. As with any filter, whether its resonators are *LCR*s, waveguides, or mechanical resonators, the response does not take on the designed response unless terminated by the designed impedances.

Fig. 2.41(b) presents the measured, tuned, and terminated filter spectrum with an inset zoom-in on the passband showing it centered at 223.4 MHz with 229-kHz, i.e., 0.1%, bandwidth and only 2.7dB insertion loss. Here, 590Ω network analyzer-simulated impedances terminate the filter as schematically described in Fig. 2.1, with a dc-bias voltage of 14V applied to the resonator body and 12.1V to tuning electrodes to correct the filter passband. Small gaps combined with the symmetric and differential design lead to 50dB out-of-channel rejection and a 20-dB shape factor of 2.7. This amount of rejection is 23dB better than a previous capacitive gap transduced differential filter design [25] that did not benefit from low parasitic resistance traces. The 39nm capacitive transducer gaps of this work generate a single-resonator coupling strength of $C_x/C_o = 0.13\%$, which is 6.4× improvement over previous efforts [25]. However, the array-composite value (with buffer and tuning disks included) shrinks to 0.07%, which is just on the edge of the requirement for an undistorted equiripple passband.

The results presented in succeeding figures, i.e., Fig. 2.41-Fig. 2.48, are measured with 0dBm output power setting applied to all four ports of the network analyzer that corresponds to $0.225V_{rms}$ signal amplitude applied to the I/O electrodes of the filter. Since the device under test is not impedance matched to the 50Ω terminals of the network analyzer, a portion of the applied 0dBm

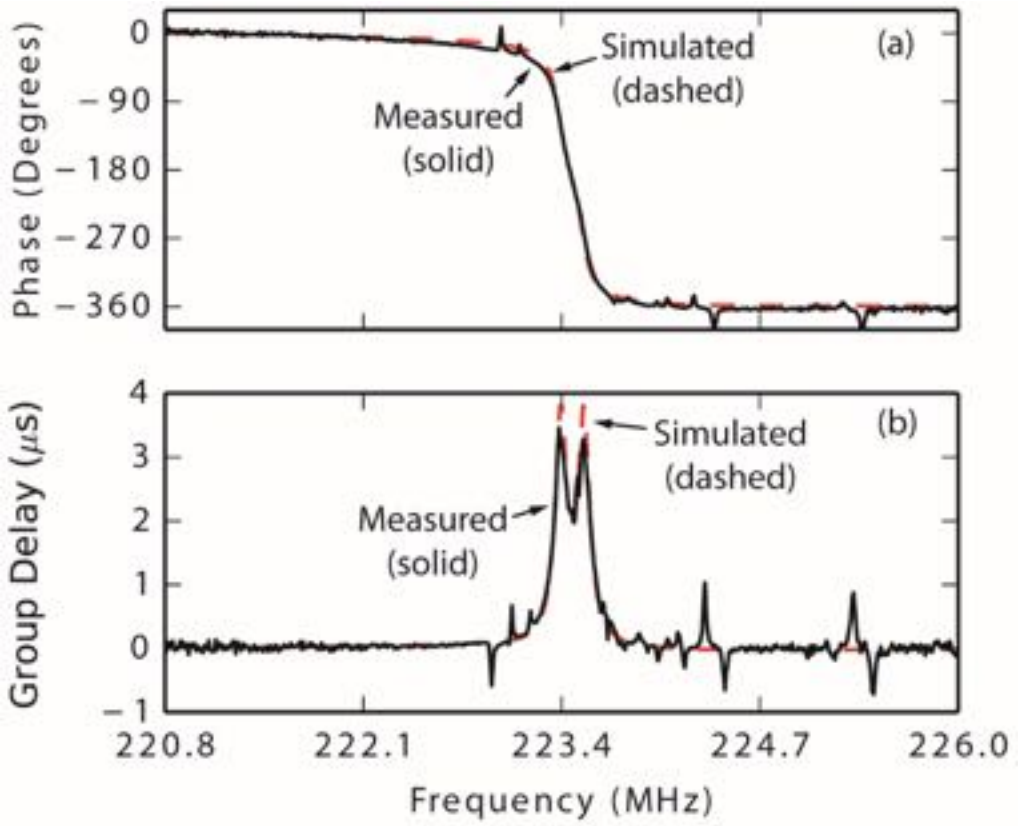


Fig. 2.43: (a) Phase response and (b) corresponding group delay of the differential filter, where the solid curves indicate measured data obtained under measurement conditions identical to Fig. 2.41, and dashed lines indicate simulated responses obtained from the electrical equivalent circuit of Fig. 2.33 using the circuit element values listed in Table 2.VII.

power reflects back to the source as indicated by the return loss, i.e. S_{11}, data presented in Fig. 2.42 obtained from the positive-input port of the filter with Z_o = 50Ω termination. Here, the in-band return loss of 0.9dB indicates that 81% of the 0dBm, i.e., 1mW, applied from the network analyzer port reflects back, and the actual power going through the filter network is 190μW, i.e., -7.2dBm, which is considerably above the GSM maximum in-band power specification of -26dBm. As the zoomed-in inset in Fig. 2.41 indicates, the filter does not suffer any distortion at -7.2dBm drive power due to Duffing non-linearity. Here, array-composite design is key to raising power handling ability so that the passband distortion under strong inputs that plagued a previous capacitive-gap transduced filter implementation [62] does not occur. Since filter linearity and power handling ability continues to improve with increasing array-size [37] [63], this hierarchical design provides enough design flexibility to accommodate wide dynamic range needs.

The dashed curve in Fig. 2.41(b) is the theoretical SPICE-simulated prediction via the circuit of Fig. 2.33 using the element values of Table 2.VII. To maximize simulation accuracy, the simulations

1) Use the negative-capacitance model [44] for each electrical port to accurately capture electrical stiffness effects, which in turn provide precise filter pole locations for arbitrary port termination impedances.
2) Capture the dominant feedthrough paths accurately, as elaborated in Section 2.17.

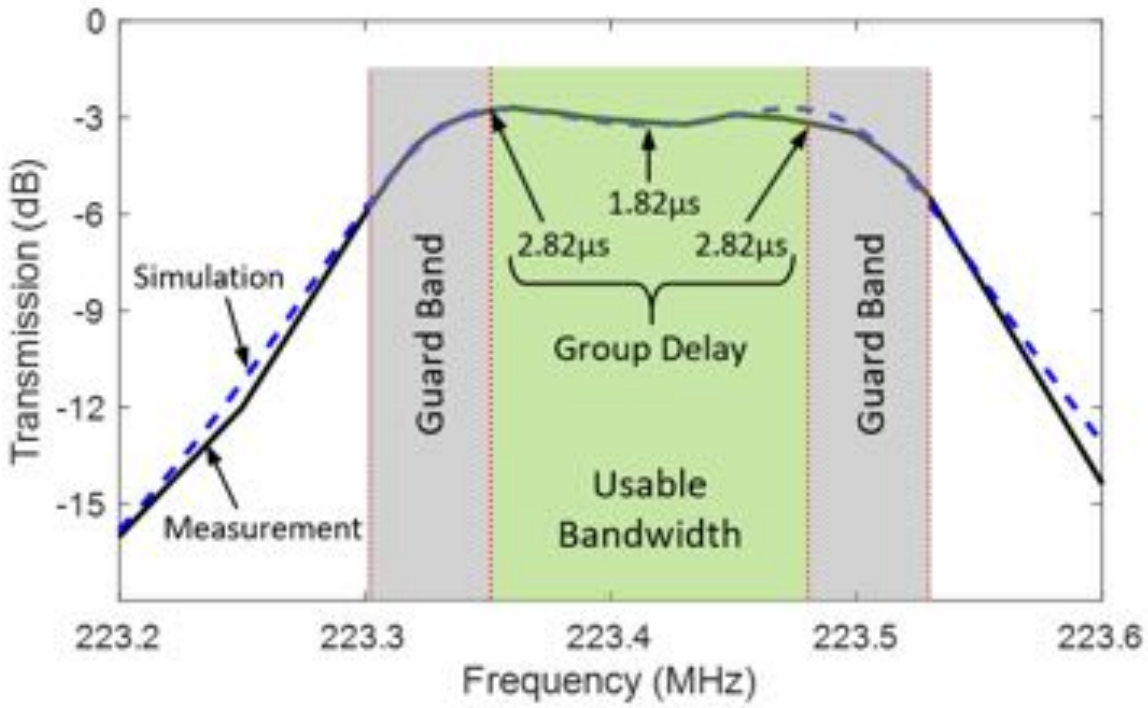


Fig. 2.44: Terminated filter spectrum indicating usable bandwidth and guard bands, where the 'Usable Bandwidth' region maintains group delay variations below 1µs.

The match between measurement and simulation is remarkable and confirms the accuracy of the filter theory and design procedure herein.

C. Measured Group Delay

Fig. 2.43(a) presents the measured phase response of the terminated filter, along with its group delay [41] in (b) obtained by taking the derivative of (a). To avoid undue distortion or intersymbol interference in digital communication systems, an ideal filter would have constant group delay, or linear phase. Any real filter, of course, has non-constant group delay.

To sufficiently suppress the increase in bit-error rate (BER) instigated by group delay-induced distortion, the group delay variation across the usable filter passband should be less than the period of the fastest processed signal. As a rule of thumb, the group delay should be much less than the reciprocal of the filter bandwidth. How much less depends upon the application, but one reasonable rule of thumb is that it be 1/5 the reciprocal bandwidth. With a bandwidth of 229 kHz, this means the variation in group delay for the demonstrated filter should be on the order of 1µs.

Fig. 2.43(b) shows that the demonstrated filter satisfies this 1µs criterion over a usable bandwidth of 128 kHz, which Fig. 2.44 plots on a zoomed scale. The measured phase and group delay response presented as the solid curves in Fig. 2.43 are in good agreement with the theoretical expectation plotted as dashed lines obtained by the simulation of the Fig. 2.33 equivalent circuit using the circuit element values listed in Table 2.VII.

D. Spurious Modes

Among the most troubling considerations in practical filter design are spurious modes, i.e., peaks of response at frequencies in the stopband. Suppression of spurious modes often requires creative solutions that are not easily designable and that often result in unique geometries, e.g., the

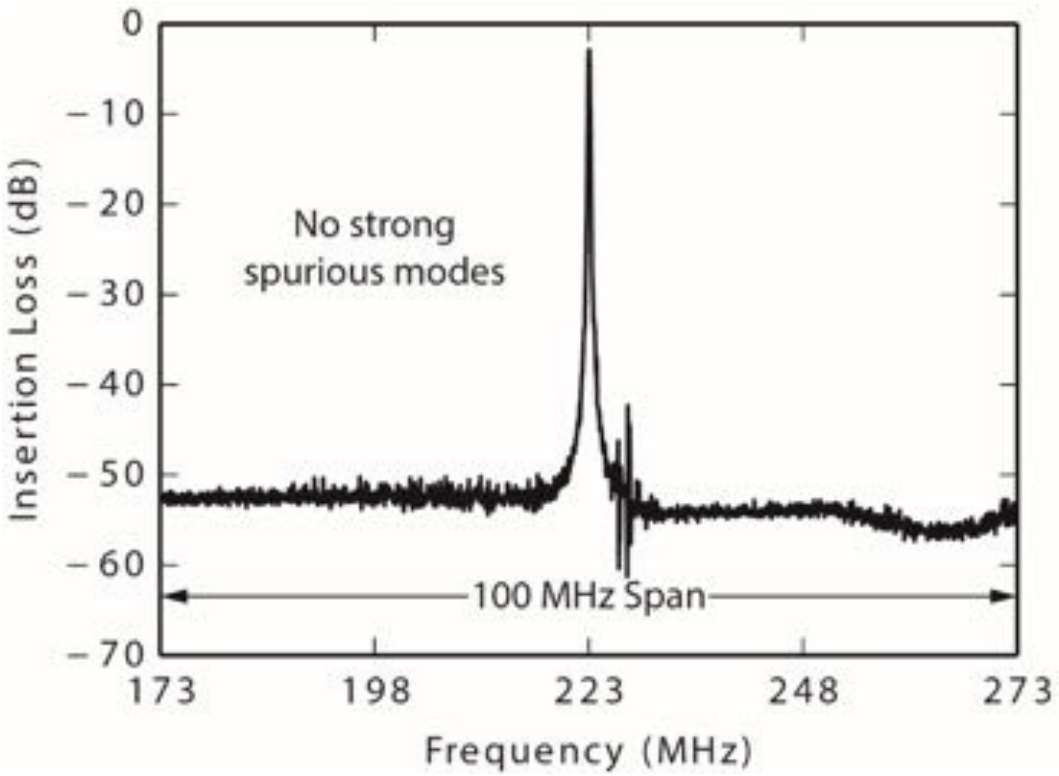


Fig. 2.45: Measured terminated spectrum over 100 MHz span showing no strong spurious modes.

polygons of FBAR filter design [64]. Interestingly, the micromechanical filter design herein suffers much less from these issues, as shown in Fig. 2.45, which presents the terminated spectrum for the Fig. 2.38 filter over a 100-MHz wide span, showing no strong spurious modes.

The spurious mode advantage evident here arises from two important features of the present filter design: 1) fully balanced differential design, with geometric and electrical symmetry; and 2) the availability of frequency tuning via voltage-controllable electrical stiffnesses. Both of these features used in tandem are instrumental to the Fig. 2.45 result.

In a similar way that a symmetric and differentially balanced mechanical and electrical design suppresses electrical feedthrough, it also suppresses the spurious vibration mode shapes that might otherwise arise in a complex mechanical network fabricated with finite production precision. As for the case of parasitic electrical feedthrough, if the filter structure is perfectly symmetric, the mechanical mode shape of Fig. 2.46(a) is undisturbed and only the desired mode ensues. Conversely, any asymmetry introduces mode shape distortion, as finite-element simulated in Fig. 2.46(b). This distortion effectively generates additional modes, i.e., unwanted spurs.

Perhaps the best testament to the importance of a fully balanced structure for spurious mode suppression comes from straight comparison of a single-ended design with the fully balanced design of Fig. 2.38. With this in mind, Fig. 2.47(b) presents the measured frequency response of the filter structure of Fig. 2.47(a), which comprises just the top half of the Fig. 2.38 design, so is not symmetric, not differentially balanced, and takes as input and output single-ended signals. The measured response clearly suffers numerous deficiencies, including feedthrough that reduces the stopband rejection to only 15dB (down from the passband level) and spurious modes only 10dB below the passband level. There is no comparison between this spectrum and that of the symmetric differentially balanced design of Fig. 2.38.

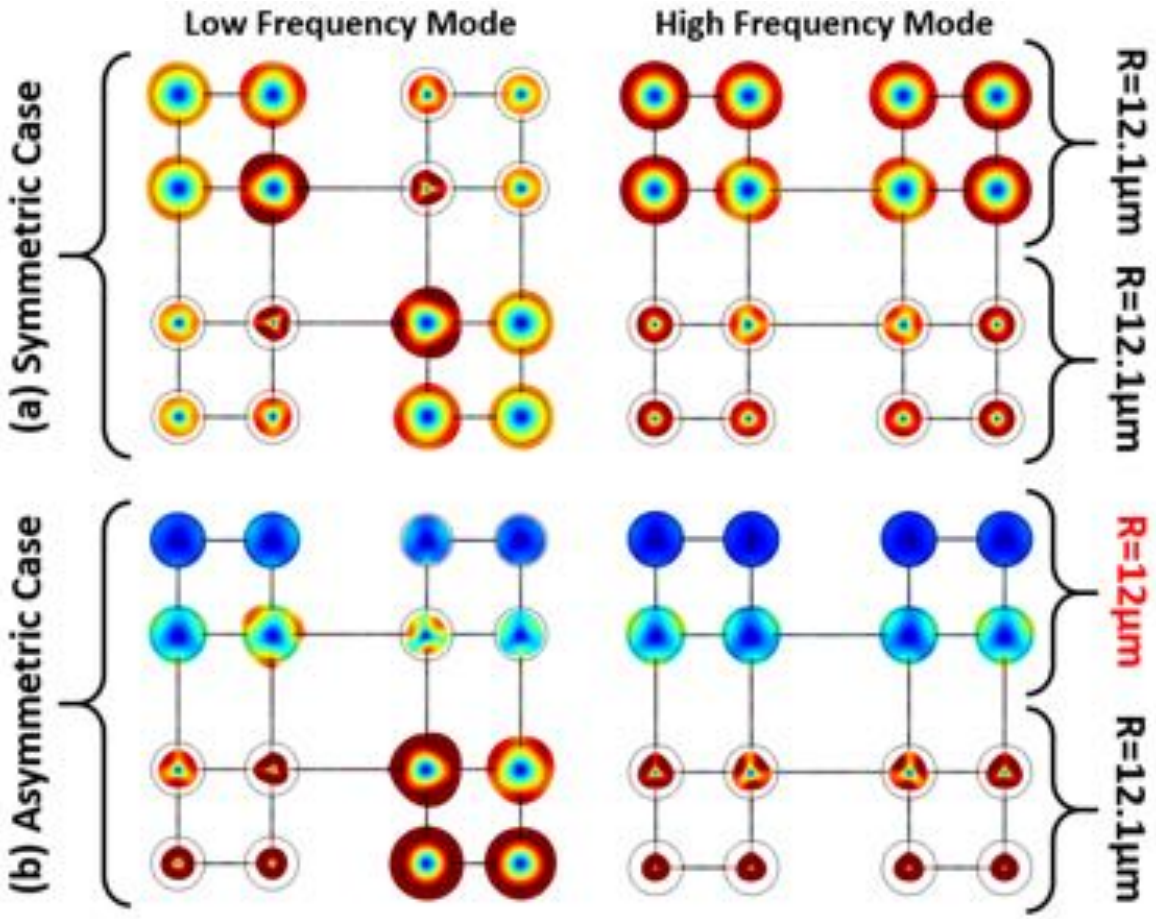


Fig. 2.46: Mode shapes with (a) full symmetry (b) 1% mismatch between the disk radii at the top and bottom half.

Clearly, symmetry and balance are key to the much better performance of Fig. 2.41(b) than Fig. 2.47(b). Indeed, just the use of a symmetric and fully balanced design affords much better performance than that of a single-ended design. However, improvements in performance to the degree seen in Fig. 2.41(b) require not only symmetric design, but also the means to perfect the symmetry after fabrication. This is where voltage-controlled frequency tuning provided by electrical stiffness plays an important role.

E. Electrical Stiffness Tuning Strategy

Indeed, post-fabrication voltage-controlled frequency tuning was instrumental to "fixing" not only feedthrough and spurious mode issues, but also the shape of the filter passband response. Fig. 2.48 emphasizes the importance of electrical tuning for this tiny percent bandwidth filter by demonstrating how proper tuning with 12.1V improves the passband shape and minimizes insertion loss compared to insufficient tuning with 5V and no applied tuning voltage. Here, 2.3dB better insertion loss comes about only after voltage-controlled frequency tuning of the array-composite resonator frequencies.

The optimum tuning voltage was determined empirically by varying V_t and simultaneously monitoring the resulting change in filter frequency response on a network analyzer, until symmetric passband ripple heights were observed around the filter center frequency, which is the expected equiripple passband shape of a Chebyshev filter. The tuning voltage that yields symmetrically

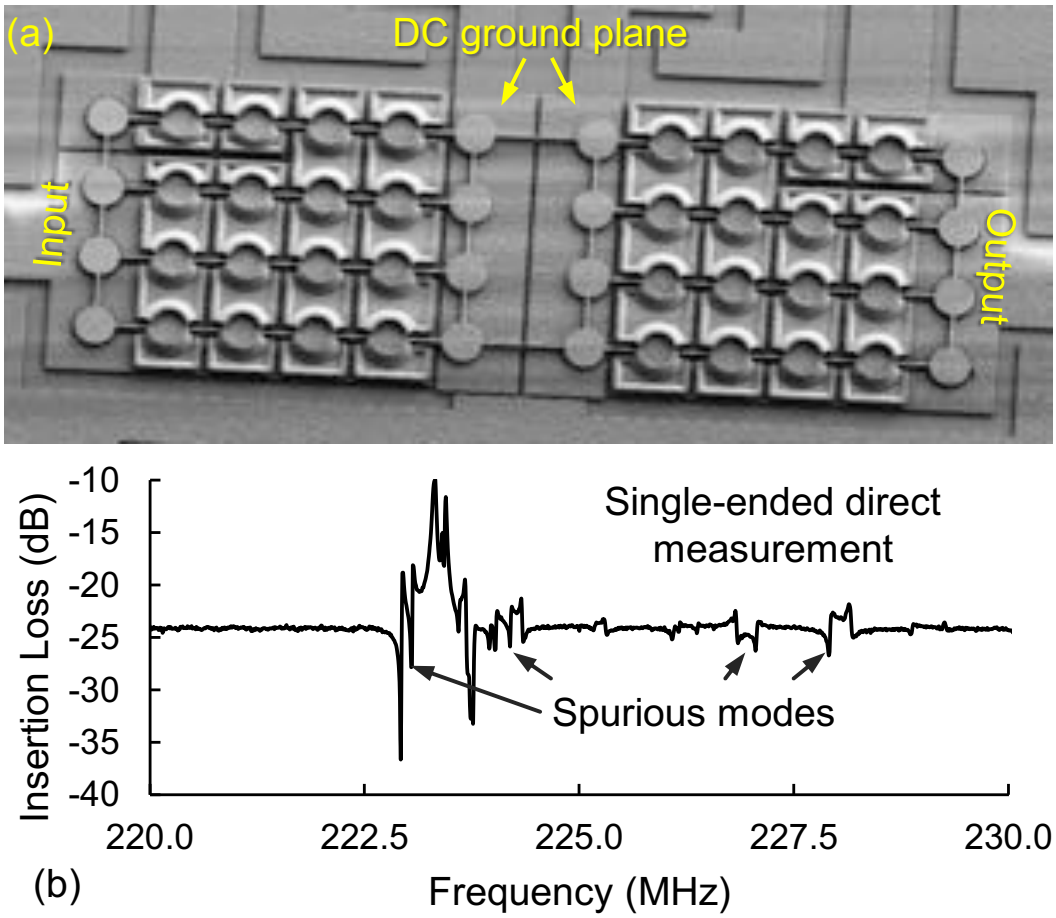


Fig. 2.47: (a) SEM image and (b) measured 590Ω terminated frequency response of a single-ended version of a disk-array filter, emphasizing the importance of differential design to suppress feedthrough and spurious modes.

positioned passband ripple peaks with equal height also achieves the minimum insertion loss as expected from the closer-to-ideal filter response. This observation is in-line with previous efforts on electrical tuning of kHz frequency capacitive comb-actuated filters [20], [65], where positioning passband resonant peaks equidistant around the filter center frequency via electrical tuning minimized insertion loss and yielded the desired filter response. Automatic tuning techniques using intelligent transistor circuitry would certainly be beneficial in future filter implementations, not only as a low cost post-fabrication tuning method, but also for real-time adaptive compensation of frequency drift over time due to aging or temperature variations.

2.22. Conclusions

The combined 2.7dB passband insertion loss and 50dB stopband rejection of the demonstrated 206-element 0.1% bandwidth 223.4-MHz differential micromechanical disk filter represents a landmark for capacitive-gap transduced micromechanical resonator technology. This demonstration proves that the mere introduction of small gaps of around 39nm goes a long way towards moving this technology from a research curiosity to practical performance specs commensurate with the needs of actual RF channel-selecting receiver front-ends. It also emphasizes the need for

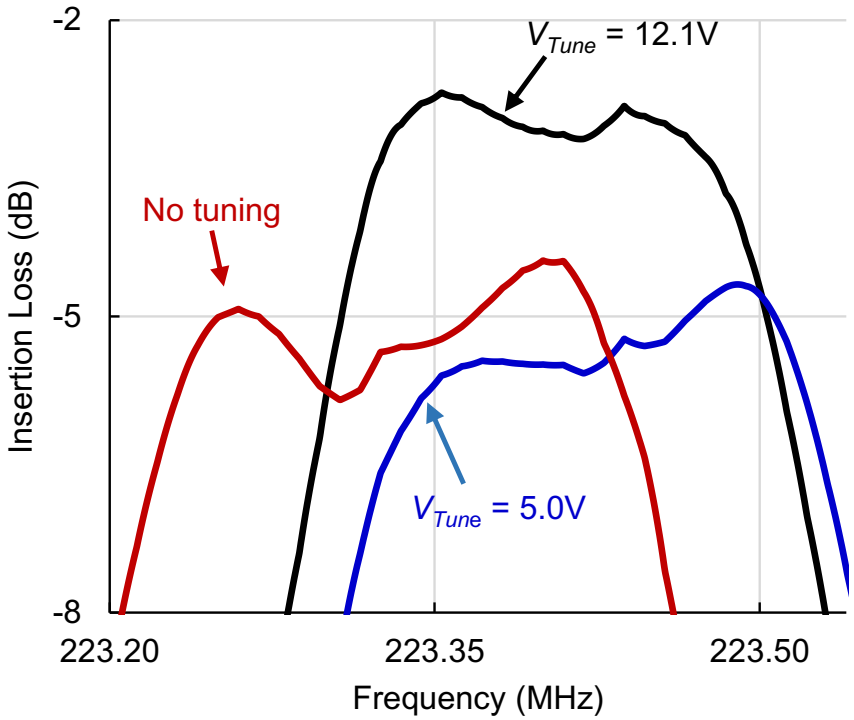


Fig. 2.48: Measured comparison of terminated filter passband spectrum for varying tuning cases.

tuning and defensive stress-relieving structural design when percent bandwidths and gaps shrink, all demonstrated by the work herein.

The presented intuitive hierarchical mechanical circuit design flow is technology agnostic and empowers a designer in much the same way that intuition facilitates transistor circuit design. Electromechanical analogies that model the resonance behavior of filter building blocks, such as vibrating disk resonators, capacitive actuation electrodes, and coupling beams, facilitate the use of conventional *LC* ladder filter design tables and methods as the starting point for filter design. This in turn simplifies realization of familiar filter types, e.g., Chebyshev, Butterworth, Linear Phase, etc.

While known filter design methods readily achieve ideal designs, they do not address the non-idealities of micromechanical realization, which include high single-device impedance, shunt I/O capacitance, finite coupler stiffness, stress, and fabrication process variations. The methods described herein address these issues via a combination of device scaling and mechanical circuit design. Specifically, capacitive transducer gap scaling very effectively raises electromechanical coupling (C_x/C_o) to needed values. The use of mechanically coupled resonator array-composites then permits tailoring of impedance values, resonator-to-resonator coupling, mismatch tolerances, and stress relief to outright enable design of practical filters. Finally, balanced differential design suppresses both electrical and mechanical spurious responses. These design strategies will likely become indispensable as the frequency and order of micromechanical filters increase to meet the demands of practical next-generation commercial transceivers.

Perhaps most encouraging is that the models presented in this study used to design the filter and predict its behavior seem to all be spot on. This means that predictions using these models fore-

telling GHz filters with sub-200Ω impedances enabled by 20nm-gaps might soon come true, bringing this technology ever closer to someday realizing the ultra-low power channel-selecting communication front-ends targeted for autonomous set-and-forget sensor networks [9], [11], [66]. Work towards these goals continues with renewed encouragement.

Chapter 3
High-C_x/C_o Hollow Disk Resonators

This chapter presents that mass and stiffness reduction via hollowing out a capacitive-gap transduced radial mode disk resonator while maintaining resonance frequency and transduction area enables a measured electromechanical coupling strength (C_x/C_o) of 0.75% at 123 MHz without the need to scale the device's meager 40-nm electrode-to-resonator gap. This is almost 7× improvement in C_x/C_o compared with a conventional radial contour-mode disk at the same frequency, same dc bias, and same gap. It also comes about via a fabrication process that deviates only slightly from a standard disk resonator process. C_x/C_o increases like this should improve the passbands of channel-select filters targeted for low power wireless transceivers, as well as lower the power consumption of MEMS-based oscillators.

3.1. Introduction

Capacitive-gap transduced micromechanical resonators [67], [45], [68], [69] routinely post Q's several times higher than piezoelectric counterparts [14], [15], [16], [70], [71], [72] making them the preferred platform for HF and low-VHF (e.g., 60-MHz) timing oscillators [73], [74], [75], [76], [77], [78] as well as very narrowband (e.g., channel-select) low-loss filters [79], [80], [33], [23], [81] targeted for low power communications [10], [11]. However, the small electromechanical coupling C_x/C_o of many capacitive-gap transduced resonators at higher frequency prevents sub-μW GSM reference oscillators [74], [82] and complicates realization of wider bandwidth filters. To the former point, the critical transconductance, hence the minimum power consumption, required to sustain oscillation with the Pierce topology is inversely proportional to C_x/C_o^2 [82] implying that low power consumption necessitates large C_x/C_o and small C_o. To the latter point, Fig. 3.1 illustrates how raising C_x/C_o from 0.11% to 0.56% nicely corrects the passband distortion in a 123-MHz, 600-kHz bandwidth micromechanical filter.

Recent fabrication technology that enables 13-nm gaps in polysilicon wine glass-mode disk resonators to make available C_x/C_o's of 1.62% at 60 MHz stands poised to solve the low-C_x/C_o problem, where the projected C_x/C_o at 123 MHz with 13-nm gaps and 5.5V bias is 1.05% [45]. Still, a method for raising C_x/C_o without such small gaps might be preferable, especially where device yield is paramount, e.g., for a high-volume product.

This chapter demonstrates one such method that achieves larger C_x/C_o by reducing mass and stiffness via hollowing out a radial mode disk resonator while keeping resonance frequency and transduction area intact. Use of this method yields a polysilicon "hollow disk" resonator having an electrode-to-resonator gap spacing of 37nm with C_x/C_o values as high as 0.75% at 123 MHz. Compared with the 0.11% expected for a conventional radial contour-mode disk resonator at the same frequency and with the same dc-bias voltage, this is almost a 7 times improvement in C_x/C_o.

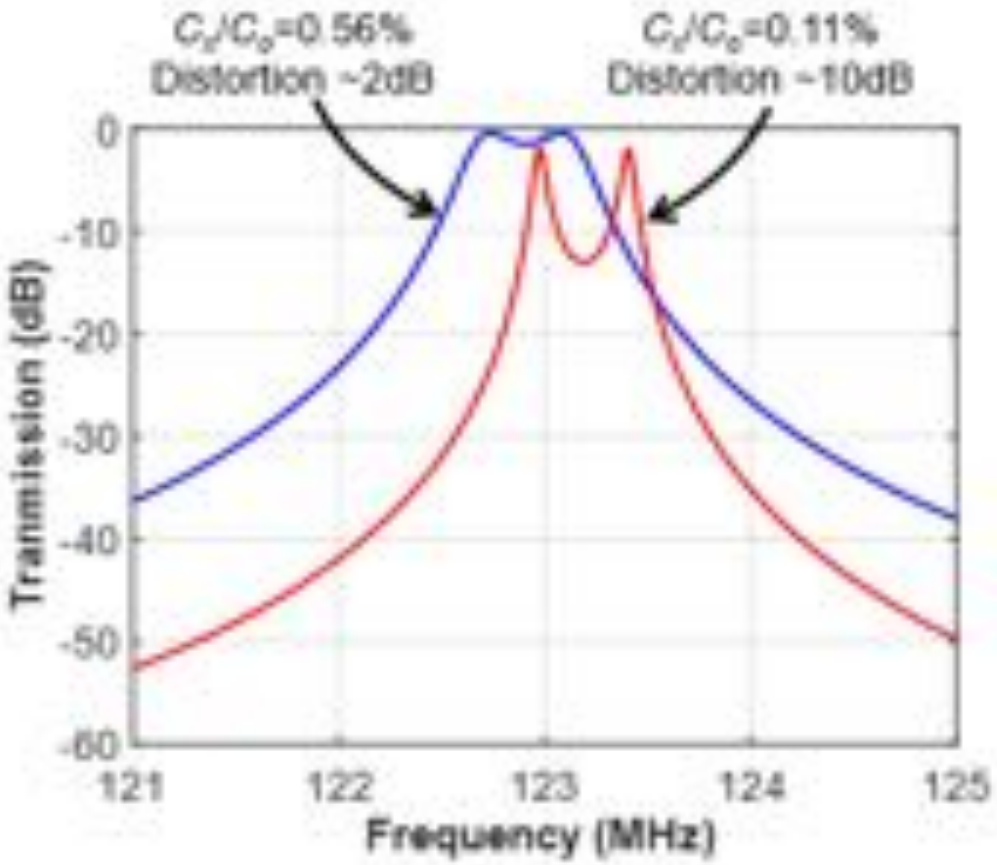


Fig. 3.1: Simulated two-resonator radial-mode solid disk filter frequency response curves demonstrating how an increase of C_x/C_o from 0.11% to 0.56% can make the difference between a distorted and flat passband, respectively, for a 123-MHz 600-kHz bandwidth channel-select filter.

After briefly reviewing conventional solid disk resonators and factors that impact their performance in Section 3.2, this paper introduces the hollow disk resonator concept and derives its equivalent circuit model in Section 3.3. Section 3.4 then uses the model to gauge performance enhancements, e.g., in C_x/C_o and motional resistance, offered by resonator hollowing. After detailing the surface micromachining process used to fabricate the devices in Section 3.5, Section 3.6 finally presents measurement results.

3.2. Conventional Disk Resonators

Before delving into the details of the described hollow disk resonator, it is instructive to first review the device it replaces. To this end, Fig. 3.2(a) presents the perspective view of a conventional solid disk resonator along with a cross-sectional view in Fig. 3.2(b) [83]. The structure consists of a 3μm-thick polysilicon disk spaced 500nm from the underlying doped polysilicon interconnect layer and anchored at the center via a circular stem. The doped polysilicon electrodes laterally separated from the disk with a tiny air gap do surround the resonating body, through which a capacitively applied small signal voltage v_{drive} atop dc-bias voltage V_P creates a dynamic electrostatic force in the air gap do between the disk edge and output electrodes that drives the disk into motion, with sizable displacement amplitudes ensuing when the drive frequency is at the disk resonance frequency f_o. Depending on the drive electrode configuration and signal frequency, the disk might resonate in the radial-contour mode where the entire disk edge moves radially in-phase or

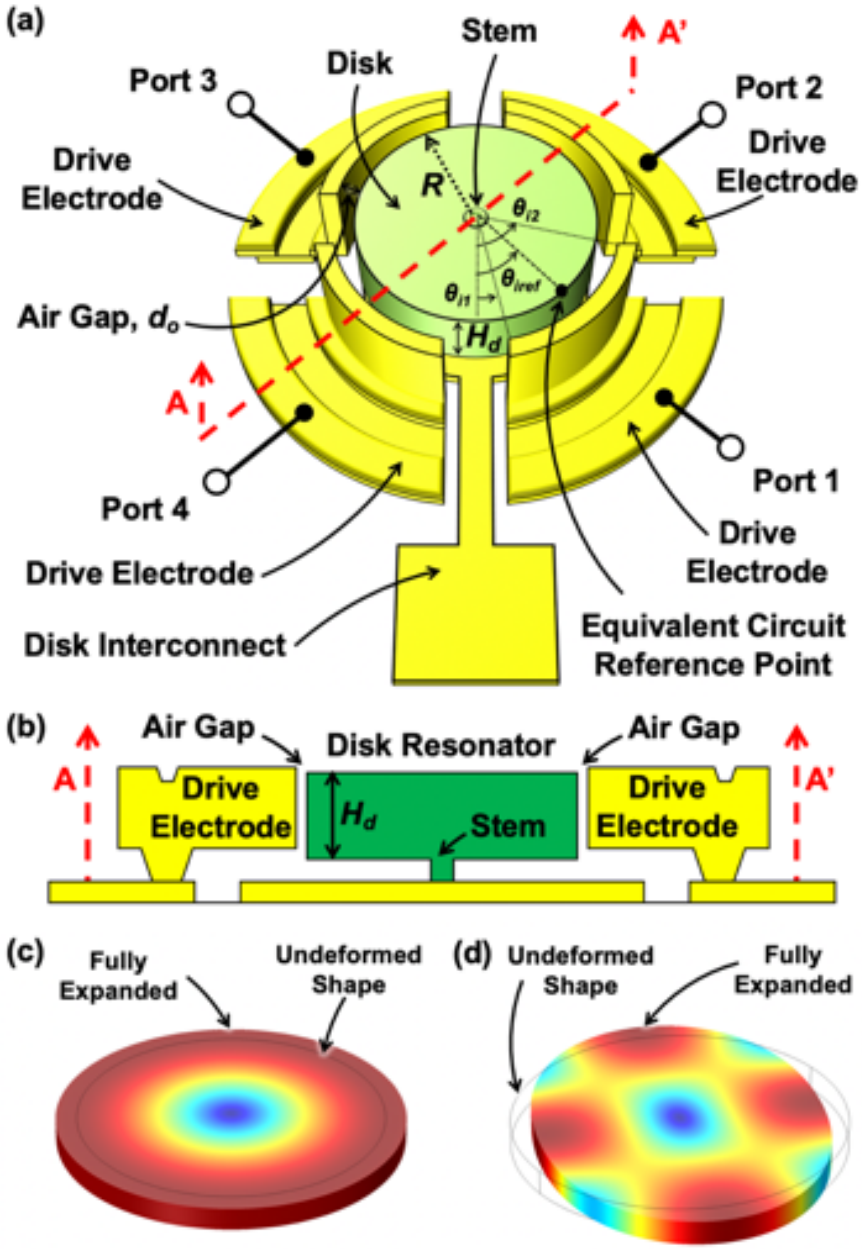


Fig. 3.2: a) Conventional disk resonator. (b) Cross-sectional view. (c) FEA-simulated radial-contour mode resonance shape. (d) FEA-simulated wine-glass mode resonance shape.

in the wine-glass mode expanding along one axis and contracting along an orthogonal one as depicted in Fig. 3.2(c) and (d), respectively. The resultant change in the overlap capacitance C_o then creates an output current i_{out} across the dc-biased time-varying capacitive gap that allows electrical detection of the device response.

Exciting a disk resonator into the radial-contour mode while maximizing the output current requires utilizing the entire overlap area between the disk edge and the output electrodes for electrostatic transduction. With fully surrounding electrodes, i.e., setting (θ_{i2} - θ_{i1}) = 90° for all four electrodes in Fig. 3.3(a), for example, the motional output current in the radial-mode takes on the following form [44]

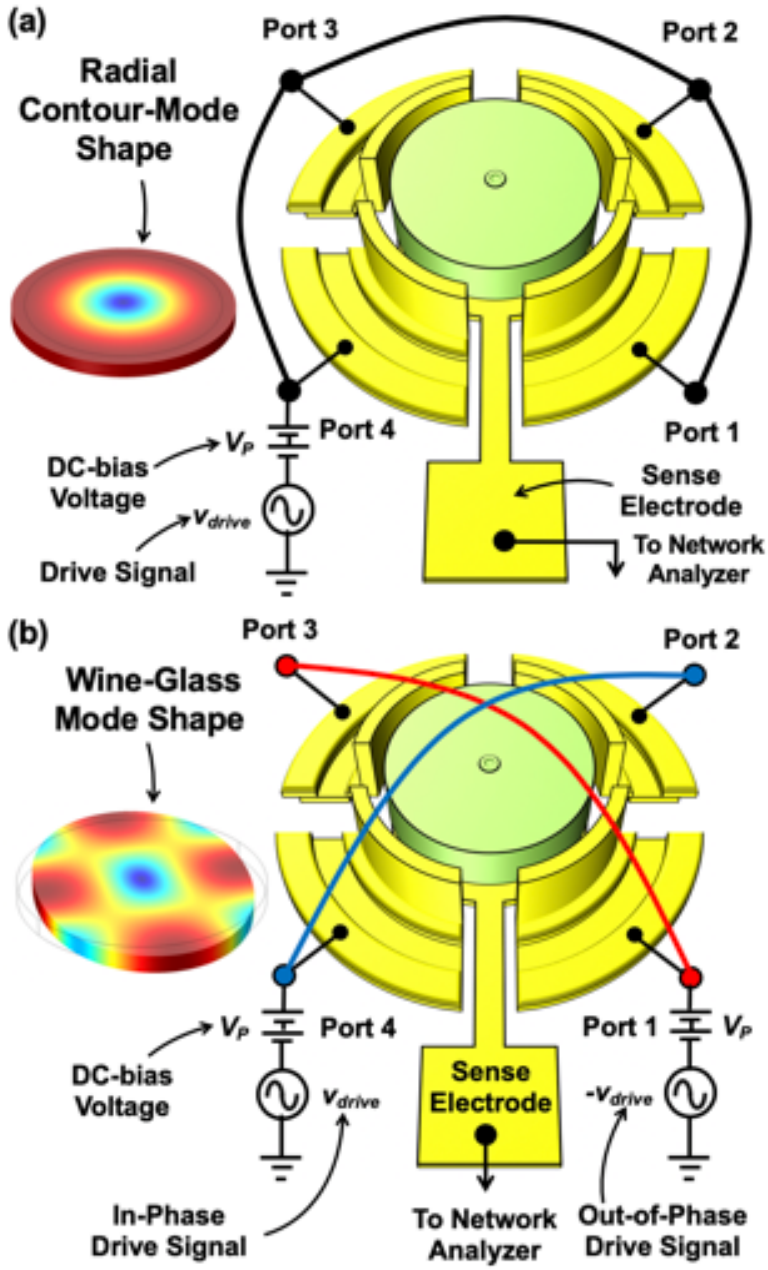


Fig. 3.3: Conventional disk resonator in a typical one-port drive and sense scheme for (a) the radial-contour mode. (b) wine-glass mode.

$$i_{out} = \left(V_P \frac{C_o}{d_o}\right)^2 \frac{Q v_{drive}}{\chi m_o \omega_o} \tag{3.1}$$

where Q is the quality factor, χ is a coefficient relating the actual mass to the dynamic mass (0.763 for a polysilicon radial-contour mode disk resonator with density ρ = 2300kg/m^3, Young's modulus E = 150GPa, and Poisson ratio σ = 0.476 [44]), m_o is the actual disk mass, and ω_o is the radian resonance frequency. Employing (3.1) for a 123-MHz radial-mode disk resonator design, with 20μm radius and 40nm gap, the typical output current with a Q of 20,000 is on the order of 18μA for a V_P and v_{drive} of 10V and 10mV, respectively, which generate a vibration amplitude of 1.11nm.

In the case of physically separated multiple output electrode designs, i.e., (θ_{i2} - θ_{i1}) < 90°, for increased functionality, electrically connecting all electrodes together and driving with a single source as seen in Fig. 3.3(a) would still excite the disk into the radial-contour mode, although with a reduced output current due to the transduction area lost between the physically separated electrodes.

As mentioned, the separated electrode design of Fig. 3.3(a) increases device functionality by allowing the excitation of other resonance modes where the displacement along the disk edge is not in-phase and circularly symmetric, i.e., wine-glass mode as shown in Fig. 3.2(d). Exciting this mode by utilizing the entire transduction area to maximize the electromechanical coupling strength with the device of Fig. 3.2(a), though, requires differential drive of the adjacent electrodes as indicated in Fig. 3.3(b). In addition, as opposed to the radial-contour mode, the wine-glass mode shape necessitates referencing the equivalent circuit variables not only to a certain radius on the disk, i.e., the disk edge $r = R$ in the radial-mode case, but also to a specific angle θ along the disk. Using the point at which the mode shape displacement is at a maximum, i.e., $\theta = \theta_{iref}$ and $r = R$, as shown in Fig. 3.2(a), the wine-glass mode χ parameter relating the effective mass m_m to the actual mass m_o turns out to be 0.360, which is less than half the radial-mode χ factor of 0.763 [44].

The resonance frequency expression of a disk like that shown in Fig. 3.2 takes on the form [44]

$$f_o = \frac{K_{mat}}{2R}\sqrt{\frac{E}{\rho}} \tag{3.2}$$

where R is the disk radius, and K_{mat} is a parameter dependent upon material properties and resonance mode shape. For polysilicon structural material, the radial-mode K_{mat} equals 0.654 whereas the wine-glass mode K_{mat} turns out to be 0.476 for the same geometric dimensions [44].

While electromechanical coupling is often gauged by the popular k_t^2 parameter, the ratio of the motional-to-static capacitance C_x/C_o of the device provides a more circuit-friendly representation of the same quantity, with a value that matches k_t^2 for most practical cases. Pursuant to obtaining an expression for the electromechanical coupling, the equivalent *RLC*-circuit parameters, i.e., the motional capacitance C_x, inductance L_x, and resistance R_x, take the form [44]

$$C_x = \frac{\eta_e^2}{k_m} = \frac{\eta_e^2}{\omega_o^2 \chi m_o} \tag{3.3}$$

$$L_x = \frac{m_m}{\eta_e^2} = \frac{\chi m_o}{\eta_e^2} \tag{3.4}$$

$$R_x = \frac{c_m}{\eta_e^2} = \frac{\chi m_o \omega_o}{Q \eta_e^2} \tag{3.5}$$

where k_m is the effective mechanical stiffness, c_m is the effective mechanical damping, and η_e is the electromechanical turns ratio given as

$$\eta_e = \sum_{i=1}^{n_{elec}} \eta_{ei} \tag{3.6}$$

where n_{elec} is the total number of electrodes used in transduction and η_{ei} is the turns ratio contributed by the i^{th} electrode port given as follows

$$\eta_{ei} = V_P \kappa_i \frac{C_{oi}}{d_o} = V_P \kappa_i \frac{\varepsilon_o H_d R(\theta_{i2} - \theta_{i1})}{d_o^2} \tag{3.7}$$

where ε_o is the free space permittivity, H_d is the disk thickness, θ_{i1} and θ_{i2} are the starting and ending electrode angles in radian, respectively, for the i^{th} port, and κ_i is the electromechanical turns ratio scaling factor expressed as [44]

$$\kappa_i = \frac{1}{(\theta_{i2} - \theta_{i1})} \int_{\theta_{i1}}^{\theta_{i2}} \frac{R_{mode}(R, \theta')}{R_{mode}(R, \theta)} d\theta' \tag{3.8}$$

where R_{mode} is the mode shape function and θ is the specific angle at which the equivalent circuit is referenced, i.e., $\theta = \theta_{iref}$ in Fig. 3.2(a). Note that for the fully surrounding single electrode case, the electrode coverage angle (θ_{i2} - θ_{i1}) equals 90° for each of the four electrodes.

As (3.6)-(3.8) indicate, being a linking parameter between mechanical and electrical domains, the electromechanical turns ratio η_e is subject to change due to the difference between the radial-contour and wine-glass mode shapes. In particular, although the scaling factor κ_i equals unity in the case of the radial-mode, it becomes smaller in the wine-glass case (once referenced to the maximum velocity point) accounting for the non-uniform displacement profile over the electrode length. With an electrode coverage angle (θ_{i2} - θ_{i1}) of approximately 80°, for example, (3.8) yields a κ_i of 0.724 for the wine-glass mode shape.

Substituting (3.6)-(3.8) into (3.3) and dividing by the overlap capacitance C_o given as

$$C_o = \sum_{i=1}^{n_{elec}} \frac{\varepsilon_o H_d R(\theta_{i2} - \theta_{i1})}{d_o} = \frac{\varepsilon_o H_d R n_{elec} \theta_{ov}}{d_o} \tag{3.9}$$

yields the C_x/C_o expression for a disk resonator in terms of mechanical and electrical design parameters

$$\frac{C_x}{C_o} = \frac{\eta_e^2}{\omega_o^2 \chi m_o C_o} = \left\{ n_{elec} \kappa^2 \frac{\theta_{ov}}{2\pi} \right\} \frac{2\varepsilon_o R V_P^2}{\pi^2 \chi K_{mat}^2 E d_o^3} \tag{3.10}$$

where the last expression in (3.9) assumes identical output electrodes with a coverage angle of θ_{ov}. Equation shows that for a given frequency a reduction in stiffness k_m generally implies a simultaneous reduction in mass m_o. In other words, to attain higher C_x/C_o, just remove mass.

3.3. Hollow Disk Resonators

This work reduces mass by simply hollowing out a solid disk resonator, then operating it in a largely radial or wine-glass mode. To illustrate, Fig. 3.4(a) compares a conventional disk resonator [83] with the hollow disk one demonstrated herein. The main difference between the two is the lack of material in the inner bulk of the latter device, essentially achieved by depositing less structural material. Here, the same sequence of surface-micromachining depositions as used in a conventional disk process [83], but with different thicknesses and etch ordering, achieves the desired hollow disk cross-section in Fig. 3.4(c).

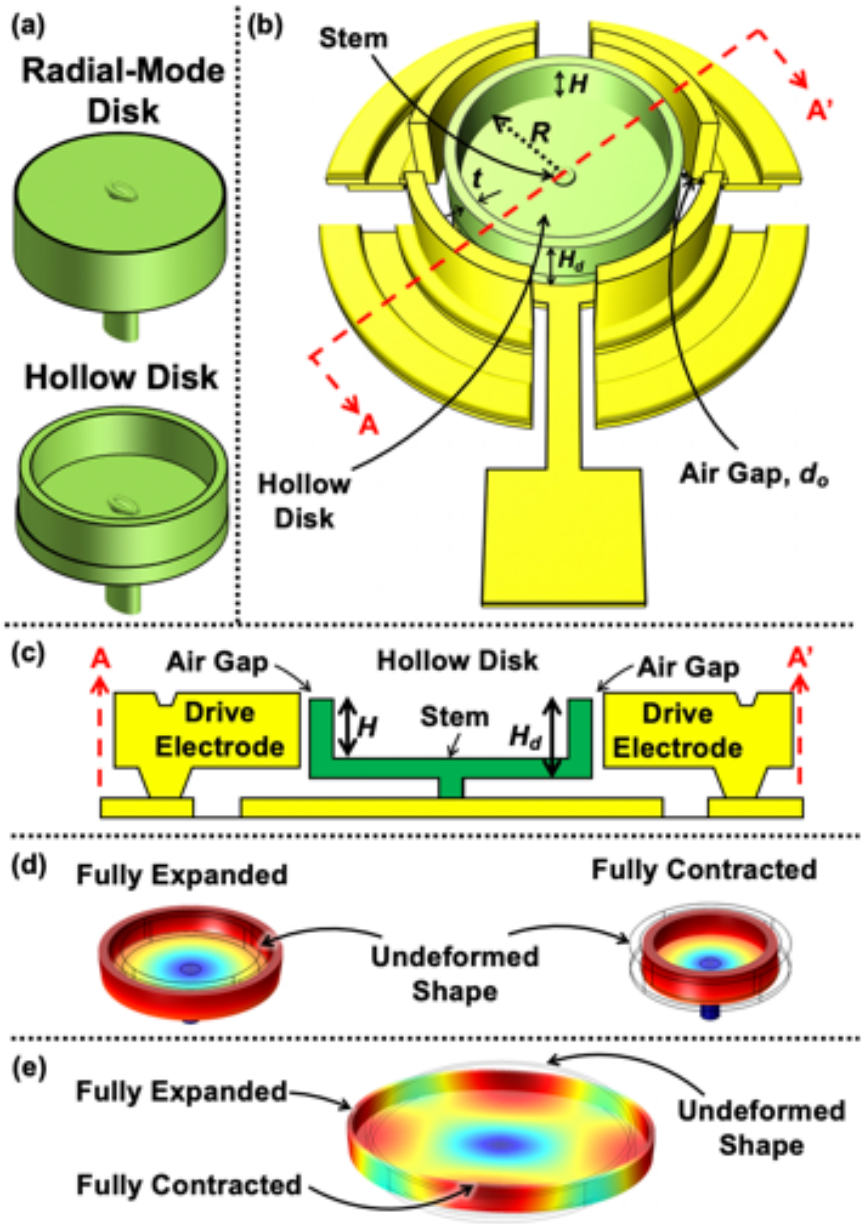


Fig. 3.4: Comparison of (a) a conventional disk resonator with (b) the hollow disk device described herein. (c) Cross-sectional view. (d) Vertically constrained FEA-simulated hollow disk radial-mode resonance shape. (e) Vertically constrained FEA-simulated hollow disk wine-glass mode resonance shape.

As shown in Fig. 3.4(b), this hollow disk resonator essentially combines a regular (but very thin) bottom disk of radius *R* with a high-aspect-ratio circular edge ring of width of *t* that provides more coupling to the electrodes. Mechanically, the bottom disk sets the stiffness, while the edge ring contributes additional mass, lowering the resonance frequency, which takes the form

$$f_{oh} = \left\{ \frac{K_{mat}}{2R} \sqrt{\frac{E}{\rho}} \right\} \frac{1}{\sqrt{1 + \Delta m / m_{mh}}} \tag{3.11}$$

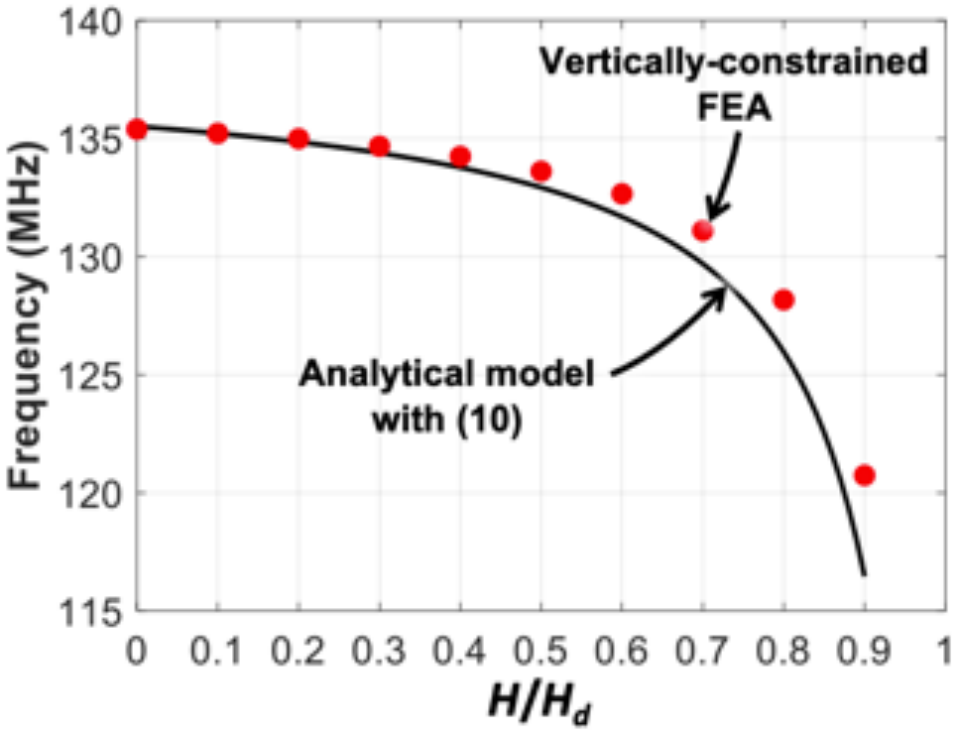


Fig. 3.5: Comparison of analytical model with (3.11) and vertically constrained FEA-simulated radial-contour mode resonance frequency for varying values of H/H_d.

where the term in the curly bracket is the resonance frequency of a disk as given in (3.2), m_{mh} and Δm are the equivalent dynamic disk mass at an edge location and the additional mass loading from the edge ring, respectively, given by

$$m_{mh} = \chi\rho\pi R^2(H_d - H)$$
$$\Delta m = \rho 2\pi RtH \tag{3.12}$$

Substituting (3.12) in (3.11) leads to

$$f_{oh} = \left\{\frac{K_{mat}}{2R}\sqrt{\frac{E}{\rho}}\right\}\left\{1 + \frac{2}{\chi}\frac{t}{R}\frac{H/H_d}{1 - H/H_d}\right\}^{-1/2} \tag{3.13}$$

The vertically-constrained finite element analysis (FEA)-simulated mode shape in Fig. 3.4 (d) does indeed resemble the mode shape of a conventional radial-contour mode disk with added mass near its edges, confirming the logic behind (3.13). Having the same resonance frequency expression with the radial mode, the analysis of (3.11)-(3.13) also holds for the wine-glass mode hollow disk resonator mode shape in Fig. 3.4(e). Fig. 3.5 further shows that the FEA simulation and the analytical expression in (3.13) agree well for varying ratios of H/H_d.

Following an approach similar to Section 3.2, the hollow disk motional capacitance C_{xh} and inductance L_{xh} take the form

$$C_{xh} = \left\{n_{elec}\kappa\frac{\theta_{ov}}{2\pi}\right\}^2 \frac{4\varepsilon_o^2 R^2 V_P^2 H_d}{\pi\chi K_{mat}^2 E d_o^4}\left\{\frac{1}{1 - H/H_d}\right\} \tag{3.14}$$

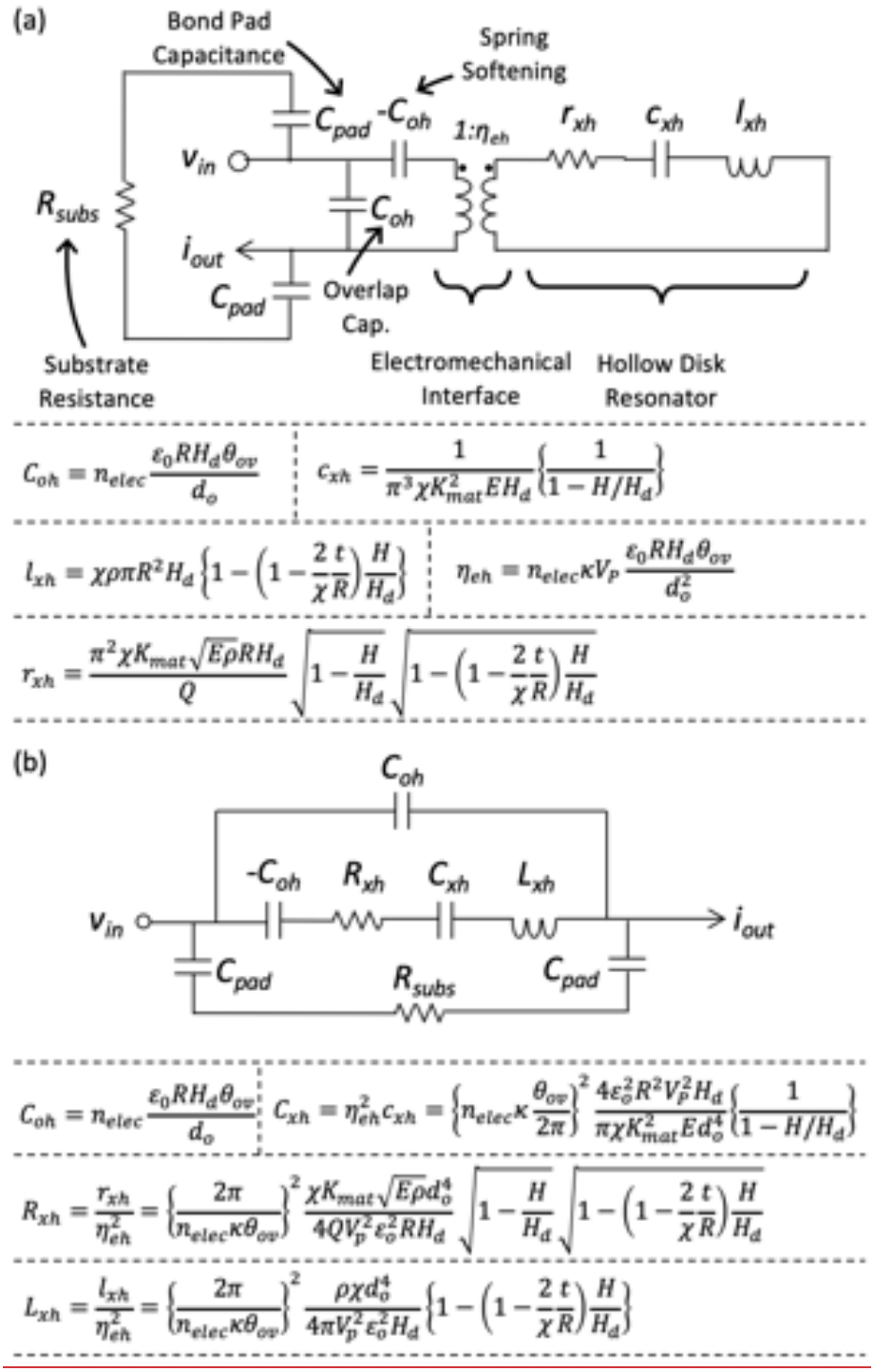


Fig. 3.6: (a) Transformer-based and (b) impedance-explicit equivalent circuits (including substrate parasitics) for a hollow disk resonator in a one-port drive and sense scheme.

$$L_{xh} = \left\{\frac{2\pi}{n_{elec}\kappa\theta_{ov}}\right\}^2 \frac{\rho\chi d_o^4}{4\pi V_p^2 \varepsilon_o^2 H_d}\left\{1-\left(1-\frac{2}{\chi}\frac{t}{R}\right)\frac{H}{H_d}\right\} \tag{3.15}$$

Using (3.14) in conjunction with the other equivalent circuit parameters summarized in Fig. 3.6 yields the following expression for the electromechanical coupling factor as gauged by C_{xh}/C_{oh}

$$\frac{C_{xh}}{C_{oh}} = \left\{n_{elec}\kappa^2 \frac{\theta_{ov}}{2\pi}\right\} \frac{2\varepsilon_o R V_P^2}{\pi^2 \chi K_{mat}^2 E d_o^3} \left\{\frac{1}{1 - H/H_d}\right\} \tag{3.16}$$

The first two terms in (3.16) are the C_x/C_o for a solid disk resonator, i.e., $H = 0$. The last term is always greater than 1, so provide a path towards larger electromechanical coupling via hollowing. In particular, this term is linearly proportional to the ratio of the hollow disk thickness H_d to the disk thickness (H_d -H) and offers a very convenient design knob.

Motional resistance R_x also benefits from hollowing out the disk structure as reduced mass leads to less mechanical damping, and hence less R_x for a given hollow disk electromechanical turns ratio η_{eh}. Expressing hollow disk motional resistance in terms of the design parameters given in Fig. 3.4 yields

$$R_{xh} = \left\{\frac{2\pi}{n_{elec}\kappa\theta_{ov}}\right\}^2 \frac{\chi K_{mat}\sqrt{E\rho}\, d_o^4}{4QV_p^2\varepsilon_o^2 R H_d} \sqrt{1 - \frac{H}{H_d}} \sqrt{1 - \left(1 - \frac{2}{\chi}\frac{t}{R}\right)\frac{H}{H_d}} \tag{3.17}$$

where Q is the quality factor.

3.4. Conventional vs. Hollow Disk Resonators in Radial Contour Mode

To better elucidate the benefits brought by the hollow disk, the following equations introduce C_x/C_o and R_x modification factors β_c and β_r, respectively, that simply indicate the ratio of the hollow disk C_x/C_o and R_x to those of the conventional disk.

$$\beta_c = \frac{C_{xh}/C_{oh}}{C_x/C_o} = \frac{1}{1 - H/H_d} \tag{3.18}$$

$$\beta_r = \frac{R_{xh}}{R_{xo}} = \sqrt{1 - \frac{H}{H_d}} \sqrt{1 - \left(1 - \frac{2}{\chi}\frac{t}{R}\right)\frac{H}{H_d}} \tag{3.19}$$

Here, $H/H_d = 0$ corresponds to the conventional disk and produces $\beta_c = \beta_r = 1$ upon substutition into (3.18) and (3.19), hence no improvement. With typical values of H_d = 3μm and H = 2.5μm corresponding to an H/H_d ratio of 0.83, however, the insets in Fig. 3.7 and Fig. 3.9 show 6 times increase in C_x/C_o and 6 times decrease in R_x using (3.18) and (3.19), respectively, implying that not only C_x/C_o but also R_x immensely benefits from the hollow disk structure. An even more aggressive design with H/H_d = 0.95 corresponding to a base disk thickness of 150nm for H_d = 3μm achieves almost 20 times improvement in C_x/C_o and R_x over its conventional counterpart.

Fig. 3.7 compares plots of C_x/C_o vs. H/H_d for 20-μm-radius conventional and hollow disks using (3.16) with V_P's of 5V, 10V, and 20V. The same C_x/C_o achieved by the H/H_d=0.91 hollow disk design with 5V and conventional disk with 20V suggests that hollow disk structure also facilitates low dc-bias operation which significantly improves the yield and reliability for RF-channel select narrow band micromechanical filters [80].

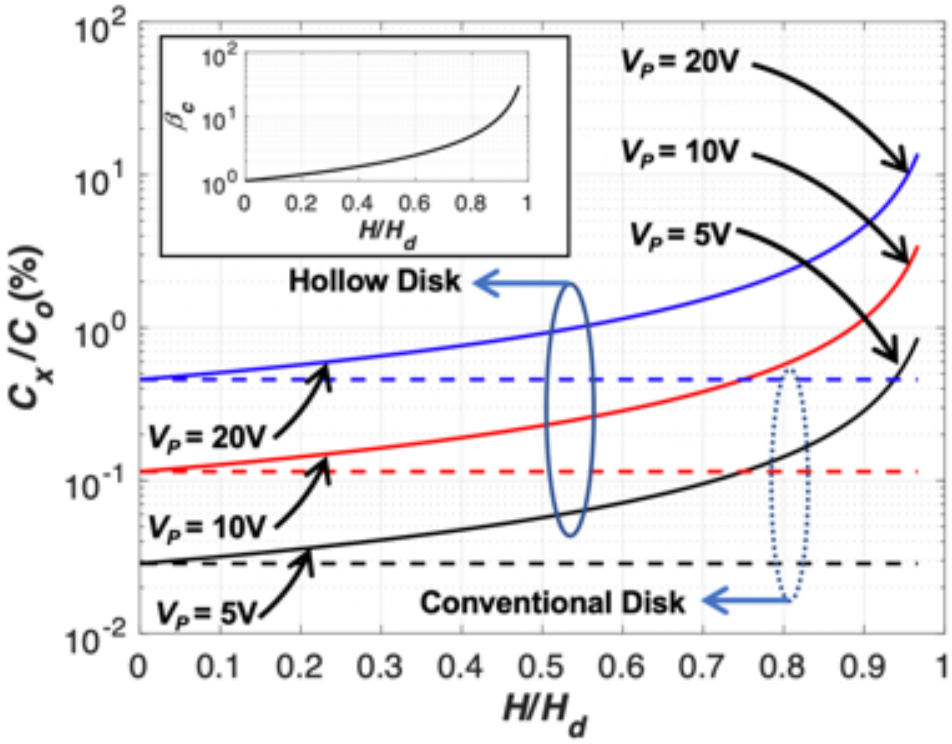


Fig. 3.7: Comparison of radial-mode conventional and hollow disk electromechanical coupling as gauged by C_x/C_o for varying values of H/h at different dc-bias voltages. Here the design parameters are: R=20µm, d_o=40nm, t=500nm, E=150GPa, ρ=2300kg/m^3, K_{mat}=0.654, and χ=0.763.

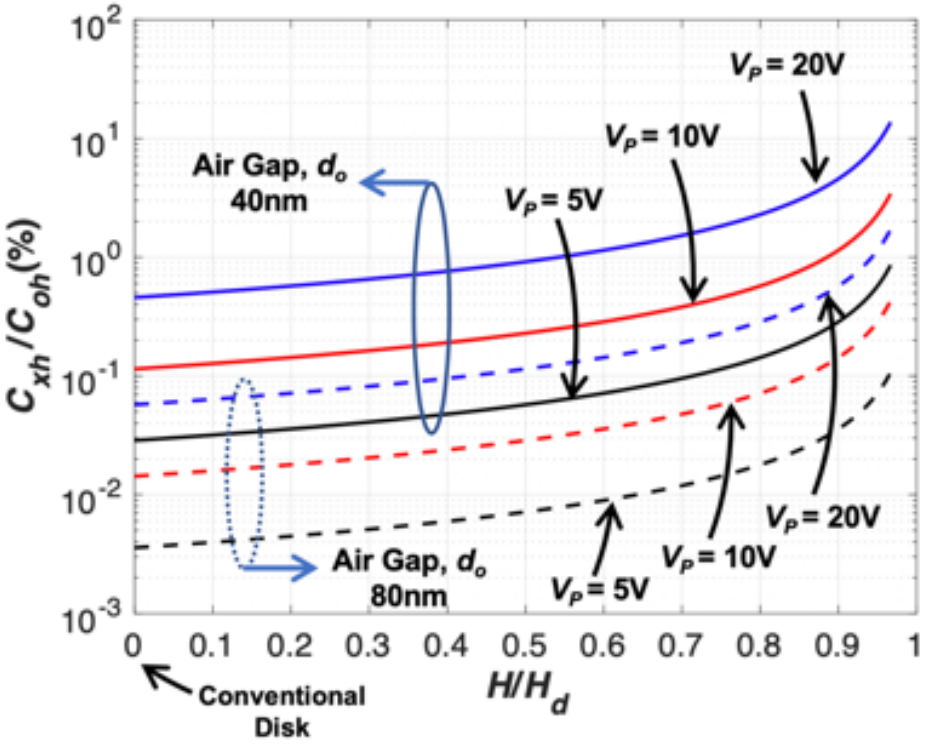


Fig. 3.8: Radial-mode hollow disk electromechanical coupling as gauged by C_x/C_o for varying values of H/H_d at different dc-bias voltages and with two different gap spacings. Here the design parameters are: R=20µm, t=500nm, E=150GPa, ρ=2300kg/m3, K_{mat}=0.654, and χ=0.763.

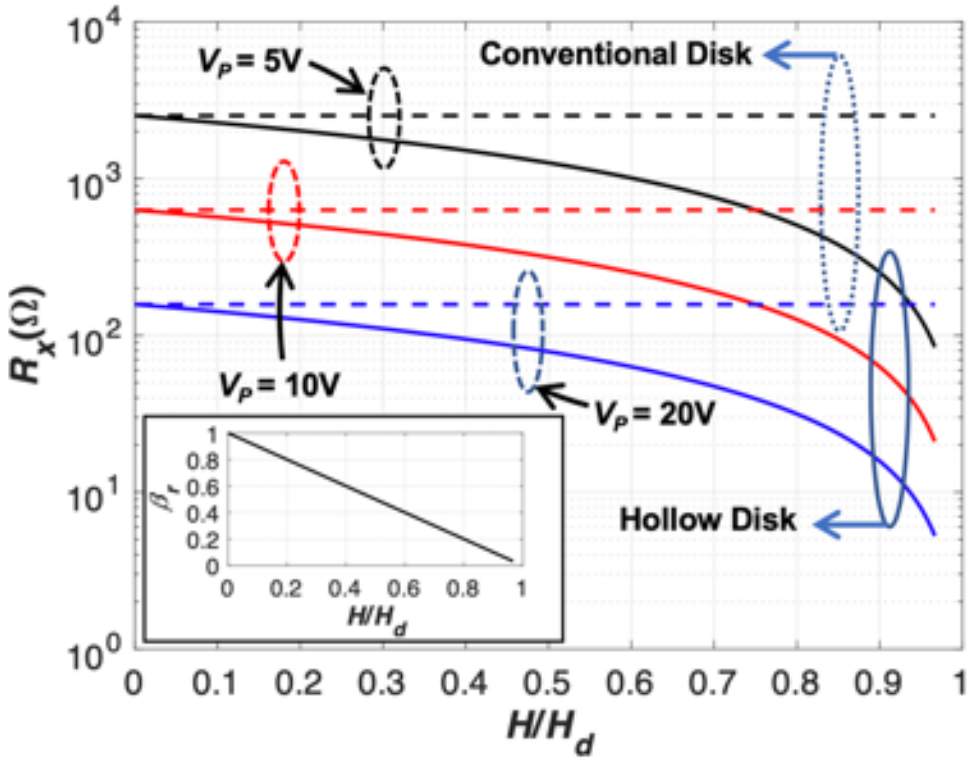


Fig. 3.9: Comparison of radial-mode conventional and hollow disk motional resistance for varying values of H/h at different dc-bias voltages. Here the design parameters are: R=20μm, d_o=40nm, Q=20,000, H_d=3μm, t=500nm, E=150GPa, ρ=2300kg/m^3, K_{mat}=0.654, and χ=0.763.

Fig. 3.8 makes similar plots for the hollow disk resonator for two different gap spacings, i.e., 40nm and 80nm. Although gap spacing is the most efficient knob to effect C_x/C_o due to its inverse third power dependence, small gap devices require meticulous process optimization to avoid low voltage pull-in and low yield [45], [68]. Where such an optimization is not desirable or possible, Fig. 3.8 shows that the most-aggressive design of H/H_d = 0.85 with 80nm gap yields the same C_x/C_o with that of a conventional disk of 40nm gap at the same voltage, hence providing another route to increase the electromechanical coupling of capacitive-gap resonators without sacrificing fabrication yield.

Fig. 3.9 compares motional resistances achieved by a hollow disk and conventional solid design at different dc-bias voltages for varying H/H_d ratios. For a typical value of H/H_d = 0.83, the hollow disk design achieves 5 times smaller motional resistance than its conventional counterpart.

Finally, Table 3.I summarizes the equivalent circuit element values of Fig. 3.6 along with the resonance frequency and C_x/C_o for hollow disk designs with different H/H_d ratios.

3.5. Device Fabrication

The fabrication process starts with successive depositions of 2μm-thick low temperature oxide (LTO) at 450°C and 500nm-thick low stress nitride at 835°C, both via low-pressure chemical vapor deposition (LPCVD), to serve as isolation layers over a lightly doped p-type silicon starting wafer. LPCVD polycrystalline silicon then follows at 590°C for 8 hours to achieve a 3μm-thick interconnect layer film, subsequently doped in a $POCl_3$ furnace for 1 hour at 1050°C. After patterning photoresist with a first mask, deep reactive ion etching (DRIE) using an SF_6 chemistry

TABLE 3.I: HOLLOW DISK EQUIVALENT CIRCUIT ELEMENT VALUES WITH DIFFERENT H/H_D RATIOS

H/H_d (-)	f_o (MHz)	R_{xh} (Ω)	L_{xh} (mH)	C_{xh} (fF)	C_{oh} (fF)	C_{xh}/C_{oh} (%)
0	135.51	4,637	12.4	0.11	90.12	0.12
0.1	135.22	4,183	11.2	0.12	90.12	0.14
0.2	134.85	3,728	9.99	0.14	90.12	0.15
0.3	134.39	3,273	8.80	0.16	90.12	0.18
0.4	133.77	2,819	7.62	0.19	90.12	0.21
0.5	132.93	2,364	6.43	0.22	90.12	0.25
0.6	131.69	1,909	5.24	0.28	90.12	0.31
0.7	129.69	1,454	4.05	0.37	90.12	0.41
0.8	125.97	998	2.86	0.56	90.12	0.62
0.9	116.46	540	1.67	1.12	90.12	1.24

delineates the interconnect layer as depicted in Fig. 3.10(a). Planarization then follows via deposition of 4μm-thick phospho-silicate glass (PSG), re-flow of PSG at 950ºC for 30min, and chemical mechanical polishing (CMP) down to the polysilicon to leave a flat surface that facilitates subsequent processing.

Hollow device fabrication then begins with a 500nm PSG deposition at 450ºC to serve as a bottom sacrificial spacer between the structural and interconnect layers as well as an additional dopant source to further reduce the sheet resistance of the interconnect traces. Next, lithography through a second mask delineates the stem hole and reactive ion etching (RIE) using an Ar:CHF_3:CF_4 chemistry opens it, as shown in Fig. 3.10(b).

At this point, the hollow disk fabrication deviates from the conventional solid disk process flow. Instead of depositing a thick layer of structural polysilicon, e.g. 3μm, the current process uses a much thinner 500nm-thick LPCVD polysilicon at 590°C followed by a 2.5μm-thick LTO deposition at 450°C. This polysilicon serves as material for the bottom disk structure while also filling the stem hole to form the stem. Lithography then delineates the disk edges and RIE using an Ar:CHF_3:CF_4 chemistry cuts through the oxide to form a mold to define the eventual hollow disk structure. The oxide also serves as a hard mask for the subsequent structural polysilicon etch, which uses a Lam TCP 9400SE polysilicon RIE etch recipe with gas flow rates of 150sccm of HBr, 4sccm of Cl_2, and 1sccm of O_2 at 12mTorr pressure with 250W and 55W RF and wafer bias powers, respectively. At this point, the cross section is as in Fig. 3.10(c).

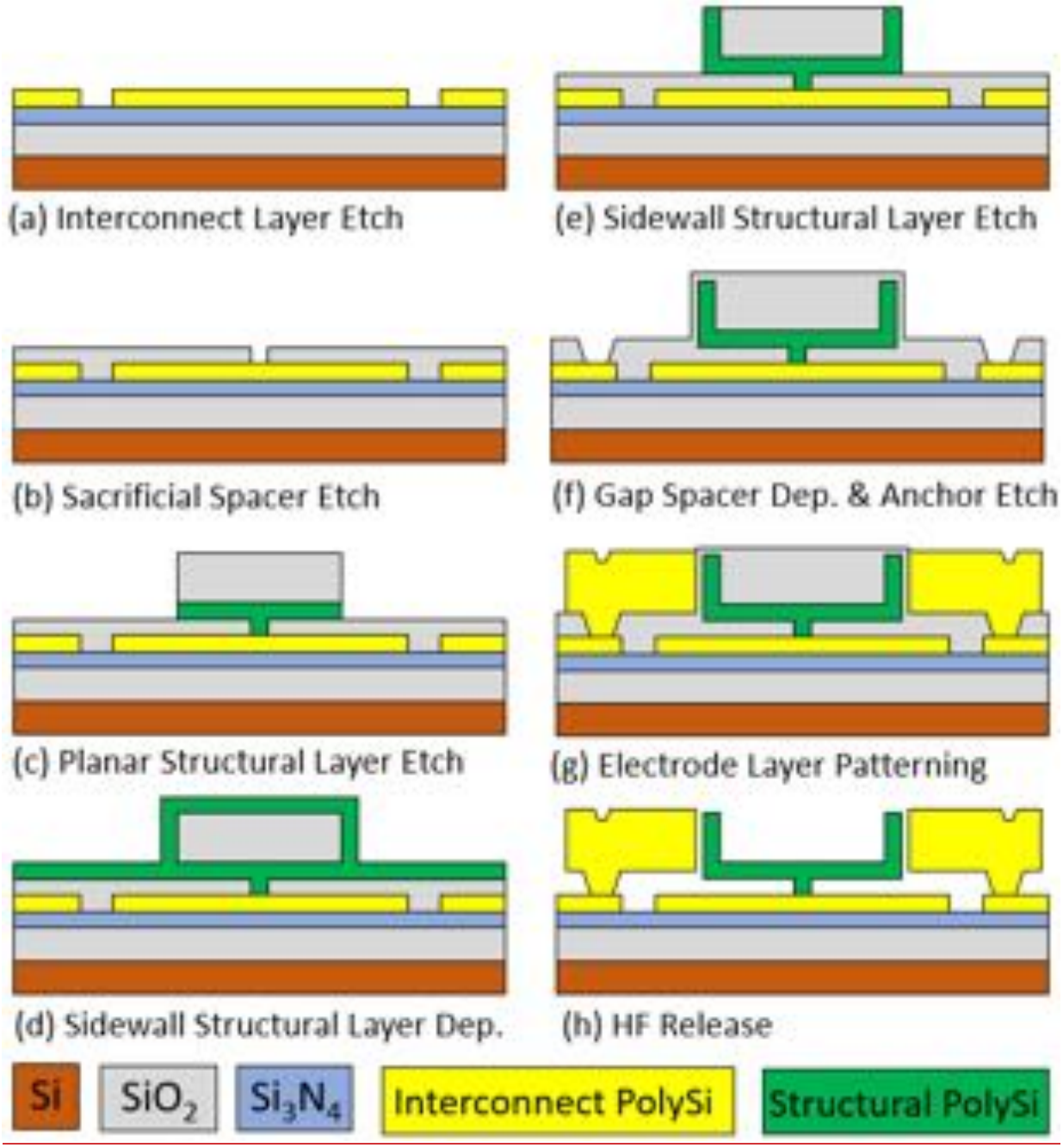


Fig. 3.10: Cross-sections describing the polysilicon hollow disk fabrication process flow after (a) patterning polysilicon interconnect layer; (b) planarizing the surface with CMP and etching stem holes; (c) depositing and patterning structural polysilicon and its oxide hard mask; (d) conformally depositing polysilicon; (e) blanket etching polysilicon to define edge-ring; (f) depositing sidewall sacrificial layer and etching anchor openings; (g) depositing and patterning electrode polysilicon layer; and (h) releasing the structure in HF. Note that Appendix A provides a detailed step-by-step process traveler.

Next, conformal deposition of 500nm LPCVD polysilicon at 590°C and blanket etching form the sidewall structural layer as shown in Fig. 3.10(d) and (e). LPCVD of high temperature oxide (HTO) at 930°C using 60sccm of dichlorosilane (DCS) and 180sccm of N_2O flow with 400mTorr

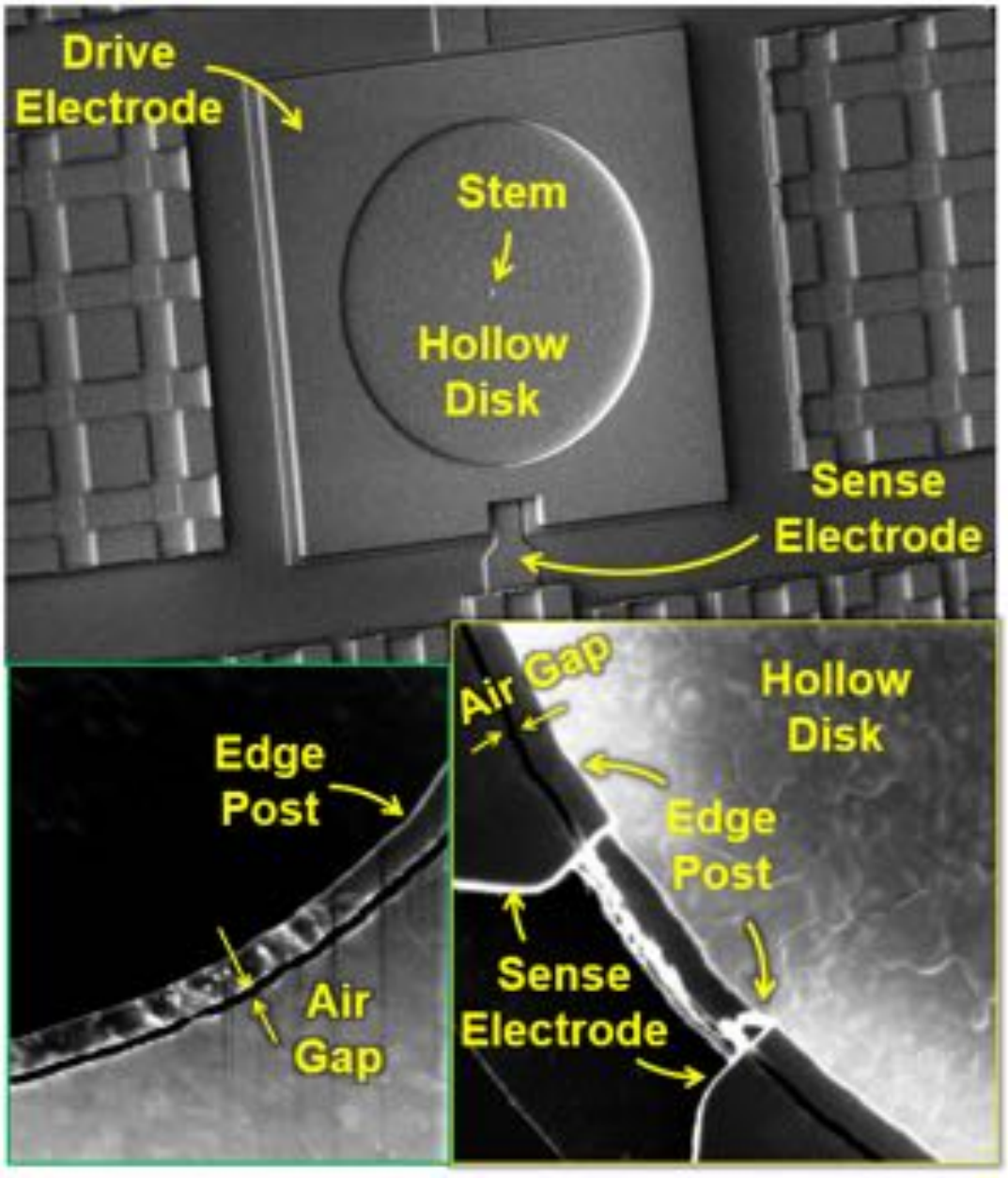


Fig. 3.11: Wide-view and zoom-in SEM's of a fabricated polysilicon hollow disk resonator.

process pressure deposits the sidewall sacrificial oxide that defines the eventual 37nm electrode-to-resonator gap. Lithography followed by an Ar:CHF_3:CF_4 RIE etches electrode anchor openings to yield the cross-section of Fig. 3.10(f). After a blanket LPCVD deposition of 3μm-thick polysilicon for 8 hours and $POCL_3$ doping for 1 hour at 590°C and 950°C, respectively, the final lithography and DRIE using an SF_6 chemistry steps define the electrodes and yield the cross-section in Fig. 3.10(g), which is ready for release. The release process employs 49% liquid HF to free the disk structure and achieve the final cross-section of Fig. 3.10(h). Note that Appendix A provides a detailed step-by-step process traveler.

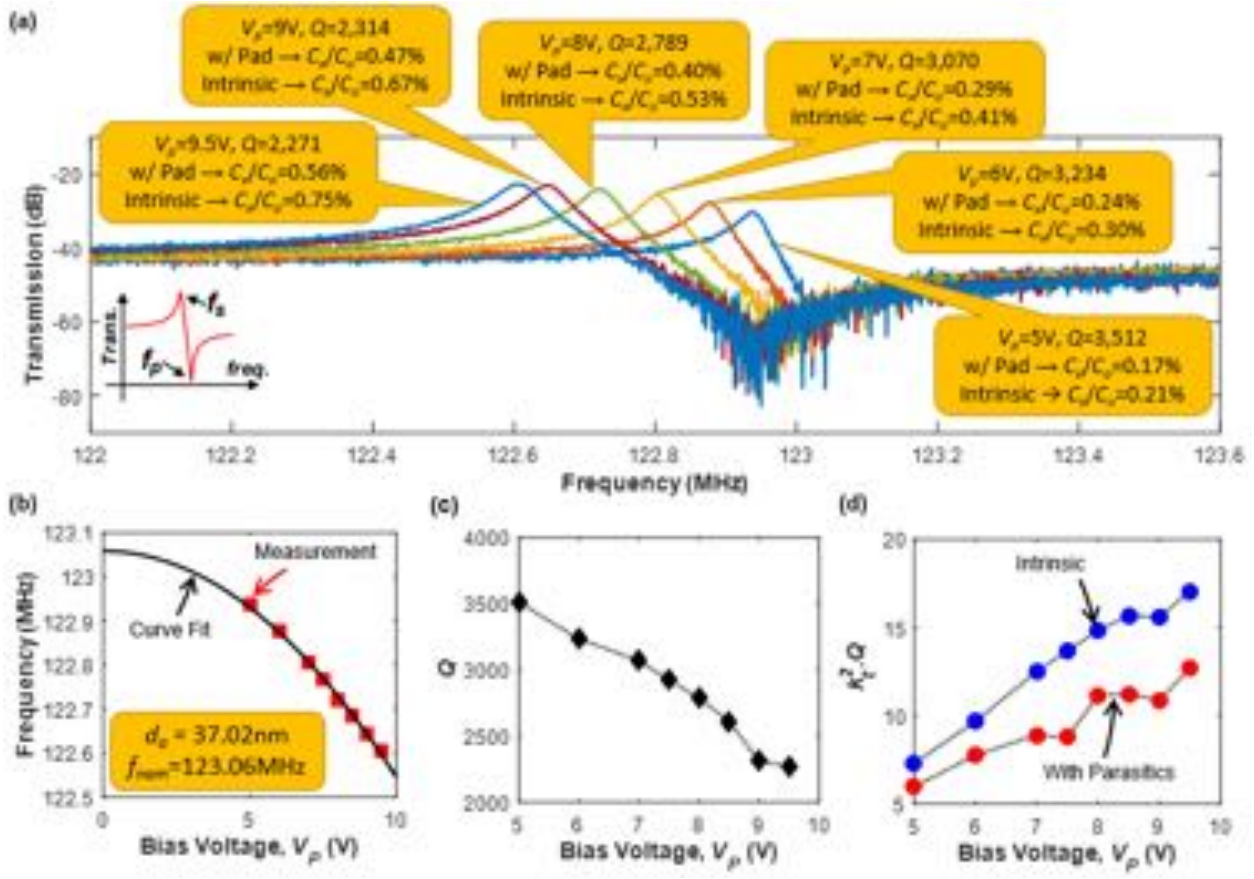


Fig. 3.12: a) Measured frequency response curves for a 123-MHz radial contour mode hollow disk resonator as a function of dc bias voltage along with C_x/C_o values extracted via (3.21) and (3.26). (b) Resonance frequency f_o plotted against dc-bias voltage V_P. (c) Quality factor measurement for varying dc-bias voltages V_P. (d) Electromechanical coupling strength C_x/C_o (or k_t^2) times quality factor figure of merit (FOM) plotted against dc-bias voltage V_P with and without parasitics.

Fig. 3.11 presents the SEM image of a fabricated and released hollow disk resonator with zoom-in's on the edge ring, gap, and overlapping I/O electrodes. Table 3.II summarizes its design and performance under various operating conditions, e.g., voltages.

3.6. Measurement Results

A Lakeshore FWPX Vacuum Probe Station housing hollow disk resonators maintained a vacuum pressure of 50μTorr during testing. Probes accessed the devices, delivering the excitation signal and sensing their output currents, which they directed to the 50Ω input terminal of a sense amplifier, then to the input of an Agilent E5071C vector network analyzer.

Fig. 3.12(a) presents measured frequency response curves for a 123-MHz hollow disk resonator at various dc-bias voltages V_P under 50μTorr vacuum with R=20μm, H_d=3μm, H=2.5μm, t=500nm, and stem radius R_s=1μm. Here, as Fig. 3.12(b) depicts, a curve-fitting method using resonant frequency versus dc-bias voltage data of Fig. 3.12(a) accurately extracts the electrode-to-edge ring gap d_o and nominal resonant frequency f_{nom} as 37.02nm and 123.06MHz, respectively [44].

A. Electromechanical Coupling Strength, C_x/C_o

A very common approach to measuring electromechanical coupling strength C_x/C_o employs parallel and series resonance frequencies, f_p and f_s as indicated in Fig. 3.12(a), respectively. Ignoring (for now) the parasitic bond pad capacitances C_{pad} in Fig. 3.6(b) and solving for the input impedance yields

$$f_s = \frac{1}{2\pi\sqrt{L_x(C_x//-C_o)}}, f_p = \frac{1}{2\pi\sqrt{L_x C_x}} \tag{3.20}$$

Here, the parallel resonance occurs at the nominal resonance frequency f_{nom} and electrical stiffness [84] pulls the series resonant frequency down, separating the two frequencies. Rearranging the expressions in (3.20) and isolating C_x/C_o yields

$$\frac{C_x}{C_o} = 1 - \left(\frac{f_s}{f_p}\right)^2 \tag{3.21}$$

Using (3.21) directly on the Fig. 3.12 data, C_x/C_o values rise from 0.17% at V_P=5V to 0.56% at V_P=9.5V, the latter of which is 5 times larger than the 0.11% expected for a 3-μm-thick conventional solid radial-contour mode disk with the same gaps and bias voltage. The benefits to filter performance are clear from Fig. 3.1.

As previously mentioned, however, (3.21) yields the intrinsic device C_x/C_o only if parasitic capacitances are negligible compared with the overlap shunt capacitance C_o. In other words, it works well only when the device feedthrough capacitance is large, which is the case for most piezoelectric resonators. As explained in [74], capacitive-gap transducers generally have much smaller C_o than piezoelectric ones, which can be problematic when the MEMS-to-transistor interface has large shunt capacitance, but for small interface capacitance permits substantially lower power operation.

Given that the present hollow disk device is capacitive-gap transduced, the bond pads shown in Fig. 3.6(b) incur parasitic capacitances C_{pad} comparable with the device's overlap shunt capacitance C_o. For example, a 60μm × 60μm bond pad alone has 54.9fF of shunt capacitance C_{pad} through the 500nm nitride and 2μm oxide layers, while the overlap capacitance C_o for the device measured in Fig. 3.12(a) is 90.2fF. In this case, use of (3.21) yields not the intrinsic C_x/C_o of the device in question, but rather the C_{pad}-loaded value (which of course is a useful quantity in itself).

To extract out the intrinsic C_x/C_o, one can re-derive it, but this time considering the bond pad capacitors in Fig. 3.6(b) and noting that the substrate resistance R_{subs} connecting them has comparably negligible impedance at the frequency of operation, i.e., 123MHz. Doing so, the expressions for the parasitic-encumbered parallel and series resonance frequencies become

$$f_s{}' = \frac{1}{2\pi\sqrt{L_x(C_x//-C_o)}}$$
$$f_p{}' = \frac{1}{2\pi\sqrt{L_x C_x \dfrac{2C_o + C_{pad}}{2C_o + C_{pad}(1 - C_x/C_o)}}} \tag{3.22}$$

TABLE 3.II: HOLLOW DISK PERFORMANCE UNDER VARIOUS DC-BIAS VOLTAGES

V_P (V)	f_o (MHz)	C_x/C_o (%)	Q	k_t^2-Q
5	122.9365	0.21	3,512	7.3
6	122.8755	0.30	3,234	9.7
7	122.8055	0.41	3,070	12.5
7.5	122.7665	0.47	2,923	13.7
8	122.7205	0.53	2,789	14.8
8.5	122.6845	0.60	2,610	15.7
9	122.6435	0.67	2,314	15.6
9.5	122.6055	0.75	2,271	17.0

With the inclusion of parasitics, the parallel resonance dip slightly shifts to the left, whereas the series resonant frequency behaves as for the case without parasitics. Rearranging (3.22) and expressing C_x/C_o in terms of the parasitic-encumbered parallel and series resonance frequencies, f_p' and f_s', yields

$$\frac{C_x}{C_o} = \alpha \frac{2C_o + C_{pad}}{2C_o + \alpha C_{pad}} \; where \; \alpha = 1 - \left(\frac{f_s'}{f_p'}\right)^2 \tag{3.23}$$

Using (3.23) with C_{pad} =54.9fF, C_o=90.2fF, and V_P=9.5V curve in Fig. 3.12(a) produces an intrinsic C_x/C_o value of 0.72%, which is substantially better than 0.56% obtained via (3.21).

Although (3.23) provides invaluable insight into the effect of parasitics on electromechanical coupling strength, accurately calculating C_{pad} is not a straightforward task. A more direct method to extract C_x/C_o would be better.

Interestingly, the expressions for series resonance frequency in (3.20) and (3.22) are identical. This suggests that series resonance frequency is impervious to bond pad parasitics, hence might be a better starting point to determine C_x/C_o. As depicted in Fig. 3.12(b), this frequency f_o is a strong function of dc-bias voltage V_P, mainly due to electrical stiffness, which influences it according to [84]

$$f_o = f_{nom}\sqrt{1 - \frac{k_e}{k_m}} = f_{nom}\sqrt{1 - \frac{C_x}{C_o}} \tag{3.24}$$

where f_{nom} is nominal (i.e., zero bias) resonance frequency, k_e and k_m are the electrical and mechanical stiffnesses, respectively, which take the form

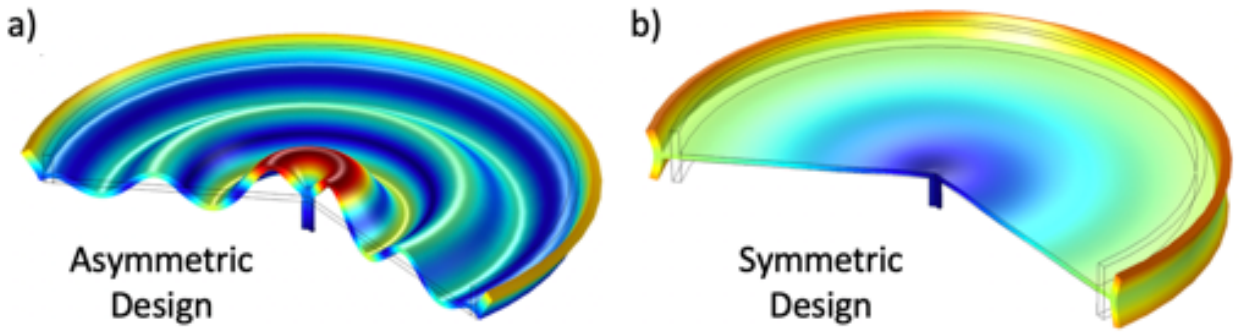


Fig. 3.13: Finite-element simulated mode shape for the hollow disk resonator (a) similar to that of Fig. 3.2(d), but this time without vertical motion constraints. The simulation clearly shows transverse (vertical) displacements that likely radiate energy into the stem anchor and subsequently to the substrate. (b) with a top-to-bottom symmetric structure showing the energy dissipation through the anchor significantly reduces and the mode shape very much resembles to that of a solid disk.

TABLE 3.III: COMPARISON CHART WITH OTHER TECHNOLOGIES

Ref.	***f_o* (MHz)**	***C_x/C_o* (%)**	***R_x* (Ω)**	***Q***	***k_t^2-Q***	***Area* (μm²)**
[85]	85	0.86	125	2,100	18	10,000
[86]	149	0.48	460	10,000	48	21,200
[45]	60	1.62	54	29,640	480	3,200
This Work	123	0.75	1,250	2,271	17	1,600

$$k_e = \frac{\eta_e^2}{C_o}\,, k_m = \frac{\eta_e^2}{C_x} \tag{3.25}$$

and where manipulation of (3.25) shows that $(k_e/k_m) = (C_x/C_o)$. Rearrangement of (3.24) yields an alternate C_x/C_o expression

$$\frac{C_x}{C_o} = 1 - \left(\frac{f_o}{f_{nom}}\right)^2 \tag{3.26}$$

which now provides the intrinsic device electromechanical coupling strength even in the presence of bond pad (or other) parasitics. Note that the curve-fitting method used to extract the electrode-to-edge ring gap d_o in Fig. 3.12(b) also extracts f_{nom}.

Now using (3.26), C_x/C_o values rise from 0.21% at V_P=5V to 0.75% at V_P=9.5V, the latter of which is almost 7 times larger than the 0.11% for a conventional solid radial-contour mode disk with the same gaps.

B. Quality Factor, Q

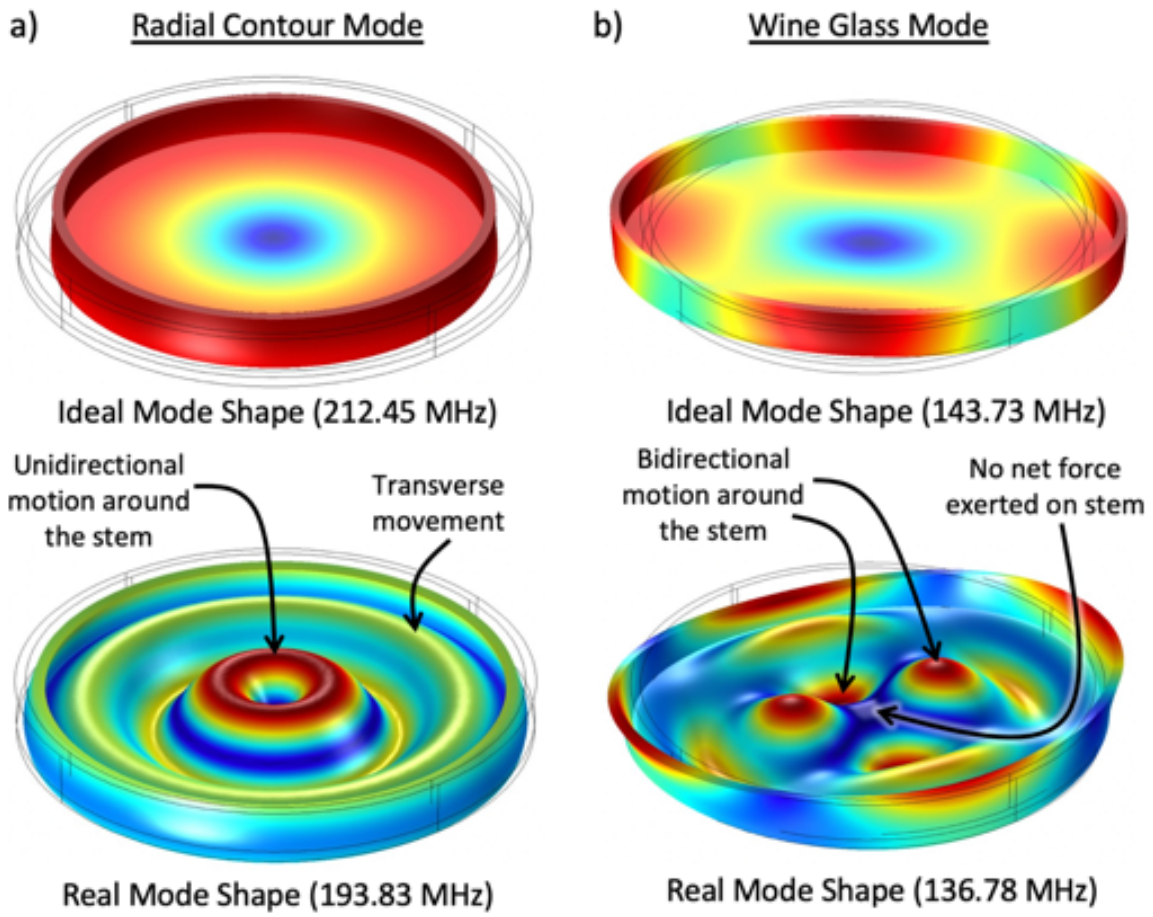


Fig. 3.14: Finite-element simulated mode shape for the hollow disk resonator (a) in radial contour mode. The top figure shows the ideal mode shape simulated by constraining vertical motion. The bottom figure depicts the real mode shape without any motional constraints, indicating clear transverse motion near the disk stem hence more anchor loss. (b) in wine glass mode. The top figure shows the ideal mode shape simulated by constraining vertical motion. The bottom figure depicts the real mode shape without any motional constraints where the out-of-phase movement of the adjacent quadrants of the base disk leaves the stem motionless substantially improving the quality factor compared to the radial contour mode of (a).

Fig. 3.12(c) plots quality factor Q at various dc-bias voltages. The measured Q of 2,271 at V_P=9.5V is well short of the >10,000 often seen for capacitive-gap transduced polysilicon devices. High film electrical resistance could be one cause of this. The problem could also stem from larger surface loss mechanisms, given the higher surface-to-volume ratio of this device.

On the other hand, anchor loss is another likely reason for lower than expected Q. In particular, lifting the vertical constraint of the finite-element mode shape simulations Fig. 3.4(d) yields that in Fig. 3.13(a), which clearly shows transverse (vertical) displacements that likely radiate energy into the stem anchor and subsequently to the substrate. A more symmetric design as in Fig. 3.13(b), with edge rings both above and below the thin disk structure, is one solution to this problem.

Even with these Q issues, the k_t^2-Q value of 17 as plotted in Fig. 3.12(d) for this resonator is decent compared with some of the best piezoelectric alternatives in Table 3.III. The 480 achieved by the 13-nm-gap capacitive-gap transduced device of [45] remains a target to match.

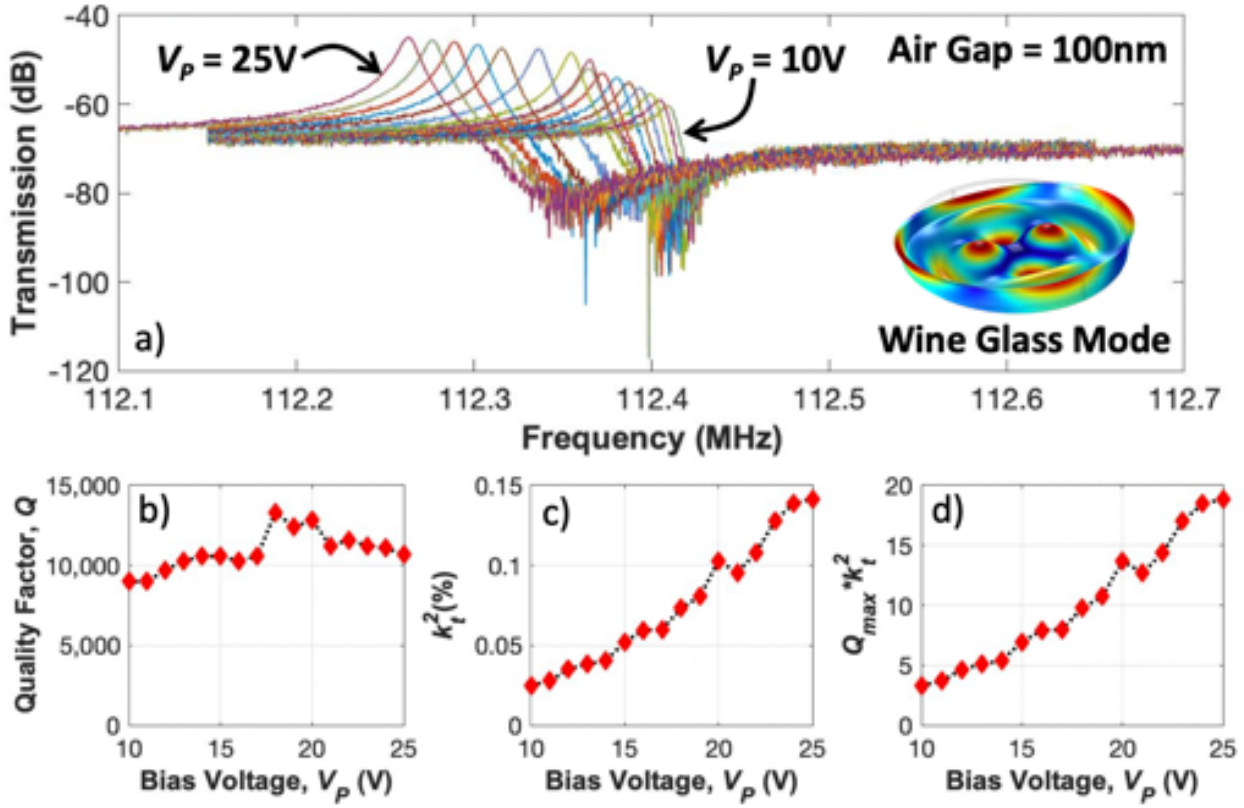


Fig. 3.15: a) Measured frequency response curves for a 112-MHz wine glass mode hollow disk resonator as a function of dc bias voltage. (c) Quality factor measurement for varying dc-bias voltages V_P. (c) Electromechanical coupling strength C_x/C_o (or k_t^2) against dc-bias voltage V_P. (d) Electromechanical coupling strength C_x/C_o (or k_t^2) times quality factor figure of merit (FOM) plotted against dc-bias voltage V_P.

Interestingly, a more convenient solution to recover high-Q's, i.e. >10,000, without altering the fabrication process is to dispense with the radial contour mode and switch to the wine glass mode. As shown in Fig. 3.14(b), the hollow disk transverse motion in the wine glass mode shape is out-of-phase in adjacent quadrants around the disk center effectively exerting no net force on the stem hence not radiating significant energy to the substrate as opposed to the unidirectional motion in the radial contour mode shape of Fig. 3.14(a) which is the main culprit behind the Q-degradation as mentioned before. To this end, Fig. 3.15(a) presents measured curves around 112MHz for a hollow disk resonator with a radius of 16μm and actuation gap of 100nm in the wine glass mode for varying dc-bias voltages. Here, the measured wine glass Q of 13,317 at 112MHz in Fig. 3.15(b) is more than 6 times better than 2,217 of the radial contour mode at 123MHz in Fig. 3.12(c).

Fig. 3.15(c) plots the electromechanical coupling factor, C_x/C_o calculated using (3.21) against dc-bias voltage V_P. At first glance, the measured C_x/C_o of 0.15% with a 25V dc-bias voltage might seem to be low compared to 0.56% with a 9.5V dc-bias of the radial contour mode in Fig. 3.12(a). However, considering that the devices of Fig. 3.15 and Fig. 3.12 possess different actuation gaps, i.e. compare gaps of 100nm and 40nm, respectively, and the electromechanical coupling coefficient dependence on the gap is inverse cubic as given in (3.16), a fair comparison is only possible if one scales the C_x/C_o measurement of Fig. 3.15 with 10V dc-bias to the 40nm-gap case. Performing such a scaling generates a C_x/C_o of 0.39% which is still slightly lower than 0.56% of the radial

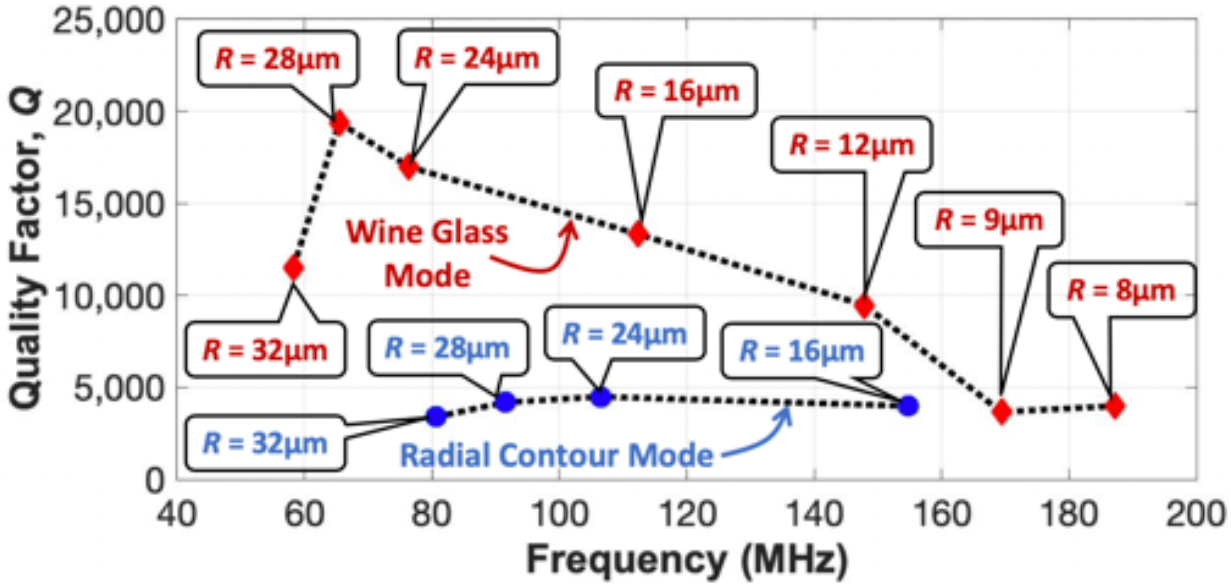


Fig. 3.16: Measured quality factors of hollow disk resonators in radial contour and wine glass modes at varying frequencies. Note that the plot also indicates the disk radius for each of the measured devices.

contour mode, however with 6 times larger Q. Fig. 3.15(d) plots the $(C_x/C_o \bullet Q)$ figure of merit (FOM) where the scaled wine glass mode FOM with a 10V dc-bias voltage for a 40nm actuation gap would be 52.02, which is more than 3 times larger than that of the radial contour mode device.

Finally, Fig. 3.16 presents measured quality factors of hollow disk resonators at varying frequencies in the radial contour and the wine glass mode shapes of Fig. 3.14. It is clear from Fig. 3.16 that the wine glass mode Q is 2-4 times better than that of the radial contour mode in the entire measurement range up to 150MHz. Note that above 160MHz, no radial contour mode quality factor measurement data is available since the device Q is too low and the feedthrough signal swamps the device response.

3.7. Conclusions

The hollowing-based increase in C_x/C_o to 0.75% at 123 MHz is impressive, given that it does not require gap scaling. When combined with gap scaling, some very large C_x/C_o values might soon be possible. Combined with the Q's in the 3,000 range, such C_x/C_o's could enable both narrow- and wide-band front-end filters for communications in this technology.

Reasonable expectation that the Q of hollow resonator devices will increase to a value more appropriate for capacitive-gap transduced resonators, e.g., 20,000 with a symmetric design, might eventually allow 40-nm-gap k_t^2-Q values on the order of 150, which begins to approach the enormous value posted by 13-nm-gap device of [45]. If this happens, then some very capable narrow-band filters and very low power, low noise oscillators might be in range for future renditions of this technology.

Chapter 4
On-Chip Precision Residual Strain Diagnostic Based on Gap-Dependent Electrical Stiffness

This chapter presents an on-chip strain measurement device that harnesses precision frequency measurement to precisely extract sub-nm displacements, allowing it to determine the residual strain in a given structural film with best-in-class accuracy, where stress as small as 15MPa corresponds to 2.9nm of displacement. The approach specifically harnesses a spoke-supported ring structure (*cf.* Fig. 4.1) surrounded both inside and outside by balanced capacitive-gap transducers that pull its resonance frequency according to strain-induced changes in inner and outer electrode-to-structure gap spacing. The use of a ring structure with balanced electrodes further eliminates uncertainty in the starting gap spacing, which in turn enhances accuracy. The importance of attaining such accuracy manifests in the fact that knowledge of residual strain might be the single most important constraint on the complexity of large mechanical circuits, such as the mechanical filter of [79].

4.1. Introduction

Recent demonstrations of sub-20nm electrode-to-resonator gaps have permitted capacitive-gap transducer electromechanical coupling strengths well past those posted by alternatives in the high (HF) to very high frequency (VHF) range, with C_x/C_o's up to 71% at 10-MHz [68] and 1.62% at 60-MHz [45]. These compare quite favorably with the 0.86% of alternatives [85], all while preserving comparatively larger Q's, e.g., 30000 versus 2100. Unfortunately, such performance comes with a price—in this case, greater susceptibility to stress. Indeed, thermal expansion-derived strain impacts small gaps much more than large ones, to point of debilitating large mechanical circuits of small-gapped resonators in the absence of defensive measures.

Interestingly, accurate knowledge of strain might be the single most important constraint on the ultimate size and performance of an array-based mechanical circuit like that of [80]. For example, finite element analysis (FEA) on a 6-disk coupled linear array under different compressive stress levels (*cf.* Fig. 4.2) shows that end resonators displace the most, i.e., 20nm at 200MPa, while the inner ones barely move, i.e., 6nm at 200MPa. The mechanical channel-select filter of [80] takes advantage of this by removing the electrodes around the end resonators (that would otherwise short) and using them as buffers to suppress the strain-derived displacement for the inner disks. Although this buffering method is effective for the array of 40-nm-gap devices in [80], it will not suffice for ultra-small gaps, i.e., sub-5nm, which are on the horizon. The desire for gaps like this

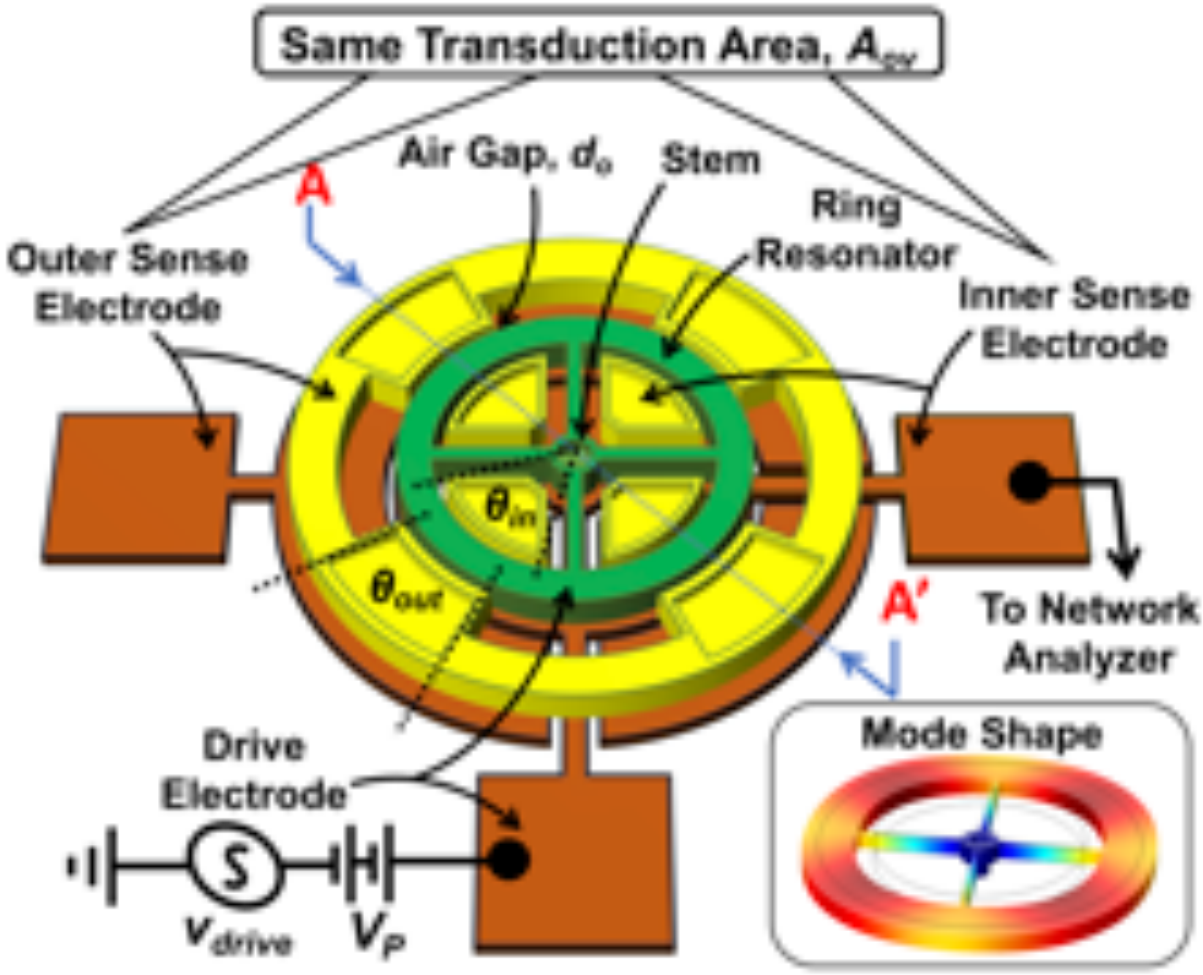


Fig. 4.1: The ring-based strain sensor described herein in a typical operating circuit with dimensions given in Table I. The inset shows the finite element analysis (FEA) simulated mode shape.

amplify the need to minimize post-fabrication residual strain—a need that will likely spur extensive fabrication recipe optimization, which in turn calls for a very sensitive, high resolution strain diagnostic tool.

Unfortunately, existing residual strain measurement techniques—including wafer bow [87] and various on-chip approaches [88], [89], [90]—either lack the precision to permit the most aggressive mechanical circuit designs or require large footprint area. For example, the Vernier stress gauge of [90] uses visual readout of indicator beam movement under a microscope, which is inherently imprecise. In addition, its sensitivity is directly proportional to its indicator beam length, which acts as a lever to amplify Vernier movement. Apart from occupying a large die area, the 100μm-long beam lengths need to measure stress down to 15MPa are susceptible to stiction and vertical stress gradients that bend them out of plane, rendering them unusable.

Pursuant to providing a more capable strain sensor, this paper presents an on-chip, spoke-supported ring-based strain measurement structure, shown in Fig. 4.1, that harnesses precision frequency measurement to precisely extract sub-nm displacements, allowing it to determine the residual strain in a given structural film with unprecedented accuracy, with measured stresses as small as 15MPa.

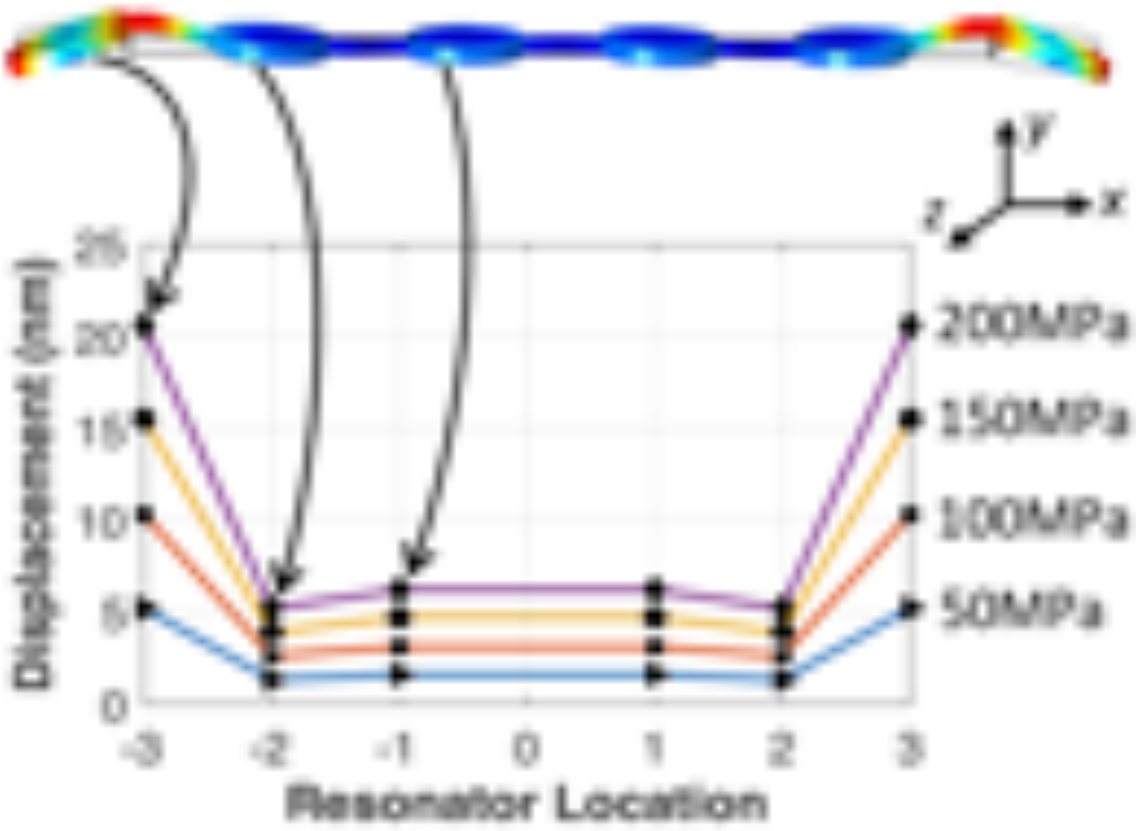


Fig. 4.2: Finite-element simulated plot of strain-induced x-axial displacement versus location for disks in a 6-disk polysilicon mechanically-coupled array under various compressive residual stress levels.

4.2. Device Structure and Operation

The strain sensor comprises a spoke-supported doped polysilicon ring surrounded by matched inner and outer doped polysilicon electrodes [54]. The device conveniently fabricates alongside tiny-gap mechanical filters via the process of [80], making it well-suited for diagnostic (or real-time) gap-control applications. Fig. 4.3(a) presents the cross-section of the strain sensor at the process step immediately before release, where a sacrificial oxide encases its ring structure on all sides. At this point, the electrode edges would ideally be the sidewall sacrificial oxide thickness d_o from the ring edges. In this state, the film is under stress due to thermal expansion differences with the substrate that manifest upon cooling from the deposition temperature to room temperature.

Removal of sacrificial oxide (via hydrofluoric acid) releases not only the structure, but also the stress, allowing the structure and substrate-anchored electrodes to freely displace relative to one another (*cf*. Fig. 4.3(b)) according to the value of residual strain ε, which takes the form

$$\varepsilon = \frac{\sigma}{E} = \frac{\Delta d_o}{R} \tag{4.1}$$

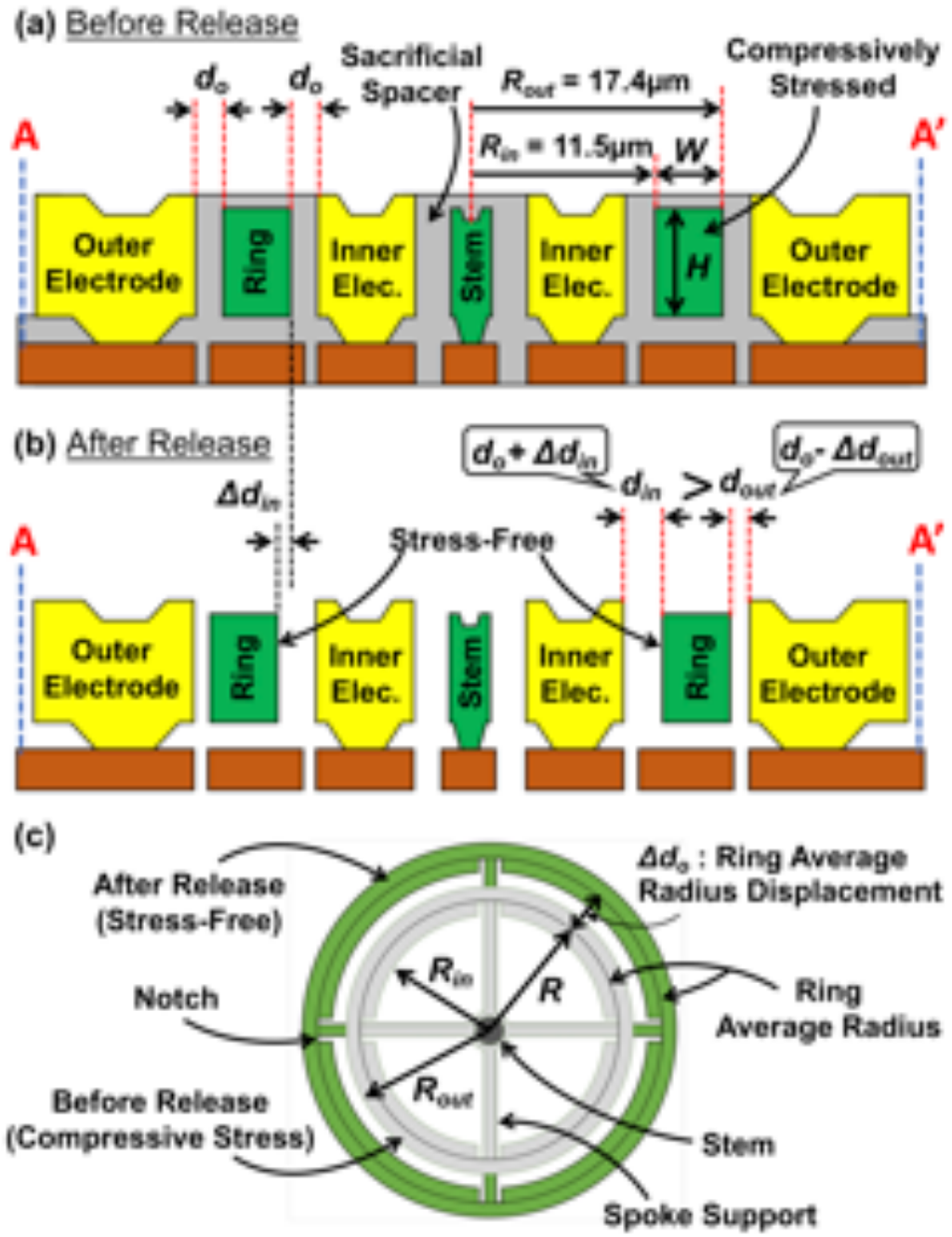


Fig. 4.3: Cross-sections through AA' in Fig. 4.1 (a) before release (b) after release. (c) Top view before and after release.

where σ is the residual stress, E is the Young's modulus of the resonator material, R is the distance from the stem to the center of the ring width, i.e., average ring radius in Fig. 4.3(c), and Δd_o is the strain-induced radial displacement at the average ring radius, given by

$$\Delta d_o = d_{out} - d_o = d_o - d_{in} \tag{4.2}$$

Equation (4.1) indicates a linear relationship between strain and actuation gap for small displacements, where measuring strain essentially amounts to measuring Δd_o. The small size of the

TABLE 4.I: GEOMETRIC DIMENSIONS AND MATERIAL PROPERTIES

Parameter	Value	Parameter	Value
Inner Radius, R_{in}	17.4μm	Outer Radius, R_{out}	11.5μm
Inner Angle, θ_{in}	65.26°	Outer Angle, θ_{out}	43.13°
Inner Coefficient, χ_{in}	0.912	Outer Coefficient, χ_{out}	1.075
Thickness, H	3μm	Young's Modulus	158GPa
Ring Width, W	5.9μm	Density	2300kg/m^3
Ring Radius, R	14.45μm	Poisson Ratio	0.226

proposed structure (*cf.* Table 4.I) predicates gap changes on the order of 1nm, which require a very sensitive measurement method. Here, frequency-based metrology employing the bias, excitation, and sensing scheme shown in Fig. 4.1 offers an excellent approach.

Specifically, when the electrode-to-resonator gaps are small, the resonance frequency of the ring structure becomes a strong function of electrical stiffness, which is in turn strongly dependent on gap spacing. Here, the expression for resonance frequency takes the form

$$f_{in(out)} = \sqrt{f_{nom}^2 - \frac{\varepsilon_o V_p^2}{2\pi^3 \rho W R} \frac{R_{in(out)}\theta_{in(out)}}{\chi_{in(out)} d_{in(out)}^3}} \tag{4.3}$$

where ε_o is the free-space permittivity, ρ is the density of the structural material, V_p is the dc-bias voltage, $R_{in(out)}$ is the distance from inner (outer) edge of the annulus to the stem, $d_{in(out)}$ is the inner (outer) electrode actuation gap, $\theta_{in(out)}$ is the inner (outer) electrode subtended angle in radians, W is the annulus width, $\chi_{in(out)}$ is a mass modifier factor relating the actual physical mass to the dynamic mass at the inner (outer) edge of the annulus, and f_{nom} is the mechanical (or nominal) resonance frequency for the ring, i.e. with no applied voltages [54].

Given this, measuring gap change (hence, strain) entails first measuring the resonance frequency of the ring for various dc-bias voltages V_P applied between the ring and either the inner or outer electrode, then curve fitting via (4.3) to obtain f_{nom} and either d_{in} or d_{out}. Δd_o is then the difference between this extracted gap and the nominal gap, d_o. Although quite straightforward, one issue limiting the accuracy with this approach is its dependence on the initial gap, d_o determined by the sidewall sacrificial layer deposition thickness, which could deviate from the target. To quantify this, a 1nm uncertainty in the initial gap, hence Δd_o, causes 69.2με error in strain, or 10.9MPa in stress for polysilicon, using (4.1) with the parameters given in Table 4.I. Considering that target stresses might be as small as 15MPa, this much error is not acceptable and calls for a better stress extraction technique independent of the starting gap, d_o.

Recognizing that after release the outer electrode gap shrinks (expands) as much as the inner electrode expands (shrinks), a balanced measurement entailing separate extraction of inner and outer electrode gaps, d_{in} and d_{out}, respectively, removes the dependency on the initial gap according to

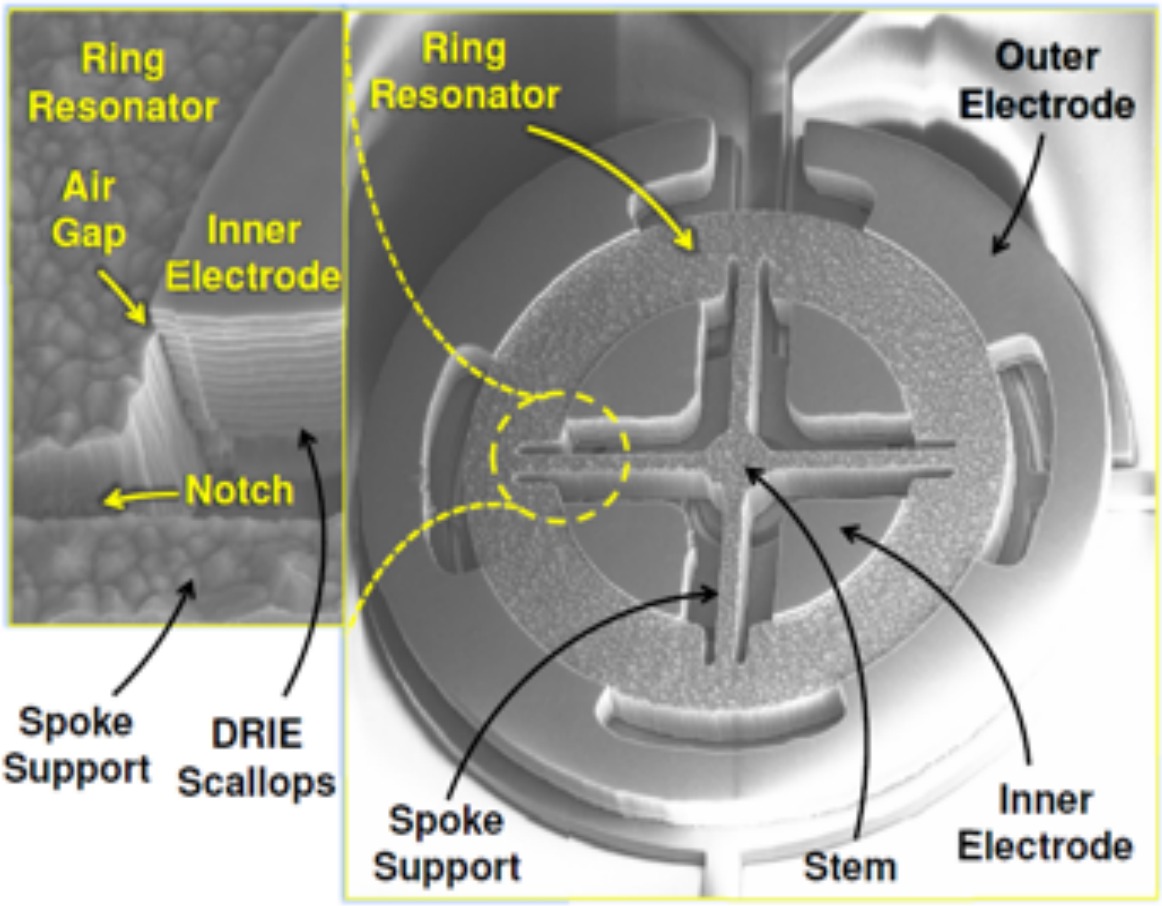


Fig. 4.4: SEM of a fabricated polysilicon strain diagnostic device.

$$\Delta d_o = \frac{d_{out} - d_{in}}{2} \tag{4.4}$$

Substituting (4.4) into (4.1) yields the residual strain, ε

$$\varepsilon = \frac{\sigma}{E} = \frac{d_{out} - d_{in}}{2R} \tag{4.5}$$

As will be seen, the dependence is strong enough and frequency measurement precision good enough that even sub-nm gap changes are precisely measurable.

4.3. Experimental Results

Fig. 4.4 presents wide- and zoomed-view SEM's of a ring-based residual strain gauge (which was fabricated alongside tiny-gap mechanical filters). Fig. 4.6 presents vacuum-measured transmission spectra for the ring operating in its first mode shape (*cf.* inset of Fig. 4.1) while driven (a) via inner electrodes only and (b) via outer electrodes only. The difference in frequency excursion for each case indicates a difference in electrode-to-resonator gap spacing that extracts very precisely upon curve-fitting the data, as done in Fig. 4.6. Here, the inner gap is 43.1nm, while the outer 40.2nm. These comprise directional changes from the extracted starting 41.65-nm gap that very precisely indicate 15.05MPa of compressive residual stress. Opposite gap changes, i.e., the

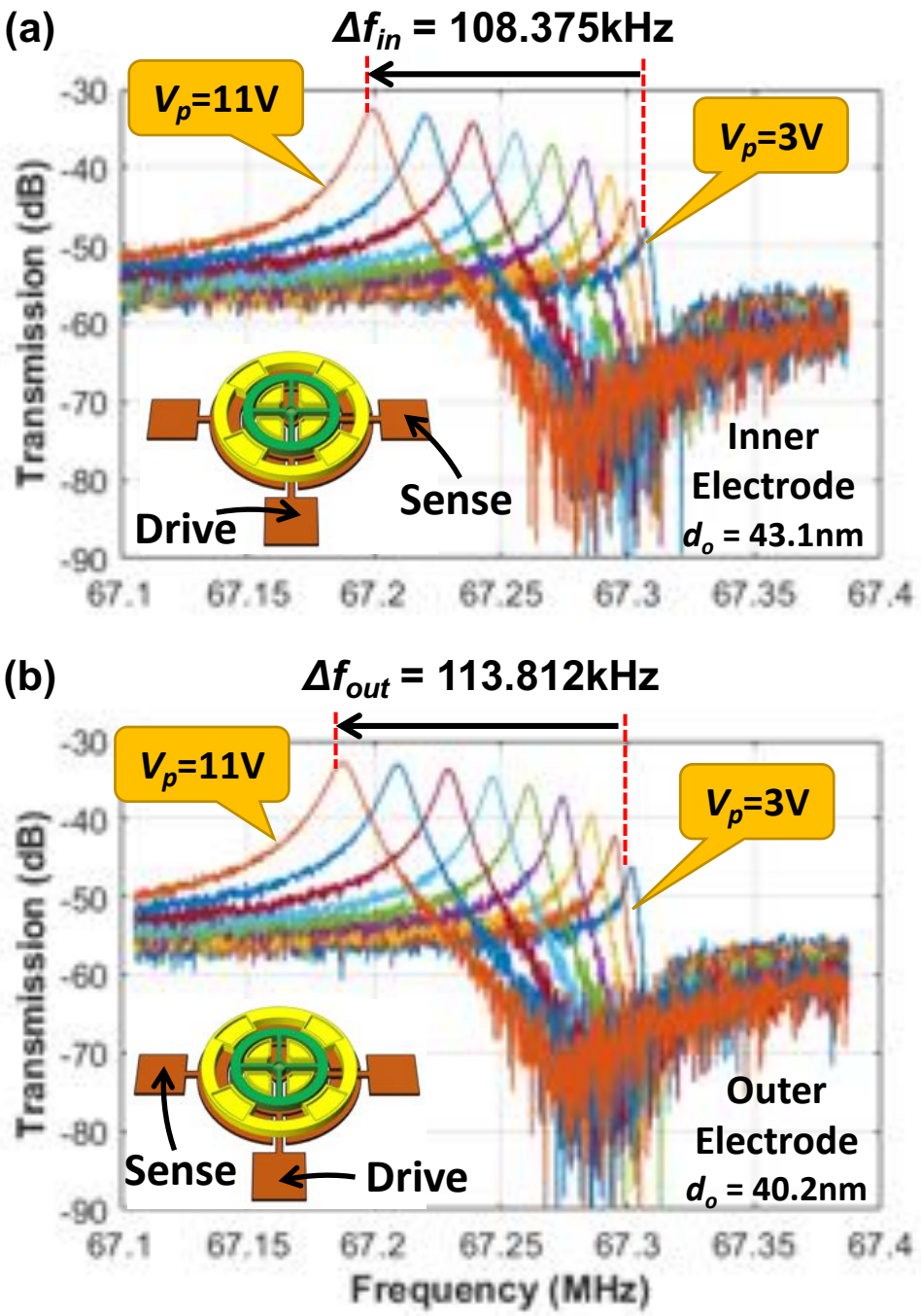


Fig. 4.5: Measured frequency spectra for a ring strain diagnostic device as a function of dc-bias voltage using the (a) inner and (b) outer port for sensing.

inner gap decreasing and outer gap increasing, would indicate tensile stress, and would be measurable just as precisely.

A. Scale Factor (Sensitivity)

Scale factor (or sensitivity) for a resonant sensor is a measure of its frequency shift per unit strain, here simply corresponding to the slope of the resonance frequency vs. strain curve before any gap change takes place, i.e., when $d_{in} = d_{out} = d_o$, as follows

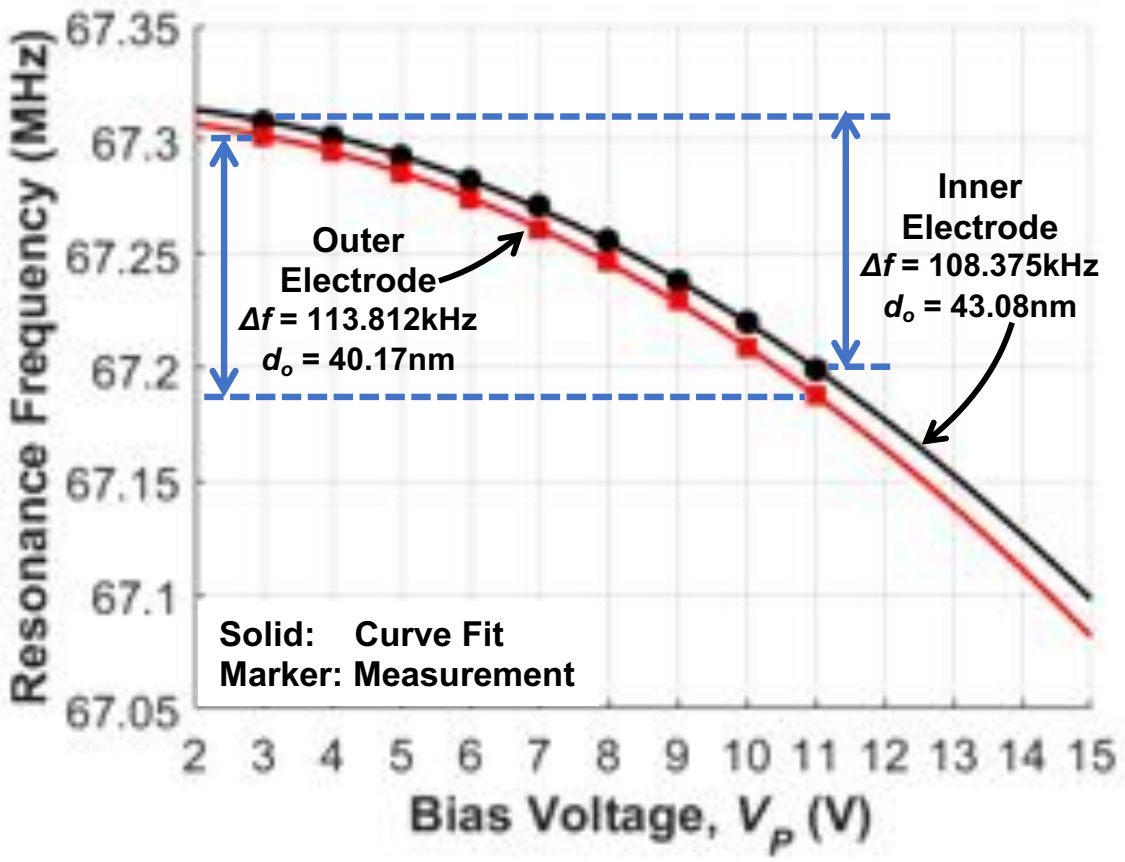


Fig. 4.6: Measured frequency spectra for a ring strain diagnostic device as a function of dc-bias voltage using the (a) inner and (b) outer port for sensing.

$$\left(\frac{\partial f_o}{\partial \varepsilon}\right)_{in(out)} = -(+)\frac{3\varepsilon_o V_P^2}{4\pi^3 \rho W f_{nom}} \frac{R_{in(out)}\theta_{in(out)}}{\chi_{in(out)} d_o^4} \tag{4.6}$$

Note that in (4.6) positive strain corresponds to tensile stress, while negative to compression. The aforementioned balanced measurement scheme further enhances the scale factor according to

$$\frac{\partial f_o}{\partial \varepsilon} = \left(\frac{\partial f_o}{\partial \varepsilon}\right)_{out} - \left(\frac{\partial f_o}{\partial \varepsilon}\right)_{in} \tag{4.7}$$

Noting that the overlap area, A_{ov} for the inner and outer electrodes are the same using the values in Table 4.I and substituting (4.6) in (4.7) yields

$$\frac{\partial f_o}{\partial \varepsilon} = \frac{3\varepsilon_o V_P^2 A_{ov}}{2\pi^3 \rho W H f_{nom} d_o^4} \tag{4.8}$$

The fourth power inverse dependence of the scale factor on the actuation gap d_o makes this sensor extremely sensitive considering its ~40nm gaps. Equation (4.8) in fact predicts a scale factor of 291.54 Hz/με for the strain sensor of Fig. 4.1 with the parameters outlined in Table 4.I under 11V dc-bias.

B. Resolution

TABLE 4.II: PERFORMANCE COMPARISON CHART WITH STATE-OF-ART STRAIN SENSORS

Technology	**MEMS Capacitive (Silicon)** [93]	**MEMS Piezoelectric (ZnO)** [94]	**MEMS Capacitive (Silicon)** [95]	**This Work**	**Unit**
Scale Factor	816μV	340μV	120Hz	292Hz	$\mu\varepsilon^{-1}$
Resolution	870	28.7	4	9.19	nε
Range	±1000	N/A	±2.5	±2768	με

Resolution is the minimum strain that the sensor of Fig. 4.1 can accurately measure through its transduction mechanism, i.e., strain to frequency conversion. Here, the minimum resolvable resonance frequency shift—largely governed by the resonator's short-term frequency stability—sets the lower resolution limit. Fortunately, the high Q of capacitive-gap polysilicon resonators at HF permit them to exhibit excellent short-term stability [84], [91]. In particular, the 61-MHz wineglass disk resonator of [92] posts an Allan deviation, σ_{ymin} of $2\text{x}10^{-8}$ at 1s integration time. Given Allan deviation, the expression for frequency jitter Δf takes the form

$$\Delta f = \sigma_{ymin} f_o \tag{4.9}$$

The resolution, $\Delta\varepsilon$ is then

$$\Delta\varepsilon = \Delta f \left(\frac{\partial f_o}{\partial \varepsilon}\right)^{-1}_{in(out)} \tag{4.10}$$

Finally, substituting (4.6) and (4.9) in (4.10) yields

$$\Delta\varepsilon = \sigma_{ymin} f_o \frac{4\pi^3 \rho W H f_{nom}}{3\varepsilon_o V_P^2 A_{ov}} d_o^4 \tag{4.11}$$

If one supposes the ring resonator herein posts the Allan deviation performance of the wineglass disk in [91], then (4.11) with the parameters in Table 4.Iand assuming an 11V dc-bias yields for resolution 9.19nε. Of course, this is a calculated value that requires measured verification. But if real, it bests many other published on-chip strain sensors, as shown in Table 4.II.

C. Range

The initial gap, d_o determines maximum permissible strain-induced ring displacement. The corresponding maximum measurable strain ε_{max} then follows by taking $\Delta d_o = d_o$ in (4.1), which yields

$$\varepsilon_{max} = \frac{d_o}{R} \tag{4.12}$$

Using (4.12), the device of this work with an initial gap of 40nm has a maximum measurable strain of ±2768με, which corresponds to ±415.2MPa of stress for polysilicon.

4.4. Conclusions

The frequency output provided by gap-dependent electrical stiffness permits the strain sensor described herein to achieve a combination of small size, large scale factor, low resolution, and large measurement range, that outpace alternatives, in some cases by substantial margins. Although the described sensor tailors specifically to tiny-gap devices, it is not difficult to see that its underlying approach will work regardless of the process or gap used.

Although presented as a diagnostic tool, this device is clearly applicable as a general strain sensor. Indeed, its small size and high performance make it a strong candidate for use as an *in situ* strain sensor that might measure real-time strain changes—due to package stress, thermal variations, or other sources—to then allow real-time corrections. Such an approach could play a significant role towards improving the long-term stability of capacitive-gap transduced oscillators beyond their already impressive marks [92], [76].

Chapter 5
Single-Digit-Nanometer Capacitive-Gap Transduced Micromechanical Disk Resonators

This chapter presents single-digit-nanometer electrode-to-resonator gaps that have enabled 200-MHz radial-contour mode polysilicon disk resonators with motional resistance R_x as low as 144Ω while still posting Q's exceeding 10,000, all with only 2.5V dc-bias. The demonstrated gap spacings down to 7.98nm are the smallest to date for upper-VHF micromechanical resonators and fully capitalize on the fourth power dependence of motional resistance on gap spacing. High device yield and ease of measurement debunk popular prognosticated pitfalls often associated with tiny gaps, e.g., tunneling, Casimir forces, low yield, none of which appear. The devices, however, are more susceptible to environmental contamination when unpackaged. The tiny motional resistance, together with (C_x/C_o)'s up to 1% at 4.7V dc-bias and (C_x/C_o)-Q products exceeding 100, propel polysilicon capacitive-gap transduced resonator technology to the forefront of MEMS resonator applications that put a premium on noise performance, such as radar oscillators.

5.1. Introduction

The promise of sub-10-nm gaps has long enticed researchers pursuing capacitive-gap transduced micromechanical resonators operating at upper-VHF and beyond. This is because the theoretical fourth order dependence of motional resistance on electrode-to-resonator gap spacing predicts that capacitive-gap transduced resonators will outperform piezoelectric ones in both coupling and Q when gaps get below a certain threshold. Indeed, the former already outperform the latter in both metrics at HF and low-VHF frequencies [96], [45], [68], which is why capacitive-gap transduced resonators have dominated the MEMS timing market. At higher frequencies, e.g., upper-VHF and beyond, while capacitive-gap devices have the higher Q's, piezoelectric ones had considerably higher coupling. That is, until now. The 7.98nm gaps demonstrated herein offer 7.5 times motional resistance R_x reduction over [45] and for the first time enable capacitive-gap transduced resonators at 200 MHz with R_x of 144Ω and a (C_x/C_o)-Q ~100, more than 2 times that of the nearest previously published upper-VHF (i.e., 150-300 MHz) resonators [97], [98].

This chapter briefly details the theory, fabrication, and demonstration of single-digit-nm gap polysilicon resonators, then illustrates how the equivalent circuits of such devices enable oscillator and filtering applications that could catapult MEMS-based timing and frequency control capabilities to levels that permit greater cognitive abilities in communication systems [9].

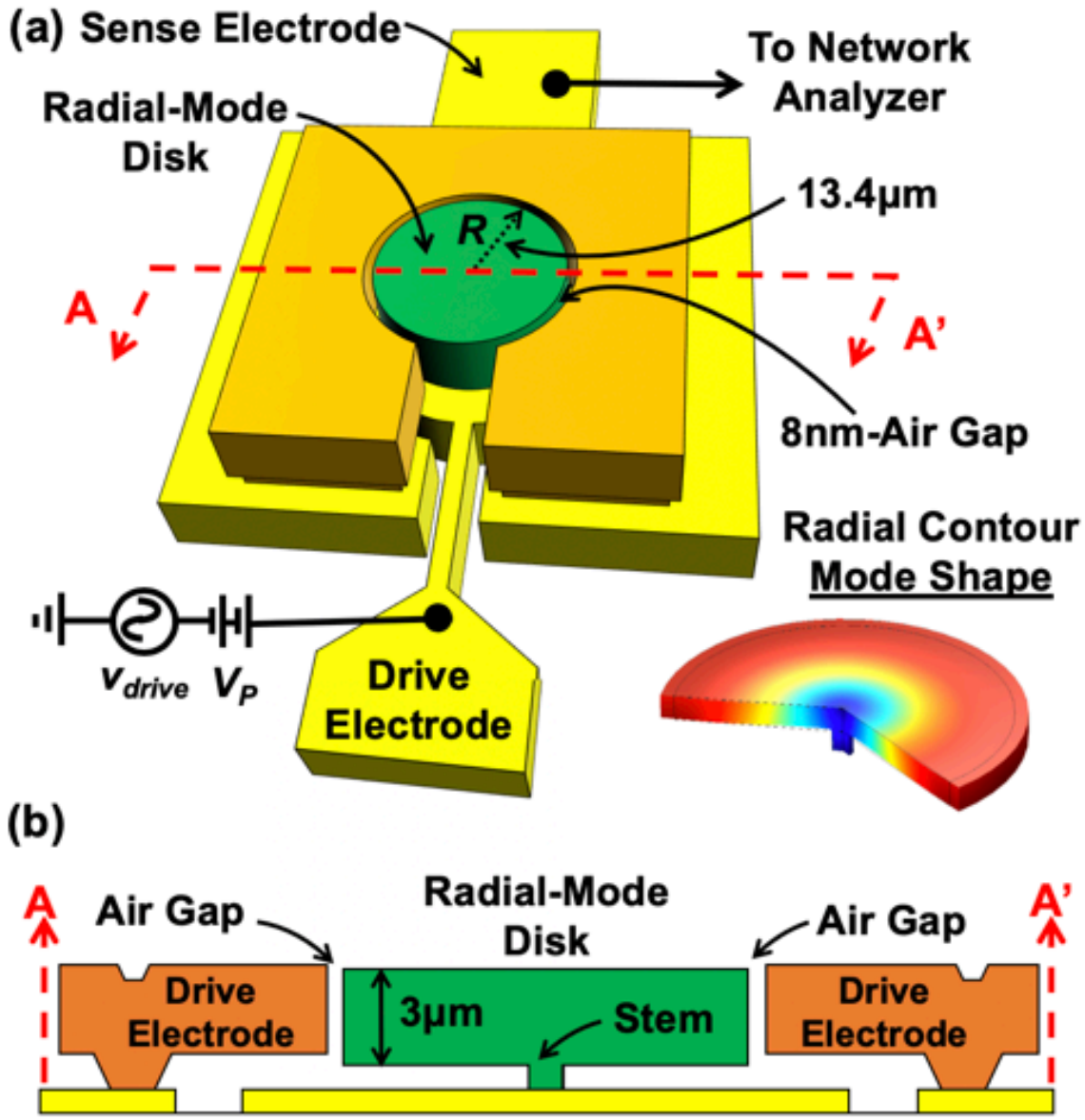


Fig. 5.1: (a) The contour mode disk resonator described herein in a typical operating circuit with dimensions and the mode shape. (b) Device cross-section.

5.2. Device Operation and Model

Fig. 5.1 presents a perspective view of the disk resonator in a typical bias and excitation circuit, together with dimensions and operating mode shape. The device is similar in structure to that of [45] but differs in its much smaller gap spacing and in its use of 3-μm-thick interconnects to reduce interconnect resistance, which helps to isolate the intrinsic Q and motional resistance during measurement.

The device operates by vibrating upon application of an appropriate combination of dc-bias V_P plus ac excitation v_{drive} across its electrode-to-resonator gap [44], where excitation at its radial-contour mode resonance frequency induces vibration in the mode shape depicted in Fig. 5.1(a). The resulting dc-biased time-varying electrode-to-resonator capacitance then sources an output

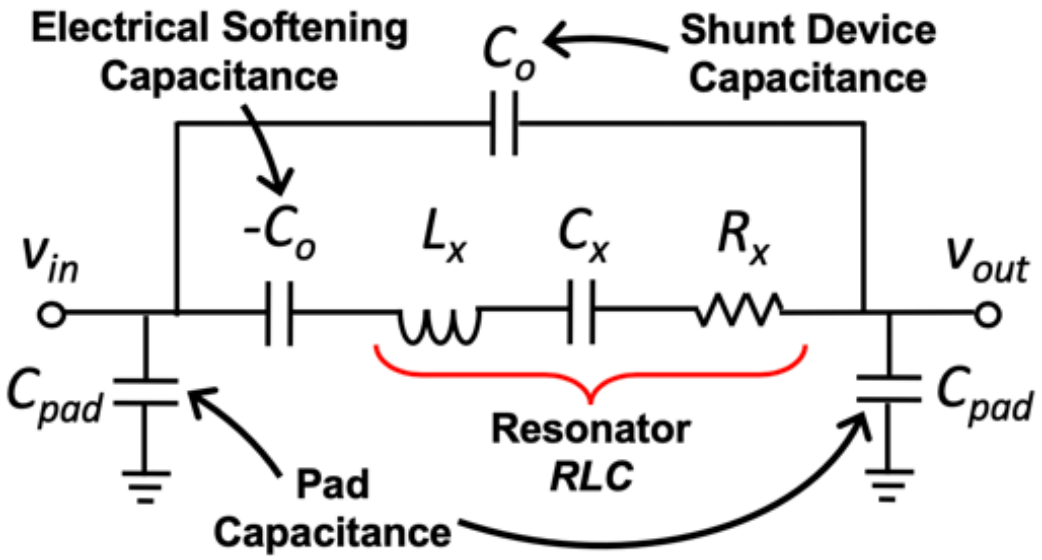


Fig. 5.2: Condensed equivalent circuit between the drive and sense terminals of the Fig. 5.1 device.

current across the device terminals in Fig. 5.1(a). The magnitude of current at resonance is governed by the motional resistance R_x in the condensed equivalent circuit of Fig. 5.2, which takes the form

$$R_x = \frac{\chi K_{mat}\sqrt{E\rho}d_o^4}{16QV_p^2\varepsilon_o^2RH} \tag{5.1}$$

where Q is the quality factor, V_P is the dc-bias, d_o is the air gap, ε_o is the vacuum permittivity, R is the disk radius, H is the disk thickness, χ is a constant that relates the static mass of the disk to its dynamic mass [44], K_{mat} is a dimensionless frequency parameter [44], E is the Young's modulus of the resonator structural material, and ρ is the density of the resonator structural material. Here, the smaller the R_x, the larger the current, so many applications prefer a small R_x. This, together with the fourth power dependence of R_x on electrode-to-resonator gap spacing d_o, fuels the desire to shrink d_o.

The device becomes more effective in various applications as the ratio of C_x to C_o in the Fig. 5.2 equivalent circuit rises. In designable parameters, this ratio takes the form

$$\frac{C_x}{C_o} = \frac{V_P^2}{d_o^3}\frac{\varepsilon_o R\theta_{ov}}{\pi^3\chi K_{mat}^2 E} \tag{5.2}$$

where again shrinking d_o very quickly improves the metric. Next generation timing and RF channel-select applications expected to enable transformative changes [9], [79] prefer simultaneous Q and C_x/C_o in the range of >10,000 and ~1%, respectively.

5.3. Fabrication

Fig. 5.3 briefly summarizes the surface-micromachining fabrication process that achieves single-digit-nm-gap devices, largely based on the process used in [80]. The main difference from [80] is the critical gap-defining step of Fig. 5.3(b), which now employs an ultra-smooth polysilicon

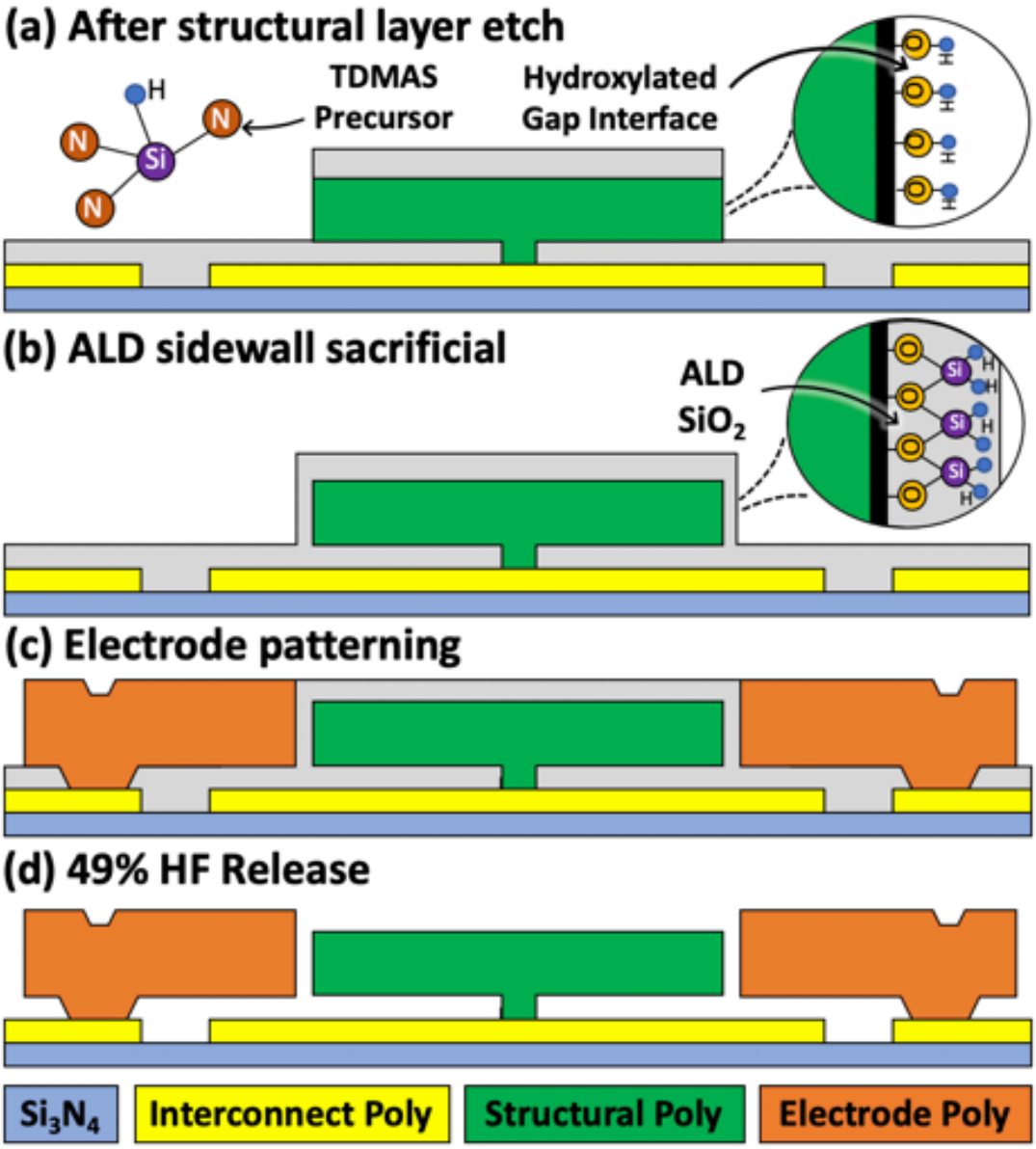


Fig. 5.3: Portions of the fabrication process flow focusing on the ALD sidewall sacrificial spacer that defines the single-digit-nm gap.

etch recipe [45], careful cleaning, and ample hydroxylation before an SiO_2 ALD step that establishes the sub-10-nm gap defining oxide. The use of ALD in lieu of the LPCVD high temperature oxide deposition of previous processes [45] outright enables the tiny gaps achieved here.

The next most critical step in the process is the device release, which now entails multiple piranha and HF soaks to adequately clear the gaps. Contrary to popular expectation, residual stress was not a big concern, as the process permits a surprisingly high (>90%) functional device yield, even without a stress anneal. Fig. 5.4 presents wide-view and zoom-in SEMs of a fabricated 8-nm-gap disk resonator, emphasizing the much smoother resonator sidewalls than electrode sidewalls, the latter of which were etched via a conventional DRIE recipe.

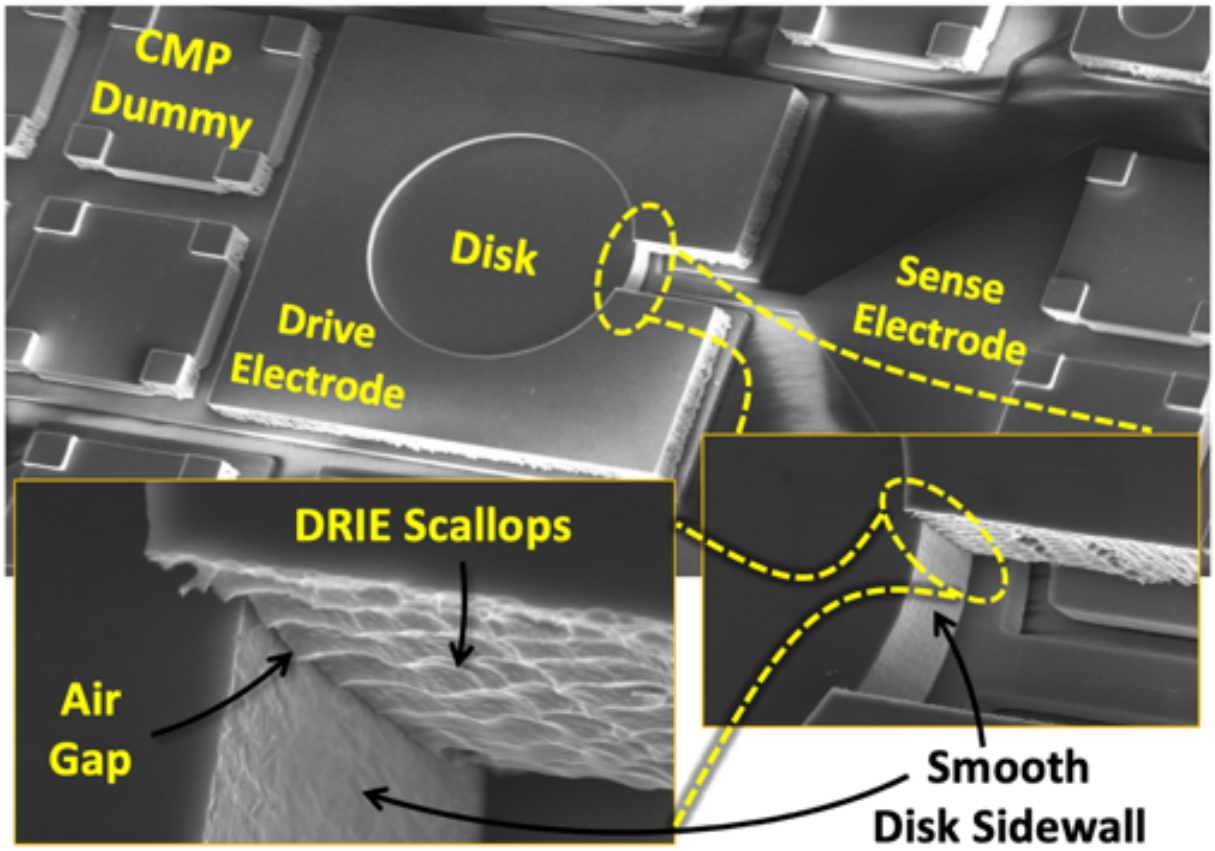


Fig. 5.4: SEM of a fabricated single-digit-nm gap contour mode polysilicon disk resonator.

5.4. Results and Discussion

For comparative purposes, the fabrication process achieved not only single-digit-nm gaps via ALD, but also larger gaps from 10 nm to 80 nm via appropriate deposition types, e.g., LPCVD. Once released, devices were quickly transferred into a Lakeshore FWPX Vacuum Probe Station that provided a 100 μTorr vacuum environment as well as probes and access ports that connect to outside measurement instrumentation. In actual measurement, an Agilent E5071C network analyzer provided the drive signal and sense port in the circuit of Fig. 5.1(a).

For single-digit-nm gap devices, the best experimental results came upon immediate measurement after release—something not needed for larger gap devices. Longer wait times between release and measurement resulted in degraded performance, e.g., lower Q, suggesting larger susceptibility to contamination, e.g., moisture condensation, which one might expect with gaps this small. Once in vacuum, however, devices stabilized and other popular concerns about gaps this small, whether real or mythical, e.g., tunneling, Casimir forces, did not materialize.

Fig. 5.5(a) presents vacuum-measured transmission spectra (both actual and sans parasitic interconnect/measurement resistance) versus dc-bias for a 13.4μm-radius radial-contour mode polysilicon disk, showing a 199.8 to 199.5-MHz frequency excursion over 0.6 to 2.5V with a Q of 12,298 at 0.6V. Fig. 5.5(b) presents a curve fit of resonance frequency versus dc-bias using electrical stiffness theory [44] that confirms an electrode-to-resonator gap spacing of 7.98nm. The scale here is perhaps best conveyed with the recognition that this gap corresponds to only 20-25 SiO_2 molecules!

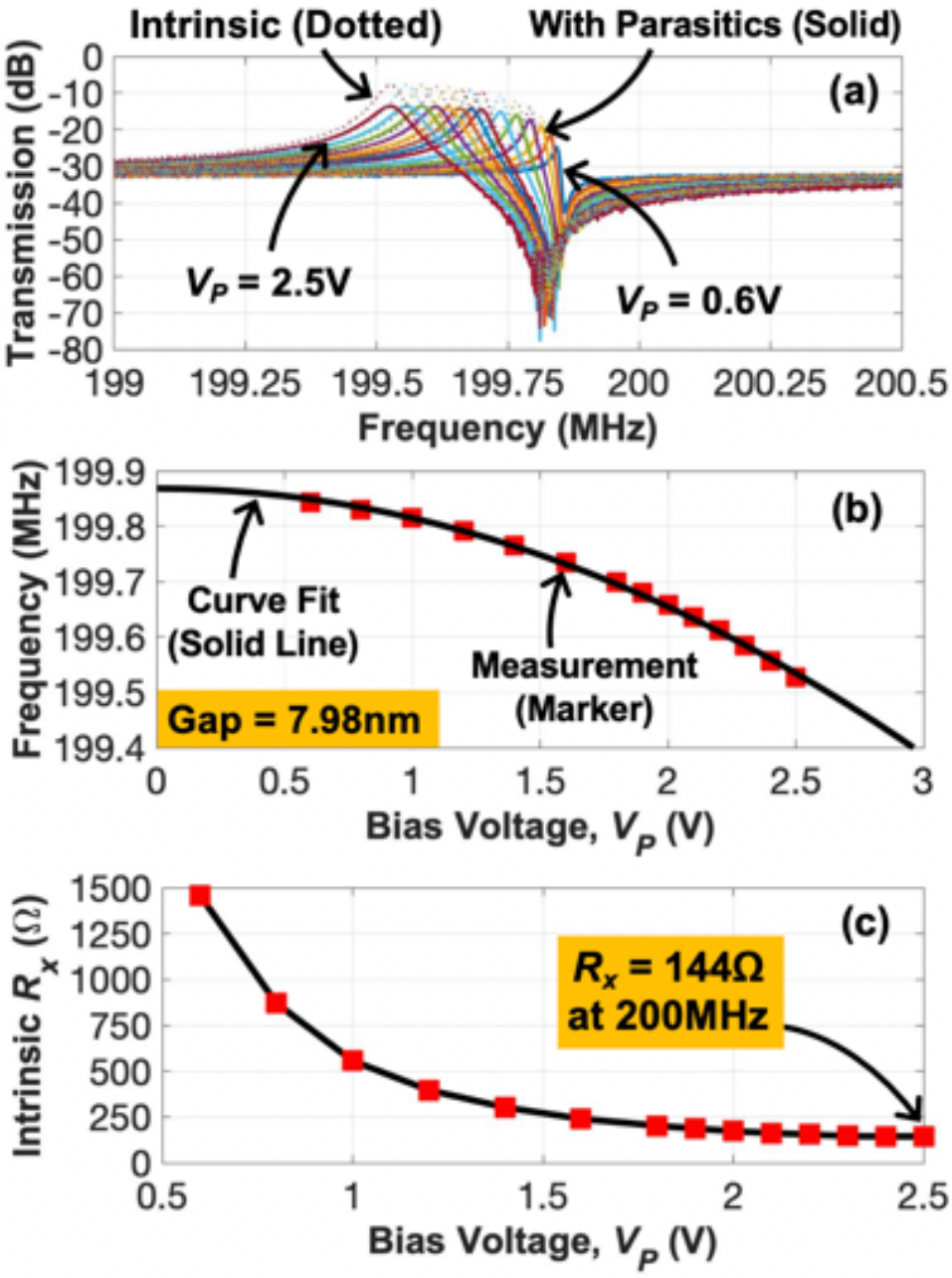


Fig. 5.5: (a) Measured frequency spectra as a function of dc-bias voltage that permit (b) curve-fitted extraction of the gap value and (c) a plot of motional resistance vs. V_P.

While Casimir effects were not seen, theory predicts that their influence is imminent as gaps continue to shrink. For instance, when accounting for Casimir force, the expressions governing the dc-bias voltage that pulls (or stretches) the disk into its electrode take the form

$$\frac{3d_{PI}}{2} - d_o = \frac{\pi^2 \hbar c R \theta_{ov}}{240 d_{PI}^4 k_r} \qquad V_{PI}^2 = \frac{k_r d_{PI}^3}{\varepsilon_o A_{ov}} - \frac{\pi^2 \hbar c}{60 \varepsilon_o d_{PI}^2} \tag{5.3}$$

where V_{PI} is the pull-in voltage, d_{PI} is the critical pull-in gap spacing, $\hbar$ is the modified Planck's constant, c is the speed of light, and k_r is the effective resonator stiffness. Fig. 5.6 solves and plots (5.3) against the traditional expression for pull-in voltage [99], suggesting that Casimir forces

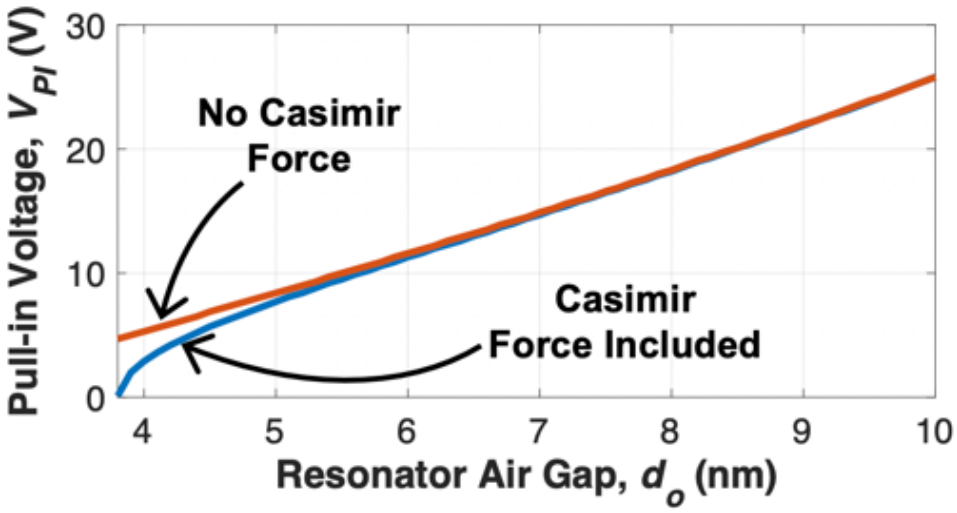


Fig. 5.6: Plot of pull-in voltage including and not including Casimir force, confirming our inability to see their influence even in the 8-nm-gap device.

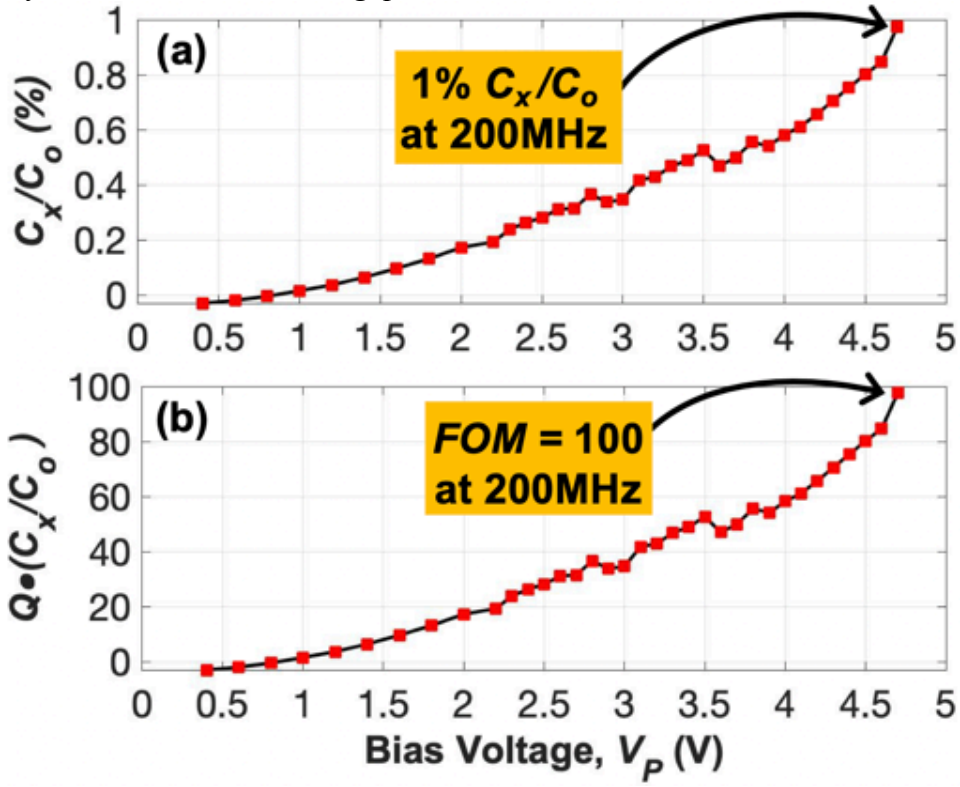


Fig. 5.7: Measured (C_x/C_o) and (C_x/C_o)-Q as functions of dc-bias voltage for a 9.4-nm-gap 200-MHz disk.

begin to influence when the gap approaches 6 nm, so are not yet apparent for the current 8-nm gap device. Using (5.3), the predicted pull-in voltage for the 8-nm-gap disk of Fig. 5.1 of 18.3V still permits a calculated motional resistance of 0.2Ω, which is quite small.

Unfortunately, devices pulled in well before 18.3V, possibly because (5.3) assumes the disk stretches symmetrically into the electrode and ignores the possibility of stem failure. Although dc-bias constraints precluded R_x's as low as 0.2Ω, they still permitted unprecedented low values for

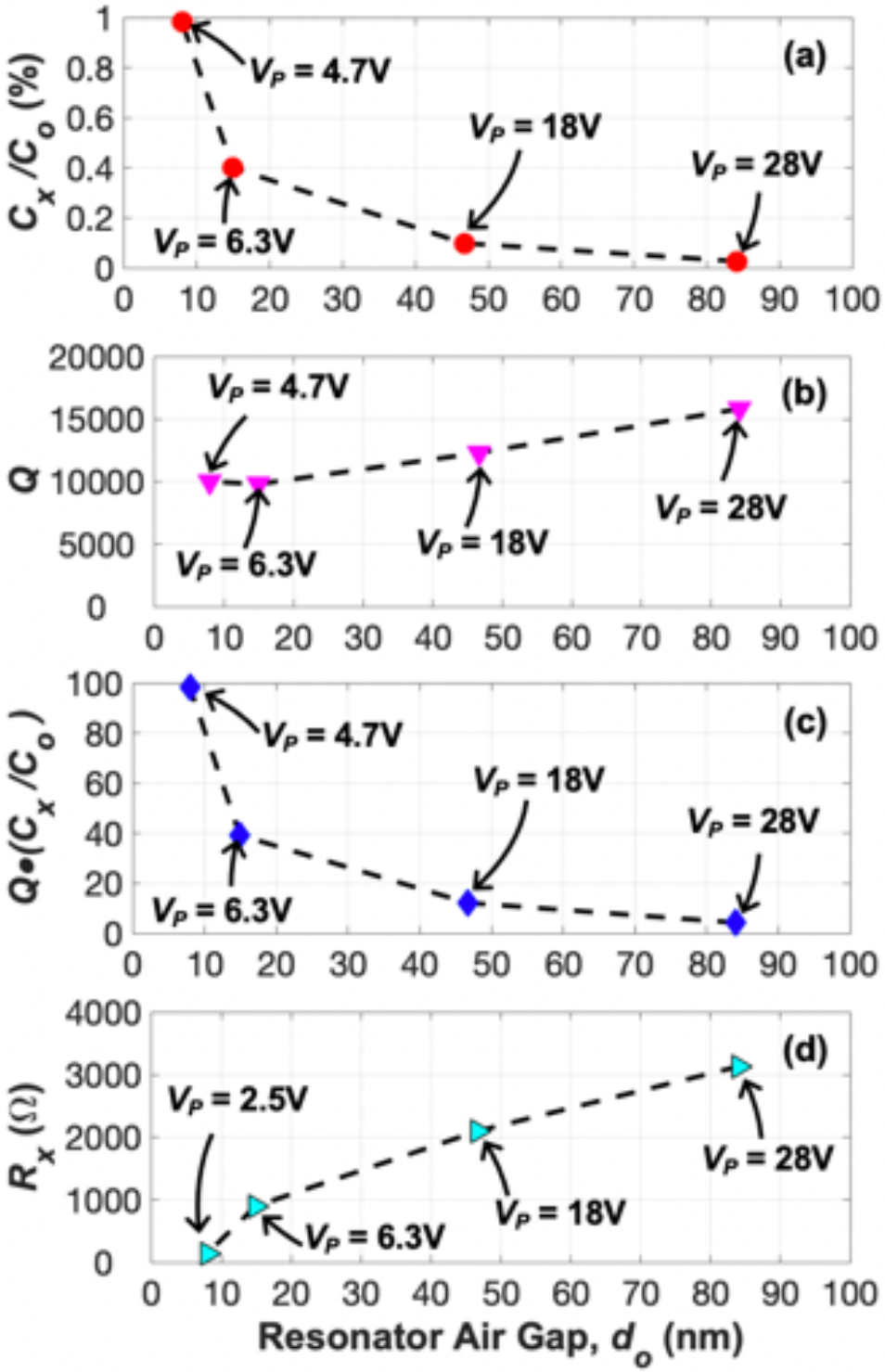


Fig. 5.8: Plots of various measured parameters versus electrode-to-resonator gap showing marked improvement in important resonator metrics as gaps shrink.

capacitive-gap transduced disks. For example, Fig. 5.6(c) shows a plot of measured motional resistance R_x versus dc-bias for a 9.4-nm-gap 200-MHz device, where 2.5V yields only 144Ω, which is commensurate with conventional RF applications. Fig. 5.7 presents the corresponding plot of (C_x/C_o)-Q, showing an impressive figure of merit of 100.

TABLE 5.I: COMPARISON CHART WITH OTHER TECHNOLOGIES.

Reference	*Technology*	f_o (MHz)	C_x/C_o (%)	R_x (Ω)	Q	k_t^2-Q	*Area* (μm²)
[85]	Piezoelectric	85	0.86	125	2,100	18	10,000
[98]	Piezoelectric-on-Si	108	0.70	-	6,300	50	72,000
[97]	Piezoelectric	220	1.60	-	2,500	40	9,000
[86]	Quartz	149	0.48	460	10,000	48	21,200
[45]	Capacitive	60	1.62	54	29,640	480	3,200
[100]	Capacitive	123	0.75	1,250	2,271	17	1,600
This Work	Capacitive	200	1.00	144	12,298	100	718

Fig. 5.8 compares the performance of 200-MHz polysilicon disk resonators with varying electrode-to-resonator gaps. Here, even though smaller gaps impose smaller maximum dc-bias voltages and seem to slightly reduce Q, they still enable higher (C_x/C_o)'s, as well as (C_x/C_o)-Q's, both of which increase as $1/d_o^{1.30}$. The figure also shows how R_x still decreases as $d_o^{1.52}$ when accounting for the observed dc-bias and Q constraints.

Table 5.I compares the device of Fig. 5.1 with other upper-VHF MEMS resonators in the literature using various transducers, showing clear advantages.

5.5. Application Opportunities

The expected impact of 8-nm electrode-to-resonator gaps perhaps best manifests in the applications they make possible. For instance, the simultaneous coupling of 1% with Q of 12,298 makes possible a Fig. 5.2 equivalent circuit with L_x = 223.55μH, C_x = 2.83fF, R_x = 22.84Ω, and C_o = 283fF that in turn enables channel-select filters using many more resonators than demonstrated in [80].

To illustrate, Fig. 5.9 presents frequency response simulations for Chebyshev filters like that of [80] but centered at 200 MHz with bandwidths of 400 kHz and using three resonators instead of just two for sharper passband to stopband transitions. One simulation (dotted line) assumes resonators like those of [80], with 40-nm gaps, with consequent passband distortion that renders the response problematic for RF channel-selection. A second simulation (dashed-dotted line) assumes resonators with Q and (C_x/C_o) achieved by AlN near 200 MHz [97], but results in even worse performance than the capacitive-gap transduced resonators of [80].

The solid curve finally corresponds to a filter simulation assuming resonators demonstrated herein with 8-nm gaps, for which passband distortion is no longer discernable. The solid curve is the only one usable for software-defined cognitive radio architecture scheme of [9].

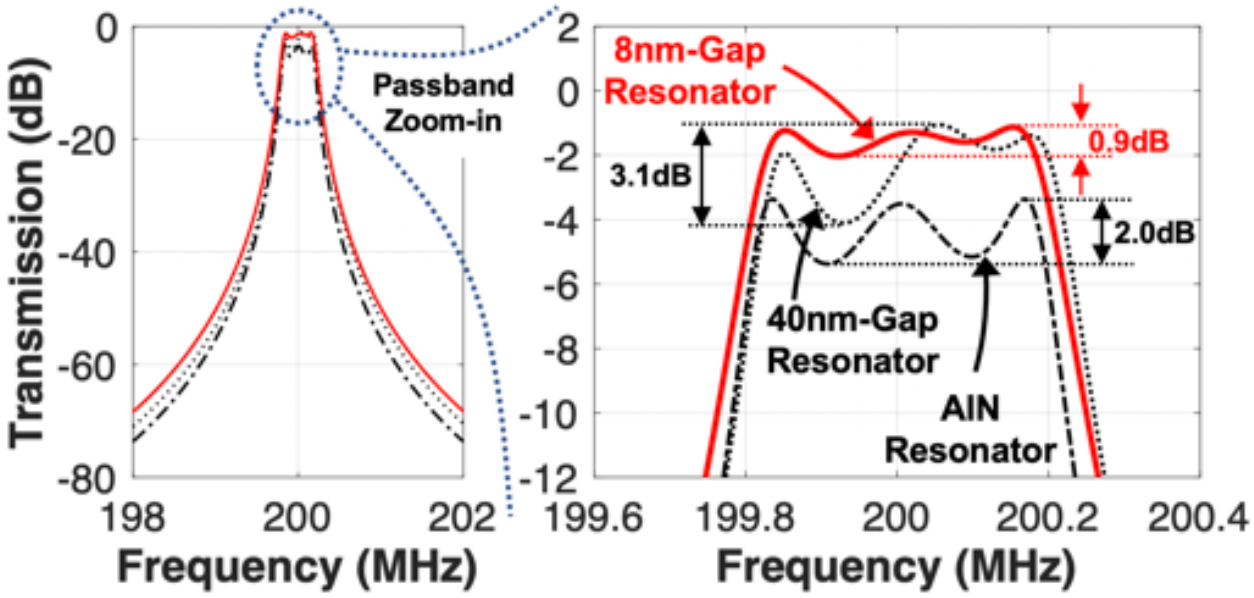


Fig. 5.9: Frequency response simulations for an RF channel-select Chebyshev bandpass filter using previous resonators versus the new 8-nm-gap resonators.

5.6. Conclusions

The demonstration herein of capacitive-gap transduced resonators with single-digit-nm electrode-to-resonator gaps now makes possible (C_x/C_o)-Q's up to 100 at upper-VHF frequencies that in turn enable simultaneous high Q >10,000 and low motional resistance <150Ω using sub-3V bias voltages. That capacitive-gap transduced resonators achieve this is especially significant for applications that require exceptional long-term stability, for which single-material resonators have historically performed best. The low-loss, stability, and strong coupling achieved here now propels capacitive-gap transduced devices towards high performance oscillator applications, e.g., low phase noise radar oscillators, and encourages research on transformative communication paradigms, such as RF channel-select-enabled software-defined cognitive radio. While 200-MHz is already useful for each of these applications, higher frequency is always welcome. Gigahertz resonators with single-digit-nm gaps are likely on the horizon.

Chapter 6
Q-Boosting of Metal MEMS Resonators Via Localized Anneal-Induced Tensile Stress

This chapter presents that introduction of tensile stress via localized Joule heating has yielded some of the highest metal MEMS resonator *Q*'s measured to date, as high as 48,919 for a 12-MHz ruthenium micromechanical clamped-clamped beam ('CC-beam'). The high *Q*'s continue into the VHF range, with *Q*'s of 7,202 and 4,904 at 61 and 70 MHz, respectively. These marks are substantially higher than the 6,000 at 10 MHz and 300 at 70 MHz previously measured for polysilicon CC-beams, defying the common belief that metal *Q* cannot compete with conventional micromachinable materials. The low-temperature ruthenium metal process, with highest temperature of 450°C and paths to an even lower ceiling of 200°C, further allows for MEMS post-processing directly over finished foundry CMOS wafers, thereby offering a promising route towards fully monolithic realization of CMOS-MEMS circuits, such as needed in communication transceivers. This, together with its higher *Q*, may eventually make ruthenium metal preferable over polysilicon in some applications.

6.1. Introduction

Oscillators referenced to high-*Q* micromechanical resonators that consume only 78 μW of power while attaining GSM-compliant phase noise performance have emerged as potential enablers for future low power autonomous wireless networks [74]. Although impressive, the bond-wired two-chip approach to realizing these MEMS-based oscillators inevitably incurs parasitic bond pad capacitances on the order of picofarads, thereby preventing these oscillators from realizing their true potential for power consumption [101]. Here, single-chip CMOS-MEMS integration to remove bond pad capacitance poses a nice solution. To date, however, high deposition temperatures for polysilicon or diamond MEMS materials hinder progress towards MEMS-last single chip integration alongside transistors. Their high structural and interconnect resistances also complicate applications that demand low loss, such as front-end filters. Structural and interconnect resistance also compromises MEMS-last integration approaches using SiGe structural material, which otherwise would meet temperature ceiling requirements for previous generation CMOS [28].

Ultimately, resistance needs might best be met by metal structural material options, many of which provide the added advantage of much lower deposition temperature making them more amenable to MEMS-last integration with CMOS. Unfortunately, to date metals post much lower *Q*'s than polysilicon, SiGe, or diamond counterparts [101]. If a metal is to replace these materials, some method is needed to enhance its *Q* without requiring transistor-damaging temperatures.

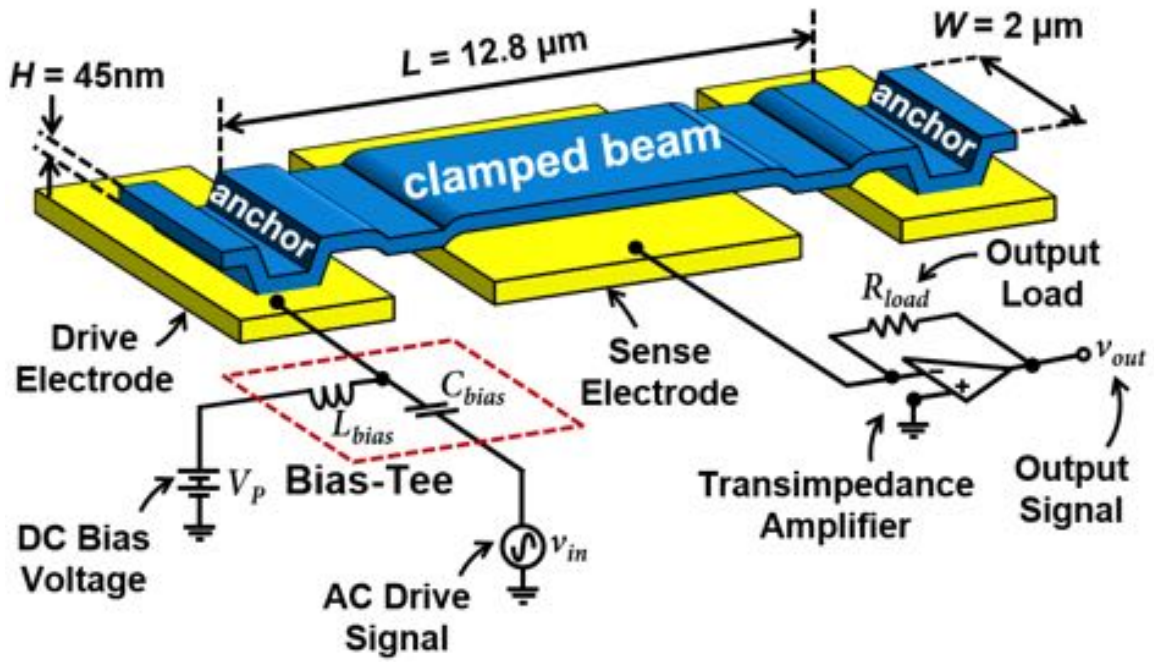


Fig. 6.1: Illustration of a single-electrode clamped-clamped (CC-beam) in a typical bias/excitation configuration.

Even without the draw of transistor-MEMS integration, there are burgeoning opportunities to apply high-*Q* metal structural material towards new all-mechanical circuits capable of detecting and demodulating RF signals while consuming no power when listening for inputs [102]. Such circuits can potentially obviate conventional sleep/wake methods intended to minimize sensor network power and in the process eliminate the clocks and computational overhead on which they rely. Here, the sensitivity, i.e., minimum detectable power, of such a circuit goes as the inverse of the *Q* of the resonator portion of the resoswitch they employ [102], which yet again, calls for a method for *Q* enhancement.

This paper demonstrates one such method that very effectively employs localized annealing to induce tensile stress in ruthenium clamped-clamped beam ('CC-beam') resonators and thereby raise their *Q*'s through mechanisms similar to those seen for nitride resonators [103], but with orders of magnitude lower thermal exposure for underlying transistors. Use of this method yields ruthenium resonator *Q*'s as high as 48,919 at frequencies approaching 12 MHz (to be compared with *Q* ~6,000 for polysilicon [21]); and retains high *Q* at VHF as indicated by *Q*'s of 7,202 and 4,904 at 61 and 70 MHz, respectively (to be compared with *Q* ~300 at 70 MHz for polysilicon [104]).

6.2. Device Structure and Operation

Fig. 6.1 summarizes the CC-beam micromechanical resonator device [21] used as a vehicle in this work in a typical bias, excitation, and evaluation circuit. The CC-beam differs from previous renditions [21] in not only the material used, which is now Ru; but also in its dimensions, which are substantially smaller than previous ones in order to maximize sensitivity for a resoswitch-based receiver application [102]. Specifically, unlike previous polysilicon CC-beam dimensions on the order of of 40.8µm-long, 8µm-wide, and 1.9µm-thick to reach 7.81 MHz, a typical Ru design herein is 12.8µm-long, 2µm-wide, and 45 nm-thick, with dimensions 3.2, 4, and 42 times smaller,

respectively. This reduces the mass and stiffness needed to achieve a given frequency, which improves (i.e., minimizes) sensitivity P_{sens} according to

$$P_{sens} = \frac{d_o^2 k_m \omega_o}{Q} \tag{6.1}$$

where k_m, d_o, and ω_0 are the mechanical stiffness, switch gap, and resonance frequency of the resoswitch, respectively. Note that smaller stiffness improves sensitivity, i.e., makes it smaller, by not only the direct stiffness term k_m in the numerator of (6.1), but also by reducing anchor dissipation, thereby raising the Q term in the denominator.

With Q as a focus, the devices herein were tested as resonators, rather than resoswitches, using the circuit of Fig. 6.1. Here, the bias-tee-combined AC-DC voltages of the drive and bias inputs together generate an amplified force at the frequency of the AC signal across the input-electrode-to-resonator gap. Sweeping the frequency of the AC source around the beam's resonance frequency generates vibrational motion that in turn creates a DC-biased time-varying capacitance across the electrode-to-resonator gap. A current then ensues, flowing through the structure and gap, out of the center electrode, and into the awaiting transimpedance amplifier detector.

As mentioned, this work boosts Q by introducing tension into the CC-beam. Of course, this tension affects not only Q, but also the resonance frequency. With tension added, the resonance frequency expression for the CC-beam becomes

$$f_o = 1.03 \frac{H}{L^2} \sqrt{\frac{E}{\rho}} \sqrt{1 + \frac{SL^2}{3.4EH^2}} \tag{6.2}$$

where f_0 is resonant frequency, E is Young's modulus, ρ is density, S is tensile stress, and Fig. 6.1 identifies geometric parameters.

6.3. Fabrication

The choice of ruthenium as a metal for this work has more to do with the fact that its oxide is also conductive, making it useful for resoswitches [105] as well as resonators. The process used to achieve the device of Fig. 6.1 employs a surface micromachining process that uses Ru for interconnect, low-temperature LPCVD oxide as a sacrificial layer, and sputtered Ru (only 45 nm-thick) as the structural material. Fig. 6.2 summarizes the fabrication process.

The fabrication starts on 6″ blank *p*-type Si wafers with successive LPCVD depositions of 2μm LTO and 500nm silicon rich nitride at 450°C and 835°C, respectively, to serve as electrical isolation layers. Note that the silicon nitride could be replaced by a lower temperature material, such as alumina, if this process were actually run over CMOS, which it presently is not. Sputtering of 60nm-thick Ru and PECVD deposition at 350°C of 60nm-thick thick oxide then follow to serve as the interconnect layer and the oxide hard mask used in its etching, respectively. Lithography via a first mask and dry etch using Ar:CHF_3:CF_4 then transfers the interconnect layer pattern into the oxide hard mask. Next, a dry etch with Applied Materials Centura DPS etcher using gas flow rates of 90sccm of O_2 and 20sccm of Cl_2 at 20mTorr pressure with source and bias powers of 300W and 50W, respectively, delineates the interconnect layer as depicted in Fig. 6.2(a); followed by a 1 minute 5:1 buffered HF dip to remove the oxide hard mask layer.

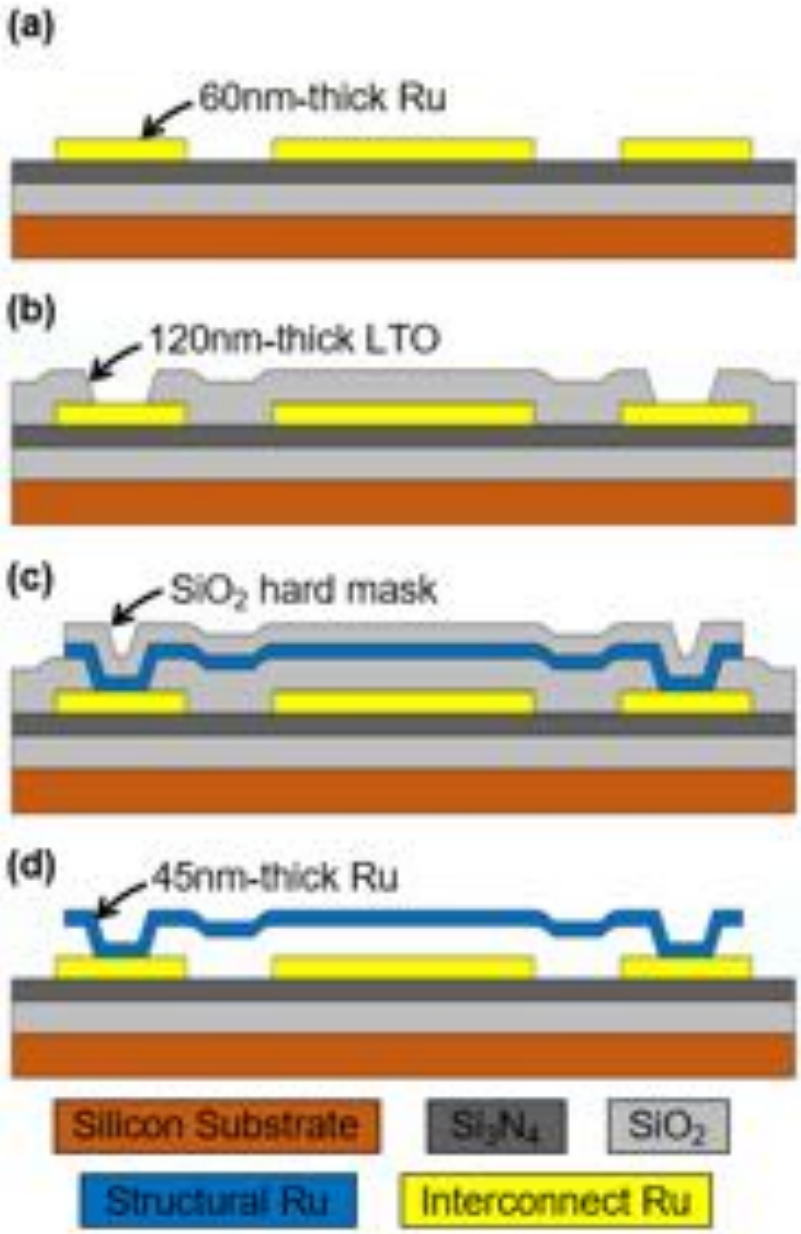


Fig. 6.2: Cross-sections describing the ruthenium metal CC-beam fabrication process flow after (a) patterning ruthenium interconnect and removing its etch hard mask; (b) depositing sacrificial layer and etching anchor openings; (c) depositing and patterning structural ruthenium; and (d) releasing the structure in HF.

Note that the need for a hard mask when etching the interconnect layer is not a consequence of the etch selectivity of the Ru dry etch chemistry over photoresist, which is actually quite adequate. Rather, it derives from a need to avoid cross-linking between Ru and photoresist observed at elevated temperatures [106]. In particular, even without hard- or UV-baking, the temperature elevation that occurs during dry etching of Ru is enough to instigate cross-linking so strong that removal of photoresist after Ru layer patterning becomes very difficult.

After interconnect layer patterning, LPCVD deposition of low temperature oxide (LTO) at 450°C coats a sacrificial oxide layer that defines the 120nm capacitive actuation gap between the

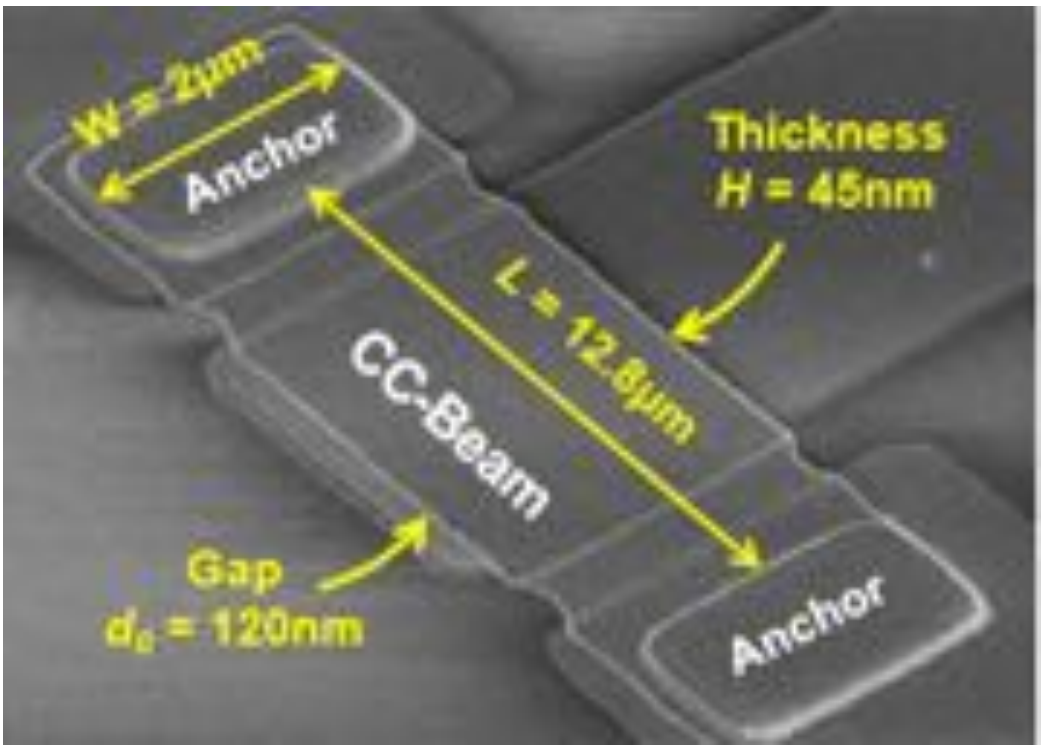


Fig. 6.3: SEM of a fabricated CC-beam resonator with key dimensions.

CC-beam and the underlying electrode. Anchor openings are then etched into the oxide sacrificial layer using Ar:CHF_3:CF_4 as illustrated in Fig. 6.2(b), followed by a sputtering of 45nm Ru to serve as the structural material. After depositing and patterning another oxide hard mask, the same chemistry that etched the interconnect layer delineates the structures as in Fig. 6.2(c). Here, a Ru etch chemistry comprised of mostly O_2 with a small amount of etch-rate enhancing Cl_2 provides good selectivity (>10) over the underlying sacrificial LTO layer [106]. This degree of selectivity becomes ever more critical for beam type devices with very small actuation gaps, i.e. < 20nm, intended for highly sensitive resoswitches.

Completed wafers are diced and the resulting dies released (when needed) in 49 wt. % liquid HF that frees the resonators. Since the small size and stiffness of the devices make them more prone to stiction, criticial point drying (CPD) is generally needed after HF release to insure adequate yield. Fig. 6.2(d) presents the final cross-section of the device. Fig. 6.3 presents the SEM of a fabricated 12.8μm-long device.

6.4. Tensile-Stressed Ruthenium CC-Beams

As shown in Fig. 6.4(a), immediately after fabrication, beams with dimensions shown in Fig. 6.1 post frequencies around 1.2 MHz with *Q*'s on the order of only 180, which is quite low. These represent the nearly stress-free performance of the devices, or at least the performance before stress introduction.

Again, the strategy behind the present work is to introduce stress in order to attain higher *Q*. If previous work with nitride resonators holds [103], better *Q* should be possible via introduction of tensile stress. This previous work introduced stress mechanically, by tightening a pull system via turns of a screw.

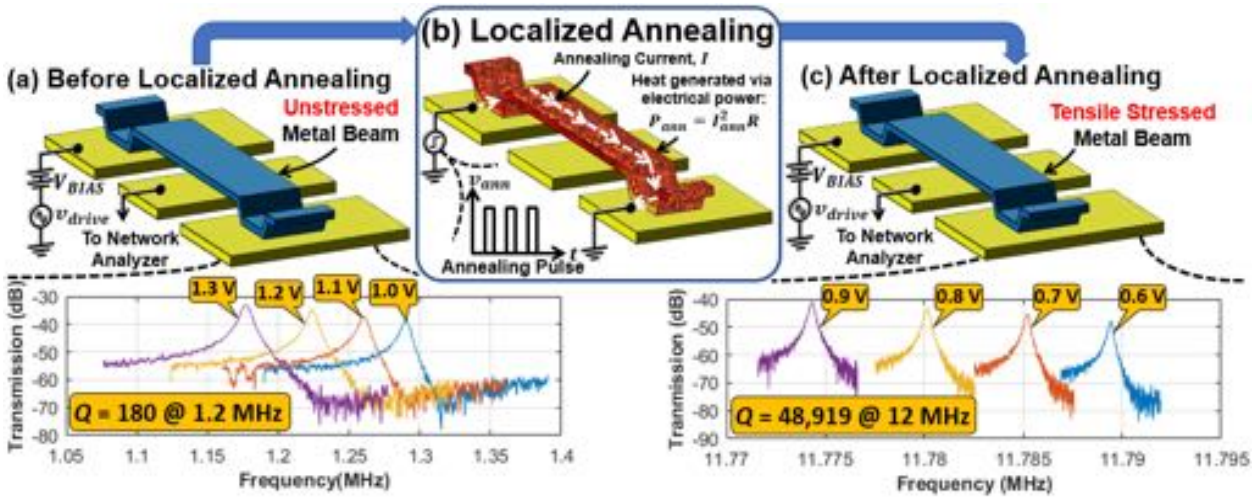


Fig. 6.4: Measured frequency response vs. DC bias voltage for a 12.8μm-long, 2μm-wide, 45nm-thick Ru CC-beam (a) before and (c) after localized anneal-stressing. (b) Schematic depicting the circuit needed for localized anneal-stressing.

Before presenting the localized anneal-based approach to tensile stress introduction that facilitates MEMS-last integration with transistors, we first confirm and gauge the degree to which tensile stress raises the Q's Ru CC-beams via rapid thermal annealing (RTA). Here, ruthenium CC-beams of different sizes were subjected to various rapid thermal anneals (RTAs) that generated tensile stress by stimulating structure reorganization and grain growth via plastic deformation [107], [108].

To better convey how tensile stress might ensue after an anneal cycle, Fig. 6.5 presents a plot of stress as a function of temperature and time during annealing and cooling periods. Initially, assuming the structural material thermal expansion coefficient is larger than that of the substrate, as the temperature rises the beam strain is predominantly elastic and compressive. When the temperature surpasses a certain value, a combination of excessive compressive strain and temperature induce recrystallization, which grows grains to relieve the stress, actually reduces the compressive stress and brings the total stress closer to zero at the end of the heating cycle.

When heating stops, the cooling process begins. Now the structure, with its relatively larger thermal expansion coefficient, shrinks faster than the substrate. Since the stress at the start of the cooling process was considerably smaller than if no recrystallization had occurred, very little of the beam shrinking during cooling goes towards compensation of compressive stress, so the beam goes into heavy tension. Tension values on the order of 700-900 MPa are typical in this work.

Using (6.2), curve fitting measured frequency versus beam length curves as in Fig. 6.6 yields the following values for material parameters: Young's modulus, E = 402.5 GPa and density ρ =13,420 kg/m^3.

Note that for large values of stress, (6.2) reduces to

$$f_o \cong \frac{0.56}{L}\sqrt{\frac{S}{\rho}} \; if \; S \gg 3.4E\left(\frac{H}{L}\right)^2 \tag{6.3}$$

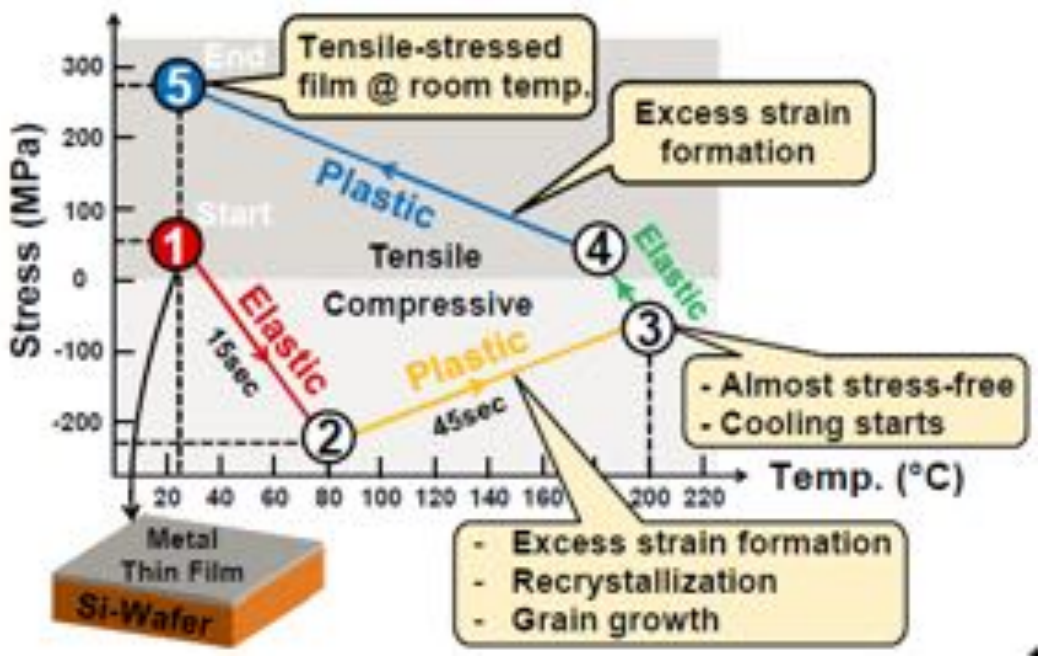


Fig. 6.5: A generic thermal annealing cycle for low-temperature sputtered metals atop Si substrate showing how film stress evolves during heating and cooling.

Here, the stress S becomes a principal determinant of resonance frequency. While on the one hand, some might argue that the frequency stability becomes too dependent on factors that might change the stress; others on the other hand might argue that this strong dependence on stress removes concern for instabilities in other parameters, such as Young's modulus and thickness. Ultimately, if the resonance frequency stability depends only on stress, then this might actually simplify strategies to maximize the stability of an oscillator referenced to this device, since one now need only find a method to stabilize stress. Yes, a tall order, but perhaps not an impossible one.

TABLE 6.I: MEASURED Q'S AND RESONANT FREQUENCIES FOR CC-BEAMS OF DIFFERENT LENGTHS AFTER VARIOUS RTA CONDITIONS

Beam Lengths	***Q* and f_o in Various RTA Conditions**		
	Temperature: 1000℃ ***Time: 3min*** ***Stress (S) : 755MPa***	***Temperature: 1050℃*** ***Time: 1min*** ***Stress (S) : 857MPa***	***Temperature: 1100℃*** ***Time: 1min*** ***Stress (S) : 923MPa***
L = 12.8μm	Q = 8,617 f_o = 10.5MHz	Q = 9,872 f_o = 11.3MHz	Q = 46,666 f_o = 11.7MHz
L = 6.4μm	Q = 6,210 f_o = 20.5MHz	Q = 7,652 f_o = 21.7MHz	Q = 16,040 f_o = 22.5MHz
L = 3.5μm	Q = 1,803 f_o = 38.2MHz	Q = 2,576 f_o = 39.8MHz	Q = 5,562 f_o = 42.9MHz

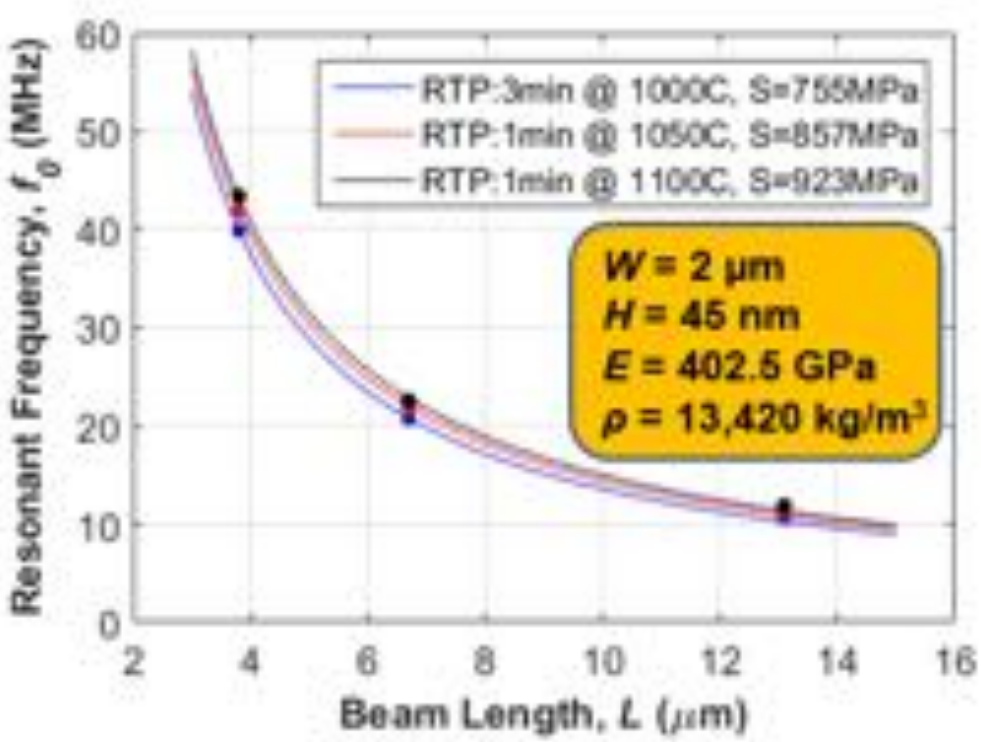


Fig. 6.6: Curve fitting measured frequency versus beam length where dots represent actual measured data and solid lines are analytically determined curves using (6.2).

The dominance of stress as a determinant in (6.3) also suppresses the influence of non-idealities on resonance frequency. This can greatly facilitate design. For example, for the beams measured in this work, the large stress obviates the beam topography factor that would otherwise reduce the resonance frequency of a CC-beam from the theoretically expected value.

Returning to the influence of stress on Q, Table 6.I documents the increase in frequency and Q experienced by beams of different lengths under various amounts of RTA-induced tensile stress. As shown, introduction of tensile stress raises the frequency of the Fig. 6.4(a) device by almost 10 times. In addition, 923 MPa tensile stress provides an impressive 256 times increase in Q, taking the Q of the Fig. 6.4(a) device from 180 to 46,066!

6.5. Localized Annealing

Although the results of Table 6.I are quite compelling, the RTA temperatures used therein could unfortunately degrade foundry CMOS transistors. This work circumvents this problem via use of localized Joule-heating, first demonstrated in [109], that raises only the MEMS resonator device to the needed stress-inducing temperature, keeping any underlying transistors near room temperature. Here, the circuit of Fig. 6.4(b) simply applies a voltage V_{ann} across the beam anchors, which then sends a current I_{ann} through the beam that Joule heats it to a desired temperature, generating tensile stress in the process. The tiny size of the device presents a correspondingly tiny thermal capacitance, allowing the beam to be heated to over 1000°C in milliseconds, which in turn allows fast pulsed annealing for more precise stress control.

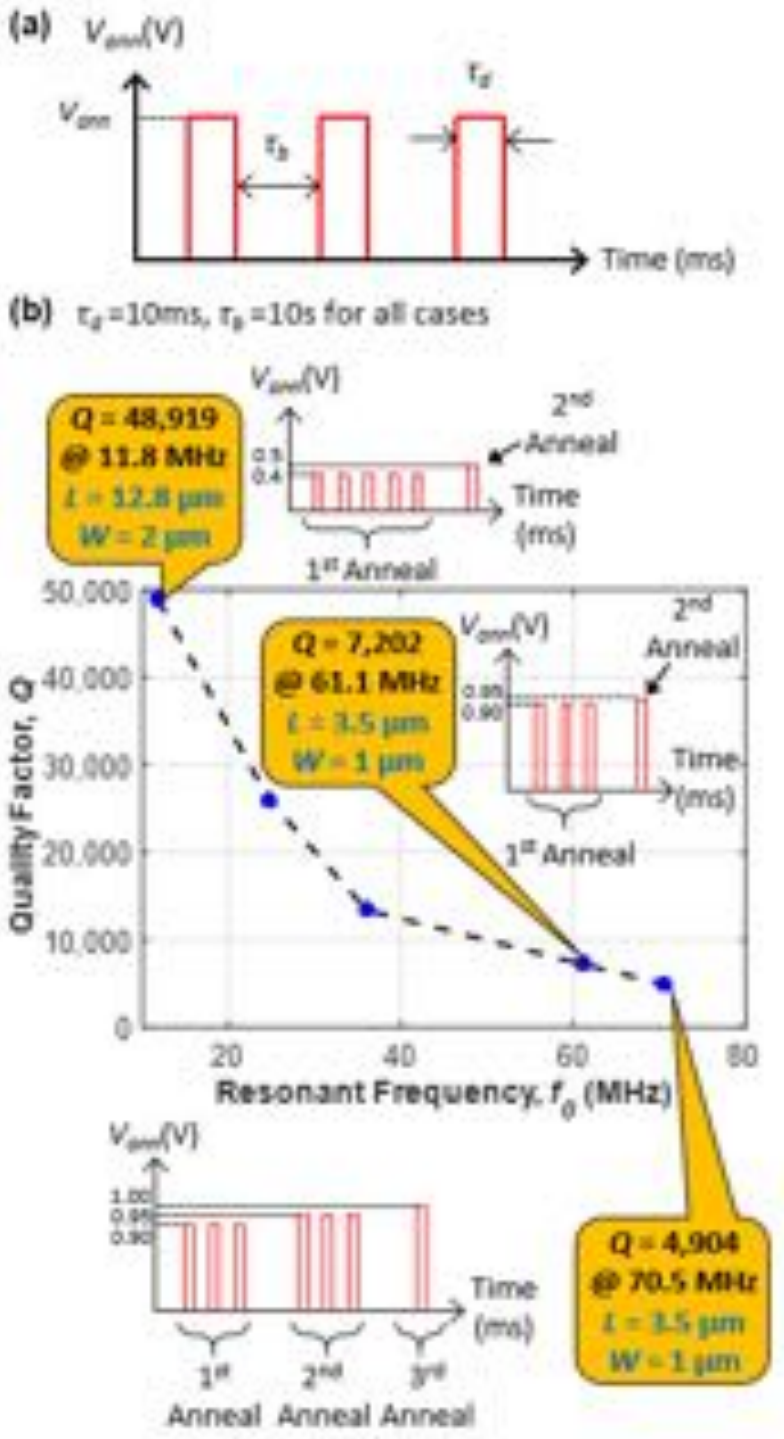


Fig. 6.7: (a) Pulse train localized annealing waveform used in this study. (b) Q after localized anneal-stressing as a function of beam frequency along with the localized annealing pulse conditions for certain frequencies.

6.6. Localized Anneal-Induced *Q*-Boosting

Localized annealing experiments took advantage of the fast heating time constants characteristic at the micro-scale by heating via pulsed voltage train sequences, as shown in Fig. 6.7(a), which

were applied across the beam annealing terminals. Here, (V_{ann}, τ_d, τ_b) sets describe specific pulse train types, where τ_d is pulse duration, and τ_b is spacing between pulses. A frequency response measurement to extract the resonance frequency and Q followed each pulse or pulse-train anneal step.

The measurement procedure was such that each device experienced successively stronger annealing each time it survived an anneal step. Specifically, if a device survives a first anneal set, the next anneal set raised the ante by either raising V_{ann} or adding pulses. This procedure continued until either excessive Joule heating destroys the beam or tensile stress breaks the beam or damages its anchors.

Fig. 6.4(c) presents frequency characteristics after localized anneal-induced stressing for a ruthenium metal CC-beam resonator with L = 12.8 μm, W = 2 μm, and H = 45 nm at various DC bias voltages. Here, the previous 1.2 MHz resonance frequency now approaches 12 MHz with a Q of 48,919 more than 272 times higher than the previous 180. Clearly, localized anneal-stressing is a game-changer for Ru metal CC-beams.

Fig. 6.7(b) gauges the efficacy of localized anneal-stressing as a function of resonator frequency by plotting measured Q versus frequency. As expected, an obvious drop in Q with increasing frequency occurs due to larger anchor loss at higher frequencies. Nevertheless, because these metal resonators are considerably thinner than previous CC-beam designs, their Q's remain high at higher frequencies, on the order of 7,202 and 4,904 at 61 and 70 MHz, respectively. These are considerably higher than the 300 typically measured for 2 μm-thick 70-MHz polysilicon CC-beams.

6.7. Conclusions

By posting Q's of 48,919 at 11.8 MHz and 4,904 at 70 MHz, both many times higher than the 6,000 and 300 typical of 2 μm-thick polysilicon counterparts, the 45 nm-thick localized anneal-stressed ruthenium metal resonators demonstrated herein may soon enable oscillators with considerably better phase noise than achieved with previous polysilicon CC-beams. Although methods to insure adequate long-term stability, e.g., via alloying, still require exploration, the results reported herein certainly enhance the feasibility of MEMS-last CMOS-MEMS integration using metal structural material.

Chapter 7
Widely Tunable 20-nm-Gap Ruthenium Metal Square-Plate Resonator

This chapter presents a capacitive-gap transduced flexural-mode square-plate resonator constructed in rapid-thermal-annealed (RTA'ed) ruthenium metal that posts quality factors (Q's) exceeding 5,000 and an impressive transducer strength C_x/C_o (equivalent to k_t^2) of up to 71% intrinsic and 36% with 55fF of bond capacitance loading, which in turn permits more than 46% voltage-controlled resonance frequency tuning (from 18.005 to 9.713MHz) with a voltage excursion from 0.5 to 2.8V. The 36% C_x/C_o is 75 times larger than the 0.48% of published AlN piezoelectric material in this HF frequency range [85]. With processing temperatures potentially below 350°C (with localized annealing), this metal resonator is amenable to integration directly over even advanced node CMOS [110], making this technology attractive for single-chip widely tunable filter and oscillator applications, e.g., for wireless communications [79].

7.1. Introduction

Low metal material deposition temperatures have long enticed researchers seeking to integrate MEMS directly over CMOS. However, metal resonators have historically suffered from low Q relative to polysilicon or diamond counterparts [101], with metal Q's for flexural modes generally in the range of 180 [101]. Recent demonstration of a localized anneal-based method to boost the Q's of Ru metal clamped-clamped beam resonators [96] and reduce aging rates [30] are now making metal attractive once again, especially for timing and communications applications. However, for applications like the super-regenerative transceiver of [12], for which resonance frequency sets the receivable channel range, such resonators would be even more useful if their frequencies were voltage-tunable over larger ranges than the 80 kHz previously shown in [12]. This work achieves a more than 100 times increase in tuning range via use of a nano-scale square-plate resonator design with 20-nm electrode-to-resonator gaps.

7.2. Device Structure and Model

Fig. 7.1 presents the perspective view of the square-plate resonator with dimensions and in a typical bias and excitation circuit configuration. The device is similar in structure to that of [37], but differs in its use of Ru metal structural material and interconnects (as opposed to polysilicon), as well as much smaller dimensions. Here, the 3.4-µm side length, 75-nm thickness, and 20-nm electrode-to-resonator gap are much smaller than the 16-µm, 2.2-µm, and 90-nm of [37]. The inset in Fig. 7.1 presents the trampoline mode shape that permits larger pull-in voltages than other designs. Tensioning via annealing [37] further strengthens it against pull-in, allowing it to stay suspended even with 2.8V across its 20-nm electrode-to-resonator gap. This then enables intrinsic and loaded C_x/C_o's of 71.2% and 36.1%, respectively, that permit the described wide tuning range.

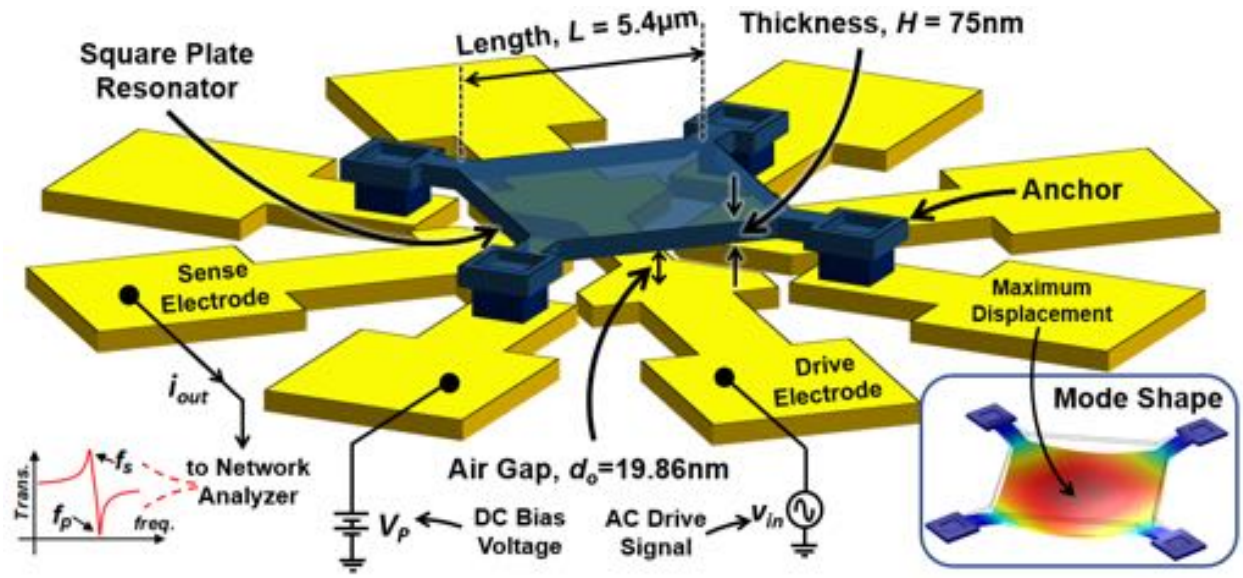


Fig. 7.1: The square plate device described herein in a typical operating circuit with dimensions. The inset shows the finite element analysis (FEA) simulated mode shape.

To elaborate on this, the Rayleigh-Ritz method offers a convenient approach to generate an expression for the trampoline mode shape employed here [111]. This method begins with a guess for the mode shape function Z_{mode} that satisfies the fixed boundary conditions at the four corners. For a square plate of edge size L centered at the origin, one good guess takes the form

$$Z_{mode}(x,y) = a_1\left\{2-\left(\frac{2x}{L}\right)^2-\left(\frac{2y}{L}\right)^2\right\}+a_2\left\{1-\left(\frac{2x}{L}\right)^2\left(\frac{2y}{L}\right)^2\right\} \tag{7.1}$$

where x and y are independent coordinate variables. a_1 and a_2 are adjustable parameters that minimize the difference between the total strain energy and work done by a point load of F applied at the center of the plate when taking values

$$a_1 = \frac{FL^2}{512D(1+\nu)}\frac{43-45\nu}{6-5\nu} \tag{7.2}$$

$$a_2 = \frac{15FL^2}{512D(6-5\nu)} \tag{7.3}$$

where ν is Poisson's ratio and D is flexural rigidity:

$$D = \frac{EH^3}{12(1-\nu^2)} \tag{7.4}$$

where E is Young's modulus and H is the square plate thickness. Use of (7.1) - (7.4) yields the equivalent mechanical stiffness k_m at the center of the square plate

$$k_m = \frac{128EH^3}{3L^2}\frac{6-5\nu}{(1-\nu)(101-75\nu)} \tag{7.5}$$

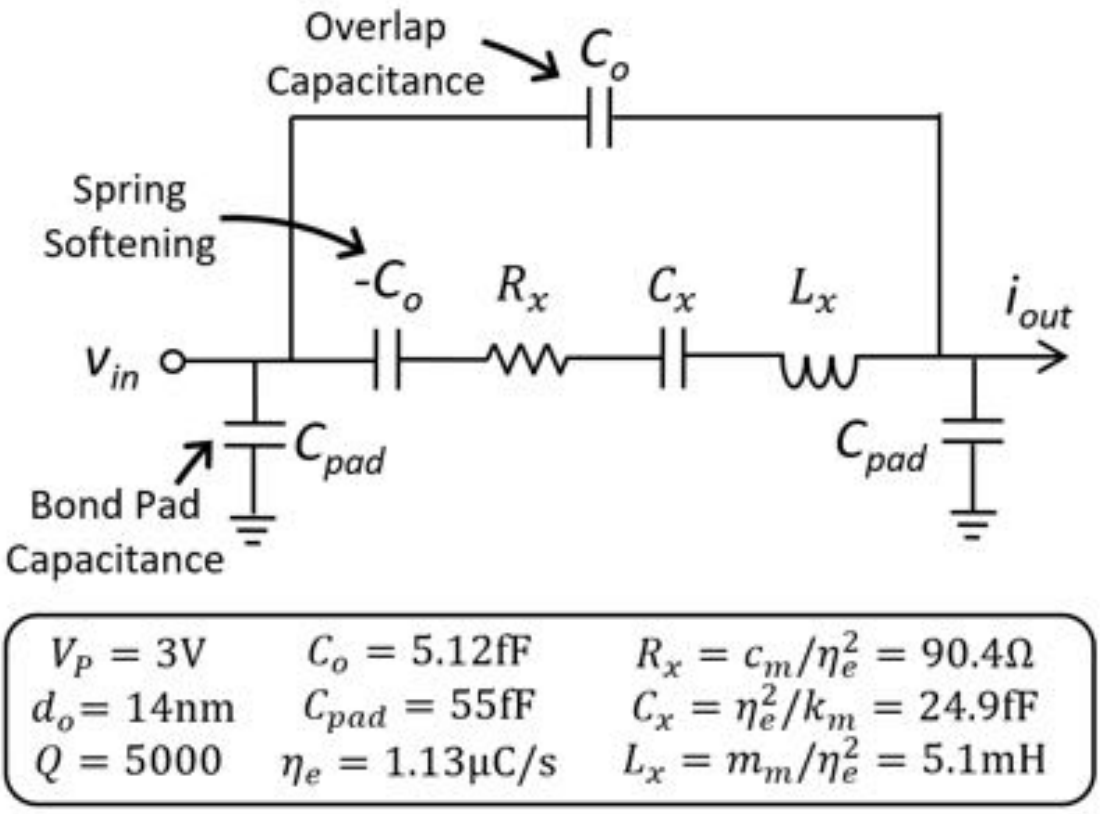


Fig. 7.2: Equivalent circuit for a square plate resonator operated as a one-port. Numerical values are for the device alone, i.e., with no parasitic line resistance.

The dynamic mass referenced to the highest velocity point, i.e., the square plate center, takes the form [49]

$$m_m = \frac{\rho H \iint Z_{mode}^2 \, dx \, dy}{Z_{mode}^2(x=0, y=0)} = \kappa_{sq} \rho H L^2 \tag{7.6}$$

where κ_{sq} is mass modification factor given as 0.559 for ruthenium with $\nu = 0.3$. Substituting (7.5) and (7.6) in the well-known resonance frequency expression leads to

$$f_{nom} = \frac{1}{2\pi}\sqrt{\frac{k_m}{m_m}} = \frac{1}{2\pi}\frac{H}{L^2}\sqrt{\frac{E}{\rho}\frac{128}{3\kappa_{sq}}\frac{6-5\nu}{(1-\nu)(101-75\nu)}} \tag{7.7}$$

where ρ is density. For the device studied in this work with $H = 75\text{nm}$, $L = 3.4\mu\text{m}$, $E = 402.5\text{GPa}$, $\rho = 13420\text{kg/m}^3$, and $\nu = 0.3$, (7.7) predicts a trampoline mode resonance frequency of 14.138MHz.

To complete the device equivalent circuit, the electromechanical coupling factor η_e referenced to the square-plate center takes the form [44]

$$\eta_e = \gamma \frac{V_P C_o}{d_o} \tag{7.8}$$

where V_P is the dc-bias voltage, C_o is the total electrode-to-resonator overlap capacitance, d_o is the electrode-to-resonator gap, and γ is a parameter that modifies the electromechanical coupling of an ideal parallel-plate capacitive-gap transducer to account for a non-constant resonance displacement (or velocity) profile over the electrode area [44] given by

$$\gamma = \frac{1}{L^2} \frac{\iint Z_{mode}(x', y')\, dx'\, dy'}{Z_{mode}(x, y)} \tag{7.9}$$

The dependence of the electromechanical coupling factor on the second power of the electrode-to-resonator gap spacing makes clear that smaller gaps can greatly increase the electromechanical coupling, as well as the electromechanical coupling strength, which takes the form

$$\frac{C_x}{C_o} = \gamma^2 V_P^2 \frac{(1-\nu)(101-75\nu)}{6-5\nu} \frac{3\varepsilon_o L^4}{128 E H^3 d_o^3} \tag{7.10}$$

Equation (7.9) together with (7.5) - (7.8) now allow specification of the device equivalent circuit in Fig. 7.2.

7.3. Structure-Assisted Tuning Range

Voltage-controlled resonance frequency tuning for the square-plate resonator comes about via the well-known electrical stiffness associated with any parallel-plate capacitive-gap transducer. Electrical stiffness not only renders the resonance frequency f_o a strong function of dc-bias voltage V_P, it also often sets the maximum value of V_P before the onset of device pull-in. The expression for the electrical stiffness k_e acting on the V_P-biased Fig. 7.1 square-plate resonator with all electrodes grounded is [44]

$$k_e = \frac{\eta_e^2}{C_o} = V_P^2 \gamma^2 \frac{\varepsilon_o L^2}{d_o^3} \tag{7.11}$$

when taking as a reference point the maximum displacement location indicated in the trampoline mode shape in Fig. 7.1 inset, γ is 0.722.

This electrical stiffness acts against the resonator's mechanical stiffness to lower the resonance frequency according to

$$f_o = f_{nom} \sqrt{1 - \frac{k_e}{k_m}} = f_{nom} \sqrt{1 - \frac{C_x}{C_o}} \tag{7.12}$$

where

$$k_m = \frac{\eta_e^2}{C_x} \tag{7.13}$$

permits the rightmost form. Equation (7.12) shows that k_e/k_m is the same as the intrinsic, i.e., no parasitics, C_x/C_o of the resonator. Thus, the higher the C_x/C_o, the larger the frequency tuning range. From (7.10) and (7.12), the 20-nm initial electrode-to-resonator gap of this work contributes to a large C_x/C_o and correspondingly large frequency tuning range.

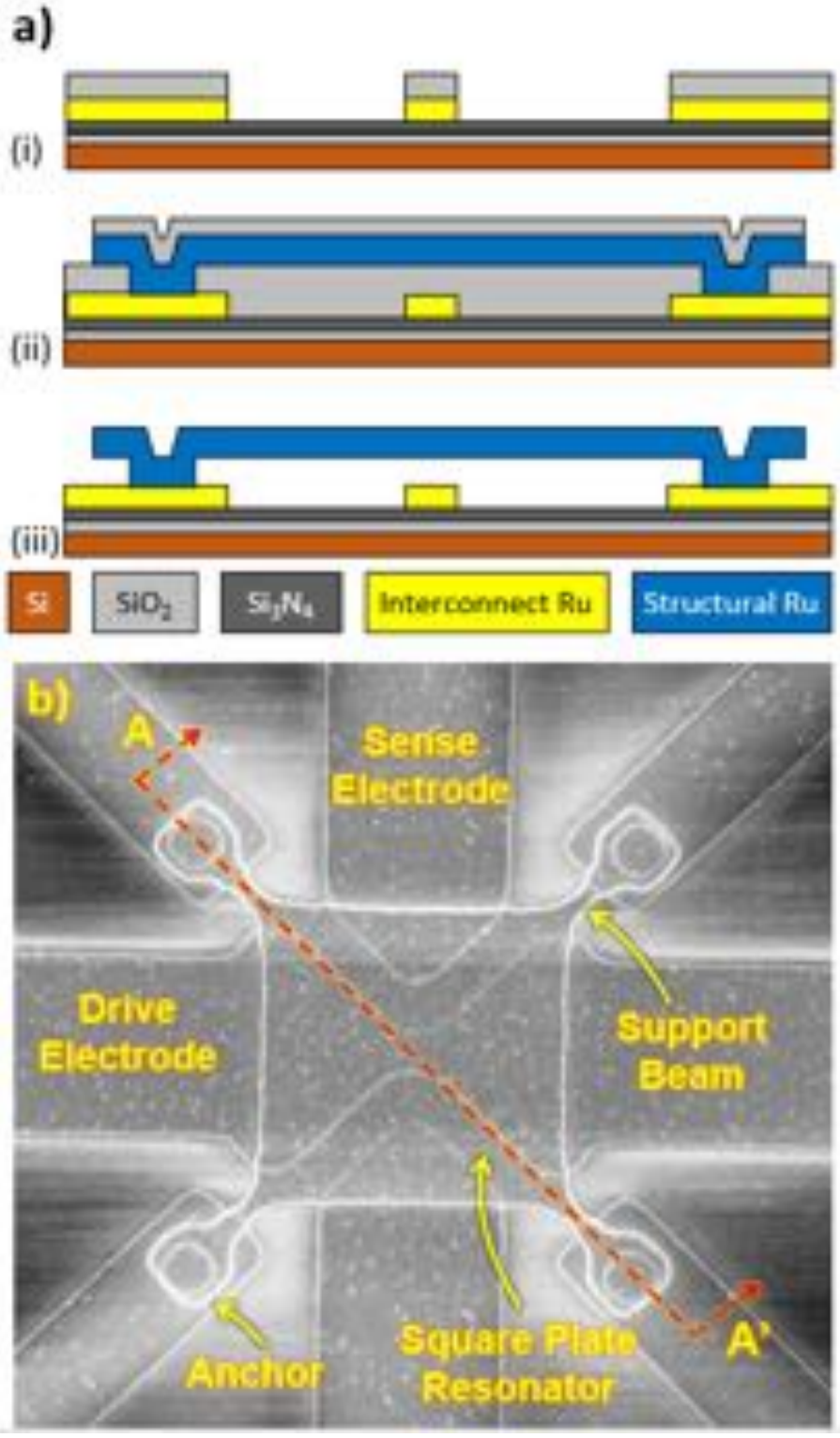


Fig. 7.3: a) Cross-sections through AA' after (i) interconnect layer etch (ii) structural layer etch (iii) HF release. b) SEM of a fabricated ruthenium metal square plate.

The smaller stiffness of this nano-scale square-plate device enhances the frequency tuning range not only by increasing the k_e/k_m term in (7.12), but also by allowing the increasing dc-bias voltage

to pull the device closer to its underlying electrode. In particular, unlike much stiffer devices with small gaps, e.g., the 13-nm-gap wine-glass disk of [45], this trampoline-mode square-plate device under 2.8V dc-bias bends significantly under the attractive force, reducing the original 20-nm gap by 33% at the plate center and increasing C_x/C_o accordingly (to 71%)!

Fortunately, as described in [96], the rapid-thermal anneal treatment given to this device not only raises its Q, but also generates tensile stress that tightens its stiffness somewhat, allowing it to stay suspended even at the 2.8V dc-bias voltage of maximum frequency tuning. At higher voltages, the device pulls in.

7.4. Fabrication

The metal surface micromachining fabrication process for ruthenium square-plate resonators was similar to that for previous clamped-clamped beams [96], except for use of a much smaller SiO_2 sacrificial spacer layer to achieve 20-nm initial electrode-to-resonator gaps. Fig. 7.3(a) presents cross-sections summarizing this process, showing the use of ruthenium for both the structure and its electrodes and silicon dioxide as the sacrificial layer and as a hard mask for precise lithography and etching. Fig. 7.3(b) presents the SEM of a freshly fabricated square plate resonator, indicating important structural and design details.

Instead of the post-fabrication localized annealing used in [96], the square plates experienced conventional rapid-thermal annealing (RTA) at 850°C for 180 seconds with 30-second temperature rise and fall times. This was a time-saving measure that (as will be seen) ended up as effective in raising device Q's. Whether this would be acceptable as a post-CMOS step is yet to be seen. If not, then localized annealing is always an option.

7.5. Experimental Results

A Lakeshore FWPX Vacuum Probe Station housed and electrically accessed Ru square-plate devices during measurement. Fig. 7.3(a) and (b) present vacuum-measured transmission spectra before and after annealing, respectively, clearly showing both a frequency shift and an increase in Q. In particular, fabricated Ru square-plate devices posted Q's in the range of only 600 before RTA. After RTA, their Q's rose to over 5000 at a dc-bias of 0.5V. RTA also permits a much wider frequency tuning range, from 18.005 to 9.713MHz over 0.5 to 2.8V—a 46% range. Needless to say, this is an astonishing range of frequency not often (if ever) seen in a resonator with such a high Q. The larger RTA'ed tuning range likely results from tensioning that flattens the square plate, bringing it closer to its electrode than an un-annealed counterpart.

A curve fit of the plot of resonance frequency versus dc-bias in Fig. 7.5(a) with electrical stiffness theory [84] confirms an initial electrode-to-resonator gap spacing of 21.95nm at V_P=1V and a final spacing of 14.69nm at the highest applied V_P=2.8V. The very fast change in frequency with dc-bias on the left side of the plot confirms the role of gap reduction as the square plate bends closer to the electrodes under the large (μN-range) attractive force.

Since from (7.12) the intrinsic (i.e., unloaded) C_x/C_o essentially equals k_e/k_m, another curve fit also yields the plot of intrinsic (i.e., unloaded) C_x/C_o versus dc-bias in Fig. 7.5(b), where 2.8V yields a whopping 71.2%!

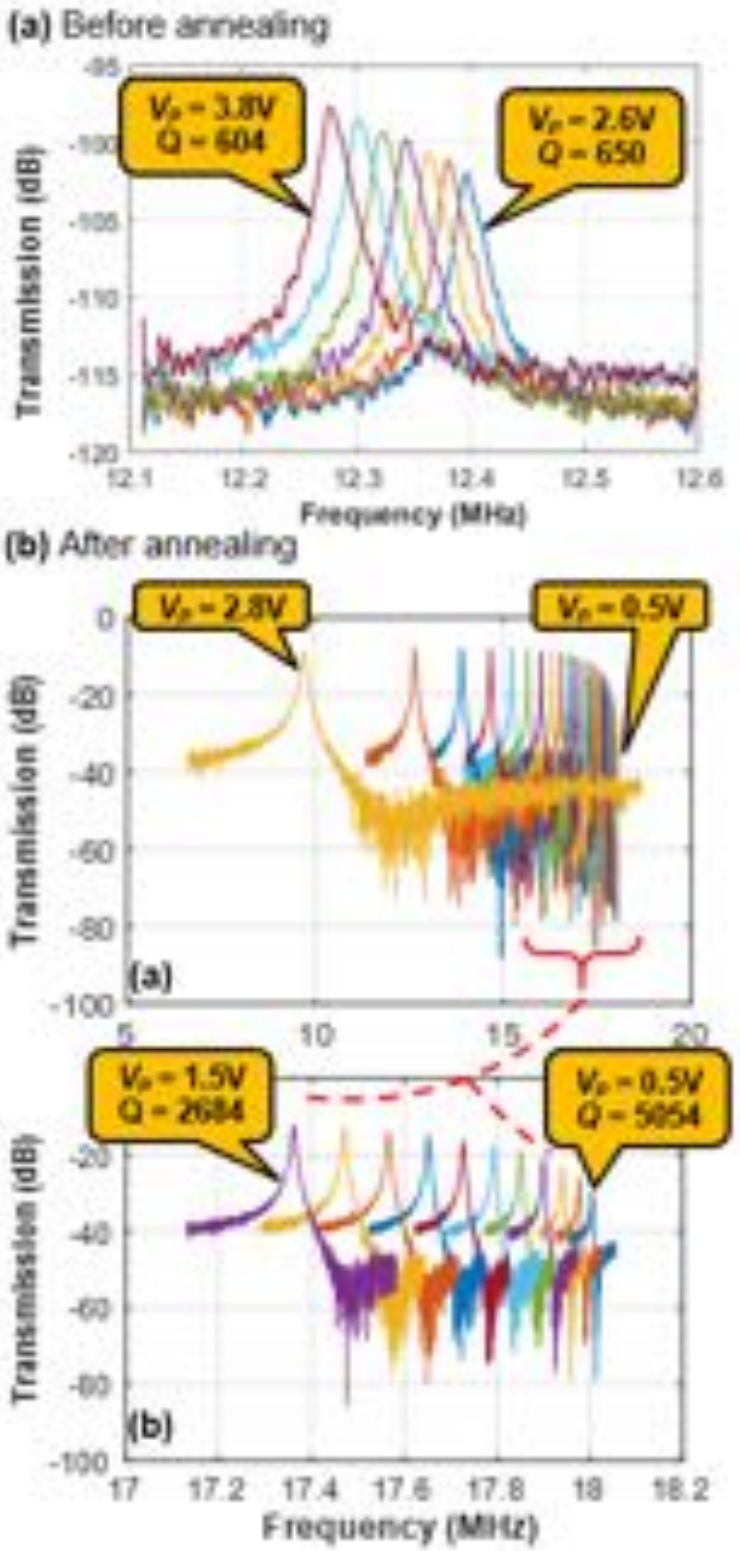


Fig. 7.4: Measured frequency spectra for a ruthenium metal square plate resonator as a function of dc-bias voltage (a) before RTA using mixing V_{LO} = 1V_{pp}, f_{LO} = 6MHz, P_{RF} = -3dBm (b) after RTA using direct measurement.

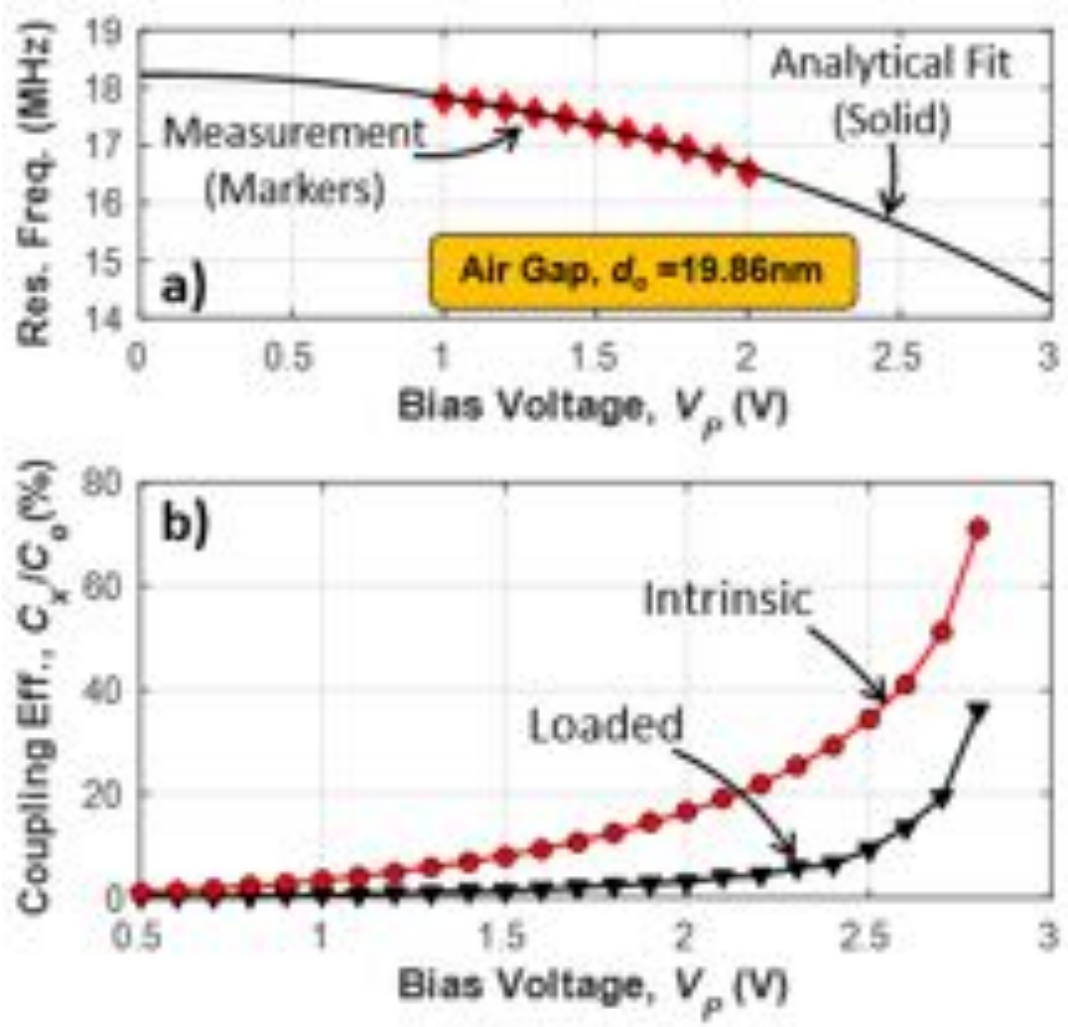


Fig. 7.5: a) Measured frequency versus dc-bias voltage with curve-fit to extract electrode-to-resonator gap. b) Intrinsic and loaded C_x/C_o versus dc-bias voltage.

The practical C_x/C_o is not this large, as it suffers somewhat from loading by parasitic capacitance. In particular, in any real situation parasitic capacitance (in the leads, measurement circuit, etc.) adds to the C_o in C_x/C_o, lowering its actual value. The common approach to attaining C_x/C_o via measurement of parallel and series resonance frequencies, f_p and f_s (indicated in Fig. 7.1), respectively, then using

$$\frac{C_x}{C_o} = 1 - \left(\frac{f_s}{f_p}\right)^2 \tag{7.14}$$

in fact yields the loaded C_x/C_o.

Fig. 7.5(b) uses (7.14) to also plot the loaded C_x/C_o versus V_P, which now sports a still-impressive value of 36.1% at V_P = 2.8V. While C_x/C_o rises with dc-bias, the Q drops due to loading by parasitic interconnect resistance, which is comparable to the motional resistance at high dc-bias, e.g., motional resistance R_x=486Ω at 2.1V. Nevertheless, the device still achieves large intrinsic and loaded (C_x/C_o)-Q products of 274 and 56 at V_P = 2.1V.

7.6. Conclusions

Many who work with high Q resonators, practitioners and researchers alike, are familiar with the adage that high Q resonators are simply not tunable, meaning that some other means to realize tuning, e.g., phase-locking to a (dirty) voltage-controlled oscillator, is necessary. The resonator of this work challenges this assumption and could be a potential game-changer for many applications that benefit from frequency tuning, including tunable oscillators and filtering for RF front-ends. The benefits of this go over and beyond the already important benefit of CMOS-compatibility, which this high-Q ruthenium structural material achieves when localized annealed [96].

Aside from tuning, note that all of the measured values—Q, C_x/C_o, tuning range, k_t^2-Q—are not only impressive for CMOS-compatible metal material, but also better than or competitive with other common micromachinable resonator materials in this frequency range, including polysilicon, diamond, and AlN. Whether they can also compete from a stability perspective, especially long-term stability, remains to be seen.

Chapter 8
Conclusions

This dissertation presented a hierarchical, intuitive, and technology agnostic procedure for designing RF channel-select filters, followed by an actual demonstration solidly confirming the validity of the design method. Two distinct methods that followed aimed at increasing the resonator electromechanical coupling coefficient to substantially improve the functionality of the demonstrated filter for future applications that require higher-order filters with sharper roll-off characteristics and less passband ripple as well as wider bandwidth. To increase the device functionality even further, the last part of this thesis introduced a fabrication and post-processing method using CMOS-compatible ruthenium metal that allows integration of micromechanical devices such as aforementioned RF filters atop CMOS.

8.1. Achievements

Chapter 2 introduced design, fabrication, and experimental demonstration of a differential input/output RF channel-select micromechanical disk filter consisting of 96 mechanically coupled capacitive-gap-transduced polysilicon disk resonators, centered at 224MHz with only 0.1% (9kHz) bandwidth all while attaining 2.7dB insertion loss and more than 50dB out-of-channel stopband rejection. Combined with inherent high-Q's of capacitive-gap disk resonators, sub-40nm transduction gaps enabled by the sidewall sacrificial layer fabrication technology and defensive design strategies employing buffer disks against fabrication residual stress were instrumental in obtaining this impressive performance with decent yield and RF-compatible 590Ω filter termination impedance. It is also worth noting that the spurious-free filter spectrum achieved in this work with more than 50dB out-of-channel stopband rejection is a direct result of the differential input/output scheme utilized in the design and granted by the flexibility of all-mechanical design. Perhaps most encouraging, the equivalent circuit model developed for this complicated structure based on mechanical and electrical parameters was spot on in capturing not only the ideal filter response, but also the parasitic nonidealities that might distort the filter performance. This implies that the GHz-filters with sub-200-Ω impedances enabled by sub-20-nm transduction gaps predicted by the same model might soon come true, bringing this technology even closer to realizing the ultra-low-power channel-selecting RF front-ends.

Having presented an initial RF channel-select filter demonstration, Chapters 3-5 then focused on design methods and fabrication techniques that could take the filter performance one step further by substantially increasing the electromechanical coupling coefficient of the resonators constituting such a filter. Specifically, Chapter 3 introduced a new type of a resonator formed via hollowing out a capacitive-gap transduced radial mode disk resonator that achieved a measured electromechanical coupling strength (C_x/C_o) of 0.75% at 123 MHz without the need to scale the device's meager 40-nm electrode-to-resonator gap. This is almost 7× improvement in C_x/C_o compared with a conventional radial contour-mode disk at the same frequency, same dc bias, and same gap. It also comes about via a fabrication process that deviates only slightly from a standard disk

resonator process. C_x/C_o increases like this should improve the passbands of channel-select filters targeted for low power wireless transceivers, as well as lower the power consumption of MEMS-based oscillators.

Considering the dependence of the electromechanical coupling on the actuation gap is inverse cubic compared to the linear dependence on the mass, Chapters 4-5 attempted to obtain strong coupling by reducing the actuation gaps to levels below 10nm from their current 37nm. To realize such an endeavor, one must first overcome fabrication-related hurdles such as precise thin film residual stress control, smooth post-etch sidewalls free of asperities, and sub-10nm sacrificial layer conformal deposition. Considering compressive stresses as low as 50MPa are sufficient to cause shorts with a sub-10nm-gap 200-MHz upper-VHF polysilicon disk resonator, Chapter 4 attacked the first hurdle by introducing an on-chip strain measurement device that harnesses precision frequency measurement to precisely extract sub-nm displacements, allowing it to determine the residual strain in a given structural film with best-in-class accuracy, where stress as small as 15MPa corresponds to 2.9nm of displacement. The approach specifically harnesses a spoke-supported ring structure surrounded both inside and outside by balanced capacitive-gap transducers that pull its resonance frequency according to strain-induced changes in inner and outer electrode-to-structure gap spacing. The use of a ring structure with balanced electrodes further eliminates uncertainty in the starting gap spacing, which in turn enhances accuracy. The importance of attaining such accuracy manifests in the fact that knowledge of residual strain might be the single most important constraint on the complexity of large mechanical circuits, such as RF channel-select filters.

Having optimized the deposition parameters to achieve minimal post-fabrication residual stress by employing such a strain diagnostic presented in Chapter 4 and fabricated alongside real devices, Chapter 5 then addressed the remaining hurdles for achieving sub-10nm gaps by using a modified polysilicon etch recipe that generates considerably smoother sidewalls to reduce the asperities that might otherwise intensify electric fields causing breakdown and an atomic layer deposited (ALD) 8nm-thick SiO_2 sidewall sacrificial layer defining the record narrow transduction gap achieves perfect conformality. The single-digit-nanometer electrode-to-resonator gaps demonstrated in this chapter have enabled 200-MHz radial-contour mode polysilicon disk resonators with motional resistance R_x as low as 144Ω while still posting Q's exceeding 10,000, all with only 2.5V dc-bias. The demonstrated gap spacings down to 7.98nm are the smallest to date for upper-VHF micromechanical resonators and fully capitalize on the fourth power dependence of motional resistance on gap spacing. High device yield and ease of measurement debunk popular prognosticated pitfalls often associated with tiny gaps, e.g., tunneling, Casimir forces, low yield, none of which appear. The tiny motional resistance, together with (C_x/C_o)'s up to 1% at 4.7V dc-bias and (C_x/C_o)-Q products exceeding 100, propel polysilicon capacitive-gap transduced resonator technology to the forefront of MEMS resonator applications that put a premium on noise performance, such as radar oscillators. Simultaneous high-Q and strong electromechanical coupling (C_x/C_o) provided by this method makes this technology attractive for future sharp roll-off, flat passband RF channel-select filters targeted for low power receivers as well as wide band filters targeted for the LTE bands.

The decent resonator performance offered by polysilicon structural material with Q's exceeding 10,000 at 200MHz comes with a drawback that LPCVD polysilicon with deposition temperatures of 590-615°C is not directly integrable atop CMOS due to thermal budget constraints. For this reason, the adopted two-chip approach to interface micromechanical resonators and filters with the transistor circuits incurs inevitable parasitics causing undue power consumption, performance degradation, and cost increase. Pursuant to mitigating this issue, Chapter 6 introduced a fabrication

and post-processing method using CMOS-compatible ruthenium metal that allows integration of micromechanical devices such as aforementioned RF filters atop CMOS. Specifically, introduction of tensile stress via localized Joule heating has yielded some of the highest metal MEMS resonator Q's measured to date, as high as 48,919 for a 12-MHz ruthenium micromechanical clamped-clamped beam ('CC-beam'). The high Q's continue into the VHF range, with Q's of 7,202 and 4,904 at 61 and 70 MHz, respectively. These marks are substantially higher than the 6,000 at 10 MHz and 300 at 70 MHz previously measured for polysilicon CC-beams, defying the common belief that metal Q cannot compete with conventional micromachinable materials. The low-temperature ruthenium metal process, with highest temperature of 450°C and paths to an even lower ceiling of 200°C, further allows for MEMS post-processing directly over finished foundry CMOS wafers, thereby offering a promising route towards fully monolithic realization of CMOS-MEMS circuits, such as needed in communication transceivers. This, together with its higher Q, may eventually make ruthenium metal preferable over polysilicon in some applications.

Finally, Chapter 7 fulfilled the promise of this dissertation in metals, i.e., *simultaneous* high-Q and strong coupling, by demonstrating the Q-boosting concept and thermal annealing method presented in Chapter 6 by employing a 20-nm-gap CMOS-compatible capacitive-gap transduced flexural-mode square-plate resonator constructed in thermal-annealed ruthenium metal that posts quality factors (Q's) exceeding 5,000 and an impressive transducer strength C_x/C_o (equivalent to k_t^2) of up to 71% intrinsic and 36% with 55fF of bond capacitance loading, which in turn permits more than 46% voltage-controlled resonance frequency tuning (from 18.005 to 9.713MHz) with a voltage excursion from 0.5 to 2.8V. The 36% C_x/C_o is 75 times larger than the 0.48% of published AlN piezoelectric material in this HF frequency range. With processing temperatures potentially below 350°C (with localized annealing), this metal resonator is amenable to integration directly over even advanced node CMOS, making this technology attractive for single-chip widely tunable filter and oscillator applications, e.g., for wireless communications.

8.2. Future Research Directions

The ever-growing need for hand-held communication devices and smart phones with long battery life as well as the vision of connected networks consisting of trillion set-and-forget-type sensors, i.e., internet of things (IoT), will continue to drive research and development on low power wireless transceivers in the upcoming decade and beyond. The concepts investigated in this dissertation lay some important groundwork towards realizing this goal by not only demonstrating a true RF channel-select filter but also providing experimentally proven resonator designs, fabrication processes, a post-processing technique, and a CMOS-compatible resonator material to obtain on-chip simultaneous high quality factor and strong coupling much needed for future low power wireless transceivers.

Pursuant to this, combining sub-10nm gaps presented in this dissertation with the demonstrated RF channel-select filter at a higher frequency, i.e., one of the LTE bands, is an important step towards this goal. To the former, the much smaller gaps will reduce the filter input impedance to RF-compatible levels using CMOS-compatible dc-bias voltages and without requiring too many array-composite resonators. Also, the strong electromechanical coupling provided by the ultra-small gaps will allow higher order filters with better roll-off characteristics and less passband ripple desperately needed for better frequency spectrum utilization as the number of users and bandwidth demand constantly increase. To the latter, mere downscaling of the disk radius achieves the

needed frequency increase. However, especially near GHz frequencies with a polysilicon disk resonator, the stem becomes a large portion of the entire disk significantly lowering the achievable quality factor. For this reason, either employing alternative resonator technologies more suitable for ultra-high frequency (UHF) regime, i.e., capacitive-gap ring resonators, or using resonator structural materials with high acoustic velocity, i.e., diamond, will be critical to attain LTE frequencies by retaining the high quality factor inherent to the capacitive-gap resonator technology.

Investigating quantum mechanical phenomena such as the Casimir force and tunneling that come into play for ultra-small capacitive gaps is another interesting research direction to follow. As this dissertation briefly mentioned, the Casimir force starts becoming increasingly effective in lowering the pull-in voltage for gaps below 6nm in a 200MHz polysilicon device putting a practical limit to the lowest achievable actuation gap. Noting that the Casimir force is directly proportional to the actuation area and UHF disk resonators are much stiffer than their lower-frequency counterparts, however, hints that this should be less of an issue as the frequencies increase. Although there is so far no definitive theoretical and experimental proof that quantum mechanical tunneling is an effective mechanism for gaps around 8nm, calculations show that the tunneling current becomes comparable to the resonator motional current for gaps below 2-3nm.

Monolithic integration of micromechanical resonators atop CMOS circuits has long been a pursuit for MEMS researchers. Ruthenium metal resonator structural material presented in this thesis combined with the low temperature fabrication and post-processing technology open up this chapter again by offering comparable or better resonator performance than its polysilicon or AlN counterparts in the same frequency regime. To this end, fabricating RF front-end filters and reference oscillators consisting of the ruthenium resonators of this work directly atop finished CMOS dies or wafers is an appealing next step as such an integration will not only decrease the overall system cost but also enormously increase the device functionality by allowing for more complex electromechanical circuits and significantly reduce power consumption with the elimination of bond pad capacitances and parasitics. Note that the observed decent performance obtained via localized annealing is inherent not only to ruthenium metal. Other low-temperature deposited metals, i.e., gold, aluminum, titanium, molybdenum, titanium nitride etc. also deserve consideration as a resonator material for monolithic CMOS integration

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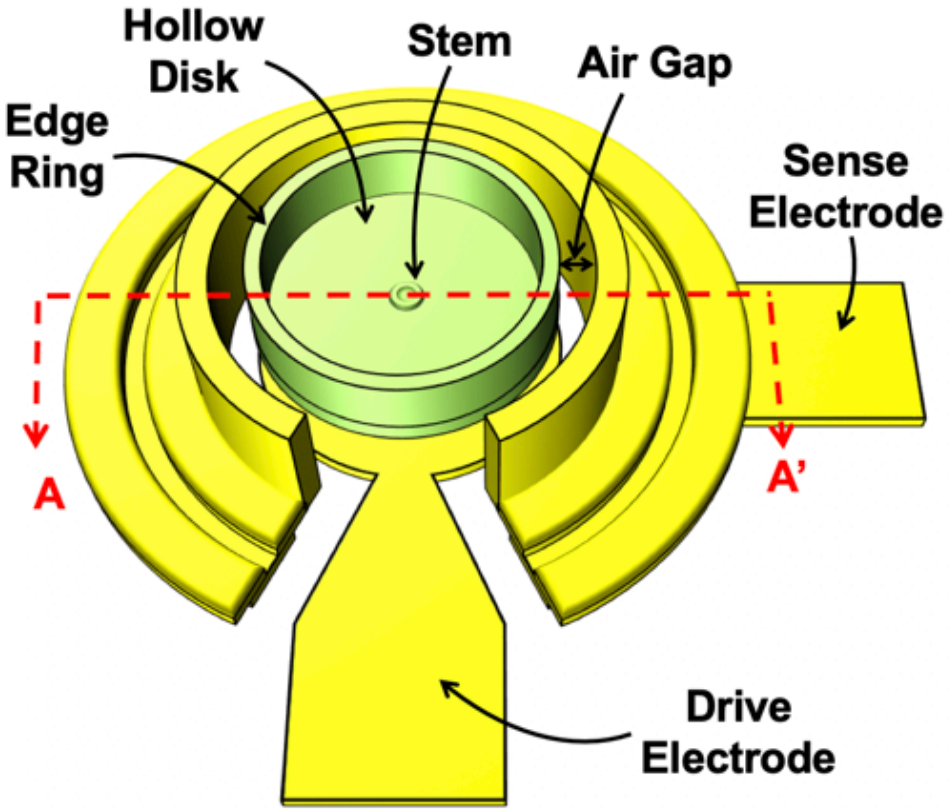
Appendix A
Polysilicon Hollow Disk Process Traveler



0. Tools needed in the Nanolab

Deposition	*Etchers*	*Lithography*	*Metrology*	*Ann./Dope*	*Release*	*Cleaning*
tystar9	lam6	picotrack1	alphastep	tystar2	cpd	msink6
tystar10	lam8	picotrack2	flexus	tystar3		msink8
tystar11	sts2	asml300	cde-resmap	tystar4		msink16
tystar12	sts-oxide	technics-c	nanospec	tystar6		msink18
tystar16	cmp	axcelis	dektak			sinkcmp
tystar17		matrix				

1. Starting wafers (P1-P2, S1-S6, O1-O4, TS0-TS6, TO1-TO4, CS1-4)

Doping: p-type
Wafer Class: prime
Wafer Size: 6”

Scribing: On the front, near the right hand side of the major flat.

Process Note-1: Never scribe the wafer back side as some tools apply vacuum on the back side to keep the wafers still and also to apply helium cooling.

Process Note-2: Make sure the scribing does not have any lines aligned with the Si wafer crystal orientation, making the wafer physically less resistant to mechanical force or impact such as water pressure during quick dump rinse (QDR), mechanical force and/or bending during wafer transfer, rotational force during spin rinse dry (SDR) etc. Use letters like 'S', 'O' that do not have any lines rather than 'I', 'H' or scribe the latter letters in angled way such that they are not aligned with the crystal axis.

Cross Section:

2. Cleaning: Pre-furnace cleaning (P1-P2, S1-S6, O1-O4, TS0-TS6, TO1-TO4, CS1-4)

Nanolab Tool:	msink6		
1st Chemical:	Piranha	*2nd Chemical:*	10:1 HF
Temperature:	120°C	*Temperature:*	Room temperature
Time:	00:10:00	*Time:*	00:02:00

3. Test Deposition: Thin oxide dummy wafer (TS0)

Nanolab Tool: tystar11
Options: tystar9, tystar12, tystar17
Recipe: 11SULTON
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 11.58nm/min
Time: 00:15:00
Process Note: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.

4. Test Metrology: Thin oxide thickness measurement (TS0)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)

Thickness:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Dep. Rate:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____

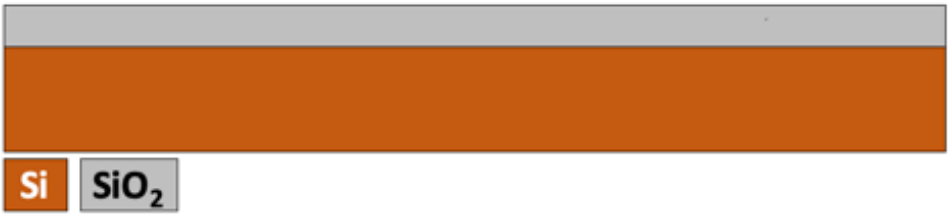
5. Deposition: Thin oxide dummy wafers (O1-O4, TO1-TO4)

Nanolab Tool: tystar11
Options: tystar9, tystar12, tystar17

Recipe: 11SULTON
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 11.58nm/min (adjust if needed)
Time: 00:08:00 (adjust if needed)
Goal: 100nm
Process Note-1: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.
Process Note-2: These wafers will be used as control and test wafers in several subsequent polysilicon depositions. The reason for the very thin oxide layer is because 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

6. Deposition: Isolation oxide (P1-P2)

Nanolab Tool: tystar11
Options: tystar9, tystar12, tystar17
Recipe: 11SULTON
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 11.58nm/min (adjust if needed)
Time: 03:00:00 (adjust if needed)
Goal: 2µm
Process Note: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.
Cross Section:



7. Annealing: Thin and isolation oxide densification (P1-P2, O1-O4, TO1-TO4)

Nanolab Tool: tystar2
Options: tystar3, tystar4
Recipe: 2HIN2ANA
Temperature: 1000°C
Time: 01:00:00
Process Note: Unannealed low temperature oxide (LTO) sometimes bubbles at high temperatures. So, annealing immediately after the deposition prevents this from happening at later stages in the process.

8. Metrology: Thin oxide thickness measurement (O1-O4, TO1-TO4)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 100nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

9. Metrology: Isolation oxide thickness measurement (P1-P2)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Expected: 2µm
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

10. Test Deposition: Isolation nitride (TS1)

Nanolab Tool: tystar9
Options: tystar17, cambridge Al_2O_3
Recipe: 9LSNVARA
Gas Flows: DCS = 100sccm, NH_3 = 18sccm
Pressure: 375mTorr
Temperature: 835°C
Time: 01:00:00

11. Test Metrology: Isolation nitride thickness measurement (TS1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

12. Deposition: Isolation nitride (P1-P2, S1)

Nanolab Tool: tystar9
Options: tystar17, cambridge Al_2O_3
Recipe: 9LSNVARA
Gas Flows: DCS = 100sccm, NH_3 = 18sccm
Pressure: 375mTorr
Temperature: 835°C
Dep. Rate: 2.78nm/min (adjust if needed)
Time: 03:00:00 (adjust if needed)
Goal: 500nm
Process Note-1: Include a bare silicon wafer ('S1') as a test wafer for the thickness measurement. 'nanospec' can measure nitride layer thickness correctly only when the underlying layer is silicon.
Process Note-2: Note that the deposition rate variation in tystar9 low stress nitride deposition is significant, i.e., ~25% from the center of the rear 6" boat to that of

the front 6" boat. So, use at most six wafers and an additional bare Si test wafer in each deposition to obtain an acceptable thickness uniformity between the process wafers.

Cross Section:

13. Post-Deposition Cleaning: Nitride surface cleaning (P1-P2, S1)

Nanolab Tool: msink6
Options: msink8, msink16, msink18

1st Chemical:	Piranha	*2nd Chemical:*	25:1 HF (or 10:1 HF)
Temperature:	120°C	*Temperature:*	Room temperature
Time:	00:10:00	*Time:*	00:05:00

Process Note: Nitride furnaces are notoriously known to deposit particles on wafer surface. Such particles, if not removed properly, may cause adhesion issues for the subsequent layer in the process, i.e., polysilicon. Cleaning with piranha and HF helps remove these particles and provides with better surface condition for the subsequent layer.

14. Metrology: Isolation nitride initial thickness measurement (S1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Expected: 500nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Use the test wafer ('S1') obtained in the previous step. Do not use the actual process wafers for this measurement as 'nanospec' can measure nitride layer thickness correctly only when the underlying layer is silicon.

15. Etch: Isolation nitride 49% HF etch rate test (S1)

Nanolab Tool: msink7
Options: msink16, msink18
Chemical: 49% HF
Temperature: Room temperature
Time: 00:10:00
Process Note: We have recently realized an enhanced 49% HF etch rate for nitride coming out of 'tystar17' and 'tystar9'. 'tystar9' low stress nitride (LSN) seems to be more resistant to 49% HF. Due to very long 49% HF release times, i.e., longer than 30min, it is important that the nitride etch rate stays below 1-2nm/min to prevent excessive polysilicon interconnect undercut. This test is necessary to make sure the isolation nitride will be resistant enough to 49% HF during device release at the end of the process.

16. Metrology: Isolation nitride 49% HF etch rate measurement (S1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Target: < 2nm/min
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Etch Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: If the target is not met, recipe changes might be needed. Note that, though, even an enhanced nitride etch rate in 49% HF might be acceptable depending on the release time. For example, 5nm/min might be excessive for a 120min-release but acceptable for a 30min-release.

17. Test Deposition: Polysilicon interconnect layer (TO1)

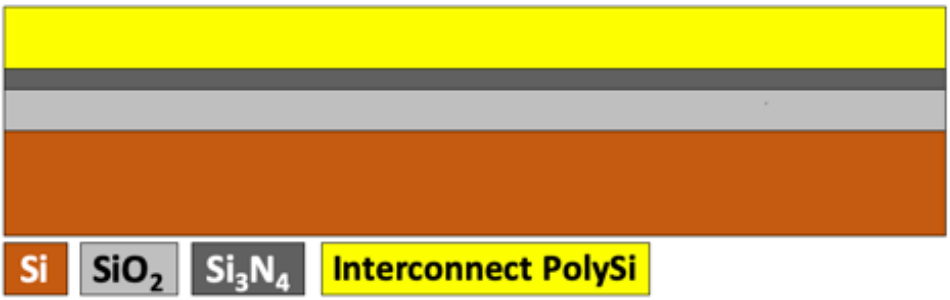
Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Time: 01:00:00
Process Note: Use a thin oxide dummy ('TO1') as a test wafer for the following polysilicon thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

18. Test Metrology: Polysilicon interconnect layer thickness measurement (TO1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

19. Deposition: Polysilicon interconnect layer (P1-P2, O1)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Dep. Rate: 6.25nm/min (adjust if needed)
Time: 08:00:00 (adjust if needed)
Goal: 3µm
Process Note: Use a thin oxide dummy ('O1') as a control wafer for the following polysilicon thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.
Cross Section:



20. $POCl_3$ Doping: Polysilicon interconnect layer (P1-P2, O1)

Nanolab Tool: tystar6
Options: tystar13, tystar11/tystar12 (dope) + tystar2/tystar3/tystar4 (drive-in)
Recipe: PCLO2.006
Gas Flows: N_2 = 200sccm, O_2 = 300sccm
Doping Temperature: 1050°C
Doping Time: 01:00:00
Drive-in Temperature: 1050°C
Drive-in Time: 02:00:00
Process Note: Place the wafers in every other slot to make sure the heat distribution stays uniform during doping and drive-in.

21. $POCl_3$ Doping: PSG removal and cleaning (P1-P2, O1)

Nanolab Tool: msink8

1st Chemical:	10:1 HF	*2nd Chemical:*	Piranha
Temperature:	Room temperature	*Temperature:*	120°C
Time:	00:10:00	*Time:*	00:10:00

Process Note: This phospho-silicate glass (PSG) layer forms during $POCL_3$ doping and must be removed afterwards. Its thickness is usually around 100-200nm. Note that after $POCL_3$ doping and PSG removal, polysilicon surface becomes extremely rough.

22. Metrology: Polysilicon interconnect layer thickness measurement (O1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 3µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note-1: Use the thin oxide dummy ('O1') obtained in the previous step for polysilicon thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

Process Note-2: Since the polysilicon surface becomes extremely rough after $POCL_3$ doping and PSG removal, optical thin film measurement might fail. In this case, a very short chemical mechanical polishing (CMP) might be necessary to polish the surface.

23. (Optional) Chemical Mechanical Polishing: Polysilicon interconnect layer (P1-P2, O1, CS1)

Nanolab Tool: cmp
Options: None
Recipe: Poly.polish
Down Force: 8psi
Back Pres.: 6psi
Table RPM: 24
Chuck RPM: 6
Slurry Name: Cabot iDiel D3543
Slurry Flow: 100ml/min
Etch Rate: 140nm/min
Time: Front Side → 1min
Process Note: Make sure to run a bare Si dummy wafer ('CS1') to check for scratches before polishing the process wafers. Major scratches are usually visible on a bare Si wafer. However, a patterned wafer is necessary to see minor scratches under a microscope.

24. (Optional) Post-CMP cleaning: Polysilicon interconnect layer (P1-P2, O1, CS1)

Nanolab Tool: sinkcmp
Options: None
Chemical: Water
Process Note: Clean the wafer front and back side with PVD sponge four times for 15sec with 90° wafer rotation each time, then follow with four full QDR cycles at sinkcmp.

Nanolab Tool: msink8
Options: msink16, msink18
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
Process Note: Transfer wafers from Cory 190 to the Nanolab immediately in a box filled with water and start piranha cleaning. It is extremely important that the wafers never dry out with cmp silica particles on them.

25. Metrology: Polysilicon interconnect layer sheet resistance measurement (P1-P2, O1)

Nanolab Tool: cde-resmap
Options: None
Program: 5 point
Expected: 4-5Ω/□

Result (P1):	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Result (P2):	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Result (O1):	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____

26. PR Coating: Polysilicon interconnect layer photoresist [P1CF] (P1-P2, O1)

Nanolab Tool: picotrack1

Options: svgcoat6
Resist Type: UV210
Thickness: 900nm
Recipe: T1_UV210-0.6_0.87um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

27. PR Exposure: PM alignment marks (P1-P2, O1)

Nanolab Tool: asml300
Options: None
ASML Job: DISKRUN_R1
Reticle: COMBI Reticle
Field: PM layer
Exposure: 20mJ
Focus: 0nm

28. PR Development: PM alignment marks (P1-P2, O1)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Twice
Process Note-1: Always run at least one dummy wafer first and visually check the developer uniformity.
Process Note-2: Develop twice for dark field masks to make sure all residual photoresist in the patterned area gets removed.

29. PR Exposure: Polysilicon interconnect layer photoresist [P1CF] (P1-P2, O1)

Nanolab Tool: asml300
Options: None
ASML Job: HOLLOWDISK_R1
Reticle: HOLLOWDISK _R1
Field: P1CF - TOPLEFT
Exposure: 20mJ
Focus: 0nm

30. PR Development: Polysilicon interconnect layer photoresist [P1CF] (P1-P2, O1)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Once

Process Note: Always run at least one dummy wafer first and visually check the developer uniformity.

31. PR Descum: Polysilicon interconnect layer photoresist [P1CF] (P1-P2, O1)

Nanolab Tool: technics-c
Options: None
Gas Flows: O_2 = 180sccm
Power: 30W
Time: 00:00:15
Process Note: 'technics-c' etch rates wildly changes from time to time. Take the numbers in the manual as a reference and make sure to test the current etch rate especially if there are designs with feature size less than 500nm where precise width control is critical.

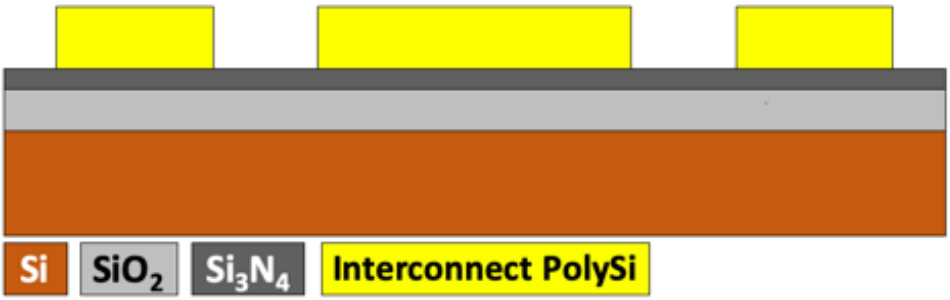
32. PR UV-bake: Polysilicon interconnect layer photoresist [P1CF] (P1-P2, O1)

Nanolab Tool: axcelis
Options: None
Program: U

33. Etch: Polysilicon interconnect layer [P1CF] (P1-P2, O1)

Nanolab Tool: sts2
Options: lam8
Recipe Name: SMOOTH SIDEWALL 1
Passivation
Cycle Time: 5sec
Gas Flows: C_4F_8 = 100sccm, SF_6 = 0sccm, O_2 = 0sccm
Pressure: 18mTorr
Power: Coil = 600W, Bias = 0W
Etch
Cycle Time: 7sec
Gas Flows: C_4F_8 = 0sccm, SF_6 = 130sccm, O_2 = 13sccm
Pressure: 35mTorr
Power: Coil = 600W, Bias = 20W @ 13.56MHz

Etch Rate: 350nm/cycle
Selectivity: 50:1
Etch Time: 14 cycles
Process Note-1: Use the test wafer 'O1' to test the current etch rate and also to condition the chamber before etching the process wafers.
Process Note-2: Note that deep reactive ion etching (DRIE) etch rate heavily depends on the amount of polysilicon to be etched as well as the location on a wafer, i.e., edge region etches faster than the center. So, it is important to visually and electrically check the wafer at the end to make sure the etch is complete.
Cross Section:



34. Metrology: Polysilicon interconnect layer conductivity check after etching (P1-P2, O1)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance between pads that are not connected on the layout. If the etch is complete, this measurement should indicate infinite resistance ('open').

35. PR Strip: Polysilicon interconnect layer photoresist [P1CF] (P1-P2, O1)

Nanolab Tool: matrix
Options: technics-c, msink1-1165, msink16 & msink18-PRS3000
Pressure: 3.75Torr
Temperature: 250°C
Power: 400W
Time: 00:02:30
Process Note: Run the recipe twice.

36. Metrology: Polysilicon interconnect layer step height measurement (P1-P2, O1)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 10µm
Expected: 3µm
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (O1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

37. Metrology: Wafer bow measurement (P1-P2, O1)

Nanolab Tool: flexus
Options: None
Program: Ozgurluk/BaseSi.dat
Target: < 20µm
Result (P1): ____
Result (P2): ____
Result (O1): ____

Process Note: If not, etch the back side using the same tool as the front side has been etched until the target is met. Note that the maximum allowable wafer bow for asml300 is 50µm.

38. Pre-Deposition Cleaning: Planarization oxide (P1-P2, O1, S2, TS2)

Nanolab Tool: msink8
Options: msink7

1st Chemical:	Piranha	*2nd Chemical:*	10:1 HF
Temperature:	120°C	*Temperature:*	Room temperature
Time:	00:10:00	*Time:*	00:02:00

Nanolab Tool: msink6
Options: None

1st Chemical:	Piranha at 120°C	*2nd Chemical:*	25:1 HF
Temperature:	120°C	*Temperature:*	Room temperature
Time:	00:10:00	*Time:*	00:02:00

Process Note: Include bare Si test ('TS2') and control ('S2') wafers for the subsequent oxide deposition step.

39. Test Deposition: Planarization oxide (TS2)

Nanolab Tool: tystar12
Options: tystar11, tystar9-HTO, tystar17-HTO
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C
Time: 01:00:00
Process Note: Use a bare silicon wafer ('TS2') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

40. Test Metrology: Planarization oxide thickness measurement (TS2)

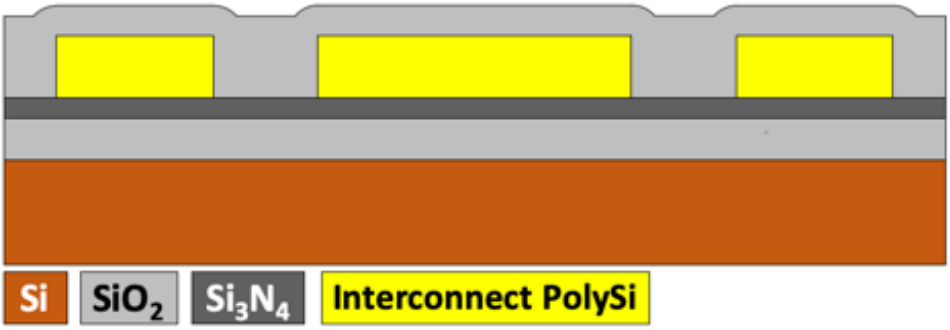
Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)

Thickness:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Dep. Rate:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____

41. Deposition: Planarization oxide (P1-P2, O1, S2)

Nanolab Tool: tystar12
Options: tystar11, tystar9-HTO, tystar17-HTO
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 14.7nm/min (adjust if needed)

Time: 04:32:00 (adjust if needed)
Goal: 4µm
Process Note: Use a bare silicon wafer ('S2') as a control wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



42. PSG Reflow: Planarization oxide (P1-P2, O1, S2)

Nanolab Tool: tystar3
Options: tystar2, tystar4
Recipe: 3HIN2ANA
Temperature: 950°C
Time: 00:30:00

43. Metrology: Planarization oxide thickness measurement (S2)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Expected: 4µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

44. Chemical Mechanical Polishing: Planarization oxide layer (P1-P2, O1, S2, CS2)

Nanolab Tool: cmp
Options: None
Recipe: 6ox6.00
Down Force: 6psi
Back Pres.: 2psi
Table RPM: 33
Chuck RPM: 15
Slurry Name: Cabot iDiel D3543
Slurry Flow: 125ml/min
Removal Rate: 234.3nm/min
Time: Front Side → 1min x 4 with 90° wafer rotation, pad conditioning
Back Side → 1min x 4 with 90° wafer rotation, pad conditioning
Front Side → 1min x 4 with 90° wafer rotation, pad conditioning

Process Note-1: Note that the provided removal rate is for a flat annealed PSG layer. Make sure to check the current removal rate using the test wafer ('S2'). The removal rate considerably enhances in the presence of topography as the effective pressure increases.

Process Note-2: As the removal rate is topography dependent, it is important to visually check the wafer both with naked eye and under a microscope after each CMP cycle to make sure 'cmp' does not start removing the underlying doped polysilicon layer excessively.

Process Note-3: 'cmp' tool is uniform when removing thin layers but it is not uniform for removing layers thicker than 1µm. The purpose of rotating wafer by 90° every minute is to enhance the uniformity over the wafer surface.

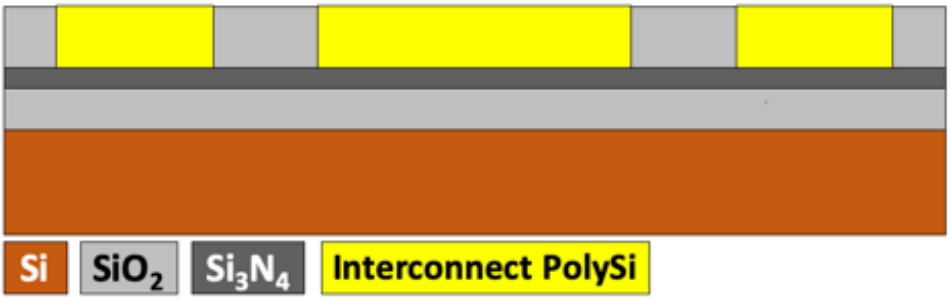
Process Note-4: The purpose of back side cmp is to correct the wafer bow so that edge-to-center CMP uniformity does not degrade during polishing.

Process Note-5: Make sure to run a bare Si dummy wafer ('CS2') and a patterned test wafer ('O1') to check for scratches before polishing the process wafers. Major scratches are usually visible on a bare Si wafer ('CS2'). However, a patterned wafer ('O1') is necessary to see minor scratches under a microscope.

Process Note-6: Note that the front side CMP should continue until all the polysilicon interconnect traces are exposed.

Process Note-7: Depending on the feature size and refill aspect ratio, there might be a need for several oxide refill and CMP cycles if there is any keyhole formation is present on the wafer. If there is a keyhole issue, then refilling with high temperature oxide (HTO) might provide with better conformality than PSG or LTO at the expense of longer deposition times.

Cross Section:



45. Post-CMP cleaning: Planarization oxide layer (P1-P2, O1, S2, CS2)

Nanolab Tool: sinkcmp
Options: None
Chemical: Water
Process Note: Clean the wafer front and back side with PVD sponge four times for 15sec with 90° wafer rotation each time, then follow with four full QDR cycles at sinkcmp.

Nanolab Tool: msink8
Options: msink16, msink18
Chemical: Piranha

Temperature: 120°C
Time: 00:10:00
Process Note: Transfer wafers from Cory 190 to the Nanolab immediately in a box filled with water and start piranha cleaning. It is extremely important that the wafers never dry out with cmp silica particles on them.

46. Metrology: Wafer bow measurement (P1-P2)

Nanolab Tool: flexus
Options: None
Program: Ozgurluk/BaseSi.dat
Target: < 50μm
Result: ____
Process Note: If not, etch the backside using 'sts-oxide' or 'lam6' until the target is met.

47. Metrology: Polysilicon interconnect layer sheet resistance measurement (P1-P2)

Nanolab Tool: probe8
Options: Wentworth
Diagnostic: 4-point probe test structures on the die layout
Expected: 5-10Ω/□
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

48. Pre-Deposition Cleaning: Oxide spacer (P1-P2, S3, TS3)

Nanolab Tool: msink8
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
2nd Chemical: 25:1 HF
Temperature: Room temperature
Time: 00:00:03
Process Note: Make sure to test the 25:1 HF etch rate first with a dummy wafer. It is always better to take the posted etch rates and chemical ratios as a reference but not to fully trust them in a university lab.

49. Test Deposition: Oxide spacer (TS3)

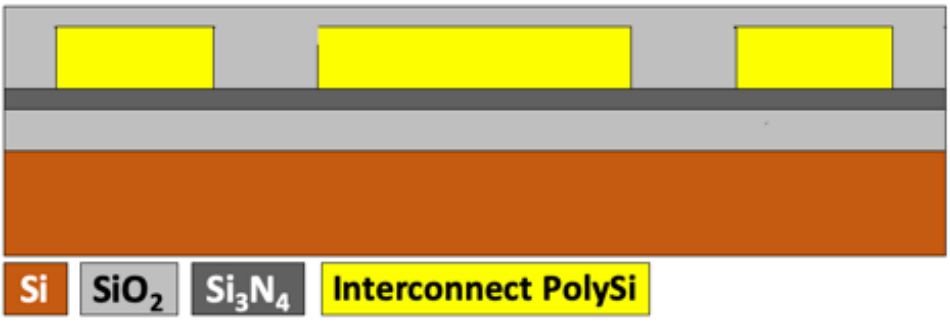
Nanolab Tool: tystar12
Options: tystar11, tystar9, tystar17
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C
Time: 01:00:00
Process Note: Use a bare silicon wafer ('TS3') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

50. Test Metrology: Oxide spacer thickness measurement (TS3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

51. Deposition: Oxide spacer (P1-P2, S3)

Nanolab Tool: tystar12
Options: tystar11, tystar9, tystar17
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 14.7nm/min (adjust if needed)
Time: 00:34:00 (adjust if needed)
Goal: 500nm
Process Note: Use a bare silicon wafer ('S3') as a control wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



52. Annealing: Oxide spacer densification (P1-P2, S3)

Nanolab Tool: tystar3
Options: tystar2, tystar4
Recipe: 3HIN2ANA
Temperature: 950°C
Time: 01:00:00
Process Note: Unannealed phospho-silicate glass (PSG) sometimes bubbles at high temperatures. So, annealing immediately after the deposition prevents this from happening at later stages in the process.

53. Metrology: Oxide spacer thickness measurement (S3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)

Expected: 500nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

54. PR Coating: Stem layer photoresist [P2DF] (P1-P2, S3)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 900nm
Recipe: T1_UV210-0.6_0.87um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

55. PR Exposure: Stem layer photoresist [P2DF] (P1-P2, S3)

Nanolab Tool: asml300
Options: None
ASML Job: HOLLOWDISK_R1
Reticle: HOLLOWDISK_R1
Field: P2DF - TOPRIGHT
Exposure: 26mJ
Focus: 0nm
Process Note: It is important to use a high enough exposure rate for this mask to make sure the stem holes are fully exposed as they are really tiny. Run a focus-exposure matrix (FEM) first if needed.

56. PR Development: Stem layer photoresist [P2DF] (P1-P2, S3)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Twice
Process Note-1: Always run at least one dummy wafer first and visually check the developer uniformity.
Process Note-2: Develop twice for dark field masks to make sure all residual photoresist in the patterned area gets removed.

57. PR Descum: Stem layer photoresist [P2DF] (P1-P2, S3)

Nanolab Tool: technics-c
Options: None
Gas Flows: O_2 = 180sccm
Power: 30W
Time: 00:00:30

Process Note-1: 'technics-c' etch rates wildly changes from time to time. Take the numbers in the manual as a reference and make sure to test the current etch rate especially if there are designs with feature size less than 500nm where precise width control is critical.

Process Note-2: It is important to do a bit longer descum for this mask to make sure any residual PR gets removed as the stem holes are really tiny.

58. PR UV-bake: Stem layer photoresist [P2DF] (P1-P2, S3)

Nanolab Tool: axcelis
Options: None
Program: U

59. Etch: Oxide spacer [P2DF] (P1-P2, S3)

Nanolab Tool: lam6
Options: sts-oxide
Recipe Name: 6001_OXIDE_ME
Gas Flows: Ar = 150sccm, CHF_3 = 25sccm, CF_4 = 25sccm
Pressure: 70mTorr
Power: 350W
Etch Rate: 540nm/min (for P2DF mask)
Selectivity: UV210 Photoresist (UV-baked) : Annealed PSG = 1:7.7
Etch Time: 3min (3 cycles of [1min SiO_2 etch + 1min rest] to prevent PR from burning)

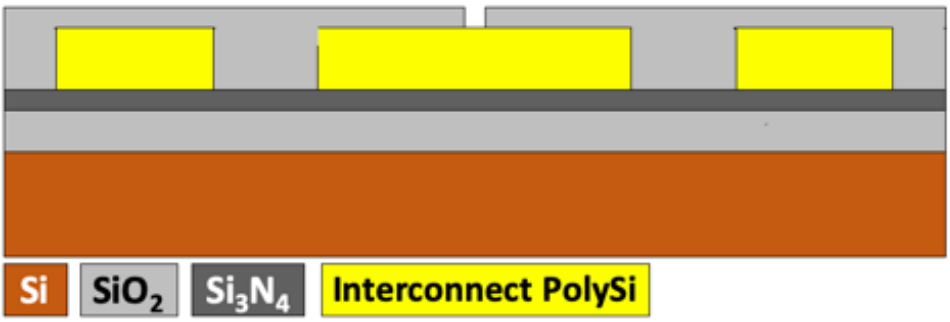
Process Note-1: With default recipe power of 500W, the SiO_2 etch rate is too fast, i.e., 740nm/min, and PR:SiO_2 selectivity is low, i.e., 1:4.25. Lowering the power substantially helps with the etch selectivity.

Process Note-2: Note that 'lam6' burns UV210 resist if the etch time is longer than 1min. To prevent this from happening, the process wafer should rest for 1min in the etch chamber with the RF power turned off after 1min etch.

Process Note-3: Make sure to run 3 dummies with the oxygen clean recipe and also check the current etch rate and selectivity using the control wafer 'S4' by doing a 1min etch beforehand. This will also condition the chamber.

Process Note-4: A 200% over-etch is performed to make sure the stem holes are fully open.

Cross Section:



60. PR Strip: Stem layer photoresist [P2DF] (P1-P2, S3)

Nanolab Tool: matrix
Options: technics-c, msink1-1165, msink16 & msink18-PRS3000

Pressure: 3.75Torr
Temperature: 250°C
Power: 400W
Time: 00:02:30
Process Note: Run the recipe twice.

61. Metrology: Stem layer step height measurement (P1-P2)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 5µm
Expected: 500nm
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Use the patterns in the diagnostics layout to make this measurement.

62. Metrology: Wafer bow measurement (P1-P2)

Nanolab Tool: flexus
Options: None
Program: Ozgurluk/BaseSi.dat
Target: < 20µm
Result (P1): ____
Result (P2): ____
Process Note: If not, etch the back side using the same tool as the front side has been etched until the target is met. Note that the maximum allowable wafer bow for asml300 is 50µm.

63. Pre-Deposition Cleaning: Polysilicon base structural layer (P1-P2, S3, O2, TO2, S4, TS4)

Nanolab Tool: msink8
Options: msink7
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink8
Options: msink7
Chemical: 50:1 HF
Temperature: Room temperature
Time: 00:00:10
Process Note-1: Include thin oxide dummy test (‘TO2’) and control (‘O2’) wafers for the subsequent polysilicon deposition step.

Process Note-2: Make your own 50:1 HF in msink8 ambient bath mixing 16L water and 320mL 49% HF. Use this bath to do native oxide removal right before the following deposition.

Process Note-3: It is important to quickly transfer wafers to the furnace after this step to prevent any native oxide formation in the stem opening.

64. Test Deposition: Polysilicon base structural layer (TO2)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Time: 01:00:00
Process Note: Use a thin oxide dummy wafer ('TO2') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

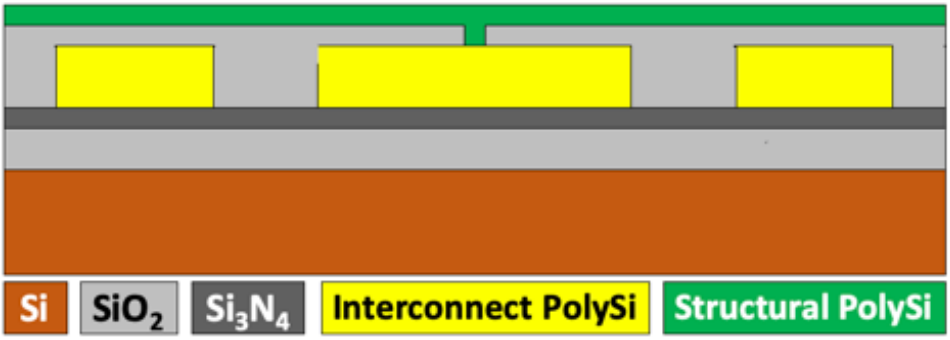
65. Test Metrology: Polysilicon base structural layer thickness measurement (TO2)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)

Thickness:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Dep. Rate:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____

66. Deposition: Polysilicon base structural layer (P1-P2, S3, O2)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Dep. Rate: 6.25nm/min
Time: 01:20:00
Goal: 500nm
Process Note: Use a thin oxide dummy wafer ('O2') as a control wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.
Cross Section:



67. Metrology: Polysilicon base structural layer thickness measurement (O2)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 500nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

68. Test Deposition: Oxide hard mask (TS4)

Nanolab Tool: tystar12
Options: tystar11, tystar9, tystar17
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C
Time: 01:00:00
Process Note: Use a bare silicon wafer ('TS4') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

69. Test Metrology: Oxide hard mask thickness measurement (TS4)

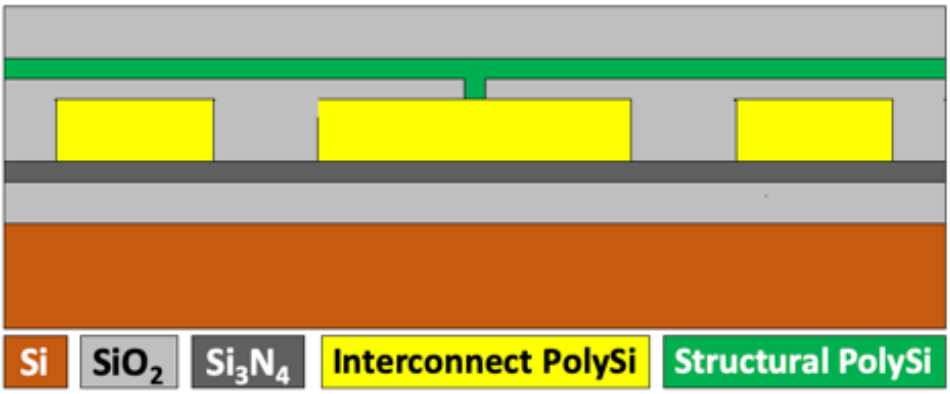
Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

70. Deposition: Oxide hard mask (P1-P2, S3, O2, S4)

Nanolab Tool: tystar12
Options: tystar11, tystar9, tystar17
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 14.7nm/min
Time: 02:50:00
Goal: 2.5µm

Process Note: Use a bare silicon wafer ('S4') as a control wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

Cross Section:



71. Annealing: Drive-in & oxide hard mask densification (P1-P2, S3, O2, S4)

Nanolab Tool: tystar3
Options: tystar2, tystar4
Recipe: 3HIN2ANA
Temperature: 950°C
Time: 01:00:00
Process Note: Unannealed phospho-silicate glass (PSG) sometimes bubbles at high temperatures. So, annealing immediately after the deposition prevents this from happening at later stages in the process.

72. Metrology: Oxide hard mask thickness measurement (S4)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Expected: 2.5µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

73. Cleaning: Oxide hard mask removal (S3)

Nanolab Tool: msink8
Options: msink7
Chemical: 10:1 HF
Temperature: Room temperature
Time: 00:05:00

74. Metrology: Polysilicon base structural layer sheet resistance measurement (S3)

Nanolab Tool: cde-resmap
Options: None
Program: 5 point
Expected: 4-5Ω/□
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

75. PR Coating: Polysilicon base structural layer photoresist [P3CF] (P1-P2, O2, S4)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 900nm
Recipe: T1_UV210-0.6_0.87um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

76. PR Exposure: Polysilicon base structural layer photoresist [P3CF] (P1-P2, O2, S4)

Nanolab Tool: asml300
Options: None
ASML Job: HOLLOWDISK_R1
Reticle: HOLLOWDISK_R1
Field: P3CF - BOTTOMRIGHT
Exposure: 16mJ
Focus: 0nm

77. PR Development: Polysilicon base structural layer photoresist [P3CF] (P1-P2, O2, S4)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Twice
Process Note: Always run at least one dummy wafer first and visually check the developer uniformity.

78. PR Descum: Polysilicon base structural layer photoresist [P3CF] (P1-P2, O2, S4)

Nanolab Tool: technics-c
Options: None
Gas Flows: O_2 = 180sccm
Power: 30W
Time: 00:00:15
Process Note: 'technics-c' etch rates wildly changes from time to time. Take the numbers in the manual as a reference and make sure to test the current etch rate especially if there are designs with feature size less than 500nm where precise width control is critical.

79. PR UV-bake: Polysilicon base structural layer photoresist [P3CF] (P1-P2, O2, S4)

Nanolab Tool: axcelis
Options: None
Program: U

80. Etch: Polysilicon base structural layer hard mask [P3CF] (P1-P2, O2, S4)

Nanolab Tool: lam6
Options: sts-oxide
Recipe Name: 6001_OXIDE_ME
Gas Flows: Ar = 150sccm, CHF_3 = 25sccm, CF_4 = 25sccm
Pressure: 70mTorr
Gap: 1.3cm
Power: 500W
Etch Rate: 717nm/min (for P3CF mask)
Selectivity: UV210 Photoresist (UV-baked) : Annealed PSG = 1 : 4.10
Etch Time: 5min (5 cycles of [1min SiO_2 etch + 1min rest] to prevent PR from burning)
Process Note-1: Note that 'lam6' burns UV210 resist if the etch time is longer than 1min. To prevent this from happening, the process wafer should rest for 1min in the etch chamber with the RF power turned off after 1min etch.
Process Note-2: Make sure to run 3 dummies with the oxygen clean recipe and also check the current etch rate and selectivity using the control wafer 'S4' by doing a 1min etch beforehand. This will also condition the chamber.
Process Note-3: 40% over-etch is included. Note that any etch longer than 5min necessitates a thicker resist or better PR-to-SiO_2 selectivity with lower power.

81. PR Strip: Polysilicon base structural layer photoresist [P3CF] (P1-P2, O2, S4)

Nanolab Tool: matrix
Options: technics-c, msink1-1165, msink16 & msink18-PRS3000
Pressure: 3.75Torr
Temperature: 250°C
Power: 400W
Time: 00:02:30
Process Note: Run the recipe twice.

82. Metrology: Oxide hard mask step height measurement (P1-P2, O2)

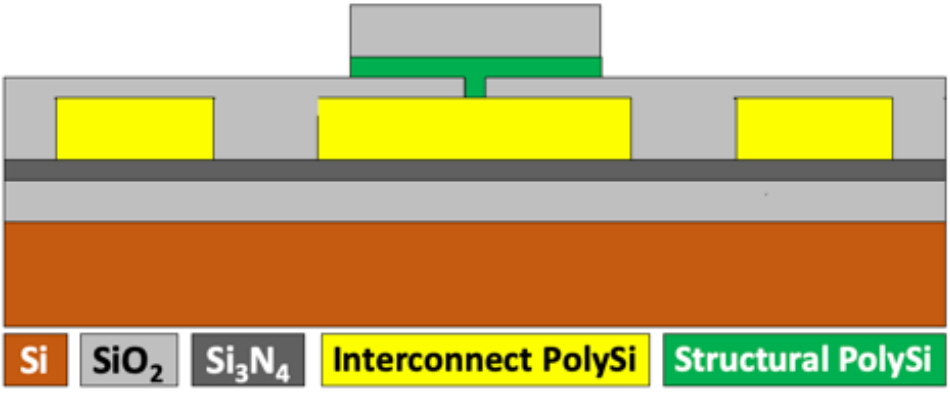
Nanolab Tool: alphastep
Options: nanoduv, ellips1, ellips2
Meas. Range: 10µm
Expected: 2.5µm
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (O2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

83. Post-Etch Cleaning: Oxide hard mask (P1-P2, O2)

Nanolab Tool: msink8
Options: msink7
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
Process Note: Note that PR must be completely removed and cleaned before the following HBr-based polysilicon etch. Otherwise, any PR present on the wafer leaves some organic residue during the HBr-based polysilicon etch.

84. Etch: Polysilicon base structural layer [P3CF] (P1-P2, O2)

Nanolab Tool: lam8
Options: None
Recipe Name: 8001_POLY_ME
Gas Flows: HBr = 150sccm, Cl_2 = 4sccm, O_2 = 1sccm
Pressure: 12mTorr
Gap: 6.03cm
TCP RF: 250W
Bias RF: 55W
Etch Rate: 172.9nm/min (for P3CF mask)
Selectivity: SiO_2 : Polysilicon = 1 : (>10)
Etch Time: 4min (2 cycles of [2min Polysilicon etch + 1min rest] to prevent wafer from over-heating)
Process Note-1: Note that 'lam8' overheats the wafer if the etch time is longer than 2min. To prevent this from happening, the process wafer should rest for 1min in the etch chamber with the TCP RF and bias RF powers turned off after 2min etch.
Process Note-2: Make sure to check the current etch rate and selectivity using the control wafer 'O2' by doing a 1min etch beforehand. This will also condition the chamber.
Process Note-3: 40% overetch is included.
Cross Section:



85. Metrology: Polysilicon base structural layer conductivity check after etching (P1-P2, O2)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (O2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance on the layout where polysilicon has been removed in the previous etch step. If the etch is complete, this measurement should indicate infinite resistance ('open')

86. Metrology: Polysilicon base structural layer and oxide hard mask step height measurement (P1-P2, O2)

Nanolab Tool: alphastep
Options: nanoduv, ellips1, ellips2
Meas. Range: 10µm
Expected: 3µm

Result (P1):	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Result (P2):	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Result (O2):	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____

87. Metrology: Wafer bow measurement (P1-P2, O2)

Nanolab Tool: flexus
Options: None
Program: Ozgurluk/BaseSi.dat
Target: < 20µm
Result (P1): ____
Result (P2): ____
Result (O2): ____
Process Note: If not, etch the back side using the same tool as the front side has been etched until the target is met. Note that the maximum allowable wafer bow for asml300 is 50µm.

88. Pre-Deposition Cleaning: Polysilicon sidewall ring layer (P1-P2, O2, O3, TO3)

Nanolab Tool: msink8
Options: msink7
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None

1st Chemical:	Piranha	*2nd Chemical:*	25:1 HF
Temperature:	120°C	*Temperature:*	Room temperature
Time:	00:10:00	*Time:*	00:00:03

Process Note-1: Include thin oxide dummy test ('TO3') and control ('O3') wafers for the subsequent polysilicon deposition step.
Process Note-2: Make sure to test the 25:1 HF etch rate first with a dummy wafer. It is always better to take the posted etch rates and chemical ratios as a reference but not to fully trust them in a university lab.

89. Test Deposition: Polysilicon sidewall ring layer (TO3)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr

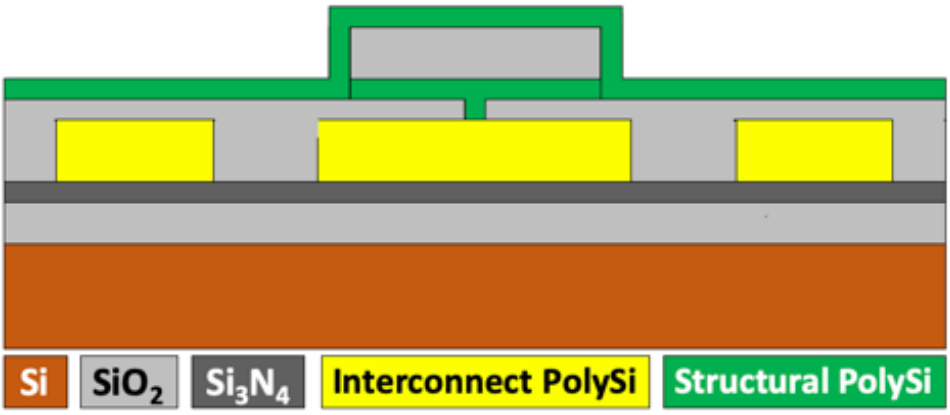
Temperature: 590°C
Time: 01:00:00
Process Note: Use the thin oxide dummy wafer ('TO3') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

90. Test Metrology: Polysilicon sidewall ring layer thickness measurement (TO3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

91. Deposition: Polysilicon sidewall ring layer (P1-P2, O2, O3)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Dep. Rate: 6.25nm/min (adjust if needed)
Time: 01:20:00 (adjust if needed)
Goal: 500nm
Process Note: Use the thin oxide dummy wafer ('O3') as a control wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.
Cross Section:

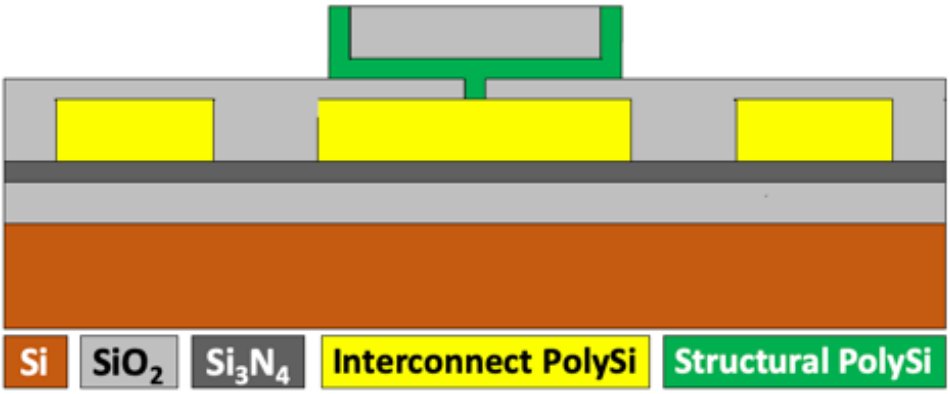


92. Metrology: Polysilicon sidewall ring layer thickness measurement (O3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 500nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

93. Etch: Polysilicon sidewall ring layer (P1-P2, O2, O3)

Nanolab Tool: lam8
Options: None
Recipe Name: 8001_POLY_ME
Gas Flows: HBr = 150sccm, Cl_2 = 4sccm, O_2 = 1sccm
Pressure: 12mTorr
Gap: 6.03cm
TCP RF: 250W
Bias RF: 55W
Etch Rate: 172.9nm/min (for P3CF mask)
Selectivity: SiO_2 : Polysilicon = 1 : (>10)
Etch Time: 4min (2 cycles of [2min Polysilicon etch + 1min rest] to prevent wafer from over-heating)
Process Note-1: Note that 'lam8' overheats the wafer if the etch time is longer than 2min. To prevent this from happening, the process wafer should rest for 1min in the etch chamber with the TCP RF and bias RF powers turned off after 2min etch.
Process Note-2: Make sure to check the current etch rate and selectivity using the control wafer 'O3' by doing a 1min etch beforehand. This will also condition the chamber.
Process Note-3: 40% overetch is included.
Cross Section:



94. Metrology: Polysilicon sidewall ring layer conductivity check after etching (P1-P2, O2)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (O2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance on the layout where polysilicon has been removed in the previous etch step. If the etch is complete, this measurement should indicate infinite resistance ('open')

95. Pre-Deposition Cleaning: Sidewall sacrificial high temperature oxide (HTO) (P1-P2, O2, S5-S6, TS5-TS6)

Nanolab Tool: msink8
Options: msink7
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None
1st Chemical: Piranha *2nd Chemical:* 25:1 HF
Temperature: 120°C *Temperature:* Room temperature
Time: 00:10:00 *Time:* 00:00:03
Process Note-1: Include bare Si test ('TS5', 'TS6') and control ('S5', 'S6') wafers for the subsequent oxide deposition steps.
Process Note-2: Make sure to test the 25:1 HF etch rate first with a dummy wafer. It is always better to take the posted etch rates and chemical ratios as a reference but not to fully trust them in a university lab.
Process Note-3: It is important to quickly transfer wafers to the furnace after this step to prevent any native oxide formation in the sidewall sacrificial gap region.

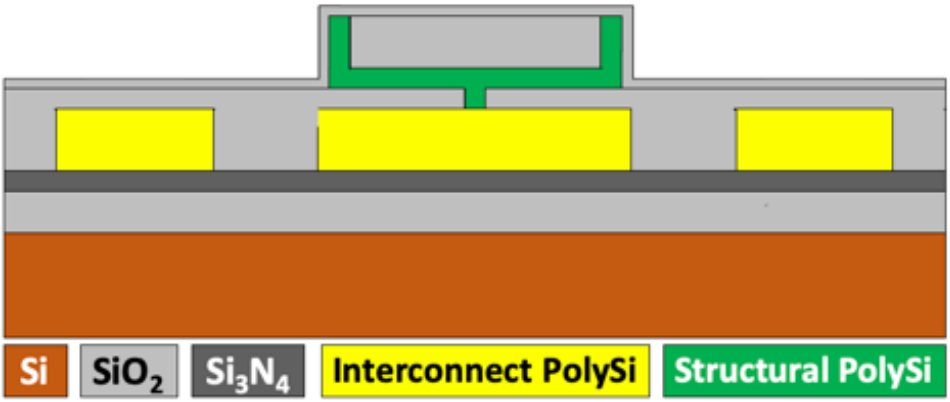
---------- Start: Sidewall Sacrificial Layer: 100nm HTO ----------

96. Test Deposition: Sidewall sacrificial high temperature oxide (HTO) (TS5)
Nanolab Tool: tystar17
Recipe: HTOSTDA.017
Gas Flows: N_2O = 180sccm, DCS = 60sccm
Pressure: 400mTorr
Temperature: 930°C
Time: 00:17:00
Process Note: Use a bare silicon wafer ('TS5') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

97. Test Metrology: Sidewall sacrificial high temperature oxide (HTO) (TS5)
Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

98. Deposition: Sidewall sacrificial high temperature oxide (HTO) (P1, O2, S5)
Nanolab Tool: tystar17
Recipe: HTOSTDA.017
Gas Flows: N_2O = 180sccm, DCS = 60sccm
Pressure: 400mTorr
Temperature: 930°C
Dep. Rate: 5.85nm/min (adjust if needed)

Time: 00:17:00 (adjust if needed)
Goal: 100nm
Process Note: Use a bare silicon wafer ('S5') as a control wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



99. Metrology: Sidewall sacrificial HTO thickness measurement (S5)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Expected: 100nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: Sidewall Sacrificial Layer: 100nm HTO ----------

---------- Start: Sidewall Sacrificial Layer: 40nm HTO ----------

100. Test Deposition: Sidewall sacrificial high temperature oxide (HTO) (TS6)

Nanolab Tool: tystar17
Recipe: HTOSTDA.017
Gas Flows: N_2O = 180sccm, DCS = 60sccm
Pressure: 400mTorr
Temperature: 930°C
Time: 00:07:00
Process Note: Use a bare silicon wafer ('TS6') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

101. Test Metrology: Sidewall sacrificial high temperature oxide (HTO) (TS6)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

102. Deposition: Sidewall sacrificial high temperature oxide (HTO) (P2, S6)

Nanolab Tool: tystar17
Recipe: HTOSTDA.017
Gas Flows: N_2O = 180sccm, DCS = 60sccm
Pressure: 400mTorr
Temperature: 930°C
Dep. Rate: 5.85nm/min (adjust if needed)
Time: 00:07:00 (adjust if needed)
Goal: 40nm
Process Note: Use a bare silicon wafer ('S6') as a control wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

103. Metrology: Sidewall sacrificial HTO thickness measurement (S6)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Expected: 40nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: Sidewall Sacrificial Layer: 40nm HTO ----------

104. PR Coating: Anchor layer photoresist [P4DF] (P1-P2, O2)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV26
Thickness: 2.2µm
Recipe: T1_UV26-3.0_2.2um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 110°C (Post)
Process Note-1: Always run at least one dummy wafer first and visually check the resist uniformity.
Process Note-2: Note that due to the 3-4µm topography present at this step, a thicker PR is needed to completely cover the wafer. After coating, make sure the wafer is fully covered with PR. If not, use even thicker PR.

105. PR Exposure: Anchor layer photoresist [P4DF] (P1-P2, O2)

Nanolab Tool: asml300
Options: None
ASML Job: HOLLOWDISK_R1
Reticle: HOLLOWDISK_R1
Field: P4DF - BOTTOMLEFT
Exposure: 50mJ
Focus: 3.50µm
Process Note: A very high exposure and change in the focus setting is needed due to thicker PR. Do a focus-exposure matrix (FEM) if needed.

106. PR Development: Anchor layer photoresist [P4DF] (P1-P2, O2)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PROX110C60s_MF26A60s
Temperature: Prox. (0.6mm) 60sec @ 110°C
Dev. Count: Twice
Process Note-1: Always run at least one dummy wafer first and visually check the developer uniformity.
Process Note-2: Develop twice for dark field masks to make sure all residual photoresist in the patterned area gets removed.

107. PR Descum: Anchor layer photoresist [P4DF] (P1-P2, O2)

Nanolab Tool: technics-c
Options: None
Gas Flows: O_2 = 180sccm
Power: 30W
Time: 00:00:30
Process Note: 'technics-c' etch rates wildly changes from time to time. Take the numbers in the manual as a reference and make sure to test the current etch rate especially if there are designs with feature size less than 500nm where precise width control is critical.

108. Metrology: Anchor layer photoresist thickness measurement before hard bake [P4DF] (P1-P2, O2)

Nanolab Tool: alphastep
Options: nanoduv, ellips1, ellips2
Meas. Range: 10µm
Expected: 2-3µm
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (O2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

109. PR Hard-bake: Anchor layer photoresist [P4DF] (P1-P2, O2)

Nanolab Tool: oven
Options: None
Temperature: 120°C
Time: 12:00:00
Process Note: UV-bake or hot plate-based hard bake destroys thick UV26 photoresist. So, the only option here is to do a long oven bake.

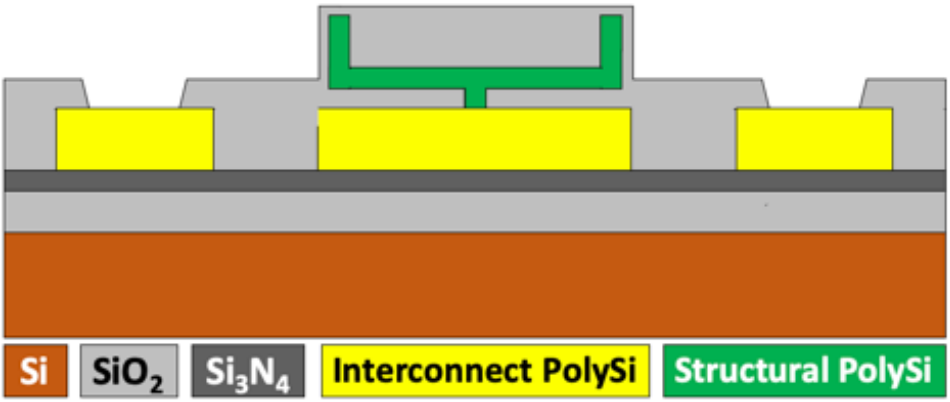
110. Metrology: Anchor layer photoresist thickness measurement after hard bake [P4DF] (P1-P2, O2)

Nanolab Tool: alphastep
Options: nanoduv, ellips1, ellips2
Meas. Range: 10µm

Expected: 2-3µm
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (O2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

111. Etch: Anchor layer [P4DF] (P1-P2, O2)

Nanolab Tool: lam6
Options: sts-oxide
Recipe Name: 6001_OXIDE_ME
Gas Flows: Ar = 150sccm, CHF_3 = 25sccm, CF_4 = 25sccm
Pressure: 70mTorr
Gap: 1.3cm
Power: 500W
Etch Rate: 717nm/min (for P3CF mask)
Selectivity: UV26 Photoresist (oven baked) : Annealed PSG = 1 : 2
Etch Time: 2min (2 cycles of [1min SiO_2 etch + 1min rest] to prevent PR from burning)
Process Note-1: Note that 'lam6' burns UV26 resist if the etch time is longer than 1min. To prevent this from happening, the process wafer should rest for 1min in the etch chamber with the RF power turned off after 1min etch.
Process Note-2: Make sure to run 3 dummies with the oxygen clean recipe and also check the current etch rate and selectivity with the test wafer 'O2' by doing a 30sec etch beforehand. Complete the 'O2' etch by doing another 1min and 30sec additional etch. This will also condition the chamber.
Process Note-3: 200% over etch is included. Be careful with excessive lateral etch.
Cross Section:



112. PR Strip: Anchor layer photoresist [P4DF] (P1-P2, O2)

Nanolab Tool: matrix
Options: technics-c, msink1-1165, msink16 & msink18-PRS3000
Pressure: 3.75Torr
Temperature: 250°C
Power: 400W
Time: 00:02:30
Process Note: Run the recipe twice.

113. Metrology: Anchor layer step height measurement (P1-P2, O2)

Nanolab Tool: alphastep
Options: nanoduv, ellips1, ellips2
Meas. Range: 5µm
Expected: 500nm
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (O2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Use the patterns in the diagnostics layout to make this measurement.

114. Pre-Deposition Cleaning: Polysilicon electrode layer (P1-P2, O2, O4, TO4)

Nanolab Tool: msink8
Options: msink7
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink8
Options: msink7
Chemical: 50:1 HF
Temperature: Room temperature
Time: 00:00:03
Process Note-1: Include thin oxide dummy test ('TO4') and control ('O4') wafers for the subsequent polysilicon deposition step.
Process Note-2: Make your own 50:1 HF in msink8 ambient bath mixing 16L water and 320mL 49% HF. Use this bath to do native oxide removal right before the following deposition.
Process Note-3: It is important to quickly transfer wafers to the furnace after this step to prevent any native oxide formation in the anchor opening.

115. Test Deposition: Polysilicon electrode layer (TO4)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Time: 01:00:00

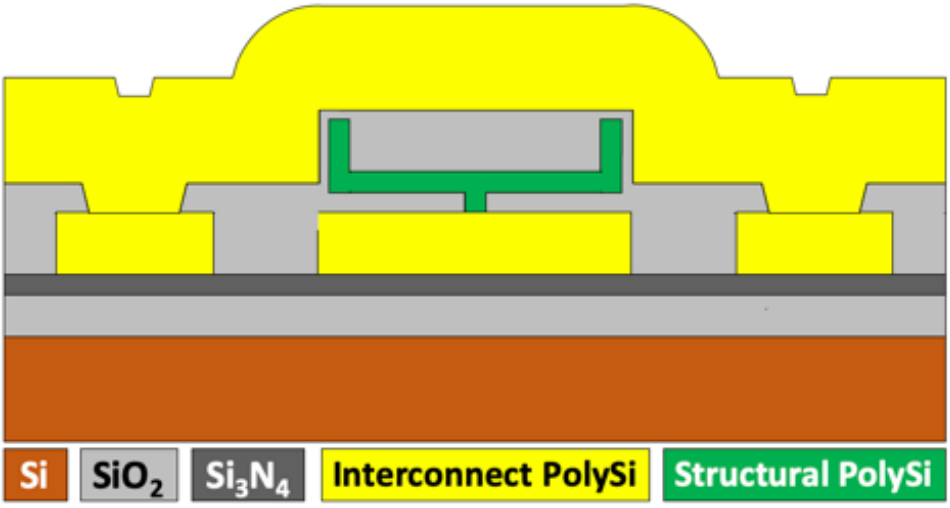
Process Note: Use a thin oxide dummy wafer ('TO4') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

116. Test Metrology: Polysilicon sidewall ring layer thickness measurement (TO4)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

117. Deposition: Polysilicon electrode layer (P1-P2, O2, O4)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Dep. Rate: 6.25nm/min (adjust if needed)
Time: 10:40:00 (adjust if needed)
Goal: 4µm
Process Note: Use a thin oxide dummy wafer ('O4') as a control wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.
Cross Section:



118. Metrology: Polysilicon electrode layer thickness measurement (O4)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 4µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

119. $POCl_3$ Doping: Polysilicon electrode layer (P1-P2, O2, O4)

Nanolab Tool: tystar6
Options: tystar13, tystar11/tystar12 (dope) + tystar2/tystar3/tystar4 (drive-in)
Recipe: PCLO2.006
Gas Flows: N_2 = 200sccm, O_2 = 300sccm
Doping Temperature: 950°C
Doping Time: 01:00:00
Drive-in Temperature: 950°C
Drive-in Time: 02:00:00
Process Note-1: Place the wafers in every other slot to make sure the heat distribution stays uniform during doping and drive-in.
Process Note-2: For temperatures above 950°C, PSG layers underneath might bubble. So, it is necessary to either keep the temperature below 950°C or replace all underlying PSG layers with LTO.

120. $POCl_3$ Doping: PSG removal and cleaning (P1-P2, O2, O4)

Nanolab Tool: msink8

1st Chemical:	10:1 HF	*2nd Chemical:*	Piranha
Temperature:	Room temperature	*Temperature:*	120°C
Time:	00:10:00	*Time:*	00:10:00

Process Note: This phosphor-silicate glass (PSG) layer forms during $POCL_3$ doping and must be removed afterwards. Its thickness is usually around 100-200nm. Note that after $POCL_3$ doping and PSG removal, polysilicon surface becomes extremely rough.

121. Metrology: Polysilicon electrode layer thickness measurement (O4)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 4µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note-1: Use the thin oxide dummy wafer ('O4') obtained in the previous step for this thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

Process Note-2: Since the polysilicon surface becomes extremely rough after $POCL_3$ doping and PSG removal, optical thin film measurement might fail. In this case, a very short chemical mechanical polishing (CMP) might be necessary to polish the surface.

122. (Optional) Chemical Mechanical Polishing: Polysilicon electrode layer (O4, CS3)

Nanolab Tool: cmp
Options: None
Recipe: Poly.polish
Down Force: 8psi
Back Pres.: 6psi
Table RPM: 24

Chuck RPM: 6
Slurry Name: Cabot iDiel D3543
Slurry Flow: 100ml/min
Etch Rate: 140nm/min
Time: Front Side → 1min
Process Note: Make sure to run a bare Si dummy wafer ('CS3') to check for scratches before processing the process wafers. Major scratches are usually visible on a bare Si wafer. However, a patterned wafer is necessary to see minor scratches under a microscope.

123. (Optional) Post-CMP cleaning: Polysilicon interconnect layer (O4, CS3)

Nanolab Tool: sinkcmp
Options: None
Chemical: Water
Process Note: Clean the wafer front and back side with PVD sponge four times for 15sec with 90° wafer rotation each time, then follow with four full QDR cycles at sinkcmp.

Nanolab Tool: msink8
Options: msink16, msink18
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
Process Note: Transfer wafers from Cory 190 to the Nanolab immediately in a box filled with water and start piranha cleaning. It is extremely important that the wafers never dry out with cmp silica particles on them.

124. Metrology: Polysilicon electrode layer thickness measurement (O4)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 4µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

125. Chemical Mechanical Polishing: Polysilicon electrode layer (P1-P2, O2, CS4, O4)

Nanolab Tool: cmp
Options: None
Recipe: Poly.polish
Down Force: 8psi
Back Pres.: 6psi
Table RPM: 24
Chuck RPM: 6
Slurry Name: Cabot iDiel D3543
Slurry Flow: 100ml/min
Etch Rate: 140nm/min
Time: Front Side → 2min x 4 with 90° wafer rotation, pad conditioning

Back Side → 2min x 4 with 90° wafer rotation, pad conditioning
Front Side → 1min x 4 with 90° wafer rotation, pad conditioning

Process Note-1: Note that the provided etch rate is for a flat polysilicon layer. Make sure to check the current removal rate using the test wafer ('O4'). This etch rate considerably enhances in the presence of topography as the effective pressure increases.

Process Note-2: As the etch rate is topography dependent, it is important to visually check the wafer both with naked eye and under a microscope after each CMP cycle to make sure 'cmp' does not start removing the underlying oxide hard mask layer excessively.

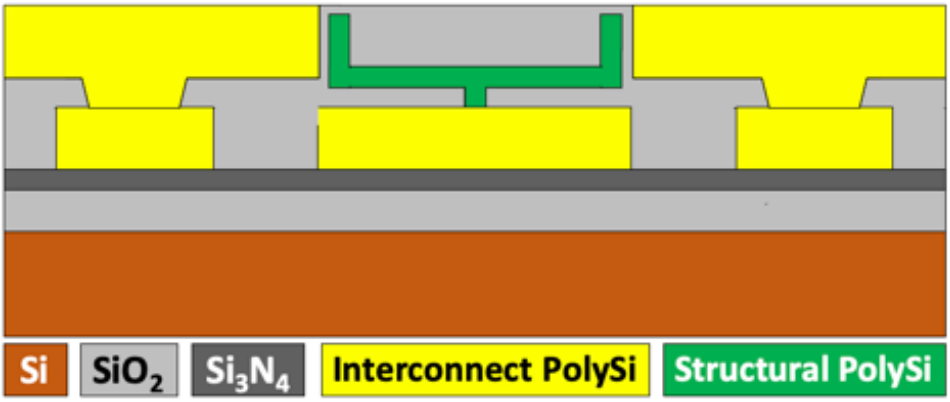
Process Note-3: 'cmp' tool is uniform when removing thin layers but it is not uniform for removing layers thicker than 1µm. The purpose of rotating wafer by 90° every minute is to enhance the uniformity over the wafer surface.

Process Note-4: The purpose of back side cmp is to correct the wafer bow so that edge-to-center CMP uniformity does not degrade during polishing.

Process Note-5: Make sure to run a bare Si dummy wafer ('CS4') and a patterned test wafer ('O2') to check for scratches before processing the process wafers. Major scratches are usually visible on a bare Si wafer ('CS4'). However, a patterned wafer ('O2') is necessary to see minor scratches under a microscope.

Process Note-6: Note that the front side CMP should continue until all SiO_2 hard mask patterns are exposed.

Cross Section:



126. Post-CMP cleaning: Planarization oxide layer (P1-P2, O2, CS4, O4)

Nanolab Tool: sinkcmp
Options: None
Chemical: Water
Process Note: Clean the wafer front and back side with PVD sponge four times for 15sec with 90° wafer rotation each time, then follow with four full QDR cycles at sinkcmp.

Nanolab Tool: msink8
Options: msink16, msink18
Chemical: Piranha
Temperature: 120°C

Time: 00:10:00
Process Note: Transfer wafers from Cory 190 to the Nanolab immediately in a box filled with water and start piranha cleaning. It is extremely important that the wafers never dry out with cmp silica particles on them.

127. Metrology: Wafer bow measurement (P1-P2, O2)
Nanolab Tool: flexus
Options: None
Program: Ozgurluk/BaseSi.dat
Target: < 20µm
Result (P1): ____
Result (P2): ____
Result (O2): ____
Process Note: If not, etch the back side using 'sts2' or 'lam8' until the target is met. Note that the maximum allowable wafer bow for asml300 is 50µm.

128. PR Coating: Polysilicon interconnect layer photoresist [P5CF] (P1-P2, O2)
Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 900nm
Recipe: T1_UV210-0.6_0.87um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

129. PR Exposure: Polysilicon electrode layer photoresist [P5CF] (P1-P2, O2)
Nanolab Tool: asml300
Options: None
ASML Job: HOLLOWDISK_R2
Reticle: HOLLOWDISK_R2
Field: P5CF - TOPLEFT
Exposure: 20mJ
Focus: 0nm

130. PR Development: Polysilicon electrode layer photoresist [P5CF] (P1-P2, O2)
Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Once
Process Note: Always run at least one dummy wafer first and visually check the developer uniformity.

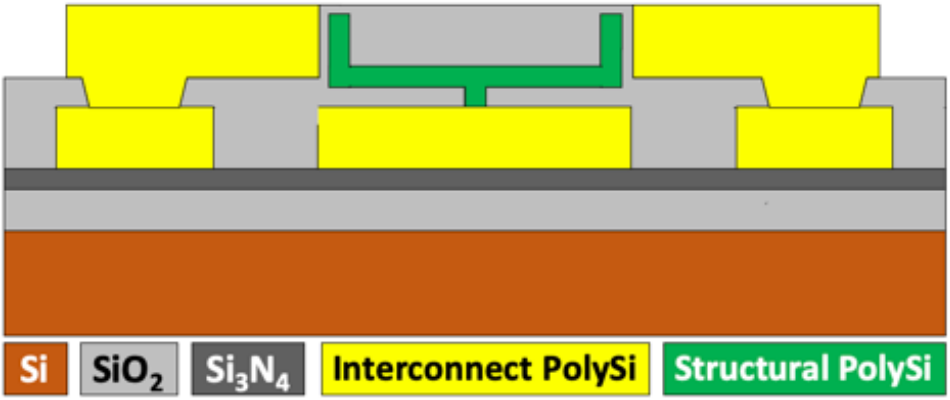
131. PR Descum: Polysilicon electrode layer photoresist [P5CF] (P1-P2, O2)

Nanolab Tool: technics-c
Options: None
Gas Flows: O_2 = 180sccm
Power: 30W
Time: 00:00:15
Process Note: 'technics-c' etch rates wildly changes from time to time. Take the numbers in the manual as a reference and make sure to test the current etch rate especially if there are designs with feature size less than 500nm where precise width control is critical.

132. PR UV-bake: Polysilicon electrode layer photoresist [P5CF] (P1-P2, O2)
Nanolab Tool: axcelis
Options: None
Program: U

133. Etch: Polysilicon electrode layer [P5CF] (P1-P2, O2)
Nanolab Tool: sts2
Options: None
Recipe Name: SMOOTH SIDEWALL 1
Passivation
Cycle Time: 5sec
Gas Flows: C_4F_8 = 100sccm, SF_6 = 0sccm, O_2 = 0sccm
Pressure: 18mTorr
Power: Coil = 600W, Bias = 0W
Etch
Cycle Time: 7sec
Gas Flows: C_4F_8 = 0sccm, SF_6 = 130sccm, O_2 = 13sccm
Pressure: 35mTorr
Power: Coil = 600W, Bias = 20W @ 13.56MHz

Etch Rate: 350nm/cycle
Selectivity: 50:1
Etch Time: 17 cycles
Process Note-1: Use the test wafer 'O2' to verify the etch rate and also to condition the chamber before etching the process wafers.
Process Note-2: Note that deep reactive ion etching (DRIE) etch rate heavily depends on the amount of polysilicon to be etched as well as the location on a wafer, i.e., edge region etches faster than the center. So, it is important to visually and electrically check the wafer to make sure the etch is complete.
Cross Section:



134. Metrology: Polysilicon electrode layer conductivity check after etching (P1-P2)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance between pads that are not connected on the layout. If the etch is complete, this measurement should indicate infinite resistance ('open').

135. PR Strip: Polysilicon electrode layer photoresist [P5CF] (P1-P2)

Nanolab Tool: matrix
Options: technics-c, msink1-1165, msink16 & msink18-PRS3000
Pressure: 3.75Torr
Temperature: 250°C
Power: 400W
Time: 00:02:30
Process Note: Run the recipe twice.

136. Metrology: Polysilicon electrode layer step height measurement (P1-P2)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 10µm
Expected: >3µm
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

137. Post-Etch Cleaning: Polysilicon electrode layer (P1-P2)

Nanolab Tool: msink8
Options: msink7, msink16, msink18
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

138. Backside Etch: Polysilicon electrode layer (P1-P2)

Nanolab Tool: sts2
Options: lam8
Recipe Name: SMOOTH SIDEWALL 1
Passivation
Cycle Time: 5sec
Gas Flows: C_4F_8 = 100sccm, SF_6 = 0sccm, O_2 = 0sccm
Pressure: 18mTorr
Power: Coil = 600W, Bias = 0W
Etch
Cycle Time: 7sec
Gas Flows: C_4F_8 = 0sccm, SF_6 = 130sccm, O_2 = 13sccm
Pressure: 35mTorr
Power: Coil = 600W, Bias = 20W @ 13.56MHz

Etch Rate: 350nm/cycle
Etch Time: Etch until shiny polysilicon layer is completely etched away. If visual check is not enough, use a multimeter to verify.

139. Backside Etch: Sidewall sacrificial layer (P1-P2)

Nanolab Tool: sts-oxide
Options: lam6
Recipe Name: Oxide etch (APS) no 2-2
Gas Flows: C_4F_8 = 15sccm , He = 174sccm
Pressure: 4mTorr
Power: Coil = 1500W, Bias = 400W @ 13.56MHz
Etch Rate: 370nm/s
Etch Time: Etch until shiny polysilicon layer is completely exposed. If visual check is not enough, use a multimeter to verify.

140. Backside Etch: Polysilicon sidewall ring layer (P1-P2)

Nanolab Tool: sts2
Options: lam8
Recipe Name: SMOOTH SIDEWALL 1
Passivation
Cycle Time: 5sec
Gas Flows: C_4F_8 = 100sccm, SF_6 = 0sccm, O_2 = 0sccm
Pressure: 18mTorr
Power: Coil = 600W, Bias = 0W
Etch
Cycle Time: 7sec
Gas Flows: C_4F_8 = 0sccm, SF_6 = 130sccm, O_2 = 13sccm
Pressure: 35mTorr
Power: Coil = 600W, Bias = 20W @ 13.56MHz

Etch Rate: 350nm/cycle

Etch Time: Etch until shiny polysilicon layer is completely etched away. If visual check is not enough, use a multimeter to verify.

141. Backside Etch: Oxide hard mask layer (P1-P2)

Nanolab Tool: sts-oxide
Options: lam6
Recipe Name: Oxide etch (APS) no 2-2
Gas Flows: C_4F_8 = 15sccm , He = 174sccm
Pressure: 4mTorr
Power: Coil = 1500W, Bias = 400W @ 13.56MHz
Etch Rate: 370nm/s
Etch Time: Etch until shiny polysilicon layer is completely exposed. If visual check is not enough, use a multimeter to verify.

142. Backside Etch: Polysilicon base structural layer (P1-P2)

Nanolab Tool: sts2
Options: lam8
Recipe Name: SMOOTH SIDEWALL 1
Passivation
Cycle Time: 5sec
Gas Flows: C_4F_8 = 100sccm, SF_6 = 0sccm, O_2 = 0sccm
Pressure: 18mTorr
Power: Coil = 600W, Bias = 0W
Etch
Cycle Time: 7sec
Gas Flows: C_4F_8 = 0sccm, SF_6 = 130sccm, O_2 = 13sccm
Pressure: 35mTorr
Power: Coil = 600W, Bias = 20W @ 13.56MHz

Etch Rate: 350nm/cycle
Etch Time: Etch until shiny polysilicon layer is completely etched away. If visual check is not enough, use a multimeter to verify.

143. Backside Etch: Oxide spacer & refill layer (P1-P2)

Nanolab Tool: sts-oxide
Options: lam6
Recipe Name: Oxide etch (APS) no 2-2
Gas Flows: C_4F_8 = 15sccm , He = 174sccm
Pressure: 4mTorr
Power: Coil = 1500W, Bias = 400W @ 13.56MHz
Etch Rate: 370nm/s
Etch Time: Etch until shiny polysilicon layer is completely exposed. If visual check is not enough, use a multimeter to verify.

144. Backside Etch: Polysilicon interconnect layer (P1-P2)

Nanolab Tool: sts2

Options: lam8
Recipe Name: SMOOTH SIDEWALL 1
Passivation
Cycle Time: 5sec
Gas Flows: C_4F_8 = 100sccm, SF_6 = 0sccm, O_2 = 0sccm
Pressure: 18mTorr
Power: Coil = 600W, Bias = 0W
Etch
Cycle Time: 7sec
Gas Flows: C_4F_8 = 0sccm, SF_6 = 130sccm, O_2 = 13sccm
Pressure: 35mTorr
Power: Coil = 600W, Bias = 20W @ 13.56MHz

Etch Rate: 350nm/cycle
Etch Time: Etch until shiny polysilicon layer is completely etched away. If visual check is not enough, use a multimeter to verify.

145. Post-Etch Cleaning: Backside layer removal (P1-P2)
Nanolab Tool: msink8
Options: msink7
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

146. Dicing (P1-P2)
Nanolab Tool: disco
Options: Manual dicing with a diamond scriber
Process Note: Sometimes dies fly away and get lost in the tool during dicing. Coating wafer with photoresist before starting dicing is a good idea to avoid this.

147. Release: Clean baskets, dishes, tweezers, and glass beakers
Nanolab Tool: msink16 & msink18
Options: None
Chemical: Piranha (Sulfuric Acid : Hydrogen Peroxide = 1 : 1)
Temperature: Set by the activated chemical
Time: 00:10:00
Process Note: Rinse all equipment with water before and after the piranha clean.

148. Release: Piranha clean dies
Nanolab Tool: msink16 & msink18
Options: None
Chemical: Piranha (Sulfuric Acid : Hydrogen Peroxide = 1 : 1)
Temperature: Set by the activated chemical
Time: 00:10:00
Process Note-1: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) before and after the piranha clean.

Process Note-2: Slowly agitate the basket during piranha clean to get bubbles out.

149. Release: Initial 49% HF release

Nanolab Tool: msink16 & msink18
Options: None
Chemical: 49% HF
Temperature: Room temperature
Time: 00:02:00
Process Note-1: This step removes the PSG hard mask and oxide spacer. Note that 2min in this step is not enough to fully release the devices.
Process Note-2: Agitate during this step to remove the bubbles formed during HF etch.
Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

150. Release: Piranha clean dies after initial 49% HF etch

Nanolab Tool: msink16 & msink18
Options: None
Chemical: Piranha (Sulfuric Acid : Hydrogen Peroxide = 1 : 1)
Temperature: Set by the activated chemical
Time: 00:20:00
Process Note-1: Clean any PSG residue left by the hard mask and oxide spacer with piranha.
Process Note-2: Slowly agitate the basket during piranha clean to get bubbles out.
Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

151. Release: Main 49% HF release

Nanolab Tool: msink16 & msink18
Options: None
Chemical: 49% HF
Temperature: Room temperature
Time: 00:33:00
Process Note-1: This step fully releases the devices.
Process Note-2: Agitate during this step to remove the bubbles formed during HF etch.
Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

152. Release: Piranha clean dies after main 49% HF etch

Nanolab Tool: msink16 & msink18
Options: None
Chemical: Piranha (Sulfuric Acid : Hydrogen Peroxide = 1 : 1)
Temperature: Set by the activated chemical
Time: 00:20:00
Process Note-1: Cleans any PSG residue left by the hard mask and oxide spacer with piranha. Also, cleans any residue remained in the actuation gap.
Process Note-2: Slowly agitate the basket during piranha clean to get bubbles out.

Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

153. Release: Final 49% HF release

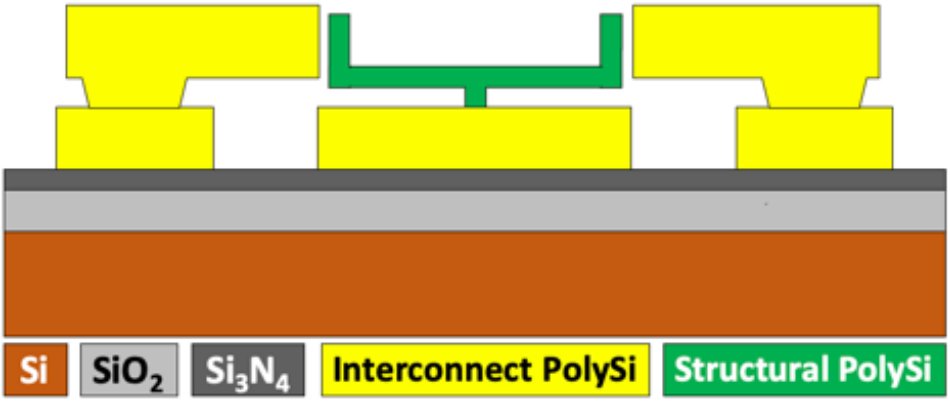
Nanolab Tool: msink16 & msink18
Options: None
Chemical: 49% HF
Temperature: Room temperature
Time: 00:05:00
Process Note-1: This step removes any oxide remained in the actuation gap as well as piranha-induced surface oxide.
Process Note-2: Agitate during this step to remove the bubbles formed during HF etch.
Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

154. Release: Methanol rinse

Nanolab Tool: msink16 & msink18
Options: None
Chemical: Methanol
Temperature: Room temperature
Time: 00:03:00
Process Note-1: Rinse the dies placed in a Teflon basket in Teflon dishes filled with methanol three times (each 1min) after this step. Methanol should completely replace DI water at the end of this step.
Process Note-2: It is extremely important that the dies never dry out between this step and the following critical point drying step to prevent stiction. Transfer dies to 'cpd' in a container filled with methanol.

155. Critical Point Drying

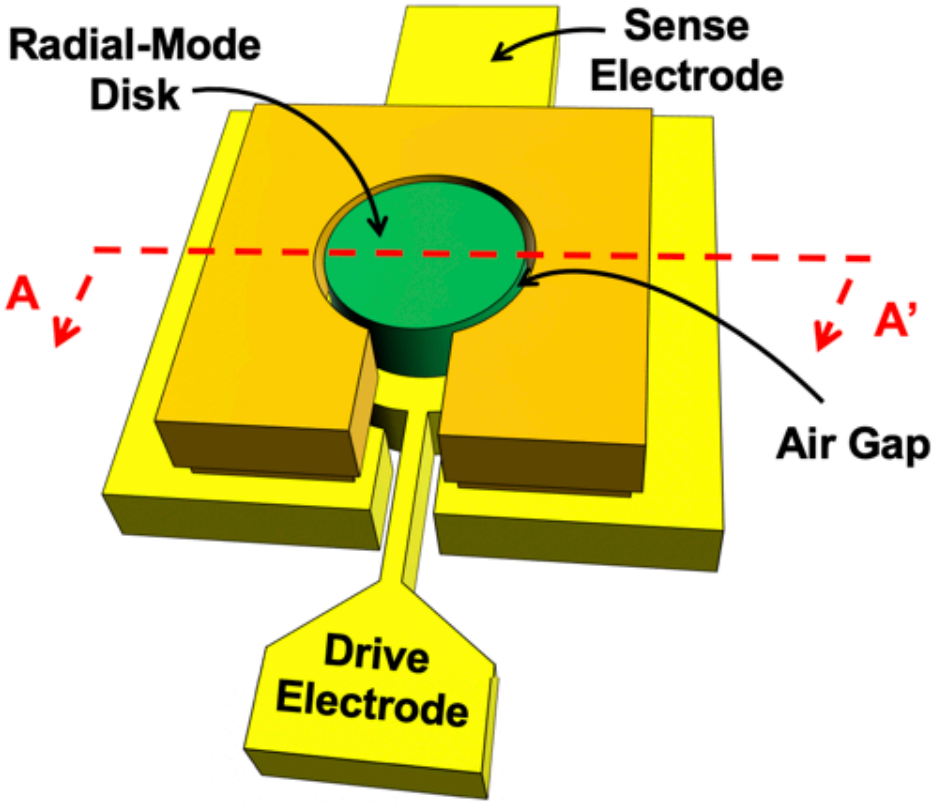
Nanolab Tool: cpd
Options: primaxx
Temperature: Set by the tool.
Purge Time: 00:25:00 (Setting '5')
Process Note: Make sure the methanol level in 'cpd' fully covers the dies before closing the chamber.
Cross Section:



156. Probe Station Testing

Tool: Lakeshore
Options: Wirebonding, MMR
Temperature: Room temperature
Vacuum: <100μTorr
Process Note: Make sure the Lakeshore probes are not bent and functional. Also, check the measurement setup, i.e., bias tees, cables etc., with a known working device in advance.

Appendix B
Polysilicon Solid Disk Process Traveler



0. Tools needed in the Nanolab

Deposition	*Etchers*	*Lithography*	*Metrology*	*Ann./Dope*	*Release*	*Cleaning*
tystar9	lam6	picotrack1	alphastep	tystar2	cpd	msink6
tystar10	lam8	picotrack2	flexus	tystar3		msink8
tystar11	sts2	asml300	cde-resmap	tystar4		msink16
tystar12	sts-oxide	technics-c	nanospec	tystar6		msink18
tystar16	cmp	axcelis	dektak			sinkcmp
tystar17		matrix				
cambridge						

1. Starting wafers (P1-P9, SN, S0-S3, S11-S19, TS0-TS3, TS11-TS19, O1-O5, TO1-TO5, CS1-CS6)

Doping: p-type

Wafer Class: prime
Wafer Size: 6”
Scribing: On the front, near the right hand side of the major flat.
Process Note-1: Never scribe the wafer back side as some tools apply vacuum on the back side to keep the wafers still and also to apply helium cooling.
Process Note-2: Make sure the scribing does not have any lines aligned with the Si wafer crystal orientation, making the wafer physically less resistant to mechanical force or impact such as water pressure during quick dump rinse (QDR), mechanical force and/or bending during wafer transfer, rotational force during spin rinse dry (SDR) etc. Use letters like ‘S’, ‘O’ that do not have any lines rather than ‘I’, ‘H’ or scribe the latter letters in angled way such that they are not aligned with the crystal axis.
Cross Section:

2. Cleaning: Pre-furnace cleaning (P1-P9, SN, S0-S3, S11-S19, TS0-TS3, TS11-TS19, O1-O5, TO1-TO5, CS1-CS6)

Nanolab Tool: msink6

1st Chemical:	Piranha	*2nd Chemical:*	10:1 HF
Temperature:	120°C	*Temperature:*	Room temperature
Time:	00:10:00	*Time:*	00:02:00

3. Test Deposition: Thin oxide dummy wafer (TS0)

Nanolab Tool: tystar11
Options: tystar9, tystar12, tystar17
Recipe: 11SULTON
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 11.58nm/min
Time: 00:15:00
Process Note-1: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.

4. Test Metrology: Thin oxide thickness measurement (TS0)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)

Thickness:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Dep. Rate:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____

5. **Deposition: Thin oxide dummy wafers (O1-O4, TO1-TO4)**
   Nanolab Tool: tystar11
   Options: tystar9, tystar12, tystar17
   Recipe: 11SULTON
   Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
   Pressure: 400mTorr
   Temperature: 450°C
   Dep. Rate: 11.58nm/min (adjust if needed)
   Time: 00:08:00 (adjust if needed)
   Goal: 100nm
   Process Note-1: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.
   Process Note-2: These wafers will be used as control and test wafers in several subsequent polysilicon depositions alongside the actual process wafers. The reason for the very thin oxide layer is because 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

6. **Deposition: Isolation oxide (P1-P9)**
   Nanolab Tool: tystar11
   Options: tystar9, tystar12, tystar17
   Recipe: 11SULTON
   Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
   Pressure: 400mTorr
   Temperature: 450°C
   Dep. Rate: 11.58nm/min (adjust if needed)
   Time: 03:00:00 (adjust if needed)
   Goal: 2µm
   Process Note: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.
   Cross Section:

7. **Annealing: Thin and isolation oxide densification (P1-P9, O1-O4, TO1-TO4)**
   Nanolab Tool: tystar2
   Options: tystar3, tystar4
   Recipe: 2HIN2ANA
   Temperature: 1000°C
   Time: 01:00:00

Process Note: Unannealed low temperature oxide (LTO) sometimes bubbles at high temperatures. So, annealing immediately after the deposition prevents this from happening at later stages in the process.

8. Metrology: Thin oxide thickness measurement (O1-O4, TO1-TO4)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 100nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

9. Metrology: Isolation oxide thickness measurement (P1-P9)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Expected: 2µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

10. Test Deposition: Isolation nitride (S0)

Nanolab Tool: tystar9
Options: tystar17, cambridge Al_2O_3
Recipe: 9LSNVARA
Gas Flows: DCS = 100sccm, NH_3 = 18sccm
Pressure: 375mTorr
Temperature: 835°C
Time: 01:00:00

11. Test Metrology: Isolation nitride thickness measurement (S0)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

12. Deposition: Isolation nitride (P1-P9, SN)

Nanolab Tool: tystar9
Options: tystar17, cambridge Al_2O_3
Recipe: 9LSNVARA
Gas Flows: DCS = 100sccm, NH_3 = 18sccm
Pressure: 375mTorr
Temperature: 835°C
Dep. Rate: 2.78nm/min (adjust if needed)
Time: 03:00:00 (adjust if needed)
Goal: 500nm

Process Note-1: Include a bare silicon wafer ('S1') as a test wafer for the thickness measurement. 'nanospec' can measure nitride layer thickness correctly only when the underlying layer is silicon.

Process Note-2: Note that the deposition rate variation in tystar9 low stress nitride deposition is significant, i.e., ~25% from the center of the rear 6" boat to that of the front 6" boat. So, use at most six wafers and an additional bare Si test wafer ('S1') in each deposition to obtain good average thickness uniformity between the process wafers.

Cross Section:

13. Post-Deposition Cleaning: Nitride surface cleaning (P1-P9, SN)

Nanolab Tool: msink6
Options: msink8, msink16, msink18

1st Chemical:	Piranha	*2nd Chemical:*	25:1 HF (or 10:1 HF)
Temperature:	120°C	*Temperature:*	Room temperature
Time:	00:10:00	*Time:*	00:05:00

Process Note: Nitride furnaces are notoriously known to deposit particles on wafer surface. Such particles, if not removed properly, may cause adhesion issues for the subsequent layer in the process, i.e., polysilicon. Cleaning with piranha and HF helps remove these particles and provides with better surface condition for the following layer.

14. Metrology: Isolation nitride initial thickness measurement (SN)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Expected: 500nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Use the test wafer ('S1') obtained in the previous step. Do not use the actual process wafers for this measurement as 'nanospec' can measure nitride layer thickness correctly only when the underlying layer is silicon.

15. Etch: Isolation nitride 49% HF etch rate test (SN)

Nanolab Tool: msink7
Options: msink16, msink18
1st Chemical: 49% HF
Temperature: Room temperature
Time: 00:10:00

Process Note: We have recently realized an enhanced 49% HF etch rate for nitride coming out of 'tystar17'. 'tystar9' low stress nitride (LSN) seems to be more resistant to 49% HF. Due to very long 49% HF release times, i.e., longer than 30min, it is important that the nitride etch rate stays below 1-2nm/min to prevent excessive polysilicon interconnect undercut. So, this test is necessary to make sure the isolation nitride will be resistant enough to 49% HF during device release at the end of the process.

16. Metrology: Isolation nitride 49% HF etch rate measurement (SN)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Target: < 2nm/min
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Etch Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: If the target is not met, recipe changes might be needed. Note that even an enhanced nitride etch rate in 49% HF might be acceptable depending on the release time. For example, 5nm/min might be excessive for a 120min-release but acceptable for a 30min-release.

17. Test Deposition: Interconnect layer oxide mold (TS1)

Nanolab Tool: tystar12
Options: tystar11, tystar9-HTO, tystar17-HTO
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C
Time: 01:00:00
Process Note: Use a bare silicon wafer ('TS1') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

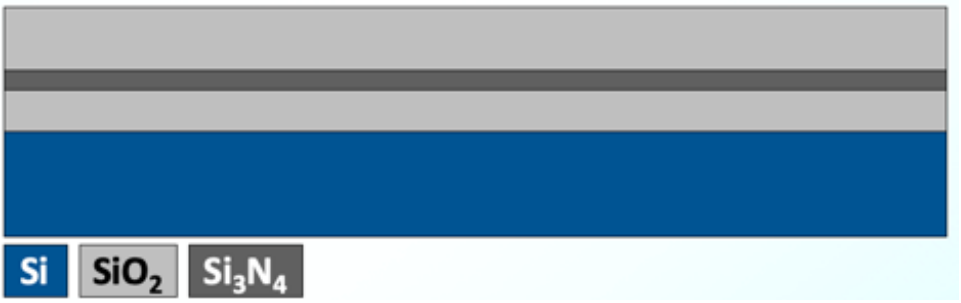
18. Test Metrology: Interconnect layer oxide mold (TS1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

19. Deposition: Interconnect layer oxide mold (P1-P9, S1)

Nanolab Tool: tystar12
Options: tystar11, tystar9-HTO, tystar17-HTO
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C

Dep. Rate: 14.7nm/min (adjust if needed)
Time: 03:00:00 (adjust if needed)
Goal: 2.5µm
Process Note: Use a bare silicon wafer ('S1') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



20. Annealing: Interconnect layer oxide mold densification (P1-P9, S1)

Nanolab Tool: tystar3
Options: tystar2, tystar4
Recipe: 3HIN2ANA
Temperature: 1000°C
Time: 01:00:00
Process Note: Unannealed low temperature oxide (LTO) sometimes bubbles at high temperatures. So, annealing immediately after the deposition prevents this from happening at later stages in the process.

21. Metrology: Interconnect layer oxide mold thickness measurement (S1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Expected: 2.5µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

22. PR Coating: Interconnect layer oxide mold photoresist [P1DF] (P1-P9, S1)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 900nm
Recipe: T1_UV210-0.6_0.87um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

23. PR Exposure: PM alignment marks (P1-P9, S1)

Nanolab Tool: asml300
Options: None

ASML Job: DISKRUN_R2
Reticle: COMBI Reticle
Field: PM layer
Exposure: 20mJ
Focus: 0nm

24. PR Development: PM alignment marks (P1-P9, S1)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Twice
Process Note-1: Always run at least one dummy wafer first and visually check the developer uniformity.
Process Note-2: Develop twice for dark field masks to make sure all residual photoresist in the patterned area gets removed.

25. PR Exposure: Interconnect layer oxide mold photoresist [P1DF] (P1-P9, S1)

Nanolab Tool: asml300
Options: None
ASML Job: DISKRUN_R2
Reticle: DISKRUN_R2
Field: P1DF - TOPRIGHT
Exposure: 20mJ
Focus: 0nm

26. PR Development: Interconnect layer oxide mold photoresist [P1DF] (P1-P9, S1)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Twice
Process Note-1: Always run at least one dummy wafer first and visually check the developer uniformity.
Process Note-2: Develop twice for dark field masks to make sure all residual photoresist in the patterned area gets removed.

27. PR Descum: Interconnect layer oxide mold photoresist [P1DF] (P1-P9, S1)

Nanolab Tool: technics-c
Options: None
Gas Flows: O_2 = 180sccm
Power: 30W
Time: 00:00:30

Process Note: 'technics-c' etch rates wildly changes from time to time. Take the numbers in the manual as a reference and make sure to test the current etch rate especially if there are designs with feature size less than 500nm and precise width control is critical.

28. PR UV-bake: Interconnect layer oxide mold photoresist [P1DF] (P1-P9, S1)

Nanolab Tool: axcelis
Options: None
Program: U

29. Etch: Interconnect layer oxide mold [P1DF] (P1-P9, S1)

Nanolab Tool: sts-oxide
Options: lam6
Recipe Name: Oxide etch (APS) no 2-2
Gas Flows: C_4F_8 = 15sccm, H_2 = 4sccm, He = 174sccm
Pressure: 10mTorr
Power: Coil = 1500W, Bias = 400W @ 13.56MHz
Etch Rate: 406nm/min
Selectivity: UV210 Photoresist (UV-baked) : Annealed PSG = 1 : 3.49
Etch Time: 00:07:00
Process Note-1: Use the test wafer 'S1' to test the current etch rate and also to condition the chamber before etching the process wafers.
Process Note-2: 15% over etch is included.
Process Note-3: It is extremely important that no oxide layer or etch residue remains in the unprotected region atop the isolation nitride layer at the end of this step. Use thicker photoresist and do more over etch if needed. Any oxide remained here will be between the interconnect layer and isolation nitride and might cause the interconnect pads and traces to float and wash away during 49% HF release at the end of the process.
Cross Section:

30. PR Strip: Interconnect layer oxide mold photoresist [P1DF] (P1-P9, S1)

Nanolab Tool: matrix
Options: technics-c, msink1-1165, msink16 & msink18-PRS3000
Pressure: 3.75Torr
Temperature: 250°C
Power: 400W
Time: 00:02:30

Process Note: Run the recipe twice.

31. Metrology: Interconnect layer oxide mold step height measurement (P1-P9, S1)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 10µm
Expected: 2.5µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

32. Metrology: Wafer bow measurement (P1-P9, S1)

Nanolab Tool: flexus
Options: None
Program: Ozgurluk/BaseSi.dat
Target: < 20µm
Result: ____
Process Note: If not, etch the back side using the same tool as the front side has been etched until the target is met. Note that the maximum allowable wafer bow for asml300 is 50µm.

33. Pre-Deposition Cleaning: Polysilicon interconnect layer – 1st pass (P1-P9, S1, O1, TO1)

Nanolab Tool: msink8
Options: msink7
1st Chemical: Piranha at 120°C
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
2nd Chemical: 25:1 HF
Temperature: Room temperature
Time: 00:00:05

Process Note-1: Include a thin oxide dummy test wafer ('O1') for the subsequent polysilicon deposition step.
Process Note-2: Make sure to test the 25:1 HF etch rate first with a dummy wafer. It is always better to take the posted etch rates and chemical ratios as a reference but not to fully trust them in a university lab.
Process Note-3: It is extremely important that no oxide layer or etch residue remains in the unprotected region atop the isolation nitride layer at the end of this step. So, the last 25:1 HF dip is critical for this reason. Any oxide remained here will be between the interconnect layer and isolation nitride and might cause the interconnect pads and traces to float and wash away during 49% HF release at the end of the process.
Process Note-4: After HF dip, make sure to quickly transfer the wafers to the furnace for the interconnect layer deposition.

34. Test Deposition: Polysilicon interconnect layer – 1st pass (TO1)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Time: 01:00:00
Process Note: Use a thin oxide dummy wafer ('TO1') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

35. Test Metrology: Polysilicon interconnect layer – 1st pass (TO1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

36. Deposition: Polysilicon interconnect layer – 1st pass (P1-P9, S1, O1)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Dep. Rate: 6.25nm/min (adjust if needed)
Time: 01:20:00 (adjust if needed)
Goal: 500nm
Process Note: Use a thin oxide dummy wafer ('O1') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

37. $POCl_3$ Doping: Polysilicon interconnect layer – 1st pass (P1-P9, S1, O1)

Nanolab Tool: tystar6
Options: tystar13, tystar11/tystar12 (dope) + tystar2/tystar3/tystar4 (drive-in)
Recipe: PCLO2.006
Gas Flows: N_2 = 200sccm, O_2 = 300sccm
Doping Temperature: 1050°C
Doping Time: 01:00:00
Drive-in Temperature: 1050°C
Drive-in Time: 02:00:00
Process Note: Place the wafers in every other slot to make sure the heat distribution stays uniform during doping and drive-in.

38. $POCl_3$ Doping: PSG removal and cleaning (P1-P9, S1, O1)

Nanolab Tool: msink8

1st Chemical: 10:1 HF *2nd Chemical:* Piranha at 120°C
Temperature: Room temperature *Temperature:* 120°C
Time: 00:10:00 *Time:* 00:10:00
Process Note: This phospho-silicate glass (PSG) layer forms during $POCL_3$ doping and must be removed afterwards. Its thickness is usually around 100-200nm. Note that after $POCL_3$ doping and PSG removal, polysilicon surface becomes extremely rough.

39. Metrology: Polysilicon interconnect layer thickness measurement – 1st pass (O1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 3µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note-1: Use the thin oxide dummy ('O1') obtained in the previous step for polysilicon thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

Process Note-2: Since the polysilicon surface becomes extremely rough after $POCL_3$ doping and PSG removal, optical thin film measurement might fail. In this case, a very short chemical mechanical polishing (CMP) might be necessary to polish the surface.

40. (Optional) Chemical Mechanical Polishing: Polysilicon interconnect layer – 1st pass (CS1, O1)

Nanolab Tool: cmp
Options: None
Recipe: Poly.polish
Down Force: 8psi
Back Pres.: 6psi
Table RPM: 24
Chuck RPM: 6
Slurry Name: Cabot iDiel D3543
Slurry Flow: 100ml/min
Etch Rate: 140nm/min
Time: Front Side → 1min
Process Note: Make sure to run a bare Si dummy wafer ('CS1') to check for scratches before processing the process wafers. Major scratches are usually visible on a bare Si wafer. However, a patterned wafer is necessary to see minor scratches under a microscope.

41. (Optional) Post-CMP cleaning: Polysilicon interconnect layer – 1st pass (CS1, O1)

Nanolab Tool: sinkcmp
Options: None
Chemical: Water

Process Note: Clean the wafer front and back side with PVD sponge four times for 15sec with 90° wafer rotation each time, then follow with four full QDR cycles at sinkcmp.

Nanolab Tool: msink8
Options: msink16, msink18
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
Process Note: Transfer wafers from Cory 190 to the Nanolab immediately in a box filled with water and start piranha cleaning. It is extremely important that the wafers never dry out with cmp silica particles on them.

42. (Optional) Metrology: Polysilicon interconnect layer thickness measurement – 1st pass (O1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 4µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

43. Chemical Mechanical Polishing: Polysilicon interconnect layer – 1st pass (P1-P9, S1, CS2)

Nanolab Tool: cmp
Options: None
Recipe: Poly.polish
Down Force: 8psi
Back Pres.: 6psi
Table RPM: 24
Chuck RPM: 6
Slurry Name: Cabot iDiel D3543
Slurry Flow: 100ml/min
Etch Rate: 140nm/min
Time: Front Side → 2min x 4 with 90° wafer rotation, pad conditioning
Back Side → 2min x 4 with 90° wafer rotation, pad conditioning
Front Side → 1min x 4 with 90° wafer rotation, pad conditioning
Process Note-1: Note that the provided etch rate is for a flat LPCVD polysilicon layer. Make sure to check the current removal rate using the test wafer ('CS2'). This etch rate considerably enhances in the presence of topography as the effective pressure increases.
Process Note-2: As the etch rate is topography dependent, it is important to visually check the wafer both with naked eye and under a microscope after each CMP cycle to make sure 'cmp' does not start removing the underlying oxide mold layer excessively.
Process Note-3: 'cmp' tool is uniform when removing thin layers but it is not uniform for removing layers thicker than 1µm. The purpose of rotating wafer by 90° every minute is to enhance the uniformity over the wafer surface.

Process Note-4: The purpose of back side cmp is to correct the wafer bow so that edge-to-center CMP uniformity does not degrade during polishing.

Process Note-5: Make sure to run a bare Si dummy wafer ('CS2') and a patterned test wafer ('S1') to check for scratches before processing the process wafers. Major scratches are usually visible on a bare Si wafer ('CS2'). However, a patterned wafer ('S1') is necessary to see minor scratches under a microscope.

Process Note-6: Note that the front side CMP should continue until all SiO_2 interconnect layer mold patterns expose.

44. Post-CMP cleaning: Polysilicon interconnect layer – 1st pass (P1-P9, S1, CS2)

Nanolab Tool: sinkcmp
Options: None
Chemical: Water
Process Note: Clean the wafer front and back side with PVD sponge four times for 15sec with 90° wafer rotation each time, then follow with four full QDR cycles at sinkcmp.

Nanolab Tool: msink8
Options: msink16, msink18
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
Process Note: Transfer wafers from Cory 190 to the Nanolab immediately in a box filled with water and start piranha cleaning. It is extremely important that the wafers never dry out with cmp silica particles on them.

45. Metrology: Wafer bow measurement (P1-P9, S1)

Nanolab Tool: flexus
Options: None
Program: Ozgurluk/BaseSi.dat
Target: < 20μm
Result: _____
Process Note: If not, etch the back side using 'sts2' or 'lam8' until the target is met. Note that the maximum allowable wafer bow for asml300 is 50μm.

46. Pre-Deposition Cleaning: Polysilicon interconnect layer – 2nd pass (P1-P9, S1, O2, TO2)

Nanolab Tool: msink8
Options: msink7
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None
1st Chemical: Piranha
Temperature: 120°C
2nd Chemical: 25:1 HF
Temperature: Room temperature

Time: 00:10:00 *Time:* 00:00:03

Process Note-1: Include a thin oxide dummy test wafer ('O2') for the subsequent polysilicon deposition step.

Process Note-2: Make sure to test the 25:1 HF etch rate first with a dummy wafer. It is always better to take the posted etch rates and chemical ratios as a reference but not to fully trust them in a university lab.

Process Note-3: It is important that no native oxide layer remains atop the polysilicon layer deposited and polished in the previous steps. So, the last 25:1 HF dip is critical for this reason. Any oxide remained here will be between the two separately deposited polysilicon layer and degrade the interconnect layer resistance.

Process Note-4: After HF dip, make sure to quickly transfer the wafers to the furnace for the interconnect layer deposition.

47. Test Deposition: Polysilicon interconnect layer – 2nd pass (TO2)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Time: 01:00:00
Process Note: Use a thin oxide dummy wafer ('TO2') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

48. Test Metrology: Polysilicon interconnect layer – 2nd pass (TO2)

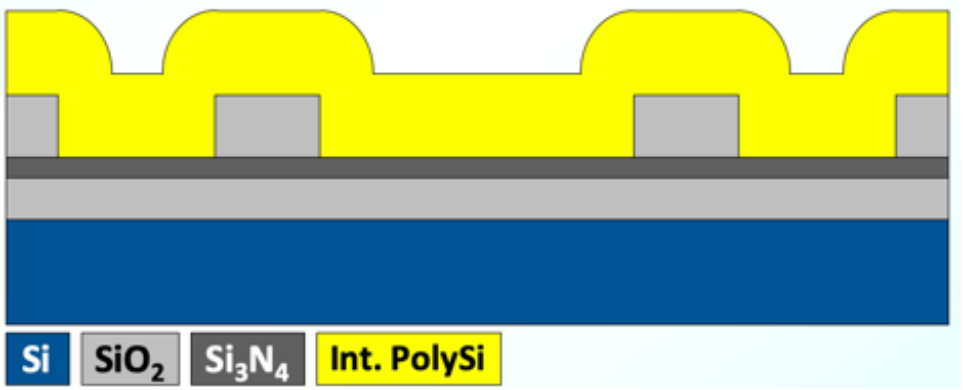
Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)

Thickness:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Dep. Rate:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____

49. Deposition: Polysilicon interconnect layer – 2nd pass (P1-P9, S1, O2)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Dep. Rate: 6.25nm/min (adjust if needed)
Time: 01:20:00 (adjust if needed)
Goal: 500nm
Process Note: Use a thin oxide dummy wafer ('O2') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

Cross Section:



50. $POCl_3$ Doping: Polysilicon interconnect layer – 2nd pass (P1-P9, S1, O2)

Nanolab Tool: tystar6
Options: tystar13, tystar11/tystar12 (dope) + tystar2/tystar3/tystar4 (drive-in)
Recipe: PCLO2.006
Gas Flows: N_2 = 200sccm, O_2 = 300sccm
Doping Temperature: 1050°C
Doping Time: 01:00:00
Drive-in Temperature: 1050°C
Drive-in Time: 02:00:00
Process Note: Place the wafers in every other slot to make sure the heat distribution stays uniform during doping and drive-in.

51. $POCl_3$ Doping: PSG removal and cleaning (P1-P9, S1, O2)

Nanolab Tool: msink8

1st Chemical:	10:1 HF	*2nd Chemical:*	Piranha
Temperature:	Room temperature	*Temperature:*	120°C
Time:	00:10:00	*Time:*	00:10:00

Process Note: This phospho-silicate glass (PSG) layer forms during $POCL_3$ doping and must be removed afterwards. Its thickness is usually around 100-200nm. Note that after $POCL_3$ doping and PSG removal, polysilicon surface becomes extremely rough.

52. Metrology: Polysilicon interconnect layer thickness measurement – 2nd pass (O2)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 3µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note-1: Use the thin oxide dummy ('O2') obtained in the previous step for polysilicon thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

Process Note-2: Since the polysilicon surface becomes extremely rough after $POCL_3$ doping and PSG removal, optical thin film measurement might fail. In this case, a

very short chemical mechanical polishing (CMP) might be necessary to polish the surface.

53. (Optional) Chemical Mechanical Polishing: Polysilicon interconnect layer – 2nd pass (CS3, O2)

Nanolab Tool: cmp
Options: None
Recipe: Poly.polish
Down Force: 8psi
Back Pres.: 6psi
Table RPM: 24
Chuck RPM: 6
Slurry Name: Cabot iDiel D3543
Slurry Flow: 100ml/min
Etch Rate: 140nm/min
Time: Front Side → 1min
Process Note: Make sure to run a bare Si dummy wafer ('CS3') to check for scratches before processing the process wafers. Major scratches are usually visible on a bare Si wafer. However, a patterned wafer is necessary to see minor scratches under a microscope.

54. (Optional) Post-CMP cleaning: Polysilicon interconnect layer – 2nd pass (O2)

Nanolab Tool: sinkcmp
Options: None
Chemical: Water
Process Note: Clean the wafer front and back side with PVD sponge four times for 15sec with 90° wafer rotation each time, then follow with four full QDR cycles at sinkcmp.

Nanolab Tool: msink8
Options: msink16, msink18
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
Process Note: Transfer wafers from Cory 190 to the Nanolab immediately in a box filled with water and start piranha cleaning. It is extremely important that the wafers never dry out with cmp silica particles on them.

55. (Optional) Metrology: Polysilicon interconnect layer thickness measurement – 2nd pass (O2)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 4µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

56. Chemical Mechanical Polishing: Polysilicon interconnect layer – 2nd pass (P1-P9, S1, CS4)

Nanolab Tool: cmp
Options: None
Recipe: Poly.polish
Down Force: 8psi
Back Pres.: 6psi
Table RPM: 24
Chuck RPM: 6
Slurry Name: Cabot iDiel D3543
Slurry Flow: 100ml/min
Etch Rate: 140nm/min
Time: Front Side → 2min x 4 with 90° wafer rotation, pad conditioning
Back Side → 2min x 4 with 90° wafer rotation, pad conditioning
Front Side → 1min x 4 with 90° wafer rotation, pad conditioning

Process Note-1: Note that the provided etch rate is for a flat LPCVD polysilicon layer. Make sure to check the current removal rate using the test wafer ('CS4'). This etch rate considerably enhances in the presence of topography as the effective pressure increases.

Process Note-2: As the etch rate is topography dependent, it is important to visually check the wafer both with naked eye and under a microscope after each CMP cycle to make sure 'cmp' does not start removing the underlying oxide mold layer excessively.

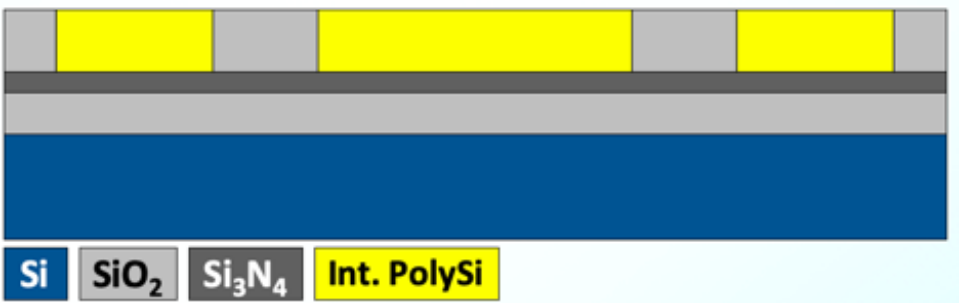
Process Note-3: 'cmp' tool is uniform when removing thin layers but it is not uniform for removing layers thicker than 1µm. The purpose of rotating wafer by 90° every minute is to enhance the uniformity over the wafer surface.

Process Note-4: The purpose of back side cmp is to correct the wafer bow so that edge-to-center CMP uniformity does not degrade during polishing.

Process Note-5: Make sure to run a bare Si dummy wafer ('CS4') and a patterned test wafer ('S1') to check for scratches before processing the process wafers. Major scratches are usually visible on a bare Si wafer ('CS4'). However, a patterned wafer ('S1') is necessary to see minor scratches under a microscope.

Process Note-6: Note that the front side CMP should continue until all SiO_2 interconnect layer mold patterns expose.

Cross Section:



57. Post-CMP cleaning: Polysilicon interconnect layer – 2nd pass (P1-P9, S1, CS4)

Nanolab Tool: sinkcmp
Options: None
Chemical: Water
Process Note: Clean the wafer front and back side with PVD sponge four times for 15sec with 90° wafer rotation each time, then follow with four full QDR cycles at sinkcmp.

Nanolab Tool: msink8
Options: msink16, msink18
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
Process Note: Transfer wafers from Cory 190 to the Nanolab immediately in a box filled with water and start piranha cleaning. It is extremely important that the wafers never dry out with cmp silica particles on them.

58. Metrology: Wafer bow measurement (P1-P9, S1)

Nanolab Tool: flexus
Options: None
Program: Ozgurluk/BaseSi.dat
Target: < 20µm
Result: ____
Process Note: If not, etch the back side using 'sts2' or 'lam8' until the target is met. Note that the maximum allowable wafer bow for asml300 is 50µm.

59. Metrology: Polysilicon interconnect layer (P1-P9)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance between pads that are not connected on the layout. If the polysilicon removal is complete, this measurement should indicate infinite resistance ('open').

60. Metrology: Polysilicon interconnect layer sheet resistance measurement (P1-P9)

Nanolab Tool: probe8
Options: Wentworth
Diagnostic: 4-point probe test structures on the die layout
Expected: 4-5Ω/□
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

61. Pre-Deposition Cleaning: Oxide spacer (P1-P9, S2, TS2)

Nanolab Tool: msink8
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
1st Chemical: Piranha *2nd Chemical:* 25:1 HF
Temperature: 120°C *Temperature:* Room temperature
Time: 00:10:00 *Time:* 00:00:03
Process Note: Make sure to test the 25:1 HF etch rate first with a dummy wafer. It is always better to take the posted etch rates and chemical ratios as a reference but not to fully trust them in a university lab.

62. Test Deposition: Oxide spacer (TS2)

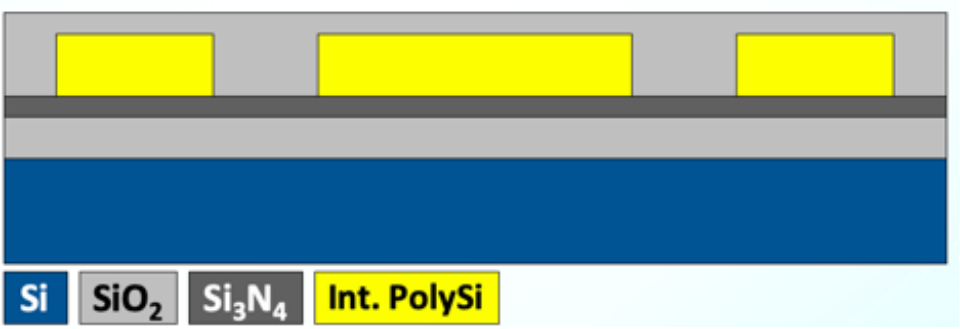
Nanolab Tool: tystar12
Options: tystar11, tystar9, tystar17
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C
Time: 01:00:00
Process Note: Use a bare silicon wafer ('TS2') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

63. Test Metrology: Oxide spacer thickness measurement (TS2)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

64. Deposition: Oxide spacer (P1-P2, S2)

Nanolab Tool: tystar12
Options: tystar11, tystar9, tystar17
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 14.7nm/min (adjust if needed)
Time: 00:34:00 (adjust if needed)
Goal: 500nm
Process Note: Use a bare silicon wafer ('S2') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



65. Annealing: Oxide spacer densification (P1-P2, S2)

Nanolab Tool: tystar3
Options: tystar2, tystar4
Recipe: 3HIN2ANA
Temperature: 950°C
Time: 01:00:00
Process Note: Unannealed phospho-silicate glass (PSG) sometimes bubbles at high temperatures. So, annealing immediately after the deposition prevents this from happening at later stages in the process.

66. Metrology: Oxide spacer thickness measurement (S2)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Expected: 500nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

67. PR Coating: Stem layer photoresist [P2DF] (P1-P9, S2)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 900nm
Recipe: T1_UV210-0.6_0.87um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

68. PR Exposure: Stem layer photoresist [P2DF] (P1-P9, S2)

Nanolab Tool: asml300
Options: None
ASML Job: DISKRUN_R1
Reticle: DISKRUN_R1
Field: P2DF - TOPRIGHT
Exposure: 26mJ (P1-P6, S6) / 34mJ (P7-P9)
Focus: 0nm

Process Note: It is important to use a high enough exposure rate for this mask to make sure the stem holes are fully exposed as they are really tiny. Run a focus-exposure matrix (FEM) first if needed.

69. PR Development: Stem layer photoresist [P2DF] (P1-P9, S2)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Twice
Process Note-1: Always run at least one dummy wafer first and visually check the developer uniformity.
Process Note-2: Develop twice for dark field masks to make sure all residual photoresist in the patterned area gets removed.

70. PR Descum: Stem layer photoresist [P2DF] (P1-P9, S2)

Nanolab Tool: technics-c
Options: None
Gas Flows: O_2 = 180sccm
Power: 30W
Time: 00:00:30
Process Note-1: 'technics-c' etch rates wildly changes from time to time. Take the numbers in the manual as a reference and make sure to test the current etch rate especially if there are designs with feature size less than 500nm and precise width control is critical.
Process Note-2: It is important to do a bit longer descum for this mask to make sure any residual PR gets removed as the stem holes are really tiny.

71. PR UV-bake: Stem layer photoresist [P2DF] (P1-P9, S2)

Nanolab Tool: axcelis
Options: None
Program: U

72. Etch: Oxide spacer [P2DF] (P1-P9, S2)

Nanolab Tool: lam6
Options: sts-oxide
Recipe Name: 6001_OXIDE_ME
Gas Flows: Ar = 150sccm, CHF_3 = 25sccm, CF_4 = 25sccm
Pressure: 70mTorr
Power: 350W
Etch Rate: 540nm/min (for P2DF mask)
Selectivity: UV210 Photoresist (UV-baked) : Annealed PSG = 1:7.7
Etch Time: 3min (3 cycles of [1min SiO_2 etch + 1min rest] to prevent PR from burning)

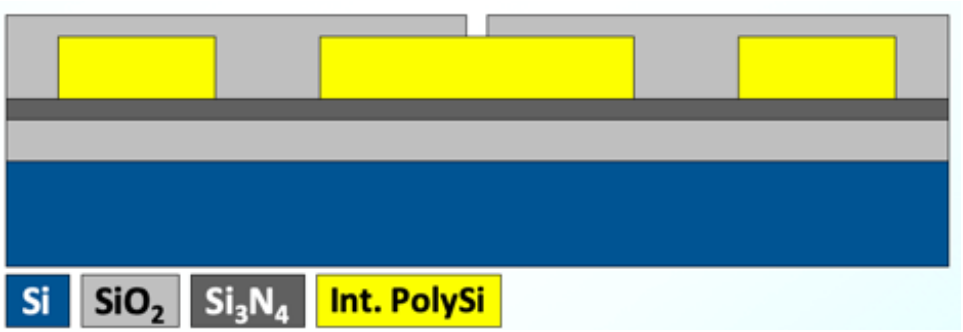
Process Note-1: With default recipe power of 500W, the SiO2 etch rate is too fast, i.e., 740nm/min, and PR:SiO2 selectivity is low, i.e., 1:4.25. Lowering the power substantially helps with the etch selectivity.

Process Note-2: Note that 'lam6' burns UV210 resist if the etch time is longer than 1min. To prevent this from happening, the process wafer should rest for 1min in the etch chamber with the RF power turned off after 1min etch.

Process Note-3: Make sure to run 3 dummies with the oxygen clean recipe and also check the current etch rate and selectivity with the test wafer 'S4' by doing a 1min etch beforehand. This will also condition the chamber.

Process Note-4: A 200% overetch is performed to make sure the stem holes are fully open.

Cross Section:



73. PR Strip: Stem layer photoresist [P2DF] (P1-P9, S2)

Nanolab Tool: matrix
Options: technics-c, msink1-1165, msink16 & msink18-PRS3000
Pressure: 3.75Torr
Temperature: 250°C
Power: 400W
Time: 00:02:30
Process Note: Run the recipe twice.

74. Metrology: Stem layer step height measurement (P1-P9)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 5µm
Expected: 600nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Use the patterns in the diagnostics layout to make this measurement.

75. Metrology: Wafer bow measurement (P1-P9)

Nanolab Tool: flexus
Options: None
Program: Ozgurluk/BaseSi.dat
Target: < 20µm
Result: ____

Process Note: If not, etch the back side using the same tool as the front side has been etched until the target is met. Note that the maximum allowable wafer bow for asml300 is 50µm.

76. Pre-Deposition Cleaning: Polysilicon structural layer (P1-P9, O3, TO3)

Nanolab Tool: msink8
Options: msink7
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink8
Options: msink7
1st Chemical: 50:1 HF
Temperature: 120°C
Time: 00:00:10
Process Note-1: Include a thin oxide dummy test wafer ('O3') for the subsequent polysilicon deposition step.
Process Note-2: Make your own 50:1 HF in msink8 ambient bath mixing 16L water and 320mL 49% HF. Use this bath to do native oxide removal right before the following deposition.
Process Note-3: It is important to quickly transfer wafers to the furnace after this step to prevent any native oxide formation in the stem opening.

77. Test Deposition: Polysilicon structural layer (TO3)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Time: 01:00:00
Process Note: Use a thin oxide dummy wafer ('TO3') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

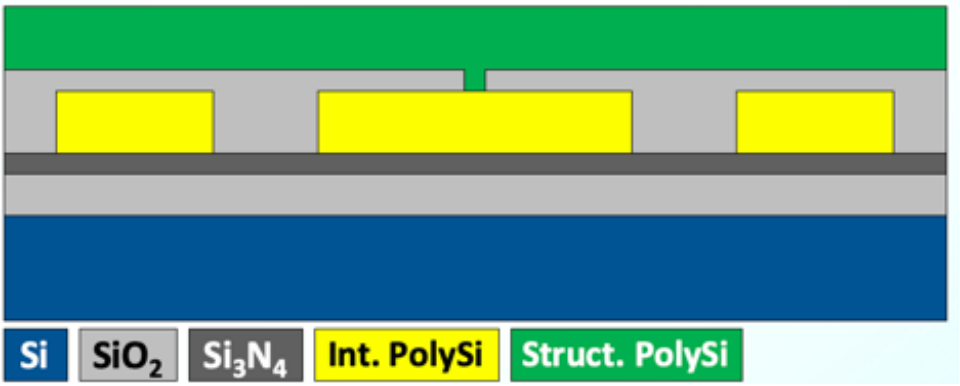
78. Test Metrology: Polysilicon structural layer thickness measurement (TO3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)

Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

79. Deposition: Polysilicon structural layer (P1-P9, O3)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Dep. Rate: 6.25nm/min (adjust if needed)
Time: 01:20:00 (adjust if needed)
Goal: 500nm
Process Note: Use a thin oxide dummy wafer ('O3') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.
Cross Section:



80. Metrology: Polysilicon structural layer thickness measurement (O3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 500nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

81. Chemical Mechanical Polishing: Polysilicon structural layer (P1-P9, CS5, O3)

Nanolab Tool: cmp
Options: None
Recipe: Poly.polish
Down Force: 8psi
Back Pres.: 6psi
Table RPM: 24
Chuck RPM: 6
Slurry Name: Cabot iDiel D3543
Slurry Flow: 100ml/min

Etch Rate: 140nm/min
Time: Front Side → 1min
Process Note: Make sure to run a bare Si dummy wafer ('CS5') to check for scratches before processing the process wafers. Major scratches are usually visible on a bare Si wafer. However, a patterned wafer is necessary to see minor scratches under a microscope.

82. Post-CMP cleaning: Polysilicon structural layer (P1-P9, CS5, O3)

Nanolab Tool: sinkcmp
Options: None
Chemical: Water
Process Note: Clean the wafer front and back side with PVD sponge four times for 15sec with 90° wafer rotation each time, then follow with four full QDR cycles at sinkcmp.

Nanolab Tool: msink8
Options: msink16, msink18
1st Chemical: Piranha at 120°C
Temperature: 120°C
Time: 00:10:00
Process Note: Transfer wafers from Cory 190 to the Nanolab immediately in a box filled with water and start piranha cleaning. It is extremely important that the wafers never dry out with cmp silica particles on them.

83. Metrology: Polysilicon interconnect layer thickness measurement (O3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 4µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

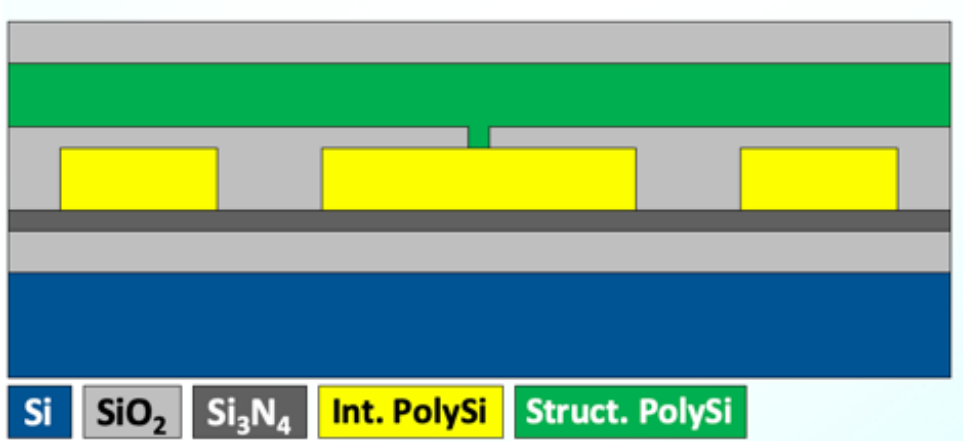
84. Pre-Deposition Cleaning: Oxide hard mask (P1-P9, O3, S3, TS3)

Nanolab Tool: msink8
Options: msink7
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None
1st Chemical: Piranha at 120°C
Temperature: 120°C
Time: 00:10:00
2nd Chemical: 25:1 HF
Temperature: Room temperature
Time: 00:02:00
Process Note: Include a thin oxide dummy test wafer ('S3') for the subsequent oxide deposition step.

85. Test Deposition: Oxide hard mask (TS3)

Nanolab Tool: tystar12
Options: tystar11, tystar9, tystar17
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C
Time: 01:00:00
Process Note: Use a bare silicon wafer ('TS3') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



86. Test Metrology: Oxide hard mask thickness measurement (TS3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

87. Deposition: Oxide hard mask (P1-P9, O3, S3)

Nanolab Tool: tystar12
Options: tystar11, tystar9, tystar17
Recipe: 12VDLTOA
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm, PH_3/Si = 40sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 14.7nm/min (adjust if needed)
Time: 02:45:00 (adjust if needed)
Goal: 2µm
Process Note: Use a bare silicon wafer ('S3') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

88. Annealing: Drive-in & oxide hard mask densification (P1-P9, O3, S3)

Nanolab Tool: tystar3
Options: tystar2, tystar4
Recipe: 3HIN2ANA
Temperature: 950°C
Time: 01:00:00
Process Note: Unannealed phospho-silicate glass (PSG) sometimes bubbles at high temperatures. So, annealing immediately after the deposition prevents this from happening at later stages in the process.

89. Metrology: Oxide hard mask thickness measurement (S3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Expected: 2µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

90. PR Coating: Polysilicon structural layer photoresist [P3CF] (P1-P9, O3, S3)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 900nm
Recipe: T1_UV210-0.6_0.87um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

91. PR Exposure: Polysilicon structural layer photoresist [P3CF] (P1-P9, O3, S3)

Nanolab Tool: asml300
Options: None
ASML Job: DISKRUN_R1
Reticle: DISKRUN_R1
Field: P3CF - BOTTOMRIGHT
Exposure: 16mJ
Focus: 0nm

92. PR Development: Polysilicon structural layer photoresist [P3CF] (P1-P9, O3, S3)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Twice
Process Note: Always run at least one dummy wafer first and visually check the developer uniformity.

93. PR Descum: Polysilicon structural layer photoresist [P3CF] (P1-P9, O3, S3)

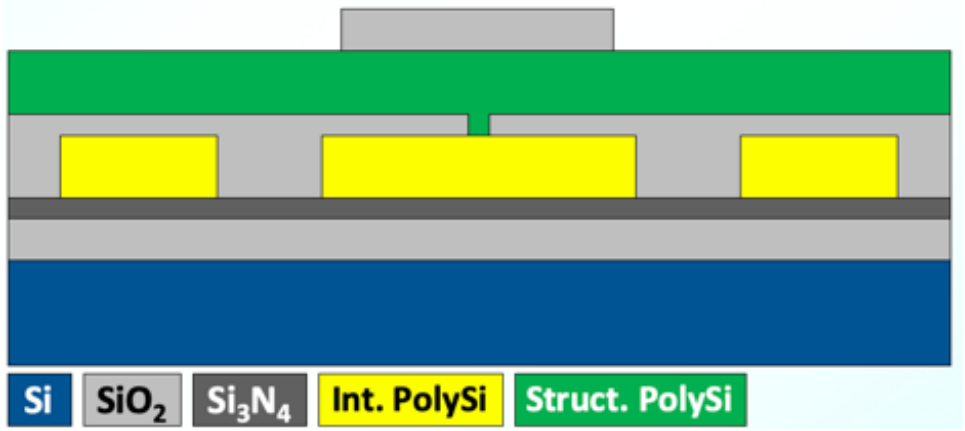
Nanolab Tool: technics-c
Options: None
Gas Flows: O_2 = 180sccm
Power: 30W
Time: 00:00:15
Process Note: 'technics-c' etch rates wildly changes from time to time. Take the numbers in the manual as a reference and make sure to test the current etch rate especially if there are designs with feature size less than 500nm and precise width control is critical.

94. PR UV-bake: Polysilicon structural layer photoresist [P3CF] (P1-P9, O3, S3)

Nanolab Tool: axcelis
Options: None
Program: U

95. Etch: Polysilicon structural layer hard mask [P3CF] (P1-P9, O3, S3)

Nanolab Tool: lam6
Options: sts-oxide
Recipe Name: 6001_OXIDE_ME
Gas Flows: Ar = 150sccm, CHF_3 = 25sccm, CF_4 = 25sccm
Pressure: 70mTorr
Gap: 1.3cm
Power: 500W
Etch Rate: 717nm/min (for P3CF mask)
Selectivity: UV210 Photoresist (UV-baked) : Annealed PSG = 1 : 4.10
Etch Time: 3min (3 cycles of [1min SiO_2 etch + 1min rest] to prevent PR from burning)
Process Note-1: Note that 'lam6' burns UV210 resist if the etch time is longer than 1min. To prevent this from happening, the process wafer should rest for 1min in the etch chamber with the RF power turned off after 1min etch.
Process Note-2: Make sure to run 3 dummies with the oxygen clean recipe and also check the current etch rate and selectivity with the test wafer 'S3' by doing a 1min etch beforehand. This will also condition the chamber.
Process Note-3: 10% overetch is included.
Cross Section:



96. PR Strip: Polysilicon structural layer photoresist [P3CF] (P1-P9, O3, S3)

Nanolab Tool: matrix
Options: technics-c, msink1-1165, msink16 & msink18-PRS3000
Pressure: 3.75Torr
Temperature: 250°C
Power: 400W
Time: 00:02:30
Process Note: Run the recipe twice.

97. Metrology: Oxide hard mask step height measurement (P1-P9, O3, S3)

Nanolab Tool: alphastep
Options: nanoduv, ellips1, ellips2
Meas. Range: 10µm
Expected: 2µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

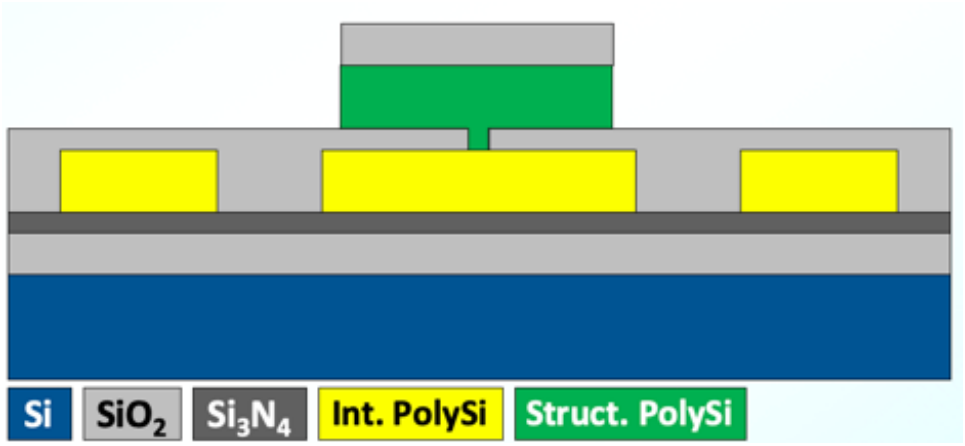
98. Post-Etch Cleaning: Oxide hard mask (P1-P9, O3, S3)

Nanolab Tool: msink8
Options: msink7
1st Chemical: Piranha at 120°C
Temperature: 120°C
Time: 00:10:00
Process Note: Note that PR must be completely removed and cleaned before the following HBr-based polysilicon etch. Otherwise, any PR present on the wafer leaves some organic residue during the HBr-based polysilicon etch.

99. Etch: Polysilicon structural layer [P3CF] (P1-P9, O3)

Nanolab Tool: lam8
Options: None
Recipe Name: 8001_POLY_ME
Gas Flows: HBr = 150sccm, Cl_2 = 4sccm, O_2 = 1sccm
Pressure: 12mTorr
Gap: 6.03cm
TCP RF: 250W
Bias RF: 55W
Etch Rate: 172.9nm/min (for P3CF mask)
Selectivity: SiO_2 : Polysilicon = 1 : (>10)
Etch Time: 22min (11 cycles of [2min Polysilicon etch + 1min rest] to prevent wafer from over-heating)
Process Note-1: Note that 'lam8' overheats the wafer if the etch time is longer than 2min. To prevent this from happening, the process wafer should rest for 1min in the etch chamber with the TCP RF and bias RF powers turned off after 2min etch.
Process Note-2: Make sure to check the current etch rate and selectivity with the test wafer 'O3' by doing a 1min etch beforehand. Don't forget to complete the structural layer etch for 'O3' later on. This will also condition the chamber.

Process Note-3: 30% overetch is included.
Cross Section:



100. Metrology: Polysilicon structural layer conductivity check after etching (P1-P9, O3)
Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance on the layout where polysilicon has been removed in the previous etch step. If the etch is complete, this measurement should indicate infinite resistance ('open')

101. Metrology: Polysilicon structural layer and oxide hard mask step height measurement (P1-P9, O3)
Nanolab Tool: alphastep
Options: nanoduv, ellips1, ellips2
Meas. Range: 50µm
Expected: 5µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

102. Metrology: Wafer bow measurement (P1-P9, O3)
Nanolab Tool: flexus
Options: None
Program: Ozgurluk/BaseSi.dat
Target: < 20µm
Result: ____
Process Note: If not, etch the back side using the same tool as the front side has been etched until the target is met. Note that the maximum allowable wafer bow for asml300 is 50µm.

103. Pre-Deposition Cleaning: Sidewall sacrificial oxide layer (P1-P9, O3, S11-S19, TS11-TS19)
Nanolab Tool: msink8
Options: msink7

Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink8
Options: msink7
1st Chemical: 50:1 HF
Temperature: 120°C
Etch Rate: 3nm/sec (HTO)
Time: 00:00:03
Process Note-1: Include bare Si test wafers ('S11' –'S19') for the subsequent oxide deposition steps.
Process Note-2: Make your own 50:1 HF in msink8 ambient bath mixing 16L water and 320mL 49% HF. Use this bath to do native oxide removal right before the following deposition.
Process Note-3: It is important to quickly transfer wafers to the furnace after this step to prevent any native oxide formation in the stem opening.

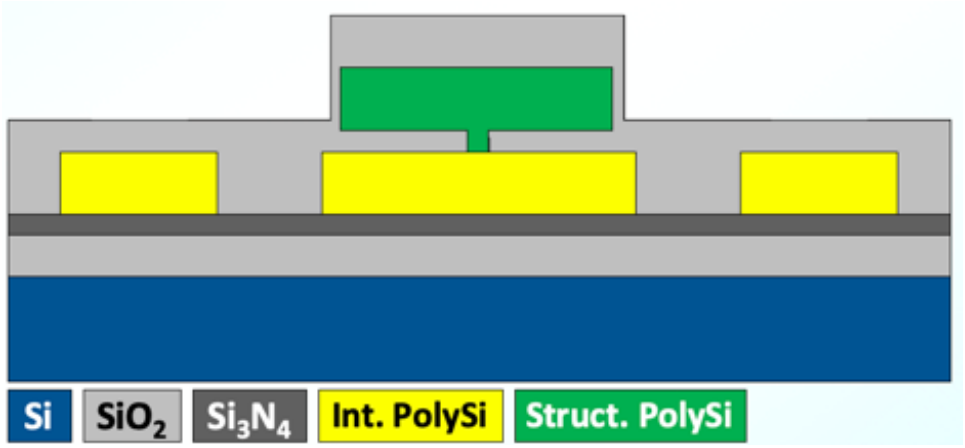
---------- Start: Sidewall Sacrificial Layer: 80nm HTO ----------

104. Test Deposition: Sidewall sacrificial high temperature oxide (HTO→80nm) (TS11)
Nanolab Tool: tystar17
Options: tystar9
Recipe: HTOFVAR.017
Gas Flows: N_2O = 30sccm, DCS = 10sccm
Pressure: 200mTorr
Temperature: 930°C
Time: 01:20:00
Process Note: Use a bare silicon wafer ('TS11') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

105. Test Metrology: Sidewall sacrificial high temperature oxide (HTO→80nm) (TS11)
Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

106. Deposition: Sidewall sacrificial high temperature oxide (HTO→80nm) (P1, O3, S11)

Nanolab Tool: tystar17
Options: tystar9
Recipe: HTOSTDA.017
Gas Flows: N_2O = 30sccm, DCS = 10sccm
Pressure: 200mTorr
Temperature: 930°C
Dep. Rate: 1.02nm/min – front 6" boat middle slot (adjust if needed)
Time: 01:20:00 (adjust if needed)
Goal: 80nm
Process Note: Use a bare silicon wafer ('S11') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



107. Metrology: Sidewall sacrificial high temperature oxide (HTO→80nm) thickness measurement (S11)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 80nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: Sidewall Sacrificial Layer: 80nm HTO ----------

---------- Start: Sidewall Sacrificial Layer: 40nm HTO ----------

108. Test Deposition: Sidewall sacrificial high temperature oxide (HTO→40nm) (TS13)

Nanolab Tool: tystar17
Options: tystar9
Recipe: HTOFVAR.017
Gas Flows: N_2O = 30sccm, DCS = 10sccm
Pressure: 200mTorr
Temperature: 930°C
Time: 00:40:00

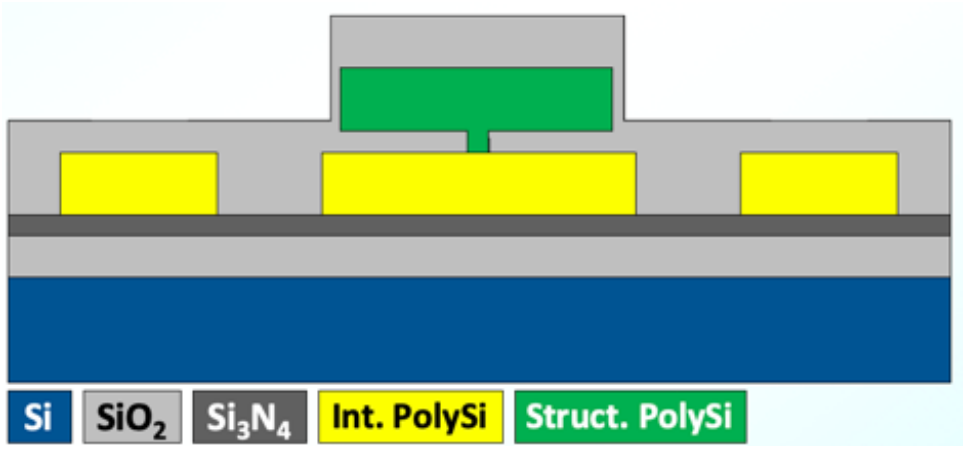
Process Note: Use a bare silicon wafer ('TS13') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

109. Test Metrology: Sidewall sacrificial high temperature oxide (HTO→40nm) (TS13)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

110. Deposition: Sidewall sacrificial high temperature oxide (HTO→40nm) (P3, S13)

Nanolab Tool: tystar17
Options: tystar9
Recipe: HTOSTDA.017
Gas Flows: N_2O = 30sccm, DCS = 10sccm
Pressure: 200mTorr
Temperature: 930°C
Dep. Rate: 1.02nm/min – front 6" boat middle slot (adjust if needed)
Time: 00:40:00 (adjust if needed)
Goal: 40nm
Process Note: Use a bare silicon wafer ('S13') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



111. Metrology: Sidewall sacrificial high temperature oxide (HTO→40nm) thickness measurement (S13)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 40nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: Sidewall Sacrificial Layer: 40nm HTO ----------

---------- Start: Sidewall Sacrificial Layer: 20nm HTO ----------

112. Test Deposition: Sidewall sacrificial high temperature oxide (HTO→20nm) (TS12)

Nanolab Tool: tystar17
Options: tystar9
Recipe: HTOFVAR.017
Gas Flows: N_2O = 30sccm, DCS = 10sccm
Pressure: 200mTorr
Temperature: 930°C
Time: 00:20:00
Process Note: Use a bare silicon wafer ('TS12') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

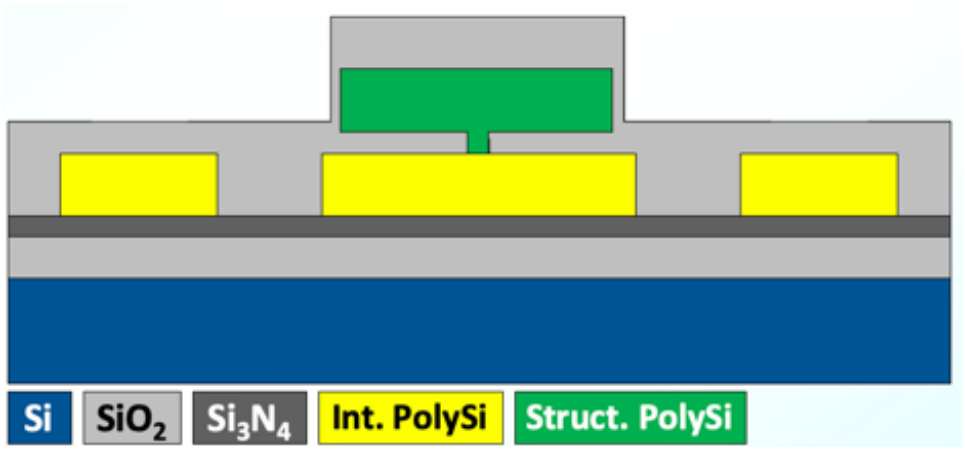
113. Test Metrology: Sidewall sacrificial high temperature oxide (HTO→20nm) (TS12)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)

Thickness:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Dep. Rate:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____

114. Deposition: Sidewall sacrificial high temperature oxide (HTO→20nm) (P2, S12)

Nanolab Tool: tystar17
Options: tystar9
Recipe: HTOSTDA.017
Gas Flows: N_2O = 30sccm, DCS = 10sccm
Pressure: 200mTorr
Temperature: 930°C
Dep. Rate: 1.02nm/min – front 6" boat middle slot (adjust if needed)
Time: 00:20:00 (adjust if needed)
Goal: 20nm
Process Note: Use a bare silicon wafer ('S12') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



115. Metrology: Sidewall sacrificial high temperature oxide (HTO→20nm) thickness measurement (S12)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 20nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: Sidewall Sacrificial Layer: 20nm HTO ----------

---------- Start: Sidewall Sacrificial Layer: 10nm HTO ----------

116. Test Deposition: Sidewall sacrificial high temperature oxide (HTO→10nm) (TS16)

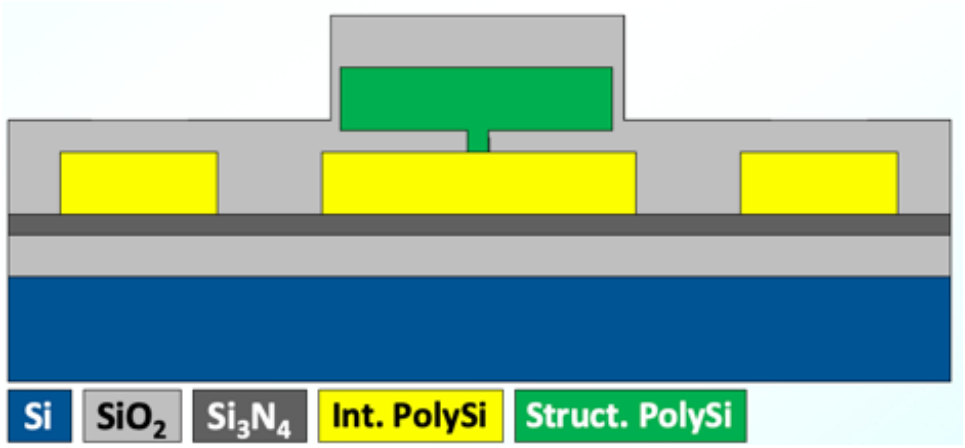
Nanolab Tool: tystar17
Options: tystar9
Recipe: HTOFVAR.017
Gas Flows: N_2O = 30sccm, DCS = 10sccm
Pressure: 100mTorr
Temperature: 930°C
Time: 00:48:00
Process Note: Use a bare silicon wafer ('TS16') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

117. Test Metrology: Sidewall sacrificial high temperature oxide (HTO→10nm) (TS16)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

118. Deposition: Sidewall sacrificial high temperature oxide (HTO→10nm) (P6, S16)

Nanolab Tool: tystar17
Options: tystar9
Recipe: HTOSTDA.017
Gas Flows: N_2O = 30sccm, DCS = 10sccm
Pressure: 100mTorr
Temperature: 930°C
Dep. Rate: 0.21nm/min – front 6" boat middle slot (adjust if needed)
Time: 00:48:00 (adjust if needed)
Goal: 10nm
Process Note: Use a bare silicon wafer ('S16') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



119. Metrology: Sidewall sacrificial high temperature oxide (HTO→10nm) thickness measurement (S16)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 10nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: Sidewall Sacrificial Layer: 10nm HTO ----------

---------- Start: Sidewall Sacrificial Layer: 10nm ALD ----------

120. Test Deposition: Sidewall sacrificial atomic layer deposition oxide (ALD→10nm) (TS14)

Nanolab Tool: cambridge
Options: None
Recipe: Plasma_SiO2
Precursor: TDMAS
Temperature: 200°C
Cycle: 162

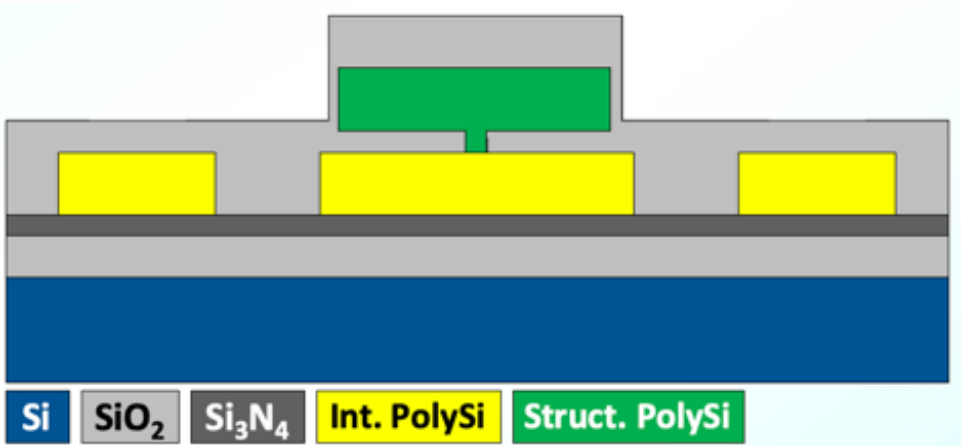
Process Note: Use a bare silicon wafer ('TS14') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

121. Test Metrology: Sidewall sacrificial atomic layer deposition oxide (ALD→10nm) (TS14)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Note that for oxides thinner than 20nm, 'nanospec' measurement usually gives erroneous results. It's better to use 'ellips2' to obtain reliable and consistent results in this thickness range.

122. Deposition: Sidewall sacrificial atomic layer deposition oxide (ALD→10nm) (P4, S14)

Nanolab Tool: cambridge
Options: None
Recipe: Plasma_SiO2
Precursor: TDMAS
Temperature: 200°C
Dep. Rate: 0.062nm/cycle (adjust if needed)
Cycle: 162 (adjust if needed)
Goal: 10nm
Process Note: Use a bare silicon wafer ('S14') pieces placed around the process wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



123. Metrology: Sidewall sacrificial atomic layer deposition oxide (ALD→10nm) thickness measurement (S14)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)

Expected: 10nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Note that for oxides thinner than 20nm, 'nanospec' measurement usually gives erroneous results. It's better to use 'ellips2' to obtain reliable and consistent results in this thickness range.

---------- End: Sidewall Sacrificial Layer: 10nm ALD ----------

---------- Start: Sidewall Sacrificial Layer: 5nm ALD ----------

124. Test Deposition: Sidewall sacrificial atomic layer deposition oxide (ALD→5nm) (TS15)

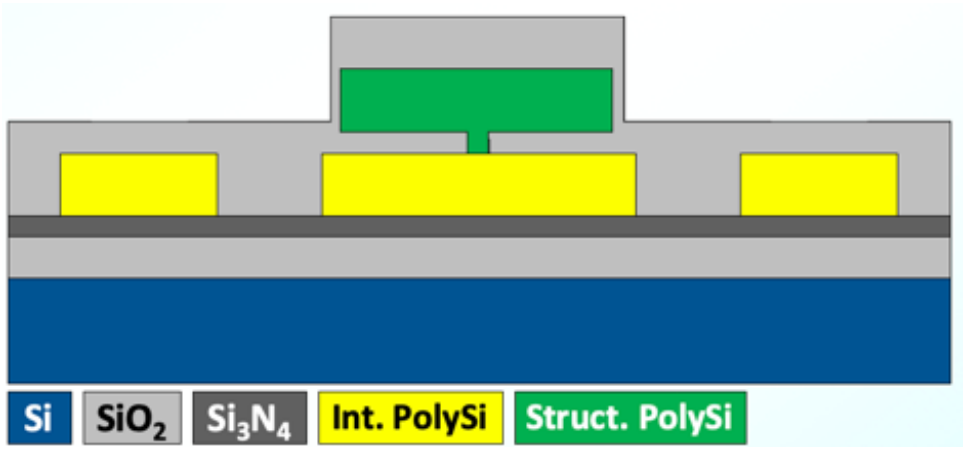
Nanolab Tool: cambridge
Options: None
Recipe: Plasma_SiO2
Precursor: TDMAS
Temperature: 200°C
Cycle: 81
Process Note: Use a bare silicon wafer ('TS15') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

125. Test Metrology: Sidewall sacrificial atomic layer deposition oxide (ALD→5nm) (TS15)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Note that for oxides thinner than 20nm, 'nanospec' measurement usually gives erroneous results. It's better to use 'ellips2' to obtain reliable and consistent results in this thickness range.

126. Deposition: Sidewall sacrificial atomic layer deposition oxide (ALD→5nm) (P5, S15)

Nanolab Tool: cambridge
Options: None
Recipe: Plasma_SiO2
Precursor: TDMAS
Temperature: 200°C
Dep. Rate: 0.062nm/cycle (adjust if needed)
Cycle: 81 (adjust if needed)
Goal: 5nm
Process Note: Use a bare silicon wafer ('S15') pieces placed around the process wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



127. Metrology: Sidewall sacrificial atomic layer deposition oxide (ALD→5nm) thickness measurement (S15)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 5nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Note that for oxides thinner than 20nm, 'nanospec' measurement usually gives erroneous results. It's better to use 'ellips2' to obtain reliable and consistent results in this thickness range.

---------- End: Sidewall Sacrificial Layer: 5nm ALD ----------

---------- Start: Sidewall Sacrificial Layer: 4nm ALD ----------

128. Test Deposition: Sidewall sacrificial atomic layer deposition oxide (ALD→4nm) (TS18)

Nanolab Tool: cambridge
Options: None
Recipe: Plasma_SiO2
Precursor: TDMAS
Temperature: 200°C
Cycle: 64
Process Note: Use a bare silicon wafer ('TS18') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

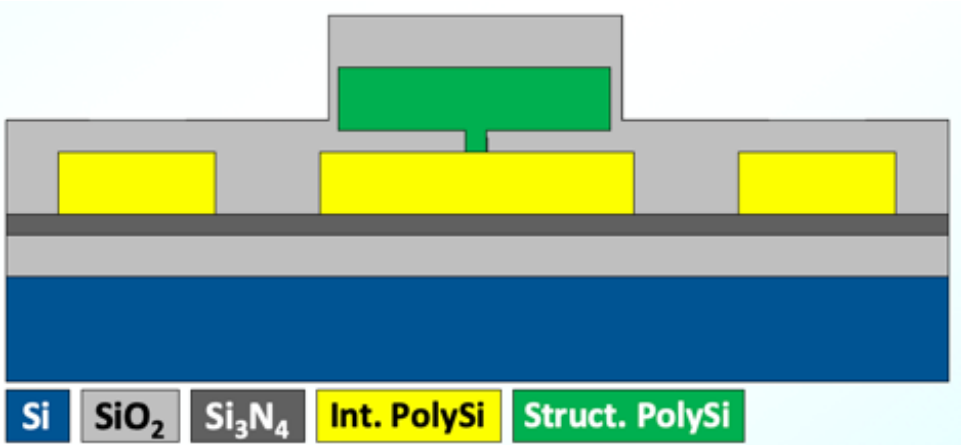
129. Test Metrology: Sidewall sacrificial atomic layer deposition oxide (ALD→4nm) (TS18)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

Process Note: Note that for oxides thinner than 20nm, 'nanospec' measurement usually gives erroneous results. It's better to use 'ellips2' to obtain reliable and consistent results in this thickness range.

130. Deposition: Sidewall sacrificial atomic layer deposition oxide (ALD→4nm) (P8, S18)

Nanolab Tool: cambridge
Options: None
Recipe: Plasma_SiO2
Precursor: TDMAS
Temperature: 200°C
Dep. Rate: 0.062nm/cycle (adjust if needed)
Cycle: 64 (adjust if needed)
Goal: 4nm
Process Note: Use a bare silicon wafer ('S18') pieces placed around the process wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



131. Metrology: Sidewall sacrificial atomic layer deposition oxide (ALD→4nm) thickness measurement (S18)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 4nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Note that for oxides thinner than 20nm, 'nanospec' measurement usually gives erroneous results. It's better to use 'ellips2' to obtain reliable and consistent results in this thickness range.

---------- End: Sidewall Sacrificial Layer: 4nm ALD ----------

---------- Start: Sidewall Sacrificial Layer: 2nm ALD ----------

132. Test Deposition: Sidewall sacrificial atomic layer deposition oxide (ALD→2nm) (TS19)

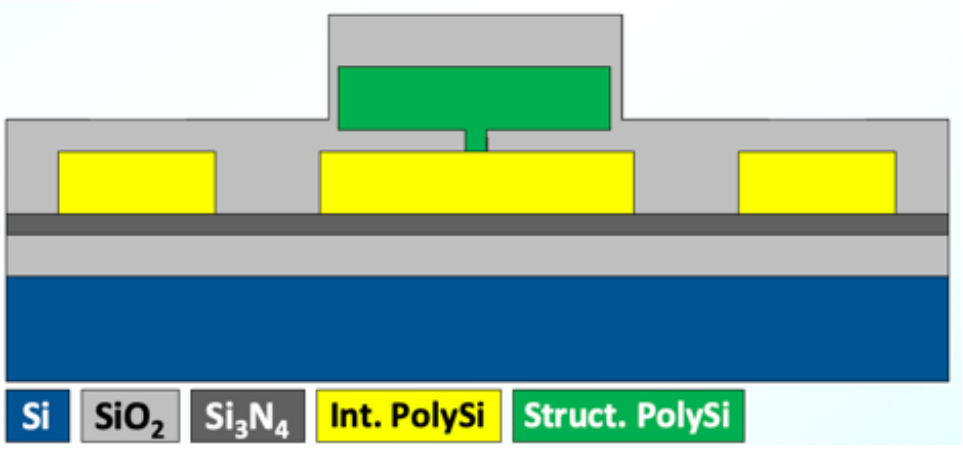
Nanolab Tool: cambridge
Options: None
Recipe: Plasma_SiO2
Precursor: TDMAS
Temperature: 200°C
Cycle: 32
Process Note: Use a bare silicon wafer ('TS19') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

133. Test Metrology: Sidewall sacrificial atomic layer deposition oxide (ALD→2nm) (TS19)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Note that for oxides thinner than 20nm, 'nanospec' measurement usually gives erroneous results. It's better to use 'ellips2' to obtain reliable and consistent results in this thickness range.

134. Deposition: Sidewall sacrificial atomic layer deposition oxide (ALD→2nm) (P9, S19)

Nanolab Tool: cambridge
Options: None
Recipe: Plasma_SiO2
Precursor: TDMAS
Temperature: 200°C
Dep. Rate: 0.062nm/cycle (adjust if needed)
Cycle: 32 (adjust if needed)
Goal: 2nm
Process Note: Use a bare silicon wafer ('S19') pieces placed around the process wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



135. Metrology: Sidewall sacrificial atomic layer deposition oxide (ALD→2nm) thickness measurement (S19)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 2nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Note that for oxides thinner than 20nm, 'nanospec' measurement usually gives erroneous results. It's better to use 'ellips2' to obtain reliable and consistent results in this thickness range.

---------- End: Sidewall Sacrificial Layer:2nm ALD ----------

---------- Start: Sidewall Sacrificial Layer: 1nm ALD ----------

136. Test Deposition: Sidewall sacrificial atomic layer deposition oxide (ALD→1nm) (TS17)

Nanolab Tool: cambridge
Options: None
Recipe: Plasma_SiO2
Precursor: TDMAS
Temperature: 200°C
Cycle: 16
Process Note: Use a bare silicon wafer ('TS17') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

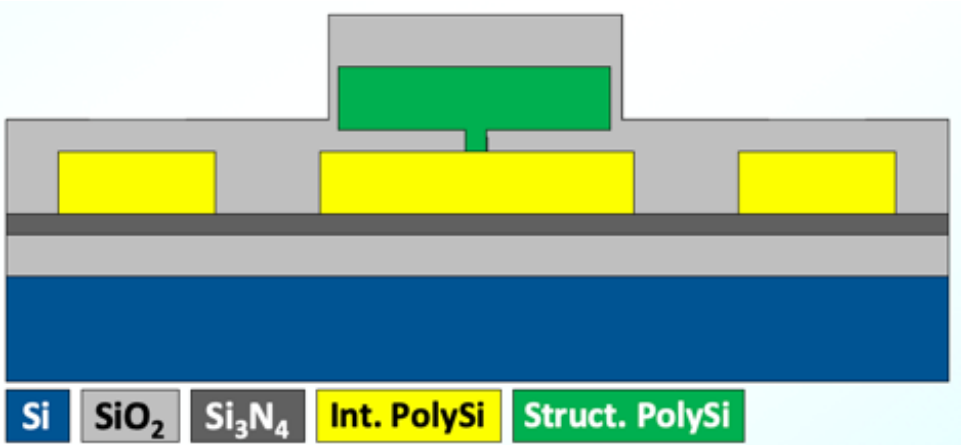
137. Test Metrology: Sidewall sacrificial atomic layer deposition oxide (ALD→1nm) (TS17)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Note that for oxides thinner than 20nm, 'nanospec' measurement usually gives erroneous results. It's better to use 'ellips2' to obtain reliable and consistent results in this thickness range.

138. Deposition: Sidewall sacrificial atomic layer deposition oxide (ALD→1nm) (P7, S17)

Nanolab Tool: cambridge
Options: None
Recipe: Plasma_SiO2
Precursor: TDMAS
Temperature: 200°C
Dep. Rate: 0.062nm/cycle (adjust if needed)
Cycle: 16 (adjust if needed)

Goal: 1nm
Process Note: Use a bare silicon wafer ('S17') pieces placed around the process wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



139. Metrology: Sidewall sacrificial atomic layer deposition oxide (ALD→1nm) thickness measurement (S17)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 1nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Note that for oxides thinner than 20nm, 'nanospec' measurement usually gives erroneous results. It's better to use 'ellips2' to obtain reliable and consistent results in this thickness range.

---------- End: Sidewall Sacrificial Layer: 1nm ALD ----------

140. PR Coating: Anchor layer photoresist [P4DF] (P1-P9, O3)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV26
Thickness: 2.2µm
Recipe: T1_UV26-3.0_2.2um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 110°C (Post)
Process Note-1: Always run at least one dummy wafer first and visually check the resist uniformity.
Process Note-2: Note that due to the 3-4µm topography present at this step, a thicker PR is needed to completely cover the wafer. After coating, make sure the wafer is fully covered with PR. If not, use even thicker PR.

141. PR Exposure: Anchor layer photoresist [P4DF] (P1-P9, O3)

Nanolab Tool: asml300
Options: None

ASML Job: DISKRUN_R1
Reticle: DISKRUN_R1
Field: P4DF - BOTTOMLEFT
Exposure: 50mJ
Focus: 3.50µm
Process Note: A very high exposure and change in the focus setting is needed due to thicker PR. Do a focus-exposure matrix (FEM) if needed.

142. PR Development: Anchor layer photoresist [P4DF] (P1-P9, O3)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PROX110C60s_MF26A60s
Temperature: Prox. (0.6mm) 60sec @ 110°C
Dev. Count: Twice
Process Note-1: Always run at least one dummy wafer first and visually check the developer uniformity.
Process Note-2: Develop twice for dark field masks to make sure all residual photoresist in the patterned area gets removed.

143. PR Descum: Anchor layer photoresist [P4DF] (P1-P9, O3)

Nanolab Tool: technics-c
Options: None
Gas Flows: O_2 = 180sccm
Power: 30W
Time: 00:00:30
Process Note: 'technics-c' etch rates wildly changes from time to time. Take the numbers in the manual as a reference and make sure to test the current etch rate especially if there are designs with feature size less than 500nm and precise width control is critical.

144. Metrology: Anchor layer photoresist before hard bake [P4DF] (P1-P9, O3)

Nanolab Tool: alphastep
Options: nanoduv, ellips1, ellips2
Meas. Range: 10µm
Expected: 2-3µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

145. PR Hard-bake: Anchor layer photoresist [P4DF] (P1-P9, O3)

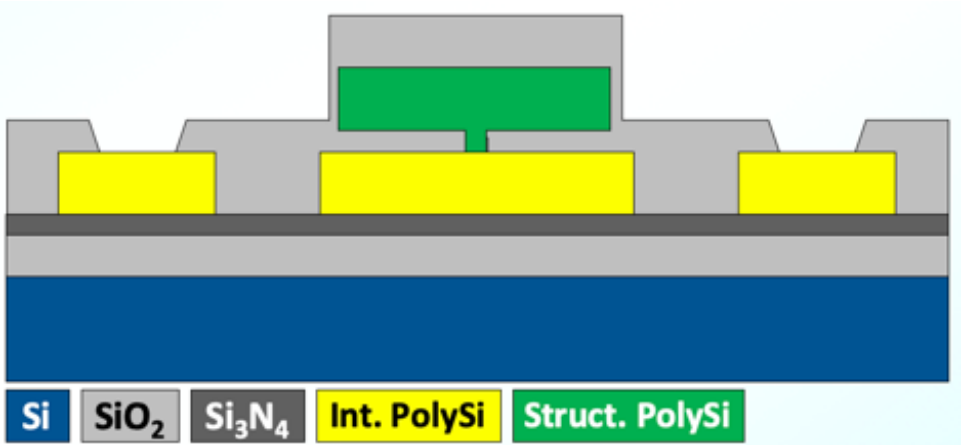
Nanolab Tool: oven
Options: None
Temperature: 120°C
Time: 12:00:00
Process Note: UV-bake or hot plate-based hard bake destroys thick UV26 photoresist. So, the only option here is to do a long oven bake.

146. Metrology: Anchor layer photoresist after hard bake [P4DF] (P1-P9, O3)

Nanolab Tool: alphastep
Options: nanoduv, ellips1, ellips2
Meas. Range: 10µm
Expected: 2-3µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

147. Etch: Anchor layer [P4DF] (P1-P9, O3)

Nanolab Tool: lam6
Options: sts-oxide
Recipe Name: 6001_OXIDE_ME
Gas Flows: Ar = 150sccm, CHF_3 = 25sccm, CF_4 = 25sccm
Pressure: 70mTorr
Gap: 1.3cm
Power: 500W
Etch Rate: 717nm/min (for P3CF mask)
Selectivity: UV26 Photoresist (oven baked) : Annealed PSG = 1 : 2
Etch Time: 2min (2 cycles of [1min SiO_2 etch + 1min rest] to prevent PR from burning)
Process Note-1: Note that 'lam6' burns UV26 resist if the etch time is longer than 1min. To prevent this from happening, the process wafer should rest for 1min in the etch chamber with the RF power turned off after 1min etch.
Process Note-2: Make sure to run 3 dummies with the oxygen clean recipe and also check the current etch rate and selectivity with the test wafer 'O3' by doing a 30sec etch beforehand. Complete the 'O3' etch by doing another 1min and 30sec additional etch. This will also condition the chamber.
Process Note-3: 100% over etch is included. Be careful with excessive lateral etch.
Cross Section:



148. PR Strip: Anchor layer photoresist [P4DF] (P1-P9, O3)

Nanolab Tool: matrix
Options: technics-c, msink1-1165, msink16 & msink18-PRS3000
Pressure: 3.75Torr
Temperature: 250°C
Power: 400W

Time: 00:02:30
Process Note: Run the recipe twice.

149. Metrology: Anchor layer step height measurement (P1-P9, O3)
Nanolab Tool: alphastep
Options: nanoduv, ellips1, ellips2
Meas. Range: 5µm
Expected: 500nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Use the patterns in the diagnostics layout to make this measurement.

150. Pre-Deposition Cleaning: Polysilicon electrode layer – 1st pass (P1-P9, O3, O4, TO4)
Nanolab Tool: msink8
Options: msink7
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None
1st Chemical: Piranha at 120°C *2nd Chemical:* 25:1 HF
Temperature: 120°C *Temperature:* Room temperature
Time: 00:10:00 *Time:* 00:00:05
Process Note-1: Include a thin oxide dummy test wafer ('O4') for the subsequent polysilicon deposition step.
Process Note-2: Make sure to test the 25:1 HF etch rate first with a dummy wafer. It is always better to take the posted etch rates and chemical ratios as a reference but not to fully trust them in a university lab.

151. Test Deposition: Polysilicon electrode layer – 1st pass (TO4)
Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Time: 01:00:00
Process Note: Use a thin oxide dummy wafer ('TO4') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

152. Test Metrology: Polysilicon electrode layer – 1st pass (TO4)
Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

153. Deposition: Polysilicon electrode layer – 1st pass (P1-P9, O3, O4)

Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Dep. Rate: 6.25nm/min (adjust if needed)
Time: 01:20:00 (adjust if needed)
Goal: 500nm
Process Note: Use a thin oxide dummy wafer ('O4') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

154. $POCl_3$ Doping: Polysilicon electrode layer – 1st pass (P1-P9, O3, O4)

Nanolab Tool: tystar6
Options: tystar13, tystar11/tystar12 (dope) + tystar2/tystar3/tystar4 (drive-in)
Recipe: PCLO2.006
Gas Flows: N_2 = 200sccm, O_2 = 300sccm
Doping Temperature: 950°C
Doping Time: 01:00:00
Drive-in Temperature: 950°C
Drive-in Time: 02:00:00
Process Note: Place the wafers in every other slot to make sure the heat distribution stays uniform during doping and drive-in.

155. $POCl_3$ Doping: PSG removal and cleaning (P1-P9, O3, O4)

Nanolab Tool: msink8

1st Chemical:	10:1 HF	*2nd Chemical:*	Piranha
Temperature:	Room temperature	*Temperature:*	120°C
Time:	00:10:00	*Time:*	00:10:00

Process Note: This phospho-silicate glass (PSG) layer forms during $POCL_3$ doping and must be removed afterwards. Its thickness is usually around 100-200nm. Note that after $POCL_3$ doping and PSG removal, polysilicon surface becomes extremely rough.

156. Metrology: Polysilicon electrode layer sheet resistance measurement – 1st pass (O4)

Nanolab Tool: cde-resmap
Options: None
Program: 5 point
Expected: 3-4Ω/□
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

157. Pre-Deposition Cleaning: Polysilicon electrode layer – 2nd pass (P1-P9, O3, O4, O5, TO5)

Nanolab Tool: msink8
Options: msink7
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

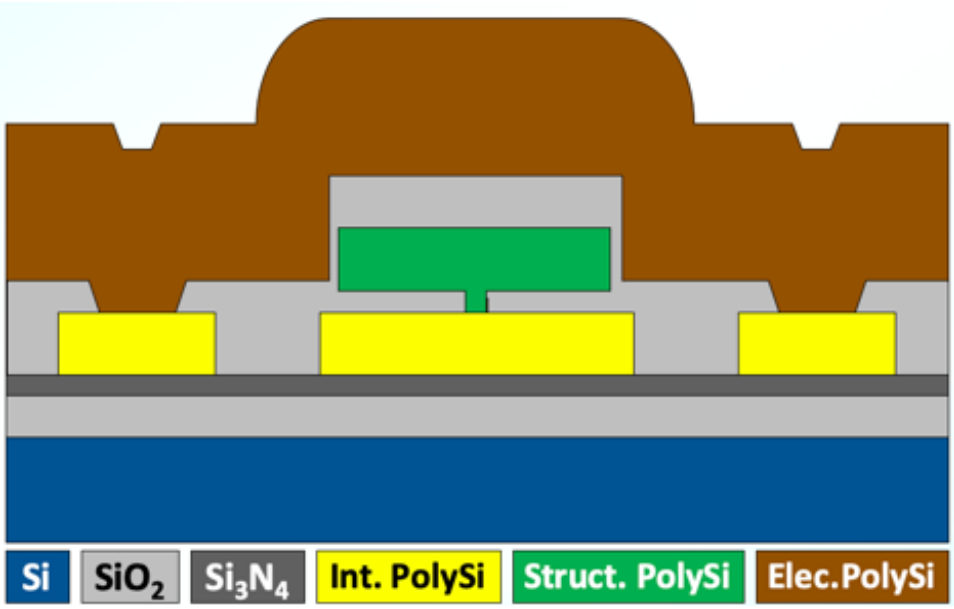
Nanolab Tool: msink6
Options: None
1st Chemical: Piranha at 120°C *2nd Chemical:* 25:1 HF
Temperature: 120°C *Temperature:* Room temperature
Time: 00:10:00 *Time:* 00:02:00
Process Note-1: Include a thin oxide dummy test wafer ('O5') for the subsequent polysilicon deposition step.
Process Note-2: Make sure to test the 25:1 HF etch rate first with a dummy wafer. It is always better to take the posted etch rates and chemical ratios as a reference but not to fully trust them in a university lab.
Process Note-4: After HF dip, make sure to quickly transfer the wafers to the furnace for the interconnect layer deposition.

158. Test Deposition: Polysilicon electrode layer – 2nd pass (TO5)
Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Time: 01:00:00
Process Note: Use a thin oxide dummy wafer ('TO5') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

159. Test Metrology: Polysilicon electrode layer – 2nd pass (TO5)
Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

160. Deposition: Polysilicon electrode layer – 2nd pass (P1-P9, O3, O4, O5)
Nanolab Tool: tystar16
Options: tystar10
Recipe: 16SUPLYA
Gas Flows: SiH_4 = 120sccm, PH_3HI = 0sccm, PH_3LO = 0sccm
Pressure: 375mTorr
Temperature: 590°C
Dep. Rate: 6.25nm/min (adjust if needed)

Time: 01:20:00 (adjust if needed)
Goal: 500nm
Process Note: Use a thin oxide dummy wafer ('O5') as a test wafer for the following thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.
Cross Section:



161. $POCl_3$ Doping: Polysilicon electrode layer – 2nd pass (P1-P9, O3, O4, O5)

Nanolab Tool: tystar6
Options: tystar13, tystar11/tystar12 (dope) + tystar2/tystar3/tystar4 (drive-in)
Recipe: PCLO2.006
Gas Flows: N_2 = 200sccm, O_2 = 300sccm
Doping Temperature: 1050°C
Doping Time: 01:00:00
Drive-in Temperature: 1050°C
Drive-in Time: 02:00:00
Process Note: Place the wafers in every other slot to make sure the heat distribution stays uniform during doping and drive-in.

162. $POCl_3$ Doping: PSG removal and cleaning (P1-P9, O3, O4, O5)

Nanolab Tool: msink8

1st Chemical:	10:1 HF	*2nd Chemical:*	Piranha
Temperature:	Room temperature	*Temperature:*	120°C
Time:	00:10:00	*Time:*	00:10:00

Process Note: This phospho-silicate glass (PSG) layer forms during $POCL_3$ doping and must be removed afterwards. Its thickness is usually around 100-200nm. Note that after $POCL_3$ doping and PSG removal, polysilicon surface becomes extremely rough.

163. Metrology: Polysilicon interconnect layer thickness measurement – 2nd pass (O4, O5)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Polysilicon on Thin Oxide (10x)
Expected: 3µm
Result ('O4'): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result ('O5'): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note-1: Use the thin oxide dummy ('O5') obtained in the previous step for polysilicon thickness measurement. 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

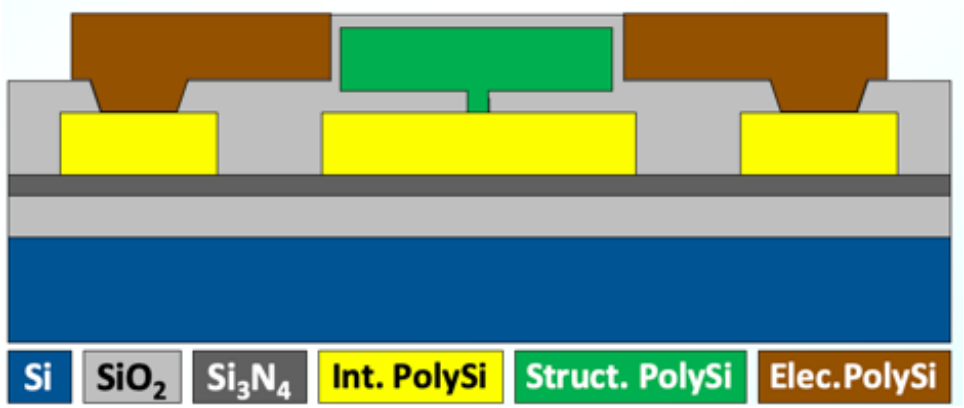
Process Note-2: Since the polysilicon surface becomes extremely rough after $POCL_3$ doping and PSG removal, optical thin film measurement might fail. In this case, a very short chemical mechanical polishing (CMP) might be necessary to polish the surface.

164. Chemical Mechanical Polishing: Polysilicon interconnect layer (P1-P9, O3, CS6)

Nanolab Tool: cmp
Options: None
Recipe: Poly.polish
Down Force: 8psi
Back Pres.: 6psi
Table RPM: 24
Chuck RPM: 6
Slurry Name: Cabot iDiel D3543
Slurry Flow: 100ml/min
Etch Rate: 140nm/min
Time: Front Side → 2min x 4 with 90° wafer rotation, pad conditioning
Back Side → 2min x 4 with 90° wafer rotation, pad conditioning
Front Side → 1min x 4 with 90° wafer rotation, pad conditioning
Process Note-1: Note that the provided etch rate is for a flat LPCVD polysilicon layer. Make sure to check the current removal rate using the test wafer ('CS6'). This etch rate considerably enhances in the presence of topography as the effective pressure increases.
Process Note-2: As the etch rate is topography dependent, it is important to visually check the wafer both with naked eye and under a microscope after each CMP cycle to make sure 'cmp' does not start removing the underlying oxide mold layer excessively.
Process Note-3: 'cmp' tool is uniform when removing thin layers but it is not uniform for removing layers thicker than 1µm. The purpose of rotating wafer by 90° every minute is to enhance the uniformity over the wafer surface.
Process Note-4: The purpose of back side cmp is to correct the wafer bow so that edge-to-center CMP uniformity does not degrade during polishing.
Process Note-5: Make sure to run a bare Si dummy wafer ('CS6') and a patterned test wafer ('O3') to check for scratches before processing the process wafers. Major scratches are usually visible on a bare Si wafer ('CS6'). However, a patterned wafer ('O3') is necessary to see minor scratches under a microscope.

Process Note-6: Note that the front side CMP should continue until all SiO_2 hard mask layer patterns expose.

Cross Section:



165. Post-CMP cleaning: Polysilicon interconnect layer (P1-P9, O3, CS6)

Nanolab Tool: sinkcmp
Options: None
Chemical: Water
Process Note: Clean the wafer front and back side with PVD sponge four times for 15sec with 90° wafer rotation each time, then follow with four full QDR cycles at sinkcmp.

Nanolab Tool: msink8
Options: msink16, msink18
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
Process Note: Transfer wafers from Cory 190 to the Nanolab immediately in a box filled with water and start piranha cleaning. It is extremely important that the wafers never dry out with cmp silica particles on them.

166. Metrology: Wafer bow measurement (P1-P9, O3)

Nanolab Tool: flexus
Options: None
Program: Ozgurluk/BaseSi.dat
Target: < 20µm
Result: ____
Process Note: If not, etch the back side using 'sts2' or 'lam8' until the target is met. Note that the maximum allowable wafer bow for asml300 is 50µm.

167. Metrology: Polysilicon electrode layer (P1-P9, O3)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

Process Note: This check entails measuring the electrical resistance measured on top of the hard mask patterns. If the polysilicon removal is complete, this measurement should indicate infinite resistance ('open').

168. PR Coating: Polysilicon electrode layer photoresist [P5CF] (P1-P9, O3)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 900nm
Recipe: T1_UV210-0.6_0.87um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

169. PR Exposure: Polysilicon electrode layer photoresist [P5CF] (P1-P9, O3)

Nanolab Tool: asml300
Options: None
ASML Job: DISKRUN_R2
Reticle: DISKRUN_R2
Field: P5CF - TOPLEFT
Exposure: 18mJ
Focus: 0nm

170. PR Development: Polysilicon electrode layer photoresist [P5CF] (P1-P9, O3)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Once
Process Note: Always run at least one dummy wafer first and visually check the developer uniformity.

171. PR Descum: Polysilicon electrode layer photoresist [P5CF] (P1-P9, O3)

Nanolab Tool: technics-c
Options: None
Gas Flows: O_2 = 180sccm
Power: 30W
Time: 00:00:15
Process Note: 'technics-c' etch rates wildly changes from time to time. Take the numbers in the manual as a reference and make sure to test the current etch rate especially if there are designs with feature size less than 500nm and precise width control is critical.

172. PR UV-bake: Polysilicon electrode layer photoresist [P5CF] (P1-P9, O3)

Nanolab Tool: axcelis

Options: None
Program: U

173. Etch: Polysilicon electrode layer [P5CF] (P1-P9, O3)

Nanolab Tool: sts2
Options: None
Recipe Name: SMOOTH SIDEWALL 1
Passivation
Cycle Time: 5sec
Gas Flows: C_4F_8 = 100sccm, SF_6 = 0sccm, O_2 = 0sccm
Pressure: 18mTorr
Power: Coil = 600W, Bias = 0W
Etch
Cycle Time: 7sec
Gas Flows: C_4F_8 = 0sccm, SF_6 = 130sccm, O_2 = 13sccm
Pressure: 35mTorr
Power: Coil = 600W, Bias = 20W @ 13.56MHz

Etch Rate: 350nm/cycle
Selectivity: 50:1
Etch Time: 17 cycles
Process Note-1: Use the test wafer 'O3' to verify the etch rate and also to condition the chamber before etching the process wafers.
Process Note-2: Note that deep reactive ion etching (DRIE) etch rate heavily depends on the amount of polysilicon to be etched as well as the location on a wafer, i.e., edge region etches faster than the center. So, it is important to visually and electrically check the wafer to make sure the etch is complete.

174. Metrology: Polysilicon electrode layer conductivity check after etching (P1-P9)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance between pads that are not connected on the layout. If the etch is complete, this measurement should indicate infinite resistance ('open').

175. PR Strip: Polysilicon electrode layer photoresist [P5CF] (P1-P9)

Nanolab Tool: matrix
Options: technics-c, msink1-1165, msink16 & msink18-PRS3000
Pressure: 3.75Torr
Temperature: 250°C
Power: 400W
Time: 00:02:30
Process Note: Run the recipe twice.

176. Metrology: Polysilicon electrode layer step height measurement (P1-P9)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 10µm
Expected: >3µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

177. Post-Etch Cleaning: Polysilicon electrode layer (P1-P9)

Nanolab Tool: msink8
Options: msink7, msink16, msink18
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

178. Backside Etch: Polysilicon electrode layer (P1-P9)

Nanolab Tool: sts2
Options: lam8
Recipe Name: SMOOTH SIDEWALL 1
Passivation
Cycle Time: 5sec
Gas Flows: C_4F_8 = 100sccm, SF_6 = 0sccm, O_2 = 0sccm
Pressure: 18mTorr
Power: Coil = 600W, Bias = 0W
Etch
Cycle Time: 7sec
Gas Flows: C_4F_8 = 0sccm, SF_6 = 130sccm, O_2 = 13sccm
Pressure: 35mTorr
Power: Coil = 600W, Bias = 20W @ 13.56MHz

Etch Rate: 350nm/cycle
Etch Time: Etch until shiny polysilicon layer is completely etched away. If visual check is not enough, use a multimeter to verify.

179. Backside Etch: Sidewall sacrificial & oxide hard mask layer (P1-P9)

Nanolab Tool: sts-oxide
Options: lam6
Recipe Name: Oxide etch (APS) no 2-2
Gas Flows: C_4F_8 = 15sccm, H_2 = 4sccm, He = 174sccm
Pressure: 10mTorr
Power: Coil = 1500W, Bias = 400W @ 13.56MHz
Etch Rate: 406nm/min
Etch Time: Etch until shiny polysilicon layer is completely exposed. If visual check is not enough, use a multimeter to verify.

180. Backside Etch: Polysilicon structural layer (P1-P9)

Nanolab Tool: sts2

Options: lam8
Recipe Name: SMOOTH SIDEWALL 1
Passivation
Cycle Time: 5sec
Gas Flows: C_4F_8 = 100sccm, SF_6 = 0sccm, O_2 = 0sccm
Pressure: 18mTorr
Power: Coil = 600W, Bias = 0W
Etch
Cycle Time: 7sec
Gas Flows: C_4F_8 = 0sccm, SF_6 = 130sccm, O_2 = 13sccm
Pressure: 35mTorr
Power: Coil = 600W, Bias = 20W @ 13.56MHz

Etch Rate: 350nm/cycle
Etch Time: Etch until shiny polysilicon layer is completely etched away. If visual check is not enough, use a multimeter to verify.

181. Backside Etch: Oxide spacer layer (P1-P9)

Nanolab Tool: sts-oxide
Options: lam6
Recipe Name: Oxide etch (APS) no 2-2
Gas Flows: C_4F_8 = 15sccm, H_2 = 4sccm, He = 174sccm
Pressure: 10mTorr
Power: Coil = 1500W, Bias = 400W @ 13.56MHz
Etch Rate: 406nm/min
Etch Time: Etch until shiny polysilicon layer is completely exposed. If visual check is not enough, use a multimeter to verify.

182. Backside Etch: Polysilicon interconnect layer (P1-P9)

Nanolab Tool: sts2
Options: lam8
Recipe Name: SMOOTH SIDEWALL 1
Passivation
Cycle Time: 5sec
Gas Flows: C_4F_8 = 100sccm, SF_6 = 0sccm, O_2 = 0sccm
Pressure: 18mTorr
Power: Coil = 600W, Bias = 0W
Etch
Cycle Time: 7sec
Gas Flows: C_4F_8 = 0sccm, SF_6 = 130sccm, O_2 = 13sccm
Pressure: 35mTorr
Power: Coil = 600W, Bias = 20W @ 13.56MHz

Etch Rate: 350nm/cycle
Etch Time: Etch until shiny polysilicon layer is completely etched away. If visual check is not enough, use a multimeter to verify.

183. Post-Etch Cleaning: Backside layer removal (P1-P9)

Nanolab Tool: msink8
Options: msink7
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

184. Dicing (P1-P9)

Nanolab Tool: disco
Options: Manual dicing with a diamond scriber
Process Note: Sometimes dies fly away and get lost in the tool during dicing. Coating wafer with photoresist before starting dicing is a good idea to avoid this.

185. Release: Clean baskets, dishes, tweezers, and glass beakers

Nanolab Tool: msink16 & msink18
Options: None
Chemical: Piranha (Sulfuric Acid : Hydrogen Peroxide = 1 : 1)
Temperature: Set by the activated chemical
Time: 00:10:00
Process Note: Rinse all equipment with water before and after the piranha clean.

186. Release: Piranha clean dies

Nanolab Tool: msink16 & msink18
Options: None
Chemical: Piranha (Sulfuric Acid : Hydrogen Peroxide = 1 : 1)
Temperature: Set by the activated chemical
Time: 00:10:00
Process Note-1: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) before and after the piranha clean.
Process Note-2: Slowly agitate the basket during piranha clean to get bubbles out.

187. Release: Initial 49% HF release

Nanolab Tool: msink16 & msink18
Options: None
Chemical: 49% HF
Temperature: Room temperature
Time: 00:02:00
Process Note-1: This step removes the PSG hard mask and oxide spacer. Note that 2min in this step is not enough to fully release the devices.
Process Note-2: Agitate during this step to remove the bubbles formed during HF etch.
Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

188. Release: Piranha clean dies after initial 49% HF etch

Nanolab Tool: msink16 & msink18

Options: None
Chemical: Piranha (Sulfuric Acid : Hydrogen Peroxide = 1 : 1)
Temperature: Set by the activated chemical
Time: 00:20:00
Process Note-1: Clean any PSG residue left by the hard mask and oxide spacer with piranha.
Process Note-2: Slowly agitate the basket during piranha clean to get bubbles out.
Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

189. Release: Main 49% HF release
Nanolab Tool: msink16 & msink18
Options: None
Chemical: 49% HF
Temperature: Room temperature
Time: Ranges from 00:20:00 (for 80nm gap) to 02:30:00 (for 5nm gap)
Process Note-1: This step fully releases the devices.
Process Note-2: Agitate during this step to remove the bubbles formed during HF etch.
Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

190. Release: Piranha clean dies after main 49% HF etch
Nanolab Tool: msink16 & msink18
Options: None
Chemical: Piranha (Sulfuric Acid : Hydrogen Peroxide = 1 : 1)
Temperature: Set by the activated chemical
Time: 00:20:00
Process Note-1: Clean any PSG residue left by the hard mask and oxide spacer with piranha. Also, clean any residue remained in the actuation gap.
Process Note-2: Slowly agitate the basket during piranha clean to get bubbles out.
Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

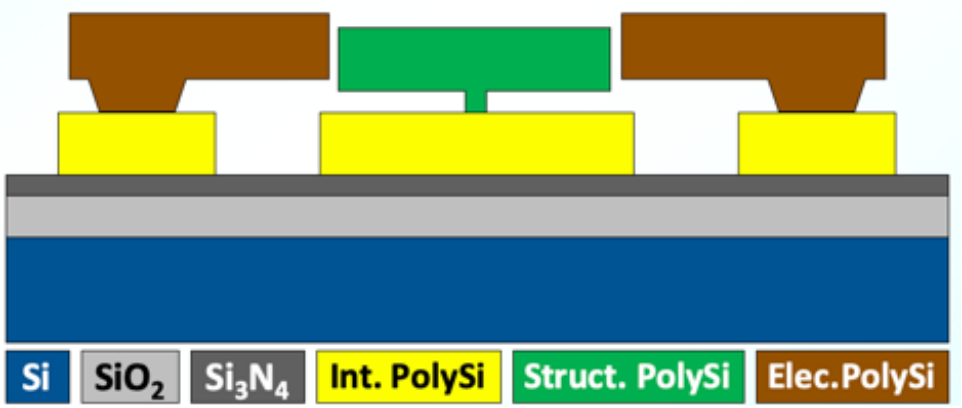
191. Release: Final 49% HF release
Nanolab Tool: msink16 & msink18
Options: None
Chemical: 49% HF
Temperature: Room temperature
Time: 00:05:00
Process Note-1: This step removes any oxide remained in the actuation gap as well as piranha-induced surface oxide.
Process Note-2: Agitate during this step to remove the bubbles formed during HF etch.
Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

192. Release: Methanol rinse
Nanolab Tool: msink16 & msink18

Options: None
Chemical: Methanol
Temperature: Room temperature
Time: 00:03:00
Process Note-1: Rinse the dies placed in a Teflon basket in Teflon dishes filled with methanol three times (each 1min) after this step. Methanol should completely replace DI water at the end of this step.
Process Note-2: It is extremely important that the dies never dry out between this step and the following critical point drying step to prevent stiction. Transfer dies to 'cpd' in a container filled with methanol.

193. Critical Point Drying

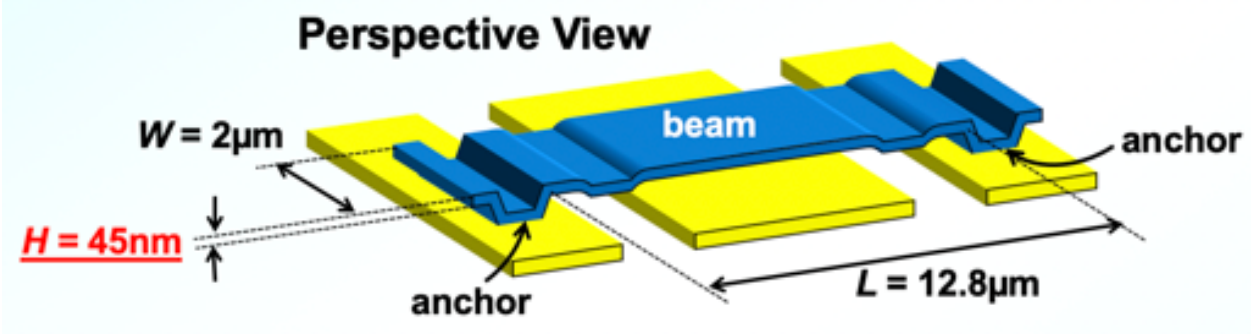
Nanolab Tool: cpd
Options: primaxx
Temperature: Set by the tool.
Purge Time: 00:25:00 (Setting '5')
Process Note: Make sure the methanol level in 'cpd' fully covers the dies before closing the chamber.
Cross Section:

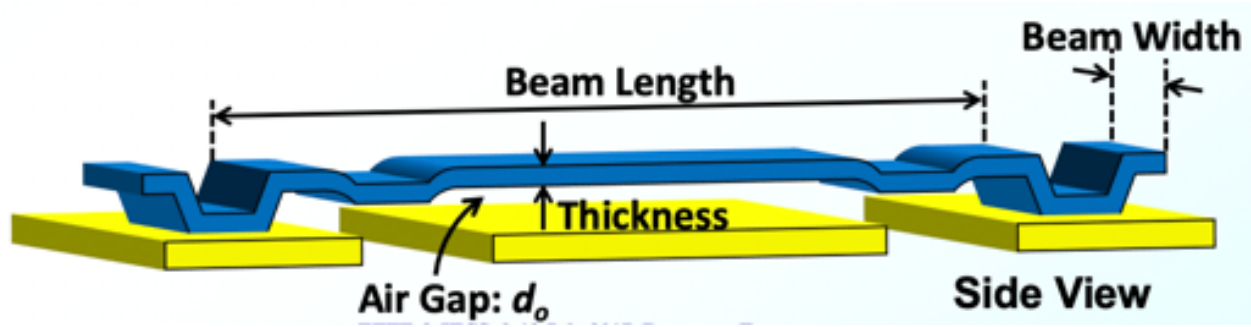


194. Probe Station Testing

Tool: Lakeshore
Options: Wirebonding, MMR
Temperature: Room temperature
Vacuum: <100µTorr
Process Note: Make sure the Lakeshore probes are not bent and functional. Also, check the measurement setup, i.e., bias tees, cables etc., with a known working device in advance.

Appendix C
Ruthenium CC-Beam Process Traveler





0. Tools needed in the Nanolab

Deposition	*Etchers*	*Lithography*	*Metrology*	*Release*	*Cleaning*	*Misc.*
tystar9	centura-mxp	picotrack1	alphastep	cpd	msink6	rtp3
tystar11	centura-met	picotrack2	flexus		msink8	
tystar12		asml300	cde-resmap		msink16	
randex			nanospec		msink18	
			dektak		msink1	

1. Starting wafers (P1, S1-S4, TS0-TS3, O1-O4, TO0-TO4)

Doping: p-type
Wafer Class: prime
Wafer Size: 6”
Scribing: On the front, near right side of the major flat.
Process Note-1: Never scribe the wafer back side as some tools apply vacuum on the back side to keep the wafers still and also to apply helium cooling.

Process Note-2: Make sure the scribing does not have any lines aligned with the Si wafer crystal orientation, making the wafer physically less resistant to mechanical force or impact such as water pressure during quick dump rinse (QDR), mechanical force and/or bending during wafer transfer, rotational force during spin rinse dry (SDR) etc. Use letters like 'S', 'O' that do not have any lines rather than 'I', 'H'. Or scribe the latter letters in angled way such that they are not aligned with the crystal axis.

Cross Section:

2. Cleaning: Pre-furnace cleaning (P1, S1-S4, TS0-TS3, O1-O4, TO0-TO4)

Nanolab Tool: msink6

1st Chemical:	Piranha at 120°C	*2nd Chemical:*	10:1 HF
Temperature:	120°C	*Temperature:*	Room temperature
Time:	00:10:00	*Time:*	00:02:00

3. Test Deposition: Thin oxide dummy wafer (TO0)

Nanolab Tool: tystar11
Options: tystar9, tystar12, tystar17
Recipe: 11SULTON
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 11.58nm/min
Time: 00:15:00
Process Note: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.

4. Test Metrology: Thin oxide thickness measurement (TO0)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)

Thickness:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Dep. Rate:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____

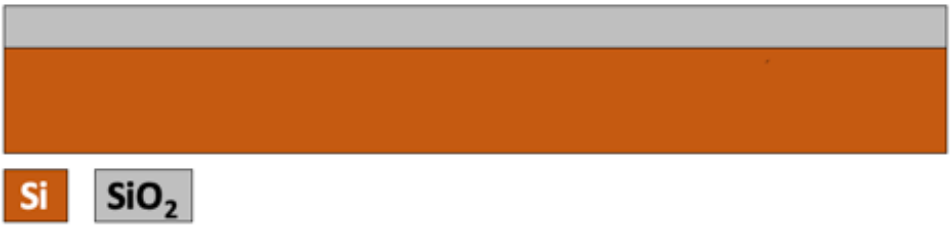
5. Deposition: Thin oxide dummy wafers (O1-O4, TO1-TO4)

Nanolab Tool: tystar11
Options: tystar9, tystar12, tystar17
Recipe: 11SULTON
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
Pressure: 400mTorr

Temperature: 450°C
Dep. Rate: 11.58nm/min (adjust if needed)
Time: 00:08:00 (adjust if needed)
Goal: 100nm
Process Note-1: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.
Process Note-2: These wafers will be used as control and test wafers in several subsequent polysilicon depositions alongside the actual process wafers. The reason for the very thin oxide layer is because 'nanospec' can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

6. Deposition: Isolation oxide (P1)

Nanolab Tool: tystar11
Options: tystar9, tystar12, tystar17
Recipe: 11SULTON
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 11.58nm/min (adjust if needed)
Time: 03:00:00 (adjust if needed)
Goal: 2µm
Process Note: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.
Cross Section:



7. Annealing: Thin and isolation oxide densification (P1, O1-O4, TO1-TO4)

Nanolab Tool: tystar2
Options: tystar3, tystar4
Recipe: 2HIN2ANA
Temperature: 1000°C
Time: 01:00:00
Process Note: Unannealed low temperature oxide (LTO) sometimes bubbles at high temperatures. So, annealing immediately after the deposition prevents this from happening at later stages in the process.

8. Metrology: Thin oxide thickness measurement (O1-O4, TO1-TO4)

Nanolab Tool: nanospec

Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 100nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

9. Metrology: Isolation oxide thickness measurement (P1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Expected: 2µm
Result (P1): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result (P2): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

10. Test Deposition: Isolation nitride (TS0)

Nanolab Tool: tystar9
Options: tystar17, cambridge Al_2O_3
Recipe: 9LSNVARA
Gas Flows: DCS = 100sccm, NH_3 = 18sccm
Pressure: 375mTorr
Temperature: 835°C
Time: 01:00:00

11. Test Metrology: Isolation nitride thickness measurement (TS0)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

12. Pre-Deposition Cleaning: Isolation nitride (P1, S1)

Nanolab Tool: msink8
Options: msink7
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None
Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

13. Deposition: Isolation nitride (P1, S1)

Nanolab Tool: tystar9
Options: tystar17, cambridge Al_2O_3
Recipe: 9LSNVARA

Gas Flows: DCS = 100sccm, NH_3 = 18sccm
Pressure: 375mTorr
Temperature: 835°C
Dep. Rate: 2.78nm/min (adjust if needed)
Time: 03:00:00 (adjust if needed)
Goal: 500nm
Process Note-1: Include a bare silicon wafer ('S1') as a test wafer for the thickness measurement. 'nanospec' can measure nitride layer thickness correctly only when the underlying layer is silicon.
Process Note-2: Note that the deposition rate variation in tystar9 low stress nitride deposition is significant, i.e., ~25% from the center of the rear 6" boat to that of the front 6" boat. So, use at most six wafers and an additional bare Si test wafer ('S1') in each deposition to obtain good average thickness uniformity between the process wafers.
Cross Section:

14. Post-Deposition Cleaning: Nitride surface cleaning (P1, S1)

Nanolab Tool: msink6
Options: msink8, msink16, msink18
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
2nd Chemical: 25:1 HF (or 10:1 HF)
Temperature: Room temperature
Time: 00:05:00
Process Note: Nitride furnaces are notoriously known to deposit particles on wafer surface. Such particles, if not removed properly, may cause adhesion issues for the subsequent layer in the process, i.e., polysilicon. Cleaning with piranha and HF helps remove these particles and provides with better surface condition for the following layer.

15. Metrology: Isolation nitride initial thickness measurement (S1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Expected: 500nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Use the test wafer ('S1') obtained in the previous step. Do not use the actual process wafers for this measurement as 'nanospec' can measure nitride layer thickness correctly only when the underlying layer is silicon.

16. Etch: Isolation nitride 49% HF etch rate test (S1)

Nanolab Tool: msink7
Options: msink16, msink18
1st Chemical: 49% HF
Temperature: Room temperature
Time: 00:10:00
Process Note: We have recently realized an enhanced 49% HF etch rate for nitride coming out of 'tystar17'. 'tystar9' low stress nitride (LSN) seems to be more resistant to 49% HF. Due to very long 49% HF release times, i.e., longer than 30min, it is important that the nitride etch rate stays below 1-2nm/min to prevent excessive polysilicon interconnect undercut. So, this test is necessary to make sure the isolation nitride will be resistant enough to 49% HF during device release at the end of the process.

17. Metrology: Isolation nitride 49% HF etch rate measurement (S1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Target: < 2nm/min
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Etch Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: If the target is not met, recipe changes might be needed. Note that even an enhanced nitride etch rate in 49% HF might be acceptable depending on the release time. For example, 5nm/min might be excessive for a 120min-release but acceptable for a 30min-release.

18. Test Deposition: PECVD oxide hard mask (TS1)

Nanolab Tool: oxford2
Options: oxfordpecvd3
Recipe: oxide1.rec
Gas Flows: N_2O = 800sccm, 10% SiH_4/Ar = 100sccm, PH_3/Si = 40sccm
Pressure: 900mTorr
Temperature: 350°C
RF Power: 20W HF Forward Power
Time: 00:20:00
Process Note: Use a bare silicon wafer ('TS1') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

19. Test Metrology: PECVD oxide hard mask (TS1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

20. Test Etch: PECVD oxide hard mask (TS1)

Nanolab Tool: centura-mxp
Options: lam6
Recipe Name: MXP-OXIDE-ETCH
Gas Flows: Ar = 150sccm, CHF_3 = 45sccm, CF_4 = 45sccm
Pressure: 200mTorr
Power: 500W
Etch Time: 00:01:00
Process Note: centura-mxp's electrostatic chuck (ESC) has known issues for sometimes not properly de-clamping wafers once the etch is complete. If the process wafer is attempted to move from one chamber to another without proper de-clamping, the moving arm hits the wafer and breaks it. So, make sure the ESC voltage on the centura-mxp screen has been set to 0V before attempting to move the process wafer.

21. Test Metrology: PECVD oxide hard mask MXP etch rate (TS1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Etch Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

22. Test Deposition: Ruthenium interconnect layer (S1)

Nanolab Tool: randex
Options: oxfordpvd1
Gas Flows: Ar = 100-110sccm (ON)
Pressure: 6mTorr
Power: 130W (with 30W reverse power)
Stage Rotation: Rotating
Pre-Sputter: 00:15:00
Temperature: Nominally room temperature / No cooling
Time: 00:40:00

23. Test Deposition: Ruthenium interconnect layer PECVD oxide hard mask (S1, TS2)

Nanolab Tool: oxford2
Options: oxfordpecvd3
Recipe: oxide1.rec
Gas Flows: N_2O = 800sccm, 10% SiH_4/Ar = 100sccm, PH_3/Si = 40sccm
Pressure: 900mTorr
Temperature: 350°C
RF Power: 20W HF Forward Power
Dep. Rate: 60nm/min (adjust if needed)
Time: 00:01:00 (adjust if needed)
Goal: 60nm
Process Note: Use a bare silicon wafer ('TS2') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

24. Test Metrology: Ruthenium interconnect layer PECVD oxide hard mask (TS2)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

25. Test PR Coating: Ruthenium interconnect layer [P1CF] (S1)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 400nm
Recipe: T1_UV210-0.6_0.43um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

26. Test PR Exposure: Ruthenium interconnect layer [P1CF] (S1)

Nanolab Tool: asml300
Options: None
ASML Job: NZERO1
Reticle: NZERO1
Field: P1CF - TOPLEFT
Exposure: 17mJ
Focus: 0nm

27. Test PR Development: Ruthenium interconnect layer [P1CF] (S1)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Once
Process Note: Always run at least one dummy wafer first and visually check the developer uniformity.

28. Test Etch: Ruthenium interconnect layer PECVD oxide hard mask (S1)

Nanolab Tool: centura-mxp
Options: lam6
Recipe Name: MXP-OXIDE-ETCH
Gas Flows: Ar = 150sccm, CHF_3 = 45sccm, CF_4 = 45sccm
Pressure: 200mTorr
Power: 500W
Etch Rate: Obtained in previous steps
Etch Time: 00:00:30 (adjust if needed)

Process Note: centura-mxp's electrostatic chuck (ESC) has known issues for sometimes not properly de-clamping wafers once the etch is complete. If the process wafer is attempted to move from one chamber to another without proper de-clamping, the moving arm hits the wafer and breaks it. So, make sure the ESC voltage on the centura-mxp screen has been set to 0V before attempting to move the process wafer.

29. Test Etch: Ruthenium interconnect layer (S1)

Nanolab Tool: centura-met
Options: lam7
Recipe Name: OZGURLUK_RU
Gas Flows: Cl_2 = 20sccm, O_2 = 90sccm
Pressure: 10mTorr
RF Power: 130W
DC Power: 50W
Etch Time: 00:03:00 (adjust if needed)
Process Note: Make sure the etch is complete with visual and electrical check.

30. Test Metrology: Ruthenium interconnect layer (S1)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance between pads that are not connected on the layout. If the polysilicon removal is complete, this measurement should indicate infinite resistance ('open').

31. Test Cleaning: Ruthenium interconnect layer PR (S1)

Nanolab Tool: msink1
Options: msink16, msink18

1st Chemical:	1165	*2nd Chemical:*	SVC-14
Temperature:	80°C	*Temperature:*	70°C
Time:	01:00:00	*Time:*	00:30:00

32. Test Cleaning: Ruthenium interconnect layer PECVD oxide hard mask (S1)

Nanolab Tool: msink8
Options: msink16, msink18
Chemical: 5:1 BHF
Temperature: Room temperature
Time: 00:01:00

33. Test Metrology: Ruthenium interconnect layer (S1)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 5µm
Expected: 50-100nm

Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

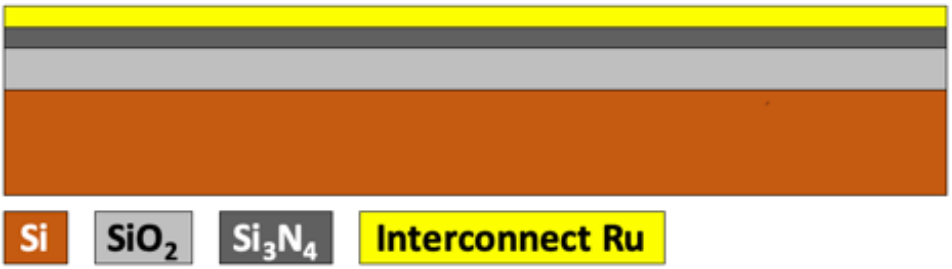
34. Pre-Deposition Cleaning: Ruthenium interconnect layer (P1, O1, S2)

Nanolab Tool: msink8
Options: msink7
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None
1st Chemical: Piranha
Temperature: 120°C
Time: 00:10:00
2nd Chemical: 25:1 HF
Temperature: Room temperature
Time: 00:02:00

35. Deposition: Ruthenium interconnect layer (P1, O1)

Nanolab Tool: randex
Options: oxfordpvd1
Gas Flows: Ar = 100-110sccm (ON)
Pressure: 6mTorr
Power: 130W (with 30W reverse power)
Stage Rotation: Rotating
Pre-Sputter: 00:15:00
Temperature: Nominally room temperature / No cooling
Time: 00:40:00
Process Note: Use a thin oxide dummy wafer ('O1') as a test wafer for the following sheet resistance measurement.
Cross Section:



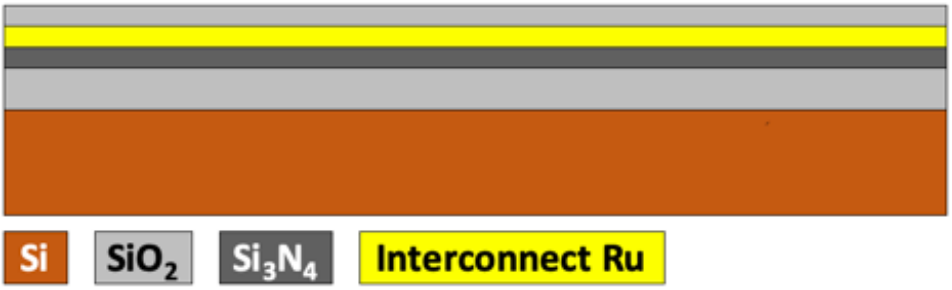
36. Metrology: Ruthenium interconnect layer (O1)

Nanolab Tool: cde-resmap
Options: None
Program: 5 point
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

37. Deposition: Ruthenium interconnect layer PECVD oxide hard mask (P1, S2)

Nanolab Tool: oxford2

Options: oxfordpecvd3
Recipe: oxide1.rec
Gas Flows: N_2O = 800sccm, 10% SiH_4/Ar = 100sccm, PH_3/Si = 40sccm
Pressure: 900mTorr
Temperature: 350°C
RF Power: 20W HF Forward Power
Dep. Rate: 60nm/min (adjust if needed)
Time: 00:01:00 (adjust if needed)
Goal: 60nm
Process Note: Use a bare silicon wafer ('S2') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



38. Metrology: Ruthenium interconnect layer PECVD oxide hard mask (S2)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

39. PR Coating: Ruthenium interconnect layer [P1CF] (P1)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 400nm
Recipe: T1_UV210-0.6_0.43um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

40. PR Exposure: Ruthenium interconnect layer [P1CF] (P1)

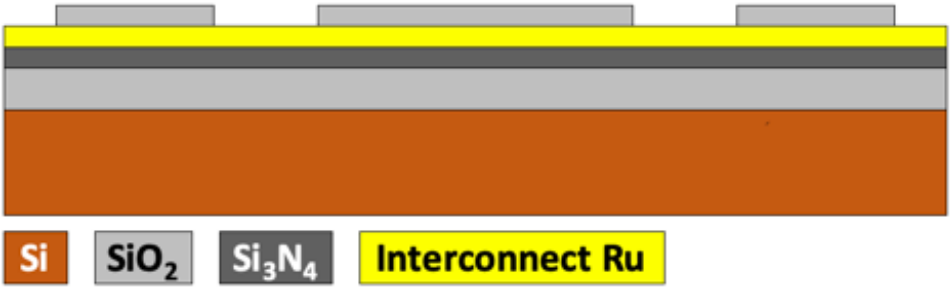
Nanolab Tool: asml300
Options: None
ASML Job: NZERO1
Reticle: NZERO1
Field: P1CF - TOPLEFT
Exposure: 17mJ
Focus: 0nm

41. PR Development: Ruthenium interconnect layer [P1CF] (P1)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Once
Process Note: Always run at least one dummy wafer first and visually check the developer uniformity.

42. Etch: Ruthenium interconnect layer PECVD oxide hard mask (P1)

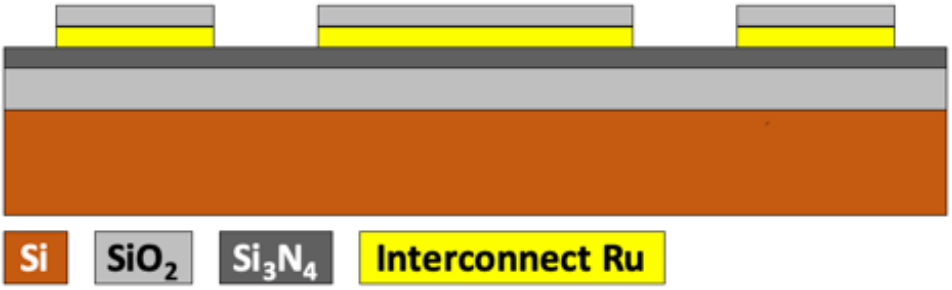
Nanolab Tool: centura-mxp
Options: lam6
Recipe Name: MXP-OXIDE-ETCH
Gas Flows: Ar = 150sccm, CHF_3 = 45sccm, CF_4 = 45sccm
Pressure: 200mTorr
Power: 500W
Etch Rate: Obtained in previous steps
Etch Time: 00:00:30 (adjust if needed)
Process Note: centura-mxp's electrostatic chuck (ESC) has known issues for sometimes not properly de-clamping wafers once the etch is complete. If the process wafer is attempted to move from one chamber to another without proper de-clamping, the moving arm hits the wafer and breaks it. So, make sure the ESC voltage on the centura-mxp screen has been set to 0V before attempting to move the process wafer.
Cross Section:



43. Etch: Ruthenium interconnect layer (P1)

Nanolab Tool: centura-met
Options: lam7
Recipe Name: OZGURLUK_RU
Gas Flows: Cl_2 = 20sccm, O_2 = 90sccm
Pressure: 10mTorr
RF Power: 130W
DC Power: 50W
Etch Time: 00:03:00 (adjust if needed)
Process Note: Make sure the etch is complete with visual and electrical check.

Cross Section:



44. Metrology: Ruthenium interconnect layer (P1)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance between pads that are not connected on the layout. If the polysilicon removal is complete, this measurement should indicate infinite resistance ('open').

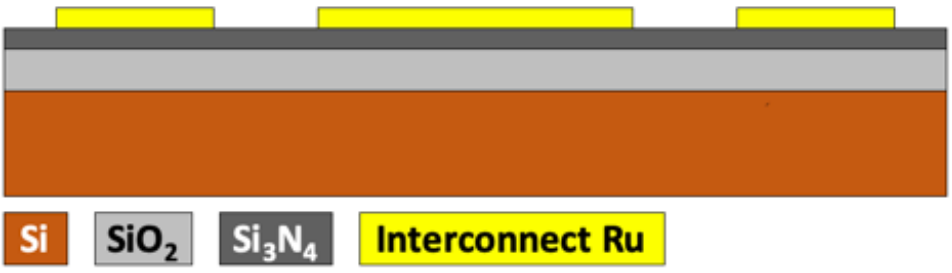
45. Cleaning: Ruthenium interconnect layer PR (P1)

Nanolab Tool: msink1
Options: msink16, msink18

1st Chemical:	1165	*2nd Chemical:*	SVC-14
Temperature:	80°C	*Temperature:*	70°C
Time:	01:00:00	*Time:*	00:30:00

46. Cleaning: Ruthenium interconnect layer PECVD oxide hard mask (P1)

Nanolab Tool: msink8
Options: msink16, msink18
1st Chemical: 5:1 BHF
Temperature: Room temperature
Time: 00:01:00
Cross Section:



47. Metrology: Ruthenium interconnect layer (P1)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 5µm

Expected: 50-100nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

48. Pre-Deposition Cleaning: Sacrificial oxide layer (P1, S3, TS3)

Nanolab Tool: msink1
Options: msink16, msink18
1st Chemical: SVC-14
Temperature: 40°C
Time: 00:10:00
Process Note: Include bare Si test wafers ('S3') for the subsequent oxide deposition steps.

49. Test Deposition: Sacrificial oxide layer (TS3)

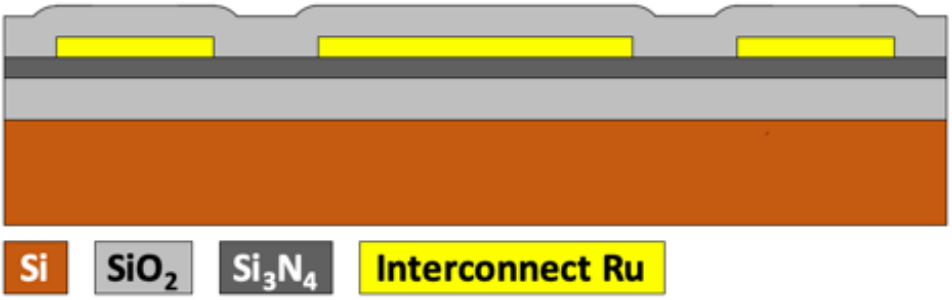
Nanolab Tool: tystar12
Options: tystar11
Recipe: 12VDLTOA
Gas Flows: O_2 = 45sccm, SiH_4 = 30sccm, PH_3/Si = 0sccm
Pressure: 200mTorr
Temperature: 450°C
Time: 00:30:00
Process Note: Note that this is a 'slowed LTO' recipe with substantially reduced process temperature and gas flows to reduce the deposition rate hence enhance conformality and uniformity.

50. Test Metrology: Sacrificial oxide layer (TS3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

51. Deposition: Sacrificial oxide layer (P1, S3)

Nanolab Tool: tystar12
Options: tystar11
Recipe: 12VDLTOA
Gas Flows: O_2 = 45sccm, SiH_4 = 30sccm, PH_3/Si = 0sccm
Pressure: 200mTorr
Temperature: 450°C
Dep. Rate: 4.8nm/min (adjust if needed)
Time: 00:25:00 (adjust if needed)
Goal: 120nm
Process Note: Note that this is a 'slowed LTO' recipe with substantially reduced process temperature and gas flows to reduce the deposition rate hence enhance conformality and uniformity.
Cross Section:



52. Metrology: Sacrificial oxide layer (S3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

53. PR Coating: Anchor layer photoresist [P2DF] (P1)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 900nm
Recipe: T1_UV210-0.6_0.87um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

54. PR Exposure: Anchor layer photoresist [P2DF] (P1)

Nanolab Tool: asml300
Options: None
ASML Job: DISKRUN_R1
Reticle: DISKRUN_R1
Field: P2DF - TOPRIGHT
Exposure: 26mJ (P1-P6, S6) / 34mJ (P7-P9)
Focus: 0nm
Process Note: It is important to use a high enough exposure rate for this mask to make sure the stem holes are fully exposed as they are really tiny. Run a focus-exposure matrix (FEM) first if needed.

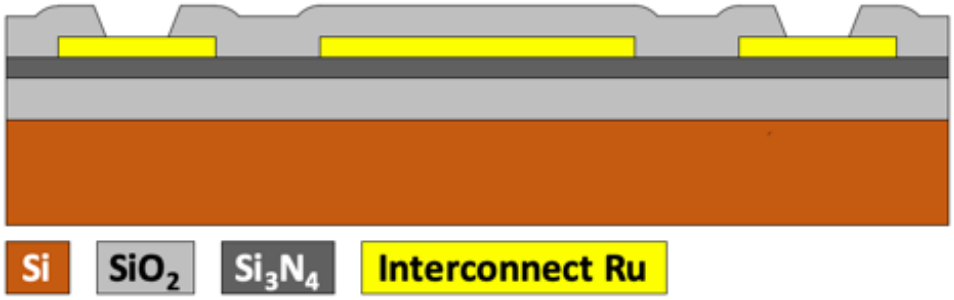
55. PR Development: Anchor layer photoresist [P2DF] (P1)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Twice
Process Note-1: Always run at least one dummy wafer first and visually check the developer uniformity.

Process Note-2: Develop twice for dark field masks to make sure all residual photoresist in the patterned area gets removed.

56. Etch: Anchor layer sacrificial oxide spacer (P1)

Nanolab Tool: centura-mxp
Options: lam6
Recipe Name: MXP-OXIDE-ETCH
Gas Flows: Ar = 150sccm, CHF_3 = 45sccm, CF_4 = 45sccm
Pressure: 200mTorr
Power: 500W
Etch Rate: Obtained in previous steps
Etch Time: 00:01:00 (adjust if needed)
Process Note: centura-mxp's electrostatic chuck (ESC) has known issues for sometimes not properly de-clamping wafers once the etch is complete. If the process wafer is attempted to move from one chamber to another without proper de-clamping, the moving arm hits the wafer and breaks it. So, make sure the ESC voltage on the centura-mxp screen has been set to 0V before attempting to move the process wafer.
Cross Section:



57. Cleaning: Anchor layer PR (P1)

Nanolab Tool: msink1
Options: msink16, msink18

1st Chemical:	1165	*2nd Chemical:*	SVC-14
Temperature:	80°C	*Temperature:*	70°C
Time:	01:00:00	*Time:*	00:30:00

58. Metrology: Anchor layer (P1)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 5µm
Expected: 120nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

59. Pre-Deposition Cleaning: Ruthenium structural layer (P1, O2, S4)

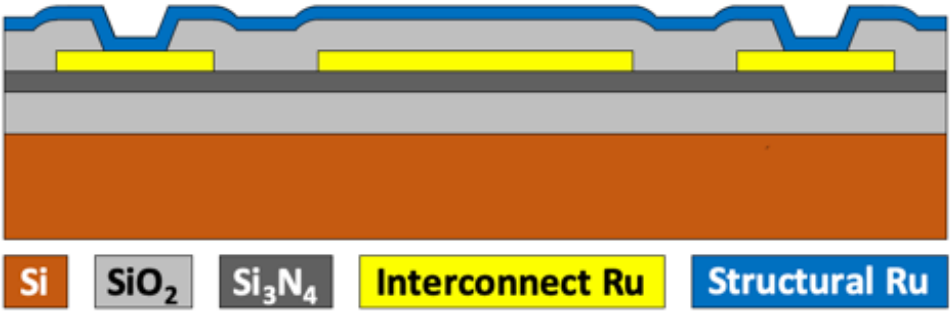
Nanolab Tool: msink1
Options: msink16, msink18

1st Chemical:	1165	*2nd Chemical:*	SVC-14

Temperature:	80°C	*Temperature:*	70°C
Time:	01:00:00	*Time:*	00:30:00

60. Deposition: Ruthenium structural layer (P1, O2)

Nanolab Tool: randex
Options: oxfordpvd1
Gas Flows: Ar = 100-110sccm (ON)
Pressure: 6mTorr
Power: 130W (with 30W reverse power)
Stage Rotation: Rotating
Pre-Sputter: 00:15:00
Temperature: Nominally room temperature / No cooling
Time: 00:30:00
Process Note: Use a thin oxide dummy wafer ('O2') as a test wafer for the following sheet resistance measurement.
Cross Section:



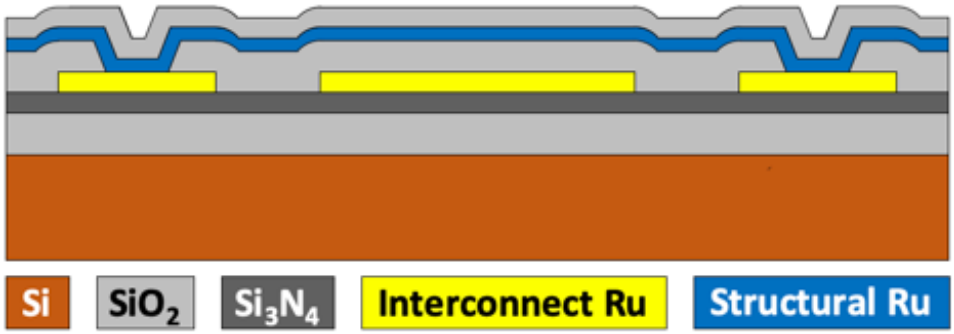
61. Metrology: Ruthenium structural layer (O2)

Nanolab Tool: cde-resmap
Options: None
Program: 5 point
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

62. Deposition: Ruthenium structural layer PECVD oxide hard mask (P1, S4)

Nanolab Tool: oxford2
Options: oxfordpecvd3
Recipe: oxide1.rec
Gas Flows: N_2O = 800sccm, 10% SiH_4/Ar = 100sccm, PH_3/Si = 40sccm
Pressure: 900mTorr
Temperature: 350°C
RF Power: 20W HF Forward Power
Dep. Rate: 60nm/min (adjust if needed)
Time: 00:01:00 (adjust if needed)
Goal: 60nm
Process Note: Use a bare silicon wafer ('S4') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

Cross Section:



63. Metrology: Ruthenium structural layer PECVD oxide hard mask (S4)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

64. PR Coating: Ruthenium structural layer [P3CF] (P1)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 400nm
Recipe: T1_UV210-0.6_0.43um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

65. PR Exposure: Ruthenium structural layer [P3CF] (P1)

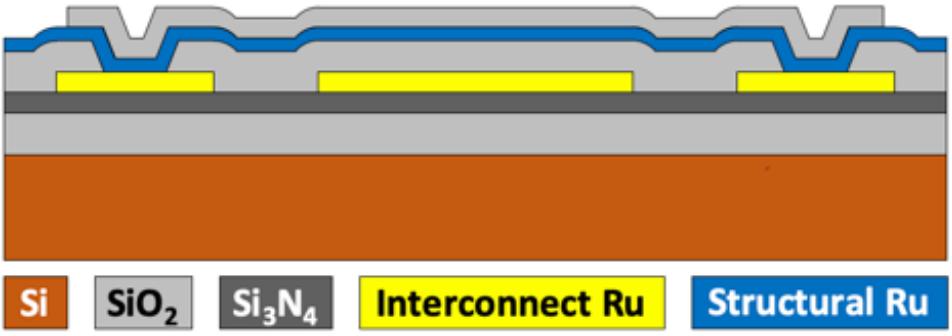
Nanolab Tool: asml300
Options: None
ASML Job: NZERO1
Reticle: NZERO1
Field: P3CF - TOPLEFT
Exposure: 16mJ
Focus: 0nm

66. PR Development: Ruthenium structural layer [P3CF] (P1)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Once
Process Note: Always run at least one dummy wafer first and visually check the developer uniformity.

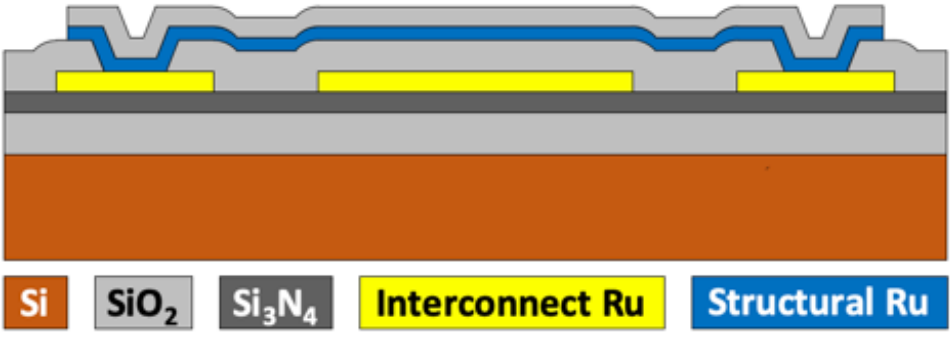
67. Etch: Ruthenium structural layer PECVD oxide hard mask (P1)

Nanolab Tool: centura-mxp
Options: lam6
Recipe Name: MXP-OXIDE-ETCH
Gas Flows: Ar = 150sccm, CHF_3 = 45sccm, CF_4 = 45sccm
Pressure: 200mTorr
Power: 500W
Etch Rate: Obtained in previous steps
Etch Time: 00:00:30 (adjust if needed)
Process Note: centura-mxp's electrostatic chuck (ESC) has known issues for sometimes not properly de-clamping wafers once the etch is complete. If the process wafer is attempted to move from one chamber to another without proper de-clamping, the moving arm hits the wafer and breaks it. So, make sure the ESC voltage on the centura-mxp screen has been set to 0V before attempting to move the process wafer.
Cross Section:



68. Etch: Ruthenium structural layer (P1)

Nanolab Tool: centura-met
Options: lam7
Recipe Name: OZGURLUK_RU
Gas Flows: Cl_2 = 20sccm, O_2 = 90sccm
Pressure: 10mTorr
RF Power: 130W
DC Power: 50W
Etch Time: 00:03:00 (adjust if needed)
Process Note: Make sure the etch is complete with visual and electrical check.
Cross Section:



69. Test Metrology: Ruthenium structural layer (P1)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance between pads that are not connected on the layout. If the polysilicon removal is complete, this measurement should indicate infinite resistance ('open').

70. Test Cleaning: Ruthenium structural layer PR (P1)

Nanolab Tool: msink1
Options: msink16, msink18

1st Chemical:	1165	*2nd Chemical:*	SVC-14
Temperature:	80°C	*Temperature:*	70°C
Time:	01:00:00	*Time:*	00:30:00

71. Test Metrology: Ruthenium structural layer (P1)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 5µm
Expected: 100-110nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

72. Dicing (P1)

Nanolab Tool: disco
Options: Manual dicing with a diamond scriber
Process Note: Sometimes dies fly away and get lost in the tool during dicing. Coating wafer with photoresist before starting dicing is a good idea to avoid this.

---------- Start: Rapid Thermal Anneal (RTA) ----------

73. Post-Processing: Rapid thermal anneal (RTA)

Nanolab Tool: rtp3
Options: None
Recipe: Ozgurluk_1000C1min
Process Note: Perform RTP with only N_2 flowing. Noe that the recipe should first stabilize around 450°C before ramping up to 900°C -1099°C. Use a rise/fall time within the 15-30sec interval. Too much RTP (this is a vague definition but usually means combination of RTP temperature and duration) may degrade the ruthenium layers and also put excessive stress on the beams causing them to break.

---------- End: Rapid Thermal Anneal (RTA) ----------

---------- Start: Localized Annealing ----------

74. Post-Processing: Clear sacrificial layer atop resonator pads

Nanolab Tool: msink16 & msink18
Options: None
Chemical: 49% HF
Temperature: Room temperature
Time: 00:00:10
Process Note-1: This step only removes the sacrificial layer atop resonator pads and does not fully release the devices.
Process Note-2: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

75. Post-Processing: Localized Annealing

Tool: Lakeshore
Options: Wentworth, MMR
Temperature: Room temperature
Pulse Voltage: 1V
Pulse Width: 10ms
Process Note: Make sure the Lakeshore probes are not bent and functional. Also, check the measurement setup, i.e., bias tees, cables etc., with a known working device in advance.

---------- End: Localized Annealing ----------

76. Release: Clean baskets, dishes, tweezers, and glass beakers

Nanolab Tool: msink16 & msink18
Options: None
Chemical: Piranha (Sulfuric Acid : Hydrogen Peroxide = 1 : 1)
Temperature: Set by the activated chemical
Time: 00:10:00
Process Note: Rinse all equipment with water before and after the piranha clean.

77. Release: Metal clean dies

Nanolab Tool: msink16 & msink18
Options: None
Chemical: SVC-14
Temperature: 70°C
Time: 00:10:00
Process Note: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) before and after the piranha clean.

78. Release: Main 49% HF release

Nanolab Tool: msink16 & msink18
Options: None
Chemical: 49% HF
Temperature: Room temperature

Time: 00:02:00
Process Note-1: This step fully releases the devices.
Process Note-2: Agitate during this step to remove the bubbles formed during HF etch.
Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

79. Release: Metal clean dies after main 49% HF etch

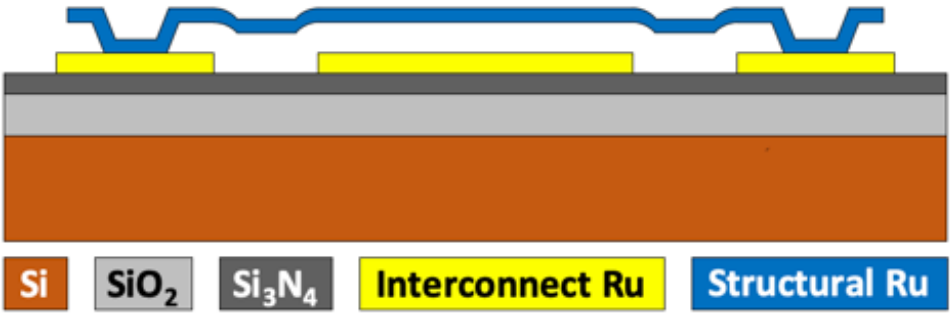
Nanolab Tool: msink16 & msink18
Options: None
Chemical: SVC-14
Temperature: 70°C
Time: 00:10:00
Process Note: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) before and after the piranha clean.

80. Release: Methanol rinse

Nanolab Tool: msink16 & msink18
Options: None
Chemical: Methanol
Temperature: Room temperature
Time: 00:03:00
Process Note-1: Rinse the dies placed in a Teflon basket in Teflon dishes filled with methanol three times (each 1min) after this step. Methanol should completely replace DI water at the end of this step.
Process Note-2: It is extremely important that the dies never dry out between this step and the following critical point drying step to prevent stiction. Transfer dies to 'cpd' in a container filled with methanol.

81. Critical Point Drying

Nanolab Tool: cpd
Options: primaxx
Temperature: Set by the tool.
Purge Time: 00:25:00 (Setting '5')
Process Note: Make sure the methanol level in 'cpd' fully covers the dies before closing the chamber.
Cross Section:



82. Probe Station Testing

Tool: Lakeshore
Options: Wirebonding, MMR
Temperature: Room temperature
Vacuum: <100μTorr
Process Note: Make sure the Lakeshore probes are not bent and functional. Also, check the measurement setup, i.e., bias tees, cables etc., with a known working device in advance.

Appendix D
Ruthenium Square Plate Process Traveler

0. Tools needed in the Nanolab

Deposition	*Etchers*	*Lithography*	*Metrology*	*Release*	*Cleaning*	*Misc.*
tystar9	centura-mxp	picotrack1	alphastep	cpd	msink6	rtp3
tystar11	centura-met	picotrack2	flexus		msink8	
tystar12		asml300	cde-resmap		msink16	
randex			nanospec		msink18	
			dektak		msink1	

1. Starting wafers (D21-D24, S1-S3, S11-S14, TS0-TS3, TS11-TS14, O1-O5, TO0-TO1)

Doping: p-type
Wafer Class: prime
Wafer Size: 6”
Scribing: On the front, near right side of the major flat.
Process Note-1: Never scribe the wafer back side as some tools apply vacuum on the back side to keep the wafers still and also to apply helium cooling.
Process Note-2: Make sure the scribing does not have any lines aligned with the Si wafer crystal orientation, making the wafer physically less resistant to mechanical force or impact such as water pressure during quick dump rinse (QDR), mechanical force and/or bending during wafer transfer, rotational force during spin rinse dry (SDR) etc. Use letters like ‘S’, ‘O’ that do not have any lines rather than ‘I’, ‘H’. Or scribe the latter letters in angled way such that they are not aligned with the crystal axis.
Cross Section:

2. Cleaning: Pre-furnace cleaning (D21-D24, S1-S3, S11-S14, TS0-TS3, TS11-TS14, O1-O5, TO0-TO1)

Nanolab Tool: msink6

1st Chemical:	Piranha	*2nd Chemical:*	10:1 HF
Temperature:	120°C	*Temperature:*	Room temperature
Time:	00:10:00	*Time:*	00:02:00

3. Test Deposition: Thin oxide dummy wafer (TO0)

Nanolab Tool: tystar11
Options: tystar9, tystar12, tystar17
Recipe: 11SULTON
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 11.58nm/min
Time: 00:15:00
Process Note-1: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.

4. Test Metrology: Thin oxide thickness measurement (TO0)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

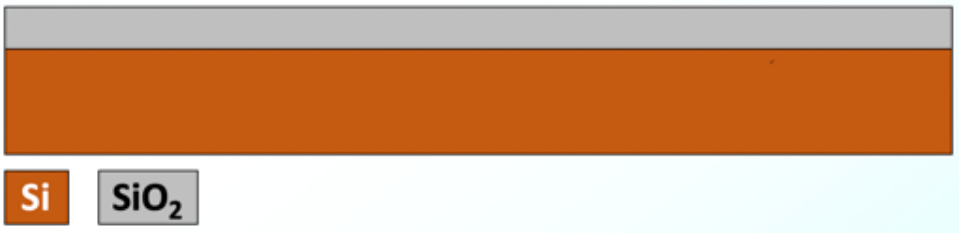
5. Deposition: Thin oxide dummy wafers (O1-O4, TO1-TO4)

Nanolab Tool: tystar11
Options: tystar9, tystar12, tystar17
Recipe: 11SULTON
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 11.58nm/min (adjust if needed)
Time: 00:08:00 (adjust if needed)
Goal: 100nm
Process Note-1: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.
Process Note-2: These wafers will be used as control and test wafers in several subsequent polysilicon depositions alongside the actual process wafers. The reason for the very thin oxide layer is because ‘nanospec’ can measure polysilicon layer thickness correctly only when the underlying layer is 100nm-thick oxide.

6. Deposition: Isolation oxide (D21-D24)

Nanolab Tool: tystar11
Options: tystar9, tystar12, tystar17
Recipe: 11SULTON
Gas Flows: O_2 = 135sccm, SiH_4 = 90sccm
Pressure: 400mTorr
Temperature: 450°C
Dep. Rate: 11.58nm/min (adjust if needed)

Time: 03:00:00 (adjust if needed)
Goal: 2µm
Process Note: 11SULTON has more aggressive PID parameters to stabilize the deposition temperature compared with 11SULTOA, making it preferable for depositions where precise temperature control is not critical.
Cross Section:



7. Annealing: Thin and isolation oxide densification (D21-D24, O1-O4, TO1-TO4)

Nanolab Tool: tystar2
Options: tystar3, tystar4
Recipe: 2HIN2ANA
Temperature: 1000°C
Time: 01:00:00
Process Note: Unannealed low temperature oxide (LTO) sometimes bubbles at high temperatures. So, annealing immediately after the deposition prevents this from happening at later stages in the process.

8. Metrology: Thin oxide thickness measurement (O1-O4, TO1-TO4)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Expected: 100nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

9. Metrology: Isolation oxide thickness measurement (D21-D24)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Expected: 2µm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

10. Test Deposition: Isolation nitride (TS0)

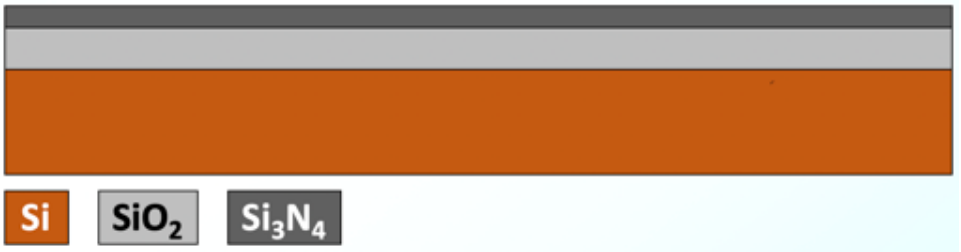
Nanolab Tool: tystar9
Options: tystar17, cambridge Al_2O_3
Recipe: 9LSNVARA
Gas Flows: DCS = 100sccm, NH_3 = 18sccm
Pressure: 375mTorr
Temperature: 835°C
Time: 01:00:00

11. Test Metrology: Isolation nitride thickness measurement (TS0)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

12. Deposition: Isolation nitride (D21-D24, S1)

Nanolab Tool: tystar9
Options: tystar17, cambridge Al_2O_3
Recipe: 9LSNVARA
Gas Flows: DCS = 100sccm, NH_3 = 18sccm
Pressure: 375mTorr
Temperature: 835°C
Dep. Rate: 2.78nm/min (adjust if needed)
Time: 03:00:00 (adjust if needed)
Goal: 500nm
Process Note-1: Include a bare silicon wafer ('S1') as a test wafer for the thickness measurement. 'nanospec' can measure nitride layer thickness correctly only when the underlying layer is silicon.
Process Note-2: Note that the deposition rate variation in tystar9 low stress nitride deposition is significant, i.e., ~25% from the center of the rear 6" boat to that of the front 6" boat. So, use at most six wafers and an additional bare Si test wafer ('S1') in each deposition to obtain good average thickness uniformity between the process wafers.
Cross Section:



13. Post-Deposition Cleaning: Nitride surface cleaning (D21-D24, S1)

Nanolab Tool: msink6
Options: msink8, msink16, msink18
1st Chemical: Piranha at 120°C
Temperature: 120°C
Time: 00:10:00
2nd Chemical: 25:1 HF (or 10:1 HF)
Temperature: Room temperature
Time: 00:05:00
Process Note: Nitride furnaces are notoriously known to deposit particles on wafer surface. Such particles, if not removed properly, may cause adhesion issues for the subsequent layer in the process, i.e., polysilicon. Cleaning with piranha and HF helps remove these particles and provides with better surface condition for the following layer.

14. Metrology: Isolation nitride initial thickness measurement (S1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Expected: 500nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: Use the test wafer ('S1') obtained in the previous step. Do not use the actual process wafers for this measurement as 'nanospec' can measure nitride layer thickness correctly only when the underlying layer is silicon.

15. Etch: Isolation nitride 49% HF etch rate test (S1)

Nanolab Tool: msink7
Options: msink16, msink18
1st Chemical: 49% HF
Temperature: Room temperature
Time: 00:10:00
Process Note: We have recently realized an enhanced 49% HF etch rate for nitride coming out of 'tystar17'. 'tystar9' low stress nitride (LSN) seems to be more resistant to 49% HF. Due to very long 49% HF release times, i.e., longer than 30min, it is important that the nitride etch rate stays below 1-2nm/min to prevent excessive polysilicon interconnect undercut. So, this test is necessary to make sure the isolation nitride will be resistant enough to 49% HF during device release at the end of the process.

16. Metrology: Isolation nitride 49% HF etch rate measurement (S1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Nitride on Silicon (10x)
Target: < 2nm/min
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Etch Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: If the target is not met, recipe changes might be needed. Note that even an enhanced nitride etch rate in 49% HF might be acceptable depending on the release time. For example, 5nm/min might be excessive for a 120min-release but acceptable for a 30min-release.

17. Test Deposition: PECVD oxide hard mask (TS1)

Nanolab Tool: oxford2
Options: oxfordpecvd3
Recipe: oxide1.rec
Gas Flows: N_2O = 800sccm, 10% SiH_4/Ar = 100sccm, PH_3/Si = 40sccm
Pressure: 900mTorr
Temperature: 350°C
RF Power: 20W HF Forward Power
Time: 00:20:00

Process Note: Use a bare silicon wafer ('TS1') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

18. Test Metrology: PECVD oxide hard mask (TS1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Dep. Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

19. Test Etch: PECVD oxide hard mask (TS1)

Nanolab Tool: centura-mxp
Options: lam6
Recipe Name: MXP-OXIDE-ETCH
Gas Flows: Ar = 150sccm, CHF_3 = 45sccm, CF_4 = 45sccm
Pressure: 200mTorr
Power: 500W
Etch Time: 00:01:00

20. Test Metrology: PECVD oxide hard mask MXP etch rate (TS1)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Etch Rate: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

21. Test Deposition: Ruthenium interconnect layer (TO1)

Nanolab Tool: randex
Options: oxfordpvd1
Gas Flows: Ar = 100-110sccm (ON)
Pressure: 6mTorr
Power: 130W (with 30W reverse power)
Stage Rotation: Rotating
Pre-Sputter: 00:15:00
Temperature: Nominally room temperature / No cooling
Time: 00:40:00
Process Note: Use a thin oxide dummy wafer ('TO1') as a test wafer for the following thickness measurement.

22. Test Deposition: Ruthenium interconnect layer PECVD oxide hard mask (TS2, TS3)

Nanolab Tool: oxford2
Options: oxfordpecvd3
Recipe: oxide1.rec
Gas Flows: N_2O = 800sccm, 10% SiH_4/Ar = 100sccm, PH_3/Si = 40sccm
Pressure: 900mTorr

Temperature: 350°C
RF Power: 20W HF Forward Power
Dep. Rate: 60nm/min (adjust if needed)
Time: 00:01:00 (adjust if needed)
Goal: 60nm
Process Note: Use a bare silicon wafer ('TS3') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.

23. Test Metrology: Ruthenium interconnect layer PECVD oxide hard mask (TS3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

24. Test PR Coating: Ruthenium interconnect layer [P1CF] (TS2)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 400nm
Recipe: T1_UV210-0.6_0.43um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

25. Test PR Exposure: Ruthenium interconnect layer [P1CF] (TS2)

Nanolab Tool: asml300
Options: None
ASML Job: NZERO1
Reticle: NZERO1
Field: P1CF - TOPLEFT
Exposure: 17mJ
Focus: 0nm

26. Test PR Development: Ruthenium interconnect layer [P1CF] (TS2)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Once
Process Note: Always run at least one dummy wafer first and visually check the developer uniformity.

27. Test PR UV-bake: Ruthenium interconnect layer [P1CF] (TS2)

Nanolab Tool: axcelis

Options: None
Program: U

28. Test Etch: Ruthenium interconnect layer PECVD oxide hard mask (TS2)

Nanolab Tool: centura-mxp
Options: lam6
Recipe Name: MXP-OXIDE-ETCH
Gas Flows: Ar = 150sccm, CHF_3 = 45sccm, CF_4 = 45sccm
Pressure: 200mTorr
Power: 500W
Etch Rate: Obtained in previous steps
Etch Time: 00:00:30 (adjust if needed)

29. Test Etch: Ruthenium interconnect layer (TS2)

Nanolab Tool: centura-met
Options: lam7
Recipe Name: OZGURLUK_RU
Gas Flows: Cl_2 = 20sccm, O_2 = 90sccm
Pressure: 10mTorr
RF Power: 130W
DC Power: 50W
Etch Time: 00:03:00 (adjust if needed)
Process Note: Make sure the etch is complete with visual and electrical check.

30. Test Metrology: Ruthenium interconnect layer (TS2)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance between pads that are not connected on the layout. If the polysilicon removal is complete, this measurement should indicate infinite resistance (‘open’).

31. Test Cleaning: Ruthenium interconnect layer PR (TS2)

Nanolab Tool: msink1
Options: msink16, msink18

1st Chemical:	1165	*2nd Chemical:*	SVC-14
Temperature:	80°C	*Temperature:*	70°C
Time:	01:00:00	*Time:*	00:30:00

32. Test Cleaning: Ruthenium interconnect layer PECVD oxide hard mask (TS2)

Nanolab Tool: msink8
Options: msink16, msink18
1st Chemical: 5:1 BHF
Temperature: Room temperature
Time: 00:01:00

33. Test Metrology: Ruthenium interconnect layer (TS2)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 5µm
Expected: 50-100nm

Result:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Dep. Rate:	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____

34. Pre-Deposition Cleaning: Chrome/Ruthenium interconnect layer (D21-D24, O1-O4)

Nanolab Tool: msink8
Options: msink7
1st Chemical: Piranha at 120°C
Temperature: 120°C
Time: 00:10:00

Nanolab Tool: msink6
Options: None

1st Chemical:	Piranha	*2nd Chemical:*	25:1 HF
Temperature:	120°C	*Temperature:*	Room temperature
Time:	00:10:00	*Time:*	00:02:00

---------- Start: 45nm-Cr / 25nm-Ru Stack (D21) ----------

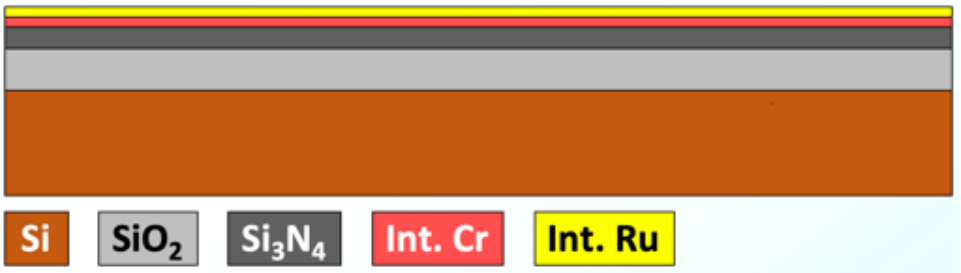
35. Deposition: Chrome/Ruthenium interconnect layer (D21, O1)

Nanolab Tool: randex
Options: oxfordpvd1
Gas Flows: Ar = 100-110sccm (ON)
Pressure: 6mTorr
Power: 130W (with 30W reverse power)
Stage Rotation: Rotating
Temperature: Nominally room temperature / No cooling

1st Target: *Chrome*
Pre-Sputter: 00:15:00
Time: 00:15:00
Goal: 45nm

2nd Target: *Ruthenium*
Pre-Sputter: 00:15:00
Time: 00:15:00
Goal: 25nm

Process Note: Use a thin oxide dummy wafer ('O1') as a test wafer for the following resistivity measurement.
Cross Section:



36. Metrology: Chrome/Ruthenium interconnect layer (O1)

Nanolab Tool: cde-resmap
Options: None
Program: 5 point
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: 45nm-Cr / 25nm-Ru Stack (D21) ----------

---------- Start: 15nm-Cr / 25nm-Ru Stack (D22) ----------

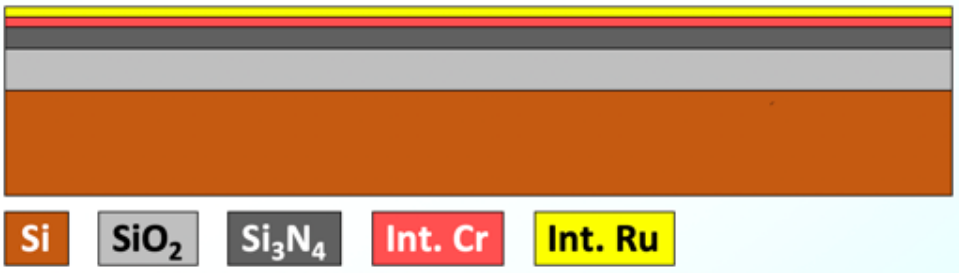
37. Deposition: Chrome/Ruthenium interconnect layer (D22, O2)

Nanolab Tool: randex
Options: oxfordpvd1
Gas Flows: Ar = 100-110sccm (ON)
Pressure: 6mTorr
Power: 130W (with 30W reverse power)
Stage Rotation: Rotating
Temperature: Nominally room temperature / No cooling

1st Target: *Chrome*
Pre-Sputter: 00:15:00
Time: 00:05:00
Goal: 15nm

2nd Target: *Ruthenium*
Pre-Sputter: 00:15:00
Time: 00:15:00
Goal: 25nm

Process Note: Use a thin oxide dummy wafer ('O2') as a test wafer for the following resistivity measurement.
Cross Section:



38. Metrology: Chrome/Ruthenium interconnect layer (O2)

Nanolab Tool: cde-resmap
Options: None
Program: 5 point
Expected: **Ω/□
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: 15nm-Cr / 25nm-Ru Stack (D22) ----------

---------- Start: 30nm-Cr / 10nm-Ru Stack (D23) ----------

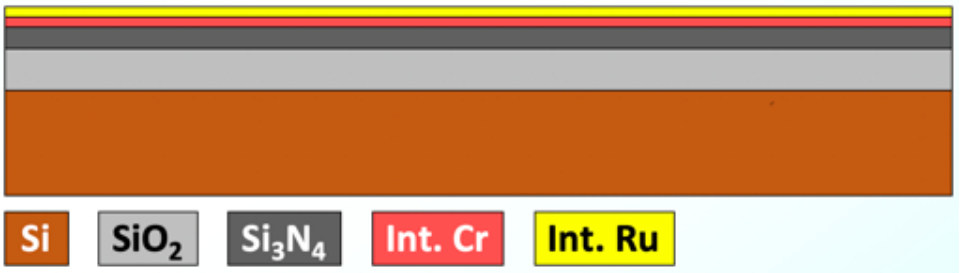
39. Deposition: Chrome/Ruthenium interconnect layer (D23, O3)

Nanolab Tool: randex
Options: oxfordpvd1
Gas Flows: Ar = 100-110sccm (ON)
Pressure: 6mTorr
Power: 130W (with 30W reverse power)
Stage Rotation: Rotating
Temperature: Nominally room temperature / No cooling

1st Target: *Chrome*
Pre-Sputter: 00:15:00
Time: 00:10:00
Goal: 30nm

2nd Target: *Ruthenium*
Pre-Sputter: 00:15:00
Time: 00:05:00
Goal: 10nm

Process Note: Use a thin oxide dummy wafer ('O3') as a test wafer for the following resistivity measurement.
Cross Section:



40. Metrology: Chrome/Ruthenium interconnect layer (O3)

Nanolab Tool: cde-resmap
Options: None
Program: 5 point
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: 30nm-Cr / 10nm-Ru Stack (D23) ----------

---------- Start: 15nm-Cr / 10nm-Ru Stack (D24) ----------

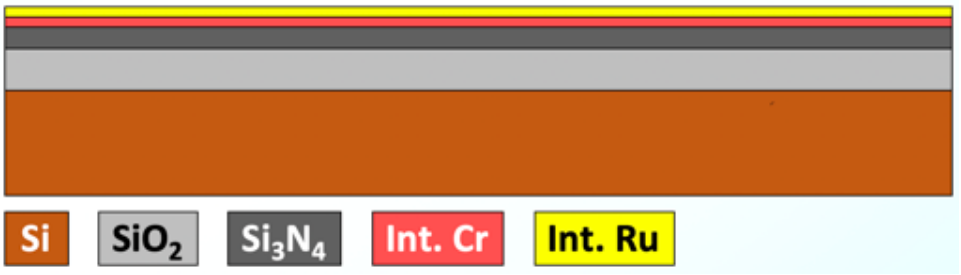
41. Deposition: Chrome/Ruthenium interconnect layer (D24, O4)

Nanolab Tool: randex
Options: oxfordpvd1
Gas Flows: Ar = 100-110sccm (ON)
Pressure: 6mTorr
Power: 130W (with 30W reverse power)
Stage Rotation: Rotating
Temperature: Nominally room temperature / No cooling

1st Target: *Chrome*
Pre-Sputter: 00:15:00
Time: 00:05:00
Goal: 15nm

2nd Target: *Ruthenium*
Pre-Sputter: 00:15:00
Time: 00:05:00
Goal: 10nm

Process Note: Use a thin oxide dummy wafer ('O4') as a test wafer for the following resistivity measurement.
Cross Section:



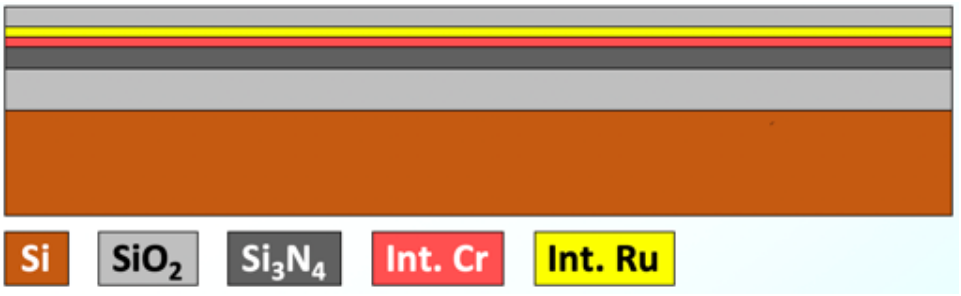
42. Metrology: Chrome/Ruthenium interconnect layer (O4)

Nanolab Tool: cde-resmap
Options: None
Program: 5 point
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: 15nm-Cr / 10nm-Ru Stack (D24) ----------

43. Deposition: Interconnect layer PECVD oxide hard mask (D21-D24, S2)

Nanolab Tool: oxford2
Options: oxfordpecvd3
Recipe: oxide1.rec
Gas Flows: N_2O = 800sccm, 10% SiH_4/Ar = 100sccm, PH_3/Si = 40sccm
Pressure: 900mTorr
Temperature: 350°C
RF Power: 20W HF Forward Power
Dep. Rate: 60nm/min (adjust if needed)
Time: 00:01:00 (adjust if needed)
Goal: 60nm
Process Note: Use a bare silicon wafer ('S2') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



44. Metrology: Interconnect layer PECVD oxide hard mask (S2)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

45. PR Coating: Interconnect layer [P1CF] (D21-D24)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 400nm
Recipe: T1_UV210-0.6_0.43um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

46. PR Exposure: Interconnect layer [P1CF] (D21-D24)

Nanolab Tool: asml300
Options: None
ASML Job: NZERO2
Reticle: NZERO2
Field: P1CF - TOPLEFT
Exposure: 16mJ
Focus: 0nm

47. PR Development: Interconnect layer [P1CF] (D21-D24)

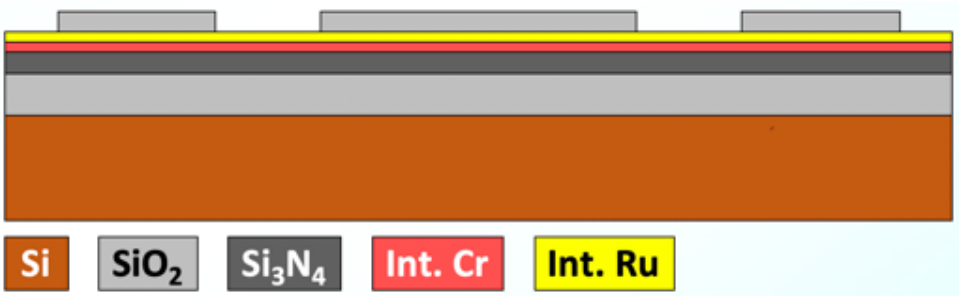
Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Once
Process Note: Always run at least one dummy wafer first and visually check the developer uniformity.

48. PR UV-bake: Interconnect layer [P1CF] (D21-D24)

Nanolab Tool: axcelis
Options: None
Program: U

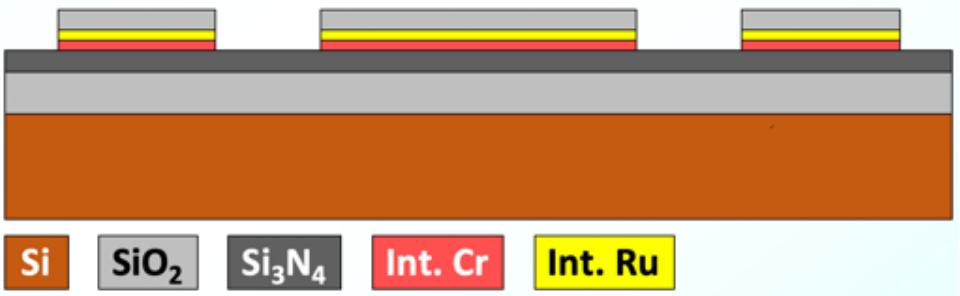
49. Etch: Interconnect layer PECVD oxide hard mask (D21-D24)

Nanolab Tool: centura-mxp
Options: lam6
Recipe Name: MXP-OXIDE-ETCH
Gas Flows: Ar = 150sccm, CHF_3 = 45sccm, CF_4 = 45sccm
Pressure: 200mTorr
Power: 500W
Etch Rate: Obtained in previous steps
Etch Time: 00:00:30 (adjust if needed)
Cross Section:



50. Etch: Interconnect layer (D21-D24)

Nanolab Tool: centura-met
Options: lam7
Recipe Name: OZGURLUK_RU
Gas Flows: Cl_2 = 20sccm, O_2 = 90sccm
Pressure: 10mTorr
RF Power: 130W
DC Power: 50W
Etch Time: 00:03:00 (adjust if needed)
Process Note: Make sure the etch is complete with visual and electrical check.
Cross Section:



51. Metrology: Interconnect layer (D21-D24)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result ('D21'): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result ('D22'): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result ('D23'): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result ('D24'): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance between pads that are not connected on the layout. If the polysilicon removal is complete, this measurement should indicate infinite resistance ('open').

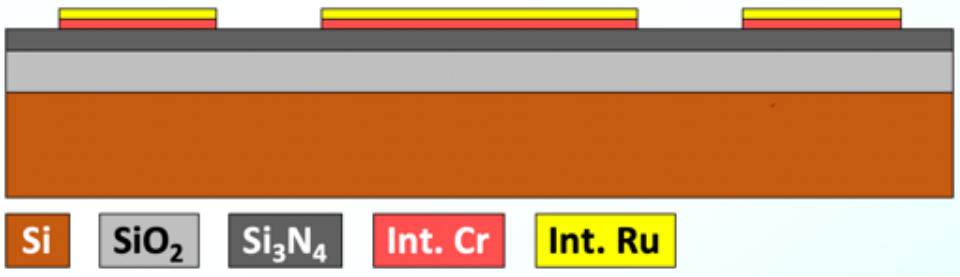
52. Cleaning: Interconnect layer PR (D21-D24)

Nanolab Tool: msink1
Options: msink16, msink18
1st Chemical: 1165 *2nd Chemical:* SVC-14
Temperature: 80°C *Temperature:* 70°C

Time: 01:00:00 *Time:* 00:30:00

53. Cleaning: Interconnect layer PECVD oxide hard mask (D21-D24)

Nanolab Tool: msink8
Options: msink16, msink18
1st Chemical: 5:1 BHF
Temperature: Room temperature
Time: 00:01:00
Cross Section:



54. Metrology: Interconnect layer (D21-D24)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 5µm
Expected: 25-100nm
Result ('D21'): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result ('D22'): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result ('D23'): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Result ('D24'): Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

55. Pre-Deposition Cleaning: Sacrificial oxide layer (D21-D24, S11-S14, TS11-TS14)

Nanolab Tool: msink1
Options: msink16, msink18
1st Chemical: SVC-14
Temperature: 40°C
Time: 00:10:00
Process Note: Include bare Si test wafers for the subsequent oxide deposition steps.

---------- Start: 80nm-thick Sacrificial LTO (D21) ----------

56. Test Deposition: Sacrificial oxide layer (TS11)

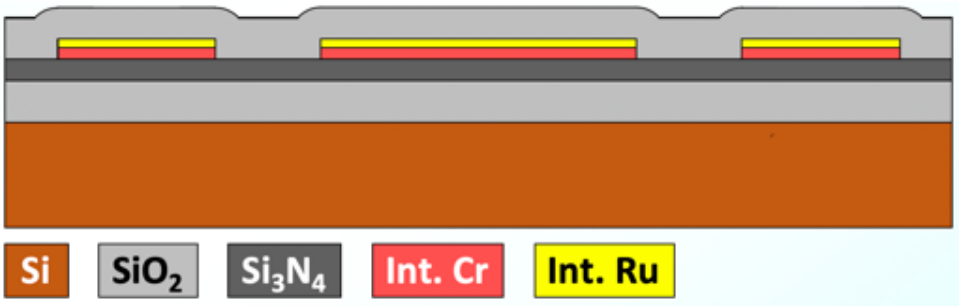
Nanolab Tool: tystar12
Options: tystar11
Recipe: 12VDLTOA
Gas Flows: O_2 = 45sccm, SiH_4 = 30sccm, PH_3/Si = 0sccm
Pressure: 200mTorr
Temperature: 450°C
Time: 00:16:00

57. Test Metrology: Sacrificial oxide layer (TS11)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

58. Deposition: Sacrificial oxide layer (D21, S11)

Nanolab Tool: tystar12
Options: tystar11
Recipe: 12VDLTOA
Gas Flows: O_2 = 45sccm, SiH_4 = 30sccm, PH_3/Si = 0sccm
Pressure: 200mTorr
Temperature: 450°C
Dep. Rate: 5.0nm/min (adjust if needed)
Time: 00:16:00 (adjust if needed)
Goal: 80nm
Cross Section:



59. Metrology: Sacrificial oxide layer (S11)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: 80nm-thick Sacrificial LTO (D21) ----------

---------- Start: 40nm-thick Sacrificial LTO (D22, D23) ----------

60. Test Deposition: Sacrificial oxide layer (TS12, TS13)

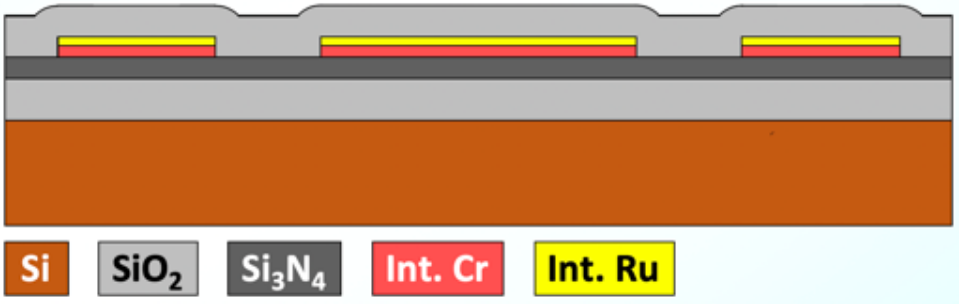
Nanolab Tool: tystar12
Options: tystar11
Recipe: 12VDLTOA
Gas Flows: O_2 = 45sccm, SiH_4 = 30sccm, PH_3/Si = 0sccm
Pressure: 200mTorr
Temperature: 450°C
Time: 00:08:00

61. Test Metrology: Sacrificial oxide layer (TS12, TS13)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

62. Deposition: Sacrificial oxide layer (D22-D23, S12-S13)

Nanolab Tool: tystar12
Options: tystar11
Recipe: 12VDLTOA
Gas Flows: O_2 = 45sccm, SiH_4 = 30sccm, PH_3/Si = 0sccm
Pressure: 200mTorr
Temperature: 450°C
Dep. Rate: 5.0nm/min (adjust if needed)
Time: 00:08:00 (adjust if needed)
Goal: 40nm
Cross Section:



63. Metrology: Sacrificial oxide layer (S12-S13)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: 40nm-thick Sacrificial LTO (D22, D23) ----------

---------- Start: 25nm-thick Sacrificial LTO (D24) ----------

64. Test Deposition: Sacrificial oxide layer (TS14)

Nanolab Tool: tystar12
Options: tystar11
Recipe: 12VDLTOA
Gas Flows: O_2 = 45sccm, SiH_4 = 30sccm, PH_3/Si = 0sccm
Pressure: 200mTorr
Temperature: 450°C
Time: 00:05:00

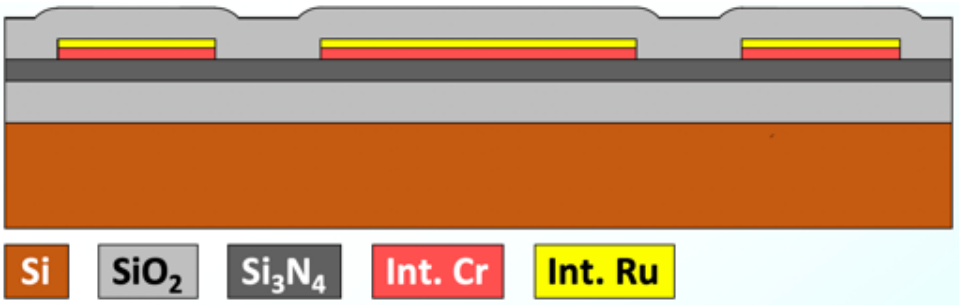
65. Test Metrology: Sacrificial oxide layer (TS14)

Nanolab Tool: nanospec

Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

66. Deposition: Sacrificial oxide layer (D24, S14)

Nanolab Tool: tystar12
Options: tystar11
Recipe: 12VDLTOA
Gas Flows: O_2 = 45sccm, SiH_4 = 30sccm, PH_3/Si = 0sccm
Pressure: 200mTorr
Temperature: 450°C
Dep. Rate: 5.0nm/min (adjust if needed)
Time: 00:05:00 (adjust if needed)
Goal: 25nm
Cross Section:



67. Metrology: Sacrificial oxide layer (S14)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

---------- End: 25nm-thick Sacrificial LTO (D24) ----------

68. PR Coating: Anchor layer photoresist [P2DF] (D21-D24)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 900nm
Recipe: T1_UV210-0.6_0.87um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

69. PR Exposure: Anchor layer photoresist [P2DF] (D21-D24)

Nanolab Tool: asml300
Options: None
ASML Job: NZERO2

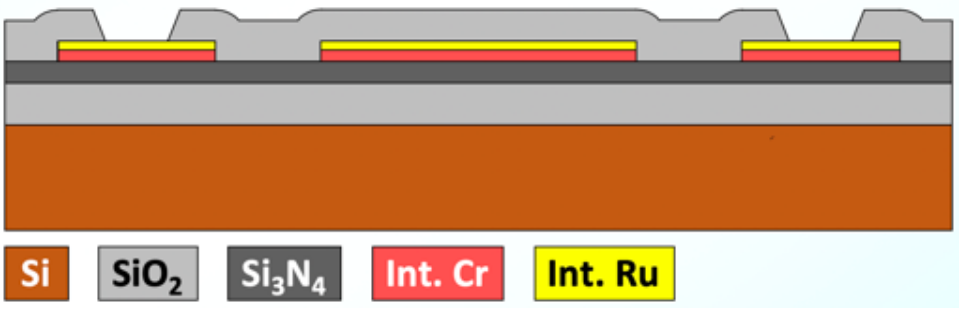
Reticle: NZERO2
Field: P2DF - TOPRIGHT
Exposure: 22mJ
Focus: 0nm
Process Note: It is important to use a high enough exposure rate for this mask to make sure the anchor openings are fully exposed as they are really tiny. Run a focus-exposure matrix (FEM) first if needed.

70. PR Development: Anchor layer photoresist [P2DF] (D21-D24)

Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Twice
Process Note-1: Always run at least one dummy wafer first and visually check the developer uniformity.
Process Note-2: Develop twice for dark field masks to make sure all residual photoresist in the patterned area gets removed.

71. Etch: Anchor layer sacrificial oxide spacer (D21-D24)

Nanolab Tool: centura-mxp
Options: lam6
Recipe Name: MXP-OXIDE-ETCH
Gas Flows: Ar = 150sccm, CHF_3 = 45sccm, CF_4 = 45sccm
Pressure: 200mTorr
Power: 500W
Etch Rate: Obtained in previous steps
Etch Time: 00:01:00 (adjust if needed)
Cross Section:



72. Cleaning: Anchor layer PR (D21-D24)

Nanolab Tool: msink1
Options: msink16, msink18

1st Chemical:	1165	*2nd Chemical:*	SVC-14
Temperature:	80°C	*Temperature:*	70°C
Time:	01:00:00	*Time:*	00:30:00

73. Metrology: Anchor layer (D21-D24)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 5µm
Expected: 25-80nm

Result ('D21'):	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Result ('D22'):	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Result ('D23'):	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____
Result ('D24'):	Mid:____	Top:____	Bottom:____	Right:____	Left:____	Avg:____

74. Pre-Deposition Cleaning: Ruthenium structural layer (D21-D24, O5, S3)

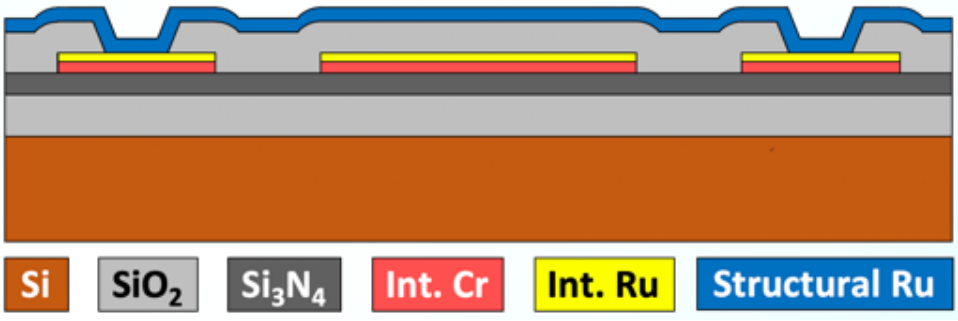
Nanolab Tool: msink1
Options: msink16, msink18

1st Chemical:	1165	*2nd Chemical:*	SVC-14
Temperature:	80°C	*Temperature:*	70°C
Time:	01:00:00	*Time:*	00:30:00

75. Deposition: Ruthenium structural layer (D21-D24, O5)

Nanolab Tool: randex
Options: oxfordpvd1
Gas Flows: Ar = 100-110sccm (ON)
Pressure: 6mTorr
Power: 130W (with 30W reverse power)
Stage Rotation: Rotating
Pre-Sputter: 00:15:00
Temperature: Nominally room temperature / No cooling

1st Sput. Time: 00:15:00
1st Rest Time: 00:10:00 (Power = 0W)
2nd Sput. Time: 00:15:00
2nd Rest Time: 00:10:00 (Power = 0W)
3rd Sput. Time: 00:15:00
Process Note: Use a thin oxide dummy wafer ('O5') as a test wafer for the following thickness measurement.
Cross Section:



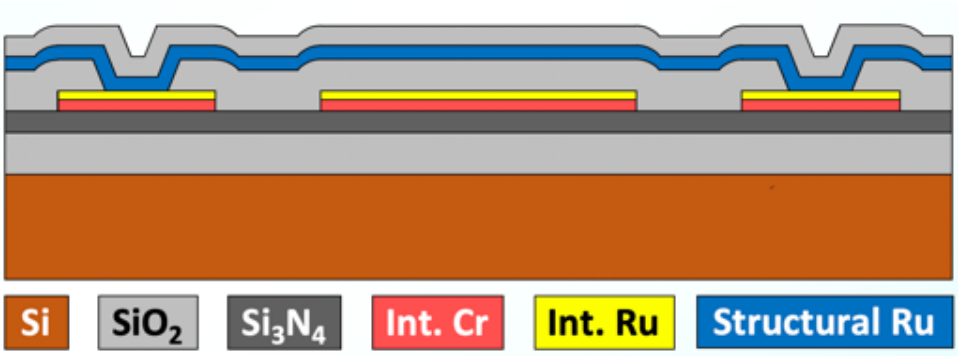
76. Metrology: Ruthenium structural layer (O5)

Nanolab Tool: cde-resmap

Options: None
Program: 5 point
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

77. Deposition: Ruthenium structural layer PECVD oxide hard mask (D21-D24, S3)

Nanolab Tool: oxford2
Options: oxfordpecvd3
Recipe: oxide1.rec
Gas Flows: N_2O = 800sccm, 10% SiH_4/Ar = 100sccm, PH_3/Si = 40sccm
Pressure: 900mTorr
Temperature: 350°C
RF Power: 20W HF Forward Power
Dep. Rate: 60nm/min (adjust if needed)
Time: 00:01:00 (adjust if needed)
Goal: 60nm
Process Note: Use a bare silicon wafer ('S3') as a test wafer for the following thickness measurement. 'nanospec' can measure oxide layer thickness correctly only when the underlying layer is silicon.
Cross Section:



78. Metrology: Ruthenium structural layer PECVD oxide hard mask (S3)

Nanolab Tool: nanospec
Options: nanoduv, ellips1, ellips2
Program: Thin Oxide on Silicon (10x)
Thickness: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

79. PR Coating: Ruthenium structural layer [P3CF] (D21-D24)

Nanolab Tool: picotrack1
Options: svgcoat6
Resist Type: UV210
Thickness: 400nm
Recipe: T1_UV210-0.6_0.43um
Temperature: Prox. (0.6mm) 5sec @ 90°C (Pre) / Prox. (0.6mm) 60sec @ 130°C (Post)
Process Note: Always run at least one dummy wafer first and visually check the resist uniformity.

80. PR Exposure: Ruthenium structural layer [P3CF] (D21-D24)

Nanolab Tool: asml300
Options: None
ASML Job: NZERO2
Reticle: NZERO2
Field: P3CF - TOPLEFT
Exposure: 15mJ
Focus: 0nm

81. PR Development: Ruthenium structural layer [P3CF] (D21-D24)

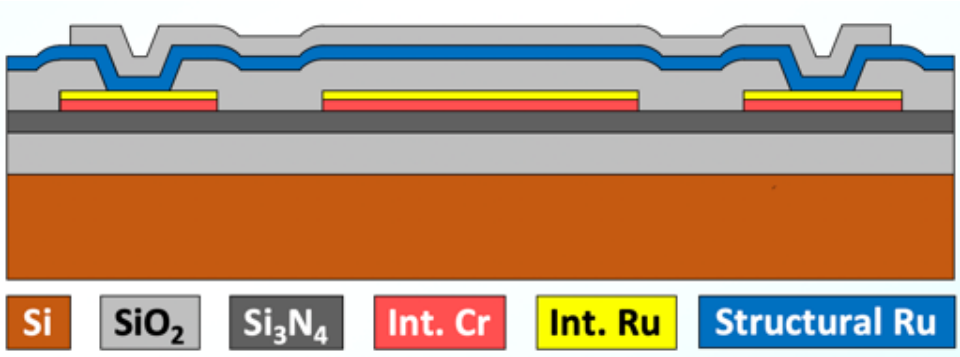
Nanolab Tool: picotrack2
Options: svgdev6
Developer: MF26A
Recipe: T2_PEB130C90s_MF26A45s
Temperature: Prox. (0.6mm) 90sec @ 130°C
Dev. Count: Once
Process Note: Always run at least one dummy wafer first and visually check the developer uniformity.

82. PR UV-bake: Interconnect layer [P3CF] (D21-D24)

Nanolab Tool: axcelis
Options: None
Program: U

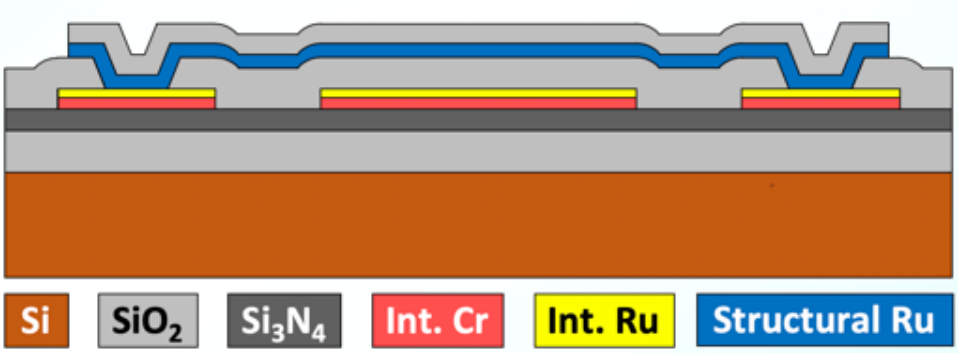
83. Etch: Ruthenium structural layer PECVD oxide hard mask (D21-D24)

Nanolab Tool: centura-mxp
Options: lam6
Recipe Name: MXP-OXIDE-ETCH
Gas Flows: Ar = 150sccm, CHF_3 = 45sccm, CF_4 = 45sccm
Pressure: 200mTorr
Power: 500W
Etch Rate: Obtained in previous steps
Etch Time: 00:00:30 (adjust if needed)
Cross Section:



84. Etch: Ruthenium structural layer (D21-D24)

Nanolab Tool: centura-met
Options: lam7
Recipe Name: OZGURLUK_RU
Gas Flows: Cl_2 = 20sccm, O_2 = 90sccm
Pressure: 10mTorr
RF Power: 130W
DC Power: 50W
Etch Time: 00:03:00 (adjust if needed)
Process Note: Make sure the etch is complete with visual and electrical check.
Cross Section:



85. Test Metrology: Ruthenium structural layer (D21-D24)

Nanolab Tool: probe8
Options: Wentworth
Expected: Electrically open (infinite resistance)
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____
Process Note: This check entails measuring the electrical resistance between pads that are not connected on the layout. If the polysilicon removal is complete, this measurement should indicate infinite resistance ('open').

86. Test Cleaning: Ruthenium structural layer PR (D21-D24)

Nanolab Tool: msink1
Options: msink16, msink18

1st Chemical:	1165	*2nd Chemical:*	SVC-14
Temperature:	80°C	*Temperature:*	70°C
Time:	01:00:00	*Time:*	00:30:00

87. Test Metrology: Ruthenium structural layer (D21-D24)

Nanolab Tool: alphastep
Options: dektak
Meas. Range: 5µm
Expected: 100-110nm
Result: Mid:____ Top:____ Bottom:____ Right:____ Left:____ Avg:____

88. Dicing (D21-D24)

Nanolab Tool: disco

Options: Manual dicing with a diamond scriber
Process Note: Sometimes dies fly away and get lost in the tool during dicing. Coating wafer with photoresist before starting dicing is a good idea to avoid this.

---------- Start: Rapid Thermal Anneal (RTA) ----------

89. Post-Processing: Rapid thermal anneal (RTA)
Nanolab Tool: rtp3
Options: None
Recipe: Ozgurluk_1000C1min
Process Note: Perform RTP with only N_2 flowing. Noe that the recipe should first stabilize around 450°C before ramping up to 900°C - 1099°C. Use a rise/fall time within the 15-30sec interval. Too much RTP (this is a vague definition but usually means combination of RTP temperature and duration) may degrade the ruthenium layers and also put excessive stress on the beams causing them to break.

---------- End: Rapid Thermal Anneal (RTA) ----------

---------- Start: Localized Annealing ----------

90. Post-Processing: Clear sacrificial layer atop resonator pads
Nanolab Tool: msink16 & msink18
Options: None
Chemical: 49% HF
Temperature: Room temperature
Time: 00:00:10
Process Note-1: This step only removes the sacrificial layer atop resonator pads and does not fully release the devices.
Process Note-2: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

91. Post-Processing: Localized Annealing
Tool: Lakeshore
Options: Wentworth, MMR
Temperature: Room temperature
Pulse Voltage: 1V
Pulse Width: 10ms
Process Note: Make sure the Lakeshore probes are not bent and functional. Also, check the measurement setup, i.e., bias tees, cables etc., with a known working device in advance.

---------- End: Localized Annealing ----------

92. Release: Clean baskets, dishes, tweezers, and glass beakers
Nanolab Tool: msink16 & msink18

Options: None
Chemical: Piranha (Sulfuric Acid : Hydrogen Peroxide = 1 : 1)
Temperature: Set by the activated chemical
Time: 00:10:00
Process Note: Rinse all equipment with water before and after the piranha clean.

93. Release: Metal clean dies

Nanolab Tool: msink16 & msink18
Options: None
Chemical: SVC-14
Temperature: 70°C
Time: 00:10:00
Process Note: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) before and after the piranha clean.

94. Release: Main 49% HF release

Nanolab Tool: msink16 & msink18
Options: None
Chemical: 49% HF
Temperature: Room temperature
Time: 00:02:00
Process Note-1: This step fully releases the devices.
Process Note-2: Agitate during this step to remove the bubbles formed during HF etch.
Process Note-3: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) after this step.

95. Release: Metal clean dies after main 49% HF etch

Nanolab Tool: msink16 & msink18
Options: None
Chemical: SVC-14
Temperature: 70°C
Time: 00:10:00
Process Note: Rinse the dies placed in a Teflon basket in Teflon dishes filled with DI water three times (each 1min) before and after the piranha clean.

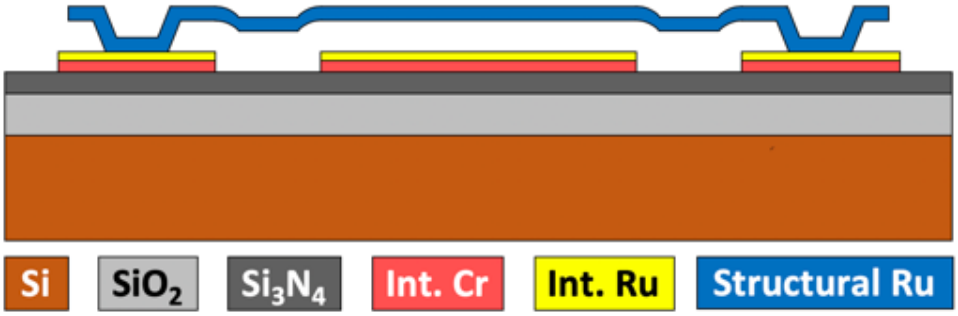
96. Release: Methanol rinse

Nanolab Tool: msink16 & msink18
Options: None
Chemical: Methanol
Temperature: Room temperature
Time: 00:03:00
Process Note-1: Rinse the dies placed in a Teflon basket in Teflon dishes filled with methanol three times (each 1min) after this step. Methanol should completely replace DI water at the end of this step.

Process Note-2: It is extremely important that the dies never dry out between this step and the following critical point drying step to prevent stiction. Transfer dies to 'cpd' in a container filled with methanol.

97. Critical Point Drying

Nanolab Tool: cpd
Options: primaxx
Temperature: Set by the tool.
Purge Time: 00:25:00 (Setting '5')
Process Note: Make sure the methanol level in 'cpd' fully covers the dies before closing the chamber.
Cross Section:



98. Probe Station Testing

Tool: Lakeshore
Options: Wirebonding, MMR
Temperature: Room temperature
Vacuum: <100µTorr
Process Note: Make sure the Lakeshore probes are not bent and functional. Also, check the measurement setup, i.e., bias tees, cables etc., with a known working device in advance.