# Ring-Amplification Technique for Bio-Signal LNA Designs

*Zhiyang Song*
*David Allstot, Ed.*

Electrical Engineering and Computer Sciences
University of California at Berkeley

Technical Report No. UCB/EECS-2015-82
http://www.eecs.berkeley.edu/Pubs/TechRpts/2015/EECS-2015-82.html

May 13, 2015

# Ring-Amplification Technique for Bio-Signal LNA Designs

by

Zhiyang Song

A capstone Report Submitted in Partial Fulfillment of

the Requirements for the Degree of

Master of Engineering

in

Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Review Committee in Charge:

Professor David J. Allstot, Capstone Advisor

Professor Jan M. Rabaey

Spring 2015

University of California, Berkeley College of Engineering

# MASTER OF ENGINEERING - SPRING 2015

**Electrical Engineering and Computer Sciences**

**Integrated Circuits**

## Ring-Amplification Technique for Bio-Signal LNA Designs

**Zhiyang Song**

This **Masters Project Paper** fulfills the Master of Engineering degree requirement.

Approved by:

1. Capstone Project Advisor:

Signature: _____ Date _____

Print Name/Department:

David J. Allstot/Electrical Engineering and Computer Sciences

2. Faculty Committee Member #2:

Signature: _____ Date _____

Print Name/Department:

Jan M. Rabaey/Electrical Engineering and Computer Sciences

# Abstract

Low power wireless medical electronic design is a heated research topic due to the development of remote medical diagnosis systems and long-term treatment assistances. In general, such medical devices contain bio-signal sensor that monitor the health status of a patient or health-conscious person. Our main goal is to design an LNA that is suitable for amplifying bio-signals in low-power remote sensing devices. In this work, the business strategy and the IP strategy is being studied and presented.

Ring-amplification technique is a novel amplifier design approach, which has the potential to achieve high gain with minimal power dissipation. The motif behind applying ring-amplification technique to low-power LNA design is that ring-amplifier has the potential to achieve high gain with low power dissipation as well as a relatively simple structure. This work reviews the current status of ring-amplifier design, as well as explores the ring-amplifier design process. The original ring-amplifier approach is not suitable for low-noise amplifier design due to its single-ended structure, therefore effort is being made to modify the ring-amplifier structure to make the amplifier suitable for employing flicker noise cancellation techniques. The eventual result of this work, the differential input ring-amplifier employing chopper stabilization, which achieved closed-loop gain of 63.93dB, THD -78dB, UGB of 12MHz and a positive phase margin which indicates the stability of the ring-amplifier. At 10Hz the output noise voltage density is $120uV/(Hz)^{1/2}$, which is approximately an order of magnitude noise reduction at low frequencies, compared to the simple ring-amplifier.



**Keywords:** Bio-signal; Low Noise Amplifier; Ring Amplifier; Low Power; Low Frequency.

# Table of Contents

**1. Problem Statement** ..... **4**

**2. Business Strategy for Low-Power LNA (Low-Noise Amplifier)** ..... **5**

2.1. Introduction ..... 5
2.2. Identification of Industry ..... 6
2.3. Potential Impact to the Industry ..... 7
2.4. Threat of Alternative Technology ..... 8
2.5. Competition in the Industry ..... 9
2.6. Potential Buyers, Suppliers, and End Users ..... 10
2.7. Power of Buyers and Suppliers ..... 11
2.8. Basic Marketing Strategy ..... 12
2.9. Social Trends ..... 13
2.10. Technological Trend ..... 13
2.11. Economic Trends ..... 14
2.12. Regulatory Trends ..... 15
2.13. Business Strategy to Cope with Contemporary Trends ..... 15

**3. Intellectual Property Strategy for Ultra-low Power LNA** ..... **17**

3.1. Introduction ..... 17
3.2. Patentability of Our Design ..... 17
3.3. Existing Similar Patent ..... 18
3.4. Possible Similarity and Distinction ..... 19
3.5. Alternative Options and Potential Risks ..... 20

**4. Technical Contributions** ..... **22**

4.1. Overview ..... 22
4.2. Literature Review ..... 23
4.2.1. Common-Source Fully-Differential Amplifier ..... 24
4.2.2. Ring-Amplifier ..... 25
4.3. Methods and Materials ..... 29
4.3.1. Ring Amplifier Design Process ..... 29
4.3.2. Adjustments and Improvement ..... 33
4.4. Results and Discussion ..... 37

**5. Concluding Reflections** ..... **47**

## 1. Problem Statement

Low power wireless medical devices are currently in the spotlight due to the development of remote medical diagnosis systems and long-term treatment assistances. In general, such medical devices contain bio-signal sensor that monitors the health status of a patient or health-conscious person. The output of the sensor is extremely weak for further processing and susceptible to noise. Thus, a low-noise amplifier is connected to the sensor to amplify the original input signal while minimizing the effect of noise. The specification of a low-noise amplifier (LNA) determines the quality of the processed signal.

Our main goal is to design an LNA that is suitable for implantable bio-signal acquisition systems. We primarily focus on the implantable medical system monitoring the electrical signal of a person's heart. The LNA provides enough voltage gain to amplify the signals while reducing the noise contamination significantly.

In addition, its power consumption is minimized to enhance the lifespan of the whole system. Currently, a bio-signal acquisition system's overall power consumption is dominated by the low-noise amplifier. The other module in the bio-signal acquisition system only consumes less than 1uW each, while a typical LNA consumes more than 10uW. By reducing the power consumption of the LNA, the device can maintain its performance or longer period of time.

## 2. Business Strategy for Low-Power LNA (Low-Noise Amplifier)

### 2.1. Introduction

According to *Deaths: Final Data for 2013*, a recent statistical report issued by Centers for Disease Control and Prevention, life expectancy of people at birth in the United States in 1950 is only 68.2 years (Center for Disease Controls and Prevention). In contrast, life expectancy at birth in 2013 is 78.8 years. Nowadays, people are expected to live almost 10 years longer than people living the middle of 1990s. Although life expectancy at birth has been steadily increasing for the past years, people are still exposed to danger of chronic diseases, such as diabetes, hypertension, and arrhythmia.

*Deaths: Final Data for 2013* shows that the leading cause of death in 2013 is diseases in heart. Moreover, diabetes is the seventh leading cause of death (Center for Disease Controls and Prevention). These chronic diseases have relevant bio-signals that indicate health status of patients. For instance, blood sugar level of a person who suffers in diabetes indicates when the person needs to inject insulin. If real-time monitoring of bio-signals is possible, doctors are able to anticipate urgent situations so that more lives can be saved. Recently, wearable or implantable wireless medical devices are developed to detect bio-signals from a patient and send data remotely to other devices.

The goal of our Capstone Project is to design a low-noise amplifier (LNA) with very low power consumption. This LNA is a part of the bio-signal acquisition system described above. When a sensor first detects a signal, the signal is extremely weak to perform subsequent process. Thus, an LNA needs to amplify the signal without adding significant noise. Most importantly, the LNA should consume as little power as possible to maximize lifespan of the medical device.

Our LNA is expected to consume less than 10μW and can minimize its power consumption depending on how the data is going to compressed in the next module called compressed sensing block.

Section 2.2 explains our business strategy focusing on industry analysis, market analysis, and relevant trends that may affect the strategy to productize our product. The paper identifies the industry and market to figure out the best way to present the product in the world. With regards to commercialization of the capstone project, we take into account various trends to sharpen our strategy.

## 2.2. Identification of Industry

We are mainly engaged in the activity of designing an LNA for ultra-low power and long-durability applications. Our main target customers will be in the business of medical implantable devices for real-time monitoring. We identify ourselves as the industry of semiconductor & circuit manufacturing and design based on the IBIS World Industry Report (Ulama). Since the industry has various facets, we need to identify ourselves in a more specific area of the industry. We specify our area as designing integrated microcircuits.

In the integrated circuit industry, there are three main types of companies. The first type is a company that both designs and manufactures microcircuits, such as Intel Corporation or Advanced Micro Devices AMD. Also, there is a company that provides manufacturing services to other companies, often referred to as a foundry, such as Global Foundries or Taiwan Semiconductor Manufacturing Corporation TSMC. The third type is an entity that only designs ICs, not actually manufacturing chips. The term, fabless, is used to describe a company that does not own a foundry for the production of wafers (Ulama). The emergence of fabless is due to the

increasingly high capital barrier in the fabrication segment of the semiconductor industry (Chen). The fabless business model requires much lower initial capital barrier and has higher return of invested capital.

The main activity of the fabless is using a design platform provided by Electronic Design Automation EDA companies. Cadence Design System is the most popular platform for designing IC. We design a circuit schematic and simulate for its functionality and performance. The circuit schematic is only an abstract level of circuit representation. It is not the actual blueprint of device manufacturing. The next procedure is to design the layout of the device. The layout includes more detailed information of how the microcircuit device is manufactured. The layout file is what needs to be transferred securely to the foundries so the deisgn can be fabricated and sent back to the designers for post-silicon testing. The procedure is often referred to as tape-out.

Since we mainly target our product application at the medical implantable devices, the performance of the medical devices industry also greatly affects the profitability of our product. Our potential customers will come from this industry. This industry includes manufacturers of electro-medical and electrotherapeutic apparatuses, such as magnetic resonance imaging equipment, medical ultrasound equipment, pacemakers, hearing aids, electrocardiographs and electro-medical endoscopic equipment (Porter). The revenue of this industry has seen steady growth of around 5 percent per year over the past 4 years. This makes our industry more lucrative.

## 2.3. Potential Impact to the Industry

Our main goal is to provide a reliable solution for remote health monitoring. Patients with chronic illnesses have to visit the hospital on regular basis; also this inconvenient practice may

overlook short-term variability of the patients' health status. Currently the main problem with remote real-time monitoring devices is power dissipation. In order to make these devices last longer, conventional circuit design techniques are impractical. For these applications, special circuit design methods need to be employed to suit the purpose of ultra-low power dissipation.

In electronic sensing devices, analog components consume much more energy than digital components. In our case, the digital module on which we will deploy our design is able to operate at as low as 22nW per channel (Allstot). However, the LNA, which is the interface between the sensor and this digital module, can only operate at as low as microwatts of power dissipation. Therefore if we can bring to the table a design that reaches the sub-microwatt region, implantable devices for remote health monitoring are much more practical.

## 2.4. Threat of Alternative Technology

External health monitoring is the most threatening alternative technology that we are facing. With the advent of more compact and powerful mobile platforms, wearable devices are booming in performance as well as popularity. It is also a much safer application compared to surgical operations that is a required step for implantable healthcare devices.

However the advantage of implantable devices should not be neglected. Implantable devices guarantee more accurate results compared to external sensing. External monitoring is prone to environmental variability such as humidity and temperature. Implantable devices are more reliable because human bodies tend to maintain temperature and humidity. Implantable monitoring devices can also interact with other implantable medical devices, such as pacemakers.

## 2.5. Competition in the Industry

The wireless medical device market is at the verge of experiencing rapid growth in the near future. In addition, we are not in the position where the dependence on the suppliers has much force on the profitability of the industry. Our suppliers are EDA companies that provide IC and layout design platforms. That is, in terms of a fabless, we do not need to worry much about the manufacturing service, or the "foundry", which is far more capital intensive and supplier dependent.

The driving force here is rivalry. Many large companies are beginning to pay more attention to the wireless medical device market, such as Analog Devices ADI, Qualcomm, and Philips. The core of competition is expected to be the R&D of the technology and innovative approaches to resolve the issue of long-lasting miniature device suitable for implantation. Because the industry is demanding and tends to favor more advanced technology, the profitability of the industry is undermined.

The main strategy that we adopt to counteract the threat from rivals is to focus on novel design techniques. For instance, Texas Instruments is taking effort to improve the power consumption of its DSP products to suit the purpose of ultra-low power applications (Ulama). However, in a severely energy constrained sensor, Compressed Sensing eliminates the need for digital signal processing (Allstot). New design methodologies tend to undercut the advantage of established rivals such as TI and ADI, who take advantage from their well-established analog design solutions.

In conclusion, the main tactic to tackle rivalry — the main threat in our go-to-market strategy — is to aim at new and unconventional design techniques for ultra-low power applications.

## 2.6. Potential Buyers, Suppliers, and End Users

As we have mentioned briefly in the section 2.1, our buyers are wearable or implantable medical device manufacturing companies. We are targeting these companies because their products could benefit from ultra-low power LNAs to maximize their lifespan. It will be a laborious task for a user to charge or replace battery everyday. If a device is implanted in a person's body, changing a battery frequently is not a feasible option. Consequently, the companies value electronic components with low power consumption. Our product will be one of their interests. We target the potential buyers of our LNA at the medical devices design and manufacturers, and they can integrate the chips with other parts of medical devices.

Aside from our potential buyers, we also need to identify who our end users are. Our end users are people who are willing to utilize medical devices employing our LNA design. The primary target-users would be patients suffering from chronic diseases. In their cases, real-time monitoring is a great benefit in order to prevent life-threatening emergencies. We predict that health-conscious people are also our potential end users because there has been a prevailing trend of attention to healthy diet and lifestyle. Some wearable medical devices are able to record heartbeat and blood pressure. People who want to keep track of their health status could benefit from those devices.

There are two main suppliers for our product: Computer-Aid Design software company and semiconductor foundry. Specifically, we need a subset of CAD software called Electronic Design Automation software to design LNA circuits. As we have mentioned in section 2.2, we will adopt fabless manufacturing model to produce LNA chips. In other words, semiconductor foundry is required to provide service of fabricating our chip design.

## 2.7. Power of Buyers and Suppliers

According to Michael E. Porter's *The Five Competitive Forces That Shape Strategy*, it is essential to analyze power of buyers and suppliers and reshape them in our favor to be competitive in the market (Porter). Fastidious customers can influence on the product's price and induce hyper-competition against rivals. On the other hand, powerful supplier can limit our profitability by charging higher price.

In our case, power of buyers is moderate. The United States medical device market is currently the largest in the world with the size of $110 billion (PRNewswire). It is expected to reach $133 billion by 2016 (PRNewswire). In addition, there are almost 6,500 medical device companies in the United States. The reason why the market has been growing rapidly is that more people are eager to buy medical devices to treat chronic diseases. For instance, Emily Krol, health and wellness analyst, says that there is a large market of consumers for products and services specifically aimed to treat diabetes (PRNewswire). Although there are a plenty of buyers in the market, the other factor makes the power of buyers strong. An LNA chip, which is a part of semiconductor chip, is standardized and there are many competitors in the world. Thus, buyers have few switching costs.

In contrast, supplier power is almost negligible and cannot affect our marketing strategy. Buying CAD software from the company is merely one-time expense. After the purchase, we can keep using the software to design circuits. The other supplier, semiconductor foundry, experiences high competition in its own field, and the process of IC manufacturing and fabrication is a standardized process (Ulama). As a result, we can switch easily among vendors, weakening the power of suppliers.

## 2.8. Basic Marketing Strategy

Marketing mix is a fundamental business tool to sharpen marketing strategy. It is associated with the four P's: product, price, promotion, and place. Our product has to have the advantages on power consumption and chip area over other competitors. Our main marketing target would be medical device company that demands such specifications. Without differentiating technology, it would be difficult to find buyers. In order to mitigate the power of buyers, we need to make sure that our LNA chips could outcompete alternative products in the market. In other words, if our chips can make a medical device that lasts twice longer than other chips, our position in the market could be secured. We focus on wearable or implantable medical device segment because this segment is sensitive to power consumption.

Price of our products should not be high unless there is a significant technological advantage over alternative products. There is no guarantee for the affluence of our potential buyers and end-users, thus setting a high profit margin may hamper the sale of our product. Medical device companies will try to minimize the cost for producing their products so as to improve market share of their products. In addition, the cost of the IC is subject to the effect of scale, which means the cost for each product is reduced as the scale of production increases. Therefore an effective approach to cut-down the cost of our product is to seek for larger market share.

Since our main type of transaction is business-to-business B2B, there are not various options for promoting the products. As a new entrant, our primary strategy is to create a solid network with our partners in the business. To prove the product's reliability and technological advantages, we should hand out the samples of our LNA chips to the potential customers for free.

Although this strategy may weaken our financial status in a short term, it will help us secure the customers in a long term.

Because we deal with B2B transactions, there is no need for physical stores for distribution. The natural option is to conduct promotion campaigns directly targeted at enterprises. This strategy implies that the promotion and quality of the products are very important factors for our sales. As we expand the business, we may sell the products to different markets other than medical device market to increase profitability.

## 2.9. Social Trends

As discussed in section 2.7, the U.S. society tends to pay more and more attention to health care. And the *Death: Final Data of 2013* reports the diseases in heart the dominant factor of death among diseases (Center for Diseases Control and Prevention). This fact indicates the mitigation of the buyers' force, according to Porter's five forces theory (Porter). Our direct customers are wireless medical device companies, who will embed our design in their products. We identify the end-users of our product as patients who are using these implantable devices. In addition, people are becoming increasingly conscious of their well-being, which implies that there is a great potential market for real-time health monitoring. In fact, CNBC is reporting a rapid growth of wireless medical device in the United States.

## 2.10. Technological Trend

As mentioned in previous section, social trends are opening a potential market for real-time health monitoring market. In addition, the rapid development of Information technology IT, such as the advances in video communication, wireless connectivity to the Internet, and the

increasingly popular web-assisted self-learning, is contributing greatly to the feasibility of exploiting this market.

Meanwhile, what plays a more important role in our product is low power IC design and manufacturing. Moore's Law, which was proposed in 1965, predicted the roadmap of the technological and economical advance of Integrated Circuit industry (Schaller). However, as the semiconductor industry proceeds deeper into the submicron region, it is increasingly difficult for the industry to advance the technology at the pace that the Moore's law had successfully forecasted for the past 40 years.

Since leakage power is becoming the dominant aspect of power dissipation in IC components, low power design technology is becoming the main concern during contemporary IC design. The influence of this industrial trend is both challenging us and exposing us to opportunities. More competitions might be generated from academia due to research but we can also make use of lately published papers to help with our low power design. In other words, the field is moving forward and refreshing itself quickly and we are traveling in a technolgy highway, exposed to both risks and opportunities.

## 2.11. Economic Trends

As we have discussed in the industry section, Integrated Circuit industry has high capital barriers for the fabrication segment, though fabless companies experience relatively lower barriers. Economic aspects play important roles in the industry. The Gross Domestic Product, GDP, growth rate in US has also increased in the past years (The World Bank). And the termination of Quantitative Easing by the US government is attracting a large amount of hot money or refugee capital from the rest of the world to the US, which is good news for new

entrants in this industry. Combined with the fact that the semiconductor industry is reaching the physical limitation of how small a device can be made, R&D investment in unconventional IC design techniques are attractive to investors targeting at new applications such as the wireless medical devices market.

## 2.12. Regulatory Trends

The U.S. government has well developed regulations in health care field. In the U.S. regulations on electronics targeted at the medical industry and automotive industry has been strict, thus we should be extremely cautious with our eventual implementation such that the performance of our prototype tally with the regulatory specifications. Also, since we are design a product that would be implanted into an individual's body and collect data for a long time, new regulations about this might appear in the future, which has not been seen. Regardless of this factor of potential change, regulatory factors are negligible in our business.

## 2.13. Business Strategy to Cope with Contemporary Trends

As mentioned in the previous section, social and economic trends are favoring our business, regulatory factors do not have strong influences on us, and the rapid development of the core technologies relevant to the industry is putting us into both risks and opportunities.

Our strategy on these trends can be concluded as follow. We need to catch the opportunity provided by the rapid growth of the wireless medical device industry and the recent uprising trends of US economy, which means we need to act quickly. More importantly, we have to do well in the technology part to avoid being outcompeted by rivalries in the industry. On the technological aspect of the strategy, we should explore on novel design methodologies to gain

technological edges over competitors. Thus, keeping firm connection with academia is also a crucial concern in our strategy.

# 3. Intellectual Property Strategy for Ultra-low Power LNA

## 3.1. Introduction

In July 1959, Robert Noyce was granted the first integrated circuit patent for his innovative idea, and the actual functional prototype was fabricated in May 1960 (Computer History Museum). After his patent, the number of patents related to IC research and design has grown exponentially over the past half century. Protection of intellectual property is a sensitive issue in the realm of IC research and design because excessive time and resources are required to make a significant breakthrough. In reality, the situation of IP protection in the industry is unsatisfactory. SEMI has reported that over 90% of the semiconductor R&D, design and manufacturing entities have experienced certain extent of IP violations (SEMI). To avoid such situation later on, we will discuss the patentability of our design and scrutinize other alternatives.

## 3.2. Patentability of Our Design

An Integrated Circuit is a product that includes at least one active element, in which majority of the components and interconnects are formed on a single piece of material to perform a desired function (World Intellectual Property Organization). Obviously the property of our product matches with this definition, thus we should attempt to patent our design as an IC product.

First, it is beneficial to clarify key technologies of interest in our project before discussing the patentability of our design. The key features of our design include two aspects: ultra-low power consumption and high signal-to-noise ratio. To achieve ultra low power design, we will employ techniques to reduce the DC bias current of the circuit, such as sub-threshold

design. To achieve the goal of high signal-to-noise ratio, we will use techniques such as chopper stabilization method and low-pass filter.

Here, we discuss some first order criteria for determining patentable ideas related to IC design. These criteria include usefulness of the design, novelty of the concept, the extent of innovation or differentiation compared to other designs aiming at the same functionality, the extent of clarity of the design description, and the boundary of the scope of the definition (Bellis). There are plenty of applications that we can employ our low-noise amplifier (LNA), such as digital interface to the external off-chip components (Enz 335). Thus if that we can meet all the required specifications, the usefulness of the design is unlikely to be contested. However, we are utilizing several existing LNA design techniques to design our prototype, so the extent of differentiation among counterparts is unlikely to be high. Therefore, we can conclude that it is unlikely for us to patent our design.

### 3.3. Existing Similar Patent

It was difficult to find a patent that is closely related to our design. The main reason was that we combined existing technologies to build up our LNA. After searching rigorously, we found a patent named Mobile Wireless Communications Device Including A Differential Output LNA Connected to Multiple Receive Signal Chains (U.S. Patent). It was published in 2010. In the semiconductor industry, it is better to pick up a patent published recently to compare because the technology life cycle tends to be short (Rethinking Patent Cultures).

### 3.4. Possible Similarity and Distinction

The patent is about a whole communication system, including receiver, transmitter, antenna and other electrical components. In contrast, our LNA is merely a part of a bio-signal acquisition system. The reason why this patent may be related to our product is that the system contains an LNA as one of its components. As shown in the figure 1, the patent has an LNA that takes the output of a receiver as input and delivers the output signal to multiple signal chains through a power divider. However, our LNA is designed to take the output of an ECG sensor as the input and deliver the signal to the compressed sensing module.

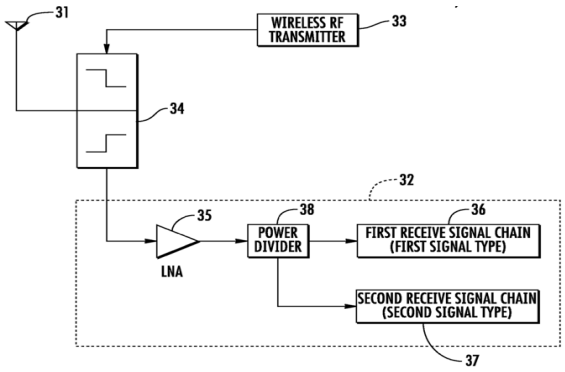


Figure 1 Schematic of the Depicted Patent

Although there is a certain extent of similarity with our system, we do not think that there is a major overlap; there is almost no risk of developing our product without purchasing a license. The patent is about a whole system, and it contains a component whose functionality is similar to our product. The idea that is patented is focused on the whole functionality of system, while we are more concentrated on designing the specific LNA component as part of the system.

Even the system's LNA specification is different from our product. The specification of our product requires only a narrow bandwidth, low carrier frequency and ultra low power consumption. On the other hand, a mobile communication system operates at radio frequency

with a relatively wide bandwidth, and the power consumption is not necessary low, as is desired in our application. When we design circuits under different specifications, the design approaches and the outcome can be drastically different. Therefore a patent is conceived unnecessary for our purpose.

### 3.5. Alternative Options and Potential Risks

Since applying for a patent is not feasible in our current situation, other alternatives should be scrutinized carefully. There are four other ways to protect intellectual property from external usage: a trademark, copyright, trade secret, and open source (Intellectual Property Crash Course). All of them have different characteristics from a patent, and each one has its own strength and weakness.

The first option is applying for a trademark. A trademark is simply a word or symbol that embodies the source or sponsorship of a particular product or service (Intellectual Property Crash Course). Our final product will be an LNA, and it does not have any particular name or symbol to strengthen its marketability. Also, a trademark does not protect the essence of our project, which is the approach to tackle the challenges in low-power LNA design.

The Second option is copyright. Unlike patent, copyright only protects the expression of an idea, and the idea itself is not secured (Intellectual Property Crash Course). Most importantly, in the United States, while IC layout design is commonly protected by patent, circuit schematics are not commonly protected (U.S. Copyright Office). Since our main focus is not the layout design, this option is not appropriate.

The third option is trade secret. The recipe for Coke is a classical example of the trade secret approach. Unlike patent, a person can keep a trade secret for a long time. A person does

not need to worry about other people seeing how his product works. A trade secret is perfect if a product is useful for several generations. However, in our case, the lifespan of the technology is very short, which is a fundamental limiting factor of the effectiveness of this approach.

The last point is an open source. This option is meaningful if we deal with software. The whole purpose of making a product open source is to improve the product with collaborative effort. In our case, the project is a circuit design so that this option is also not applicable. While other professionals in the field could have beneficial suggestions or criticizes a certain design, it is extremely difficult to contribute to another person's design by improving based on the design.

Finally, we should think of some potential risks of not protecting our ideas with legal enforcement. We conceive that, at this point, there is no such urgent need. Usually it takes years for a patent to be issued after the first application. It means that we need to devote extra time and resources to such process. Knowing that technology life cycle is very short in our industry, it is better for us to focus on developing more superior technology until it is more suitable for a patent.

# 4. Technical Contributions

## 4.1. Overview

The overall objective of our Capstone Project is to design a Low Noise Amplifier (LNA) for ultra-low power wireless transceivers in bio-signal acquisition systems. The LNA has mainly two features: ultra-low power dissipation and high noise tolerance, while achieving suitable gain for further processing.

The project consists of mainly three parts:

- Designing and analysis of the chopper stabilization modulator and demodulator;
- 1/f flicker noise analysis; amplifying circuitry design;
- Analysis of the non-linearity and distortion analysis of the amplifying circuit;
- Thermal noise analysis and techniques to compensate for thermal noise in low power LNA designs.

The task divisions are in bundles aiming at a specific section of the design problem. This makes it easier for one person in the team to concentrate on the tackling a specific problem in the design. When each individual task is completed, the design is merged to test for systematic functionality and performance. This is the ideal case while in reality the segmentation of the analog / RF circuit design is non-trivial since the various specifications may imply opposite directions in the design. For instance, to eliminate the effect of the flicker noise, the chopping frequency should be high, while for thermal noise the modulation frequency should be low. Thus co-optimization is often required.

In the project I am mainly engaged in the design of the amplifying circuit and distortion analysis. My component is the main amplifying component in the design. It is also crucial for the

amplifier to have reasonable gain at frequency range from mid-band to -3dB band of a few kHz. It is also crucial to keep the non-linearity of the circuit low to alleviate the impact of distortion.

## 4.2. Literature Review

With the advent and rapid development of the solid-state device and integrated circuit fabrication technology, it is possible to achieve very high voltage gain with minimal static power. But the ultra-low power design has a fundamental limiting factor, which is the electronic noise inherent to the active devices as well as the passive resistors in the system (Leacher 1515). The existence of electronic noise and the non-linear response of solid-state devices are the main sources of distortion in the LNA design. Thus reducing the gain in the power of the input-referred noise is beneficial for reducing the distortion of the amplifier.

Our LNA design is part of the design project for an ultra-low power wireless medical implantable transceiver for bio-signal acquisition system, based on compressed sensing technique. A structural diagram of the system is shown below, where ECG is the ECG sensor module that senses the electro-cardio signal of the person implanted with this device. The LNA is the focus of our Capstone Project. CS is the compressed sensing module, which further processes the output signal of our LNA design. ADC is the analog-to-digital converter that converts the compressed signal into digital signal. The power amplifier and the antenna then transmit the modulated signal to a portable mobile base station (Dixon 156).

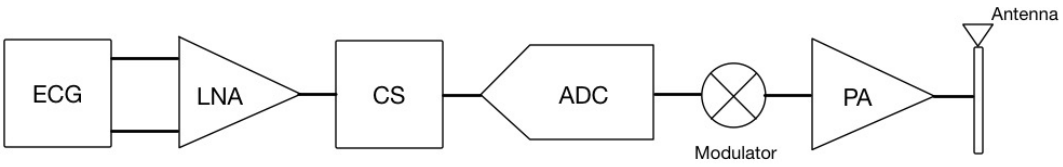


Figure 2. Structural Diagram of Bio-signal Acquisition System

We based our design on the SAED 30nm technology provided by Synopsys (32/28nm Interoperable PDK). This differs from the preceding study in that the technology we used has a supply voltage of 1.05V, which is lower than the referenced study of 1.3V (Lim 203). Although a reduction of supply voltage helps alleviate power concerns, the devices from this technology has serious short-channel effects that hamper the gain as well as the frequency performance of amplifier circuits comprised of these devices. Also since the operation regions of the transistors are not well defined in the deep-submicron region, the approach for sizing the transistors also differs from the long-channel devices.

The flicker noise of MOSFET devices is given by the equation below:

$$\overline{i_{1/f}^2} = \frac{K_f I_D \Delta f}{L^2 C_{ox} f}$$

where $K_f$ is the process-dependent coefficient, $I_D$ is the DC bias current $C_{ox}$ is the gate capacitance, and L is the length of the MOSFET. Since the frequency of the ECG signals, i.e. the heart rate of a human is typically in the range of 0.1 to 10 Hz, the ECG signal is extremely prone to contamination of flicker noise (Lin 680).

### 4.2.1. Common-Source Fully-Differential Amplifier

A design approach to incorporate chopper stabilization technique with a fully-differential amplifier. The chopper stabilization technique is applied both at the input and the output of the amplifier to reduce the amount of contamination to low frequency signals by flicker noise. The schematic in figure 3 presents the depicted topology. The mid-band gain of the amplifier is

$$A_v = \frac{g_{m1}}{g_{m4}}$$

where $g_{m1}$ is the transconductance of the input differential pair and $1/g_{m4}$ is the approximation of the output impedance due to the diode connected PMOS load (Enz 338).

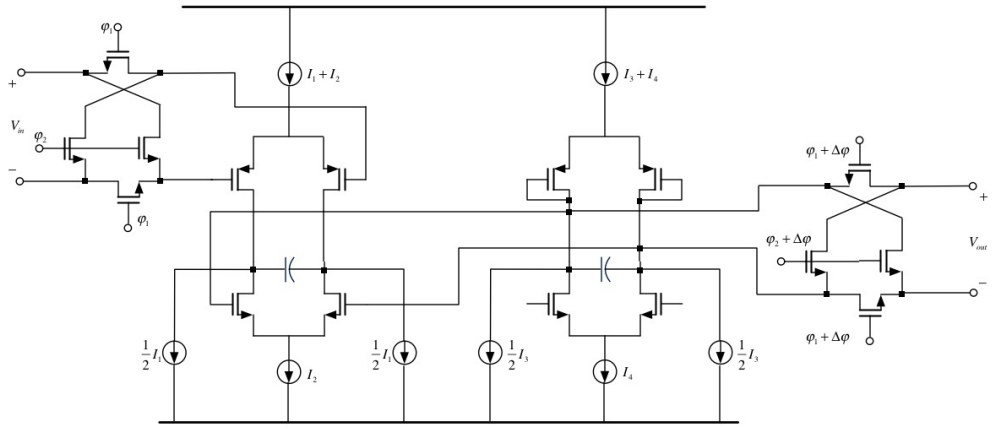


Figure 3. Fully Differential Amplifier (Enz 338)

### 4.2.2. Ring-Amplifier

Conventional analog circuit design approaches is becoming less effective since the scaling of technology strongly favors the time domain of high-speed digital circuit, thus a highly scalable approach for deep sub-micron analog design should be found in the time domain (Hershberg 2928).

A novel approach to design the amplifiers in the deep sub-micron technology nodes is the ring-amplifier topology. Ring-amplifier is an unconventional way to achieve high gain in deep sub-micron amplifier design, since it utilizes the large signal slew-based operation of three-stage ring-oscillators (Hershberg 2929). The structure is particularly attractive in contemporary deep sub-micron technology because of its relatively simple structure and its capability to suit technology scaling. However, ring amplifier design is a relatively new topic and there has been

no analytical approach given by researchers yet, the design of ring-amplifier requires a certain extent of intuition and fine-tuning.

The topology of the ring-amplifier is presented in figure 4. The fundamental difference between the ring-amplifier and its origin, the ring-oscillator, is that the signal path for the third stage inverter is split into two different paths for the PMOS and NMOS transistors respectively. This enables the input of the pull-up transistor and the pull-down transistor to be embedded with separate DC voltages, thus enabling both transistors of the output stage to operate at the sub-threshold region. Biasing the output transistors at sub-threshold regions is not only beneficial for power consumption consideration, but also crucial for the biasing the amplifier at appropriate operation regions, particularly stability of the closed-loop configured ring-amplifier. The difference between the embedded DC bias voltages $V_{RN}$ and $V_{RP}$ is defined as the dead-zone voltage $V_{DZ}$. In order to stabilize the amplifier, the dead-zone voltage should satisfy the following relationship:

$$V_{DZ} = \left| V_{RN} - V_{RP} \right| \geq \left| \frac{V_{DD} - V_{SS} - 2V_T}{A_2} \right|$$

where $A_2$ is the voltage gain of the second inverter stage. Aside from the DC bias voltages, the input range is also a crucial concern for the stable operation of the amplifier. When applying MDAC feedback network structure, the input DC level is not a key concern since the sampling capacitors between the input terminal and internal node can hold the DC voltage difference; in order to stabilize the amplifier, the AC input magnitude should satisfy the following relationship:

$$V_{IN} \leq \frac{1}{2A_1}\left( \frac{V_{DD} - V_{SS}}{A_2} - 2V_{OS} \right)$$

where $A_1$ and $A_2$ are the voltage gains of the first two stages respectively, and $V_{OS}$ is the DC offset voltage for the input of the second stage. In bio-signal applications the AC input range is not a serious threat to the amplifier operation because of the small signal amplitude, but DC input voltage may vary significantly, which is compensated by the switched capacitor nature of the pseudo-MDAC structure that periodically corrects the DC bias points (Carnes 5251).

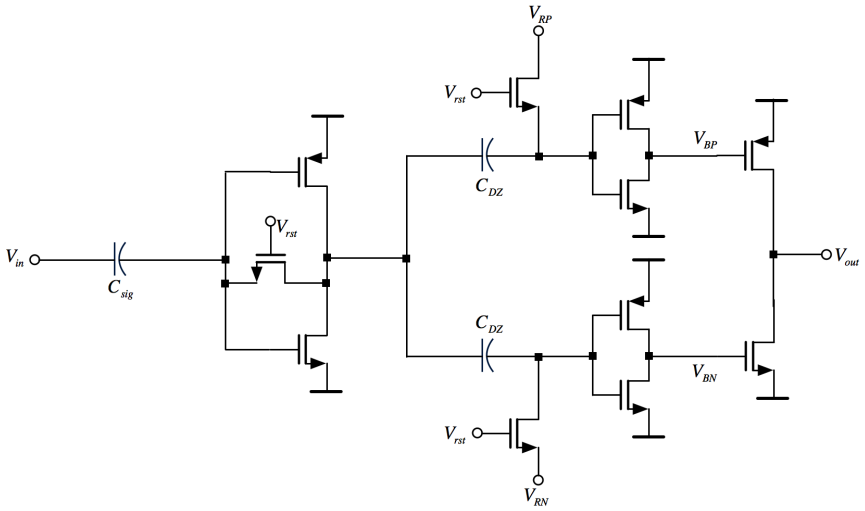


Figure 4. Schematic of the basic ring-amplifier structure

The time-domain response of the ring amplifier, once the ring-amplifier satisfies the stability criterion, is categorized into three periods: initial ramping, stabilization and steady amplification (Hershberg 2930). When the amplifier transitions from the periodic reset mode into the amplifying mode, the internal nodes in the amplifier will experience initial slewing due to physical mismatches and external interferences. This initial voltage ramping will create an overshoot voltage, which in the case of a ring-oscillator makes the successive slewing gain a larger overshoot voltage and eventually achieves oscillation. The reason why the ring-amplifier does not oscillate is that the overshoot voltage for the output transistors induced by the preceeding opposite overshoot voltage is significantly smaller than the ring-oscillator case, since

the output transistors are biased at subthreshold region. Thus the output resistance is significantly larger once the output enters the stable operating regions. This fundamental difference reduces the overshoot voltage of each successive voltage ramping and by a number of repetition the output voltage will stabilize and lock itself into the dead-zone region. The differences between each oscillation is

$$\Delta V_{overshoot} = \frac{t_d \cdot I_{slew}}{\sum C_{out}}$$

Thus the expression for stability criterion is presented below.

$$\frac{t_d \cdot I_{slew}}{\sum C_{out}} \leq \frac{1}{2 \cdot A_1}\left(\frac{V_{DD} - V_{SS}}{A_2} - 2 \cdot V_{DZ}\right)$$

This equation gives a clear relationship between $t_d$, $I_{slew}$ and $V_{DZ}$, which link to the speed, output range and power dissipation of the amplifier. The effect of feedback network on stability and gain will be discussed in detail as the design process in section 4.3.

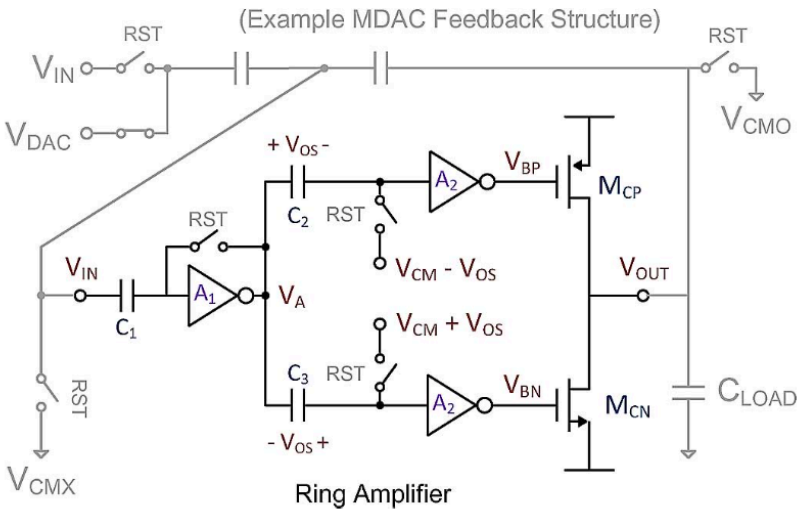


Figure 5. Ring Amplifier Applied in MDAC Feedback Structure (Hershberg 2929)

## 4.3. Methods and Materials

### 4.3.1. Ring Amplifier Design Process

The motif of designing the LNA based on the ring-amplification structure is due to its attractiveness for the purpose to achieve high gain and consuming low power at ease due to its relatively simple structure, as long as the stability issue for the amplifier is appropriately resolved. Unfortunately, the idea of using ring-oscillator structure to implement amplifier is a relatively new idea, thus there has been no readily available analytical methodology to describe the slew-based amplifying operation of the amplifier in the frequency domain. Thus, much of the effort we have made during the design process of ring-amplifier is explorative, through which we identify some of the important influencing factors for the ring-amplifier performance, as well as some issues we encountered during the design process.

The main difference between using an inverter as an amplifying stage and a conventional common source amplifier with active load device is that the signal path is no longer connected to only one of the transistors in the stage, enabling the push-pull operation of the NMOS-PMOS pair which is similar to the operation of static CMOS logic gates. In general, the voltage transfer curve of the inverter transitions more rapidly as channel length of the transistor increases. Also, larger W/L ratios for the transistors will increase the $g_m$ of the transistors, which increases the gain of the inverter.

First, the allocation of gain for each stage is determined. Since the gain of each stage affects the noise performance of the original ring-amplifier, i.e. before the addition of noise-alleviation techniques such as the chopper technique, it is important to appropriately assign the gain of each stage. The overall noise figure of the amplifier is defined as:

$$NF_{RING-AMP} = \left( F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 \cdot A_2} \right)\Bigg|_{dB}$$

where the subscript depicts the order of the inverter stage. Thus for a given gain requirement, allocating the highest gain to the first stage will help significantly reduce the noise figure of the amplifier. Thus the lengths of the transistors for the first stage should be set large to achieve high gain. Also, since our scenario application is ECG sensors whose output voltage is typically less than 1mV, if the target gain for the successive two stages is 46dB than the output swing of the first stage need not be larger than a few millivolts to achieve an output swing of 300mV. Therefore the static current of the first stage could be reduced to conserve power. For the second stage, the DC bias voltages of the second stage greatly determines the DC voltage of the third stage, which is crucial for the stability of the inherently closed-loop configured ring-amplifier. Since the DC bias voltages $V_{RN}$ and $V_{RP}$ generate the DC voltages $V_{BP}$ and $V_{BN}$ through 2nd stage inverters, $V_{BN}$ and $V_{BP}$ should be stable against variations in $V_{RN}$ and $V_{RP}$. One method is to size the transistors to have maximal threshold voltage. However, this is difficult to practice since once the ring-amplifier settles to the operating point, the second stage inverters are prone to entering triode region, resulting in low overall voltage gain (Lim 202). A more practical way to stabilize $V_{BP}$ and $V_{BN}$ is to reduce the large signal gain of the 2nd stage, thus the lengths for the transistors of the 2nd stage should be minimal.

The sizing of the 3rd stage inverter is the trickiest part of the design process, not only because it affects the overall gain of the amplifier, but also the stability of the amplifier. The transistors in the 3rd stage should be biased in the sub-threshold region by $V_{BP}$ and $V_{BN}$, in order to trigger the diminishing overshoot transition, as discussed in section 4.2.2. Therefore it is appropriate to size the transistors such that they possess the largest $V_t$ values. This will result in a

large dead zone region, which alleviates the dependency of stability on $V_{BP}$ and $V_{BN}$ variation. Once the threshold voltages of the amplifier is determined, the values for $V_{BP}$ and $V_{BN}$ can be determined, as well as the values for $V_{RP}$ and $V_{RN}$. While the determination of $V_{RP}$ and $V_{RN}$ can be easily done by simulating the VTC of the 2nd stage inverter, the determination of $V_{BP}$ and $V_{BN}$ is not supported by a convenient model yet. The sub-threshold conductance due to the underlying parasitic bipolar transistor is

$$I_{ds} = 100 \cdot \frac{W}{L} \cdot e^{-q(V_{gs}-V_t)/\eta kT} (nA)$$

which clearly indicate an exponential increase with increasing $V_{gs}$ (Hu 283). In a normal common source amplifier this equation is sufficient to derive the $g_m$ and $r_o$ of the amplifying transistor, but since in an inverter there is no load device and both transistors collaborate to amplify the signal and $r_o$ is constantly varying, this approach is inaccurate due to the push-pull operation of the two complimentary devices. The third stage is also crucial for the stability of the amplifier in closed-loop configuration, so the 3rd stage also needs to be adjusted to compensate for charge sharing due to $C_f$. The schematic of the closed-loop ring amplifier is shown in figure 6.

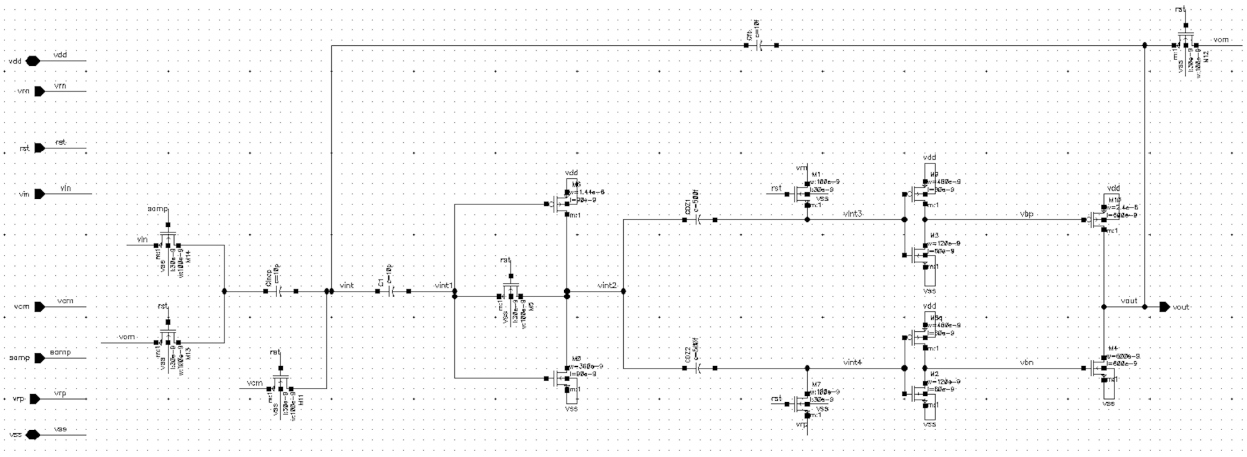


Figure 6. Ring-Amplifier Schematic

The next major concern in the ring amplifier design is stability. Because of the inherent closed-loop configuration, the stability of the amplifier not only depends on the three stages, but also depends significantly on the feedback factor, i.e. mainly the feedback capacitor $C_f$. For bio-signal applications the bandwidth requirement for the amplifier is relaxed, therefore in our design we sacrificed bandwidth for stability of the amplifier by introducing large capacitors as the charge holding capacitors in the input to create a dominant pole at the input. Reducing bandwidth also helps us to meet with the stringent power requirement imposed by implantable applications. The feedback factor is

$$f = \frac{C_f}{C_f + C_{in}}$$

Since the amplifier gain is inversely related to the feedback factor, $C_f$ should be as small as possible. However the pole at the output node also depends on $C_f$, thus its value should also be large enough to stabilize the amplifier.

In the process of the ring-amplifier design, we discovered that the closed-loop gain and stability are not significantly affected by the inverter stages, but significantly affected by the feedback loop. This is mainly because the three slew-based inverter stages render the amplifier high open-loop gain; plus at low frequency range, capacitors exhibit high impedances and dominate the feedback factor. In our design process, the feedback capacitor has a value of $C_f$ = 10fF. A capacitor with such a small value is not feasible in older technologies due to fabrication mismatches, however in modern deep-submicron technologies, with careful layout matching techniques small capacitor values can be well controlled. E.g. in a 32nm SOI technology, this capacitor value can be implemented with multi-finger fringe capacitor of 0.45fF / finger

(Tripathi). The input capacitances are set to 10pF in order to have small feedback factor and hence enlarge the closed-loop gain.

The switches in the circuit are implemented with simple NMOS transistors, since except for the switch that is connected to the input terminal, none of the other switches are in the signal path. The switches mainly influence the noise of the amplifier and spikes during the periodic reset transitions. Shot noise and flicker noise are directly related to the DC current flowing through the junctions in the transistors, thus the switches contributes little noise since little DC current flow through them. Thermal noise is related to the on-state resistances of the switches, therefore increasing the W/L ratios of the switches will reduce the thermal noise introduced by the switches. In practice, however, we discovered that if the size of the switches is large, the voltage spikes are large, due to charge injection effects induced by the parasitic $C_{gs}$ and $C_{gd}$. Combined with the fact that the noise contribution of the switches is relatively minor, the switches are minimum sized (Gray 736).

### 4.3.2. Adjustments and Improvement

There are several problems with the original circuit topology presented in figure 6. First, the stability of the amplifier is extremely sensitive to variations of the DC voltages $V_{RN}$ and $V_{RP}$, $C_f$ and DC input voltage. In extreme cases, 1mV variation of $V_{BP}$ and $V_{BN}$ will make the ring-amplifier oscillate. Second, there is significant DC output voltage shift when in the amplifying mode. This DC shift is mainly due to the DC shift of the first stage output and therefore inert to adjustments in transistor sizing and DC bias of the third stage. Increasing the value of the input capacitors of the second stage $C_{DZ}$ will alleviate the output DC shift, but only by as much as 10%.

Another problem is the transistor sizing of the first stage. As discussed in section 4.3.1, the gain of the first stage should be high. However the gain of the first stage affects almost all the aspects of the ring-amplifier performance significantly, including stability, gain, and output DC level, thus modifying the gain of the first stage will very likely make the ring-amplifier inoperable.

Another factor that makes the previous topology inappropriate for our scenario application is its single-ended input structure. The DC voltage level from the ECG level can vary by as much as 100μV, thus many ECG sensors provide differential output to enable amplifying schemes that are inert to input DC voltage shifts (Texas Instruments 3). Furthermore, since the output signal range is at low frequencies, the primary type of noise that contaminates the desired signal is the flicker noise. The flicker noise cancellation scheme we apply to the amplifier is the chopper stabilization technique, which also requires differential signal paths for optimal noise cancellation performance.

To enable the incorporation of chopper stabilization technique with the amplifier, it is required to adjust the input structure to differential input structure. A structural diagram of the modification is shown in figure 7. Because approximately 49% of the total amplifier noise is introduced by the 1$^{st}$ stage, applying chopper module to the 1$^{st}$ stage is sufficient for the purpose of noise reduction. Since the 1$^{st}$ stage is now differential output, the corresponding input structure of the 2$^{nd}$ stage is also changed into differential input. Another modification is to directly apply the embedded bias voltages $V_{RN}$ and $V_{RP}$ to the input of the last stage, instead of the input of the second stage. The rationale behind this modification is that the variation of $V_{RN}$ and $V_{RP}$ by 1mV could result in as much as 60mV deviation for $V_{BN}$ and $V_{NP}$. Thus the amplifier is more stable if $V_{RN}$ and $V_{RP}$ are directly embedded to $V_{BN}$ and $V_{BP}$, respectively.

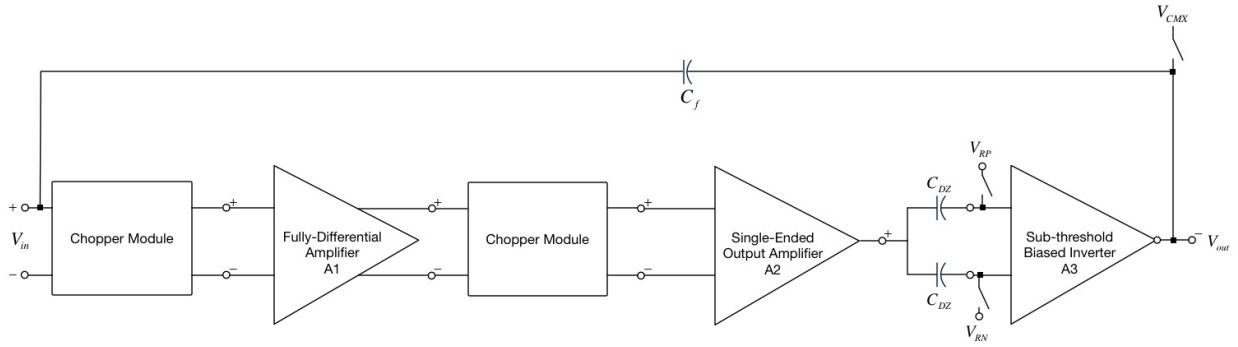


Figure 7. Fully-Differential Structure of the Modified Amplifier

High 1st stage gain is desired for optimal noise performance. One approach is to use folded-cascode structure. However folded-cascode structure is prone to performance deterioration if biased with low DC current, not to mention it contributes much more noise due to resistive degeneration. Thus a fully differential common-source amplifier is first adopted. While having better noise performance than cascode amplifier, the gain of such structures in 30nm technology could barely reach 26-28dB.

When we refer back to the high gain property of the inverter in deep-submicron technology, we noticed that the input signal flows to both the NMOS and PMOS transistors, resulting almost twice as much transconductance as the simple common-source amplifier case. We also noticed that the amplifier ring-amplifier has been established with reset-amplify mode of operation. These allow us to introduce a dedicated amplifying structure, which we call fully differential inverter. The symbolic representation and the transistor-level schematic are presented in figure 8. This structure improves the gain of the 1st stage to 32dB. Another advantage of this structure is the utilization of a current source to determine the bias current of the differential inverter. This effectively reduces the extent of output DC shift.

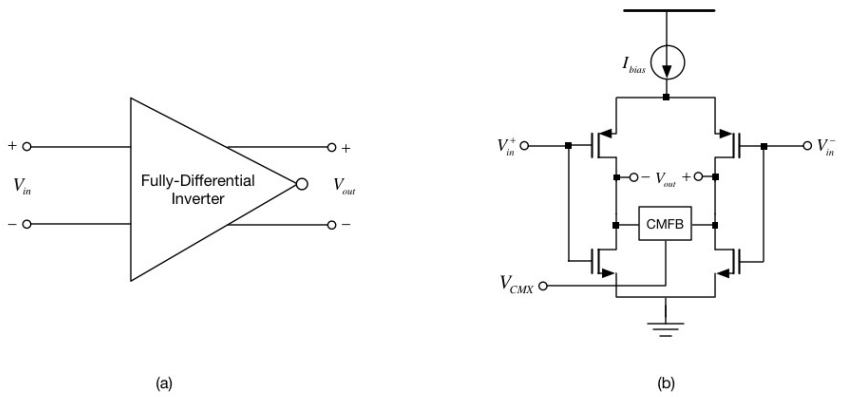


Figure 8. Dedicated Fully Differential Inverter

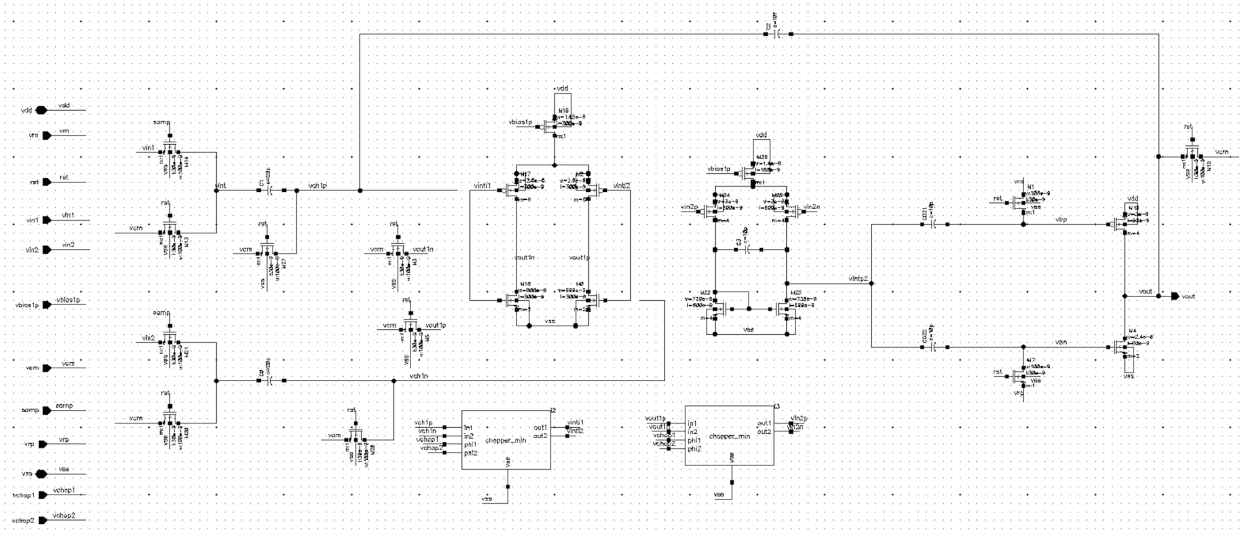

Figure 9. Schematic of the Modified Ring-Amplifier

There are prerequisites for implementing this structure. First, the input AC signal range should be small enough to ensure both transistors are biased in saturation region. Second, there should be a frequent reset action to ensure that the DC bias for the fully differential inverter is corrected periodically. The environment of the 1st stage inverter satisfies both conditions. A drawback of this structure is the increased noise level due to utilizing the transconductance of the NMOS transistor, but since we would applying the chopper technique to the 1st stage, the noise introduced by the 1st stage will be modulated by the chopping frequency, thus it is less likely to

contaminate the desired signal which is modulated back to low frequency ranges by the 2nd chopper. The schematic of the modified amplifier is presented in figure 9. Also note that the dominant pole is at the output node of the second stage. This is obvious in that the dead-zone capacitors should be kept large in order to lower the frequency of the low-frequency zero, hence enlarging the low-frequency voltage gain. Also the second stage has moderate gain, thus the output resistance of this node is high.

Another point of notice is that since the LNA is to amplify very-low frequency signals, the zeros in the circuit should locate at extremely low frequencies. The AC feed-through capacitors $C_{DZ}$ between the second stage and the third stage should be enlarged, in order to move the RHP zero contributed by $C_{DZ}$ to be located at extremely low frequency. To add stability to the amplifier, a differential-mode configured frequency compensation capacitor is added to the output node of the second stage. It further reduces the bandwidth of the amplifier and the phase margin is increased to approximately 30° when the amplifier is open-loop configured.

## 4.4. Results and Discussion

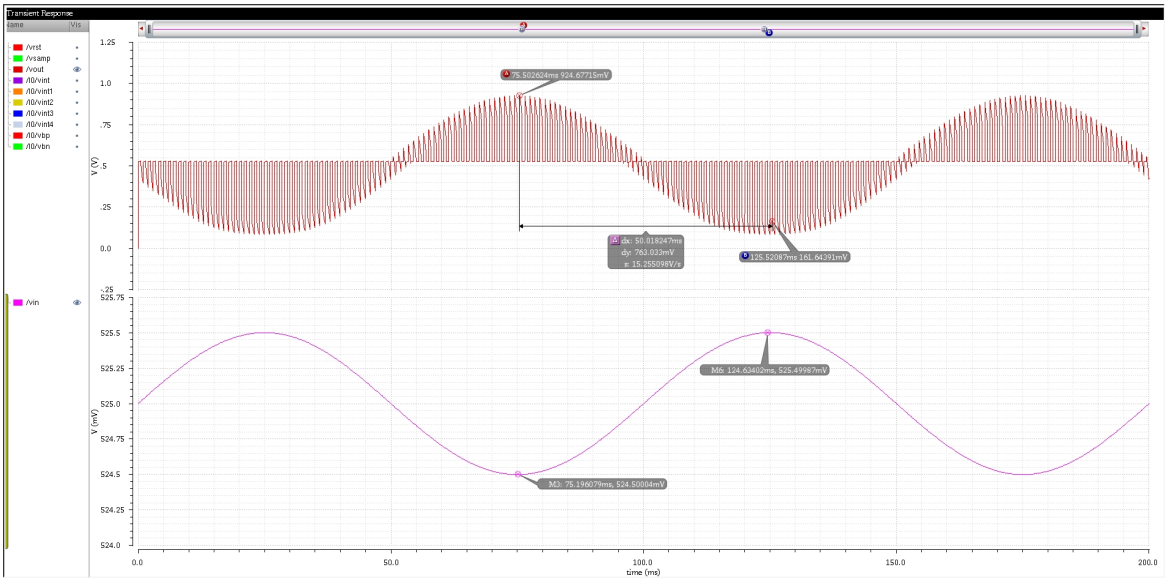


Figure 10. Transient Waveform of the Ring-Amplifier

The transient simulation of the ring-amplifier is shown in figure 10. The input stimulus has $V_{pp}$ = 1mV and $f_{in}$ = 10Hz. The basic ring-amplifier structure also suffers from output DC shift when the amplifier enters amplifying mode.

The small signal PAC simulation result is shown in figure 11. The low frequency voltage gain is $A_v$ = 51.73dB. Due to convergence problems encountered in frequencies higher than 20MHz in the PAC simulation, the plot terminates at 20MHz; however the phase and voltage gain magnitude given in the plot below indicates a positive phase margin.

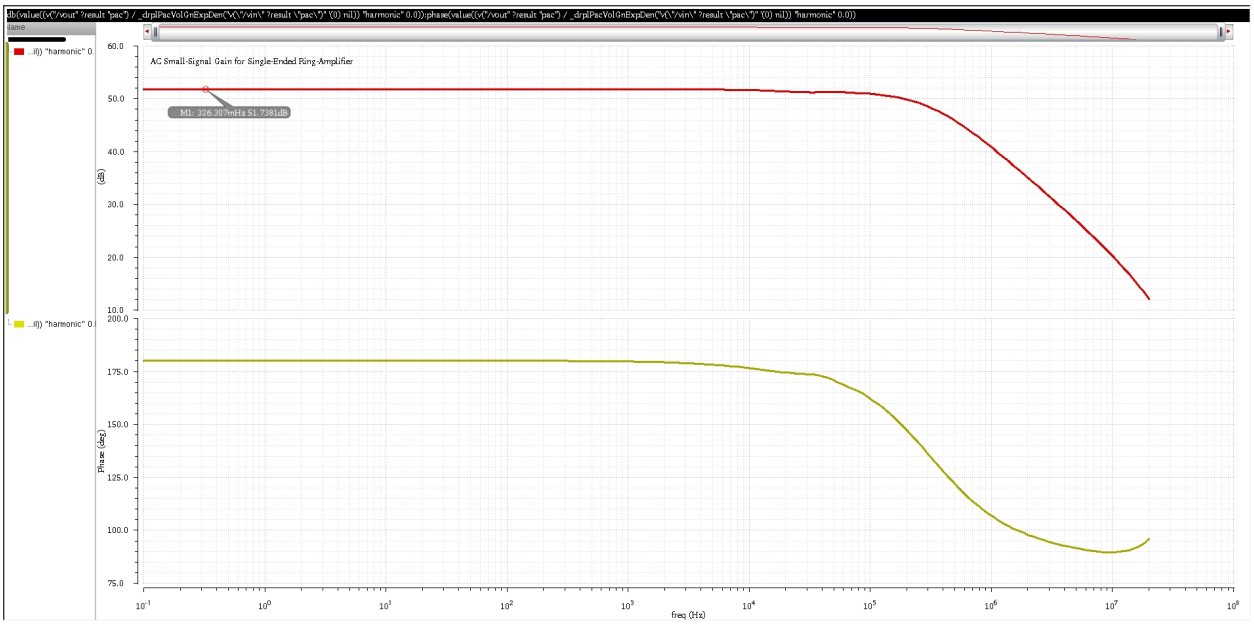


Figure 11. PAC Frequency and Phase Response of the Single-Ended Ring-Amplifier

The output noise spectrum is shown in figure 12. At 10Hz the output noise voltage is $871uV/(Hz)^{1/2}$.

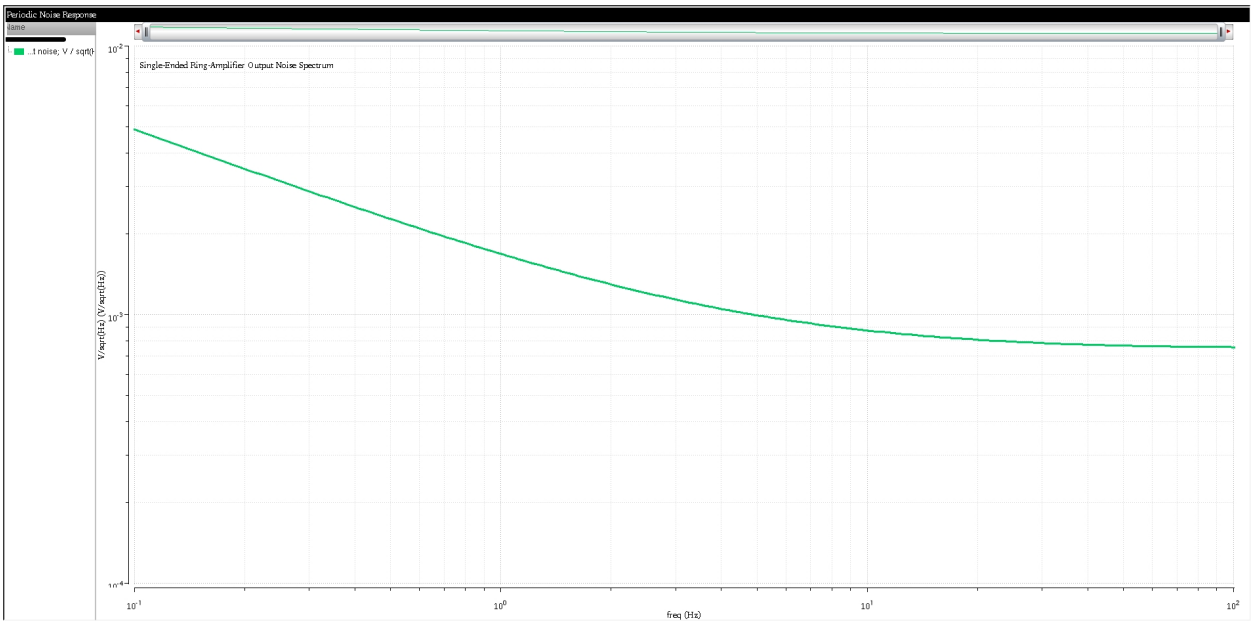


Figure 12. Output Noise Voltage Spectrum of the Single-Ended Ring-Amplifier

The output total harmonic distortion is shown in figure 12. At 1mV input voltage magnitude the output THD is 14.3%.

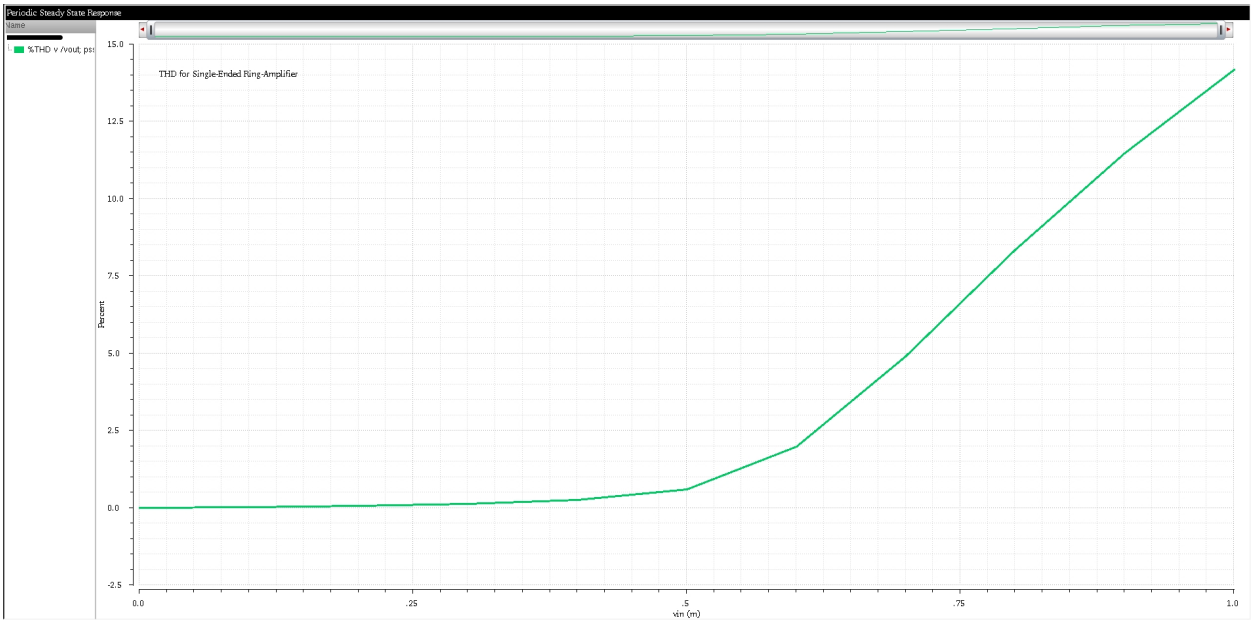


Figure 12. Output Total Harmonic Distortion of the Single-Ended Ring-Amplifier

The transient simulation waveform of the modified ring-amplifier, i.e. the amplifier without the choppers, is shown in figure 13. As can be seen from the waveform, the output DC shift is significantly alleviated.

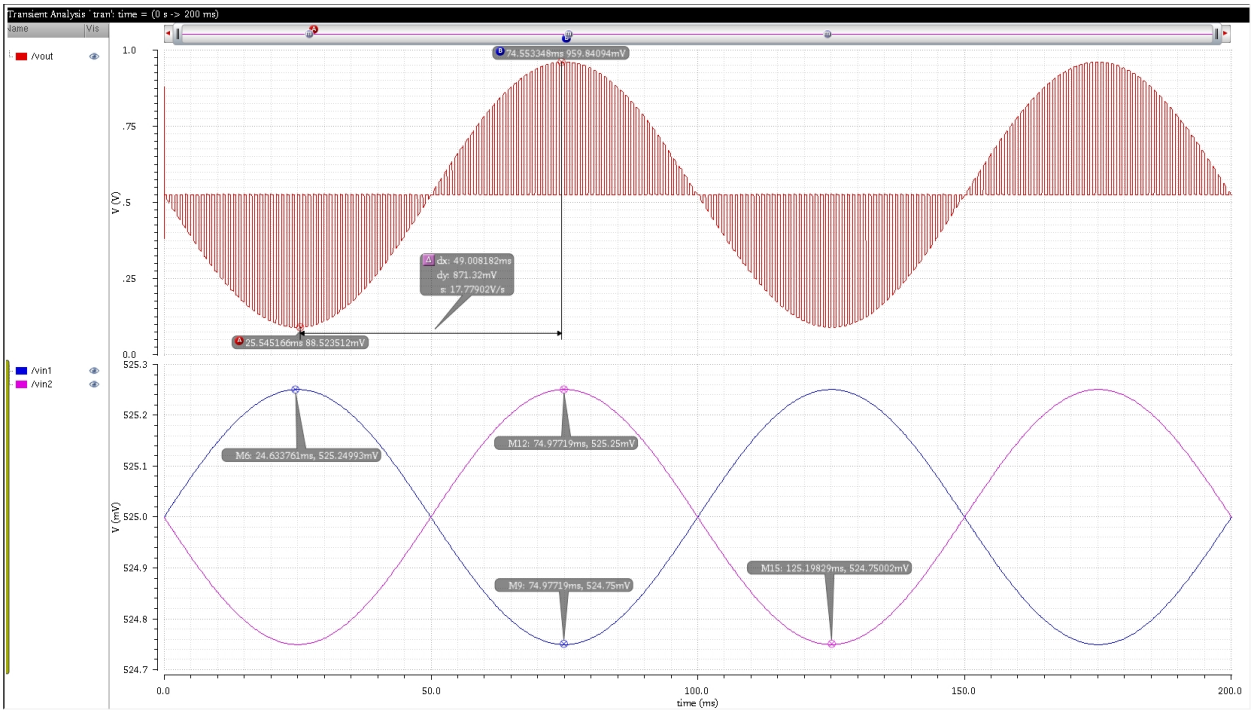


Figure 13. Transient Waveform of the Differential Input Ring-Amplifier

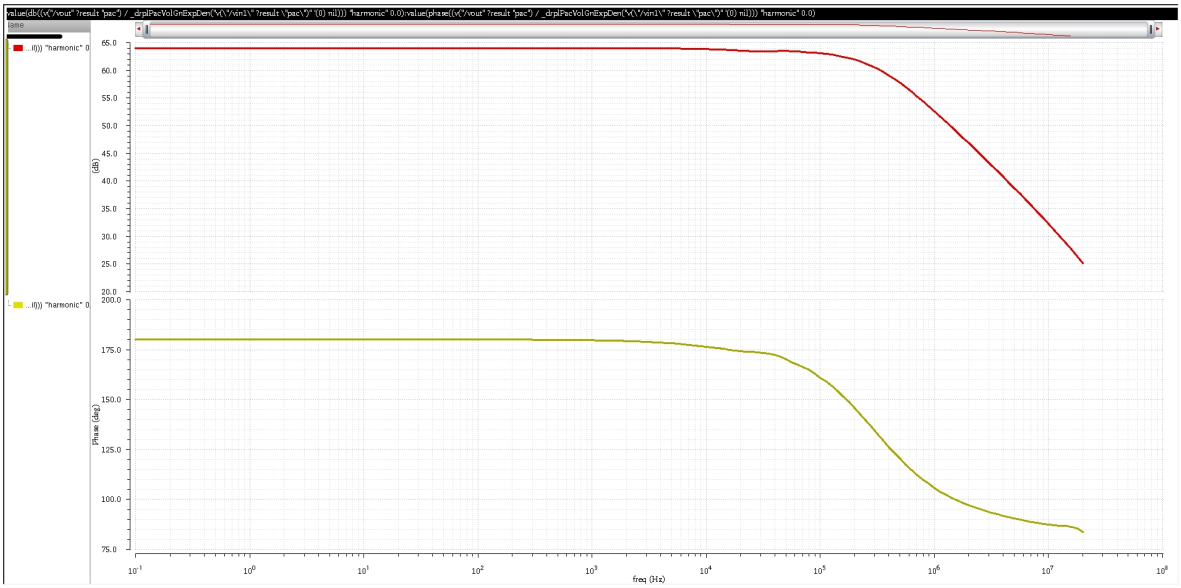


Figure 14. PAC Frequency and Phase Response of the Modified Ring-Amplifier

The small signal PAC simulation result is shown in figure 14. The low frequency voltage gain is $A_v$ = 63.93dB. Similar to the single-ended case, a positive phase margin is expected.

The output noise spectrum is shown in figure 15. At 10Hz the output noise voltage is 1300uV/(Hz)$^{1/2}$.

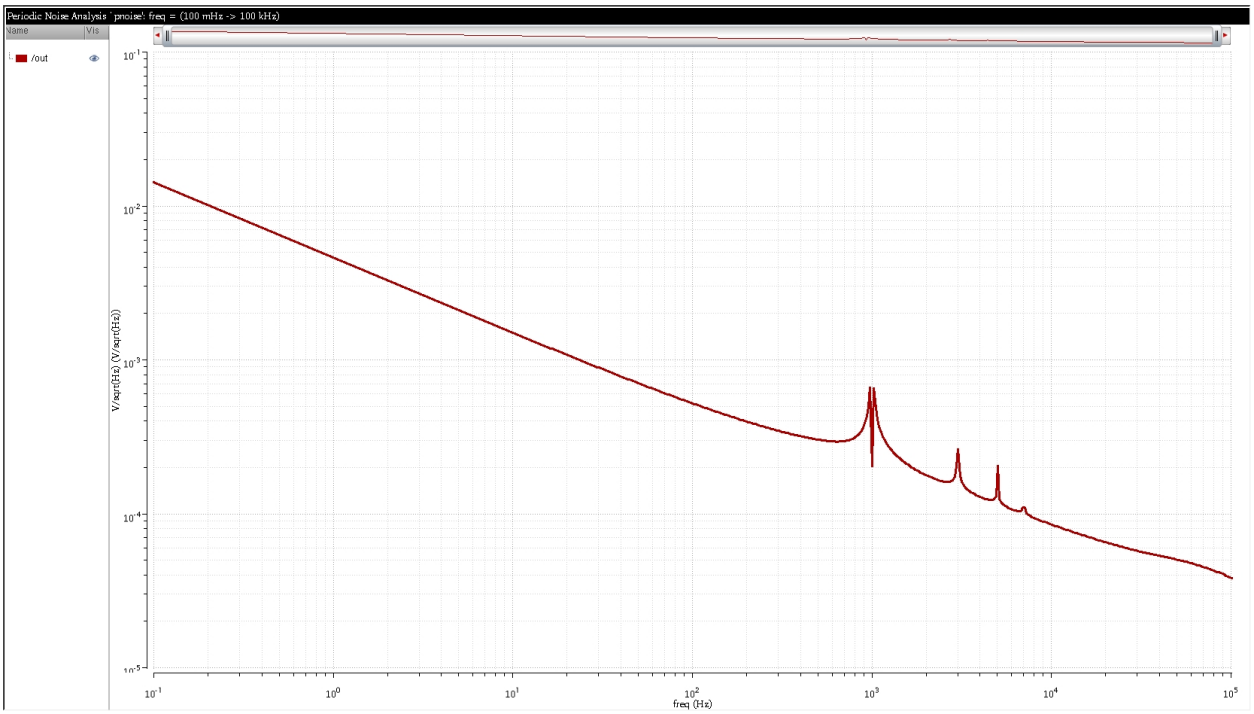


Figure 15. Output Noise Voltage Spectrum of the Modified Ring-Amplifier

The output total harmonic distortion is shown in figure 16. At 1mV input voltage magnitude the output THD is 27.8%.

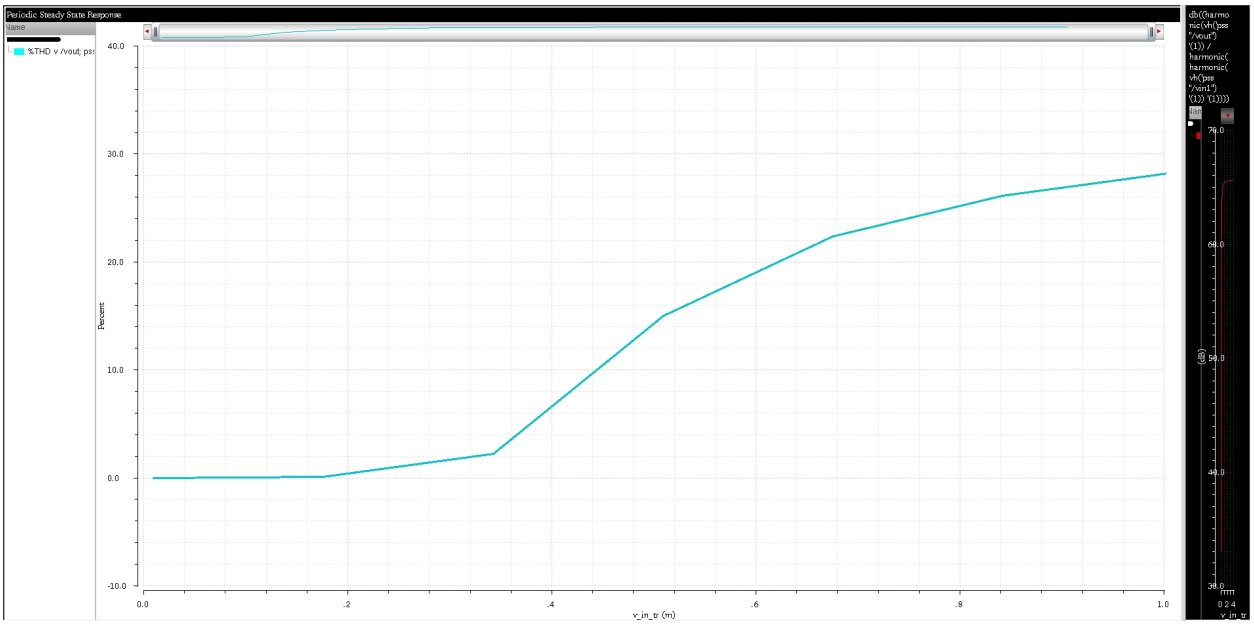


Figure 16. Output Total Harmonic Distortion of the Modified Ring-Amplifier

The transient waveform for the modified amplifier with chopper stabilization is shown in figure 17.

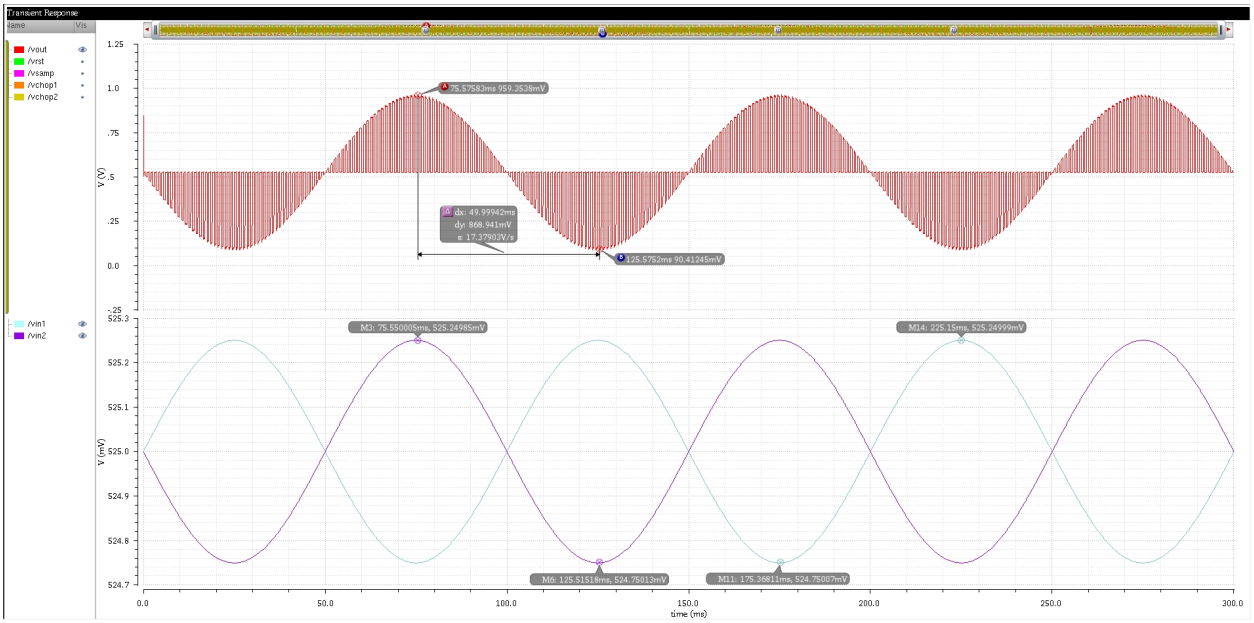


Figure 17. Transient Waveform of the Differential Input Ring-Amplifier with Chopper Stabilization

The small signal PAC simulation result is shown in figure 18. The low frequency voltage gain is $A_v$ = 57.77dB. By applying differential compensation capacitor at the output node of the second stage amplifier, the UGB is brought down to below 20MHz where the PAC result would converge. The PAC analysis gives UGB = 12MHz, and phase margin of approximately 30°.

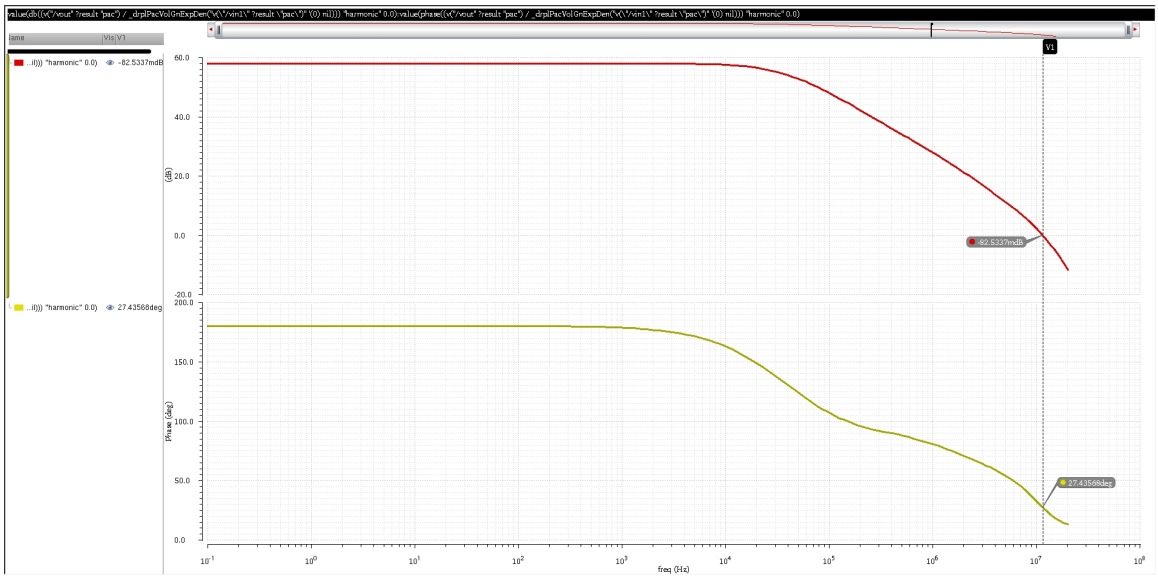


Figure 18. PAC Frequency and Phase Response of the Modified Ring-Amplifier

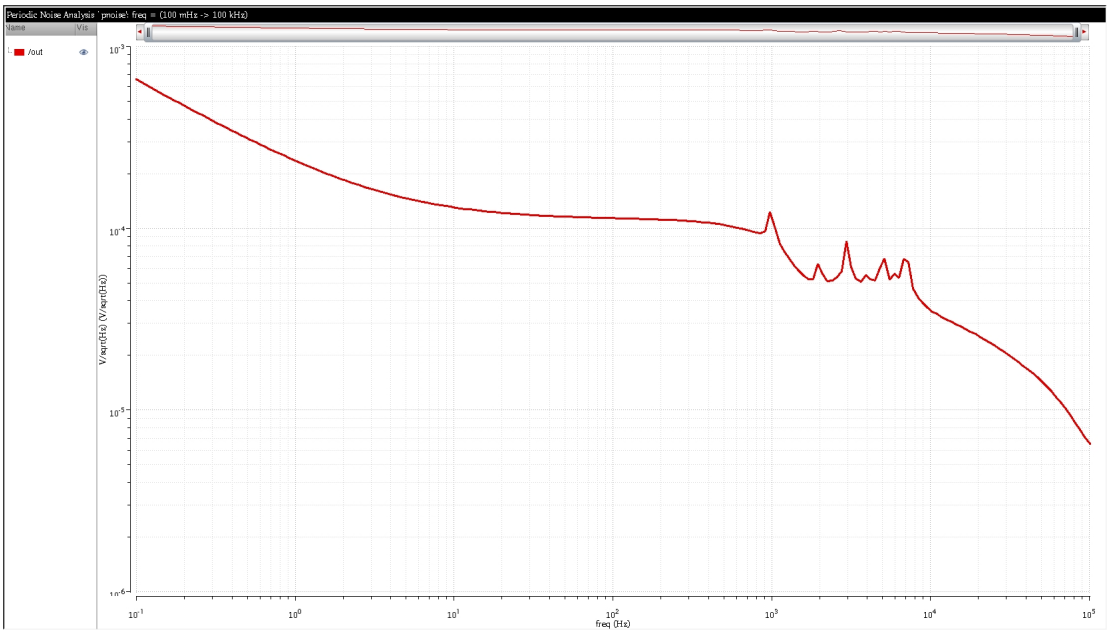


Figure 19. Output Noise Voltage Spectrum of the Modified Ring-Amplifier

The output noise spectrum is shown in figure 19. At 10Hz the output noise voltage is 120uV/(Hz)$^{1/2}$. Compared to the unchopped amplifier case, the total output noise voltage is reduced by approximately an order of magnitude.

The output total harmonic distortion is shown below. At 1mV input voltage magnitude the output THD is 28%.

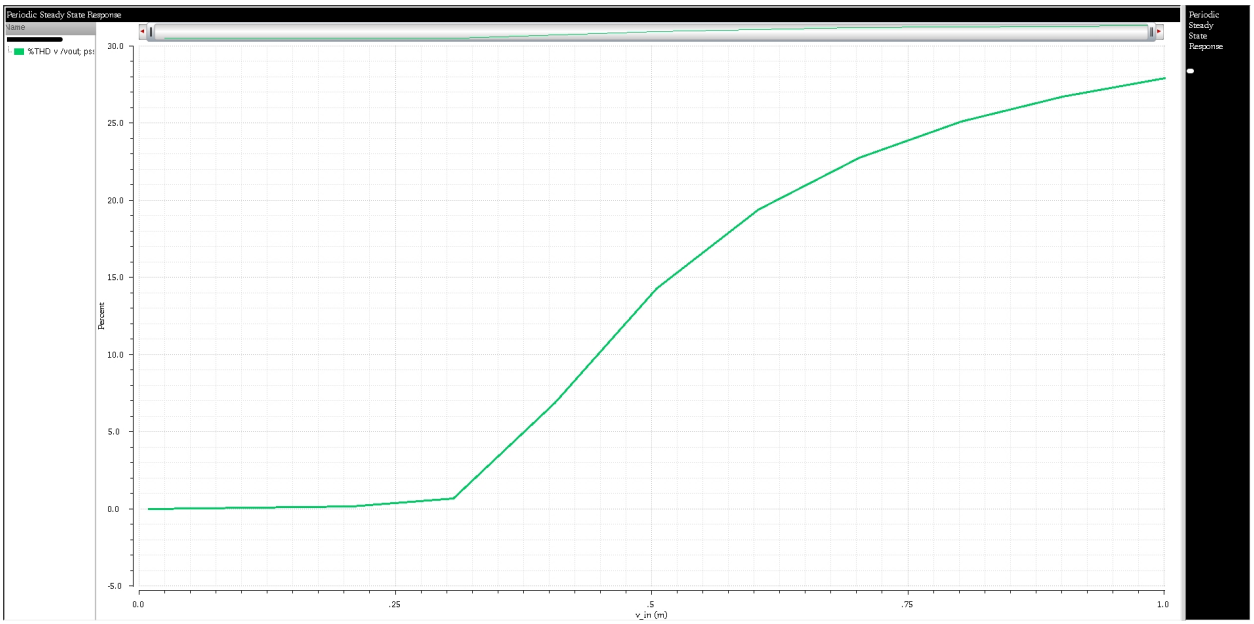


Figure 20. Output Total Harmonic Distortion of the Modified Ring-Amplifier

The FFT analysis results of the original ring-amplifier, the unchopped and the chopped differential input amplifier is shown in Figure 21. While having good noise performance, the amplifier suffers from serious distortion. The distortion of the unchopped amplifier is well controlled, but noise performance is inferior, due to the noise contributions of the NMOS amplifying transistors of the 1$^{st}$ stage. The chopped amplifier has better noise performance compared with the unchopped case, while compromising some extent of distortion.

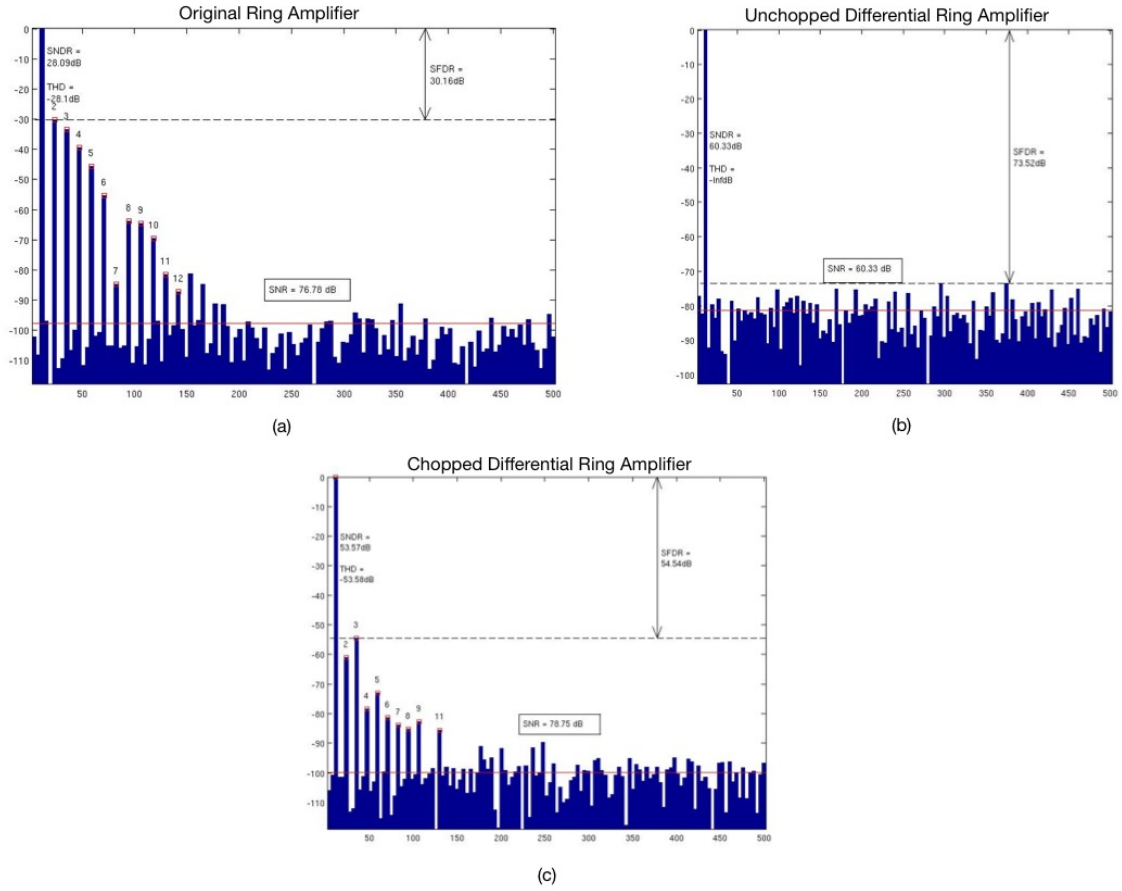


Figure 21. FFT Analysis Results for the Three Types of Implementations

A comparison of the performance of the three implementations is given in Table 1. It can be concluded that the fully differential ring-amplifier with chopper stabilization has the most well balanced performance in terms of distortion and noise performance.

Table 1 Performance Comparison of Three Different Topologies

| Topology | Original | Unchopped | Chopped |
|---|---|---|---|
| **Static Power (μW)** | 2.75 | 5.51 | 5.37 |
| **$A_{CL}$ (dB)** | 51.73 | 63.93 | 57.77 |
| **THD ($V_{in}$=1mV) (%)** | 14.3 | 27.8 | 28 |
| **Noise $V_{on}$ ($f_{in}$=10Hz) (μV/$Hz^{1/2}$)** | 871 | 1300 | 120 |
| **SNR ($V_{in}$=1mV) (dB)** | 76.76 | 60.33 | 78.75 |

The design process of our Capstone Project has rendered us some insights in ultra-low power LNA design as well as some useful experiences for designing ring-amplifier, which is a relatively new idea. Here we conclude some of the important points of notice for ring-amplifier design. For low noise purposes, the 1st stage should target at high gain. The second stage should have gradual VTC curve to stabilize the DC bias voltage of the 3rd stage. The DC bias voltages for the 3rd stage $V_{BP}$ and $V_{BN}$ should be co-optimized with the sizing of the transistors of the 3rd stage, to stabilize the amplifier in closed-loop configuration. The closed-loop gain is greatly influenced by the feedback factor, due to the large open-loop gain of the three-stage inverters.

## 5. Concluding Reflections

Through the Capstone Project, not only have I honed my knowledge and skills in low power and low noise amplifier design at low frequency ranges, but also gathered a sense of how to identify, address and resolve issues encountered when conducting a project. Initially, the main problem we encountered was achieving high gain when designing with 30nm technology. We have tried various conventional amplifier topologies but all failed to achieve the desired performance. During the design process we discovered a relatively new topology called the ring-amplifier, which is a competent candidate for achieving high gain while consuming ultra-low power dissipation. Albeit its potential, the ring-amplifier is currently not thoroughly studied, thus there is no convenient model to pilot the design process. Some key insights for the design of ring-amplifier resulted from the exploration process, and are discussed in detail in the technical contribution section.

Much of the plight we encountered is due to lack of analytical model to pilot the procedure of ring-amplifier design. Thus it will be extremely beneficial not only to the ring-amplifier design itself, but also to the realm of analog design in the deep-submicron technology nodes, if a readily available analytical model for ring-amplifier is proposed.

# Work Cited

"32/28nm Interoperable PDK." Synopsys. Synopsys Armenia Educational Department, 2011. Web. 10 Mar. 2015.

Allstot, David J. et al, “Compressed Sensing Analog Front-End for Bio-Sensor Applications”, IEEE Xplore Database, Web. 15 Feb. 2015

Bellis, Mary. “How to Qualify for a Patent.” About.com Inventors. About.com, n.d. Web. 24 Feb. 2015.

Carnes, Josh. and Un-ku Moon. “The Effect Of Switch Resistance On Pipelined ADC MDAC Settling Time”. Circuits and Systems 2006 (2015): 5251. Web. 16 Mar. 2015.

Centers for Diseases Control and Prevention. “Deaths: Final Data for 2013”. Web. 15 Feb. 2015

Chan, Wen-Yen. “Mobile wireless communications device including a differential output LNA connected to multiple receive signal chains.” U.S. Patent No. 8,125,933. 28 Feb. 2012.

Chen, Roawen. “The Future of Semiconductor Industry from ‘Fabless’ Perspective”, Web. 15 Feb. 2015

Dixon, Anna M., Emily G. Allstot, Daibashish Gangopadhyay, and David J. Allstot. "Compressed Sensing System Considerations for ECG and EMG Wireless Biosensors." IEEE Xplore. 156 - 166, Apr. 2012. Web. 9 Mar. 2015.

Enz, Chiristian C., Eric A. Vittoz, and F. Krummenacher. "A CMOS Chopper Amplifier." Journal of Solid-State Circuits. IEEE Xplore, June 1987. Web. 9 Mar. 2015.

Gray, Paul R., Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer. 4th ed. New York: John Wiley and Sons, 2000. Print.

Hershberg, Benjamin et al. “Ring Amplifiers For Switched-Capacitor Circuits”. 2012 IEEE International Solid-State Circuits Conference (2012): 2928-2935 Web. 15 Mar. 2015.

Hoopes, Stephen. “IBISWorld Industry Report 52411b Health & Medical Insurance in the US”. Web. 15 Feb, 2015

Hu, Chenming. “Modern Semiconductor Devices For Integrated Circuits”. Upper Saddle River, N.J.: Prentice Hall, 2010. Print.

“Intellectual Property Crash Course.” *Patents, Copyrights, Trade Secrets, & Trademarks*. N.p., n.d. Web. 25 Feb. 2015.

Leach, Marshall W., JR. "Fundamentals of Low-Noise Analog Circuit Design." Proceedings of the IEEE 82.10 (1994): 1515. Web. 9 Mar. 2015.

Lim, Yong, and Michael P. Flynn. “11.5 A 100MS/S 10.5B 2.46Mw Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers”. 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC) (2014): 202-203 Web. 15 Mar. 2015.

Lin, Chia-Hung. "Frequency-domain Features for ECG Beat Discrimination Using Grey Relational Analysis-based Classifier." Computers & Mathematics with Applications 55.4 (2008): 680-90. Web. 11 Mar. 2015.

McKinsey & Company. “McKinsey on Semiconductors”. Web. 15 Feb. 2015

Porter, Michael. "The Five Competitive Forces That Shape Strategy." Print.

Porter, Michael. “What is Strategy?” Harvard Business Review, Print.

PRNewswire. “Global Wireless Portable Medical Device (Monitoring, Medical Therapeutics, Diagnosis, Fitness & Wellness) Market - Forecast to 2020.” Web. 15 Feb. 2015

“Role of Intellectual Property in the Intellectual Property (IP) Challenges and Concerns of the Semiconductor Equipment and Materials Industry.” Role of Intellectual Property in the Intellectual Property (IP) Challenges and Concerns of the Semiconductor Equipment and Materials Industry (2008): 1. SEMI. SEMI, Apr. 2008. Web. 24 Feb. 2015.

Schaller, Robert R. “Moore's law: past, present and future.” Spectrum, IEEE 34.6 (1997): 52-59.

Texas Instruments. “Low-Power, 2-Channel, 24-Bit Analog Front-End for Biopotential Measurements (Rev. B)”. (2011): 3-4. Sept. 2012. Web. 15 Mar. 2015.

“The Role of Patents and the Wireless Medical Device Market.” Rethinking Patent Cultures. N.p., 06 May 2014. Web. 26 Feb. 2015.

The World Bank “GDP growth (annual percentage)” Web. 15 Feb. 2015

Tripathi, Vaibhav, and Boris Murmann. “Mismatch Characterization Of Small Metal Fringe Capacitors”. IEEE Trans. Circuits Syst. I 61.8 (2014): 2236-2242. Web. 15 Mar. 2015.

Ulama, Darryle. “2014 IBISWorld Industry Report 33441a: Semiconductor & Circuit Manufacturing in the US”. Web. 15 Feb. 2015

United States. U.S. Copyright Office. “UNITED STATES CODE TITLE 17—COPYRIGHT”. N.p.: n.p., n.d. *WIPO*. Web. 25 Feb. 2015.

“World Intellectual Property Organization.” Washington Treaty on Intellectual Property in Respect of Integrated Circuits. World Intellectual Property Organization, n.d. Web. 24 Feb. 2015.

“1959 - Practical Monolithic Integrated Circuit Concept Patented” 1959 - Practical Monolithic Integrated Circuit Concept Patented - The Silicon Engine | Computer History Museum. N.p., n.d. Web. 24 Feb. 2015.

Yang, Xiao. et al, “Design of Low Power Low Noise Amplifier for Portable Electrocardiogram Recording System Applications”, IEEE Xplore Database, Web. 15 Feb 2015.