Transistor Circuits for MEMS Based Transceiver

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MEMS-based wireless Transceiver

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This **Masters Project Paper** fulfills the Master of Engineering degree requirement.

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Final Report

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I. Project Description

In recent years, the push for low power wireless sensor networks has called for the introduction of RF-MEMS transceiver devices capable of operating on scavenged power. The design of ultra-low power MEMS based transceivers stands to revolutionize the fields of industrial monitoring, environmental monitoring, and biomedical imaging.

This report demonstrates a MEMS based transceiver capable of supporting these low power applications. Included are design and simulation results using transistor circuits implemented with a commercial TSMC 180nm technology. The entire system is estimated to consume 57.8uW of power at a Vdd=1.8V, duty cycled at 50%. The transceiver system implements a modified OOK modulation scheme and utilizes a MEMS resonator, an oscillator, an envelope detector, a comparator, a power amplifier, and an output buffer. The system is currently optimized for data rates of 5kHz, but can easily support much higher data rates. This design demonstrates operation at 60MHz VHF, but the tunable nature of the MEMS device allows for use of frequencies up to UHF.

The remainder of this report is organized as follows. Section II explains the current state of the industry that the transceiver is to be commercialized in. This section also uses that information to propose a viable go-to-market strategy for a startup seeking to commercialize this technology. Section III presents a detailed description of my individual contributions toward the Capstone project. Section IV is a consolidated paper with brief descriptions of the performance of each individual block in the transceiver architecture. It also includes simulation results showing the performance of the transceiver as a whole after all individual work was integrated together. Section V finishes with concluding reflections on the progress of the capstone project and potential directions for future work.

II. Industry Analysis and Proposed Market Strategy

This paper provides a detailed industry analysis of our MEMS transceiver chip by first comparing against other competing technologies already present in the market and then proposing a viable go-to-market strategy with our technology. The biggest competitors to our MEMS-based wireless transceiver technology are WiFi, Zigbee, and Bluetooth. Therefore, we begin by proving our transceiver technology as a viable competitor against these existing technologies due to lower cost and lower power consumption. Despite this fact, our analysis of the wireless semiconductor industry using Porter's five forces will show that barriers to entry into this industry are extremely high. We identify an alternate strategy to bring our technology to market; we plan to vertically integrate our technology into an electrical sensing system for agriculture. We will show that we can not only exploit the weak forces in the agricultural sensing systems market, we can also capture most of the value chain by having exclusive access to our MEMS technology. By entering the agricultural sensing market, our strategy is to dominate the market by being both a chip designer and a systems manufacturer.

The objective of our capstone team is to build a fully-functional low power transceiver chip that successfully integrates a microelectromechanical system (MEMS) resonator. We accomplish this by creating a strict power budget of 60 micro watts for the entire system and using block-level design methodology to implement the CMOS transistors in the transceiver chain. We conduct this process in three steps. First, we create a schematic of our transceiver circuit and verify its functionality in simulation. Next, we implement the layout that corresponds to our schematic by

designating the locations of connections, wires, doped wells, and metal layers. Finally, once the chip has been fabricated, we need to use PCB boards to conduct the final tests needed to verify its operation. These steps will allow us to achieve a low-power MEMS transceiver chip that is ready for commercial use at the end of the year.

Before discussing about specific competing technologies to MEMS, it is important to appreciate the context of how transceivers operate and what are some design metrics for a good transceiver. This paper will first distinguish the power advantages of our MEMS transceiver chip from other conventional transceivers. We will then show why these advantages are relevant by illustrating the need for minimizing power use in today's transceiver applications.

Transceivers allow for wireless communications by transmitting and receiving wireless signals. To avoid interference, signals traveling in the air must travel in different frequency channels. This often requires them to be converted into higher frequencies in a process called modulation. When the signal then reaches its destination, the receiver then needs to recover the original signal from the modulated signal in a process called demodulation. It is the job of the transceiver to modulate and demodulate signals being sent and received; it does this by using a resonator to generate a reference frequency that is tuned to the desired sending or receiving frequency of the signal.

When designing a transceiver chain, the most difficult problem is isolating the desired signal from other unwanted signals that are received from the antenna. Engineers define the Q factor of a resonator as its ability to resonate at a specific frequency. Resonators with a low Q factor are less selective; they resonate not only at the tuned frequency, but also at other nearby frequencies. For smaller channels, the Q of the resonator needs to be high in order to minimize insertion loss, or loss of signal strength (Nguyen, 2013, p. 112). Most conventional transceivers

implement resonators that need additional filtering to isolate the signal. This costs power. Although we would like to fit many channels into our band, smaller channel bandwidths require stronger filtering and consume more power.

Herein lies the advantage of MEMS technology. Mechanical resonators generate larger Q factors than resonators using quartz crystals. MEMS resonators provide record on-chip Q factors operating at gigahertz frequencies while still maintaining excellent thermal and aging stability (Nguyen, 2013, p. 110). In particular, the capacitive-gap RF MEMS resonator that we use for our MEMS transceiver circuit produces exceptionally high Q around 100,000 and can be tuned to select 1kHz-wide channels over a 80kHz range (Rocheleau, Naing, Nilchi, & Nguyen, 2014, p. 83). The high Q factors of MEMS resonators eliminates any steps involving additional filtering and takes away the power consumption overhead required for reducing insertion loss from the resonator. Eliminating the filtering step also results in a simpler design for the system as a whole.

Next, this paper provides examples of applications using our low-power MEMS-based transceiver to show its relevance in the market today. The main interests of our technology will come from wireless sensor node markets, where low power and simplicity are much more important than data transmission rate (Rocheleau, Naing, Nilchi, & Nguyen, 2014, p. 83). Since the wireless sensor market is wide and diverse, this paper uses body area network (BAN) sensors and environmental sensor networks (ESNs) as case studies to illustrate the needs for simple, low-power transceivers.

BAN sensors are used to collect information directly from the person's body. Designers integrate BAN sensors into smart textiles to detect the wearer's heart rate, stress, motion, and energy expenditure (Peiris, 2013, p. 1). A transceiver chip will then enable the sensors to send this physiological information to an interface where either the person or a medical professional can

view it and form educated decisions. The biggest challenge with these devices is miniaturizing the BAN node and keeping it low power while maintaining a broad range of applications. A full on-chip application-specific implementation for BAN has already been designed using the wireless protocol Zigbee and consumes approximately 4mW of power when transmitting and receiving. A tiny lithium coin-cell battery can easily provide enough power for this radio. Although current implementations of BAN are functional, an approach to combine MEMS technology with ICs has already been discussed as the next step to further miniaturize the features of the BAN project (Peiris, 2013, p. 2). If we decreased power consumption from the milliwatt range to the microwatt range using MEMS, the battery life will increase by several orders of magnitude.

ESNs are another area where we can employ low-power transceivers. These sensors constantly monitor the natural environment to study how they work and detect natural hazards such as floods and earthquakes. The transceiver allows for communication between the sensors and a Sensor Network Server, where it can be viewed at a base station (Hart, Martinez, 2006, p. 178). The biggest advantage of ESNs is that they allow us to monitor remote or dangerous areas that have long been inaccessible to study (Hart, Martinez, 2006, p. 177). The designer of these sensors needs to satisfy both low power and low maintenance constraints; these will ensure that the system will operate with minimum intervention for sensor maintenance or changing batteries. MEMS technology can provide the low power and simplicity needed for these sensor nodes. An approach to build tiny cubic millimeter sensor nodes called Smart Dust using MEMS technology has already been proposed, although environmental robustness is an additional design constraint for this particular application (Hart, Martinez, 2006, p. 180).

We have shown that some wireless sensor applications such as BANs and ESNs need ultra-low power transceivers. To show that MEMS is a feasible technology, we now require a closer

examination of the major competitors in wireless sensor applications. The most recognizable competing technology in wireless communications is WiFi. WiFi is the biggest threat to our technology because of its wide use in applications from cell phones to computers. Because it is supported across many platforms, WiFi is even used extensively for smart wearable and connected medical device applications. Thus, WiFi takes a sizeable chunk of the market that we hope to apply our technology. The cost per WiFi chip is moderately expensive at a bulk price of $3 for 1000 chips (Smith, 2011). Although this cost is slightly inflated, WiFi's biggest strength is that it is the fastest means of wireless communications in the industry. Supporting up to 11 to 54Mbps (megabits per second), WiFi takes a commanding lead over the second fastest wireless method, which is Bluetooth at 1Mbps (Smith, 2011). This means that WiFi transfers data up to 54 times faster than Bluetooth. Our transceiver can be configured for high data rates but at the expense of additional power consumption. Therefore, to secure a special niche for low power and low cost, our design is not optimized for speed. We operate at speeds of 200kbps, which is much lower than WiFi. However, the relaxed speed constraint allows us to design our transceiver architecture to be much simpler than typical WiFi chips and less costly as a result (Dye, 2001). By using a simple design, our MEMS-based chip is expected to be less costly at about $2.5 for 1000 chips.This is another strength of our MEMS transceiver in addition to the aforementioned low-power advantages from using a high-Q MEMS resonator. Although WiFi is a major competitor in the wireless communications field, low power applications that do not require excessively high data rates should favor our transceiver over WiFi.

Zigbee is another wireless communication method that is less recognizable because it does not directly target the consumer market. However, Zigbee is widely used in some battery powered systems such as home networks, and smart watches that require moderately long distance

communications (Lawson, 2014). Zigbee accomplishes long distance travel with intellectual property known as mesh networking. Mesh networking is a method of having all the devices in a given area working together to transmit your information. For example, in city of 100 smart phones spread out evenly, information can be transmitted across the entire region by having phones send information to each other and successively passing data forward one phone at a time until the data reaches its the final destination. This type of networking is analogous to a relay run where runners pass the baton to subsequent runners until the finish line is reached. By utilizing this type of IP, Zigbee is able to serve information across very long distances and therefore commands the market of long distance communications.

Our technology can also achieve long distance travel by using low frequency techniques. High frequency networks that do not use mesh techniques cannot travel far because higher frequency signals have a larger probability of disappearing when coming into contact with obstructions like buildings. In comparison, lower frequency signals can wrap around obstructions without losing data. Therefore, implementing low frequency signals in our design allows us to compete with Zigbee's long distance travel. A weakness of using Zigbee chips is that they need to always be powered on in order to accurately pass information through. In networks of battery powered cell phones, Zigbee will drain batteries very rapidly. Our transceiver chip easily beats Zigbee in power consumption because our chip does not need to be powered on at all times to achieve long distance travel. Furthermore, as a result of the mesh network design, Zigbee requires complicated circuitry and this makes their bulk price very costly at $3.2 for 1000 chips (Smith, 2011). The clear advantage that Zigbee has is in addition to long range is that their data rates are higher at 500kbps. However, much like the argument against WiFi, our design relaxes the speed constraint for optimizing cost and power consumption. Our chip has the competitive advantage in

markets that require low cost, low power chips for long-distance, battery-operated devices that can tolerate producing moderate data rates.

So far, we have discussed Zigbee and WiFi as two major competitors of our technology. These two standards currently dominate the long distance travel market and the wearables market, respectively. Our transceiver chip hopes to steal some of the market share by offering low power alternatives with comparable long distance capability for battery powered devices. However, it should be said that Zigbee and WiFi are not the only two competitors. The wireless communications industry is a saturated field and there are several other standards that dominate some other markets we hope to enter.

The final competing wireless technology discussed in this paper is Bluetooth. Bluetooth is a global wireless technology standard that enables convenient, secure connectivity for an expanding range of devices and services. This is a widely used communication channel for sharing voice, data, music and other information wirelessly between paired devices such as cars, medical devices, computers, and even toothbrushes. Its wide use poses a threat to our MEMS technology. Bluetooth runs at a high frequency carrier of 2.5GHz but is suitable for sending information only up to a range of 100 meters. As we have discussed in the case of Zigbee, we can configure our system to communicate information over long ranges by choosing to operate at lower frequencies. Furthermore, the cost of Bluetooth is about 2.7$ for 1000 chip-sets and we expect to operate at roughly the same cost due to our simpler design methodology.

In the area of low power, Bluetooth low energy (BTLE), a new version of Bluetooth developed in 2011, could put our technology at great risk. BTLE ranks number one in the market list for lowest energy consumption. Known as Bluetooth smart, this wireless standard extends the use of Bluetooth wireless technology to devices that are powered by small coin cell batteries such

watches and toys. BTLE transceivers can allow these devices to runs for years on a small battery. Although BTLE is currently the industry leader in low power transceivers, this technology still operates at power levels in the milliwatt range (Siekkinen, 2012). Our MEMS transceiver is designed to operate with microwatts of power, which will provide a significant power improvement to BTLE at roughly the same cost per chip.

This paper will next identify both primary and potential end-user stakeholders of our project. Our primary stakeholders are our advisors and sponsors. These include Professor Clark Nyugen, his post-doc assistant Tristen Rocheleau, and PhD. student Thura Naing. They have written journal papers on the theory of our MEMS-based wireless transceiver and have built the initial draft circuits that prove the operation of the high-Q MEMS resonator alone. Professor Nyugen, who is the co-director of Berkeley Sensor & Actuator Center (BSAC), is also our primary sponsor for the project. Since our design is still developing, it is possible future designs can operate at higher frequency and data rate. If that is the case, it will draw more attention and interest from different industries. We currently do not have any issue with budgets since BSAC fully sponsors the project. However, collaborating with top companies like Apple and Samsung would be a reasonable choice if we need to look for other sources of budgets in the future.

Since this project is still in progress, we currently have no actual end-users using our transceiver chip. However, we use market analysis to identify potential consumers and applications that require wireless transceivers with low power consumption. Since we have already discussed several case studies of potential applications, this section focuses more on potential consumers. From the consumer's point of view, our low power chip means that consumers would no longer need to replace their battery very often. People using sensors implanted in the human body will find our technology very necessary. Implantable medical electrical devices gradually become

feasible as an assisted medical treatment, especially for detecting biological signals that doctors can use to monitor the condition of the patient. These implantable devices need extremely low power to prevent any potential harm to the body. If the device consumes a low enough amount of power, the energy provided to the device can be acquired from the body itself through energy harvesting, allowing the device to operate for an indefinitely long period of time. For this reason, companies specialized in biomedical imaging may also be interested in our product.

Besides applications in the medical field, the market of our product can also be expanded to other broad fields. Wearable electronic devices have recreational, scientific research and even military uses. These devices need low power transceivers because they often cannot be charged frequently or conveniently while in use. For example, in environmental science, it is necessary for scientists to tag the animal to track their migration and living habit. The longevity of the tagging device is important to maximize the time the device is continuously transmitting signals back to the research center without any battery replacement. Moreover, there are some situations that the battery life is critical. For military applications, the wearable device should have a long life to work in any emergency situation, since it would be terrible if the device was running out of power in a critical moment. This simple consumer-focused analysis, together with the application-focused analysis presented at the beginning of this paper, shows a strong likelihood of a potential market for our technology centered around wireless applications that specifically require low power.

Although market analysis presents many exciting possibilities for our technology, it does not produce a feasible go-to-market strategy for our technology. We have already alluded to abiding by a strategy to vertically integrate ourselves forward into producing an agricultural sensor for end-users. We will conduct a detailed industry analysis using Porter's five forces to justify this decision (Porter, 2008). More specifically, we will compare the barriers to entry between the

precision agriculture industry and the semiconductor industry to show the infeasibility of selling our transceiver as a standalone chip in a startup company. In comparison, we discuss how we as a company in the precision agriculture industry will manage the threat of new entrants to ingrain our success in this industry. We will then analyze the other forces in the context of the precision agriculture industry to further show why it is a more appealing alternative to our startup strategy.

To understand how it is possible to vertically integrate, we first introduce the typical value chain for a sensor product. GTQ, a company that produces sensors, identifies five major sectors in this value chain: fabricating the chip inside the sensor, integrating the chip into a sensor, creation of a probe, adding additional electronics to create a measurement system, and adding software to develop the instrument for a specific application (Sensors Value Chain). Companies selling individual, general-purpose sensors like GTQ occupy the first two sectors while instrumentation companies would occupy the other sectors by customizing for a specific application. We envision ourselves as an instrumentation company. However, while a typical environmental sensing company would purchase all of its components, our strategy is to do the same for everything except for the wireless transceiver chip, which is the final product of our capstone project and will be further developed as part of our company's IP.

There are two reasons why we have chosen to vertically integrate forward. The first reason is related to where the value lies in this value chain. The sensor instrument marketed to the end user costs much more than the general components a company like QTR would sell to instrumentational companies. Two of our competitors in the agricultural sensing industry - ConnectSense and Twine - sells environmental sensors at costs of $149.99 per unit and $214.99 per unit. On the other hand, individual sensors supplied by the circuit board & global electronic parts manufacturing industry

average to about 10 USD per module. By choosing to go into instrumentation, we will position ourselves to obtain most of the wealth in this value chain.

The more important reason is that barriers to entry in the industry of circuit manufacturing are very high. IBIS, a provider of industry-based research, describes this industry of selling "widely available general purpose chips" as being dominated by existing major players. IBIS states that "the size of existing participants in the industry means new entrants need to spend more on marketing to establish industry links and gain market presence" (Ulama). In Porter's words, the incumbents in this industry can access distribution channels that newer entrants cannot (Porter). There is also the issue of brand name; IBIS argues that companies are reluctant to "risk the quality of their own products" by purchasing from startups in this space (Ulama). Furthermore, Porter argues that intense price competition occurs when different companies sell undifferentiated products, which applies in this industry (Porter). The production of semiconductors at reduced costs favors larger companies that have larger "production throughput" and "plant technology" (Ulama). These situations are unfavorable for startups, who would get quickly outscaled and outcompeted in response even if they developed a novel technology that allowed them to temporarily penetrate the market.

In comparison, the barriers to entry in the industry of precision agriculture are less intense. IBIS states that the main issue is finding highly skilled workers who know how to "incorporate several communications protocols, from GPS to Wi-Fi…" (Antayle). However, as electrical engineers who have developed a transceiver chip, we are well-versed in this knowledge and are therefore in a good position to enter the industry. IBIS also states that "almost two-thirds of revenue (is) up for grabs among many small players", which further supports why we should enter this particular industry (Antayle). Furthermore, IRIS rates competition as being low in this industry

since firms can “compete on the basis of enhanced functionality or widened application” rather than on price alone (Antayle). Therefore, we will not receive much retaliation if we entered this industry as compared to the circuit manufacturing industry.

A key issue to address is how we as incumbents of the precision farming industry will address the threat of new entrants. It is true that the absence of big players in this industry may allure other competitors into this space. However, as was presented in the value chain analysis, most instrumental companies purchase their components rather than manufacture their own. Our company would have exclusive access to MEMS-based transceiver technology, which based on our previous paper on competitive analysis will outcompete existing transceiver technologies in both cost and low power. Herein lies our competitive advantage. IBIS argues that one of the key success factors in this industry, in addition to having the aforementioned highly trained technical labor, is the “protection of intellectual property/copyrighting of output” (Antayle). New entrants that plan on purchasing components will not have access to this technology; therefore, we can inherently build the better sensor instrument just from having better transceiver technology for this application.

This paper will now present the rest of Porter’s five forces solely in the context of the agricultural sensing industry to further strengthen our identification of this as the industry where our technology can flourish. Since this paper has now shifted its focus specifically to the agricultural sensor industry, we begin by briefly introducing the need for sensors in agriculture. We then begin discussing the remainder of Porter’s five forces by presenting an analysis of the rivalry within the industry and how our technology will leverage low power consumption in order to differentiate ourselves and mitigate rivalry. This paper will draw from information previously presented regarding competing technologies – Zigbee, WiFi, and Bluetooth – in order to study our

rivals in the context of the technology they apply in their sensors. Additionally, this paper will identify how our technology, in a market with several competitors, can better serve the consumers in this industry.

There is an immense need for smart connected sensors in the agricultural industry. In 2014, IBM composed a report which stated that 40% of food produced by developed nations is thrown away. The IBM study also found that weather damages and destroys 90% of crops grown by farmers [Gerson 2014]. This statistic is disheartening considering the amount of people on this planet that can benefit from food. On top of that, farmers are dedicating precious natural resources such as water and land to grow the wasted food. Our capstone team believes we can help. Specifically, our project can provide farmers with the sensors and wireless monitoring tools they need to improve crop yield and reduce food waste. Pursuing the sensor and wireless monitoring application can disrupt the agriculture industry and the market is ready for technologies that can gather soil and other weather information. Market researcher BCC expects the environmental sensing and monitoring technology business to grow from $13.2 billion in 2014 to $17.6 billion in 2019 [BCC Research, 2014].

Wireless agricultural sensors gradually play an important role in agriculture. The use of sensors mainly helps to monitor the environment data, including the weather change, soil quality, temperature, and water quality. By collecting these data, farmers can better control the cultivate process and cut costs by reducing the waste of water and chemicals. Sensors can apply to livestock farms as well. Farmers can tag individual animals with sensors to accurately monitor their behavior, health, and body temperature. From the consumer's point of view, we are positioning our MEMS transceiver chip, and thus our sensors, to be a long-lasting system. This feature is very attractive for U.S. farms; since the average farm size today is 441 acres (Agriculture Council of

America, 2014), it is very time-consuming for farmers to manually set sensors on their farmland and then replace batteries at a later time.

In an industry study conducted by IBISWorld, the precision agriculture market is currently fragmented by players that provide farmers with surveying, agriculture construction, and asset management services [Neville 2014]. In fact, many of the companies are described as distributors, rather than developers, of third-party sensor systems. By entering this market, we will be providing farmers with a unique hardware solution rather than a service. There are very few companies in direct competition with us, and many of the rivals in this emerging market appear to be startup companies. According to Michael Porter's "The Five Competitive Forces That Shape Strategy," the intensity of rivalry among competitors can drive profits down [Porter 2008]. Our industry analysis identifies the agricultural sensor industry as having weak rivalry because most of our competitors are of equal size and power. There are no clear leaders in the market and thus, each rival exerts equal forces that are weak.

To show that most start-ups are still in the development phase, this paper re-identifies two rivals with products in the market – ConnectSense and Twine. The former company offers environmental sensors with batteries that last 3 years at a cost of $149.99 per unit while the latter offers comparable sensors that last 2-3 months and cost $214.99. The battery life of these rival products are lacking when considering their application. In a large farm where several of these sensors are used to monitor the environment, frequent battery changing or charging can become tedious. As discussed earlier in this paper, WiFi is one direct competitor to our transceiver technology. Therefore, it should come as no surprise that both ConnectSense and Twine employ WiFi technology in their units. There are also many systems proposed or in development that take advantage of other competitors such as Zigbee. For example, a Zigbee based agriculture system to

monitor soil, temperature, and humidity was described in the Institute for Electrical and Electronics Engineers (IEEE) Journal [Xialei 2010]. However, we had concluded that our transceiver technology enables us to create systems that consume less power than comparable WiFi or Zigbee systems. Taking advantage of our edge, we can position ourselves to offer a longer lasting system to solve an unmet need. Also according to Porter, price competition is likely to occur with rivalry when competitors offer similar products where price is the only differentiating factor. Because our technology allows us to have low power as the differentiating factor, our capstone team does not expect an impending price war by entering the agricultural industry.

Porter also stated that rivalry can cause a company to specialize and this creates a high exit barrier. The exit barrier for environmental sensors are low because our products have applications in many industries such as home, health, and telecommunications. Therefore, if exiting the agriculture industry becomes our only option, our resources and technology can easily pivot for applications in other markets.

This paper next analyzes the threats from our customers in the context of the industry they operate in. The agriculture market is an industry with low market share concentration. The top four companies in the Agribusiness industry account for less than 10.0% of industry revenue (Neville, 2014). The reason for the low concentration is due to the naturally fragmented feature of this industry, since the farms are never big enough to dominate the market. In the domestic market, about 97% of U.S. farms are operated by families, individuals or family corporations (American Farm Bureau Federation, 2014). The agriculture companies are generally segmented by their locations and their different agricultural products. As a result, the force from our customers are generally weak since there are a large number of companies with similar size.

Next, we present a detailed analysis of the power of our potential suppliers and how we will overcome this force. In addition to our transceiver chip, the final sensor module will consist of various components like humidity, pressure and temperature sensors supplied by the circuit board & global electronic parts manufacturing industry. As stated before, the cost of these components averaged over a 1000 modules is expected to be less than 10 USD per module. These electronic parts/component suppliers don't impose serious switching costs as they can be easily replaced due to their low cost, variety of substitutes, and negligible cycle time [Sensors Value Chain. (2012)]. Therefore, these particular suppliers are weak.

Our transistor level designs of the MEMS transceiver chip itself will need to be fabricated on a wafer before it can be used as a part of a sensor module. Our current supplier of choice for this chipset is a semiconductor foundry called Taiwan Semiconductor Manufacturing Company Limited (TSMC). Our advisors have chosen TSMC to be our foundry as TSMC offers a variety of product lines on MEMS and is best known for its strength in advanced low-power processes [IHS Technology. 2012]. TSMC also has a production capability of 16,423,625 wafers/year, which is more than all the other major foundries combined [foundry-ranking-capacity-2013-2014]. The production capacity of the foundry clearly defines the time taken by the foundry to fabricate a design. By choosing to work with the leader in production capabilities, we minimize the time we spend waiting for the chip to come back after sending off our design.

We acknowledge that the component and sensor manufacturing industries are less powerful when compared to the chipset fabrication industry due to two main reasons. Firstly, the transceiver is the most vital component in our module, and the fabs are ultimately the ones providing us with the chip. The significance in ensuring the operation of our transceiver is represented by its huge cost. The chipset costs about 60~70 USD per module, which is more than 6 times the cost of

components [IBIS World Industry Report, Sarah Kahn - January 2015]. We as chip designers are obligated to work with the best in the industry - namely, TSMC - to mitigate risks of imperfect chips both immediately upon fabrication and during the lifetime of the sensor. Secondly, the choice of supplier for the chipset is evaluated and integrated into the design process right at the beginning of a project, which considerably affects the cost of switching from one supplier to another. The entire design of semiconductors is done with technology files provided by the foundry to dramatically reduce the risk of failed chips during the manufacturing step. As a result, the layout provided by the semiconductor designer to the foundry is a significant representation of sunk costs and engineering efforts. Switching foundries will require redesigning from the very start and translates to wasted time, engineering effort, money, and product quality.

These two reasons identify our supplier as a strong force, which according to Porter endangers our profits in this industry. The best we can do to accommodate this powerful force is to formulate all of the problems in the early stages of the project and select the best supplier for us in terms of cost and performance. Additionally it is important to understand that, given that the nature of our capstone project is to design a working transceiver chip that would eventually require fabrication, avoiding business deals with the strong chip fabrication industry was not an option for us.

Finally, we will discuss the effect of substitute technologies outside of competing wireless transceiver technologies, which we have already analyzed. For the application of agricultural and agronomical sensors, wireless technology itself may not be necessary. Instead, farmers can choose to use actual wires to transmit data. By contrast with wireless transmission, wire transmission has advantages in speed, reliability and security. Not only does it allow faster and almost lossless data transmission, it also has full control of who and what gets online. It keeps away all unauthorized

visitors, therefore securing the confidentiality of the collected data. However, the disadvantages far outweigh the advantages. To build a wire infrastructure, cost is a fundamental barrier. Our target application is not restricted to an office. Instead, it might cover tens or even hundreds of acres of farmland. In this case, the wire cost is tremendous. For instance, prices for copper wires is about $100 per 1000 ft. (Southwire 2015). If we used wires to surround an acre of land, we need about 850 feet which will cost $85 with copper wires. This does not take into account the complications of the actual infrastructure, which will further increase the actual price beyond this estimation. In contrast, the price for semiconductors that constitute our wireless transceivers is steadily decreasing (IBISWorld Business 2015). Therefore, wireless technologies provide a more cost-efficient option than wired technologies.

Based on this analysis, our strongest threats are other wireless solutions. If customers are already using a wireless transceiver like WiFi or Bluetooth, our MEMS-based wireless transceiver is not the only possible low energy alternate. Energy harvesting is another viable options. This technology aims to convert ambient energy (i.e. motion, solar and thermal energy) into electrical energy. The danger of this technology against our position as a energy efficient solution is that customers may choose to integrate energy harvesting technology to their pre-existing WiFi or Bluetooth transceivers. Since this technology has already been successfully implanted into some watches, the technical barrier to combine energy harvesting and existing wireless transceivers is small. However, their main weakness is still cost. If our customer has no existing agricultural sensors, then our product is definitely cheaper than the combination of a WiFi or Bluetooth based sensor with additional circuitry for energy harvesting. In general, the threat of substitutes for our product as an agricultural sensor is weak.

This paper now concludes by summarizing the points made regarding the viability of our go-to-market strategy and the competitive advantages of our MEMS transceiver technology compared to other existing wireless technologies. We have analyzed the agricultural sensor industry using Porter's five forces to show that, apart from the inevitably strong supplier force, the other forces are weak enough to justify our decision to vertically integrate into this industry. This is a strategy made in contrast to directly entering the semiconductor industry as a startup and handling its high barriers to entry. We have also shown that our simple design architecture for our transceiver results in competitive advantages of low power and low cost for our MEMS-based wireless transceiver relative to the existing technologies WiFi, Zigbee, and Bluetooth. Although advantages exist for using MEMS technology, it has the danger of being overshadowed by these three commonly-used and widely-trusted technologies. Our go-to-market strategy will ensure that our MEMS technology can successfully outcompete in metrics that are very relevant to the agricultural industry (cost and power) without being overshadowed by the brand names of these existing technologies.

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III. Technical Contribution

Section I: Project statement

In order to complete this project, the five members in our team have divided the tasks --- Kelvin Liang designs envelop detector; Darryl Yu is responsible for voltage buffer; Yuehan Xu works on oscillator design; Soumya Mantha focuses on power amplifier; and I take the challenge to develop a comparator. The reason to design this comparator aims to convert analog sinusoidal wave signals into "0" and "1" digital signals. Therefore, this comparator is extremely important for its indispensable position. If it malfunctions, the accuracy and reliability of the data will deteriorate seriously.

Section II: Design flow and literature review

Understanding the importance, I need to first fully aware the details of this comparator's functionality. When Frequency Shift Keying (FSK) modulated signals enter the transceiver as seen in figure 1a, they give rise to the periodically restarted oscillation waveform (Figure 1b) (Tristan, 2). When its envelope is detected (Figure 1c), the job of my comparator should be able to discriminate "0"s and "1"s as the envelop amplitudes exceed the trigger voltage, recovering the original data (Figure 1d) (Tristan, 2). This is challenging as no previous work has been done by our graduate mentors for this part of the circuits. They bought commercial CMOS operational amplifiers from DigiKey in their early testing procedure. However the size and power consumption of such amplifiers would never fit for an on-chip design. I need to design everything from scratch.

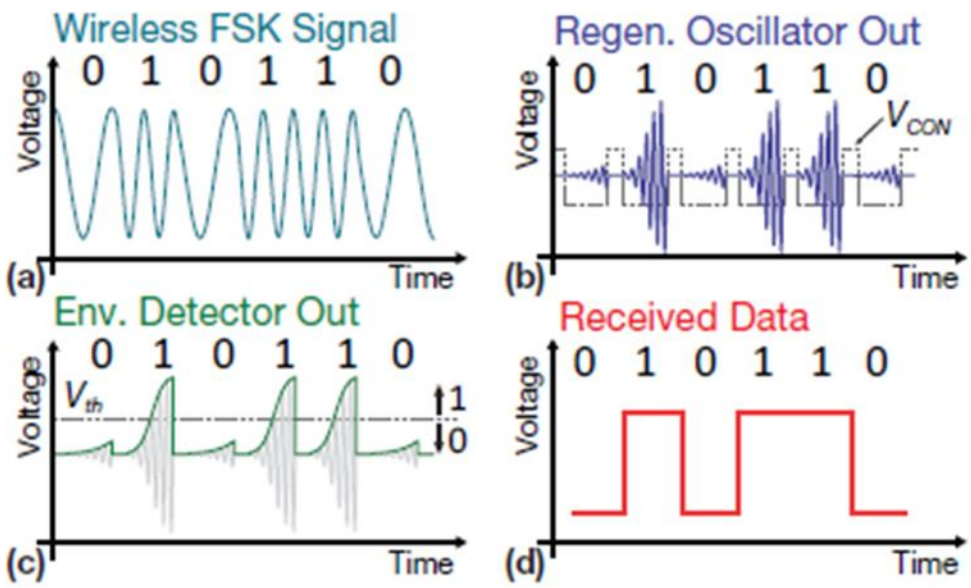


Figure 1 (Tristan, 2)

Before doing the actual design, I still have to figure out the technology. We are using the 180nm technology from TSMC, a tiny size that the knowledge I have learned previously from my analog circuit design class may not fully apply. That is, the Square-Law model no long suffices to design the actual circuit as it suffers from leakage and variability introduced by manufacturing and other physical limitations. Realizing this fact, I used another approach called "gm/id" methodology. The key idea of this method reveals the relations between circuit parameters with pure simulation methods instead of mathematical models. For example, after I complete all simulations, I could figure out what parameters to change in order to increase or decrease the current to the amount I desire.

After finishing the preparation, I then need to decide the general structure and architecture of my design. This is an iterative process as the specifications and new problems during the design force me to modify or change the topology whenever necessary. Once I obtain some hints or designs from the papers, I will need to analyze or verify with actual simulation tools. The software

we are using are Cadence Virtuoso5, and the models are provided by TSMC. It is possible that the design might not work in our simulation as the models are different. That is where I need to modify the circuit. Moreover, in this project, I have kept learning from both the project itself and coursework like analog circuit design. The more I know, the more thoughts I have while designing my comparator circuits. Hence this process iterates multiple times before I reach an acceptable solution.

So, what is the analog description of our comparator? This comparator would have two inputs, one from the data generated and modified by oscillator and envelope detector, the other from a set reference voltage. The comparator needs to amplify the difference between the two inputs. If the data input is higher, the positive difference would amplify the output to supply voltage, which is known as "1" in digital circuits; if the reference voltage is higher instead, the negative difference would drop output ground, which is "0". This function is the same as a differential operational amplifier. Therefore, the initial design I have thought of is to use CMOS operational amplifier as a comparator. Another reason I choose this topology is because it has been used in previous testing conducted by our graduate mentors. However, as I mentioned before, they bought a commercial one which is off-chip. My goal is to design an on-chip CMOS operational amplifier that satisfies the functionality of a comparator.

I have two choices for this design. One is to design a multi-stage amplifier that has small gain for each stage. One could derive the final gain by multiplying these small gains. For example, if I want to build an amplifier with gain 10000, I could build a 4-stage amplifier with stage gain 10. Yet, there are several problems with this topology. A multi-stage design means that the number of transistors also grows multiple times to that of a single stage one. As circuit designers, we do not favor large area for an on-chip design. Also, each stage has to consume power respectively.

The expected increment of power consumption is a bane for our project since we are aiming at ultra-low power. Hence, this topology might not be a viable option. The other possible way is to design a single stage differential amplifier with extremely large gain. This topology, by contrast, has the advantage of low power and small area. However, the tiny bandwidth is the price I have to pay for this design. In CMOS circuit design, gain and bandwidth are trade-off for each other. The high gain leads to a small bandwidth that only allows signals with low frequency to pass to the output. In other words, this design may pose risk of losing data. By evaluating both options, I decide to reject CMOS operational amplifier as the architecture of my comparator design.

Technical papers from Institute of Electrical and Electronics Engineers (IEEE), the world's largest professional association for engineers, provide ideas for other comparator designs. From one of the peer reviewed paper, I learn the latch design for comparator (Figure 2a). This design is clocked and generates two phases --- "reset" phase and "evaluation" phase (Ali Valaee, 1). These two phases are present for all the subsequent comparator designs. Particularly for this design, when the clock is on, the circuit is in "reset" phase. The outputs will be pulled down to ground by NMOS transistors M3a and M3b during this phase. When the clock is off, the circuit is in "evaluation" phase. It then starts comparing the input signals. This is a traditional digital comparator design for an SRAM. This design could operate at 600MHz with 18 micro-watt power consumption under a supply voltage of 0.9V (Ali Valaee, 1). However, several problems occur in my analysis and verification. Firstly, the value the capacitance for the capacitors at the output might be a burden. For a digital circuit design, this is not a big issue. Yet, for an analog comparator design, we do not want these capacitors because they consume a large area and likely to drag the performance of the circuit. Secondly, during the "reset" phase, not only the NMOS transistors are pulling down the output, PMOS transistors are also trying to pull it up. Hence, the recovery time for outputs to return

to ground voltage is relatively long in this case. Thirdly, the regeneration of output signals in "evaluation" phase might be slow. From Figure 2b, I see that the time taken for the output to regenerate is about 2us. This might be acceptable for some applications, but in our case, I would like to shrink this regeneration time as small as possible in order to have a better bit rate. Fourthly, power consumption is too much for our project. This design will consume more power since we are operate all our circuits under 1.8V instead of 0.9V in the paper. It already exceeds the limit for our target power consumption. The last concern is the kickback noise. This problem arises because of the large parasitic capacitance connecting input and output. Yet, this problem is relatively trivial in our case. The kickback noise is a serious problem if I need to drive my comparator at hundreds of MHz or even GHz range. In practice, the rate of comparison for our comparator is as low as about 5 kHz, leaving enough time for this noise effect to diminish. Considering all these problems, this design may be far from the best choice, but it provides hints for a different design from operational amplifier.

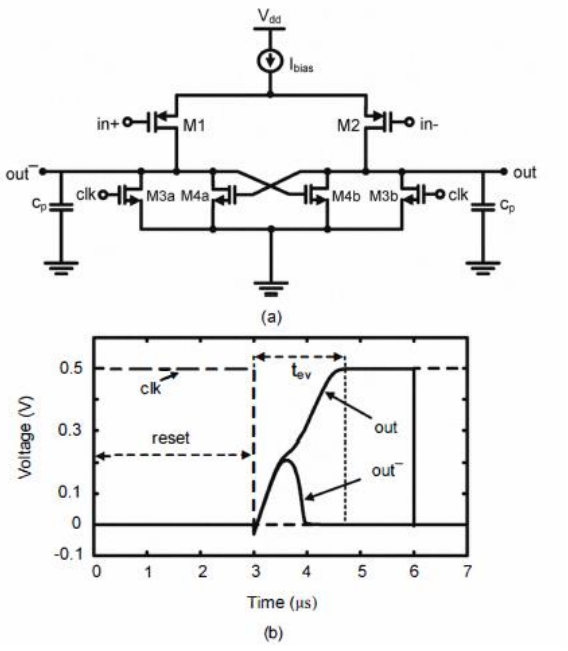
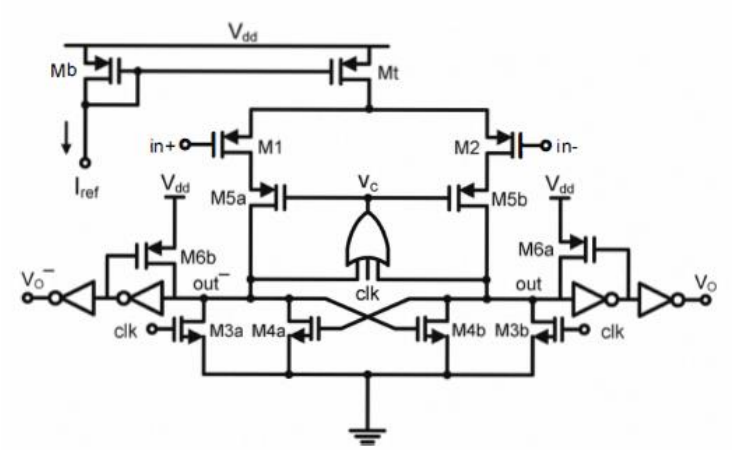


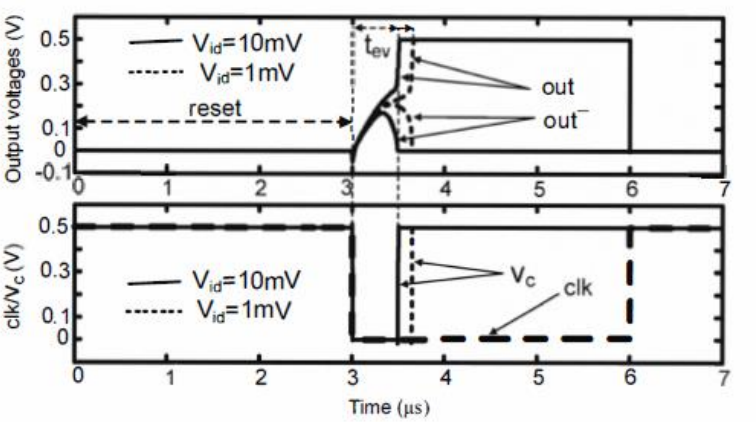
Figure 2 (Ali Valaee, 1)

In the same paper, the author builds another design based on the previous latch comparator, as shown in Figure 3a. This design aims to solve the power consumption problem of the previous design, and it has some advantages on other concerns as well. By contrast, this design has two modifications. One is an OR gate controlled PMOS pair, the other is a pull-up network circuit comprised of one PMOS and two inverters at the outputs respectively. The functions of these added components annihilate power consumption when the comparator is not working. In the previous design, the circuit keeps consuming power, regardless of necessity. Yet in this design, when the clock is on, the output of the OR gate is always "1" that turns off the PMOS pair M5a and M5b. Theoretically, the circuit consumes no power in the "reset" phase. Also, during the "evaluation" phase, when one of the "out" signals reaches certain value (the actual value depends on sizes of transistors), it will also switch off the PMOS pair M5a and M5b, just as the mechanism in the "reset" phase. This "out" signal will then be pulled up to supply voltage by the pull-up network circuit. In this way, the regeneration time is much smaller as the job done by the pull-up network takes little time, as shown in Figure 3b. From the plot, the regeneration time is about 0.5us, which is much better since we can have higher bit rate. The recovery time is also shorter as only NMOS pairs are pulling down the output during the "reset" phase. However, the biggest benefit of this design is not as satisfactory. The author claims that this design saves much more power, but that analysis only works if everything stays ideal. That is, the author is assuming that no power is consumed within OR gate and NOT gates. It is true if I can design to generate perfect clock signals. Yet, in reality, these signals have some slope when they step up or down. It means that at some moment, these gates can be shorted, creating a huge short circuit current. When I simulate this circuit in Cadence, I see multiple spikes in the power plot caused by this short circuit. This extra power consumption is almost unavoidable. Hence, this design saves power, but not as optimally

as expected. Moreover, this design includes too many transistors. If I layout this circuit, I will have to arrange large area to place digital gates involved in this design. Also, more transistors bring more parasitic capacitance that poses risks on actual performance. That means, even though the design schematic may work in simulation, it may fail to function properly if it is produced. Hence, I still need better designs.



(a)



(b)

Figure 3(Ali Valaee, 3)

The next design is from another peer reviewed paper, as shown in Figure 4 (Amir, 2). During the "reset" phase, the PMOS M10 is open, forcing both output nodes to ground voltage. In the meantime, the NMOS M7 is close and effectively balances the voltages at outputs. The recovery time is therefore greatly reduced. In terms of regeneration time, this design also has its unique benefit. In electrical engineering, this is a typical StrongArm comparator design. Both PMOS latch pair M3 and M4, and NMOS latch pair M5 and M6 are effectively regenerate the output signals during the "evaluation" phase. Comparing with the previous two designs with only one latch pair doing the job of regeneration, the efficiency for this design increases exponentially. Moreover, I can observe advantages in power consumption. During the "reset" phase, the supply voltage is isolated by PMOS M8, since clock signal turns it off. Without any supply, no power consumption can exist except negligible leakage. During the "evaluation" phase, there is no OR gate controlled switch as the one in Figure 3a, but once the output reaches either supply voltage or ground voltage, it will turn off the latch pairs. For example, if the positive output node goes to supply voltage, it will turn off PMOS M4; the negative terminal will go to ground and then turn off NMOS M5. In this case, both branches in the circuits are off, providing no power consumption in theory. By contrast with the previous design, the absence of multiple gates in this design reduces extra power consumption as well. Some minor concerns relate to kickback noise, but since I have explained earlier, it is not a serious issue in our project. If anytime I feel necessary to reduce this factor, I can build a pre-amp or preamplifier circuit to separate output and input.

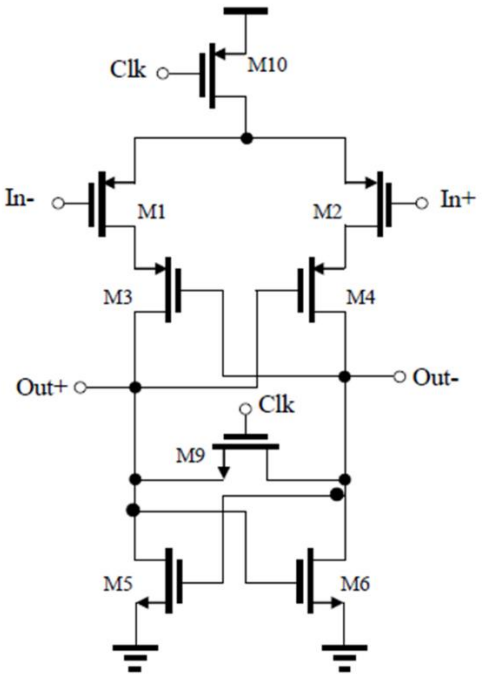


Figure 4

However, before I verify this design, I think I can make some modifications to improve the performance. From another paper that also talks about low power CMOS comparator design, the author introduces a circuit design topology, as in Figure 5. The benefit of this design is that when the clock signal is low, voltage supply and ground are disconnected to the latch by the transistor M10 and M11 (Ili, 2). Therefore in this "reset" phase, the two output voltages will be equalized to about one half of the supply voltage. In this way, the recovery time is greatly reduced since the circuit now only needs to recover half supply voltage instead of full supply voltage. Combining this design into the design in Figure 4, I develop a modified version, as in Figure 6.

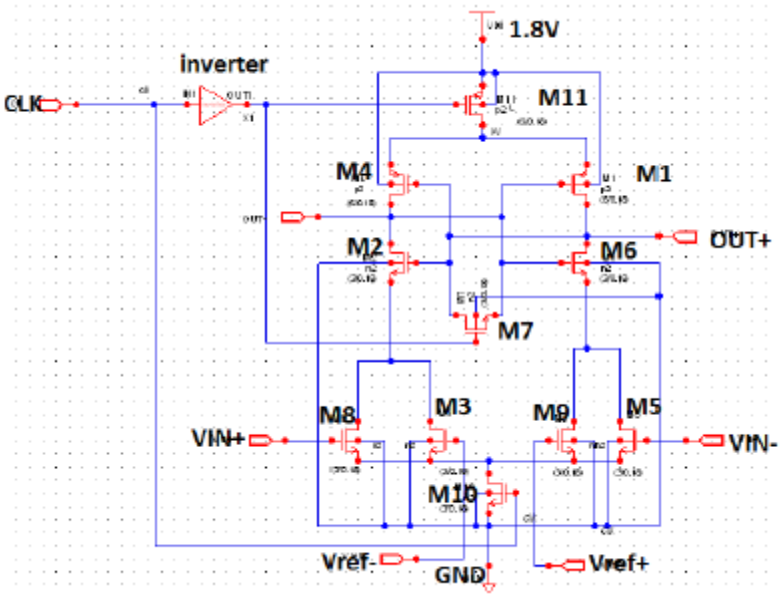


Figure 5 (Ili, 2)

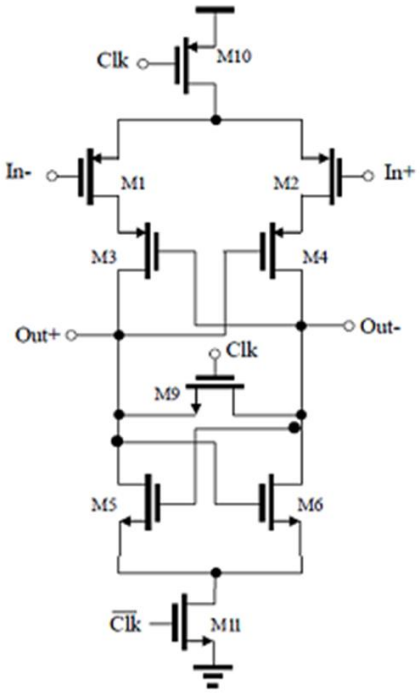


Figure 6

Section III: Verification and result analysis

I verify my design in Cadence. For simplicity, I set my common mode voltage at both inputs to be 800mV, and add 1mV differential input voltage at the positive input. The transient analysis in Cadence displays a nice square wave. The output is reset to about 930mV during the "reset" phase, and regenerate to 1.8V, the supply voltage in 8ns, as shown in Figure 7. The improvement in maximum allowable bit rate reaches almost two orders of magnitude, if we compare this result to that in Figure 3b.

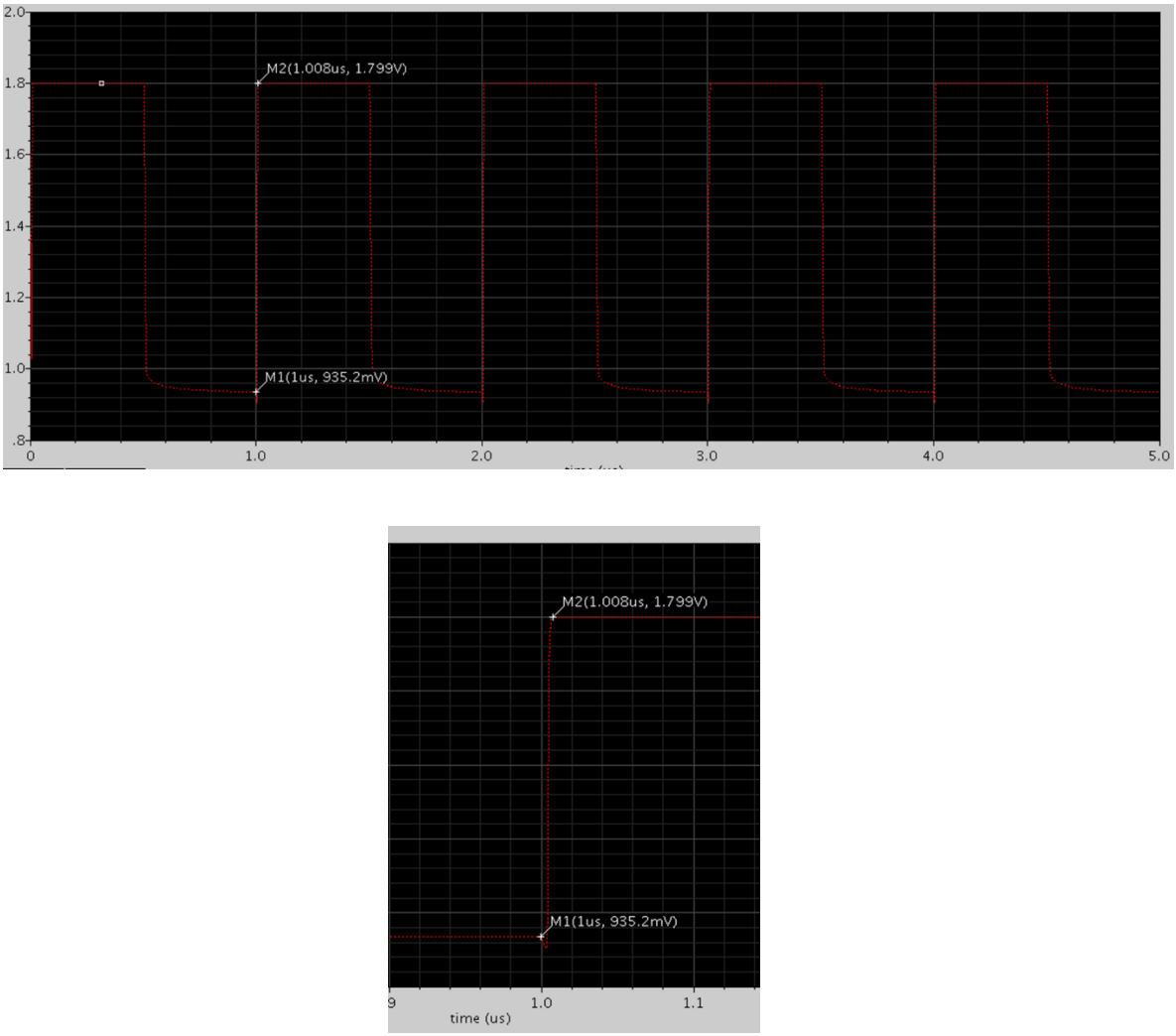


Figure 7

Till this step, my comparator design is almost done. Other problems appear in the process of integration with other parts designed by my teammates. One of them occurs when the output of my comparator inputs to a D flip-flop. As a D flip-flop is a typical digital instrument, it works effectively only when the input is close to ground or supply voltage. Though my comparator works well by its own, its magnitude of half supply voltage is a bane to the flip-flop. To solve this problem, I add a PMOS at the output to pull up the voltage to supply voltage during the "reset" phase. The recovery time would increase, but not to a level as much as that of the design displayed in Figure 4. One can think of this mechanism as a linear superposition of the original mechanism and the pull-up mechanism. These two mechanisms happen at the same time but dominate by the pull-up one. Hence, the recovery time is more than that of the design in Figure 6, but less than that of the design in Figure 4. Some more power is consumed in the "reset" phase, when this pull-up component is working. To control this component, I use a clock signal. When the clock is off (i.e. the "reset" phase), it will also turn on the PMOS to enable the pull-up function. By adding this part, I have the design in Figure 8.

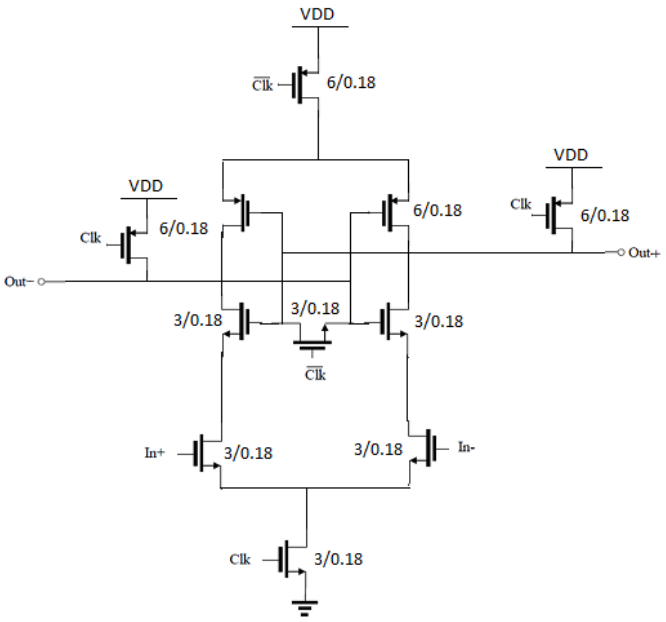


Figure 8

Another problem comes from the noise consideration. Since we are developing real chips, we have to take into account the noises from transistors. The major noise sources in my design are thermal noise and flicker noise. Also, I have to consider the noise from the output of the envelope detector. The importance of knowing the noise is that I have to make sure the input signals would be large enough to cover the noise effect. However, traditional method of simulating or analyzing linear or partially linear circuits may not apply to comparators as they are non-linear circuits.

Also, we have to notice the effect of the offset. Since comparator is sensitive to any mismatch and non-idealities, asymmetry may cause DC offset at the input. Again, for a comparator, it is hard to find its offset in simulation. Yet, both problem of DC offset and noise can be greatly reduced with a preamplifier. Adding a preamplifier will increase power, so I first need to know the rising time from the oscillator to decide if I want to make this trade-off.

At this moment, my final design is displayed in Figure 8. I may add a preamplifier circuit, depending on the further integration work with my teammates, especially Yuehan who is doing the design of an oscillator. I am starting the pre-layout and plan to finish the actual layout during the Spring break.

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IV. Consolidated Paper

This chapter of the report will provide the summary of the system level integration and performance of the receiver and transmitter. This chapter will provide a summary of the oscillator, comparator, power amplifier, and buffer blocks.

Oscillator

The function of oscillator in a transceiver system is to create a constant high frequency signal to carry the information signal. In a transmitter system, the oscillator output modulates the information signal, and the power amplifier amplifies the signal to be transmitted afterwards. In the receiver chain, the oscillator and envelope detector demodulates the transmitted signal and then sends it to comparator for decoding.

The oscillator in this system is designed as a MEMS-based oscillator, where the MEMS device is used as a resonator to replace the crystal that is used in traditional oscillators. The advantage of the MEMS-based oscillator is that it provides high Q to have a more accurate channel selection, and the simple design also contributes to low power consumption.

Oscillators typically consume the majority of power in the receive chain. Therefore, the topology of the oscillator determines the power consumption of whole system at some degree. Based on the low power consumption specification, the Pierce oscillator schematic, which consumes relatively low power, is being used. The schematic is shown below in Figure 1:

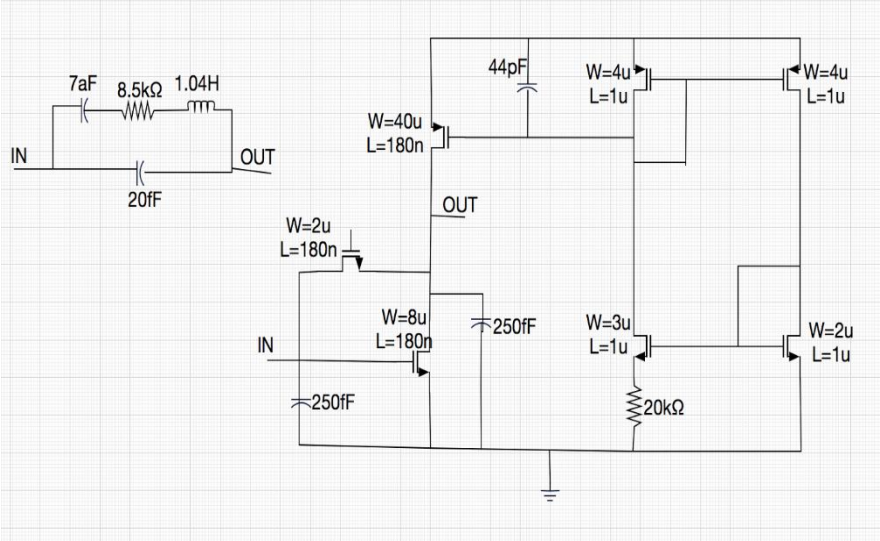


Figure 1: Pierce Oscillator

The feedback loop of this oscillator has a phase shift of 360°, and in order to make it oscillate, we also need to design for a negative resistance greater than 8.5kΩ looking into two ports of resonator. Since positive resistance consumes power, we can regard negative resistance as an energy source. If this "energy source" provides energy larger than the power consumption of resistor in the resonator, then this oscillator can work well.

According to the equation of negative resistance:

$$\mathrm{Re}(Z_c) = -\frac{g_m C_1 C_2}{(g_m C_3)^2 + w^2 (C_1 C_2 + C_2 C_3 + C_3 C_1)^2}$$

In the circuit shown in Figure 1, the nodes "IN" and "OUT" link with the MEMS device by bond pad connection, and we assume the parasitic capacitance on the bond pad is around 250fF.

The transconductance of the common source amplifier is 165.68uA/V, and the value of negative resistance is 13.66kΩ.

The output waveform and power consumption is shown below in Figure 2 and Figure 3.

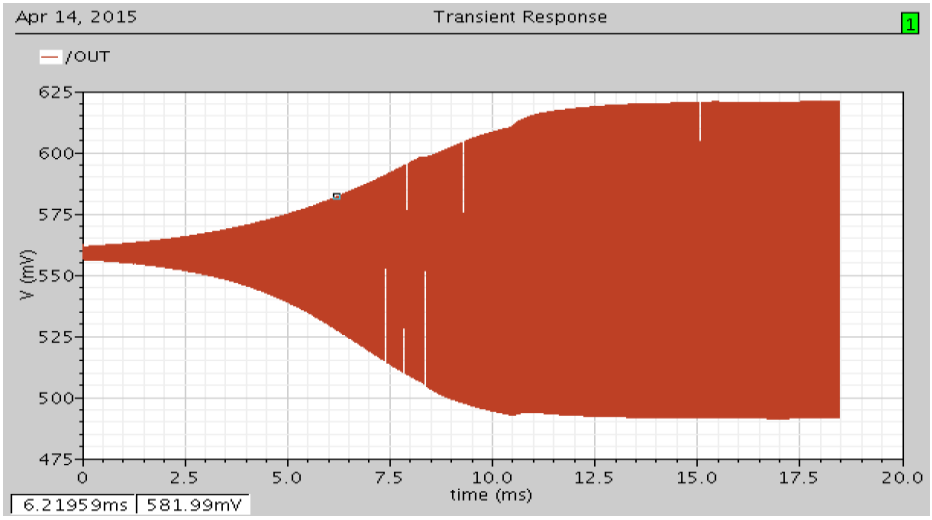


Figure 2: Growing Waveform of The Oscillator

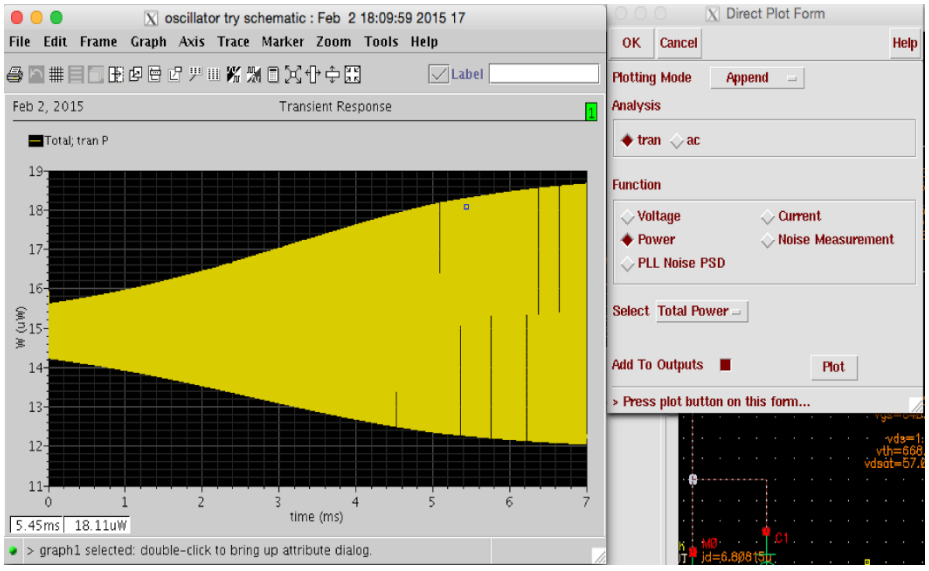


Figure 3: Power Consumption of The Oscillator

The resonance frequency of 58.98MHz, and the amplitude is 128mV. The power consumption is 15uW.

The amplitude of the oscillator output in each period differentiates ‘1’ and ‘0’. The simulation required different stimulating signals to generate the different growing speed. Further, the oscillator required a reset to toggle a ‘0’ in simulation. The reset to the oscillator was generated by switching the resonator resistance to a much higher resistance to destroy the quality factor. The stimulating circuit with a reset is shown in Figure 4.

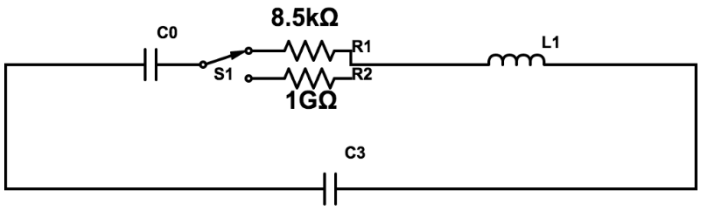


Figure 4. Stimulating Circuit

R1 corresponds to the working state, and R2 corresponds to resetting state. When the circuit switches to R2, the high resistance destroys the quality factor so that the oscillator can no longer work. The switch S1 is set to be periodically switches between R1 and R2. The output waveform is shown below in Figure 5.

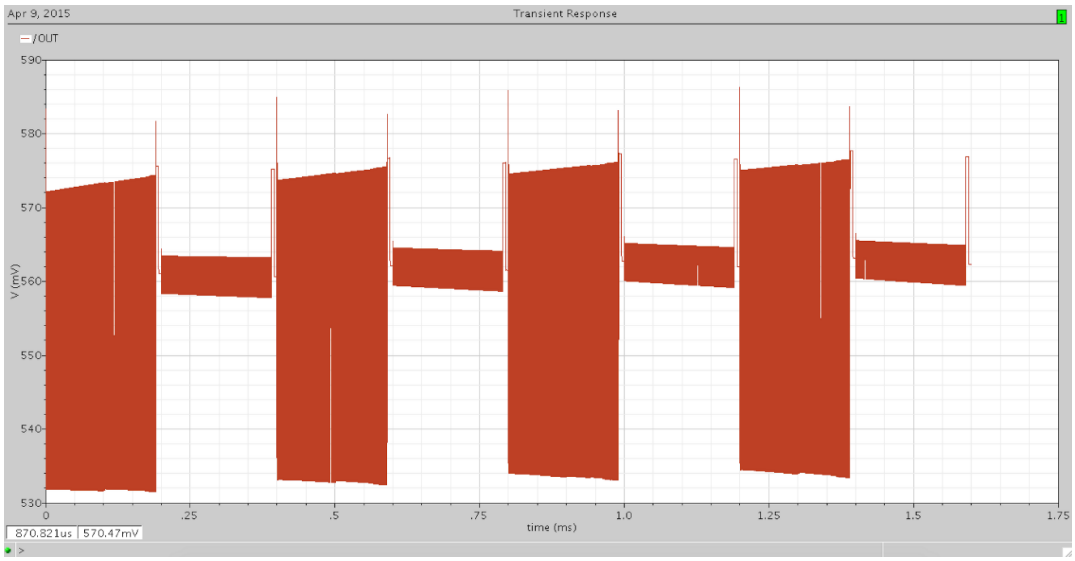


Figure 5. Output Waveform of Oscillator

In addition, an FSK signal is needed on the transmitter side. The method to generate an FSK signal is to switch the value of capacitance between two values. 7aF capacitance was used to generate 59MHz signal, and 6.5aF capacitance to generate 61MHz signal. The MEMS resonator model is shown below in Figure 6:

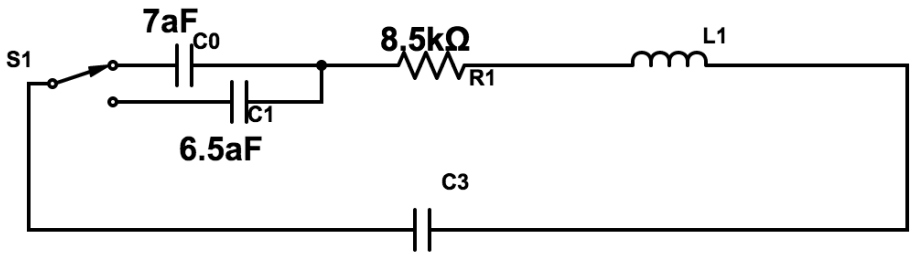


Figure 6. MEMS Resonator Model

Design Specification	Value
Resonance frequency	58.9MHz
Power Consumption	15uW

Envelope Detector

The envelope detector designed is a key piece of the transceiver system because it serves to detect the information stored in the envelope of wireless signals. In order to bias the envelope detector circuit into a temperature stable state of operation, a temperature independent current source was implemented. This temperature independent current source was also taken advantage of by the oscillator and the buffer circuits.

The design of the envelope detector had several key specifications. The consumption of the envelope detector was limited to several nW. Second, the envelope detector needed to be able to measure amplitude variations as small as several microvolts with good carrier rejection. Lastly, the envelope detector needed to be temperature independent because any variation to the bias level of the circuit will affect the threshold level of the comparator block.

Classic envelope detectors are simple to design because they require a basic diode and low pass filter circuit. However, to meet the specifications laid out above, the envelope detector used in this system needed to be based off an entirely different architecture. The main issue with using the classic diode detector with low pass filter circuit configuration, as highlighted in [2], is the need for a significant amount of gain to bring the radio frequency amplitude above the turn on

voltage of the diode. The high gain required in the classic diode detector is not suitable for our low power design. Many of the alternative envelope detector architectures capable of receiving low radio signals consumed far too much power. In [3], an operational transconductance amplifier (OTA) based envelope detector can demodulate signals as low as 257mV while consuming 6.3mW of power. In [4], [5] and [6], differential envelope detectors capable of receiving RF as low as 5mV consumed 20µW, 10µW and 1µW respectively.

The envelope detector implemented in this transceiver was designed with 180nm TSMC process. The design implemented a single ended source follower stage with low bandwidth to filter out the carrier. A PMOS biased in the triode region is used in the output stage for capacitive low pass filtering. A copy of the input branch is also used to supply the DC bias voltage as a reference voltage for the comparator. The final envelope detector, shown in Figure 22, is capable of recovering signals with amplitudes as low as 2mVpp. Overall, the envelope detector consumed 167.1nW of power.

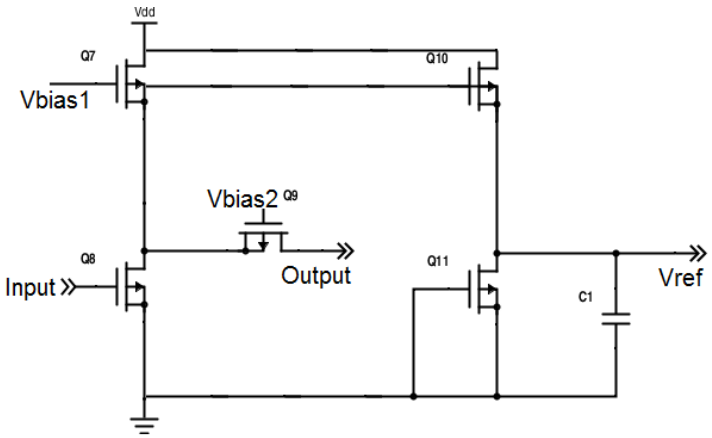


Figure 7. Single Ended Source Follower Envelope Detector

The noise equivalent circuit used for the hand calculations is shown in Figure 8. The noise simulation plots verifying the hand calculation is shown in Figure 9. From the equation below, the minimum detectable signal with a nominal noise figure (NF) and signal-to-noise ratio (SNR) requirement is

Min Det. Signal = Noise Floor + 10log(BW) + NF + SNR

Min Det. Signal = -53.9dBm

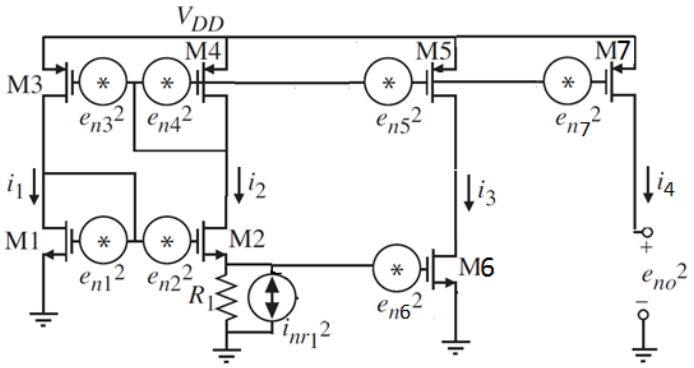


Figure 8. Noise Equivalent Circuit

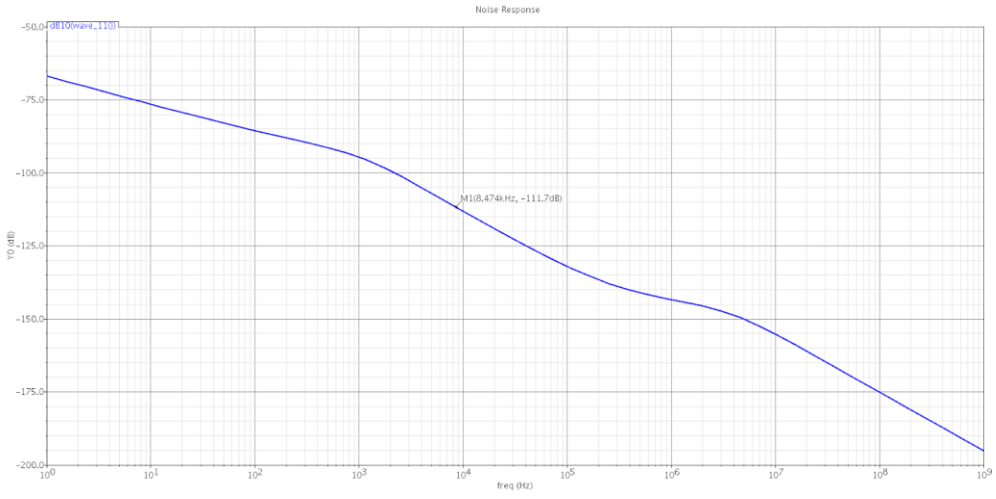


Figure 9. Noise Plot

Therefore, the minimum detectable is 2mVpp. The simulation proving the ability to demodulate signals with 2mVpp amplitude is shown in Figure 10. On the other end of the spectrum, the maximum amplitude the envelope detector can detect before clipping is simulated to be 1V. Therefore, the dynamic range of this block is

$$0\text{dBm}-(-53.9\text{dBM}) = 53.9\text{dB}.$$

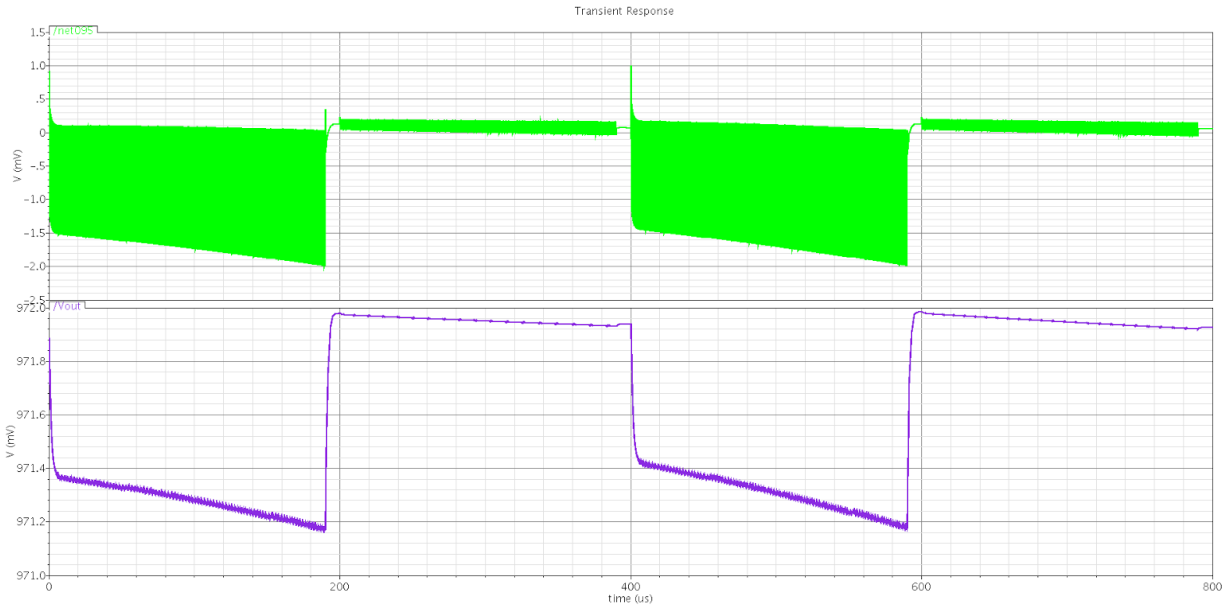


Figure 10. Minimum Detectable Signal

The envelope detector discussed was biased with 83nA of current and required stable reference supply. The design of the reference followed the methodology proposed in [7], which discusses a stable bandgap reference. The final design of the current reference is shown in Figure 11 and is capable of supplying 83nA of current with a 0.3% variation across the 0°C to 70°C temperature range. This stability was achieved by cancelling the temperature dependence of the

resistor in the circuit with a diode connected NMOS transistor in parallel. The low current supply was achieved using maximum long channel devices in 180nm TSMC transistors.

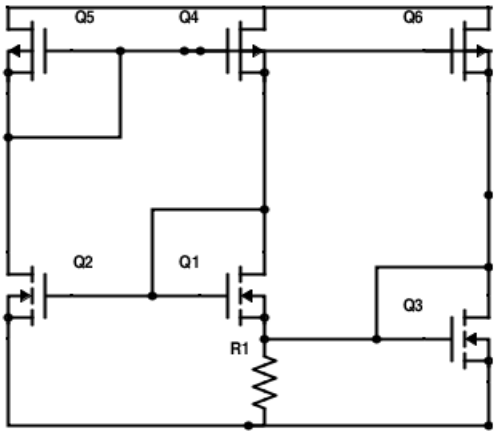


Figure 11. Temperature Independent Current Reference

The final design of the envelope detector with current reference is shown in Figure 12.

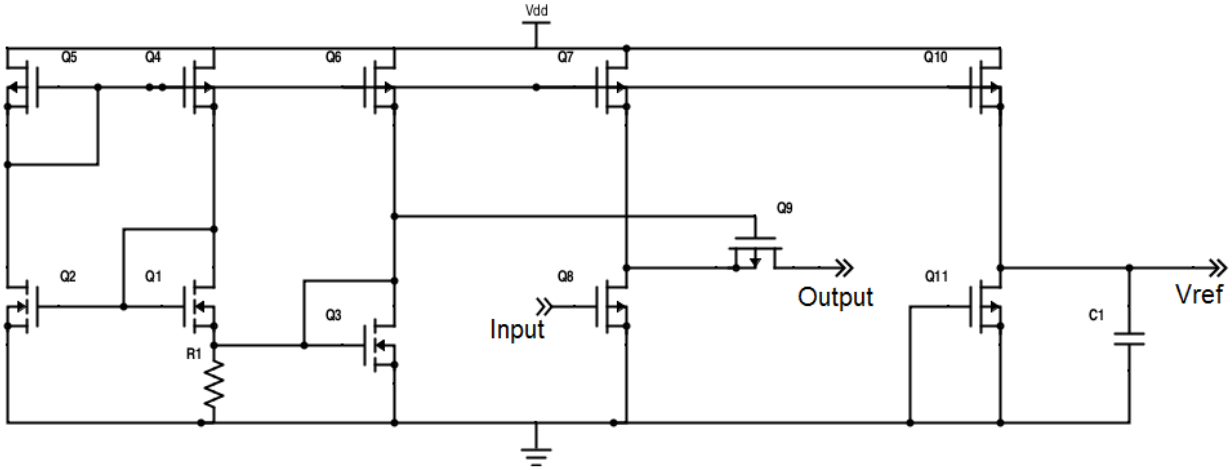


Figure 12. Envelope Detector and Current Reference

As part of the integration process, the layout of the envelope detector, current reference and the oscillator was designed. The layout is shown in Figure 7 with a die area of 750um^2.

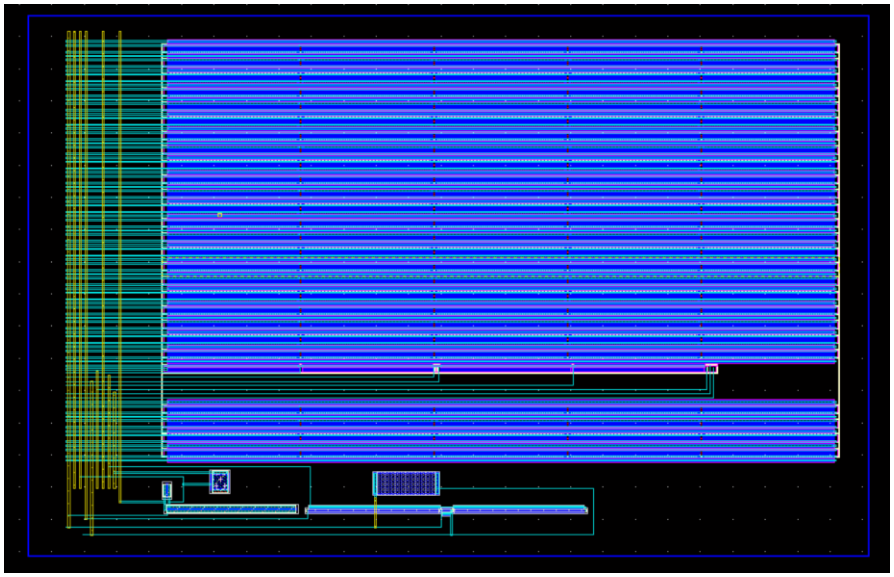


Figure 13. Layout of Oscillator, Current Supply, and Envelope Detector

Block Summary	
Envelope Detector	
Minimum Detectable Signal	2mVpp
Dynamic Range	53.9dB

Envelope Delay	.5us
Envelope Bandwidth	1MHz
Carrier Bandwidth	500MHz
Total Power Consumption	167.1nW
Current Reference	
DC Current 0°C	83.21nA
DC Current 25°C	83.55nA
DC Current 70°C	83.89nA
Total Power Consumption	250.6nW
Layout	
Die Size (Oscillator, Envelope Detector, Current Source)	750um^2

Comparator

When Frequency Shift Keying (FSK) modulated signals enter the transceiver, they give rise to the periodically restarted oscillations [1]. When the oscillation envelope is detected, the comparator should be able to discriminate “0”s and “1”s [1].

The schematic for the comparator is shown below in Figure 14.

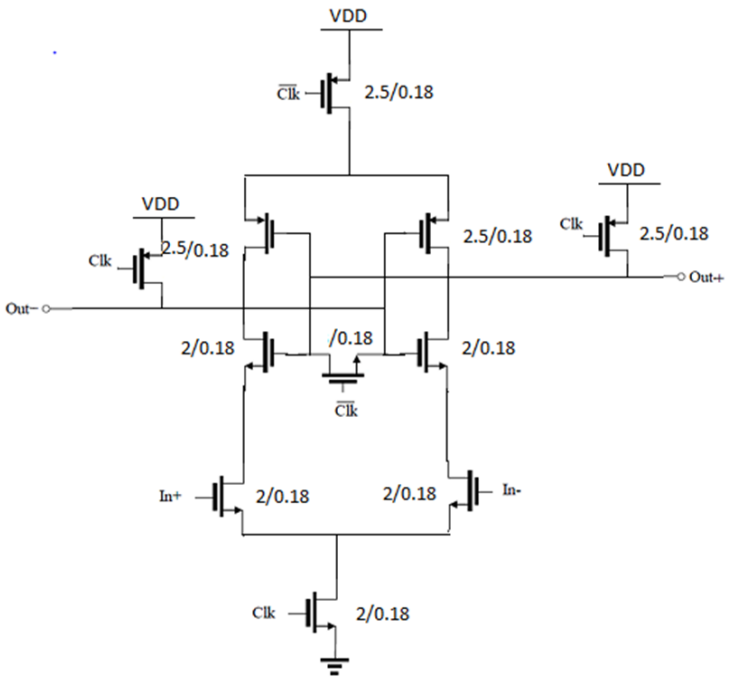


Figure 14. Comparator Schematic

The benefit of this design is that in the reset phase, when the clock signal is low, voltage supply and ground are disconnected from the latch. Therefore, no power consumption occurs in this phase. Since digital circuits normally only accept supply voltage and ground voltage as “1”s and “0”s, a PMOS pair was added to pull the output to supply voltage. During the evaluation phase, when the clock signal is high, the comparator is powered and starts to compare the input signals at the “In+” and “In-” terminals. The latch circuit grows the input difference and finally reflects either “1” or “0” at the output terminal.

The functionality of the comparator is confirmed with Figure 15. The first plot is the input signal, the second one is the clock signal and the third one is the output signal. The test signal was a sinusoidal wave with 1mV amplitude at 800mV DC level. The reference voltage used to discriminate the “0” and “1” was 800mV. From the output signal plot, it is shown that when the clock is on, if the input signal is above 800mV, the output is “1”; vice versa.

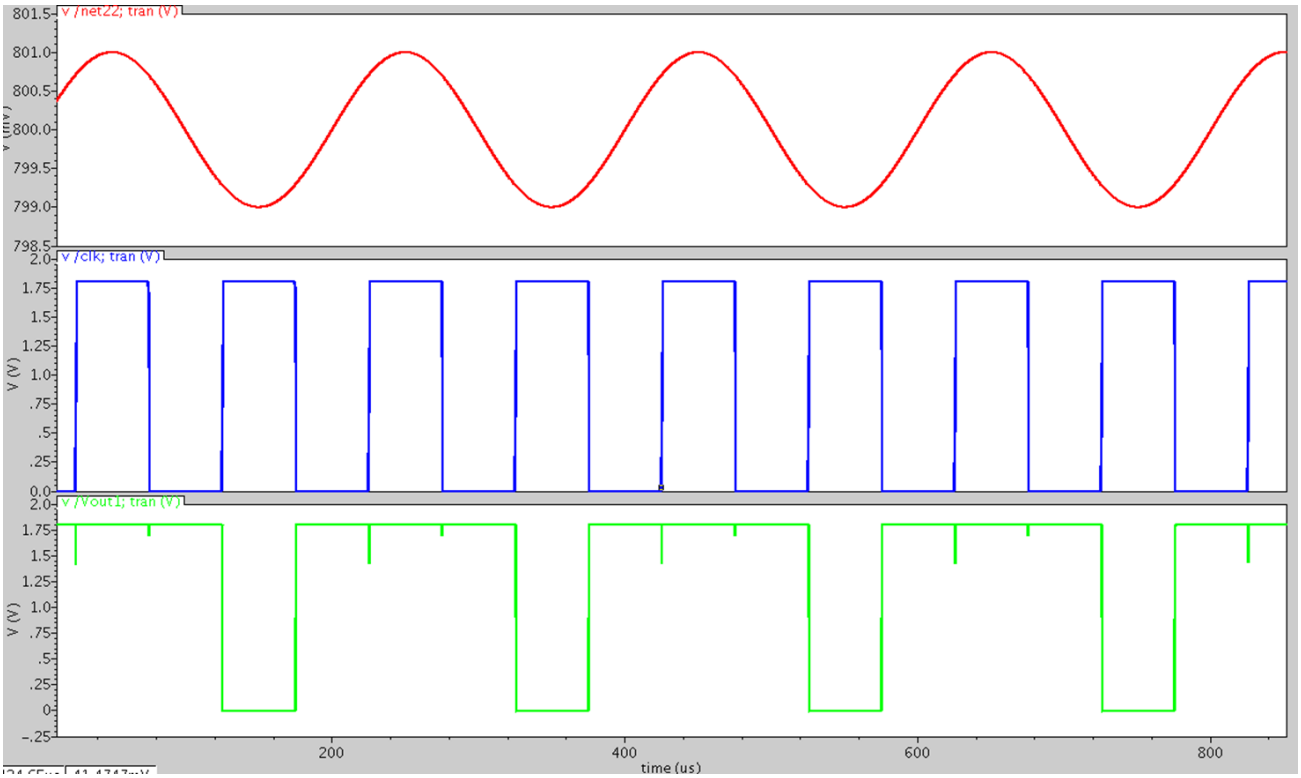


Figure 15. Comparator Functionality

This comparator circuit consumes 237nW of power, which fits our team’s purpose of building an ultra-low power transceiver.

Complete Receiver Chain

The schematic for the complete receiver chain, which consists of the oscillator, the envelope detector, and the comparator, is shown in Figure 16.

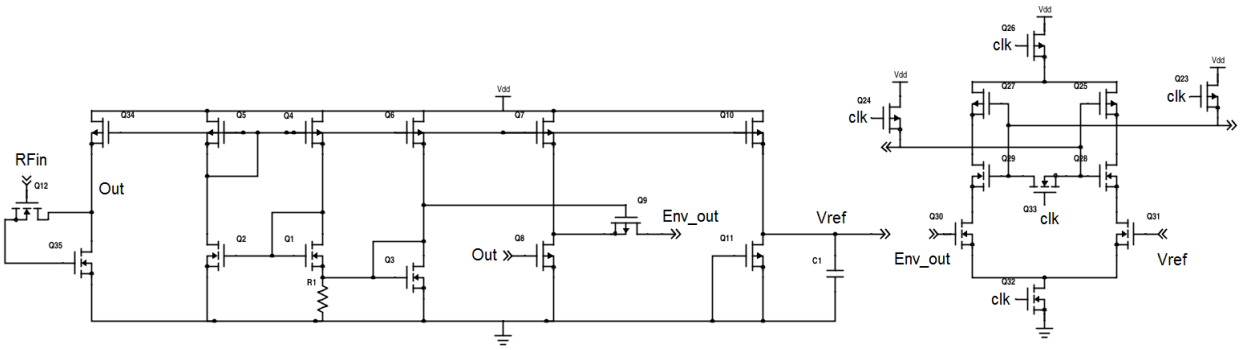


Figure 16. Receiver Chain

The capstone team verified the functionality of the receiver chain by inputting a test 1010 signal that is generated by the oscillator. The results of the simulation are shown in Figure 17. As shown, the green signal is the generated 1010 signal from the oscillator. The purple square wave is the output of the envelope detector and as expected, it is the negative envelope of the input oscillator signal. The dc purple signal represents the reference voltage that the comparator uses to determine the received bits. For envelope amplitudes below the reference level, the comparator will clock a 1 and for envelope amplitudes above the reference level, the comparator will clock a 0. The red signal represents the clock signal. The blue signal represents the output of the comparator. An output synchronous flip flop that is edge triggered by the clock shown will latch a 1010, as expected.

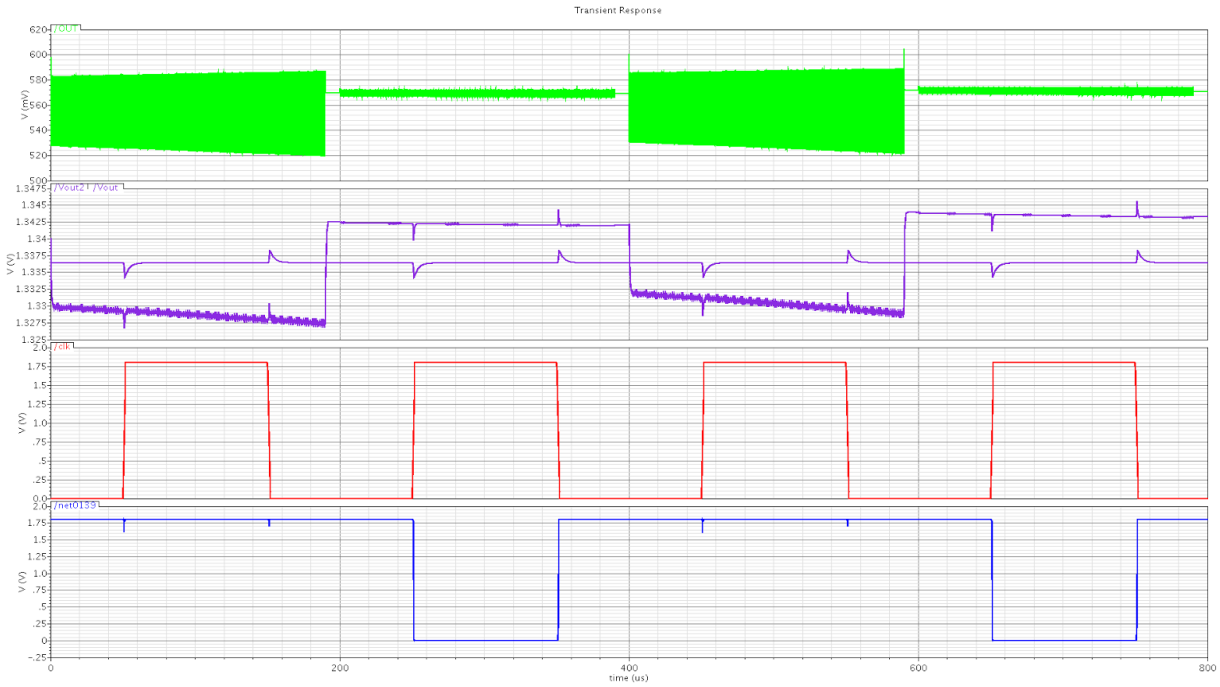


Figure 17. Verification of Receiver

Power Amplifier

This part of the paper summarizes the design of a Power amplifier (PA) for the transmitter part of the system. This block functions to establish connections and send information from the digital system to the external world.

Given the fact that reducing the power consumption is the overall goal of this project, the power consumed by the individual blocks must also be minimized. This translates to the concept of power efficiency, meaning ‘the amount of power used to generate and transmit a decodable burst of data from the system’. The major trade off for efficiency is a characteristic called linearity. Linearity defines ‘the relationship between the output and the input, and the change in output for

a given change in the input level'. Below is a table of the performance statistics of each of the power amplifier classes available.

CLASS	A	B	C	D	E
Theoretical efficiency	50%	78.5%	80%	100%	100%
Linearity	Linear	Non-linear	Non-linear	Non-linear	Non-linear

Since efficiency is our major consideration in this system, a class D amplifier was used. This choice was made after surveying highly efficient PA's in papers written in [8] and [9]. The other requirements needed for proper operation of the PA block include current bias generation, voltage bias at the input, and inclusion of passives.

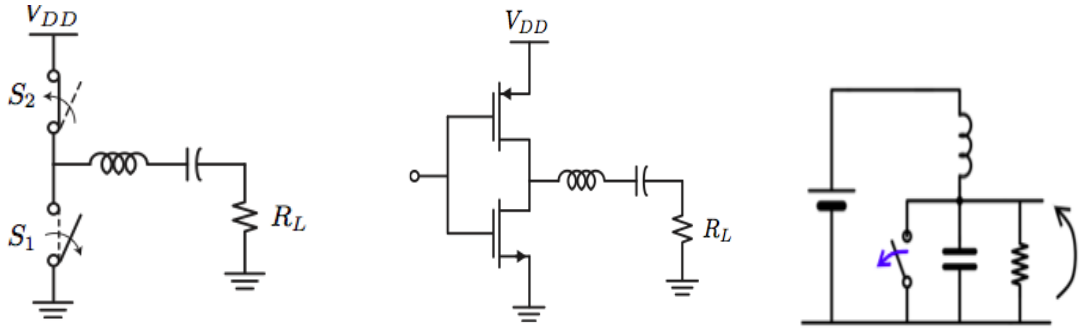


Figure 18. Class D & E Amplifier models [10]

From the above table, class D and class E amplifiers can be theoretically characterized as having an efficiency of 100% [10], this is because they don't allow for any dissipation of energy

within the system, thus translating all of its energy to the required output load, which is an antenna used for transmission in most cases.

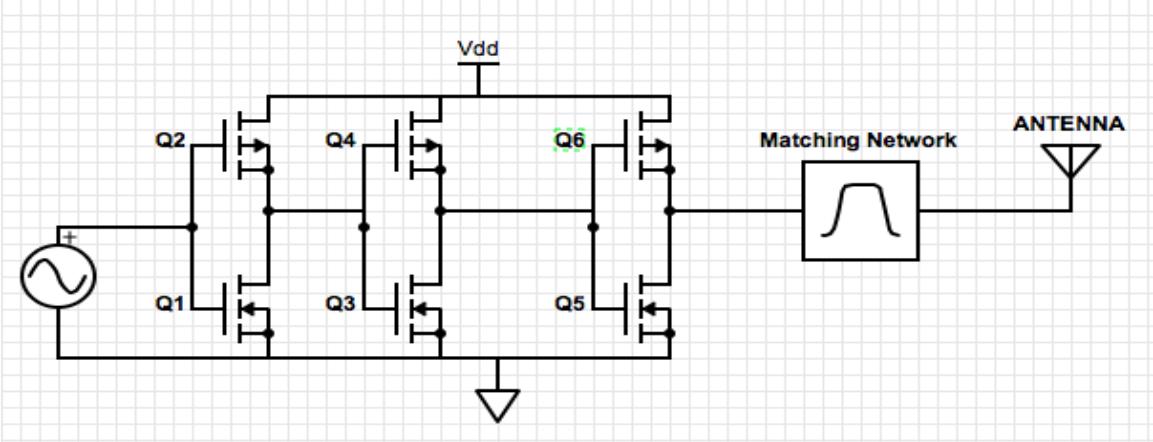


Figure 19. Architecture of the Power Amplifier

The control over power transmitted to the load depends on the impedance (resistance) of the load seen by the output node of the amplifier. In order to meet the specification of the power drawn by the load precisely, this load seen by the output node has to be transformed to a different value. This process of transforming the load can be done by using a network called 'matching network' to match the output node to the impedance needed for maximum power transfer. For this power amplifier, a T-match was employed because it isolates the DC component and the AC component – which is of our interest at the output node and also provides the impedance transformation needed. The final schematic of the power amplifier is shown in Figure 20.

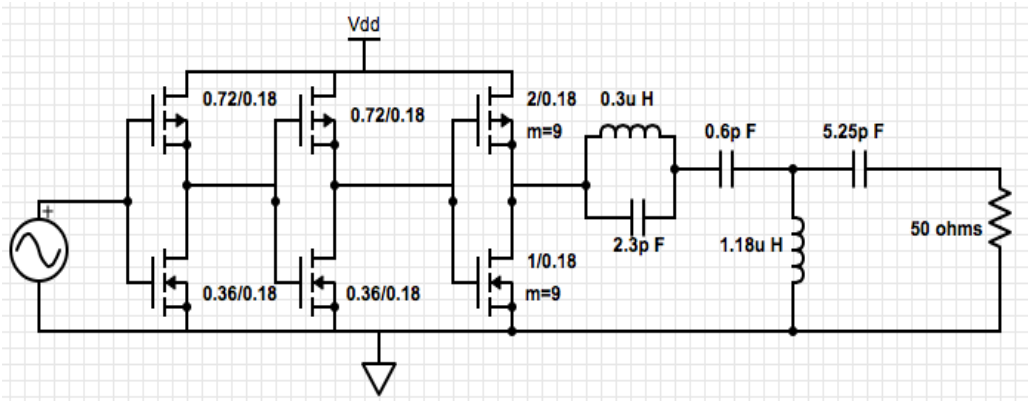


Figure 20. Power Amplifier Schematic

The layout of the power amplifier is shown in Figure 21.

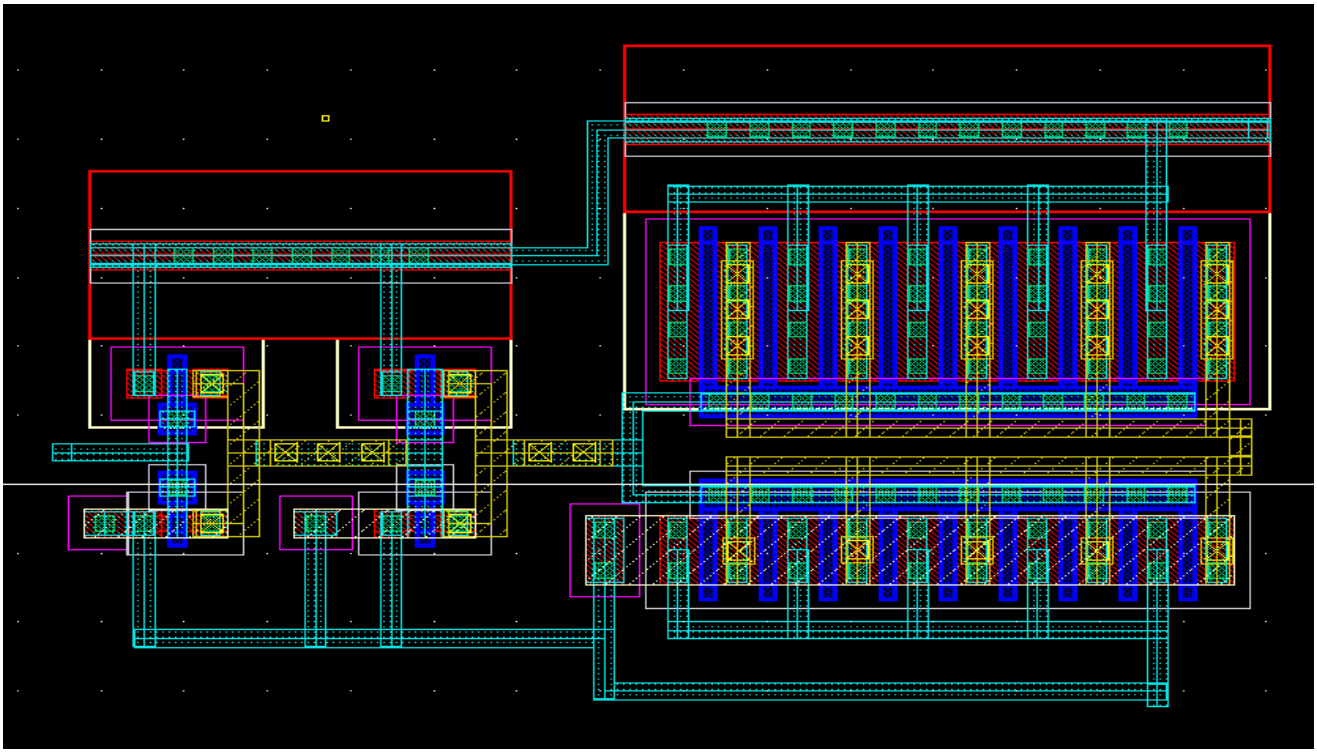


Figure 21. Power Amplifier Layout

Following waveforms show the simulated results for the various performance metrics.

POWER-GAIN & OUTPUT WAVEFORMS: The reported power gain is 47 dB at the fundamental frequency. Waveforms below depict the voltage and current waveforms at the port or the virtual antenna. We can see that the waveforms are purely sinusoidal.

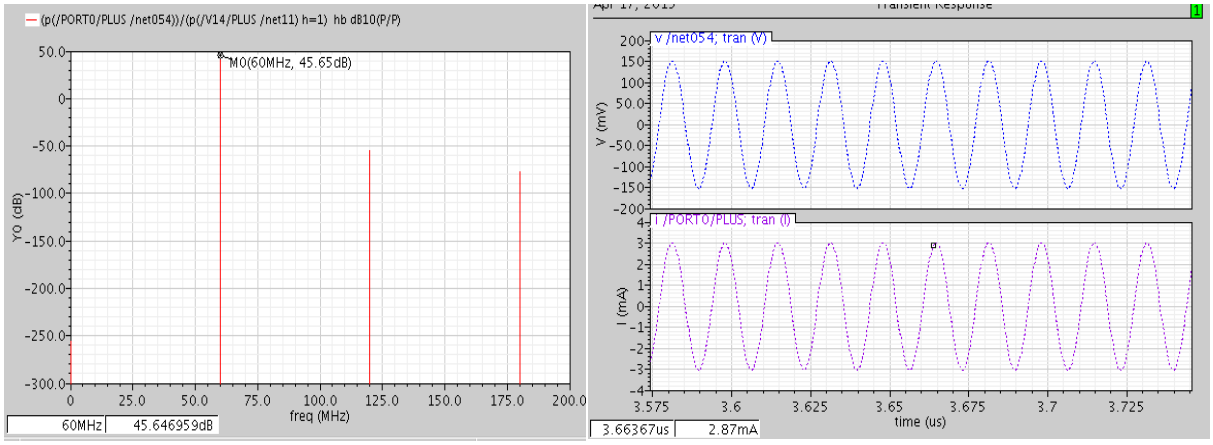


Figure 22: measured power gain & simulated output waveforms

POWER: The first plot shows the power levels without the L–match filtering at the port. The second plot shows the power levels with both the L-match filtering at the port and 3rd harmonic filtering. We see that harmonic power is high and can affect the efficiency.

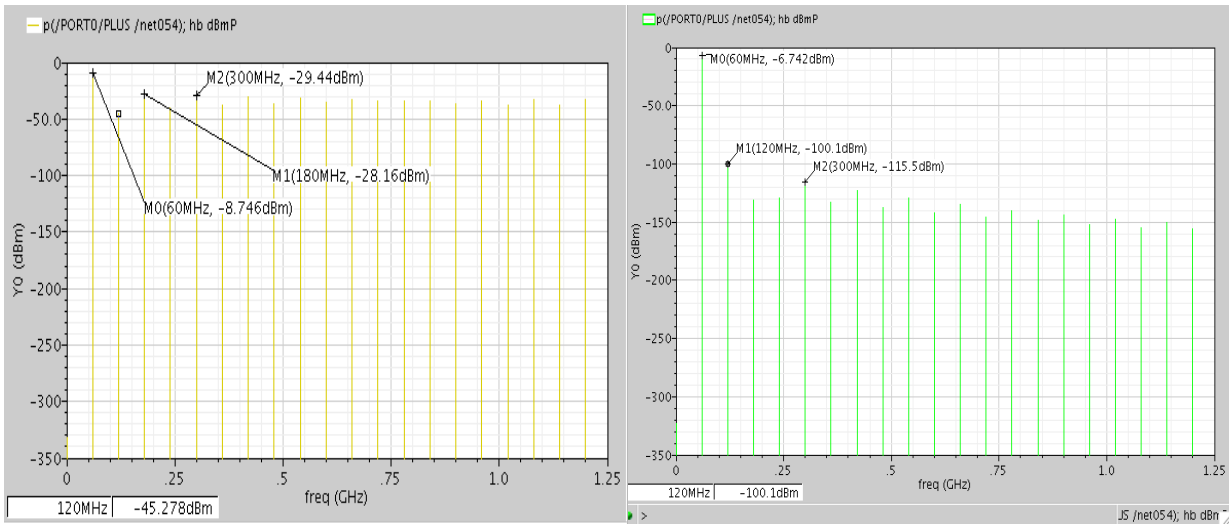


Figure 23: Power without the L- match filtering

Match type	L(uH)	C1(pF)	C2 (pF)	C-Block	Max eff	Power (dBm)	Drawback
pi	0.184	41.5	371	1.2pF	89%	-3.5	Needs dc-block
T+3wo filter	1.18	0.587	5.25	-	86.5%	-7	No dc block needed
Pi+T filtering	1.18	0.587	5.25		89%	-7.2	Needs 3 inductors

Figure 24: Impedance calculated for different matches

EFFICIENCY: The reported efficiency is 88.35%.

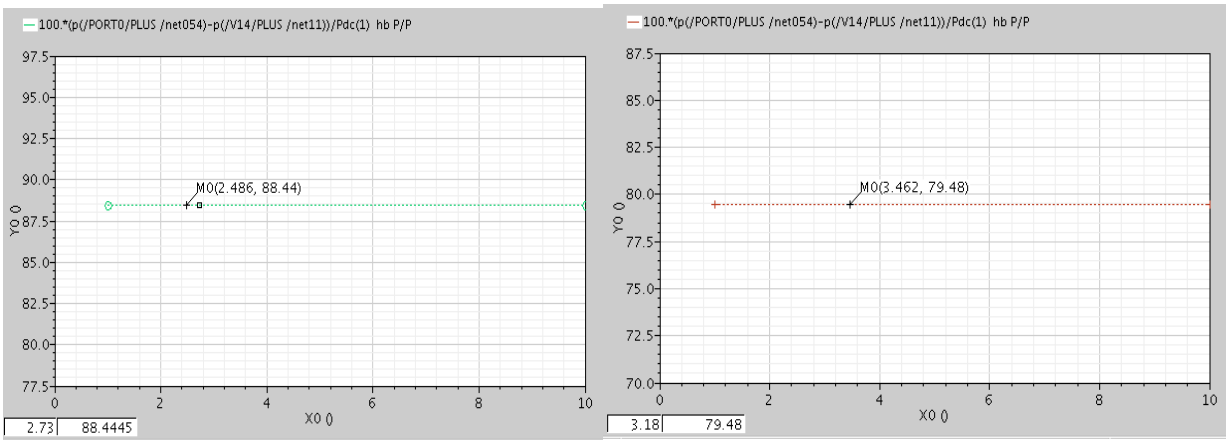


Figure 25: Measured efficiency with filtering & before harmonic "block network"

It is evident that the efficiency improves by 16%, by adding a third harmonic block.

DRAIN WAVEFORMS:

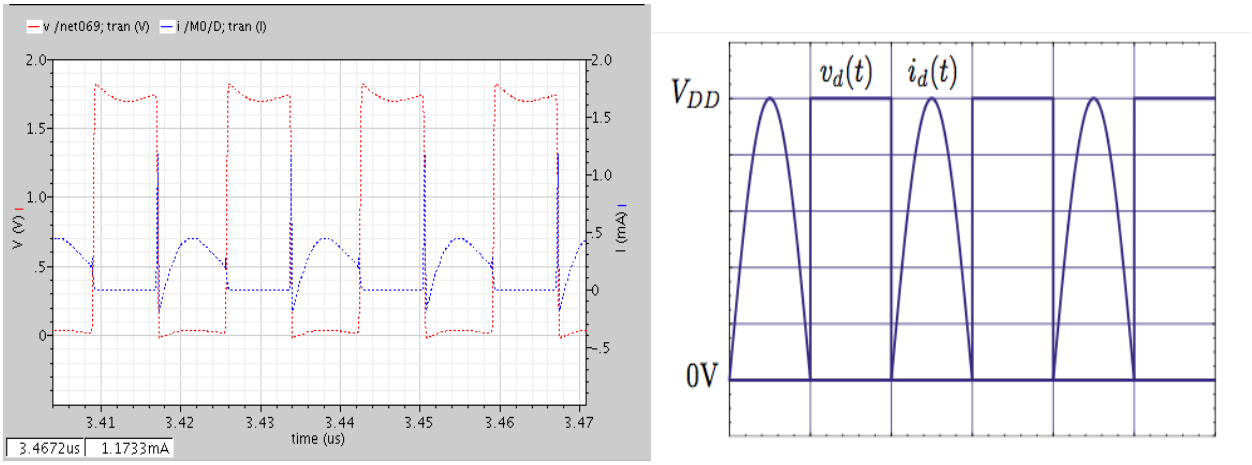


Figure 26: Drain waveforms Ideal class D output waveforms

The contributors for efficiency degradation are:

1. Harmonic dissipation: we see that the total harmonic power added from the second to 19th harmonic sums up to 1.2% after adding the 3rd harmonic filter.

2. Parasitic losses: The passive devices have a quality factor of 20.Therefore, the internal resistance of the components adds up to a loss of 2.4%.

3. C*V^2*f Losses: The input gate capacitance of the inverters is 1.5f F each and the amplification stage offers a gate cap of 31f F. This produces a loss of 6.722uW = 3.4 %

	Short circuit current	Harmonics	Passive parasitics	Driver C*V^2*f	Total loss
loss	6.4%	1.2%	2.4%	3.4%	13.4%

Figure 27: Loss contributors

Transmit Chain

The oscillator is integrated with the Power amplifier by connecting the output of the oscillator to the input of the PA. An input FSK is generated by the oscillator and given to the PA.

The plot below in Figure 28 shows how an input data stream is modulated and transmitted by the power amplifier into the antenna.

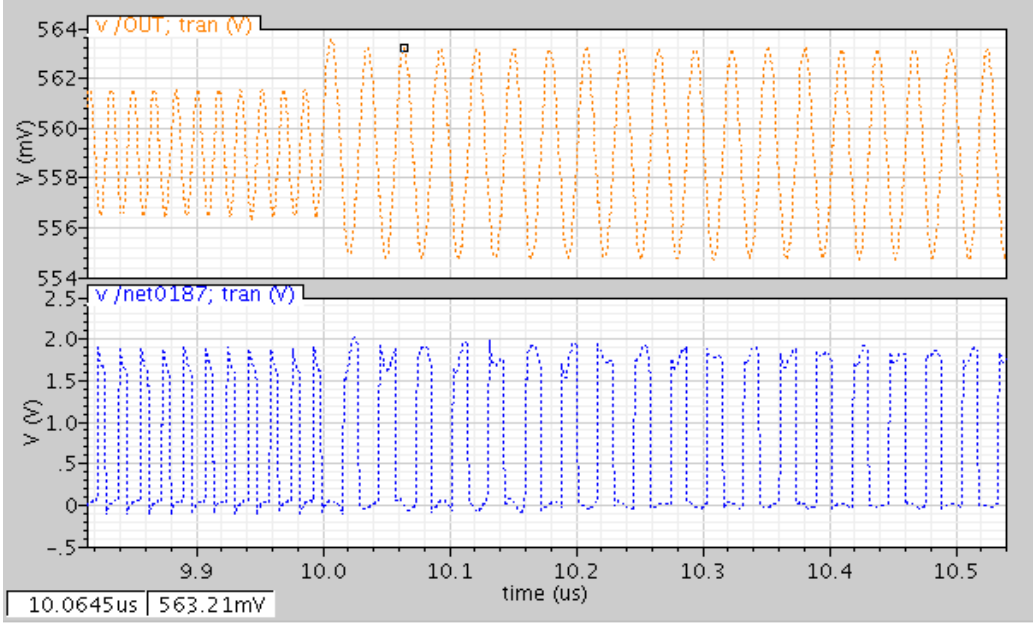


Figure 28. Transmit Waveform

Voltage Buffer

We require a voltage buffer to interface with the 50Ω transmission line required to test our chip. This voltage buffer has several design requirements. The most important is a voltage gain of 1 to accurately represent the input signal. Impedance matching at the output is necessary to ensure that the maximum available power from the input signal is delivered to the load. The buffer also requires high enough bandwidth, output voltage swing, and linearity to send signals to the output negligible distortion. The input signals of interest are the output signals of each block in the transceiver chain except the power amplifier; in general, these are a 60Mhz signal with 0.8V peak to peak (pk-pk) and a 5khz signal with 1.8Vpk-pk. A bandwidth requirement of 600Mhz is necessary to capture harmonics of the 60Mhz signal. Die area and power consumption will not be considered as primary design constraints. Since our project is currently focused on verifying functionality, cost and commercialization details are not concerns. Additionally, the buffer will

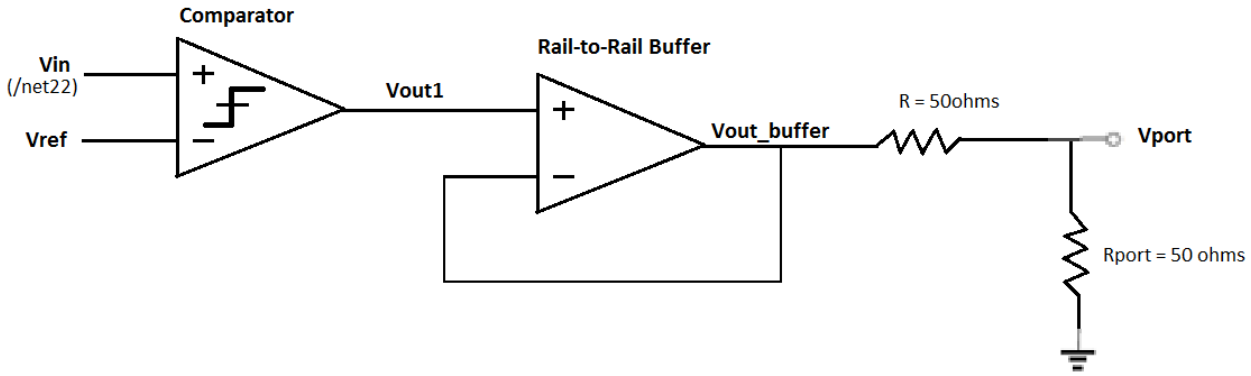
connect a separate power rail from the rest of the transceiver to negate its power contribution during normal operation of the MEMS transceiver.

Given the design requirements presented, two different buffer topologies were implemented. A wideband buffer was designed for 60MHz while a rail-to-rail buffer was designed for 5 kHz. For the purposes of this paper, which is to discuss the integration of the voltage buffer into the transceiver system, we encourage the reader to briefly refer to the summary of the performance of both buffers as given in the "Individual Technical Contributions" report for the voltage buffer. Details on the topologies, transistor sizes, design methodology, and test results of the buffers is discussed in more detail in that report.

The integration of the voltage buffer to the transceiver system required proper modeling of the interface between the buffer and the block being measured. The additional capacitance that would be added after attaching the buffer must be taken into consideration during design time for the measured block. The input PMOS device of the wideband buffers were sized to be 20um/180nm, which resulted in an input loading of ~10fF. Since the functionality of both the envelope detector and the oscillator already required large capacitances on the order of ~100fF at their outputs, this additional loading was not a concern. The integration of the comparator with the rail-to-rail buffer was more challenging; the input of this buffer had a PMOS device with size 36u/180nm in parallel with a NMOS device with size 12u/180nm, which summed to a significant capacitance. A redesign of the transistor sizes in the comparator was necessary. Figure 29 shows the schematic and resulting plots of a rail-to-rail buffer integrated with the redesigned comparator. As shown in part (b) of the figure, the output of the buffer follows the comparator's output up to its maximum voltage swing of 1.67V, which is the expected performance.

A different issue that needed to be resolved for the wideband buffers was being able to take in the input signal and display it accurately at the output. The ability for the buffer to do depended on its maximum input common mode range and the voltage range of the signal being monitored. Refer back to Figure 17 in the "Complete Receiver Chain" section for the the output signal of the oscillator and the envelope detector. The wideband buffer with a PMOS input pair can accept voltages between 200mV and 1V. This was acceptable for the oscillator, which after integration yielded a signal centered around 600mV and stayed within this range. However, another wideband buffer with an NMOS input pair needed to be implemented to monitor the output of the envelope detector. The new buffer with a common mode input range between 600mV and 1.4V can accept the signal at the envelope detector's output, which is centered around 1.2V. The resolution of the two issues described above allowed us to successfully integrate the voltage buffers with the blocks we are interested in measuring: the oscillator, the envelope detector, and the comparator.

(a)



(b)

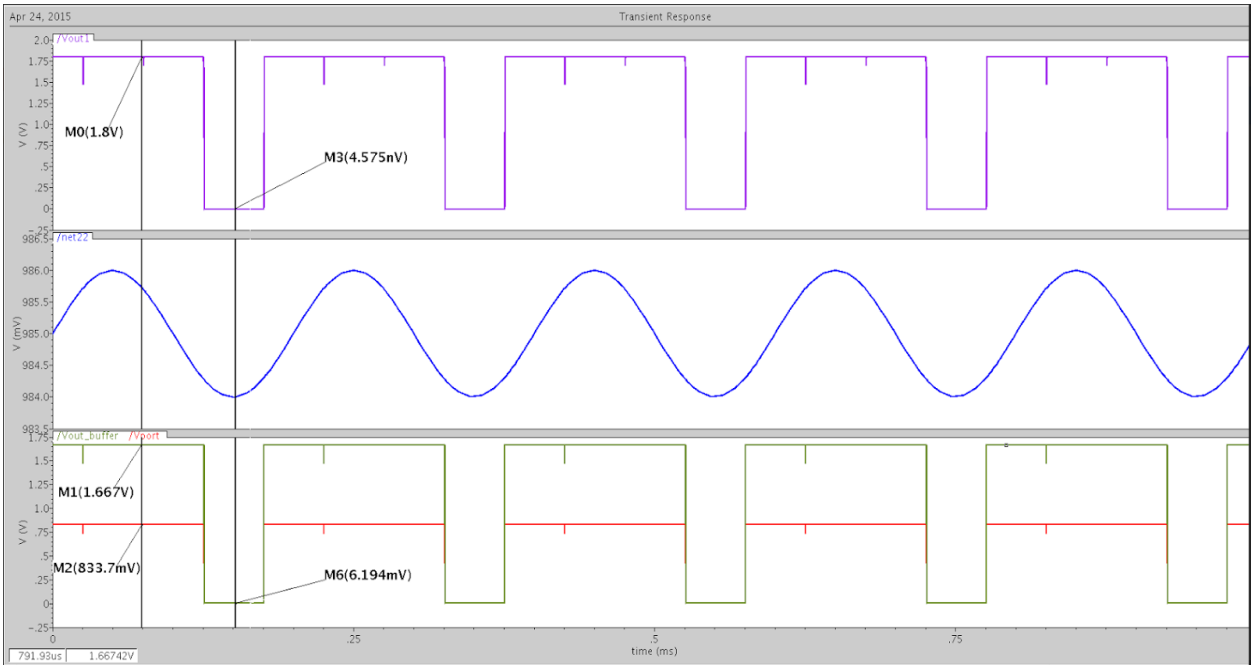


Figure 29: Test Setup (part a) and Transient Response (part b) for comparator and rail-to-rail buffer. Blue trace is the test signal (output of envelope detector), purple trace shows output of the comparator, green trace shows the output of the voltage buffer, and red signal shows the signal being sent to the load after matching.

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V. Concluding Reflections

In this part of the report, I will include some reflections on the entire progress of the report. I will focus on differences between planned and actual project achievements, teamwork and personal lessons. At the end of this section, I will comment on possible future work of both this project and the entire Capstone program.

At the beginning of the project, the initial goal is to not only complete the schematic design, but also implement layout for the entire system and tape out. There are multiple reasons we fail to achieve the goal, but I think the most important one is the gap between our team's expectations and our mentors'. Initially, most team members had no extensive design experience, nor did we possess certain necessary integrated circuit design knowledge. We generally had no idea about the difficulty. On the other hand, as far more experienced designers, our mentors sometimes assumed we know the information and expected us to solve design problems we met in the process. The reluctance that we had to consume considerable time on background knowledge caused large delay in project progress. The other reason is that we were constantly attempting to optimize our circuit schematic in order to achieve better energy performance. At the first day, we were told to target the power consumption of the entire system to be 5 microwatt. Yet, the fact is that this level of power consumption is impossible according to the basic settings. We only realized it until very late but lots of time has been wasted.

Teamwork is another important issue. It was hard to schedule a meeting on weekends, as two of our team members often refused to accommodate the needs of the team. I do believe we can achieve better teamwork if we can think more for each other.

Yet, I still learn a lot from this project. I know more about circuit design as well as project management. Also, the tough process provides me remarkable experience on how to start and deal

with projects which I do not have enough knowledge and information. I think I will be much more prepared if I face this kind of scenario again in my future career life.

The natural future work of this project would be layout and verification. Since the design part has been done, this part of work should be comparatively easy. I also would like to give some suggestion to the Capstone program. I think that all mentors should be more informed that they are working with new graduate students, not Ph.D. students. Both teams and mentors need to learn how to work with other well in order to obtain better project experience. Finally, sincere thanks to MEng program of UC Berkeley!