9.7-ENOB SAR ADC for Compressed Sensing

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Brian Wang

This **Masters Project Paper** fulfills the Master of Engineering degree requirement.

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Abstract

Moore's law has allowed the microprocessor market to innovate at an astonishing rate. We believe microchip implants are the next frontier for the integrated circuit industry. Current health monitoring technologies are large, expensive, and consume significant power. By miniaturizing and reducing power, monitoring equipment can be implanted into the body and allow 24/7 health monitoring. We plan to implement a new transmitter topology, compressed sensing, which can be used for wireless communications with microchip implants. This paper focuses on the ADC used in the compressed sensing signal chain. Using the Cadence suite of tools and a 32/28nm process, we produced simulations of our compressed sensing Analog to Digital Converter to feed into a Digital Compression circuit. Our results indicate that a 12-bit, 20Ksample, 9.8nW Successive Approximation ADC is possible for diagnostic resolution (10 bits). By incorporating a hybrid-C2C DAC with differential floating voltage shields, it is possible to obtain 9.7 ENOB. Thus, we recommend this ADC for use in compressed sensing for biomedical purposes. Not only will it be useful in digital compressed sensing, but this can also be repurposed for use in analog compressed sensing.

Introduction

Thanks in great part to Moore's law, the energy cost of digital logic is constantly decreasing, and is allowing for ever more computing with miniscule amounts of power. One exciting new application of computing is in wireless body-area networks, where a collection bio-sensors communicate wirelessly with a base-station such as a smartphone [1]. The smartphone would then transmit data to a physician to allow live monitoring, or be able to contact emergency services in life-threatening situations.

Traditional transmitter topologies take an analog signal, sample it at the Nyquist rate, process it in a DSP, and then transmit it through a radio. These segments take 2%, 25%, and 73% of total power respectively [2]. However, many biological signals are sparse (or compressible) in some domain (i.e. time, frequency), and traditional transmitter topologies fail to take advantage of this.

Compressed sensing aims to compress these sparse bio-signals and reduce the amount of data processed through a DSP and RF front-end, thereby reducing power. Typical compressed sensing can compress by a factor of anywhere from 2 to 16 [3], which translates to a 2x to 12.3x longer battery life, which is important when replacing a sensor may mean surgery.

There exist two types of compressed sensing – analog and digital [3]. Analog compressed sensing uses a compression analog front-end before the ADC so that a slower sub-sampling ADC can be used. Techniques used in analog compression include a MDAC integrator that multiplies the input with a random coefficient, and linear feedback shift-registers utilizing either Fibonacci or Galois hybrid algorithms to generate a sufficiently randomized coefficient matrix. Digital compressed sensing uses a digital multiplication and accumulation after the

Nyquist-rate ADC. While a digital compressed-sensing circuit loses in terms of power from a faster ADC, it also reduces noise by utilizing spike-detection.

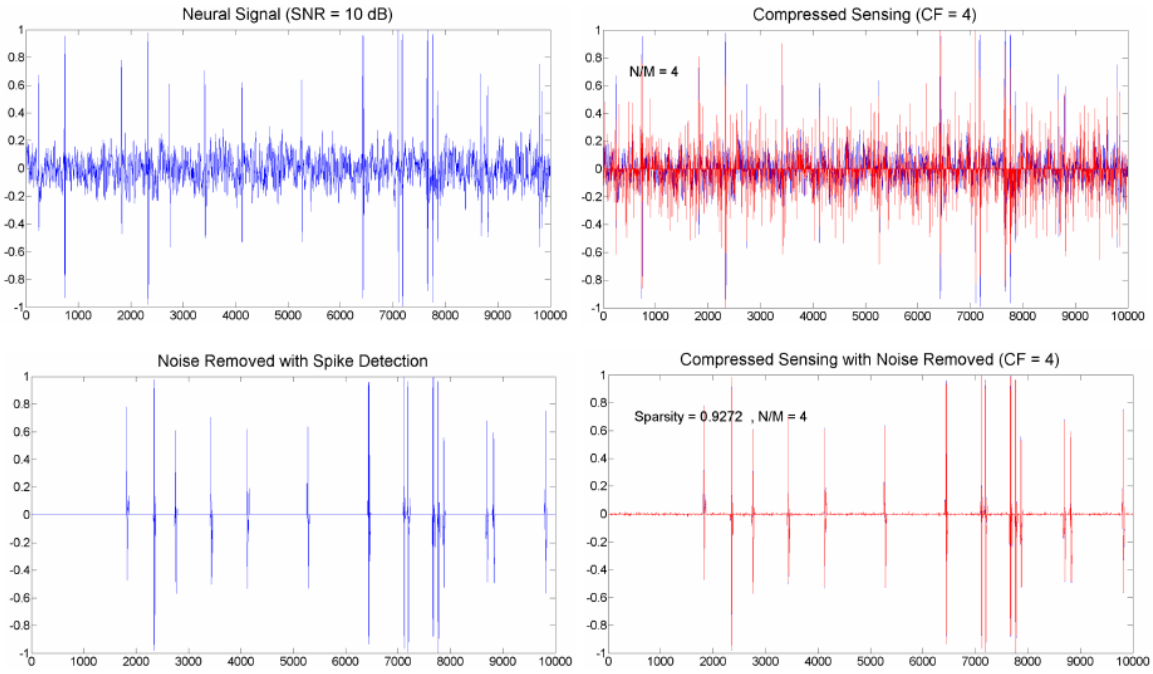

Figure 1 - Compressed Sensing on Neural Signal without (top) and with (bottom) spike detection

All of this requires an ADC, which is the focus of this paper. Brain signals are the focus of this specific application, and the frequency ranges of brain signals range from 0.5Hz up to 150Hz [4]. The signal used for analysis of the digital compressed-sensing circuit is at 20Ksample/s, which defines the operating speed of our ADC. Diagnostic quality is also defined to be 10 ENOB. Thus, we designed a 12-bit 20Ksample/s ADC.

This ADC can also serve as a drop-in replacement in [3] to replace the single-ended 6.5 ENOB SAR ADC to improve the performance of the analog compressed-sensing front-end described in the paper – to that effect, this ADC will be differential to complement the signal chain, and because the sampling-rate only needs to be 2Ksample/s, the transistor widths can be downsized to reduce power.

Literature Review

Among ADCs, SAR ADCs are known to be particularly power efficient due to the low number of analog components required [5][6]. In fact, the only analog component required is the comparator. The low number of analog components means that there is less of a need for transistor biasing that draws unnecessary power. One drawback of the SAR architecture is that it is unsuited for high-speed operation – however, biomedical signals are at a low enough frequency where that is not an issue.

Many SAR ADCs utilize a binary-weighted DAC to compare the digital output to the analog input [7][8]. However, these binary-weighted DACs can quickly grow to be very large for a modest number of bits and consume too much power. To borrow computer-science terminology, capacitance and power grows as a factor $O(2^n)$. While it is possible to scale down the size of the entire DAC, capacitor noise sets the lower-limit.

$$Vnoise = \sqrt{\frac{kT}{C}}$$

Equation 1 – Capacitor Noise equation

There are hybrid implementations that combine a C2C array and a resistor ladder[8]. However, these hybrid combinations do not work well due to the series resistance of the switches between the resistor strings.

Another way of implementing the DAC is called a C2C array [3]. Each successive bit is connected in series at the end of the C2C ladder, and has a proportionally smaller effect on the output. Thus, the capacitance and power scales proportionally with the number of bits – O(n). However, the C2C arrays have issues with linearity, and most C2C arrays have been unable to

attain more than 6-ENOB. One reason for the nonlinearity may stem from the parasitic capacitance of the capacitor array coupling the bottom plates of the capacitors in the capacitor array to ground. Thus, a floating voltage shield [9] which reduces the voltage across the parasitic capacitance can be useful.

Implementing a differential SAR can also be difficult. While a single-ended ADC is straightforward and easy to implement, there are several ways to implement a differential SAR. Differential circuits allow for common mode rejection and commonly improves signal to noise ratio. There are also methods to integrate a sample/hold block into the capacitor DAC itself [10]. Finally, it is possible to reduce the number of times a capacitor is switched between voltage states to reduce power by using a switching algorithm that only switches once per conversion-step [9].

A SAR architecture requires a high-gain comparator. For 12 bit accuracy, a gain of 4000 is required. A comparator differs from an opamp or OTA in that it does not need to be stable in feedback. As such, there are comparators that are made up of a series of cascaded OTAs. However, the most popular comparators are ones based on positive-feedback latches[11]. These comparators do not consume constant bias current and converge to an output faster than cascaded OTAs. Thus, we decided upon the conventional [12] StrongARM style latch as our comparator. A bonus effect of using the StrongARM latch is that it has no flicker noise because there is no bias current flowing through it.

The SAR control logic is well documented in literature, and is based on the standard sequencer and code register design. Among three different types of SAR control logic studied in [13], the following utilized the least amount of power.

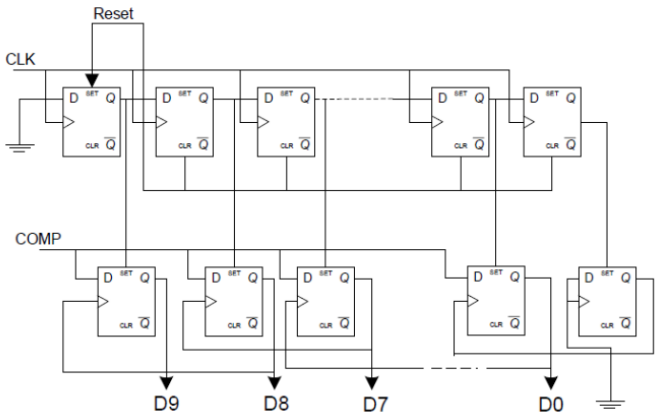

Figure 2 SAR logic block diagram [13]

Finally, because a SAR architecture requires switching of capacitor arrays, we needed to look at switch design. The simplest switch is an NMOS or PMOS connected to ground or VDD, respectively. However, because single mosfets introduce charge into the circuit when they switch, they are not suitable for switching analog signals . One method for preventing that is by using a dummy switch that is shorted across the drain and gate to absorb the rogue charge introduced by a mosfet turning off[14]. By turning on the dummy switch, the charge gets absorbed into the channel and overlap capacitance of the dummy switch. Another method is to use transmission gates. When the gate of the NMOS in a transmission gate goes high, the gate of the PMOS goes low, which is not unlike the configuration of a dummy switch. Provided the transistors are sized similarly, we can ensure that injected charge is close to zero.

Methods and Materials

Our simulations are based on a 32/28nm process library used in the UC Berkeley graduate-level courses. This simulation technology node is based off of industry models.

The industry models are derived from years and millions of dollars of research, companies have an interest in keeping their technology secret. Thus, in order to use those industry models, researchers have to sign NDAs, and the legal issues are not feasible for multiple classes of 40+ students that changes every semester. Thus, this 32/28nm process library was created by UC Berkeley researchers to facilitate teaching current transistor technology without requiring NDAs and avoids legal issues.

One issue with the 32/28nm library used at UC Berkeley is the lack of 32/28nm specific capacitors. While an industry model would have capacitor geometries and layouts, they were not implemented in the UC Berkeley, and thus we were unable to do a layout and extract capacitor parasitics. However, research on recent technology nodes indicate that parasitic bottom-plate capacitance is usually on the order of 1-8% [15] - thus, I modeled excess capacitance as a conservative estimate of 10%, and connected a 10% unit-capacitance sized capacitor between internal nodes and ground (or the FVS node).

One issue that kept recurring was GMIN. GMIN is the default admittance added to internal nodes of a non-converging simulation to make it converge. However with our small capacitor sizes, the default GMIN of 1pS was causing unacceptable droop in our C2C DAC. To remedy the situation, we first tried setting GMIN to be 1zS. However, that did not stop the droop, so in the end, I decided to connect 100ExaOhm resistors between all of our nodes and ground.

Another recurring issue is the strange glitches during simulation. During some simulations, the conversion would simply terminate and all of the previously set bits would switch states. The bit at which this occurred was random, as were the simulation voltages that caused it. During the glitches, the simulation logs would indicate non-convergence errors and would successively try more conservative convergence algorithms (TRAP, GEAR, etc). This was eventually solved by hard-setting the minimum simulation step size instead of letting the simulator choose the minimum simulation step. We theorize that this occurs because the auto-selected minimum step size was simply $1/1000^{th}$ of the simulation length. Our 32/28nm gates had transients well below the millisecond timescale, even when driving large femtofarad capacitances. When we chose long simulations, the minimum step size was simply too large for the Newton Raphson algorithm to converge within an acceptable error tolerance, causing convergence issues. However, we postulate that sometimes the transient would jump to an incorrect state that the simulator would interpret as being within the error bounds, and the simulation would be incorrect from that point onward.

The comparator was also designed in the 32/28nm process. The comparator was first sized to minimum transistor dimensions to obtain a working prototype. Then, transistor length was swept across a range to make switching power equivalent to static leakage power at 20kHz, the operating frequency. Width was kept at minimum to both reduce capacitance and reduce leakage. On the same token the PMOS/NMOS ratio was kept at 1. This does not affect offset because both of the cross-coupled inverters are similarly sized.

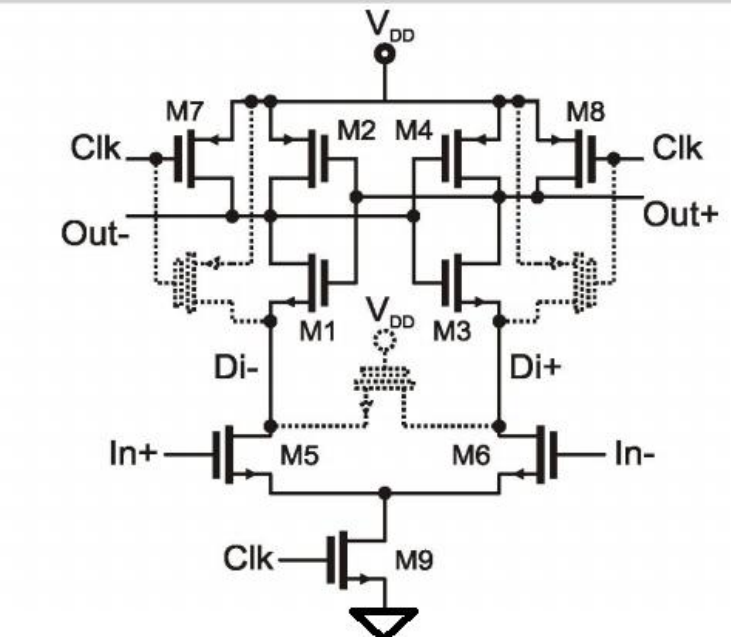

Figure 3 Standard latch comparator [12]

We opted to keep all of the clock switches that reset all of the latch nodes. This was to reduce the effect that previous comparator evaluations had on the next evaluation. We also opted to use a PMOS based differential pair – this way our clock resets would run off of NMOS and discharge the internal latch nodes better.

We also buffered the output of the comparators with inverters. This was because our digital SAR logic was single-ended, and uneven loading can cause the comparator to have an offset [18]. This can be easily seen when the clock goes from high to low – at that point, the output nodes slowly drop down from VDD with RC time-constant equivalent to the on-resistance of the inverter and the capacitance of the load+gate capacitance of the cross coupled inverter. When one side has more capacitance than the other, the RC constant will differ, and they will discharge at different rates and create a natural offset. The added benefit of an inverter output buffer is that the comparator no longer has to drive all of the SAR logic capacitance, and we are

able to use optimize the digital fanout ratio with an inverter chain. Thus, we added another 4x-sized inverter at the end to increase our comparator drive capability.

The SAR logic was first implemented in verilog functional blocks to test functionality. A bug was discovered where the last bit would not toggle, so the sequencer was extended by an extra set of flip-flops, so that the last non-toggling bit went nowhere, and we had enough bits to control our DAC. Then, the verilog flip-flops were replaced with transmission-gate based flip-flops. Kevin optimized the digital logic-gate transistor lengths to reduce static leakage power.

Our first SAR was a single-ended SAR with a binary DAC. We implemented this because it was easier to debug our control logic and probe our DAC's internal voltages. I chose to start out with a binary DAC and work slowly towards a hybrid-binary-C2C DAC with floating-voltage shield, so that if anything went wrong along the way, we would know which step caused the error. We did not measure linearity, but simply tested a few input voltages (Vin = 0, which was either 100000000000 or 0111111111111, and Vin = +/- VDD/6 which outputs 010101010101 and 101010101010 respectively) and compared the digital output to our analog input. Afterwards, I implemented a C2C DAC with no parasitic capacitance in order to have a working concept. After using it to replace the binary DAC, we again simulated and confirmed it worked. Then I implemented a C2C DAC with parasitic capacitance, and confirmed that our outputs were no longer what they were before we implemented parasitic capacitances. Then I implemented a C2C DAC with parasitic capacitance that couples to a floating voltage shield, and we simulated and confirmed that linearity was improved. Finally, I implemented a range of hybrid-binary-C2C DACs, and simulated each one to confirm linearity.

At this point, the SAR ADC was still single ended. To make the ADC differential, I implemented a MUX that samples the top-plates to the input pins and the bottom plates to the common-mode voltage during the RESET phase, and outside of RESET, disconnects the common-mode voltage and connects the positive DAC to VDD and the negative DAC to GND. Then, based on the comparator output, the SAR logic either leaves the specific DAC pins connected as they were right after RESET, or swaps the connections. This way, each conversion step at most switches each capacitor once. Two side benefits of going differential were that the input differential voltage range expanded from [0,VDD] to [–VDD , VDD], and that the DAC now has a sample/hold circuit built in.

DNL and INL were difficult to measure in simulation. DNL and INL are usually measured on an actual fabricated device using a method such as that outlined in IEEE-1057. One method in simulation is to simply sweep the input differential voltage[16] – however each ADC conversion cycle required over a minute of transient simulation and over 1000 points of data to be saved per voltage node. To do a long enough transient simulation would require two days of non-stop simulation, and the resulting output would be over 4-million points per output voltage node. Assuming the simulation did not crash or run out of memory, it would still be a very slow simulation.

The simulation method I used in the end was a piecewise simulation. I ran short transient simulations across voltages I knew to be transition points for certain bits, and measured the DNL and INL there. The sweep range was 6mV (or 12 LSBs) and the sweep time was long enough for 13 conversions. I repeated the process for each bit, duplicated them a corresponding number of times to match the number of times the bit transition happens, and compiled them together in the end. My reasoning was that missing codes from a certain bit transition were likely to

manifest themselves during other transitions. While this may miss certain types of nonlinearities listed in [17] (such as those from the C2C DAC), it was a first order estimate that was reasonable to simulate.

Discussion

First we decided on the unit capacitance of our DAC. Based on the KT/C noise of a capacitor [Equation 1], and with ½ LSB = 2VDD/(2^13) = 256uV, we calculated that the minimum C was 10fF.

Then we tested the validity of the floating voltage shield. Without the floating voltage shield, it was difficult to even get the 2nd bit. The following is a the analog voltage output of a FVS C2C DAC and a non-FVS C2C DAC hooked up to the same SAR logic control.

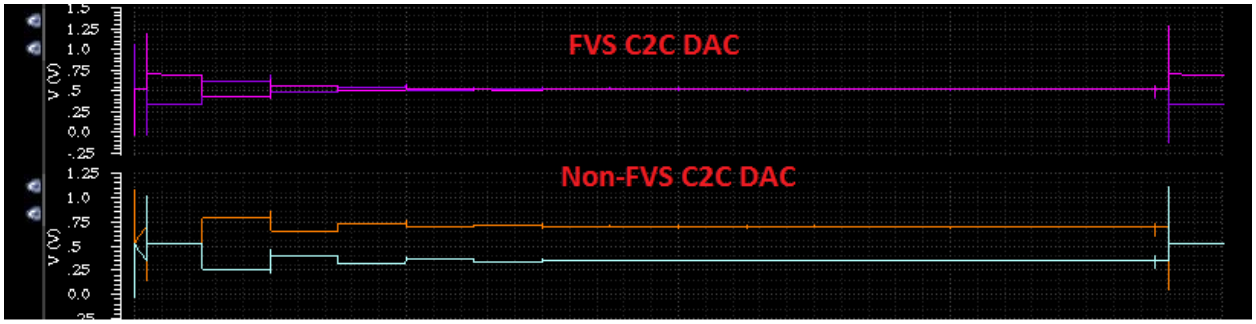

Figure 4 Floating Voltage shield comparison of DAC output

As seen above, with Vin = VDD/6 (output code 101010101010, meaning the two lines would cross each other at each transition) the non-FVS C2C DAC had issues even converging on the 2nd transition, whereas the FVS C2C DAC had no problems converging for multiple bits. Thus, it is shown that the floating voltage shield concept proposed by [9] does improve linearity significantly.

Our results were as follows: Testing at Vin = VDD/6 (expected output code 101010101010) with a 100% parasitic capacitance (CPAR = CIN), a C2C DAC with floating voltage shield would be able to obtain 2 bits of accuracy, outputting the wrong value at the 3rd bit.. With 10% parasitic capacitance, (CPAR = CIN/10) the same C2C DAC would obtain six

bits of accuracy. With 1% capacitance, (CPAR = CIN/100), the same C2C DAC would obtain up to 8 bits of accuracy.

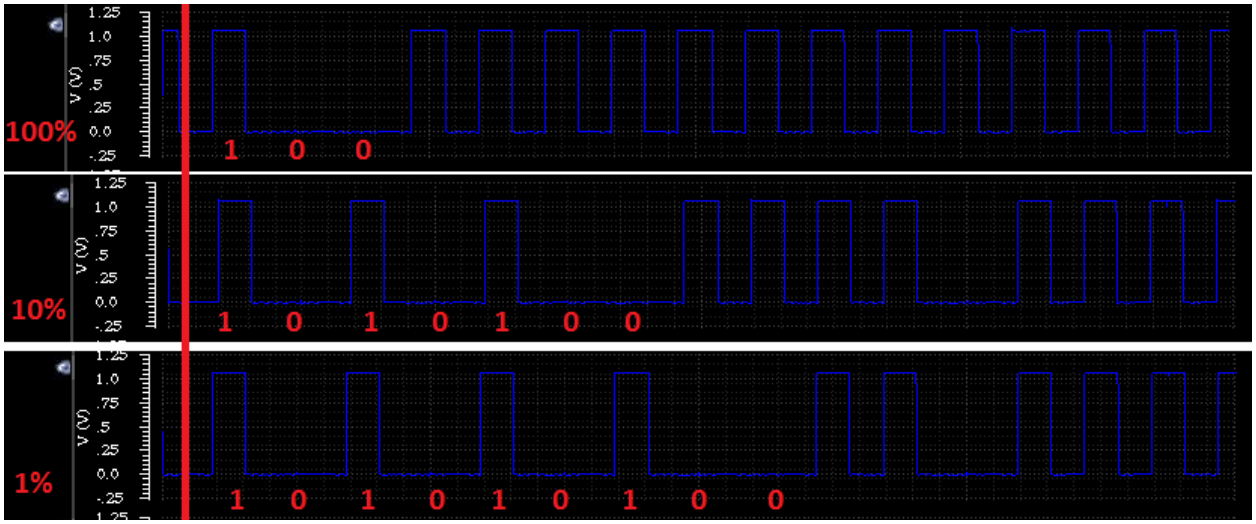

Figure 5 Output codes of FVS C2C DAC across a range of parasitic capacitances

This leads to an expectation that a hybrid 4-binary 8-C2C DAC would be able to provide 10 bits of accuracy.

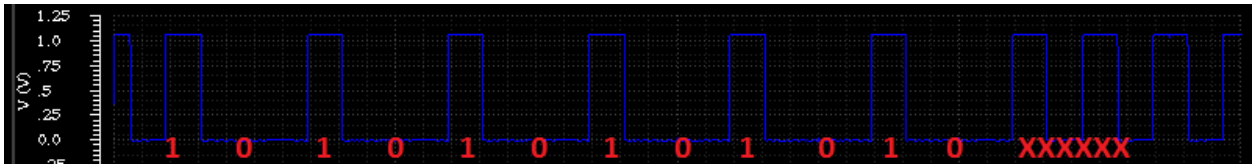

Figure 6 Hybrid C2C DAC output with Vin = VDD/6 and CPAR = CIN/10

However, in the process of testing different combinations of hybrid DACs, I discovered that a 9-C2C 3-binary DAC was sufficient for our needs. For an input of Vin = VDD/6 (expected output 101010101010), the hybrid DAC was correct for all 12 bits. A lower number of binary bits means less total DAC capacitance and power, which led us to choose a 9-C2C 3-binary hybrid DAC.

The digital logic was implemented with transmission flip-flops, which offer power savings [19]. By sweeping the gate lengths, we determined that the optimal gate-length was 70nm.

The latch comparator was designed with minimum power consumption in mind. To that effect, the comparator was clocked at 20kHz, and the length of the transistors was swept from 30nm to 200nm with the parametric sweep. The optimal length was found to be 60~70nm (much like the digital SAR logic) – past that point, there leakage current was not reduced significantly. Meanwhile, the clock power increased proportionally to gate length.

During the first phase, all of the nodes are pulled to either VDD or ground by reset switches. During the second phase, the reset switches are turned off, and the comparator is allowed to settle to a steady state. Based on the input, differential pair will pull on one of the inverters more than the other. This quickly manifests itself in a positive feedback loop, and an output is realized.

The comparator makes a decision relatively quickly. We did not need to optimize for speed due to the inherently high f_T of the 32/28nm process node.

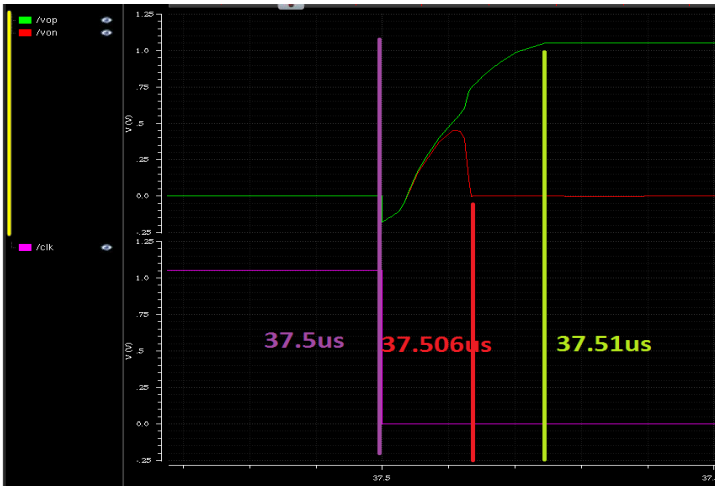

Figure 7 Comparator transient

Using an input difference of ½ LSB (512uV) the comparator reaches positive feedback around 5ns after the clock edge. 6ns after the clock edge, one output pin has already reached a rail, and after 10ns, both outputs have railed out. We are running our comparator at 240kHz, which means it has 4us to make a decision – plenty of time for our latch.

The comparator noise is as follows:

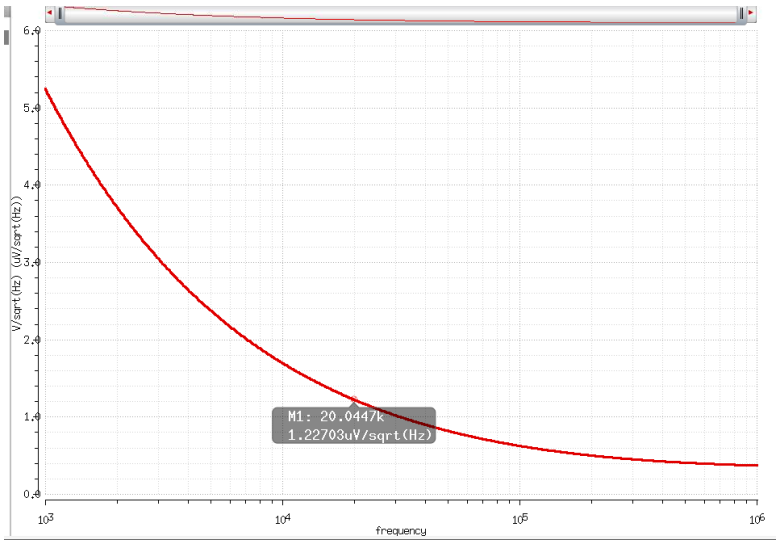

Figure 8 Comparator Noise

The comparator noise is much less than the KT/C thermal noise or the quantization noise.

Using the method described in the Methods and Materials section, DNL and INL were measured and the results were compiled in an excel spreadsheet. The DNL and INL are +4 and -4, respectively.

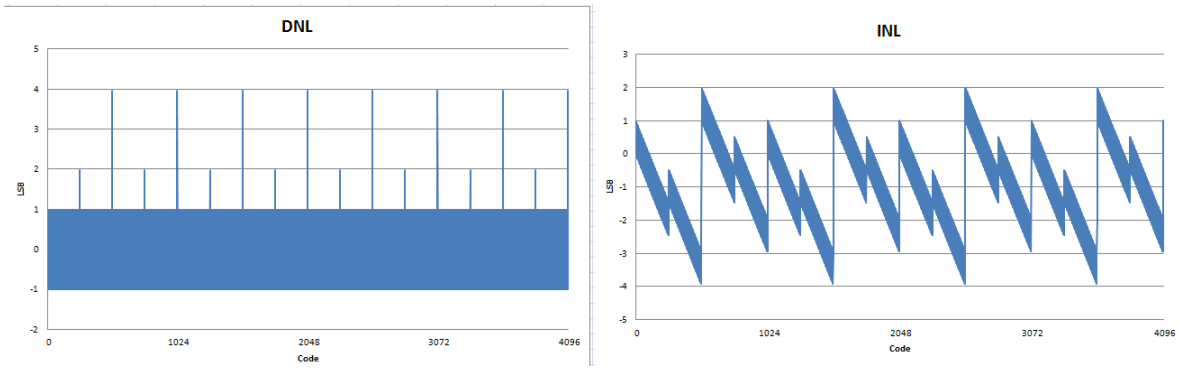

Figure 9 DNL and INL graphs

One issue that is apparent from the DNL plot is that the last bit does not seem to work. The non-working bit manifests itself as one code being twice as long as it should be, and one code completely missing, which translates to DNL jumping constantly between -1 and 1. We tried to reduce the parasitic capacitance to 0, but the missing bit would not go away. This is likely due to the voltage drop across the sampling switches, and could be fixed by utilizing bootstrapping.

Another issue that becomes apparent in the INL plot is the missing codes at the 5^{th} and 3^{rd} MSB. At the 5^{th} MSB, there is a transition with two missing codes. At the 3^{rd} MSB, there are more missing codes that sometimes cancel out and sometimes add on top of the missing codes at the 5^{th} MSB. As such, the INL plot appears as a sideways Z shape with differing amplitudes of INL. However, these missing codes at the 5^{th} and 3^{rd} MSB go away when CPAR is set to a value less than 10% of CIN. Thus, these nonlinearties can be attributed to C2C DAC parasitics.

Based on the INL, the SFDR can be approximated. Assuming a slow input signal, the SFDR is:

$$SFDR = 20\log\left({}^{2^B}/_{INL}\right)$$

Equation 2: SFDR from INL equation

With an INL of -4 in a 12-bit converter, the SFDR is 60dB, or 2.05mV of the full scale range of 2VDD = 2.1V. In this case, the SFDR much larger than the capacitor KT/C noise (256uV) and the quantization noise (74dB). The comparator noise is also irrelevant. In short, SFDR dominates the SNDR of the comparator, and we can calculate ENOB using SFDR as an approximation for SNDR.

$$ENOB = \frac{SNDR(dB) - 1.76dB}{6.02dB}$$

Equation 3: ENOB from SNDR

Plugging SNDR ~= SFDR = 60 to [Equation 3], our ENOB is 9.7. While not quite at diagnostic quality of 10 ENOB, it is possible to improve INL and SFDR to raise our ENOB above 10 with a better capacitor layout scheme that reduces parasitic capacitance.

ADCs are often ranked on a figure of merit that balances such characteristics as ENOB, power, and frequency [20]. One popular FOM (Figure of merit) metric is the following:

$$FOM = \frac{POWER}{2^{ENOB} * f_s}$$

Equation 4: Figure of Merit [21]

A recent survey [21] of ADCs indicates that sub 10fJ/conv-step converters are among the most power efficient, and the vast majority of the sub-10fJ/conv-step converters are SAR ADCs.

However, few are implemented in sub 45nm technology. One 200ksample ADC implemented in 40nm technology using a skip-and-detect algorithm and two types of comparators achieved 0.85fJ/conv-step [22]. However, they did not utilize a C2C array, opting to use a binary weighted DAC instead. By comparison, our ADC utilizing a FVS C2C array and implemented in 32nm technology achieves 0.59fJ/conv-step.

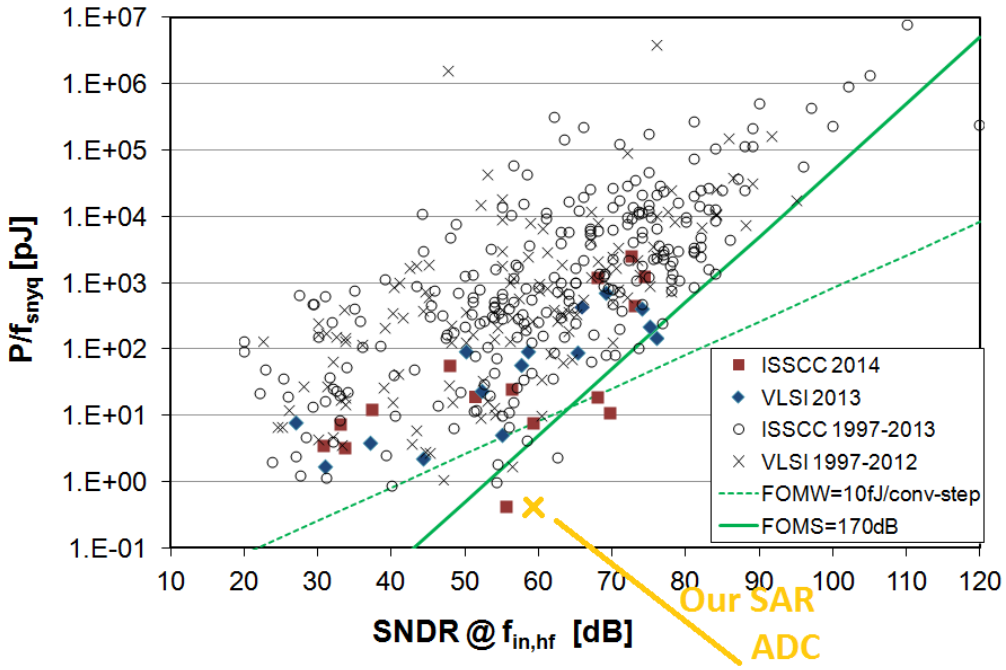

Figure 10 - Figure of Merit Energy comparison

Conclusions

Overall, while the performance is impressive, our ADC still has many issues. These issues will only get worse when layout happens and issues such as mismatch and parasitics come into play.

One issue was the excessive INL that resulted in high SFDR and reduced ENOB. However, this was because we were overly conservative in estimating the parasitic capacitance on the DAC. Modern capacitor processes can achieve parasitic capacitances below 1% of the capacitor's nominal capacitance. Utilizing CPAR = CIN/100 should reduce the INL and bring ENOB above 10.

Clock/gate boosting, or bootstrapping [23] is another technique that may improve our performance. Our current switches are implemented as transmission gates, which reduce charge injection. However, the transmission gates do not scale well to low voltages, which means our voltage is fixed to around 1.05V.

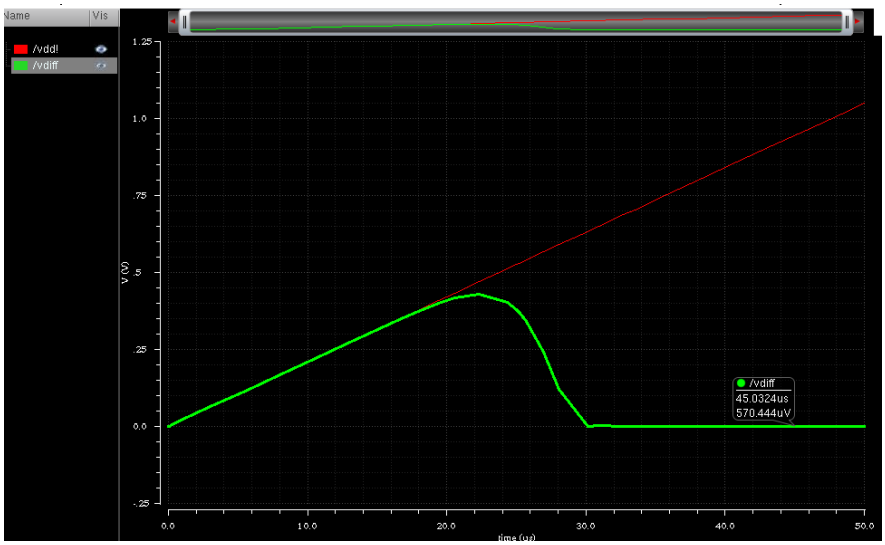

Figure 11 - Transmission Gate gate sweep

As seen in the Figure 11, even at 0.8V, the voltage drop across the transmission gate is 1LSB. This voltage drop may be the reason why the last bit in our conversion never works. Consequently, we may be able to improve our performance and power by bootstrapping both gates on the transmission gate. This will allow the gate to operate at higher voltages and also reduce the voltage drop across the transmission gate itself, allowing the ADC to run at reduced voltage levels and increasing the linearity at the same time.

Another power saving tactic mentioned in [6] is to turn off bits that we do not need. This will reduce DAC capacitance and control circuitry, and consequently reduce power consumption. This can be used in low-power modes, where accuracy is not as important.

In spite of these drawbacks, our power consumption is a mere 9.8nW, and our figure of merit is 0.59fJ/conv-step. As it is, this will work well enough for its intended purpose of digital compressed-sensing. It can also serve as a drop-in replacement for the analog compressed-sensing front-end discussed in [3]. Next steps include implementing bootstrapping and implementing an actual layout once a capacitor is available in the 32/28nm library.

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