High Voltage Level-Shifter Circuit Design for Efficiently High Voltage Transducer Driving

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Research Project

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***Abstract*—This report describes a level shifter with crow-bar current suppression is proposed to achieve simultaneously high switching speed and low power dissipation for high-voltage transducer driving. Unlike prior implementations, the new circuit does not require additional high-voltage supplies nor static power consumption. The prototype switches up to 32 V with only 1.8 V input consuming less than 0.5 pJ/V^2 per transition. Delays as low as 16 ns and 8.2 ns for falling and rising transitions respectively with 1.8 V input are ideal for time-critical phased array beamforming applications and could be further reduced to 2.6 ns and 4.7 ns when driven with 3.3 V supply. Together with buffer circuitry, the circuit is able to handle loads up to 100 pF efficiently with frequency above 10 MHz, which makes the circuit favorable for high voltage transducers application such as ultrasonic imaging.**

I. Introduction

Many sensor interfaces. need high voltage actuation. Applications include electrostatic actuation or ultrasonic transducers [1], [2], where typical operating voltage varies from above 10V for piezo-electric transducers and Piezo-electric Micro-machined Ultrasonic Transducers (PMUT) to above 50V for Capacitive Micro-machined Ultrasonic Transducers(CMUT). Furthermore, the high resolution requirements necessities above 10MHz driving frequency for the transducers with over 10pF parasitic capacitance. To address the requirements we are presenting a driver capable of both high voltage and high band-width operation.

The remaining part of this report is organized as following: Section II. briefly describes the high voltage IC process and typical high-voltage sensor interface circuit. Section III. summarizes previous solutions for high-voltage driving. Section IV. explains the circuit we proposed for efficient high-voltage level-shifting. Experiment results are given in Section V, and finally conclusion is in Section IV.

There are several high-voltage processes available from various foundries. For example, the TSMC 32V/0.18um process, consists of normal transistors operating at nominal V_{DD}=1.8V, and special-designed high-voltage transducers operating at a relatively high supply voltage HV_{DD}=32V. Due to potential latch-up problems, the high-voltage transistors is inside high-voltage wells isolated with high-voltage guard-ring and high-voltage bottom isolation layer. Fig. 1 gives an example for

The high-voltage MOSFET (HVMOS) has thicker oxide thickness to prevent oxide breakdown from high gate voltage. A clear drawback is reduced C_{ox} and turn-on current. Furthermore, the minimum gate length of HVMOS in this process is limited to 1.5μm. Also HV devices need to be spaced further than LV transisters, not to mention area consumed by guard-ring itself. These several drawback make it challenging to design a high-speed high voltage circuit efficiently without large area or power penalty.

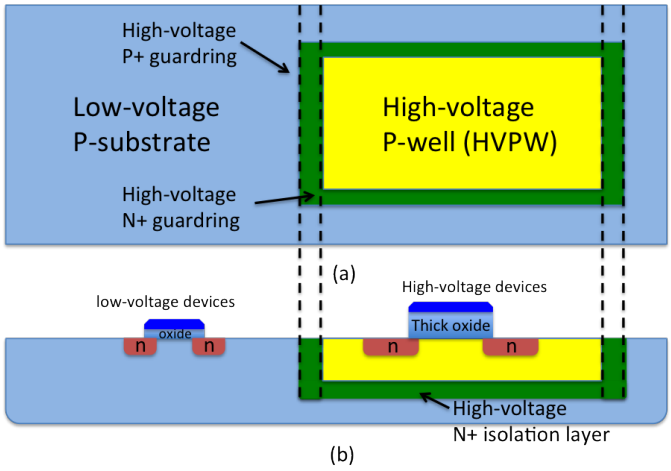

Fig. 1. Typical layout for high-voltage process (a)topview (b)sideview.

To minimize the area and power overhead, typical high-voltage sensor interface circuits perform most of the signal processing such as delay and frequency control in low voltage domain, following by a level-shifter to shift up the signal to high-voltage domain as illustrated in Fig. 2. The level-shifter often consumes significant power due to high supply voltage and has limited bandwidth due to the low f_T of thick-oxide high voltage transistors. Level-shifter described in this theses avoids these problems.

II. Previous work summary

There are several existing solution to convert low-voltage control signal to high voltage domains. Due to poor transconductance of high-voltage transistors, straightforward solutions based on linear amplifiers suffer from low efficiency and high circuit complexity. Similar to PWM audio amplifiers [3], drivers with only two output levels avoid these problems. These solutions exploit the inherent low-pass characteristic of the transducer to filter out harmonics but require high

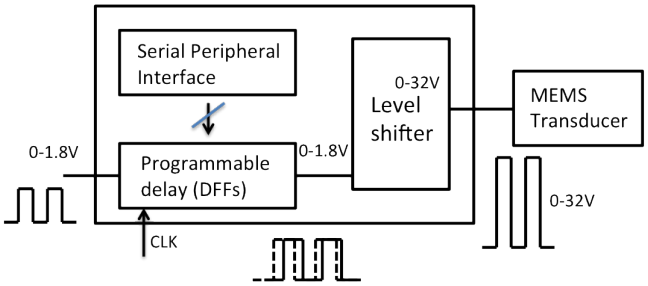

Fig. 2. Typical high-voltage sensor interface driver.

switching speed to meet bandwidth requirements and meet signal-to-noise ratio requirements.

The PWM driver interfaces the low-voltage digital control input to a high voltage switched output. Depending on the application, output voltages in excess of 30 V are required, corresponding to step-up ratios of up to 16 with 1.8 V input. Ideally, this entire gain is realized in a single stage to minimize circuit complexity and power in intermediate stages.

Fig. 3a shows an implementation of a latch-based level-shifter comprising an NMOS differential pair with low-voltage input and a PMOS negative resistance load [4]. Although simple, this circuit has several drawbacks. Firstly, the large overdrive voltage of the PMOS devices set by the high-voltage supply necessitates very wide NMOS transistors to overpower the load with the low-voltage input signal. The consequent high input capacitance limits the maximum operating speed and increases the power dissipation in the driver circuit. Secondly, although static, the circuit is subject to high dynamic power dissipation, owing to the crow-bar current flowing during the transition when both the NMOS and PMOS transistors are on, as indicated in the timing diagram. Particularly for step-up ratios in excess of five, high operating speeds and for small capacitive loads—characteristics that are representative of many MEMS applications [1]—these losses can significantly degrade the efficiency.

Several solutions have been proposed to overcome these limitations. The circuit in Fig. 3b employs degeneration in the NMOS devices to limit the maximum current to I_0 [5]. While this reduces the crow-bar current and hence improves power efficiency, this solution further degrades the maximum operating speed.

The circuit in Fig. 3c avoids these drawbacks by separating the functions of voltage step-up and output driver [6]. The latter consists of NMOS and PMOS switches with non-overlapping control signals generated with a level-shifter similar to that in Fig. 3a, but with cascodes in series with the NMOS input pair. Biasing the cascodes at approximately half the high-voltage supply reduces the PMOS overdrive voltage and hence the required NMOS pull-down strength. Although this solution can achieve fast switching times, the need for a separate high voltage supply is undesirable.

In this work, we propose a new architecture to suppress the crow-bar current that simultaneously achieves high switching speed and low-power operation while avoiding additional

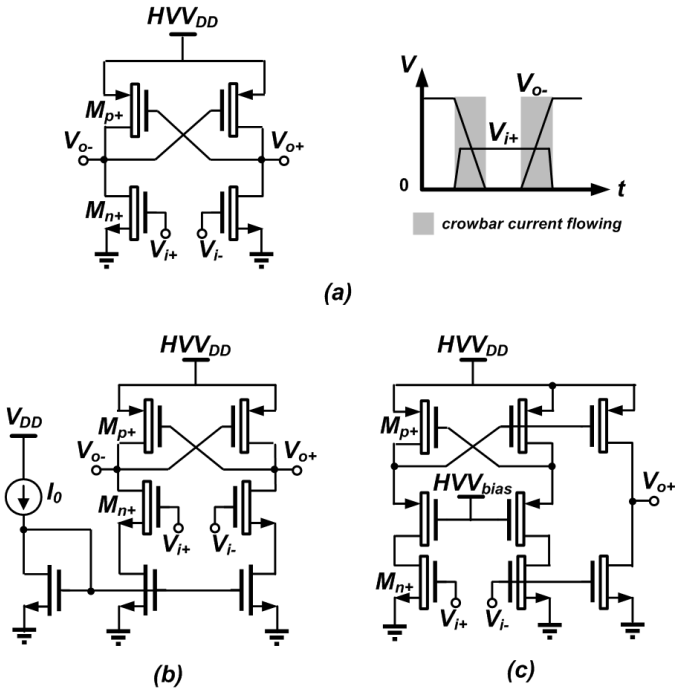

Fig. 3. Level-shifter. (a) Conventional (b) current limited (c) voltage limited.

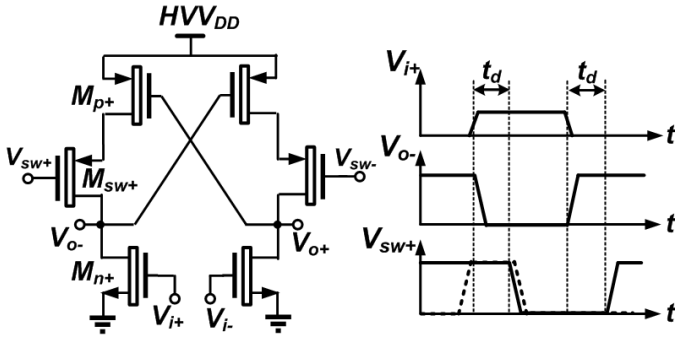

Fig. 4. High-speed level-shifter with crow-bar current suppression.

supplies.

III. Circuit Operation

A. Concept of crowbar current suppression

Fig. 4 shows the concept of the circuit proposed in this work. It retains the basic latch structure but introduces additional high voltage devices in series with the latching transistors. The timing diagram shows the signal waveform during a high-to-low transition of V_{o-}. As indicated by the dashed waveform, switch $M_{\mathrm{sw}+}$ is opened before the low-to-high transition of V_{i+} and closed after the output has settled. This effectively removes the pull-up $M_{\mathrm{p}+}$ from the output during the transition, thus enabling use of small NMOS pull-down $M_{\mathrm{n}+}$ with low input capacitance and permitting high speed operation. Opening $M_{\mathrm{sw}+}$ also prevents crow-bar current from flowing.

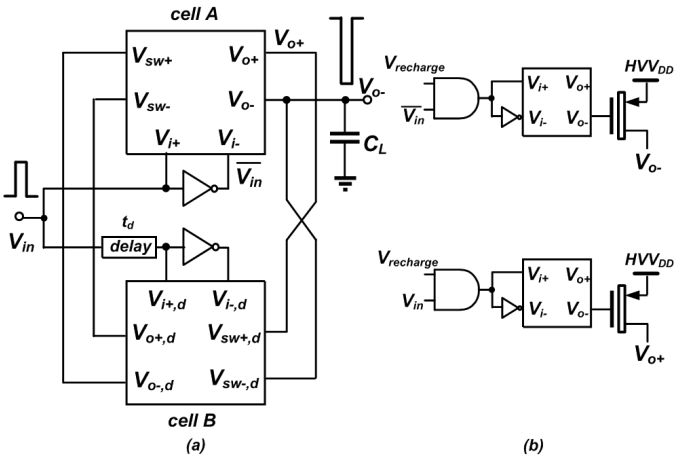

Fig. 5. (a) Block diagram for the proposed high speed level-shifter. (b) Idle recharge circuit.

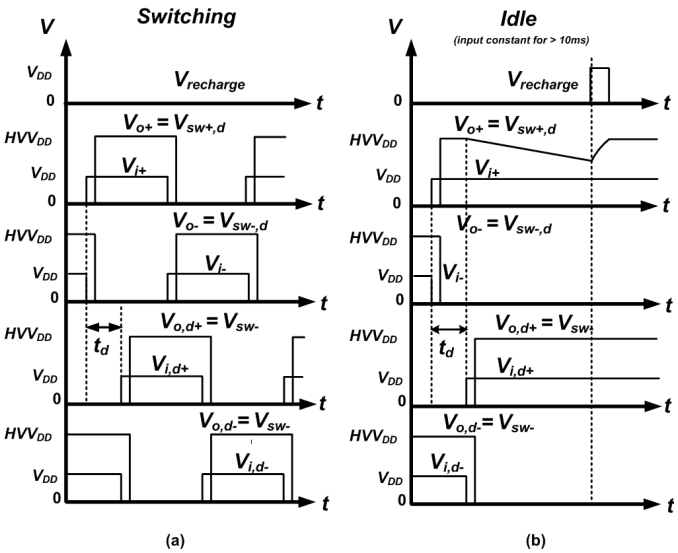

Fig. 6. Output waveform for the proposed circuit in (a) switching (b) idle operation.

Circuit implementations of the level-shifter in Fig. 4 have to overcome two problems: First, the dashed waveform for $V_{\mathrm{sw}+}$ leads the raising edge of V_{i+}. Although in some situations an appropriate control signal may be available, the solution adopted in this implementation, indicated by the solid trace, opens $M_{\mathrm{sw}+}$ after a fixed delay t_d after V_{i+} falls for preparing the incoming high-to-low transition of V_{o-}. The second challenge is that the switch controls V_{sw+} and V_{sw-} are high voltage signals themselves, requiring a level-shifter and hence high voltage switch control on their own. This is accomplished with two cross-coupled circuits like those shown in Fig. 4 where each cell provides the high voltage switch signals of the other.

B. Complete level-shifter circuit

From the timing diagram in Fig. 4 it is evident that the switch control signals are simply delayed and inverted versions the input and can hence be generated with an identical level-shifter driven with a delayed input. Fig. 5a shows the complete diagram consisting of two identical level-shifters whose outputs supply switch control signals for the other cell as indicated in timing diagram in Fig. 6b. Although functionally identical, in practice the device sizes in the two cells are chosen differently to accommodate for differences in the load.

C. Idle recharge

A potential problem occurs with this circuit when the output is not switching for a prolonged time, approximately $10ms$ for this implementation. Consider the circuit in Fig. 4 where V_{o+} is high. The stacked PMOS and NMOS devices are then on and off, respectively. To prepare for the next cycle operation, the switch transistor, controlled by V_{sw-}, is on initially but turns off after a short delay, as illustrated in the idle timing diagram in Fig. 6b. At that point V_{o+} becomes floating. In applications requiring static operation this situation must be avoided.

The problem can be circumvented by introducing a recharge circuit as shown in Fig. 5b consisting of static level-shifter in Fig. 3a and recharge signal $V_{recharge}$. As $V_{recharge}$ goes high, the circuit turns on HVPMOS to recharge V_{o+} back to HVV_{DD} and vice versa for V_{o-} when V_{o-} is high. Since $V_{o+,d}$, unlike V_{o+}, is always driven until V_{o-} changes state, there is no need to add recharge circuit to cell B. Unlike the core circuit, the operating speed of the recharge circuit is low facilitating implementation with small transistors to reduce power consumption and self-loading for the core circuit. In this work, $V_{recharge}$ is generated off-chip with an FPGA to indicate lack of activity in V_{in}.

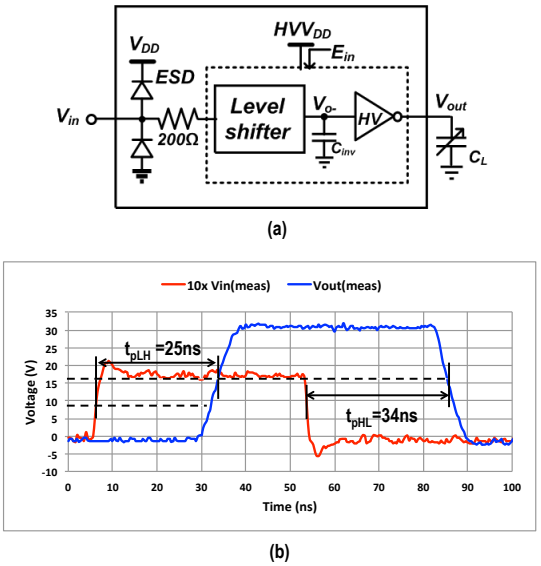

Fig. 7. Test setup (a) circuit diagram (b) waveform for 1.8 V input.

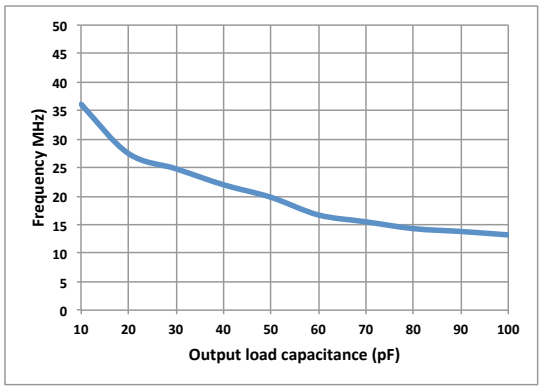

Fig. 8. Maximum frequency versus load capacitance

IV. Experimental Results

A. Maximum operating frequency

Fig. 7 shows the test setup and output waveforms. An inverter is used to isolate the level-shifter from the large off-chip load. With a 10 pF load capacitance, the delays (50 % V_{in} to 50 % V_{out}) are 25 ns and 34 ns for raising and falling edges, respectively.

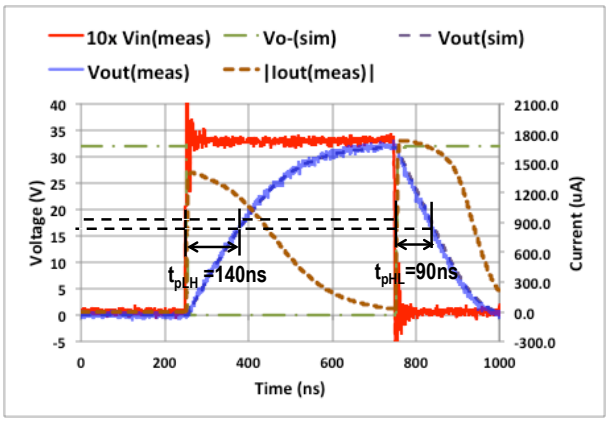

Fig. 9. Output waveform for minimum-sized level-shifter.

Fig. 8 shows the measured maximum frequency versus load capacitance for a 10 % HVV_{DD} to 90 % HVV_{DD} output swing. It indicates a maximum rate in excess of 20 MHz for loads up to 50 pF, suitable for demanding applications such as ultrasonic imaging [2].

B. Minimum-sized level-shifter

For lower operating speeds the buffer can be omitted to reduce power dissipation. Fig. 9 shows the 32 V high voltage output of a minimum-sized level-shifter to a 3.3 V control input. The delay is approximately 140 ns and 90 ns (50 % V_{in} to 50 % V_{out}), dominated by the 10 pF load from the oscilloscope probe. Without the output probe capacitance, the energy consumption is 430 pJ per switching operation.

The low power dissipation makes the circuit attractive to interface between different voltage domains in digital circuits

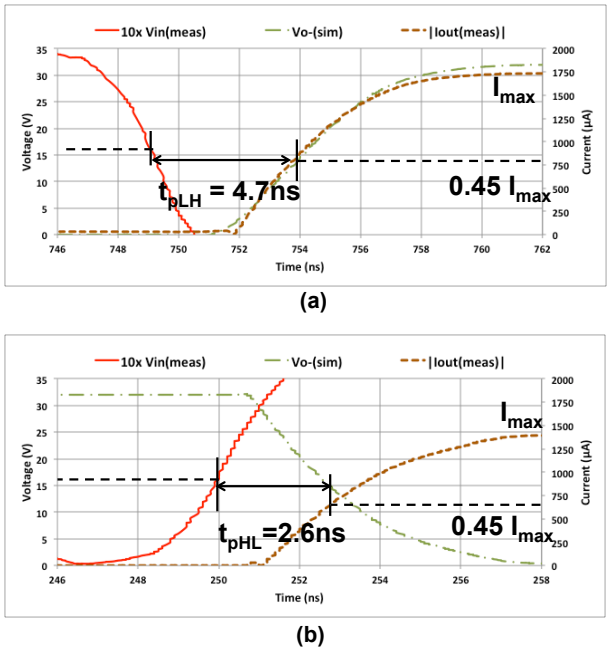

Fig. 10. Delay for (a) rising and (b) falling V_o for 3.3 V input.

with topical loads of less than 100 fF [4], [6]. In this case, delay drops to 4.7 ns and 2.6 ns with 3.3 V input and 16 ns and 8.2 ns for 1.8 V input for raising and falling transitions respectively (Fig. 10). These numbers are inferred from inspecting the current flowing into the load capacitor which drops to to approximately 45 % (inferred from simulation) of its peak value when $V_{\text{o}-}$ reaches 50 % of the final level. The simulation waveform of $V_{\text{o}-}$ is also shown in the figures to prove the 45 % current estimation.

C. Chip area and comparison

Fig. 11 shows the die photograph of the minimum-sized level-shifter fabricated in a 180 nm CMOS with 32 V high voltage transistors and 6 levels of metal. Unlike conventional level-shifters which require much larger NMOS than PMOS devices to adjust for the large difference in overdrive voltage, in this design both devices are of comparable size, resulting in substantially reduced die area. Note also that in this design guard rings and other layout overhead take up significant area that could be shared in an application requiring several level-shifters.

Tab. 1 compares the performance to prior art. The proposed circuit has a significantly higher maximum operating voltage of 32 V versus 10 V and works for inputs as low as 1.8 V. Unlike the result in [6], it does not require an auxiliary high voltage supply. It has no static power dissipation and thanks to crow-bar current suppression achieves the lowest energy (normalized with $(HVV_{DD})^2$) per switching operation. The table summarizes results with and without the output buffer. The dynamic energy reported in the table includes both the

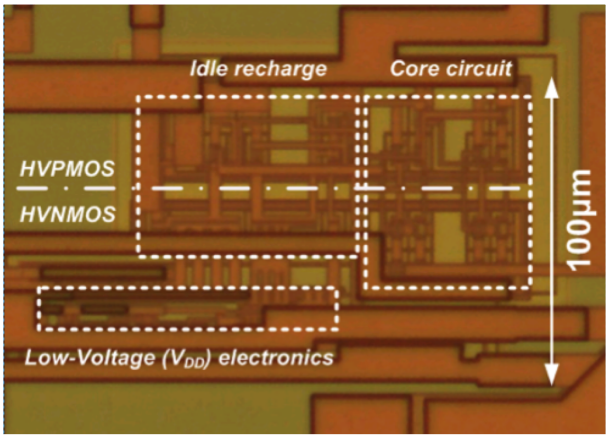

Fig. 11. Die Shot.

Table 1. Performance Summary

	[6] Level-shifter JSSC,11	[7] Level-shifter ESSCIRC,11	[8] Ultrasonic ITCAS-II, 13	This work (with buffer)	This work (without buffer)
Output voltage(V)	6.7-10	2.5-5.0	0-10	0-32	0-32
High voltage supply(V)	6.7, 10	2.5, 5	10	32	32
V_{DD}(V)	3.3	1.2	1.8	1.8	1.8/3.3
Load condition	unloaded	unloaded	15pF	10pF	unloaded
*Dynamic energy per cycle / V^2	0.5pJ/V^2 *simulated	112pJ/V^2	N/A	15.3pJ/V^2	0.42pJ/V^2
Static Power	~0	5uW	> 2mW	~0	~0
Circuit latency	3 ns	0.52 ns falling 0.61 ns rising *simulated	47.5 ns falling 42.5 ns rising	32 ns falling 25 ns rising	16.0/2.6 ns falling 8.2/4.7 ns rising
Chip area (active)	N/A	N/A	0.022mm^2	0.028mm^2	0.015mm^2
Technology	0.35um HV	65nm	0.18um BCD	0.18um 32V	0.18um 32V

energy consumed in the level-shifter and delivered to the load ($5pJ/V^2$ for 10pF). The circuit has no static power dissipation other than leakage.

V. Conclusions

Series switches eliminate the crow-bar current to enable high-speed and low-power operation of a rail-to-rail level-shifter. The small size and high output voltage up to 32 V are particularly attractive for MEMS applications such as ultrasonic beam forming [1], ultrasonic imaging [2] and electrostatic actuation. The architecture has also the potential to reduce power dissipation in digital I/O level-shifters [4].

Acknowledgment

The authors would like to thank the Taiwan Semiconductor Manufacturing Company (TSMC) for chip fabrication and Pramod Murali for helpful discussions.

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