Sensing Systems Using Large Area Printed Organic Electronics

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Technical Report No. UCB/EECS-2023-240
http://www2.eecs.berkeley.edu/Pubs/TechRpts/2023/EECS-2023-240.html

December 1, 2023

Acknowledgement

This thesis has been in collaboration with my other colleagues, which would not have been possible without them.Thanks to Adrien Pierre, who trained me, guided me through the lab since my undergraduate time at Berkeley.
Thanks to Lilian Solares with whom worked together in the lab as well.
Thanks to Prof Boser's group, Burak Eminoglu and Eftyhmios Papageorgiou.
Thanks to all the Arias group who supported me on this way.
Words cannot express the support and love of my parents, brother and lovely uncle Alireza. And in the end, I want to especially thank my fantastic advisor Prof. Ana Arias who allowed me to stay and work in her lab. Ana’s EE 134 class was the lucky and life-changing course that I took in my undergrad time.

Sensing Systems Using Large Area Printed Organic Electronics

by

Mahsa Sadeghi

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering - Electrical Engineering & Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

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Summer 2020

The dissertation of Mahsa Sadeghi, titled Sensing Systems Using Large Area Printed Organic Electronics, is approved:

Chair _____ Date _____

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University of California, Berkeley

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Abstract

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Organic electronics is an emerging technology with advantages of mechanical flexibility, solution-processability, and high-throughput manufacturing at low temperatures on inexpensive and light-weight substrates such as plastic, paper, and fiber in large-scales not possible with high-temperature processing techniques. While the performance of devices cannot rival the silicon counterpart, the performance should be tuned to meet the required specifications of the application in mind. This thesis will overview the performance of the organic thin transistors (OTFTs) and organic phototransistors (OPTs) optimized and used for circuits and large area sensing applications. The work first covers the printing techniques employed for the fabrication of organic devices on the flexible substrate. There have been device-level optimizations for scale ratio tuning and power improvement by using a bilayer gate dielectric structure. We also introduce a novel technique for rapid and digital modulation of the scale ratios. Interconnection is done with the screen printing method for the fabrication of printed flexible logic circuits and an OTFT weak classifier for data classification. The OPTs, with a good dual performance as both transistor and photodetector, are capable of merging the sensing and function generation in one substrate, which can reduce system complexity.

To my parents, brother, and uncle Alireza

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Acknowledgments

This thesis has been in collaboration with my other colleagues, which would not have been possible without them. I was lucky to start my lab works with Adrien Pierre, who trained me, guided me through the lab since my undergraduate time at Berkeley. Thanks to my lovely counselor Shirley Blake who was one of the reasons I got into UC Berkeley for my undergraduate studies. She may rest in peace. Thanks to Lilian Solares with whom worked together in the lab as well. I 'll miss Shane Bernard kickboxing classes and gym time with my friends and colleagues Alla Zamarayeva and Natasha Yamamoto. I also had fun times with them in our printed electronics lab. Thanks to Prof. Boser group and friends and colleagues, Burak Eminoglu and Eftyhmios Papageorgiou, for their continuous help and support. I learned a lot from them. I want to thank my friends and colleagues Yasser Khan and Seiya Ono, for their help, discussion, and technical support. I especially thank my close friends Shirin Gerami, Samin Ahmadzadeh, and Ahmad Fotovat, who changed life view through our charity works and trips since my high school time. I want to thank my dear friends Peyman Delparastan, Rozhan Rabbani, Ali Moin, and Hossein Najafi, Sajjad Moazeni, for their excellent help and support.

Thanks to my beloved friends Ethan Chorin and his dog Newton, and Johnny Pujol. Thanks to Maruf Ahmed, and Anju Toor for their help and support. Thanks to Neeka Mirpour. I want to thank all the Arias lab members, especially Jonathan Ting, Claire Lochner, Aminy Ostfeld, Maggie Payne. I would also thank Carlos Biaou, who has been a great friend and colleague. The piano and classical music have been my other love and passion, and I would like to especially thank my piano instructor, Prof. Jeffrey Sykes, at UC Berkeley, with whom I continued my piano studies during grade school. Thanks to my lovely cousins Mojgan Damghani, and Kevin Zahedi who have greatly supported me in United States. Thanks to my dear Sahand Shahlapour, whom I had the opportunity to know in the last year of my grad school and has supported me since then and I feel blessed. I am fortunate to have Ali, my elder brother, who has been my role model, supporter, and close friend since I was born. I could not have survived in the united states during the hard times of immigration without my uncle Alireza's help and support. Words cannot describe my parents' sacrifices for me and their struggles for my brother and me. Thanks to my wonderful mom and dad!

And in the end, I want to especially thank my fantastic advisor Prof. Ana Arias who allowed me to stay and work in her lab. Ana's EE 134 class was the lucky and life-changing course that I took in my undergrad time.

Chapter 1

Introduction

For many years, inorganic semiconductors have been utilized as the active layer of thin-film transistors (TFTs). Since the 1980s, many applications have successfully incorporated TFTs. Among them, mass-produced commercially available displays can be highlighted as one of the most prosperous products by employing TFTs for backplanes. In recent years, the perception of large-area printed and flexible electronics, such as foldable displays, has developed a strong attention to organic semiconductors (OSCs) due to their mechanical properties. The use of solution-processable OSCs combined with large-area printing techniques are believed to have the highest impact on the manufacturing costs by eliminating costly lithography methods. [21]. Organic thin-film transistors (OTFTs) use small molecules, polymers, or the mixture of both, for the active layer. The solution solubility of the OSCs enables high-throughput fabrication of OTFTs at lower costs and temperatures. The low-temperature processing techniques are compatible with manufacturing on a variety of flexible [30, 155] and even stretchable materials [77, 99] not achievable by high-temperature conventional methods. Another benefit to mention is the great potential for continuous enhancement in the OSC's performance and functionalization by molecular structure tailoring and physical bending [91]. The versatile device structure of OTFTs enables integration of various functions with similar processes on the same plastic, creating flexible integrated systems in compact form factors without a significant increase in thickness and weight [37]. In general, the mentioned benefits attributed to the organic electronics, can be promising for emergence of many rising applications using the OTFTs.

1.1 Thin-film transistor device structure and performance

TFT is a three-terminal device, including a thin semiconducting channel layer, organic or inorganic, source and drain electrodes responsible for charge injection into the channel, an insulating layer for capacitive control of the charge in the channel, and a gate electrode controlling the charge flow in the channel from the source and drain electrodes. The distance

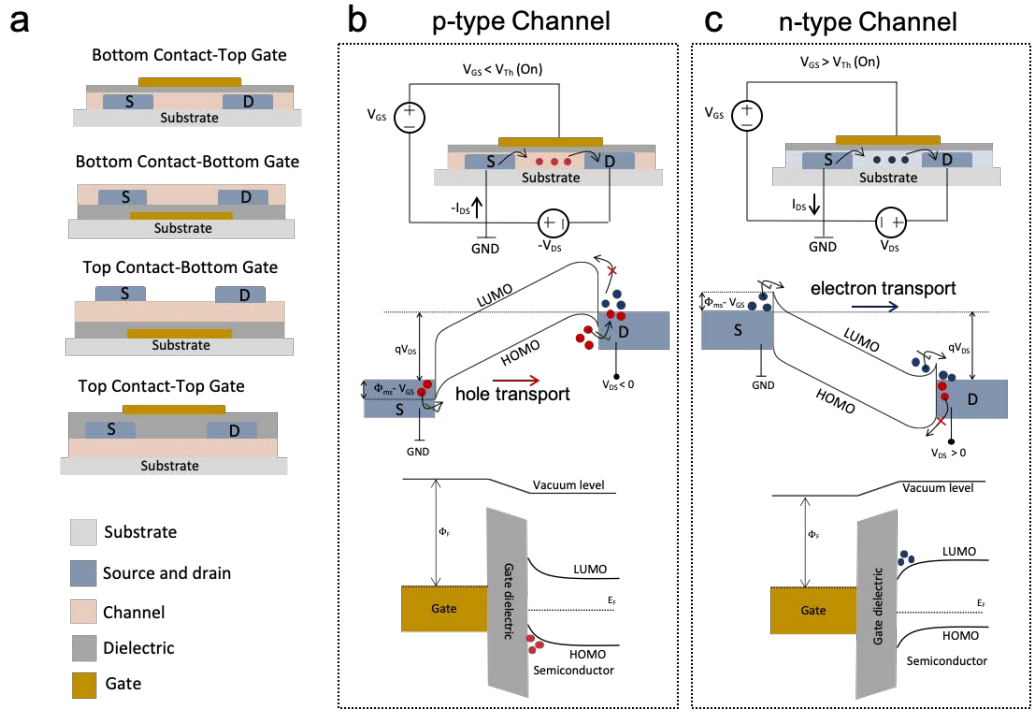

Figure 1.1: (a) Four standard configurations of the TFT device; bottom contact-top gate (BC-TG), bottom contact-bottom gate (BC-BG), top contact-bottom gate (TC-BG), top contact-top gate (TC-TG). (b) The biasing of the OTFTs in on-state with a p-type semiconductor channel on the top and the n-type semiconductor channel on the bottom. (c) Energy band diagrams of OTFT device with the p-type and n-type channel. In the p-type OTFT with the biasing condition of negative V_{DS} and negative VGS, only the holes can transport through the channel while the high barrier blocks the electrons to enter the channel. In the n-type OTFT, with the positive V_{DS} and positive V_{GS}, only the electrons can transport with the holes blocked due to the high barrier.

between the source and drain electrodes and the width of the source and drain electrodes interfacing the channel are known as length (L) and width (W) parameters accordingly. The W/L is called scale ratio, a critical parameter for design, and impacting speed in the circuits. Variation of the arrangement of the gate, and source and drain electrodes relative to the semiconductor channel results in various OTFT structures. Figure 1.1a demonstrates four possible architectures of the TFT device. OTFT devices have adopted two main TFT structures, including top contact-bottom gate (TC-BG) and bottom contact-top gate (BC-TG). In addition, another known structure is the dual-gate (DG) configuration [67][106]. The TC-BG is the popular configuration incorporated in the OTFTs with a wide variety of dielectric and semiconductor materials [6]. In the top-contact structure, the semiconductor

channel is deposited onto the patterned source and drain electrodes while in the bottom-contact structure the order is reversed. The two structures with the same components show different behaviors with top contact devices demonstrating higher mobility and performance in comparison with the bottom contact configuration [36, 96, 129]. The higher contact resistance due to the contact barrier at the metal-semiconductor barrier [96], the non-uniformity and poor morphology of the deposited semiconductor channel around the patterned source and drain electrodes [58, 71, 76] are some of the underlying reasons explaining the inferior performance of bottom contact structure. In the bottom contact structure, the charge flow in the channel is finite to narrow lines along the channel width at the edge of the contacts resulting in a reduction of contact area in comparison with the top contact structure. The smaller contact area generates large contact resistance [40]. It is shown that even by fixing the contact resistance, the bottom contact structure still suffers from lower mobility in comparison with the top gate structure suggesting that structural difference impacts mobility and performance [38]. The operation principles of OTFTs can be defined and compared with metal-oxide-semiconductor field-effect transistors (MOSFET) despite the differences such as channel formation. Both devices are voltage-controlled current-source devices with the gates capacitively coupled to the channel. In a MOSFET, the channel forms in an inversion process while the OTFT channel is formed by charge accumulation in the semiconductor layer [46]. Upon the application of proper bias voltages between the gate and source electrodes called V_{GS}, the accumulation charge is induced and controlled at the semiconductor and dielectric interface. The minimum voltage required for the formation of accumulation charge at the interface is known as threshold voltage (V_{Th}), one of the crucial parameters to be tuned in circuit design [87]. Much of the accumulated charge at the interface is mobile in response to proper voltage bias between the source and drain electrodes which causes charge flow between the source and drain electrodes. When no gate voltage is applied, the channel conductance is very low due to the absence of mobile charge carriers known as the OFF state. The OTFT becomes ON when adequate mobile charges are accumulated in the channel by Increasing the gate voltage and passing the V_{Th} in the negative and positive direction for the p-type and n-type semiconductor channel accordingly. In an OTFT device, which is generally unipolar, only one type of majority carrier transports in the channel, electrons in the lowest unoccupied molecular orbital (HOMO) for an n-type device and holes in the p-type device in the lowest unoccupied molecular orbital (LUMO). The HOMO level is analogous to the valence band of silicon and contains bonding states of the $\pi - orbitals$ with filled electrons and LUMO level, comparable to the silicon conduction band, consists of empty higher energy anti-bonding (π*) orbitals. Figure 1.1b shows the on-state biasing (negative V_{GS} and V_{DS}) of a p-type device and the horizontal (from the source to the drain) and vertical (from the gate to the channel) with the mentioned applied biases. Figure 1.1c depicts the mentioned schematics for the on-state of an n-type device with the positive V_{GS} and V_{DS} biasing. In the p-type device, the fermi level (E_F) of the metal is adequately matched with the HOMO level of the semiconductor enabling the charge injection and transportation from the source to the drain with the electrons blocked facing a large barrier. This is reversed for the n-type device. The large barrier from a distanced HOMO to the E_F stops the holes. Electrons enter

the channel owing to the closeness of the LUMO level to the E_F of the metal.

1.2 Materials

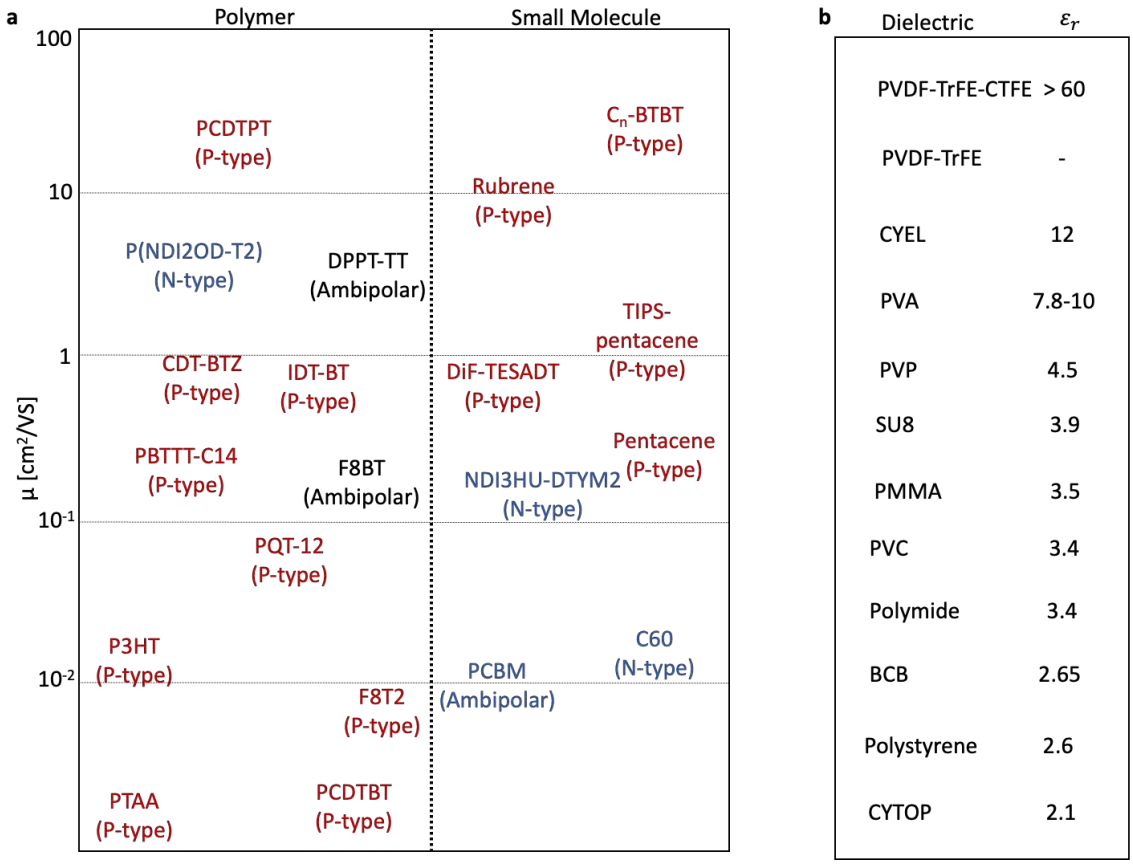

Figure 1.2: (a) Summary and comparison of the mobilities of typical n-type and p-type materials used in many applications. The very high reported mobilities are believed to be overestimated due to the extraction of μ from transistor ideal model such as high contact resistance [37]. (b) Summary of common gate dielectric materials used in OTFTs [37].

Organic Semiconductors

Higher mobility (μ) has been one of the primary concerns of OTFTs with printed organic semiconductor layers strongly influenced by the crystallinity [27]. Over the past years, many works have focused on improving the charge μ mobility. While there has been a significant improvement, most of the reported data are contaminated with overestimation in the

reported mobility over the past 30 years, known as mobility hype, discussed precisely in the review paper [107]. Usually, the mobility is extracted using the gradual channel approximation (GCA) introduced by Shockley's theory defined for an ideal device. GCA is under on several assumptions, such as no ohmic contacts, zero channel thickness, no diffusion, and mobility being independent of biasing conditions [78, 114]. The OSCs deviate from the ideal model due to the covalently bonded molecules held together by weak van walls bonding, causing disordered microstructures. OSCs don't have extended states and are cluttered with trapping sites, also sensitive to measurement abnormalities generated by minority carrier injection and barrier [107]. The design and processing of the OSCs, with large intrinsic bandgaps of 2-4 eV, play an essential role in the formation of high built-in voltages at the interface to the contact and high Schottky barriers in the OTFTs [10]. One of the critical features showing the deviation of OTFTs from the ideal model is known as the "kink," "hump," or "double slope" caused by the contact resistance (R_C). Extraction of the mobility from the steeper and low-voltage region in the kink results in an inaccurate overestimation of μ as transistor characteristics are governed by charge injection and R_C is strongly effected by change of V_G at lower voltages [107]. Based on the studies and computer-aided models[107], a change of R_C and the ordering of OSC strongly affect the linear shape of $\sqrt{I_D}$ vs V_G, seen in the ideal model. At lower values of R_C there is a linear relationship between the $\sqrt{I_D}$ and the V_G and μ is extracted accurately. By a significant R_C increase, there are transformations in the shape of the linear structure and the derived overestimated. Figure 1.2a [37], summarizes a large number of common n-type and p-type in two categories of small-molecules and polymers used in many applications. In general, both vapor deposition techniques and solution processing techniques can be used to process the OSC materials. Most of the commonly used small molecules and polymers, as shown in Figure 1.2a, are p-type due to the better work function matching of p-type materials, which have large bandgaps to the available electrode materials. For a long time OSCs such as (3-hexylthiophene-2,5-diyl) (P3HT) [100] and polytriarylamines (PTAA) [142] with mobility of 0.01-0.01 cm^2/Vs of 0.001 cm^2/Vs were commonly used polymers in many works. However, reported mobilities remained at a certain level for a long time and did not pass a limit of 1 cm^2/Vs. In recent years, considerations of techniques and materials such as donor-accepter (D-A) [138, 162], small molecule/polymer blends [52, 92, 105, 118] have successfully improved. However, many reported μs are overestimated negligence of non-idealities as explain at the beginning of the section. Many works have focused on enhancing n-type materials μs due to the demand for complementary circuits requiring higher mobilities to match the performance of p-type semiconductors. So far, reported electron mobility is about 1.2 cm^2/Vs the small molecules [161] and 6.4 cm^2/Vs in the polymers [12, 37].

Gate Dielectrics

Achieving higher power efficiencies and lower operational voltage is another hurdle for the OTFTs to overcome and improve due to the constraints defined by many envisioned applications in functional systems [144]. The gate areal capacitance (C_i) is a critical element

tuning the carrier charge at the interface of the semiconductor and dielectric layer, which is proportional to the dielectric constant (ε_r) and the dielectric thickness (d). The subthreshold characteristics of a device determine the operating voltage required for switching the transistor and change of the channel conductivity by applying the gate voltage. The subthreshold voltage regime range is determined by the voltage difference between the turn-on (V_{ON}) and the threshold voltage (V_T) of the device. The threshold voltage is the minimum gate voltage needed to switch the device from two states of ON and OFF [132]. The larger (C_i) for enhancement of the speed and power is attainable by either increase of the ε_r and reduction of thickness. Many OTFT works have utilized the commercially thermal oxidized (SiO_2) along with the self-assembled monolayers (SAM) for improving the carrier mobility and molecular packing in the channel by suppression of the hydroxyl group effects which contradicts the vision of cost-effective manufacturing and mechanical flexibility. Figure 1.2 b presents a summary of commonly used low-k dielectric materials in most works [37]. The increase of the C_i using the low-materials requires thinning the dielectric layer and prone to increase of gate leakage. High-k materials offer a reduction of operational power. However, the direct interface of high-k material with the channel degrades carrier mobility due to energetic disorders resulted by dipoles [37, 142]. In addition, to problems such hysteresis and instabilities are raised by using the high-k materials [133]. It is shown that the bilayer gate dielectric structure, with the low-k material in close contact with the channel, and the high-k layer on top eliminates the dipole effect on the carrier mobility [39, 133]. Some of commonly used high-k materials are Cyanoethylpullulan (CYEPL) [103], ferroelectric polymer poly (vinylidenefluoride-trifluoroethylene) [4], and relaxor ferroelectric polymer poly(vinylidene fluoridetrifluoroethylene-chlorofloroethylene) [P(VDF-TrFE-CFE)] [60]. The advancements in the materials enable more consideration of OTFTs for many large-area applications. OSCs offer mobilities higher than the a-Si TFT used in the backplanes. On-demand full additive printing of OTFTs is demanding and cost-effective. However, the strict requirements of high-end applications such as LCDs, e-paper displays, and X-imagers in which OTFT performs as a switch requires more fine structure and complicated multilayer integration and the additive techniques [37].

1.3 Applications

In particular, lower performances and variability are problems attributed to the OTFTs impediment to the adoption of fully printed devices for high-performance applications and cost-effective processing techniques [98]. In some reports, solution processing techniques are combined with the photolithography for gaining higher resolutions and device performance accordingly [116]. While there are benefits due to the merits of organic materials and solution processing, the ultimate prospect is more adoption of scalable and low-temperature budget printing techniques, with less assistance of costly photolithography techniques. As OTFT cannot compete with the performance of silicon counterpart, the goal is consideration for a suitable application instead of replacement. The optimization and development of OTFTs

in the large area depend on four main figures of merit: cost, power, and performance, and area which are demand-specific. The functionality of solution-processed OTFTs with the advantages discussed before is well-suited for low-cost (RFID) cards, flexible circuits, and chemical and biological sensors. OTFTs have been commonly used for row-column addressing of the sensors. [157]. In wearable sensors, the conformability and softness of flexible and stretchable electronics attached to the body enable health monitoring with minimal stress and discomfort associated with the wear [156]. The use of an amplifier circuitry printed adjacent to the sensor on the body can improve the reliability (signal-to-noise ratio (SNR)) and long term stability for in vivo monitoring periods with microvolt sensitivity [119]. In general, transistor-based sensors are combine the benefit of sensing and amplification. The sensors usually have high sensitivity as a slight change in the effective gate voltage induced by analyte can significantly change the output current [84]. The OTFTs sensors with benefits of high throughput sensing and high sensitivity have a broad spectrum of use in applications such as light-sensing (phototransistor)[93], environmental monitoring (chemical sensor) [55], artificial skin (pressure sensor) [86], food safety detection [6], or medical diagnostics [102]. In large-area sensors, the process of data readout and analysis of the whole array requires a hybrid system, which is complicated due to a large number of interfaces needed from the sensor array to the CMOS IC. The interfacing issue can be addressed using the active matrix; however, at large scales, the number of interfaces becomes noticeable. One introduced solution is the interfacing of the array of sensors to a variability-prone large array of OTFTs, to process the data and only transfer the high-level data to the CMOS. The compressed signal can be analyzed for decision making using the data-driven models enabled by machine learning algorithms [144]. In many sensing applications, only high-level information is required instead of a complicated analysis of the raw data from the whole array. For instance, detecting rising temperatures on the system's area can be sufficient to report an abnormality. As said before, organic electronics provide the benefits of low-cost scalable sensing—the use of OTFT for processing interfaced with the large printed flexible sensor to reduce the interface complexity. Only passing the high-level data can be demanding, especially for sensing applications and algorithms that can add intelligence to the system. However, the interconnection and the interfacing from the organic TFTs to the flexible sensor is a significant limitation. Besides, the fabrication of a sensor in the array with the OTFT can be challenging using printing solution processing techniques. As mentioned before, OTFT sensors behave as both sensor and amplifier. This dual performance can reduce system complexity by combining processing and sensing in one array and only passing the high-level information to the CMOS domain. The large number of interfaces going from the sensor array to the OTFT array can be eliminated.

1.4 Thesis organization

This thesis primarily focuses on novel printing techniques for the fabrication of a large array of organic thin-film transistors (OTFTs) and organic phototransistors (OPTs). There are

optimizations done for tuning of the scale ratio of devices, which is challenging using printing techniques and low viscosity inks. The devices are interconnected form circuits and finally used for sensing applications and data classification.

The second chapter demonstrates a novel fabrication technique used along with other printing techniques to form high-performance devices in a large flexible array of OTFTs with low variability on plastic. The primary printing technique combines surface energy patterning with blade coating. The source and drain electrode geometries are optimized to result in high yield. A small molecule/polymer blend in high boiling point solvents optimized ratio is utilized for the semiconducting layer.

In the third chapter following the same device materials used in the second chapter, we introduce a method for scale ratio tuning of devices in the large array. In this technique, the source and drain electrode geometry and width is optimized to change and alter the channel crystal. We demonstrate a method for the interconnection of OTFTs in the array and show the functionality of devices by making unipolar logic circuits.

The fourth chapter's primary focus is the demonstration of a novel technique for digital on-demand tuning the scale ratio of devices along with a large array. The electrodes are optimized to result in a high yield for the interdigitated structure. Using inkjet printing, we can digitally select the discrete electrodes to define the scale ratio of devices. The functionality is proved by making enhancement-load inverters.

In the fifth chapter, we show improvement of the power by using a bilayer gate dielectric structure. The combination of the high-k with a thin polymer layer significantly improves the power. The use of a high-k structure in close contact with the semiconducting layer degrades the carrier mobility due to the dipole effect. The insertion of a thin layer in between resolves this issue and enable the use of high-k materials for speed and power improvement.

In the sixth chapter, we use array of flexible OTFT for function generation used for a sensing and decision-making application. The connection of a flexible organic sensor substrate to the array of OTFTs is challenging and adds complexity. The OPTs are sensor-based OTFT providing the possibility of a combination of sensing and function generation in one substrate. We demonstrate a system to reduce complexity and merge the sensors and OTFTs in one substrate.

The final chapter briefly summarizes the derived conclusions of the discussed chapters along with future directions of research for large area printed flexible electronics with decision-making applications.

Chapter 2

All-printed flexible organic TFTs by surface tension-guided blade coating

2.1 Introduction

While the device performance of solution processed organic thin film transistors (OTFTs) has improved, it is necessary to investigate novel printing and processing techniques which produce devices with good electrical and mechanical properties while maintaining minimal variability and high device yield. Gravure, flexo, and inkjet printing have been previously used to fabricate fully printed devices [3]. While gravure and flexo are highly scalable and well suited for large areas, flexo printing typically results in rougher films and gravure printing often suffers from incomplete cylinder wiping [33]. On the other hand, inkjet printing is ideal for printing smooth, well-patterned thin films but is challenging to scale to rapid large area patterning due to the requirement for precisely positioned pL volume droplets [5]. Blade coating and slot die coating are alternative thin film deposition methods to inkjet printing that enable higher throughputs at the expense of inherently being a one-dimensional coating method. OTFTs have also been fabricated using a slot die printing technique known as zone-casting in which the solvent controllably evaporates at the tip of the meniscus, depositing high quality crystals with carrier mobilities as high as 11 cm^2/Vs, but with printing speeds limited to few hundreds of $\mu m/s$ [14, 20]. Furthermore, device reliability and performance is found to improve through the use of surface energy patterned (SEP) substrates to self-align inkjet-printed source drain electrodes[8] and pattern zone-casted semiconductor for partially printed devices [20, 90][6, 9, 10, 11]. In order to improve the large area scalability of high performance semiconductors, it is important to move away from the zone-casting regime [9, 20] and achieve a process in which the ink can be quickly deposited onto a substrate[2] and then controllably dry to form high quality patterned semiconductor thin films. While in the majority of studies reporting "solution-processed" TFTs comprise a printed or spin-coated semiconductor layer with photolithographically or thermally evaporated metal contacts[9, 11-13], far fewer reports have strived to achieve high quality printed contacts[2, 4, 8]. Lift-

off photolithographic processes and vacuum deposition of expensive metals such as gold must be replaced in order to move to more scalable, simpler, inexpensive and energy efficient OTFT fabrication. Additionally, the quality of the dielectric-semiconductor interface has a significant impact on mobility[14]. Despite the high mobility of fluoropolymer-semiconductor interfaces[15], few reports provide detail on steps to create a fully-printed gate stack with this dielectric[16, 17]. It is clear that good printability is a prerequisite for achieving high performance OTFTs. Poor printing control will result in topographical unevenness, which leads to high device-to-device variability and low yield. As a consequence, low device yields create barriers for circuit designs, application development and overall technology adoption. In this communication we combine blade coating at speeds of 1-2 cm/s on SEP plastic substrates and inkjet printing to achieve high yield and high performance fully-printed flexible OTFTs with minimal variability. Specifically, we demonstrate the benefit of using aqueous solutions of PEDOT:PSS and small molecule-polymer semiconductor blends[18] at blade coating speeds beyond zone casting. Furthermore, by the use of surface energy patterning, we report for the first time a fully-printed top gate device with a highly hydrophobic fluoropolymer gate dielectric.

This chapter overviews a novel printing technique of blade coating combined with surface energy patterning used for the fabrication of a large array of OTFTs [109]. The chapter also addresses the fabrication process flow and optimizations.

2.2 Surface Energy Patterning Using Doctor Blade Coating Technique

The doctor blade coating is a well-established popular thin-film coating technique over large areas. The method enables a precise and reliable linear deposition used both at the lab scale and roll-to-roll fabrication. Surface energy is critical for many of the coating applications. Figure 2.1a describes the surface energy which is the energy needed to create a new surface area. The surface energy of a solid-vapor surface defines the wetting of a liquid on the surface. Figure 2.1b depicts the summary of the process and the parameters to be tuned and optimized for a specific printing, especially in combination with the SEP process. A moving blade applies a shear force on the dispensed ink at the edge of the blade and uniformly spreads it on the substrate. In the coating process the blade height, speed, ink volume are crucial parameters requiring optimization to improve the printing. The surface energy pattering of a designed feature using blade coating is demonstrated in Figure 2.1c. This process is simple and could be scaled to manufacturing as it is compatible with large area processing and it does not require photolithography and lift-off. Previous work on slot die coating, which has similar mechanics to blade coating, on surface energy patterned surfaces has focused on patterning by the dewetting of the ink after coating a uniform liquid film over the substrate[23]. This style of printing deposits an excessive amount of ink on the substrate which uncontrollably segregates onto the hydrophilic regions, creating an

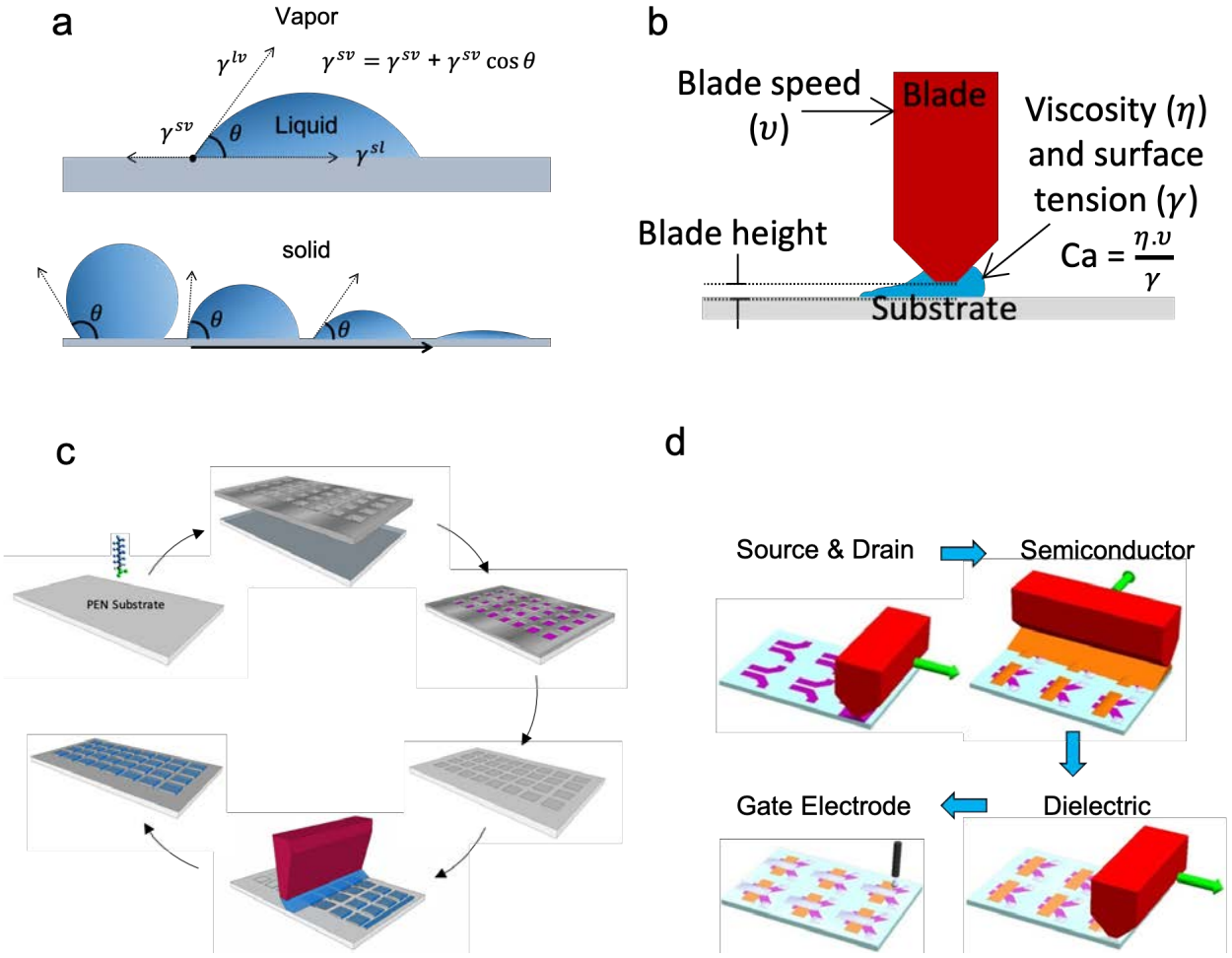

Figure 2.1: (a) The illustration of the relationship between the surface energy and contact angle. (b) The doctor blade coating process and the printing parameters. (c) Process flow of the surface energy patterning (SEP) using blade coating. (d) The printing steps of OTFTs with the bottom contact top gate structure using the SEP blade coating method for the source and drain and the semiconductor channel. The gate dielectric is blade coated, and the electrode contacts and the gate are inkjet-printed.

inhomogeneous array of features with poor pattern fidelity. As a first step in the process, a hydrophobic self-assembled monolayer (SAM) of fluoroalkylsilane (21.2 mNm^{-1}) is deposited on the plastic substrate before it is briefly exposed to low power oxygen plasma through a stainless steel stencil mask. The ink of the desired material is then dragged by a doctor blade, suspended above the substrate, and selectively wets the hydrophilic regions. We found that it is important to decrease the blade height below the critical thickness at which a wet film

of the ink spontaneously dewets from the substrate[24] and use an ink with a low capillary number. By doing so, the meniscus of the ink closely follows the blade and controllably wicks into patterned areas to enable highly uniform arrays. The device geometry used here is bottom-contact top-gate (BCTG) where the first layer patterned with high fidelity forms the source drain electrodes. The OTFT fabrication process flow is reported in Figure 2.1d showing the SEP blade-coated source drain electrodes, semiconductor, blanket blade-coated gate dielectric layer and inkjet-printed gate electrodes. Each printed layer of the device stack has its own optimal ink formulation and patterning process in order to optimize the printed OTFTs. The surface energy-driven patterning process of blade coating on SEP substrates requires an ink with a low capillary number (Equation 2.1) to ensure that viscous forces do not dominate the surface tension forces needed for self-assembled patterning. A slow blade coating speed (υ), a low ink viscosity (η) and high ink surface tension (γ) are desired for good patterning.

$$C_a = \frac{\eta.\upsilon}{\gamma} \tag{2.1}$$

Furthermore, the surface energy of the patterned area itself may be altered in order to affect the transfer of ink to the substrate. Printing viscous high molecular weight polymer solutions on unmodified plasma-defined patterns results in complete overflooding of the substrate. However, by treating the plasma-defined patterns with HMDS vapor much less ink transfers to the hydrophobic patterns, and viscous inks are able to be printed with high fidelity. It is found that faster coating speeds result in more ink transfer to the patterns which improve pattern fidelity and minimize variability.

Electrode Geometry Design and Optimization

The high surface tension and low viscosity of water make aqueous solutions of PEDOT:PSS ideal for reliable blade coating at higher speeds. Furthermore, PEDOT:PSS is an excellent choice for OTFT source drain electrodes because of its smooth film surface, inexpensiveness, good hole-injection properties, and sufficiently low resistivity. Blade-coated source drain electrodes printed using the as-received 0.8 wt.% PEDOT:PSS solution, shown in Figure 2.2a, exhibit poor pattern fidelity and shorted source and drain (SD) features. Adding 50 vol.% water to the original solution is sufficient to reduce the capillary number by 41% and improve pattern fidelity, as shown in Figure 2.2b. This ink modification changes the viscosity and surface tension of the original solution from 8 cP and 38 mNm^{-1} to 5 cP and 40 mNm^{-1}, respectively. The absence of coffee ring and other edge effects on the resulting SD features decreases the probability of ink dewetting from the electrodes. The coefficient of variance (CV) of 50 μm channel length (L) devices is 8% over 43 measured devices (100% yields) as shown in Figure 2.2c. A low CV is established as a result of the surface energy patterning, which acts as a driving force for self-assembly into the desired pattern, eliminating line edge roughness effects seen in other printing processes such as gravure and inkjet printing [29]. SD electrode resistance is on the order of approximately $10k\omega$, which is sufficiently low considering the I_{ON} values of our devices ($\leq 5\mu A$). Figure 2.2d shows SD printing yield for

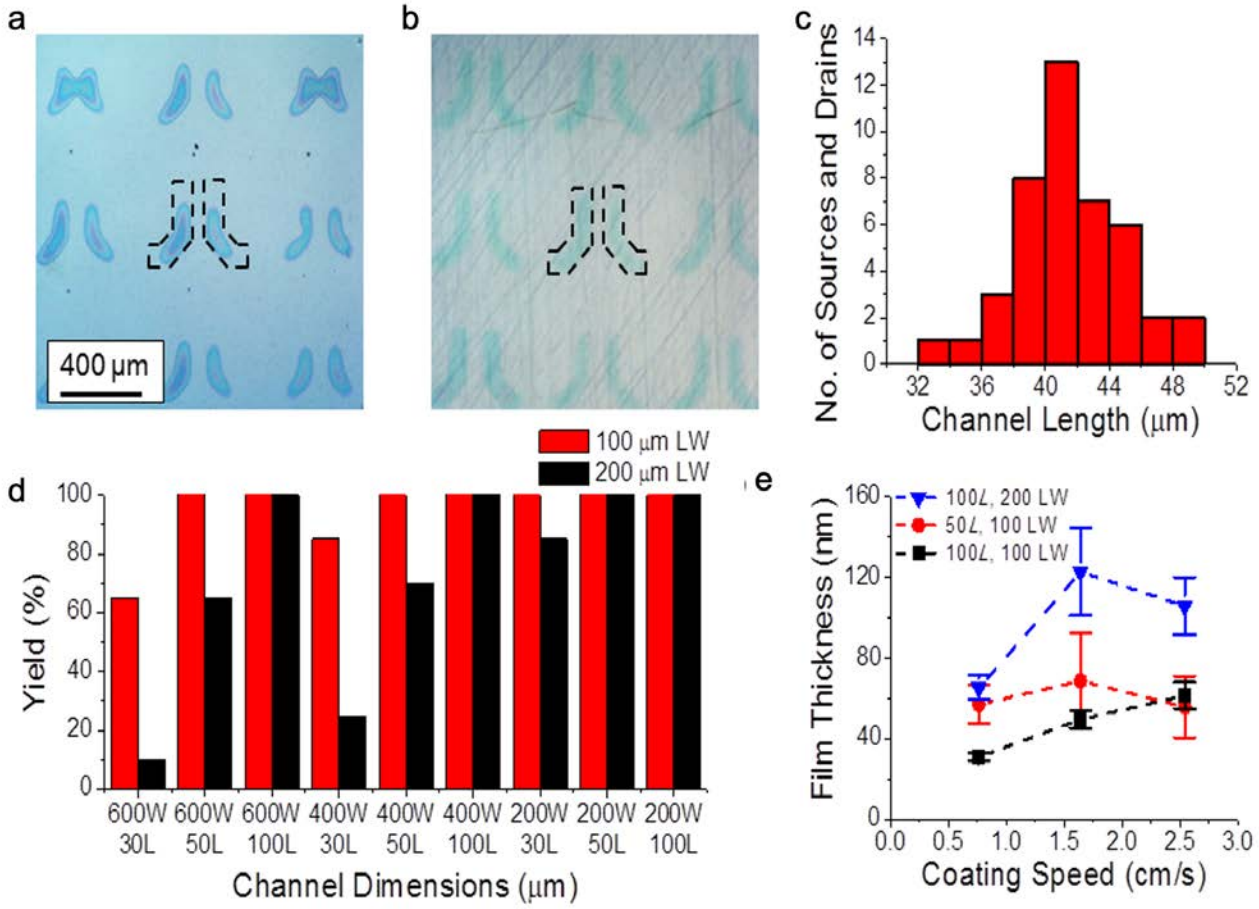

Figure 2.2: (a) Optical micrograph of SEP blade coated source and drain electrodes using the original (as received) PEDOT:PSS solution. (b) Optical micrograph of SEP blade coated source and drain electrodes using diluted PEDOT:PSS solution by adding 50 vol.% water. (c) Channel length variability for source drain electrodes in (b). (d) Source drain yield for several pattern geometries with varying line widths (LW) and TFT W/L for the same PEDOT:PSS solution in (b). (e) PEDOT:PSS film thickness at various coating speeds at 125 μm blade height for 600 μm W SD features of multiple L and LW.

rectangular-shaped SD electrodes of 200 μm and 100 μm line feature width and 200, 400 and 600 μm feature length. With this design TFTs with channel widths (W) of 200, 400 and 600 μm and channel lengths (L) of 30, 60 and 100 μm were printed using the optimized PEDOT:PSS ink formulation. The yield for 20 measured SD for each W and L is significantly higher for narrower feature line widths (LWs) as a consequence of less ink volume transfer to the hydrophilic patterns which reduces the likelihood of bridging between SD electrodes. For the 100 μm feature width series, all 50 and 100 μm L structures display 100% yield,

whereas only 30 μm L structures from the 200 μm W series display 100% yield. As such, the maximum reliable W/L is between 12 (600 μm/50 μm) and 13.3 (400 μm/30 μm) for 100 μm feature width. Figure 2.2e displays the deposited film thickness of PEDOT:PSS solution at several coating speeds for 600 μm W SD features of various L and LWs for a blade height of 125 μm above the substrate. 100 μm L and 100 μm LW SD feature thicknesses increase monotonically with minimal variability as coating speed increases. Decreasing the L to 50 μm for these features results in thicker films at lower speeds with more variability as a result of the close spacing of the features compared to the size of the well-controlled meniscus. The same trend is observed for scaled up features (100 μm L and 200 μm LW) albeit thicker films. In order to deposit uniform thin films it is important to ensure that 1) spacing between features is larger than their size and 2) the blade height is at most the same as the spacing between features.

Semiconductor Optimization

The semiconductor used in this work is a mixture of the high performance small molecule 2,8-difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene (diF TES ADT) with the low mobility amorphous polymer poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA). Low vapor pressure solvents curtail coffee ring effects and generally improve transistor performance[25], however the use of these solvents can result in dewetting from lower surface energy substrates as they evaporate[26]. The hydrophilic nature of oxygen plasma-treated patterns in our process favors good printability by enabling better ink wetting and decreases hole injection barrier from PEDOT:PSS electrodes[27]. However, small molecule organic semiconductors such as TIPS-Pentacene can exhibit poor OTFT performance when deposited on hydrophilic surfaces as a result of poor π-stacking[12]. As shown in Figure 3a despite the hydrophilic surface of the plasma-treated pattern, the low viscosity of small molecule solutions facilitates dewetting even for an additive amount of slow-evaporating tetralin (vapor pressure 0.37 $mmHg$) in mesitylene (vapor pressure 2.49 $mmHg$). This film formation results in rough semiconducting layers, which may cause device failures by introducing severe gate dielectric leakage. Figure 2.3a-c shows polarized microscopy pictures for several printed OTFTs arrays. While dewetting from edges is not an apparent issue when spin coating or blade coating very large patterns or non-patterned films, it becomes apparent that polymer additives are necessary in small molecule solutions in order to modify the rheological properties of the ink to prevent dewetting when printing beyond zone-casting speeds. As shown in Figure 3b, the printability and pattern fidelity is improved as 10% of PTAA is added to the semiconductor mixture resulting in more viscous ink. Further improvement on printability and film formation, shown in Figure 2.3c, was observed as the amount of PTAA is increased to 50% and the solvent is composed of 2:1 mesitylene:tetralin mixture. The quality of the printed semiconductor films was further characterized in OTFT structure. Our top gate devices were completed by a blade-coated layer of an amorphous fluoropolymer and thermally evaporated aluminum gate electrode as shown in Figure 2.4. Devices are measured in air as in previous OTFT reports to demonstrate stability[28]. Figure 2.2d shows the transfer

Semiconductor Formulation	Yield	$\mu_{sat}(cm^2/V.s)$	Log(I_{ON}/I_{OFF})	V_{th}(V)
9:1 mes:tet, 1:0 diF	10/16	0.39±0.13	4.93±0.23	0.78±0.65
9:1 mes:tet, 9:1 diF	16/16	0.47±0.18	4.2±0.11	-0.81±0.41
2:1 mes:tet, 1:1 diF	16/16	0.68±0.23	5.49±0.15	-0.22±0.37
2:1 mes:tet, 1:1 diF	13/16	0.1±0.09	1.07±0.2	1.11±4.37

Table 2.1: Yields and average saturation mobility, on-off ratio and threshold voltage ±standard deviation for devices with various diF (diF TES ADT:PTAA) and mesitylene:tetralin composition.

characteristics of the devices shown in Figure 2.3a-c with the array and device characteristics summarized in Table 2.1. Furthermore, Figure 2.3d shows that the substhreshold region for devices with PTAA exhibit an exponential behavior rather than a power law for the pure diF TES ADT film, which is indicative of a crystalline-behaving band structure[29] which has been attributed to the vertical segregation of diF TES ADT and PTAA[22]. By further increasing the polymer and tetralin concentration to 50 wt.% and 33 vol.%, respectively, the mobility improves to an average of 0.68 cm^2/Vs with values as high as 1.6 cm^2/Vs, which is comparable to values of 2 cm^2/Vs seen in optimal spin-coated devices[22]. Decreased subthreshold slope (Figure 2.3d) and negative threshold voltage shift (Table 2.1) are also accompanied by increasing the polymer and tetralin concentration. As a figure of comparison, Table 1 also reports that control spin-coated devices using the aforementioned semiconductor ink formulation on pentafluorothiophenol-treated Au SD have much worse performance and yield and more variability than printed devices. Slower evaporation rates result in slight dewetting off the topographically higher printed SD electrodes as shown in Figure 2.3c. Despite this problem, the same surface energy of the plasma-treated PEDOT:PSS contacts and underlying plastic substrate in the channel enables a continuous film morphology across the contacts and channel regions regardless of ink formulation as shown in Figure 2.3e-f. This continuity may enable high mobility short channel devices by preventing SD crystal nucleation seen with metallic bottom contacts[30]. The resulting continuity of morphology is similar to what is seen by the addition of nucleation promoters in OTFTs[26].

2.3 Gate Electrode

The fully printed OTFT process is finalized with printing the top gate electrode. A surface tension-guided process is also used to print the gate electrode on the fluoropolymer dielectric. Printing on fluoropolymer is particularly challenging because of its hydrophobicity. In previous reports interlayers were deposited in order to improve gate electrode printability and adhesion[18, 20]. Here, four corner dots of metallic nanoparticles are first inkjet-printed then sintered on the blade-coated dielectric. Next, more metallic nanoparticle ink is inkjet-printed over the dots as shown in Figure 2.5a. The surface area of the droplet reduces as the sol-

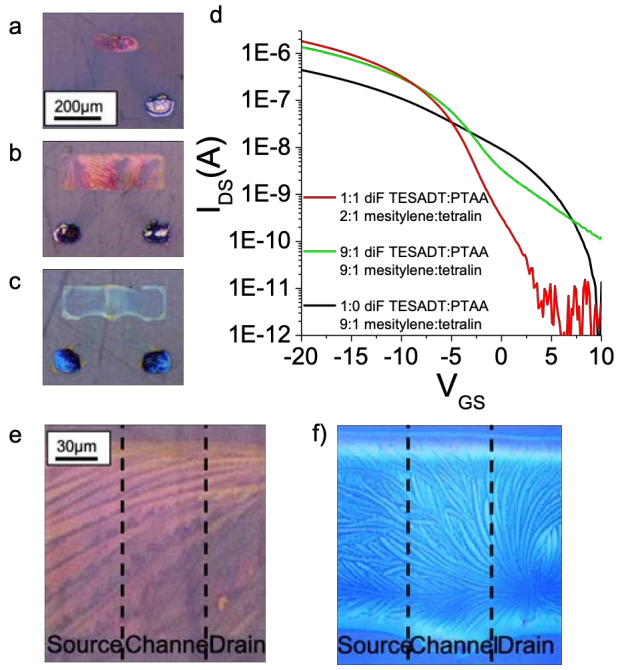

Figure 2.3: (a), (b), (c) Polarized optical microscopy of semiconductor films (prior to gate electrode thermal evaporation) printed from inks composed of 1:0 and 9:1, 9:1 and 9:1, 1:1 and 2:1 diF TES ADT:PTAA and mesitylene:tetralin, respectively.

vent evaporates during the sintering process until the corners become pinned to these dots. Additive concentrations of fluorosurfactant in the metallic nanoparticle ink facilitate self-alignment of the ink during solvent evaporation while minimizing the contact angle so as to prevent the droplet from breaking up. This method avoids the necessity of an interlayer[18], thus maintaining the original gate capacitance. In addition, this method is incredibly robust to the initial form of the large droplet since the silver ink eventually self-aligns to the corner dots with good surface adhesion. Such processing robustness substantially reduces the need for precise drop positioning and volume control, thus enabling higher throughput printing. Our data shows that 100% of 256 printed gate electrodes show great printing fidelity. The capacitance per unit area varies only 9% over a distance of 2.5 cm as a result of varying dielectric thickness with minimal variation in mobility. The device-to-device reproducibility confirms the robustness of our all-printed gate stack. All the printing techniques in Figure 2.1d are used to fabricate an all-printed OTFT array on plastic, as shown in Figure 2.5b, using the optimal semiconductor ink formulation from Table 2.1. Device yield is 96% for a 200 nm thick dielectric, the only failure mechanism being dielectric shorting. Figure 2.5c shows the statistical distribution of various device characteristics for this array. The mean mobility is reduced to 0.31 cm^2/Vs as shown in Figure 2.5c compared to 0.68 cm^2/Vs for the

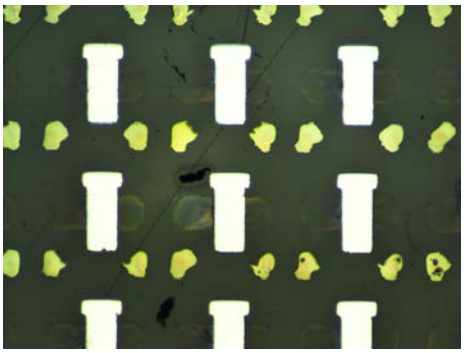

Figure 2.4: (a) Optical microscopy of OTFTs with evaporated aluminum gates.

devices with evaporated gate electrodes (Table 2.1). This result may originate from residual solvent left in the stack since the array is not placed in the high vacuum and temperature environment of a thermal evaporator. However, all-printed devices demonstrate less variability, with a mobility CV of only 20% compared to 34% for the high mobility devices in Table 1. These devices have mean on-off ratio over 105, which is enabled by fully overlapping the gate electrode over the channel width (preventing leakage current around the gate), and mean subthreshold slopes of 1.17 V/dec with a CV of only 11%. Furthermore, these devices have a mean threshold voltage of -0.07 V with a standard deviation of only 0.21 V, which is far less than that reported for spin-coated diF TES ADT-polymer blends[31]. The transfer and output characteristics of a typical device, as shown in Figure 2.5d and e respectively, demonstrate good square law behavior, high saturation output resistance, and no contact barrier. Mechanical testing reveals less than 20% decrease in on-current at a bending radius of $3mm$. Devices fail at 1.7 mm radius of curvature as a result of the substrate surface cracking. We also fabricated an array of OTFTs with aluminum-evaporated gates, as shown in Figure 2.4. The future chapters utilize the gate-evaporation process for device fabrication.

2.4 Conclusion

In summary, we have developed printing methods and optimized material formulations for the fabrication of fully printed and flexible OTFTs. In our work, all layers are processed from solution and deposited and patterned by printing. These printed devices exhibit high reliability, low variability, ideal electrical behavior and good mechanical properties. Blade coating on SEP plastic substrates combines the scalable properties of a roll-to-roll compatible printing technique used to fabricate high quality homogeneous thin films with the practicality of generating two-dimensional patterns. Using this technique, scalable self-aligned blade-coated SD electrodes with minimal variability can be very reliably printed. Furthermore, blending polymers with high performance small molecules enables more reliable printing with higher boiling point solvents, improved device performance and yields. Finally, surface

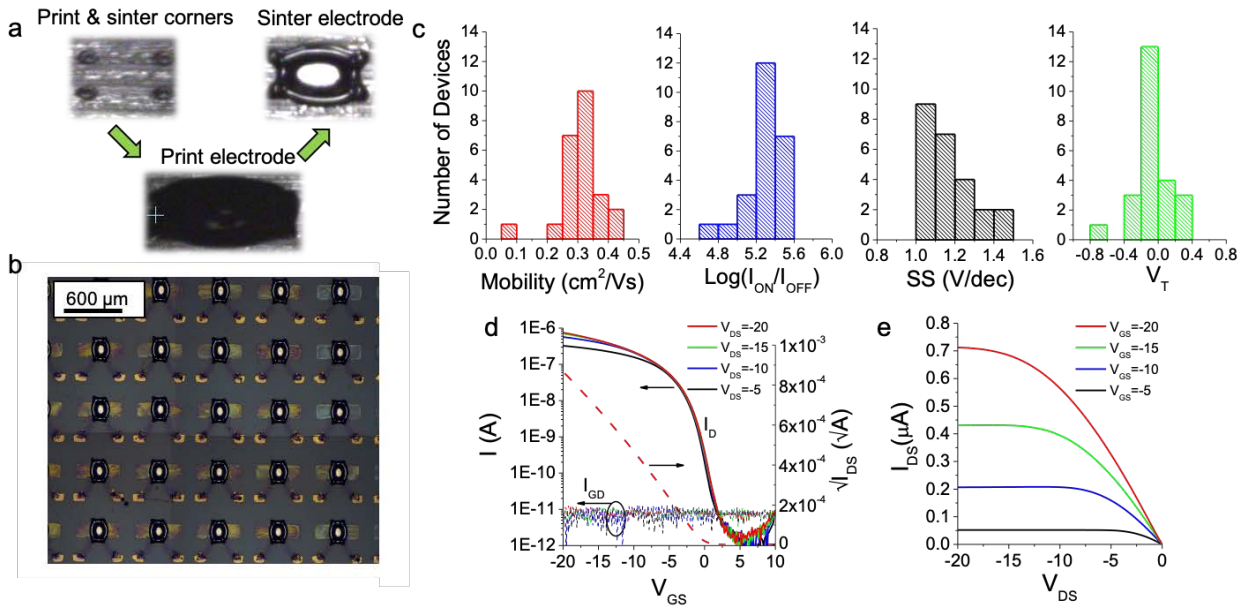

Figure 2.5: (a) Surface tension-guided inkjet printing of gate electrode on fluoropolymer dielectric. b) zoomed-out photograph of the all-printed array. (c) Statistical distribution of mobility, on/off ratio, subthreshold slope and threshold voltage. (d) Transfer characteristic of a typical all-printed device. (e) Output characteristic of a typical all-printed device.

tension is utilized to print the gate electrodes. Fully-printed devices on plastic demonstrate a high yield of 96% with good carrier mobility (average 0.31 cm^2/Vs), subthreshold swing (average 1.17 V/dec), high on-off ratio (average 2.2×10^5), zero threshold voltage, very low variability in all aspects of device performance and good mechanical robustness. The high reliability and good performance of these arrays was achieved by characterizing the reliability and yield of each layer on the OTFT stack. The high yields combined with high device performance indicate that SEP blade coating is a scalable and robust technique which can be used to design electronic circuits where device reliability is required and could lead to all-printed systems on plastic.

Chapter 3

Logic Circuits on Printed Flexible Electronics

3.1 Introduction

Organic electronics (OE) is an emerging technology with advantages of mechanical flexibility [66, 155], solution-processability, and high-throughput manufacturing at low temperatures on inexpensive and light-weight substrates such as plastic [13, 43], paper [64, 74], and fiber [41] in larger scales. While OE cannot yet rival high-performance silicon (Si)-based electronics, flexibility and low-cost mass production are some of the reasons for OE venturing into many new rising technologies not accessible by Si technology. Inorganic field-effect transistors (FET) have been the essential building blocks of any circuit design, such as amplifiers, digital logic units, and memory devices. OTFTs are not meant to substitute Si-based technology due to their drawbacks of high variability, lower speed, and performance. Some applications adopting OTFTs include identification (RFID) tags [7, 24, 128], electronics papers, large-area flexible displays, flexible circuits for wearable sensors [121]. OTFTs can be fabricated in large areas using solution-processed semiconductors (OSCs). Low-temperature solution processing approaches employ fast and inexpensive printing techniques with minimal material waste and thermally compatible with large area plastic substrates [57, 119]. However, Si-based technology applies high-vacuum and high-temperature deposition process along with complicated photolithographic patterning techniques for device fabrication and interconnection. Si electronics are not scalable and not proper for large-area applications due to costly fabrication steps [130]. Some technologies have utilized printing methodologies combined with photolithography to improve resolution and performance. For example, inkjet printing pattern resolution can be improved by adopting soft lithography to confine surface wettability [125]. Improvement of resolution is required for achieving higher speed and lower power circuitry. For applications where OTFT performance is sufficient, it is advantageous to avoid costly photolithographic methods. Fundamental logic and analog circuits, such as inverters and amplifiers have been fabricated using both complementary and

unipolar OTFTs for the designs. The fabrication of complementary OTFT inverter, which applies both n-type and p-type organic materials, adds further complications to fabrication steps. Besides, lower mobilities of n-types, in comparison with p-types, requires additional sizing modifications to match the output currents of the n-type and p-type transistors in an inverter gate. Compensation for low mobility requires the scale ratio change of n-type OTFTs to increase the current and match the performance of p-type devices. Use of mono-type designs, on the basis of p-type materials, reduces the fabrication complexity at the cost of increase in noise margins and static consumption power [48]. In general, the performance of circuits should be tuned to meet the specifications of application in mind. This chapter presents printed mono-type logic designs using fast printing methods for the fabrication of a large array of devices and interconnections in one printing step.

At first, this chapter investigates a method for scale ratio tuning of devices with the same fabrication process described in the previous chapter. Then the focus is on the interconnection of devices to fabrication logic circuits.

3.2 Fabrication of Array of OTFTs With Various Scale Ratio

Printing of OTFTs employs surface energy patterning (SEP) technique combined with self-assembled monolayer (SAM) of fluroalkylsilane on PEN (polyethylene naphthalate) substrate to decrease the surface energy [109, 117]. In the SEP technique, a mask with desired patterns is placed on the substrate with the SAM layer followed by oxygen plasma-treating to create hydrophilic/hydrophobic regions. Figure 3.1a depicts fabrication of the array of OTFTs. The hydrophilic source and drain (SD) electrodes and rectangular reservoir are defined using a stainless still mask with the SD patterns. A blade drags PEDOT:PSS, dispersed on the reservoir, from the top to the bottom of the substrate along the y-axis at an optimum blade height and speed. The ink only remains in the hydrophilic regions, which form the SD electrodes. The rectangular 2mm×2mm bumps are inkjet-printed on the electrodes. The mask with two scale ratios (W/L) of 450μm/50μm and 150μm/50μm is used for SEP of channels. Blade coating of channels is done along the x-axis, perpendicular to the course of the SD printing. The change of direction results in higher mobilities due to the formation of crystal grains along the channel from source to drain. The dielectric is blanket coated over the whole array. The gates are evaporated as shown in Figure 3.1b. Figure 3.1c shows an optical microscopy of a blade coated SD. The electrodes have 550 μm of width and 50 μm of spacing which defines the channel length. The electrode geometry parameters such as linewidth, channel length (L), and width (W) are optimized to reduce the shorting of SDs and increase device yield in the array. To illustrate this, electrodes with larger linewidth and area, contain more ink which increases the possibility of ink absorption and shorting. Smaller channel lengths below 50 μm also increase the chance of shorting. There is an optimum electrode linewidth (LW), L, and W which results in 100% yield. Due to the

etching variability, any increase in W after the optimum point causes shorting the channel. The ink from the source to the drain bridge and the device gets shorted. In order to vary the W/L ratios and form rectangular channels on the electrodes, the SD width is increased to its possible maximum optimized W. The electrodes have W of 550 μm and 100 μm safety margin which can result in maximum W of 450μm. Figure 3.1d and 3.1e demonstrate the devices with two W/L of 150 μm/50 μm and 450 μm/50 μm. The cross-section and top view of the device are shown in Figure 3.1f and Figure 3.1g.

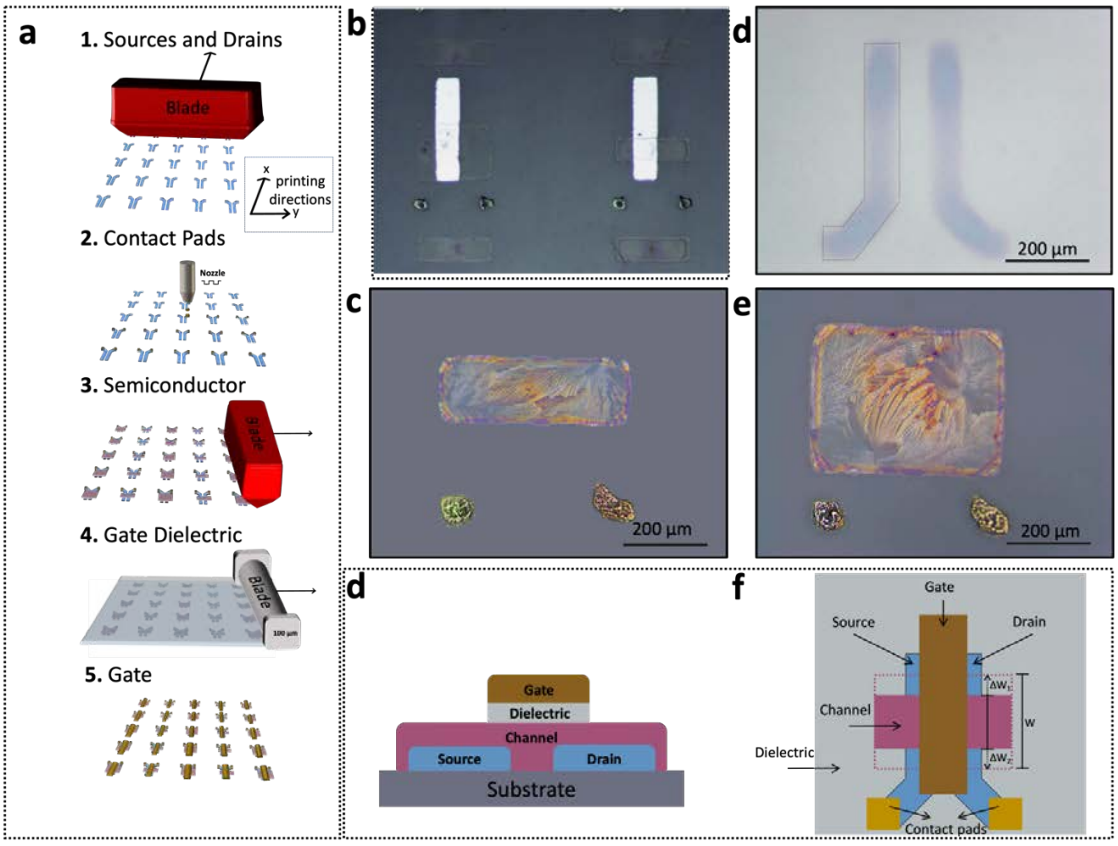

Figure 3.1: (a) The fabrication and printing processes of large array of organic thin film transistors (OTFT) adopting self-assembled energy patterning (SEP) blade-coating of sources and drains, inkjet printing of contacts, SEP blade-coating of semiconductor channels, blanket blade coating of the gate dielectric, and evaporation of gate. Optical microscopy of (b) evaporated gate, (c) PEDOT:PSS source and drain, d) 1:1 dif:TES:ADT to PTAA semiconductor channel with width (W) of 150 μm and e) W of 450 μm. (f) The cross-section and (g) top view of the top gate OTFT with varying W.

DC characterization of fifty OTFTs with W/L of 450 μm/50μm and 150 μm/50μm chosen along the array is done in air by deriving output characterisation plot for each device. The statistical distribution of on-off ratio, saturation mobility (μ_{sat}), threshold voltage (V_{th}), and subthreshold swing (SS) of twenty five OTFTs with W/L of 150 μm/50μm is shown and studied in Figure 3.2a. For these 25 devices, the mean of on-off ratio is 4.88 with standard deviation (SD) of 0.68, the average μ_{sat} of 0.4 $cm^2/V.S$ and SD of 0.14, and average SS of 1.2 V/dec, and mean V_{th} of -0.4 V and SD of 0.64. The output and transfer characteristics of an OTFT with the mentioned W/L are shown in Figure 3.2c and 2d respectively. The OTFT behavior is explained and studied considering the square-law theory. V_{th} is measured by adopting the quasi-universal method consisting of the transfer characteristics plotted as $\sqrt{I_D}$ vs. V_G. The V_{th} is the extrapolation of the linear fit to this plot in the linear range of the discussed plot to I_D of 0 [101]. The saturation mobility is extracted using the $\sqrt{(I_D)}$ vs. V_G as following:

$$\mu = \frac{2L}{WC_i}(\frac{d\sqrt{I_D}}{dV_{GS}})^2 \tag{3.1}$$

For V_{GS} smaller than the V_{th}, there is a small flow of current in the subthreshold region which is orders of magnitude smaller than the current in the inversion layer. The transfer characteristics plot shows an exponential dependence of I_D on the gate voltage below the threshold voltage. SS, the inverse of the slope of the $logI_D$ vs. V_{GS}, can be used to delineate the subthreshold behavior. Figure 3.2d depicts the statistical distribution of on-off ratio, μ_{sat}, V_{th}, and SS. The twenty five devices show the mean on-off ratio of 5.19 and SD of 0.44, average μ_{sat} of 0.89 $cm^2/V.s$ with SD of 0.25, mean V_{th} of 0.54 V with SD of 0.37, and average SS of 1.11 with SD of 0.29. Figure 3.2e and 3.2f show the output and transfer characteristics of the OTFT with W of 450 μm. The performance of OTFTs with W of 150 μm and 450 μm, imply good square-law, low I_{off} current, and high output resistance, and no contact barrier. By increase of W, average mobility has been improved from 0.4 to 0.89 $cm^2/V.s$. This mobility enhancement is attributed to the larger grain boundary formation along with the direction of the carriers in the channel from source to drain. Screen printing method is compatible with the interconnection of discrete devices as the silver ink solvent is insoluble in amorphous fluoropolymer (AF), and the device performance is retained in the array after printing and annealing step. Figure 3.3a depicts the photograph of several logic gates in an array of OTFTs with screen printed interconnects. Before printing the silver ink, the surface wettability of AF layer is improved by applying few seconds of air plasma. Screen printing contains two main parts of flood step and squeegee step. The screen mask is formed of a fine mesh and an emulsion coating to prevent the ink transfer in the non-patterned sections. At first, the flood-blade uniformly spreads the ink on the designed mask with a light flood. Then, the squeegee blade forces the ink into the openings transferring the interconnection patterns on the beneath substrate aligned to the mask [47]. The screen-printing process is summarized in Figure 3.3b. The printing parameters such as squeegee/flood pressure and snap-off distance-the gap between the substrate and the intact mask-are optimized to prevent device performance degradation. High applied pressure on

the array can increase the possibility of shorting the devices and gate leakage. Figure 3.3c and 4.3d depict the optical microscopy and circuit diagram of an enhancement-load inverter accordingly. It is formed from two OTFTs with one as a drive transistor whose gate is the input voltage (V_{In}) and the other as a diode-connected transistor, whose gate is connected to the drain and supply voltage V_{DD}. In the diode connected load, the gate voltage (V_G) is the same as the drain voltage, so $\mid V_{DS} \mid > \mid V_{GS} \mid - \mid V_{th} \mid$ always holds and the device operates in the saturation regime and acts as a resistive load. When V_{in} is larger than V_{th}, the drive transistor is off so V_{Out} is pulled up to the V_{DD} supply voltage. As V_{In} decreases and becomes more negative, the drive transistor starts conducting getting into the saturation region and the V_{Out} pulls down to the ground. The gain, the slope of the voltage transfer curve, of the inverter is as calculated in equation 3.3. The voltage transfer characteristics and the gain of two inverters with two different W_{Drive}/L_{Drive} of 450 μm/50 μm and 150 μm/50 μm are compared in Figure 3.3e and 3.3f. With increasing the W_{Drive}, the gain of the inverter is increased from 1.78 to 4.35. The logic circuits should be designed in a way to switch properly and tolerate noisy conditions [15]. Logic gates may encounter noise voltages emanated from different parts of the circuit. This arises the noise immunity term which is quantified with noise margin (NM). Figure 3.3g and 4.3h illustrate the NMH (high level noise margin) and NML (low level noise margin) results associated with the discussed inverters with two various W_{Drive}. The NM is defined with two critical voltage points at the gain of -1. When the input voltage is at logic 0 the maximum amount of voltage that is still interpreted as logic 0 is VIH. For output at logic 0, the maximum voltage to be considered a logic 0 is VOH. NMH is the absolute difference between these two voltages. For input and output voltages to be recognized as logic 1, the minimum voltages are VIL and VOL accordingly, whose difference is defined as NML. The inverter with W_{Drive} of 150 μm is showing NMH and NML of 1.2 V, and 6.7 V. With an increase of W_{Drive} to 450 μm, NMH and NML are 0.16 V and 13.3 V. Figure 3.4a shows the gain and voltage transfer characteristics of enhancement-load inverter under four different V_D biasing conditions of -5V, -10V, -15V, and -20V. The performance of printed logic circuits is summarized in Figure 3.4b-i. The top plot of each section indicates one of the test points for which the logic gate is biased at a certain operating point and the voltage is measured when the output settles to its final value. The bottom plot is the voltage transfer curve when one of the inputs is swept from -20V to 20V while the other inputs are biased at a certain voltage. Figure 3.4b shows a logic circuit for two-input NAND gate. When both inputs VA and VB are high and the devices are on, the output node is pulled down to the ground which is "0" state. When either of the inputs or both are low, the output node is tied to V_{DD} through the pull-up device as there is no current path to the ground via the stacked OTFTs. The performance of a three-input NAND gate is presented in figure 3.4c. With all inputs V_A , V_B, and V_C at high state "1" the output node is pulled down to ground. When at least one of the inputs is "0", there is no current path to the ground and the output is at high state "1". Figure 3.4d and 4.4e demonstrate a two-input and three-input AND gate logic respectively. The AND gate is a compound of a NAND gate followed by an inverter. The output of the NAND gate logic as described before is inverted to the opposite state. When all of the inputs are high, the output is high and when one of

the inputs is low the output is pulled down to the ground. A three-input NOR gate logic is made of three OTFTs in parallel and stacked with a diode-connected OTFT as depicted in Figure 3.4f. When all of the OTFTs are off, the output node is pulled up to state "1". When one of the inputs are high, there is a pathway for the current to the ground and the output node is pulled down. Figure 3.4g presents an OR logic in which the output of a NOR gate is inverted. The output is pulled up when all of the inputs are low. For the rest of the cases the output is at high state. A XOR gate is presented in Figure 3.4h. When V_A is high and V_B low, OTFT2 is off and OTFT1 is on resulting in current flowing through the device and setting the first stage output to "0" and then gets inverted by the following inverter and V_C becomes "1". The same scenario holds with the case of low V_A and high V_B. With the inputs both low or high, the devices OTFT1 and OTFT2 are off and the output of the first stage is pulled up and then inverted to state "0". The XNOR logic gate is described in Figure 3.4i. For the V_C output to be "0", OTFT3 should always be on along with at least one of the OTFT4 or OTFT5 at the on state. For OTFT3 to be on, the output of the first stage should be high, which happens when either of V_A or V_B is low. On the other hand, at least one of the V_A or V_B should be high for the parallel combination of OTFT4-5 to be on. For both of the conditions to be satisfied, V_A and V_B should have opposite states. In any other case, the stacked combination of the second stage does not have any path to the ground leaving the output to be high.

3.3 Conclusion

We are demonstrating fundamental unipolar logic circuits by employing screen printing for interconnection of OTFTs in a large array. The scale ratio of devices is modulated by changing the channel island on the source and drain electrodes. There are two scale ratios of 450μm/50μm and 150μm/50μm, with average mobilities of 0.4 and 0.89 $cm^2/V.s$a accordingly. The increase of mobility is due to the formation of larger crystal grains from the source to the drain electrode along the channel. Increasing the drive transistor scale ratio shows improvement in the dc gain and noise margin of the enhancement-load inverter. The other printed circuit logics such as NAND, AND, NOR, OR, XOR, and XNOR perform as expected as shown in the transfer curves.

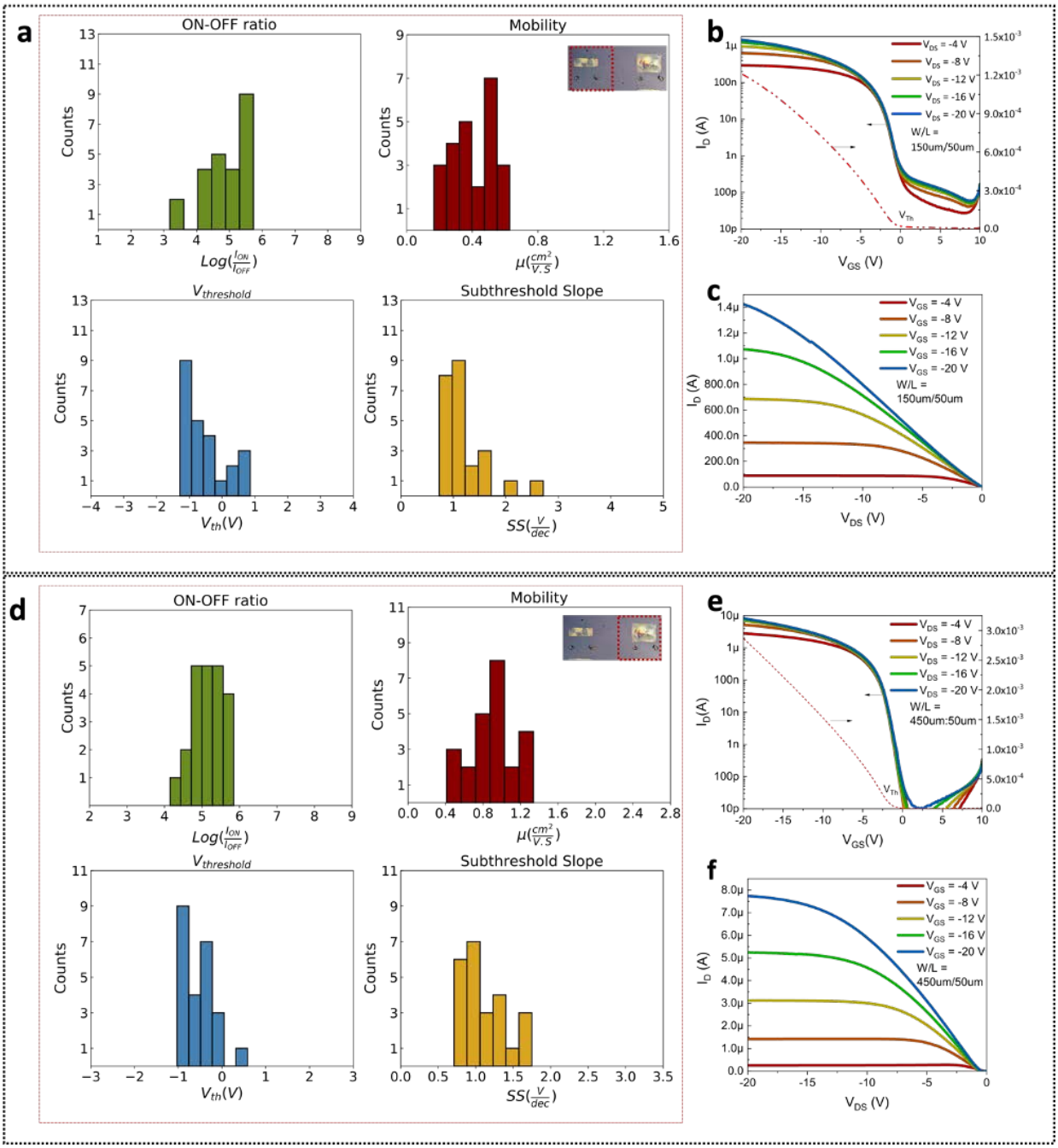

Figure 3.2: (a) Statistical distribution of on-off ratio, mobility, threshold voltage, and subthreshold slope, (b) transfer characteristics, and (c) output characteristics of an OTFT with scale ratio of 150μm/50μm. d) The statistical distribution of on/off ratio, mobility, threshold voltage, and subthreshold swing, e) transfer characteristics, and f) output characteristics of an OTFT with scale ratio of 450μm/50μm. The two OTFTs are adjacent to each other.

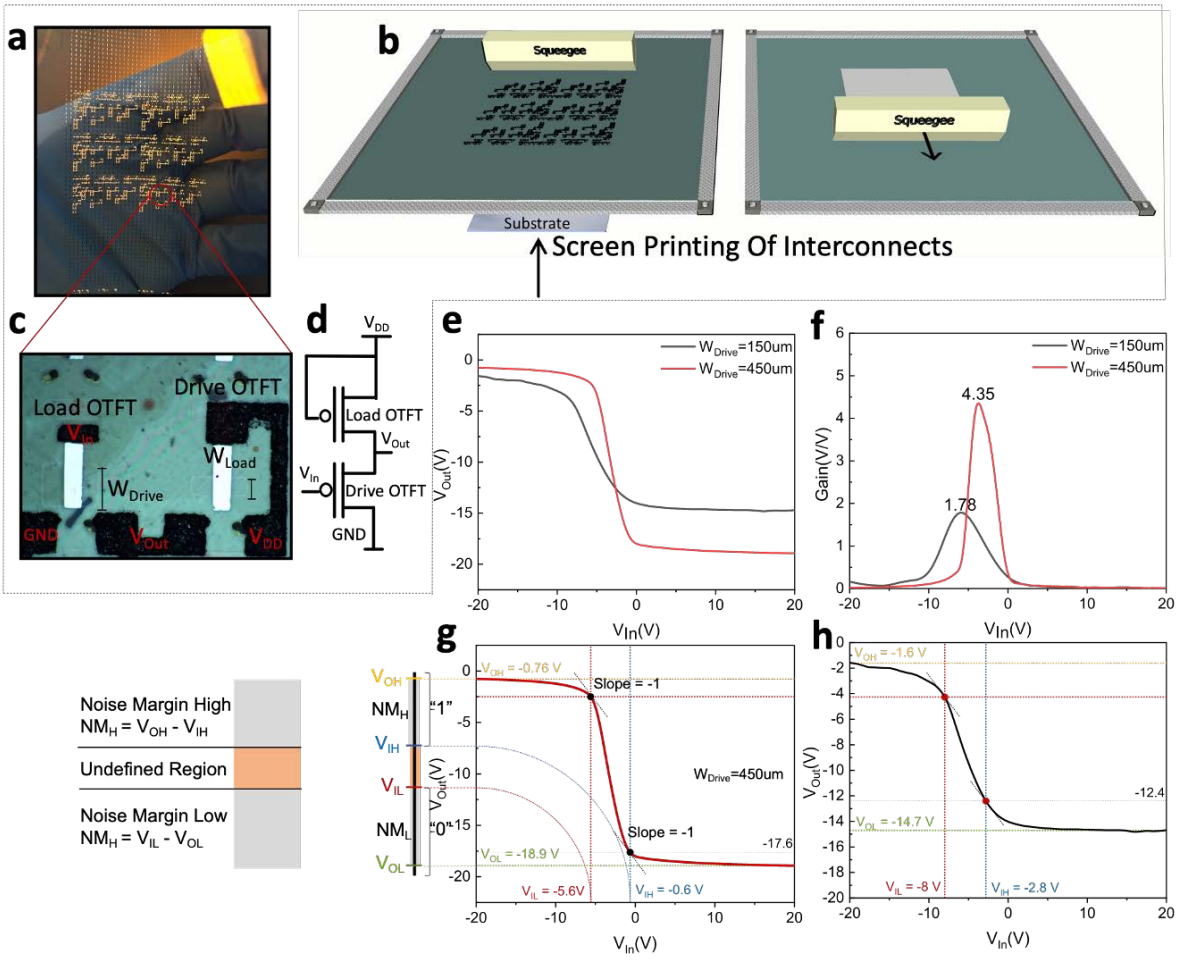

Figure 3.3: (a) Photograph of an array of OTFTs with screen-printed interconnection layer on top of devices. (b) Screen printing process of interconnection layer. The substrate is placed beneath the screen with a distance and the squeegee pushes the silver ink in the openings to transfer the interconnection layer on the array. (c) Optical micrograph and (d) circuit configuration of an enhancement-load inverter with drive OTFT scale ratio of 450μm/50μm and load OTFT scale ratio of 150μm/50μm. Circuit configuration of an enhancement-load inverter. Comparison of e) voltage transfer characteristics, (f) gain curves ,and (g-h) noise margin of two inverters with various WDrive of 450 μm and 150 μm.

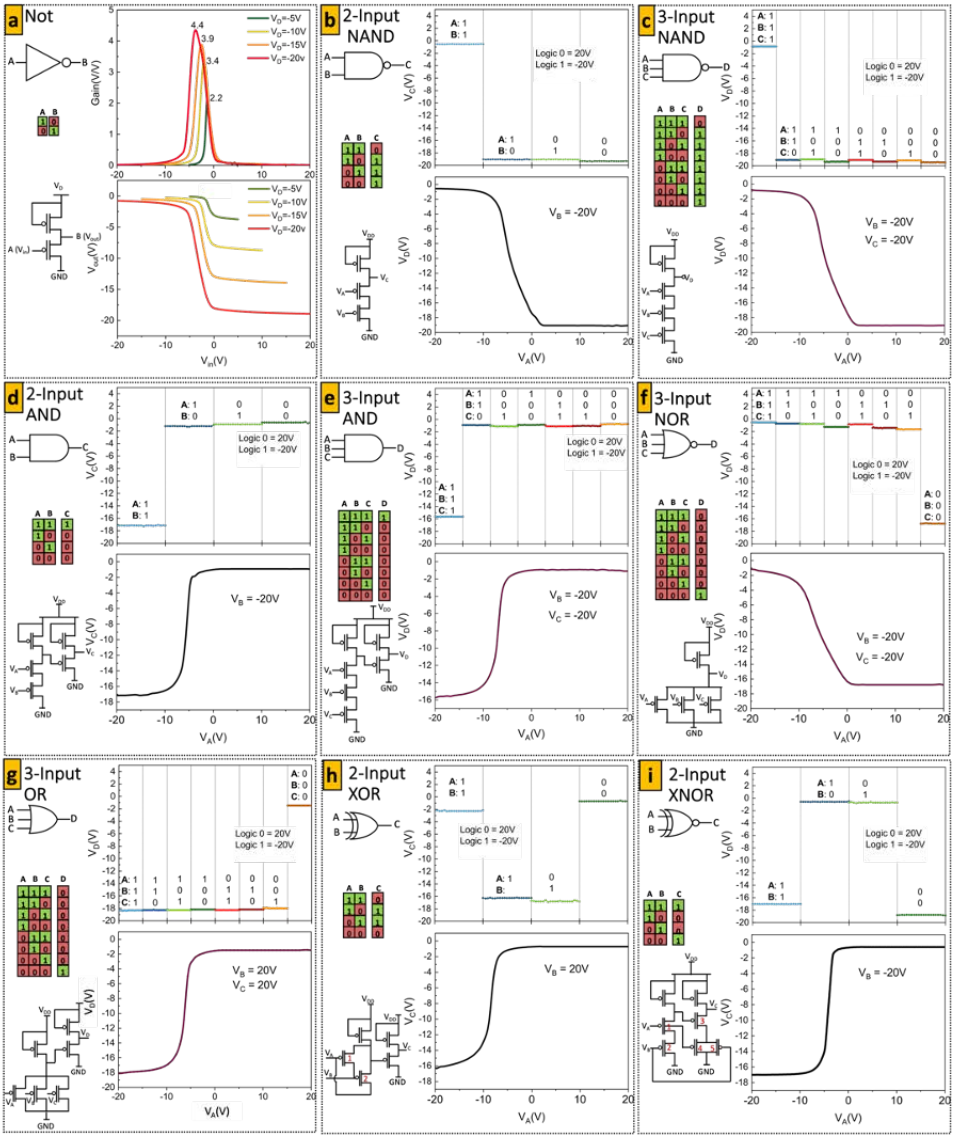

Figure 3.4: The performance of various printed logic circuits. (a) The gain and transfer function characteristics plots of the inverter are presented with V_{In} swept from -20 V to 20V, V_{DD} biased at various voltages of -5 V, -10 V, -15 V, and -20 V, drive transistor scale ratio $W_Drive/L_Drive = 450\mu m/50\mu m$, and diode connected load transistor scale ratio of $W_Load/L_Load = 150\mu m/50\mu m$. The performance of other circuit configurations is shown and summarized in figure (b-i). The top plot shows the performance of the logic gate biased at a certain operation point when output is settled to its final value. The bottom plot is the transfer function, V_Out vs. V_In, with V_DD biased at -20 V, one of the input voltages swept from -20V to 20V, and the other input voltages biased at a specific voltage mentioned on the plot. The performance of (b) two-input NAND, (c) three-input NAND, (d) two-input AND, (e) three-input AND, f) three-input NOR, g) three-input OR, (h) two-input XOR, and i) two-input XNOR.

Chapter 4

Printed Flexible Organic Transistors with Tunable Aspect Ratios

4.1 Introduction

Over the past several years, many large-area printed electronics have demonstrated significant benefit from their utilization of organic thin film transistors (OTFTs) where inexpensive and fast fabrication techniques using solution processing materials have shown great promise [37, 42, 124]. Crystalline silicon technology can be challenging to apply in fabrication and distribution of electronics over a large area, mainly due to high processing and manufacturing cost per unit area in addition to the high cost of single crystal wafer substrates. Low temperature simplified solution processing techniques minimizes materials waste and has the potential to replace some expensive procedures. This has made OTFT technology an increasing constituent of large-area electronics, both at device and integrated circuits level [24, 32, 120, 124, 166]. Solution-processed small-molecule organic semiconductors (SOCs) are successfully used as active layers of OTFTs, which find applications in active-matrix electronic-paper displays, OLED displays, circuits for radiofrequency identification RFID, and simple logic circuits [16, 24, 131, 134]. The recent advancements of solution-processed SOCs used in TFTs shows device performance reaching that of amorphous Si and solution-processed metal oxides. This high performance makes SOCs p-type OTFTs a strong candidate for several future CMOS applications [25, 70, 108]. Modulation of scale ratio of devices in a large array is one of the important parameters that governs circuit design. While most printing techniques can provide faster fabrication processes, the rapid on-demand modulation of W/L scale ratio in large array of devices remains as a challenge and a topic to investigate; especially for the myriad of specified circuit designs and application requirements. For instance, the tuning of the gain in each stage of an amplifier [14, 85, 89] or logic circuits [120] requires the modulation of OTFT W/L ratio. These configuration changes can be challenging, costly and time-consuming for common electrode printing techniques, such as screen printing and gravure printing [28, 33, 61]. These conventional mask-based

approaches utilize a fixed pattern transfer that requires a full re-design for every new device structure [72, 113]. Inkjet printing on the other hand is a nonimpact digital prototyping method that provides instant change of patterns [104, 126]. This elimination of mask can reduce the processing costs especially for larger scale production [135]. However, throughput of inkjet printing can become a limiting factor, specially when depositing over large area [125]. Interdigitated source and drain structure have been used in previous reports as a method to modify W/L ratio for a specific circuit design [14, 66, 119, 151]. The channel width (W) is modulated by changing the finger count. Meanwhile, channel length (L) is the smallest space between source and drain electrodes and the resolution is associated to the printing technique. Low switching speed is one of the drawbacks of printed OTFTs compared to conventional Si technology, which can result from a number of factors such as mobility, dielectric layer thickness, and channel length. Achieving channel lengths smaller than 10 um while maintaining high device to device yield is very challenging with printing techniques, especially for low-viscosity inks. The solution found to overcome this challenge is to utilize a combination of patterning techniques including the combination of conventional photolithography and direct-write printing techniques [65]. In parallel, there has been an interest to develop methods to decrease the source and drain electrode geometry and channel length using many printing methods. Interdigitated SD are typically used in electronics to increase channel width while maintain small channel lengths, resulting in higher W/L ratios. There are few reports on printed interdigitated electrodes, and all of them are achieved with a combination of photolithographic and printing methods [70, 134, 137]. This chapter shows a method for on demand change of W/L ratio along the array.

This chapter describes the electrode geometry optimization for surface energy patterned (SEP) blade coating in order to achieve 50 um channel length using interdigitated SD geometry with 100% yield using low-viscosity PEDOT:PSS solution. In addition, the method describes how different pairs of electrodes can be selected by printing in order to modulate, on demand, the W/L ratios of a large array of devices. This method uses only direct-write printing techniques and results in high yields and a range of W/L ratio values which is needed for device integration into circuits.

Inkjet Printing Process

Inkjet printing is a printing technique widely used for many printed electronics applications. The technique is appealing due to its additive printing, independence to a pre-manufactured mask, and noncontact approach, which applies no force onto the substrate and previous layers. As opposed to conventional printing, digital printing facilitates the precise positioning of a liquid droplet on the substrate based on the information at each binary unit of the designed pattern. Other printing techniques require the change of the masters and setup process for the change of the designs at the cost of investment and time. While the throughput of inkjet printing is limited compared to high-end conventional printing, the technique has the benefit of versatility and adaptability to many electronic applications [11]. In the inkjet printing process, a specified amount of ink in a chamber is ejected to a nozzle through

a quasi-adiabatic decrease of chamber volume as a result of a piezoelectric action. The chamber filled with the ink gets contracted in response to an applied voltage. A sudden reduction of chamber ink volume generates a shockwave in ink, which causes a drop to eject from the nozzle and falls on the substrate under the gravity of gravity and air resistance until impingement on the substrate and spread under momentum required in motion. The schematic of an inkjet printing process with a piezoelectric print head is shown in Figure 4.1a. A typical waveform applied to the print head to create droplets is shown in Figure 4.1b. Many types of waveforms can be applied to the head for droplet generation. The magnitude and the profile of the waveform modified based on the nozzle size and the ink rheology, the droplet size, and the required velocity [11]. The flow of the ink on the substrate depends on the surface energy. The aid of plasma treatment can modify the surface energy. Two commonly used plasma treatment include CF_4 and O_2 for making the surface hydrophobic and hydrophobic accordingly. Figure 4.1c is an illustration of a substrate exposed to an oxygen plasma to increase the surface energy of the substrate. The improvement in the shape of an inkjet-printed pattern is shown and compared in Figure 4.1 d-e. Exposure to 5 seconds of plasma has improved the inkjet-printed pattern, as shown in Figure 4.2e. After depositing on the substrate, the final pattern forms by evaporation of the ink solvent. The formed shape strongly depends on the ink viscosity, a function of the molar mass of the ink [122, 136].

Discrete Interdigitated Fabrication Process

OTFT arrays are fabricated using a combination of surface energy patterning (SEP), blade coating and inkjet printing [109]. A hydrophobic self-assembled monolayer (SAM), fluroalkyl-silane, is deposited on the plastic substrate and patterned by etching the monolayer through a stainless-steel mask with low energy plasma. The complete process flow used for fabrication of discrete devices is given in Figure 4.2. The stainless-steel mask defines hydrophilic regions which will form the source and drain (SD) electrodes. We use blade coating to deposit PEDOT:PSS as a conducting material for SD. Eleven interdigitated electrodes are printed in an area of 1700×980 μm^2 with a separation of 50 μm, shown in Figure 4.3a. The gap between electrodes defines the channel length of a given OTFT in the array. Subsequently inkjet printing is utilized to print Ag nanoparticles onto contact pads of each electrode. It is at this stage in the fabrication that a given width transistor can be defined. Printing Ag contacts on all of eleven electrodes would result into channel width (W) of 2500 μm with the channel length (L) set by the 50 μm distance between electrodes. Blade coating is used to deposit semiconductor and the gate dielectric layer over the entire area, covering all of the eleven electrodes. The optical microscopy of the channel along with the previous steps is shown in Figure 4.3b. While the gate dielectric, 120 nm thick, fully covers the channel it leaves the ink jetted Ag contacts exposed. These contacts are typically 300 nm thick and are protruding over the dielectric layer. At the final stage of device fabrication, the gate electrode is deposited by thermal evaporation together with parallel metal bars that connect the selected SD electrodes (electrodes with printed Ag contact pads). The top view

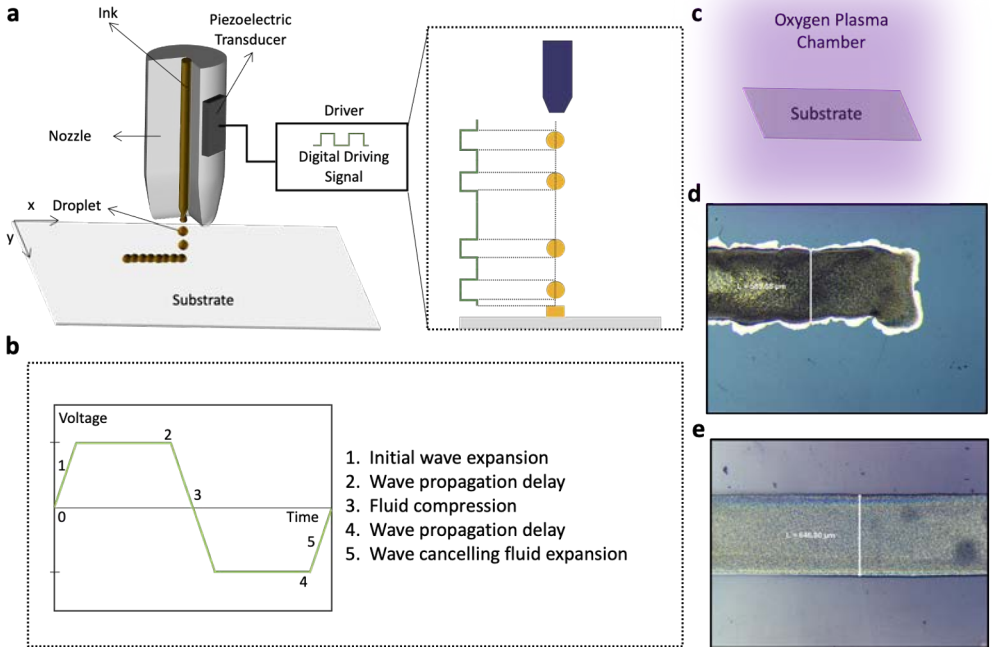

Figure 4.1: (a) Structure of drop-on-demand inkjet printing process with a piezoelectric print head. The contractions in response to an applied voltage to the chamber results in a sudden change of the volume of ink, which forms wave shocks and ejection of droplets on the substrate surface. (b) A typical waveform with brief descriptions of each segment of the waveform. (c) Illustration of a substrate in the plasma chamber. Plasma treatment modulates the surface energy of the substrate and wettability of the ink. Comparison of two silver (Ag) inkjet-printed rectangular pattern (d) without exposure to plasma and (e) after five seconds of oxygen plasma, increasing the surface energy and improving the wettability of the ink on the substrate.

schematic and cross-section of the interdigitated device structure are shown in Figure 4.3c and 3.3d. The optical micrograph of a portion of an array of printed OTFTs with different W/L ratios is shown in Figure 4.3e.

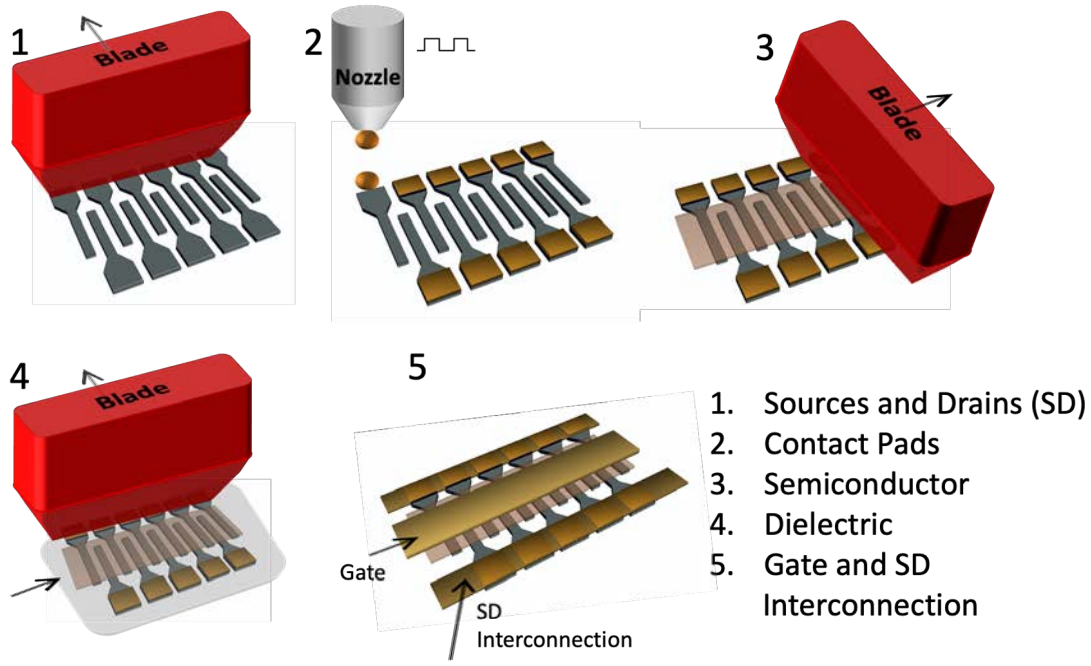

Figure 4.2: The printing and fabrication steps for organic thin film transistors using self-assembled energy patterning blade coating for discrete source-drains and semiconductor channels, inkjet printing contacts, blanket coating a dielectric layer, and gate and finger-connection evaporation.

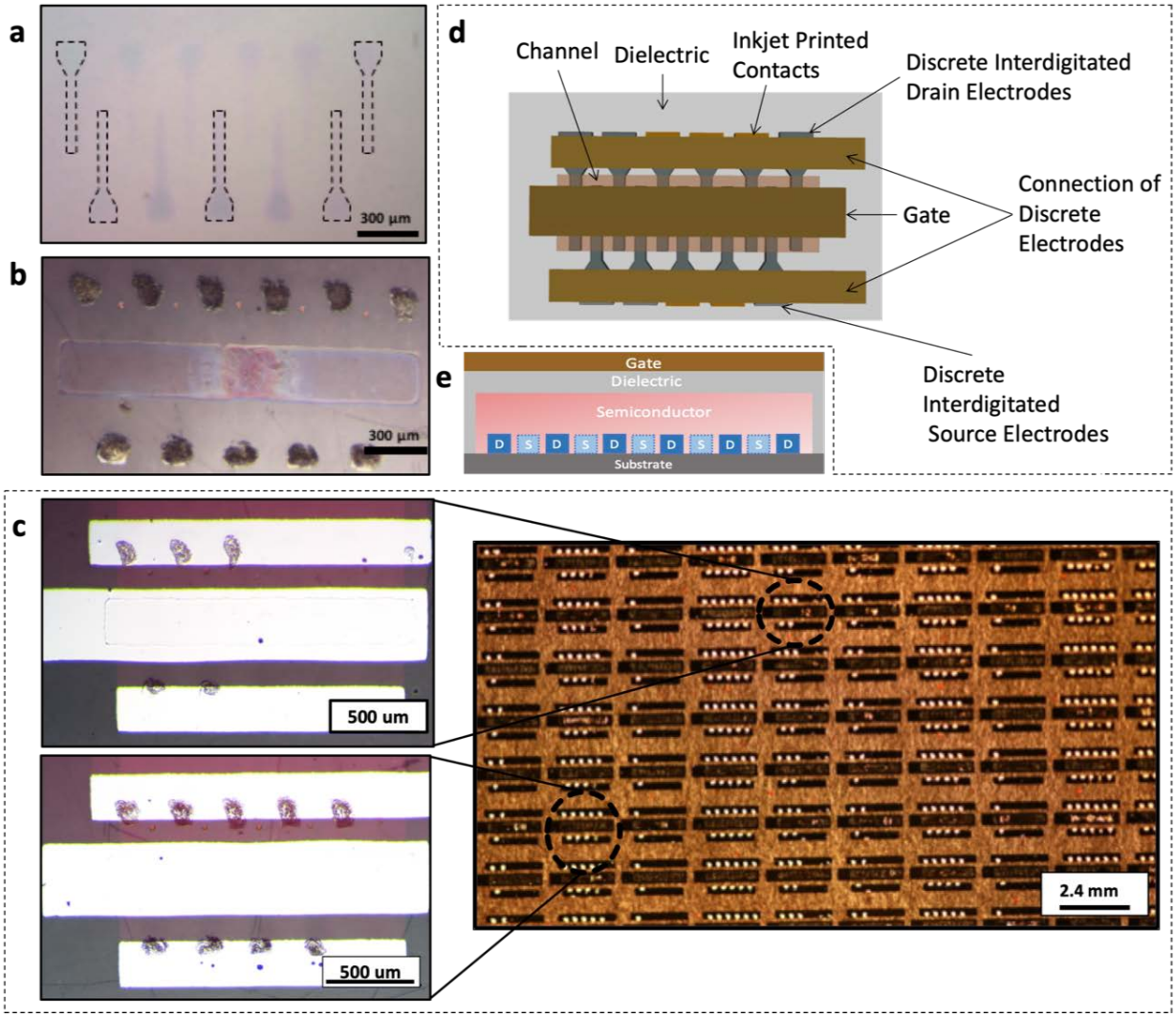

Figure 4.3: (a) Optical microscopy image of blade coated PEDOT:PSS interdigitated sources and drains electrodes. (b) Blade coated diF-TES-ADT:PTAA semiconductor film and the inkjet-printed contacts on the electrodes. (c) Optical microscopy images of two OTFTs and zoomed-out digital image of a portion of array of devices with various W/L ratios. (d) Top-view schematic of the device structure. (e) Cross-section view of the device.

4.2 Discrete Interdigitated Source and Drain Electrode Design

Printing technologies are promising for manufacturing flexible large-area electronics using functional ink materials. Solution processing methods facilitate the deposition of diverse

materials, and the stability and reliability of printing techniques using these functional inks are crucial [2]. In general, conventional lithography-based methods have a much higher yield (number of functional devices) in comparison with printing technologies owing to well-established and sophisticated methods with more accuracy, reliability, and stability. Yield and variability are limiting factors in the fabrication of devices using printing techniques. The identification of roots of failure in printing and optimization can result in the improvement of the yield [127]. In most works interdigitated structure is utilized for scale ratio modifications [24, 35, 85]. To investigate the pattern formation with surface energy patterning and blade coating, the common comp shape interdigitated structure was considered. Figure 4.4a demonstrates Aluminum interdigitated source and drain electrodes evaporated through a designed stainless steel mask with 100 % yield as expected. Using the identical design for surface energy patterning results in incomplete patterns, as shown in Figure 4.4b. One of the underlying reasons behind the deficiency in the patterns is the geometry of the sources and drains. In the comb shape design, most of the ink resides in the rectangles interconnecting the parallel source and drain electrodes. During the blade coating, most of the ink resides in those rectangular regions with the insufficient flow in the fingers. However, changing the edges in the interconnection section of the electrodes and the perpendicular rectangular part eases the ink flow into the electrodes and finally improved patterns, as shown in Figure 4.4c. The schematic of two different designs is summarized in Figure 4.4d. Figure 4.5 demonstrates the 2D map of the discrete source and drain electrodes and the effect of the geometry and spacing on the yield, as explained previously.

4.3 Performance and Reliability

Discrete Interdigitated Organic Thin Film Transistors Performance

The number of on-demand inkjet-printed source and drain contacts, can digitally modulate drain current I_D as following:

$$I_D \propto (n-1) \times W/L; 1 \leq n \leq 10 \tag{4.1}$$

where n is the number of inkjet-printed contacts on discrete source and drain electrodes. By increasing n, W is increased while L is kept constant. The increase of W increases I_D. For example, a device with n = 5 has the W/L of $(1000\mu m/50\mu m)$. The transfer characteristics of three typical devices with n =3, 8, 11 are shown in Figure 4.6a, b, and c. The output characteristics of these devices are shown in Figure 4.6d, e, and f. The gate leakage currents associated with those 3 devices are demonstrated in Figure 4.6g, h, and i. By adding to the number of active channels I_D is increasing as expected. The variability in change of I_D is later studied and explained by crystal structure of the semiconductor channel. The performance of devices indicate no contact barrier, high output resistance, good square law and low I_{off} current. The transfer and output characteristics of n of 1,3,4,5,6,8, and 9 are

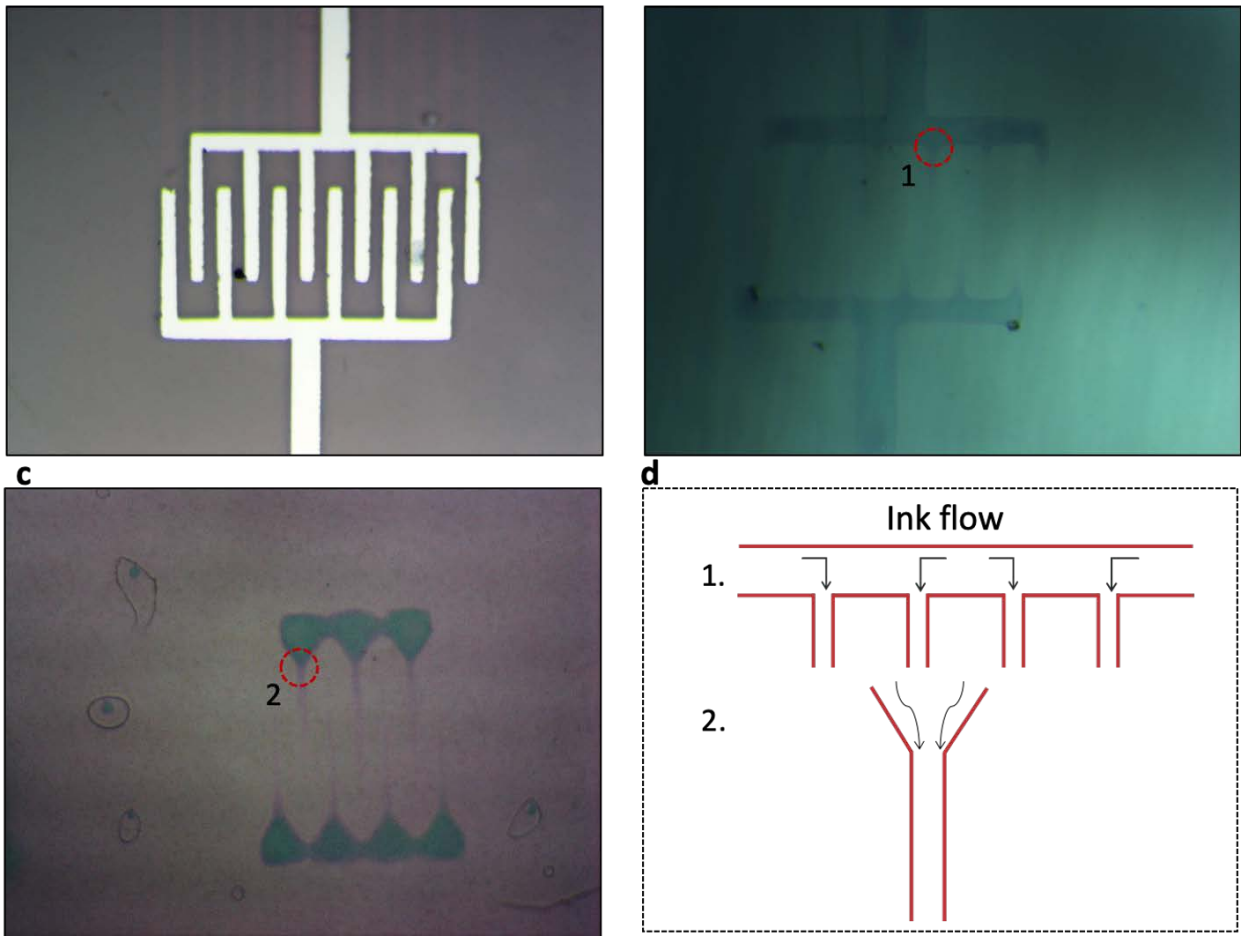

Figure 4.4: (a) Optical microscopy of Al evaporated interdigitated source and drain electrodes. (b) Optical microscopy of surface energy pattered (SEP) blade-coated interdigitated sources and drains electrodes. The masks used for evaporation and SEP process are identical. (c) Discrete interdigitated SEP blade-coated source and drain electrodes. (d) Illustration and comparison of the ink flow in two different designs of 1 and 2.

shown in Figure 4.7. Performance of OTFTs is characterized by studying 64 single channels. A single channel, shown in Figure 4.8a, is defined as the active channel area between two contact-printed discrete source and drain electrodes. The selected single channels are along an array where their DC electrical characteristics are measured and characterized in air by output characteristic curves derived for each channel. The V_{th} is found by the interception of the fitting curve to the $\sqrt{I_D} - V_G$ plot as shown in Figure 4.8b. The saturation mobility was calculated from transfer characteristics $I_D - V_G$ in the saturation regime plotted as $\sqrt{I_D} - V_G$ and the μ is calculated using the I_D saturation equation as following: (2)

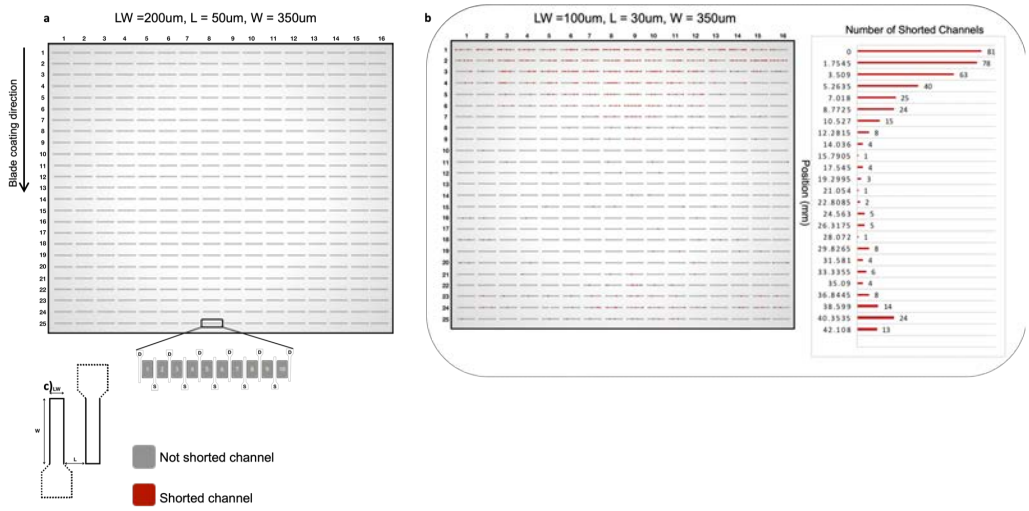

Figure 4.5: (a) LW = 200μm, L = 50μm, W = 350μm with 100% yield, (b) LW = 100μm, L = 30μm, W = 350μm with 441 shorted channels and 89% yield. (c) Source and drain geometry with three variables of line width (LW), length (L), and width (W). 2D yield map of 4000 Channels (10 channel device $\times$ 16 Col $\times$ 25 Rows) for two different source and drain geometries.

$$\mu = \frac{2L}{WC_i}\left(\frac{d\sqrt{I_D}}{dV_{GS}}\right)^2 \tag{4.2}$$

Figure 4.8c demonstrates an example of subthreshold slope (SS) derivation, which is defined to be the inverse slope of the $\log(I_D)$ vs. V_{GS} in the subthreshold region. The SS, V_{th}, $\log(I_{ON}/I_{OFF})$ and μ statistical distributions of 64 single channels are shown in Figure 4.8d. The mean subthreshold swing is 1.39 V/dec. For these channels, the average threshold voltage is -0.96V with a 1.07 standard deviation and the mean mobility of the devices is 0.38 cm^2/Vs with a standard deviation of 0.23.

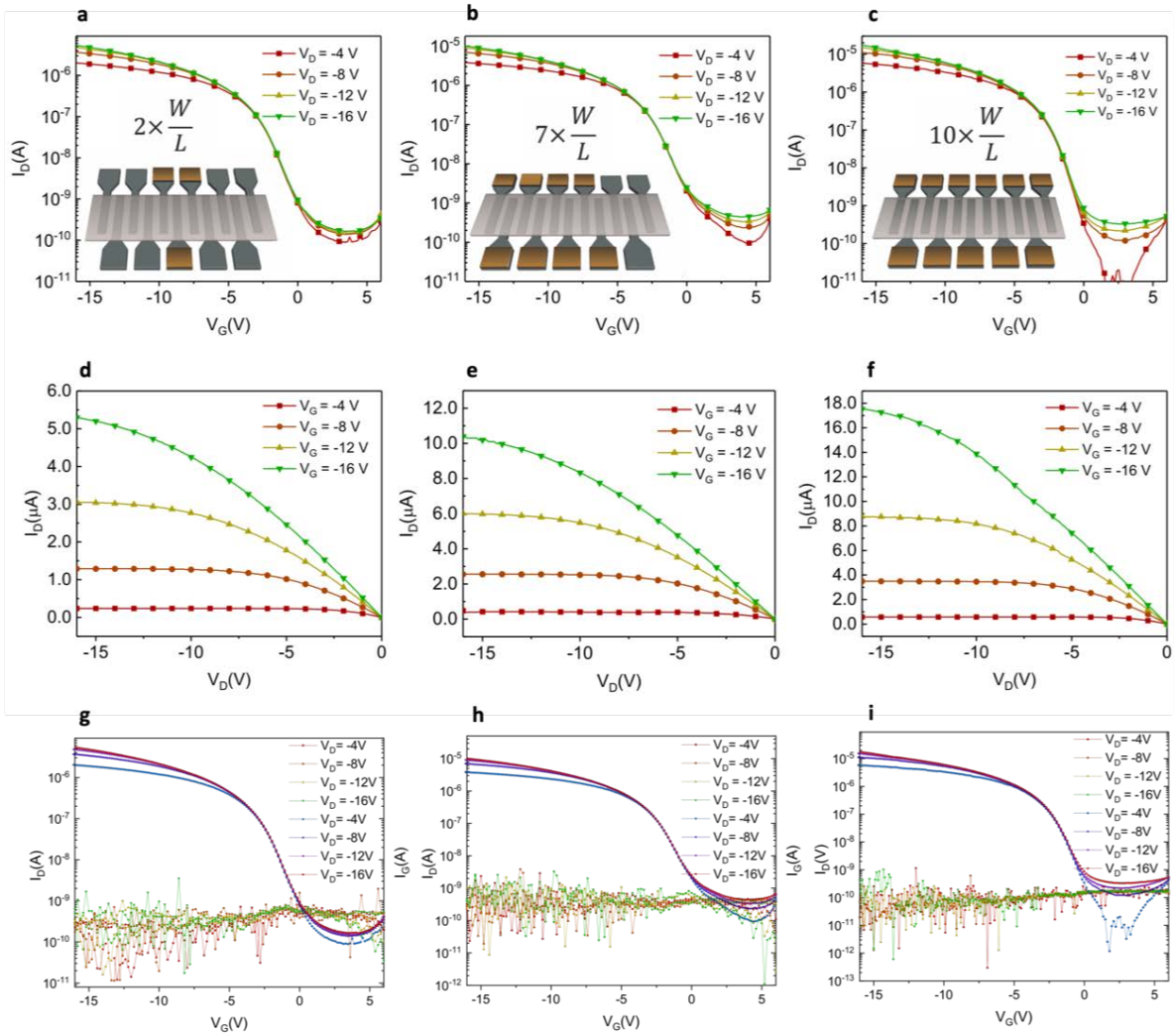

Figure 4.6: Channel width (W) and length (L) of a single channel are 250m and 50m. The scale factor (W/L) is changed and increased by adding the number of inkjet-printed contacts. Transfer characteristics of devices with scale ratios of (a) 2×W/L , (b) 7×W/L, (c) 10×W/L. Output characteristics of devices with various scale factors of (d) 2×W/L, (e) 7×W/L, (f) 10×W/L, and gate currents of (g) 2×W/L, (h) 7×W/L, and (i) 10×W/L

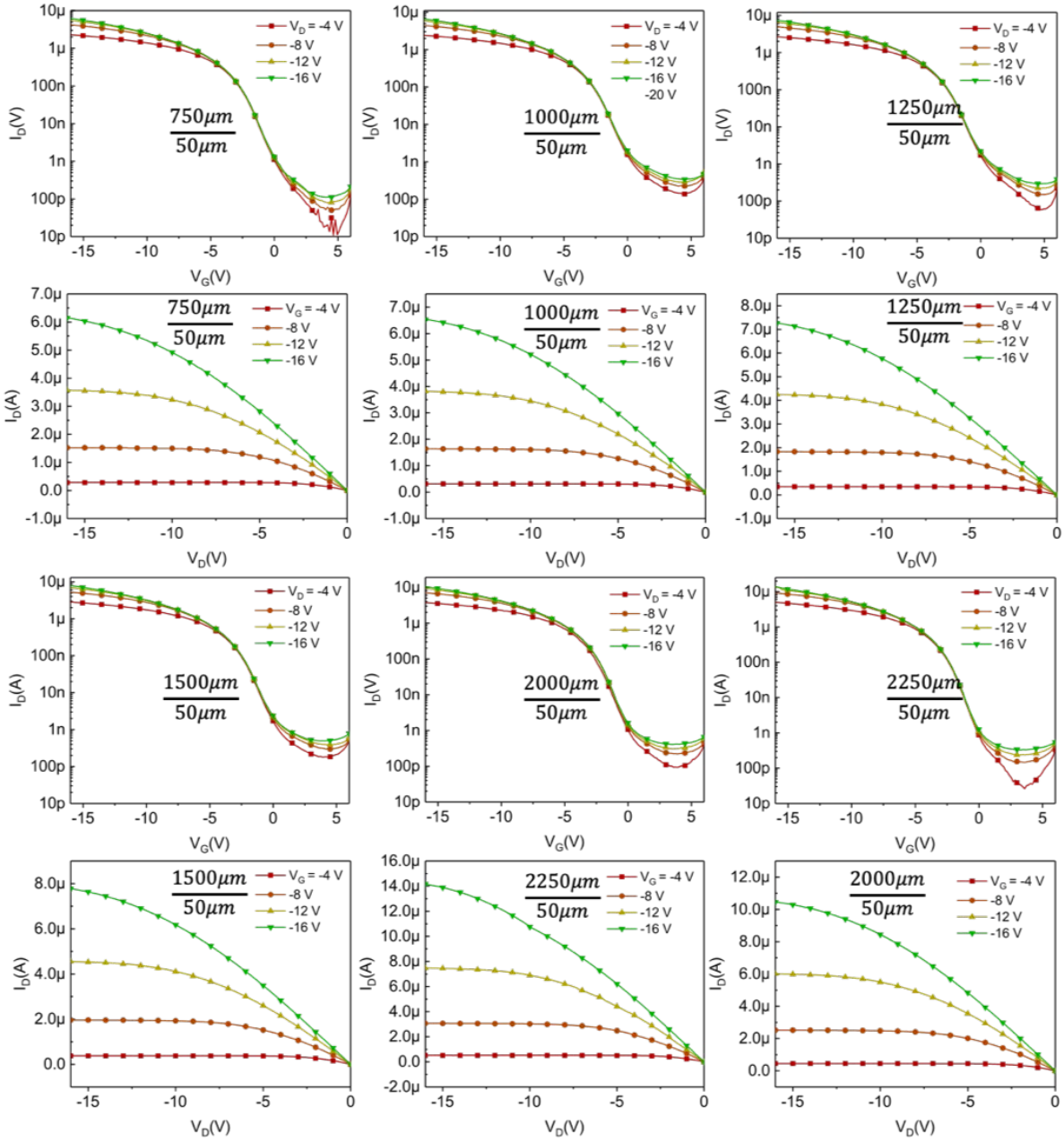

Figure 4.7: ID-VD and ID-VG output characteristics of devices with scale factors of 3×W/L, 4×W/L, 4×W/L, 5×W/L,6×W/L,8×W/L and 9×W/L.

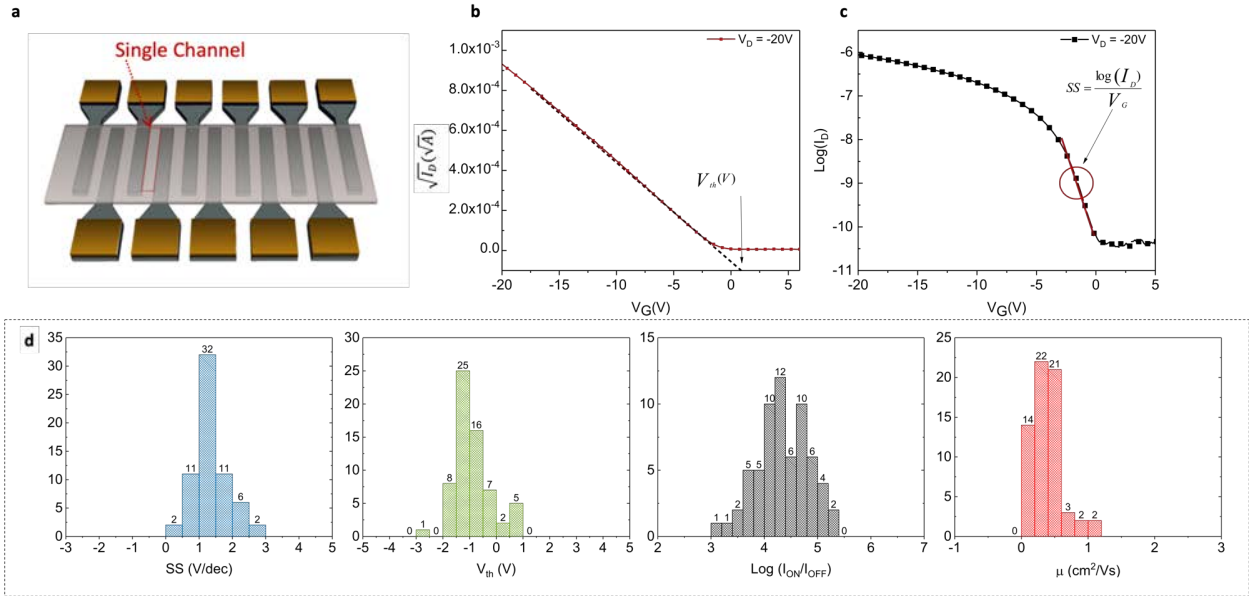

Figure 4.8: (a) The schematic of a single channel between two contact printed electrodes. The performance of 64 single channels is characterized and the parameters are extracted. (b) Representative example of $\sqrt{I_D}$ vs. VG for threshold voltage (V_{th}) extraction. (c) Example of subthreshold slope measurement. (d) The statistical distribution of subthreshold slope (SS), threshold voltage, on/off ratio and mobility of single channels.

Influence of Crystal Grains on Device Performance

The electrical characteristics of individual device channels are demonstrated in Figure 4.9a, showing variations in Vth, μ and SS changes for adjacent channels in a single device. In order to study underlying reasons for such variations, Atomic Force Microscopy (AFM) was utilized to obtain information on the morphology and surface features of the individual channels. AFM images of random spots along individual channels in a typical device are shown in Figure 4.9b. The images are readily interpretable as presence of a number of crystalline domains with different orientations (along the source electrode to drain) and well-defined boundaries that extend up to tens of microns which is largely in agreement with the literature [22, 56, 63, 94, 97]. Importance of good connectivity between domains and well-aligned crystallography across transistor channels has been previously highlighted as these features have been shown to greatly influence charge mobility and performance as well as device-to-device variability due to presence of deep charge traps in the boundaries [35, 56, 94](Mahsa's Note: Could not add the citation num 38 and 42). Moreover, domains show distinctive ribbed thickness variations and needle-like crystallites are occasionally apparent at the boundaries. These have been previously correlated with poorer device performance due to hindrance in charge transport across domains in the channels [19, 50, 83].

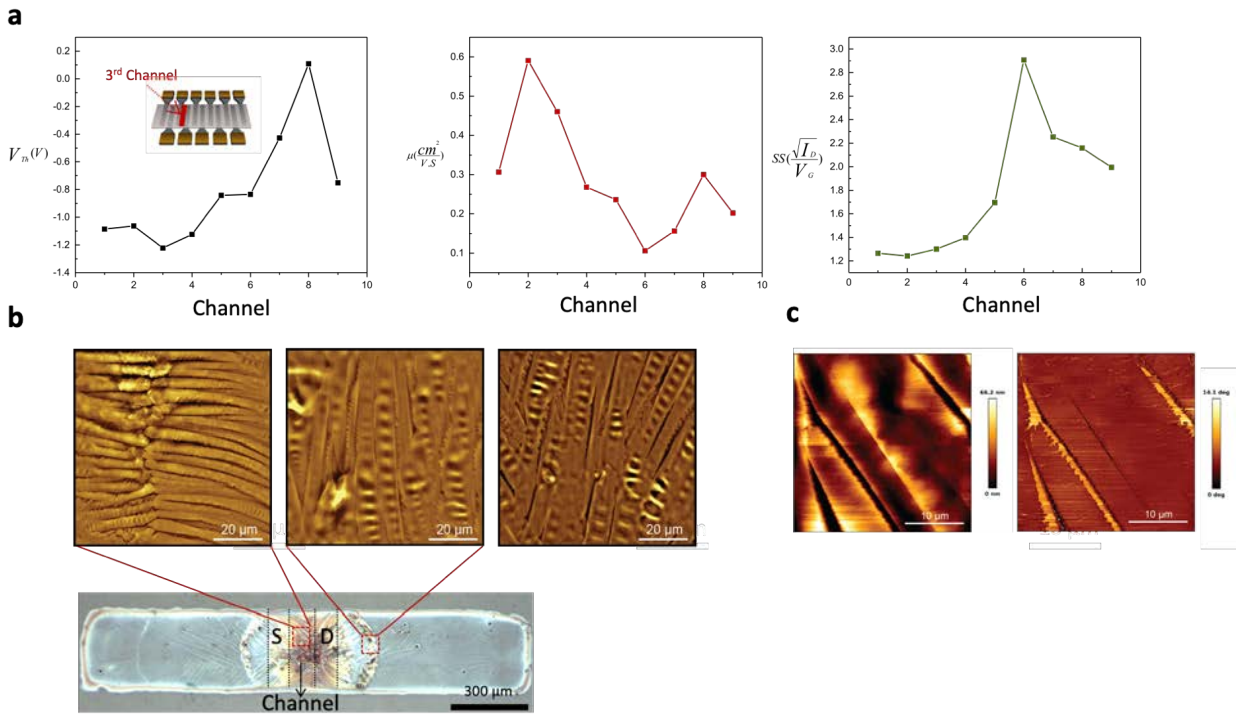

Figure 4.9: (a) Threshold voltage, mobility, and subthreshold slope of each individual channel in a single organic thin film transistor. (b) Atomic force microscopy (AFM) images of three 100μm$\times 100\mu$m regions in different areas of the semiconductor channel.

4.4 Organic Circuits

Organic electronics provides the possibility of fabrication of flexible circuits at low-temperature and lower cost in large area [88]. By using the uncomplicated fabrication techniques compared with conventional photolithography-based techniques, it is possible to change and modify circuit designs at a rapid time. Generally, a specific circuit design necessitates the change of scale ratio of devices. Still, the quick change of scale ratio is a limiting factor for some fabrication techniques. While inkjet printing is considered an on-demand technique, many failures can happen in the printing and resulting in defective OTFTs [127]. In this chapter, combination of SEP blade coating of the discrete electrodes with inkjet printing only for contacts has two main benefits. First, by merging the two fabrication methods, inkjet printing can be only used for deposition of small square shaped contacts on the solution processed discrete electrodes. The simplified inkjet printed contacts decrease the possibility of defects common for bigger patterns. Secondly, it provides the possibility of digitally selection of the electrodes and modulation of the scale ratio required for any specific circuit design. Digital circuit functionality can be maintained in different ways including static and dynamic

logic. The reliability of this fabrication technique was proven through the demonstration of static logic inverters which are the most fundamental element of a more complicated digital circuit. Figure 4.10a shows the circuit schematic of an enhancement-load inverter with two OTFTs one operating as the drive transistor and the other as the load transistor. The drive transistor turns ON with the supply voltage VDD applied to the gate of the drive transistor, Vin (input node). Then the resistance becomes significantly smaller than the load transistor and the output voltage is pulled to the ground voltage considered as logic '0'. With logic '0' applied to the input voltage, the drive transistor is OFF and the saturated-load transistor pulls the voltage at the output node to a difference value between the supply voltage VDD and the threshold voltage which is logic '1'. Figure 4.10b shows and compares the electrical transfer characteristics of two inverters. The voltage gain, the maximum small signal amplification, of the enhancement-load inverter is determined by the ratio of scale factor of the two devices:

$$Gain = dV_{out}/dV_{in} = \sqrt{\frac{W_{drive}.L_{load}}{W_{load}.L_{drive}}} \tag{4.3}$$

This equation is derived under the assumption that the load and drive transistors both have the same electrical characteristic of V_{th} and μ. For OTFTs with variabilities in electrical characteristics, the equation is legitimate, and the gain is proportional to the ratio of the scale factors of the two inverters, in Figure 4.10b one has W_{Drive} of 2000μm and the other with W_{Drive} of 1000μm, both with the same channel length of 50μm. The inverters show satisfactory transfer characteristics as expected. The increase of W_{Drive} results in higher voltage gain and improvement in the noise margin. Figure 4.10c and d show obtained voltage transfer curves and signal voltage gain with V_D supply voltages of -4V to -20V.

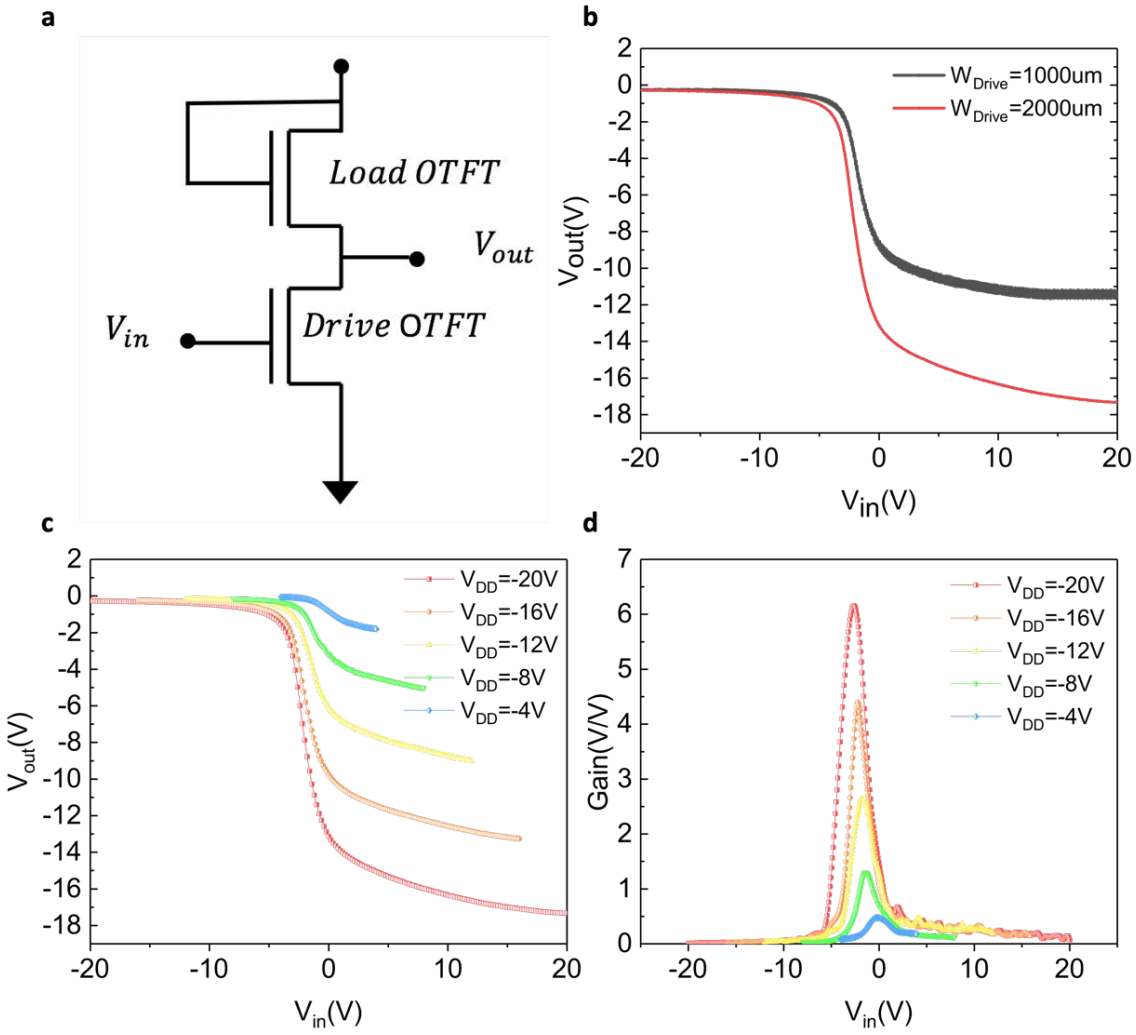

Figure 4.10: (a) Circuit configuration of an enhancement-load inverter. (b) Voltage transfer characteristics comparison of two different inverters, one with drive channel width (W_{Drive}) of 2000μm (8×W/L) and the other with W_{Drive} of 1000μm (4×W/L); both inverters have the same channel load width (W_{Load}) of 250×m (1×W/L). Increase of W_{Drive} results in improvement of gain. c) Voltage transfer characteristics of an inverter with W_{Drive}=1000μm and W_{Load}=250μm and d) the plotted slope of transfer curves with the gain defined at the maximum point. The gain of the inverter is approximately around 6 at supply voltage of -20V.

	SS(V/dec)	**V_{th}(V)**	**$\mu(cm^2/V.s)$**
mean	1.36	-0.96	3.8
SD	0.5	1.07	0.27

Table 4.1: Average subthreshold swing, V_{th}, and μ of devices.

4.5 Conclusion

In conclusion, this chapter demonstrated a fast fabrication method for on-demand modulation of scale ratio along a large array of devices. The combination of inkjet printing for channel modulation with SEP blade coating is proper for large area electronics due to fast fabrication and change of channel width without the need for change of the process for a new design. Devices exhibit an expected change in output characteristics with modulation of channel width from 250μm to 2500μm. The individual channels show good average subthreshold swing of 1.39 V/dec, threshold voltage of -0.96V with a standard deviation of 1.07 and mobility of the devices is 0.38 cm^2/Vs. The variability witnessed in the electrical characteristics of devices is inherent in the nature of variation in the printing techniques and most importantly resulted from the lack of control in the formation of the crystal structure. Despite the variations, we have been able to fabricate enhancement-load inverters with good voltage transfer curves. An inverter with selected WDrive of 2000μm has a dc gain of 6 with supplied voltage of -20V.

Chapter 5

Bilayer gate dielectric for high performance and low-voltage printed flexible organic field-effect transistors

5.1 Introduction

Organic electronics has inherent advantages over its inorganic counterpart: low cost, mechanical flexibility, transparency and low temperature processing [29, 95, 141, 153, 163]. Functionality of organic electronic devices relies on the electrical and optical properties of π-conjugated organic molecules. The main advantage of these materials is the solution processability, which enables utilization of numerous deposition techniques, such as printing and/or coating methods [69, 126, 154]. Printing is a powerful technology for the mass production of the organic electronic devices at relatively low cost and fast processing time with reasonable device yield [45, 109]. Additionally, printing materials of desired patterns directly onto the substrate results in a significant reduction of material waste, compared to the certain conventional fabrication approaches such as spin-coating. Last decade witnessed emergence and evolution of numerous organic electronic devices such as organic solar cells [1, 23], organic field-effect transistors [31, 109], organic light-emitting diodes [59, 79, 165] and sensors [53, 62]. Among these technologies, organic field-effect transistors (OFETs) has gained particular attention, due to ability to be combined into numerous setups, such as logic circuits, microprocessors, drivers for flat panel displays, sensors and memories [123, 149, 150, 152]. Despite the tremendous potential of OFETs, their widespread commercialization has been hindered by the low field-effect mobility (μ) and the high operational voltage of these devices. To improve the electrical performance of OFETs, significant efforts have been directed towards design and synthesis of new organic semiconductors materials. As a result, OFETs showing field-effect mobilities as high as 10 $cm^2/V.s$ [73] were demonstrated. Furthermore, the charge transport on the OFETs channel can be improved by controlling the semiconductor/dielectric interface and the bulk properties of the dielectric layer [82, 140]. The choice of

the dielectric material in OFETs is another important consideration for achieving high device performance. Low operating voltage of the transistors is a critical requirement to enable portable applications that often rely on low-cost printed power sources [159]. Until recently, the majority of the organic electronic circuits were demonstrated with relatively high operational voltage of 10 V and above [75, 139, 158]. Lower operational voltage of OFETs can be achieved by minimizing the thickness and maximizing the dielectric constant of the dielectric layer. Most of the organic dielectric materials have low dielectric constant ($\varepsilon_r \simeq 2-4$) and, hence, using a thin dielectric layer ($d \leq 20$ nm) is a more common approach to achieve low operational voltage OFETs [68, 145]. However, using thin gate dielectric layer in OFETs can contribute to increase the gate leakage current, resulting in a poor device performance and low yield. Recently, a new high dielectric constant material (high-k) ferroelectric relaxor terpolymer, poly(vinylidenefluoride-trifluoroethylenechlorofluoroethylene) P(VDF-TrFE-CFE) was developed by introducing dopants of chlorofluoroethylene (CFE) to the ferroelectric copolymer poly(vinylidenefluoridetrifluoroethylene) (P(VDF-TrFE)) [8, 17]. The CFE units reduce the polarization domains in the relaxor terpolymer P(VDF-TrFE-CFE) and consequently minimize the effects of remnant polarization and hysteresis under high electric field [17]. The highest among known polymers dielectric constant ($\simeq 60$ at room temperature) can be achieved for the P(VDF-TrFE-CFE) [80], Nevertheless, few papers have reported low voltage operational organic OFETs and memories using this material [80, 81, 146, 148]. Moreover, using high-k gate dielectric in OFETs can result in the high dipolar disorder at the semiconductor/dielectric interface and the residual polarization effects [143]. This leads to formation of charging traps at the interface, contributing to an increase in threshold voltage and subthreshold swing, as well as reducing the field effect mobility of charge carriers in OFETs [49, 142]. The dipolar disorder at the semiconductor/dielectric interface can be mitigated by incorporating a thin layer of low-k insulator material between the semiconductor and the high-k dielectric layer [164]. The low-k insulator protects the semiconductor layer from the dipolar disorder in the high-k dielectric layer. Thus, using the bilayer gate dielectric combines the advantage of the two types of insulators materials, in which the low-k dielectric reduces the effects of the dipolar disorder at the semiconductor/dielectric interface, while the high-k dielectric enables the high gate capacitance. In order to reduce the operating voltage of surface enabled blade coated OFETs (Figure 5.1b) reported in previous chapters, we have used a bilayer gate dielectric composed of high-k P(VDF-TrFE-CFE) and a thin layer of low-k fluoropolymer (Figure 5.1d). The polymers are shown and summarized in Figure 5.1a. To compare the performance we have also built OFETs using only the high-k P(VDF-TrFE-CFE) as gate dielectric layer (Figure 5.1c). The P(VDF-TrFE-CFE) dielectric layer is deposited by spray-coating, while the low-k fluoropolymer (DUPON) dielectric is deposited by blade-coating. The source/drain electrodes and the semiconductor layer are deposited by blade-coating on surface energy patterned (SEP) substrates, following the experimental procedures described in details on the previous work [109]. A blend of a small molecule 2,8-difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene (diF TES ADT) with an amorphous polymer poly[bis(4-phenyl)-(2,4,6-trimethylphenyl)amine] (PTAA) (1:1) is used as active layer, while the source and drain electrodes is prepared from an aqueous

solution of PEDOT:PSS. The gate contact of the devices is deposited by thermal evaporation of aluminum. The electrical characterization of the OFETs was carried out in air and all the devices reported here show operational voltage $\leq$8 V. The average threshold voltage, sub-threshold swing, log of on/off ratio and field effect mobility values for the P(VDF-TrFE-CFE) based OFETs and the bilayer devices are -0.79 V and -1.3 V, 0.55 V/dec and 0.71 V/dec, 3.9 and 3.9, 0.03 $cm^2/V.s$ and 1.3 $cm^2/V.s$, respectively. We demonstrated the functionality of the devices through the enhancement-load design, used in chapter 3 and 4.

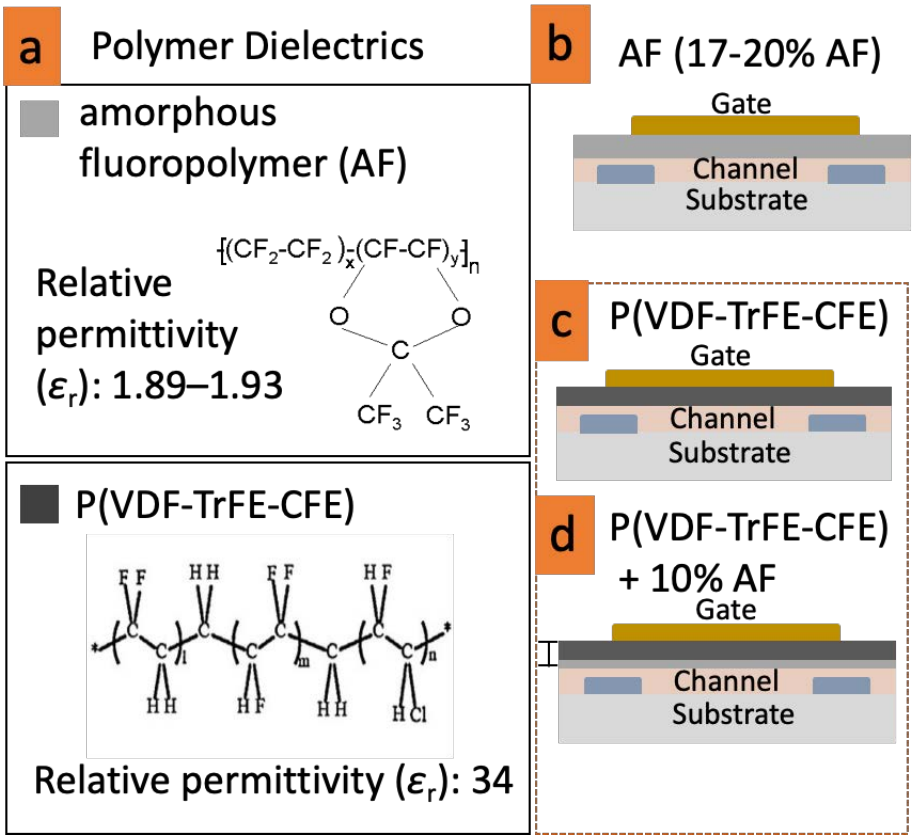

Figure 5.1: Molecular structures of (a) amorphous fluropolymer(AF) and high-k dielectric P(VDF-TRFE-CFE) (PVDF). Cross-section device structure with different gate dielectrics of (b) AF, (c) PVDF, and (d) bilayer AF/PVDF.

5.2 Spray Coating Method

Spray coating is a high-throughput coating method used in graphic arts and industry. The technique is ideal for a variety of surface morphologies and solution rheologies, which enables

achieving the desired film properties at large scales with low cost [34]. Despite the advantage of simple processing, issues such as film thickness control and roughness have been limiting factors for applying this method for particular layers of the OTFT device such as the semiconductor layer for which the mentioned matters are crucial. The angle of the brush (θ), the distance of the head, the direction of the coating, speed, spray pressure, temperature of the substrate, and the dispense rate are parameters affecting the film's quality [54]. The variations in the technique can be optimized and more controlled by automatizing the setup. Figure 5.2 depicts the deposition technique in which the fast flow of air results in the local reduction of air pressure and pulling the solution. The rapid influx of the air sprays and atomized small droplets that stick and instantly dry due to the higher temperature of the substrate. This technique is used for deposition of the high-k dielectric discussed in this chapter.

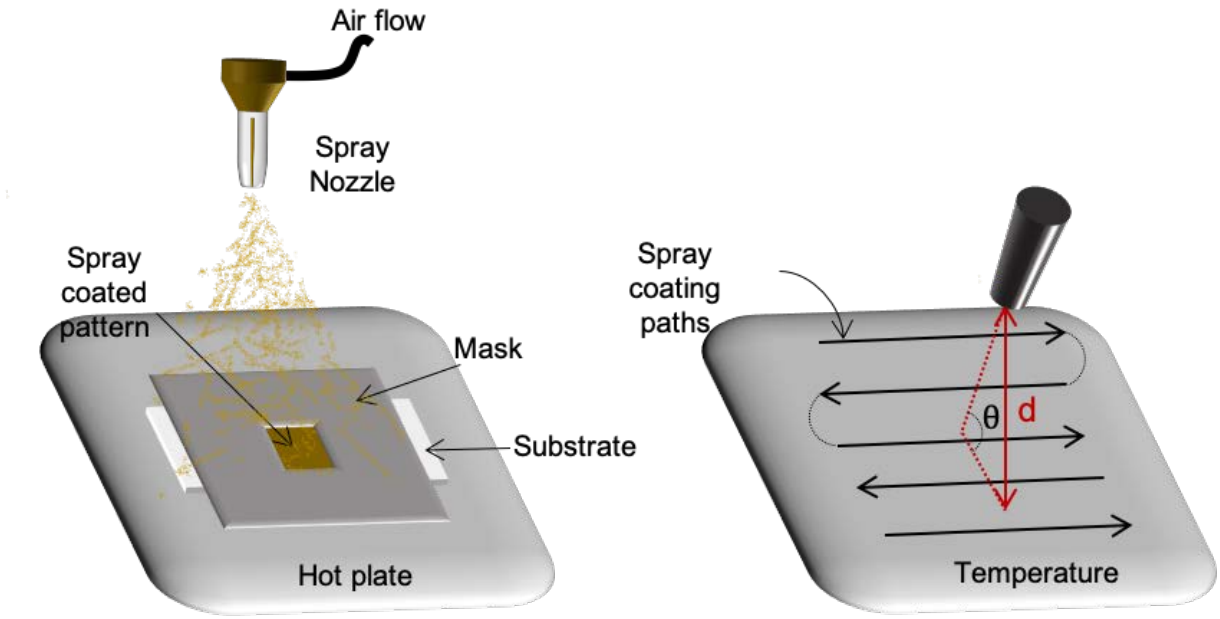

Figure 5.2: The schematic of spray coating setup and method.

5.3 Fabrication of OTFTs with Bilayer Gate Dielectric

Top-gate bottom-contacts OFETs were fabricated on polyethylene naphthalate (PEN) (DuPont PQA1) substrates. The PEN foils were cleaned with isopropanol and then plasma treated for 10 seconds. For the SEP process, first, a hydrophobic self-assembled monolayer (SAM) of

fluoroalkylsilane (FDTS) was deposited on the plastic substrate under light vacuum (0.1–1 Torr) for 20 minutes. To complete the SEP process, a stainless steel stencil defining the source and drain electrodes was pressed against the PEN substrate and then oxygen plasma-treated for 0.9 minutes at 20% power and 0.2 mbar. After the SEP process, explained in chapter 1, 35 μL of PEDOT:PSS solution was deposited by blade-coating at height of 100 μm above the substrate at 1.6 cm/s. The PEDOT:PSS source and drain electrodes were heated at 120°C for 10 minutes. Silver nanoparticles were deposited by ink-jet printing to define the source and drain contact pads. Silver patterns were cured at 120°C for 10 minutes. A second SEP process was performed at the same conditions as described before for the source and drain electrodes, while using a different layout mask (defining the channel characteristics) and then plasma-treated for 0.5 minutes. The semiconductor ink was composed by dissolving 10 mg/mL of the mixture of diF TES ADT: PTAA (1:1) in mesitylene:tetralin (1:1). The semiconductor layer was blade coated at a blade height of 150 μm with a blade speed of 1 cm/s inside a nitrogen glovebox. The active layer was dried at 120°C for 10 minutes. The 20 mg/mL of relaxor terpolymer P(VDF-TrFE-CFE) was dissolved in methyl ethyl ketone (MEK) and spray-coated on the entire area of the substrate. The spray coating process was realized inside a fume hood. The PEN substrate was kept on a hotplate at 120°C during the deposition process. Finally, aluminium gate electrode was thermally evaporated using a shadow mask. The fabrication steps for the P(VDF-TrFE-CFE)-based OFETs are shown and summarized in Figure 5.2a.

The same experimental procedures are used to fabricate the bilayer OFETs, adding the fluoropolymer deposition step between the active layer and P(VDF-TrFE-CFE) dielectric layer. The amorphous fluoropolymer (DuPont AF) diluted in FC770 (10 vol.%) was blade coated at blade height of 50 μm at speed of 2 cm/s. After letting the fluoropolymer film dry in a vacuum plate inside the glovebox for several minutes, it has heated at 120°C for 10 minutes on the hotplate.

5.4 Device Characterization

All the OFETs were characterized by output (I_d/V_d) and transfer (I_d/V_g) curves performed in air using an Agilent B1500a semiconductor analyzer. The transistor parameters, as the field effect mobility (μ), threshold voltage (V_{th}) and subthreshold swing (SS) were calculated in the saturation regime ($\mid V_d \mid = 8$ V) using the gradual channel approximation model [160]. The unipolar inverter were characterized by the voltage transfer characteristic (V_{in}/V_{out}) and then the voltage gain and the noise margin were calculated from the $dV_{out} = dV_{in}$ and by the maximum product criteria (MPC) [44], respectively.

Using an ink with low capillary number is essential for achieving good pattern fidelity by surface energy-driven patterning process of blade coating on SEP substrates. It ensures that viscous forces do not dominate the surface tension forces needed for self-assembled patterning. The capillary number is given by $C_a = \eta.\upsilon/\gamma$ where η is the ink viscosity, υ is the blade speed and γ is the surface tension as explained in chapter 1. Thus, a slow blade

speed, low ink viscosity and high ink surface tension are ideal parameters required for a good patterning. An excellent pattern fidelity and high yield are obtained for the source/drain electrodes and the semiconductor layer, as shown in Figure 5.3b and 5.3d. The optical microscopy images of the inkjet printed silver electrical contact pads and of the final device structure are shown in Figure 5.3c and 5.3e. The current-voltage characteristics (output

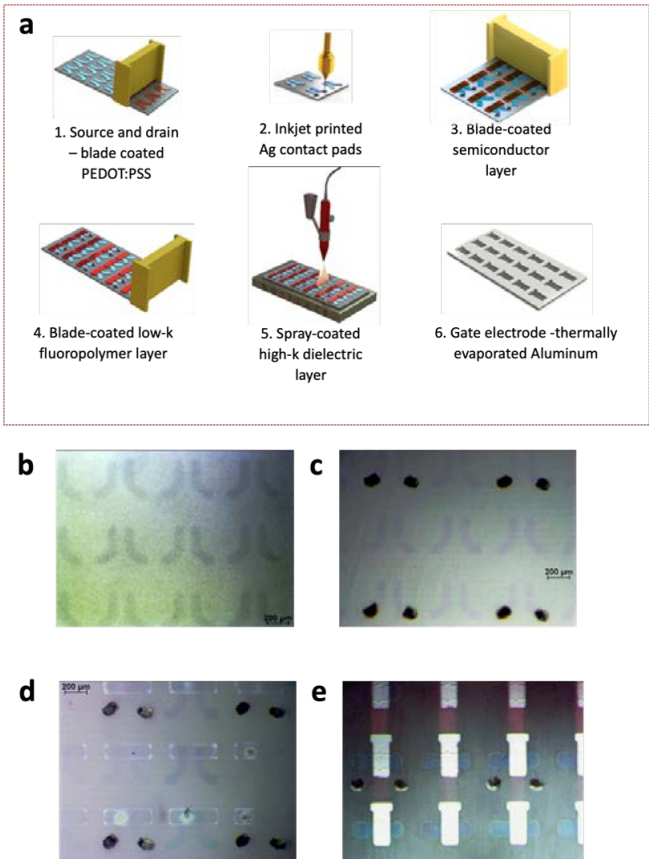

Figure 5.3: Fabrication steps of the P(VDF-TrFE-CFE) based OFETs: combination of SEP blade-coating for the source drain and semiconductor layers, blade-coating for the low-k dielectric insulator in the bilayers transistors, spray-coated of the P(VDF-TrFE-CFE) insulator layer and thermal evaporation of aluminum for the gate electrode. Optical microscopy images of (a) the blade coated PEDOT: PSS source/drain electrodes, (c) inkjet printed silver contact pads, (d) blade coated semiconductor layer and (d) thermally evaporated aluminum gate electrode (final device structure with bilayer gate dielectric).

and transfer curves) of a P(VDF-TrFE-CFE) based OFET are shown in figure 5.4b-c). The thicknesses of the spray coated P(VDF-TrFE-CFE) layer is in the range of 400 nm. The P(VDF-TrFE-CFE)-based OFETs operate effectively at gate voltages as low as 8 V, showing

	SS(V/dec)	$\mathbf{V}_{th}$**(V)**	$\boldsymbol{\mu(cm^2/V.s)}$	$\boldsymbol{log(I_{on}/I_{off})}$
mean	0.55	-0.79	0.03	3.9
SD	0.49	-0.67	0.91	0.21

Table 5.1: Average field-effect mobility, threshold voltage, on/off ratio, subthreshold swing and coefficient of variation for the P(VDF-TrFE-CFE) based OFETs.

a maximum on-state drain current of 0.25 μA and off-state current below as 10^{-11} A. The high dielectric constant ($\varepsilon \simeq$ 34- Figure 5.5a) and capacitance per area (40 nF/cm^2 - Figure 5.5b) of the P(VDF-TrFE-CFE) leads to the high electric displacement and the high on-state drain current at low gate voltages ($\leq$ 8 V), as shown in Figure 3(a). Overall, we have measured 25 devices from 2 different batches. The statistical distribution of the transistor parameters are shown in Figure 5.4a. The mean for each parameter and the coefficient of variance, which is defined as the ratio of standard deviation to the mean, are summarized in table 1.

The device yield is 96% for the OFETs fabricated only with the polymer P(VDF-TrFE-CFE) as gate dielectric layer. As can be seen in Figure 5.4a, these devices exhibit V_{th}, S, $log(I_{on}/I_{off})$ and μ values between -0.1 and –2.3 V, 0.1 and 1 V/dec, 3 and 5.1; 10^{-3} and 10^{-1} cm^2/Vs, respectively. However, despite the large variability of the transistors' parameters, 58.3% of the devices show $V_{th} \leq$ -0.6 V and 3.0$\leq log(I_{on}/I_{off}) \leq$4.0, while 75% of the OFETs exhibit SS $\leq$ 0.7 V/dec and 0.01 $\leq \mu \leq$ 0.07 cm^2/Vs. The variability can be confirmed by the coefficient of variance shown in table 1. The average performance parameters of these devices are as follows: μ = 0.03cm^2/Vs , V_{th} = -0.79 V, $log(I_{on}/I_{off})$ = 3.9 and S = 0.55 V/dec. Although the OFETs with the P(VDF-TrFE-CFE) as gate dielectric layer have showed low operational voltage ($\leq$8 V), they exhibited significantly lower field effect mobility values compared to diF TES ADT: PTAA-based OFETs using low-k dielectric materials (0.1 $\leq \mu \leq$ 2.4 cm^2/Vs) [51, 109, 112] as result of the high dipolar disorder at the semiconductor/dielectric interface.

In order to improve the field effect mobility and reduce the dipolar disorder at the interface of the devices, we inserted a thin layer of fluoropolymer between the active layer and the high-k relaxor terpolymer P(VDF-TrFE-CFE). Coating on top of the fluoropolymer layer is particularly challenging due its high hydrophobicity. The water contact angle of the obtained blade coated fluoropolymer layer is 113° (Figure 5.6), which is too hydrophobic for spin-coating or blade-coating the high-k relaxor terpolymer P(VDF-TrFE-CFE) on top. Therefore, the spray coating method was chosen as a deposition technique for P(VDF-TrFE-CFE) layer. The thicknesses of the blade coated fluoropolymer layer was around 120 nm, while the thicknesses of the spray coated P(VDF-TrFE-CFE) layer was kept 400 nm for the bilayer gate dielectric devices. Although, the low-k buffer layer lowered the effective dielectric constant by 44%, the dielectric constant of the bilayer ($\varepsilon \simeq$ 19- Figure 5.7a) remains higher than that of the commonly used dielectric polymers such as polystyrene ($\varepsilon \simeq$ 2.6) and

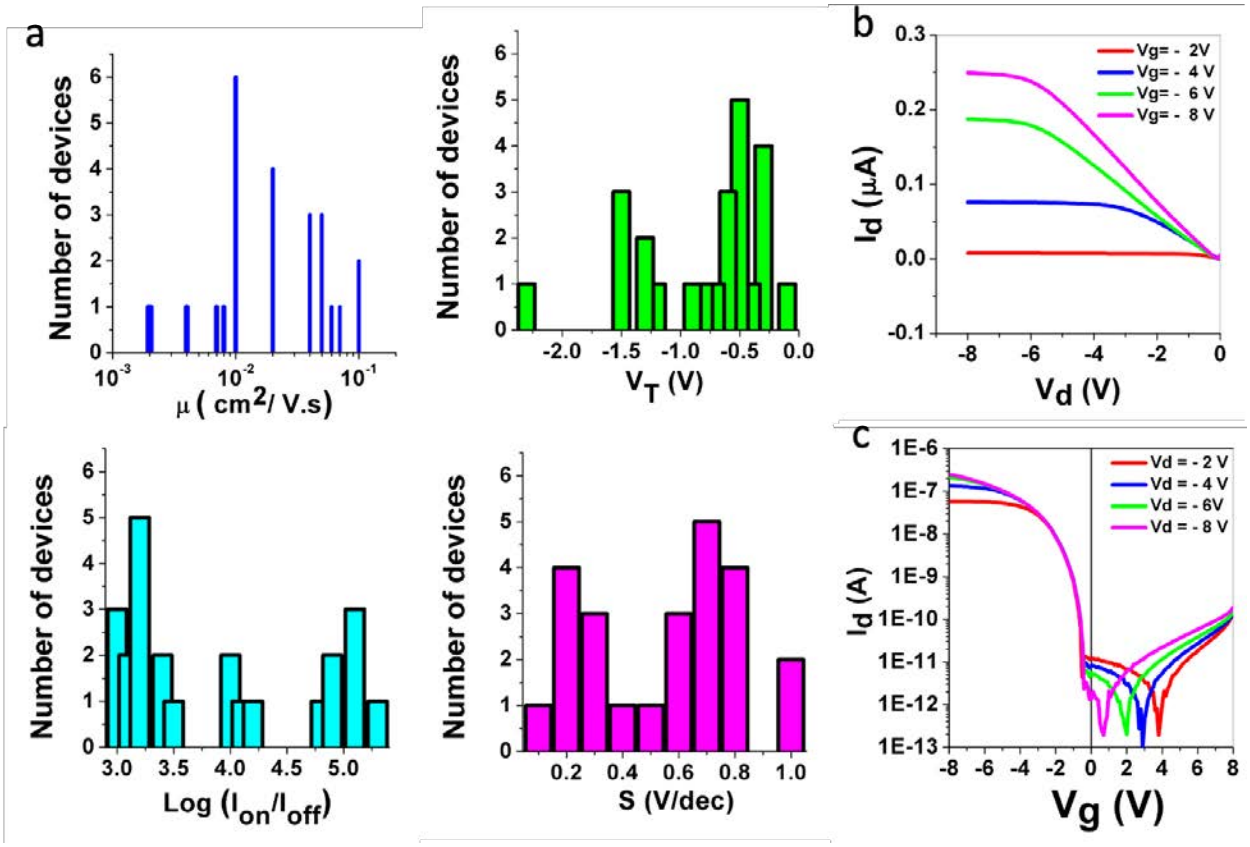

Figure 5.4: (a) Statistical distribution of the transistor parameters (field effect mobility, threshold voltage, on/off ratio and subthreshold swing) and (b) typical current-voltage characteristics of a P(VDF-TrFE-CFE) based OFET and

PMMA ($\varepsilon \simeq 3.5$). A large capacitance per area of 18 nF/cm^2 (Figure 5.7b) can be achieved for the bilayer gate insulator devices, which is almost 10 times larger than the capacitance obtained using a low-k dielectric material of the same thickness [18]. We have measured 25 OFETs from 2 batches. The typical current-voltage characteristics obtained for the bilayer OFETs are shown in Figure 5.8b. The statistical distribution of the transistor parameters for the bilayer devices are shown in figure 5.8a, whereas the average performance and the coefficient of variance for each parameter are summarized in table 2. As can be seen in figure 5.8b, the bilayer OFETs operate at low voltages ($\leq$ 8 V), showing maximum on-state current of 1 μA and off-state current of 10^{-10} A. The bilayer devices show μ_{FET}, V_{th}, $log(I_{on}/I_{off})$ and SS values between 1 and 1.9 cm2/V.s, -1 and -1.8 V, 3.7 and 4.2, 0.5 and 0.8 V/dec, respectively. The bilayer transistors and transistors with only P(VDF-TrFE-CFE) as gate insulator exhibit similar performance characteristics for V_{th}, $log(I_{on}/I_{off})$ and SS. However, the bilayer transistors show significantly higher values of μ, comparable to the

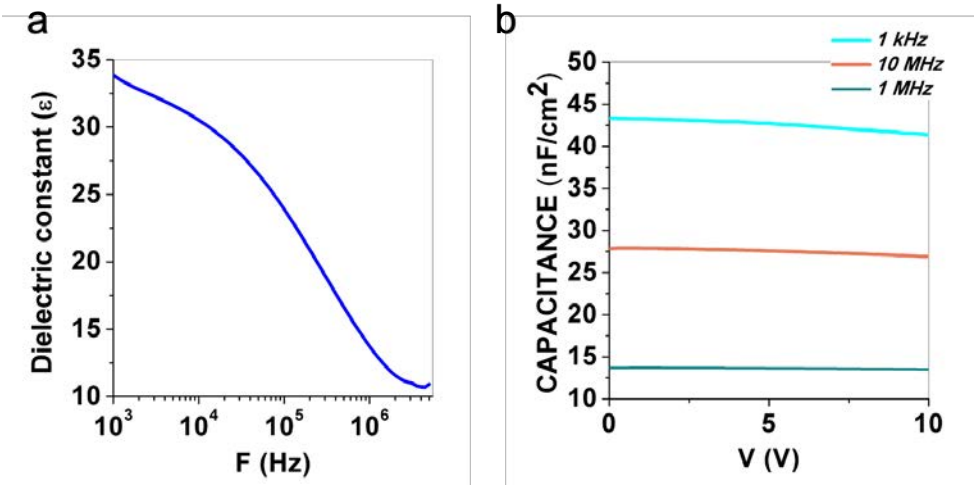

Figure 5.5: (a) Dielectric constant with respect to frequency for the relaxor terpolymer P(VDF-TrFE-CFE) films. (b) Capacitance per area versus voltage for the relaxor terpolymer P(VDF-TrFE-CFE) films.

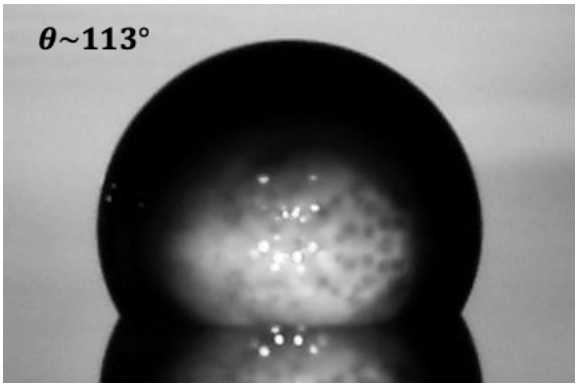

Figure 5.6: Water contact angle of the blade coated fluoropolymer layer.

best results reported for the diF TES ADT: PTAA based OFETs [112]. In addition, the bilayer OFETs have demonstrated less variability compared to transistors using only the P(VDF-TrFE-CFE), as can be seen from the coefficient of variance presented in table 2.

To demonstrate device operation at low voltages, we have built an enhancement-load inverter. Two enhancement mode transistors compose the unipolar inverter, one used as driver device, whose gate is the input voltage, and the second acts as a load device. Figure 5.9 depicts the voltage transfer characteristic (VTC) of the unipolar inverter, which demonstrated the low operational voltage of ≤ 8 V. The dc voltage gain of this unipolar

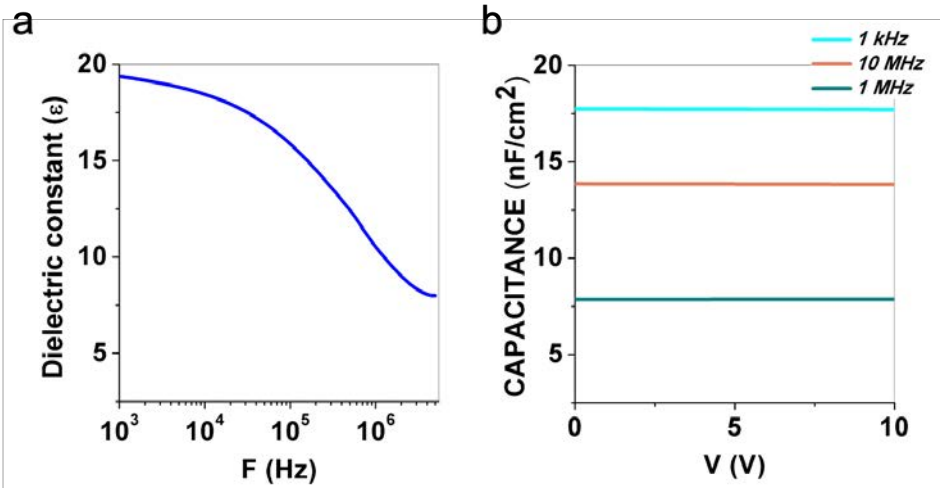

Figure 5.7: (a) Dielectric constant with respect to frequency for bilayer films composed by the low-k fluoropolymer and the high-k P(VDF-TrFE-CFE). (b) Capacitance per area versus voltage for bilayer films composed by the low-k fluoropolymer and the high-k P(VDF-TrFE-CFE)

	SS(V/dec)	V_{th}**(V)**	$\boldsymbol{\mu(cm^2/V.s)}$	$\boldsymbol{log(I_{on}/I_{off})}$
mean	0.71	-1.3	1.3	3.9
SD	0.11	-0.19	0.22	0.04

Table 5.2: Average field-effect mobility, threshold voltage, on/off ratio, subthreshold swing and coefficient of variation for the bilayer OFETs.

inverter, the low and high noise margin at supply voltage V_{DD} of -8 V are 1.2, 56%$\frac{1}{2}V_{DD}$ and 73.5%$\frac{1}{2}V_{DD}$, respectively. The low voltage gain of the unipolar inverter can be attributed to the similar channel dimensions (W and L) and field effect mobilities (μ) of the driver and load transistors, since the voltage gain is given by equation 3.3.

5.5 Conclusion

In summary, low operating voltage printed flexible OFETs using a high-k relaxor terpolymer P(VDF-TrFE-CFE) are reported. We have demonstrated that the mobility of the P(VDF-TrFE-CFE) based OFETs can be increased two orders of magnitude by using a thin layer of a low-k fluoropolymer dielectric layer between the semiconductor and P(VDF-TrFE-CFE) dielectric layer. An enhancement-load logic inverter using the bilayer transistors has been built and has shown operational voltage as low as 8 V. Overall, this work presents process

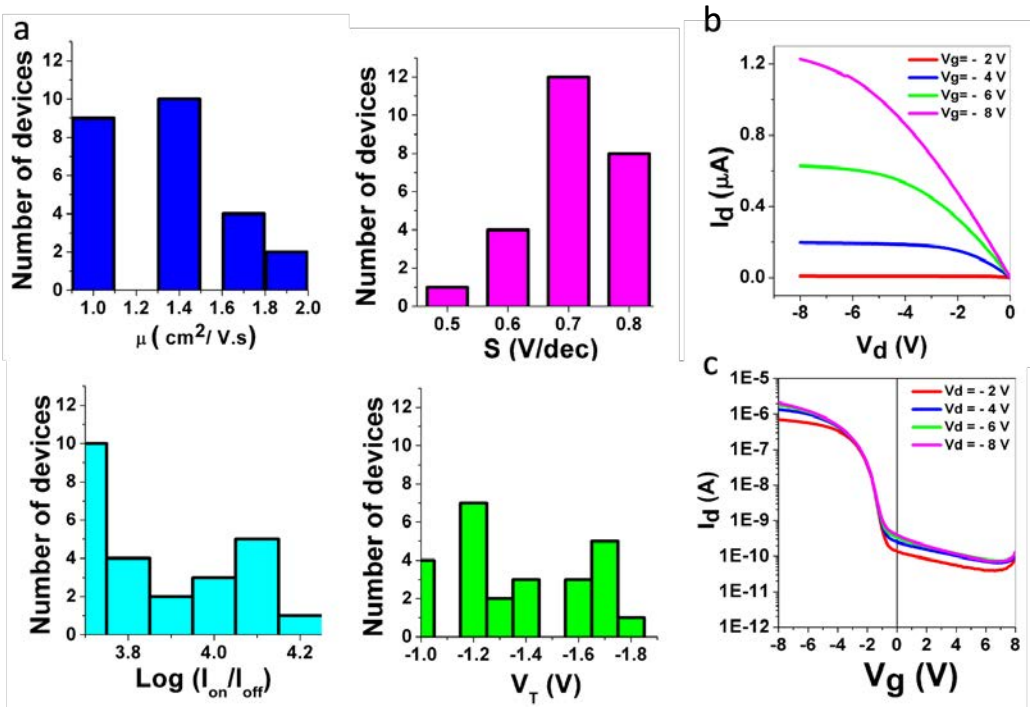

Figure 5.8: (a) Statistical distribution of field-effect mobility, threshold voltage, on/off ratio and subthreshold swing for 25 devices.(b) Typical current-voltage characteristics of a bilayer OFET

for fabricating printable and flexible OFETs that meet the performance and the low power supply requirements of portable circuit applications.

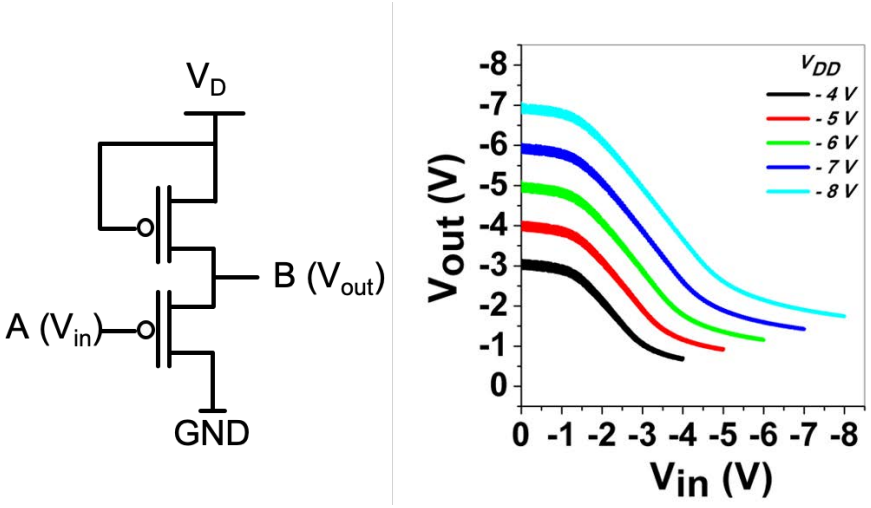

Figure 5.9: Circuit configuration of an enhancement-load logic inverter and voltage transfer characteristic (VTC)

Chapter 6

Sensing System Using Large Area Printed Flexible Organic Electronics

6.1 Introduction

Organic electronics enable scalable, cost-effective fabrication of large-area devices due to the merits of uncomplicated and low-temperature budget processing of organic materials on various types of flexible substrates. OTFTs and OTFT-based large-area sensors are promising for many rising applications with the advantages of lower cost and higher sensitivity, flexibility and biocompatibility. While lower performance and variability are limiting factors for many high-end technologies to adopt OTFTs, their performance can be sufficient for applications where only the high-end information is required. The data from a large array of sensors involves processing and analysis in CMOS side. Data transmission requires a large number of interfaces between the sensor array and CMOS. Large number of connections decreases system reliability while the large-scale raw data analysis is not even unnecessary for many applications. One approach for complexity improvement is interfacing the sensors to the large array of OTFTs to implement simple function processing by only passing the high-level information to CMOS for decision-making using machine learning [144] as shown in the dotted section of Figure 6.1a. Interfacing a large array of flexible organic sensors to OTFT is challenging and affects reliability and circuit robustness. Passing data through interconnections from the substrate of sensors, such as organic photodiodes with low currents, to OTFT substrate deteriorates SNR and requires an amplification stage in between. OTFT-based sensors have the advantage of dual-performance by integrating sensing and function generation (amplification) which incorporates two functionalities performed in two separate substrates in only one. This can result in enhancement of system complexity and fabrication challenges. In this chapter, we start by generating a linear function as a decision boundary using OTFTs discussed in chapter 1 and chapter 2 for weak classification of a specific pattern and then implementing an error-adaptive boosting algorithm for strong classification as shown in Figure 6.1b and c. We use the organic phototransistors (OPTs) as an OTFT-

based sensor to combine sensing and function generation (linear function) in one batch for decreasing system complexity. We show that the performance of organic devices integrated in a system is sufficiently high for decision making using machine learning. OTFT-based sensors are promising for many bio applications and wearable devices. Low cost and flexible large array of organic sensors on the body in assistance with machine learning can be used to do decision making and processing from received signals.

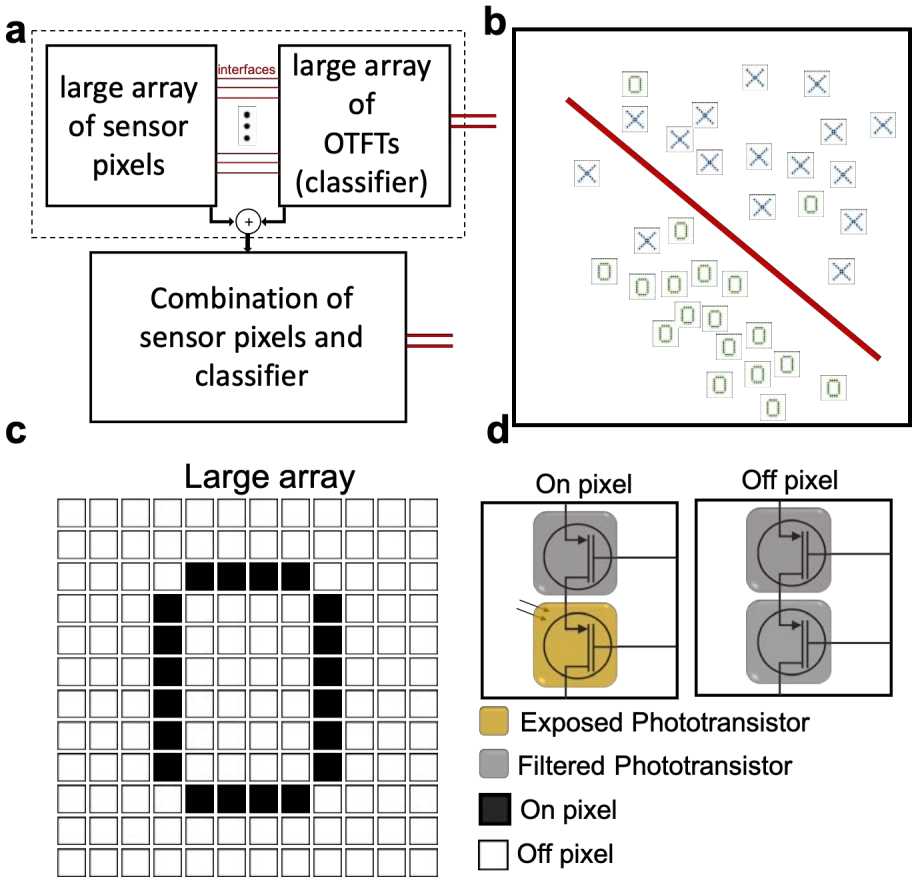

Figure 6.1: (a) The dotted section demonstrating the reduction of the number of interfaces from a large array of sensors to CMOS for processing using organic thin-film transistors (OTFT). Reduction of system complexity by utilizing sensor-based (OTFTs) for combination of sensing and function generation. (b) An example of a linear classifier. (c) An example of a generated pattern with large array of sensors. (d) Demonstration of dual performance of organic photodiode (OPTs) as both sensor and transistor for function generation.

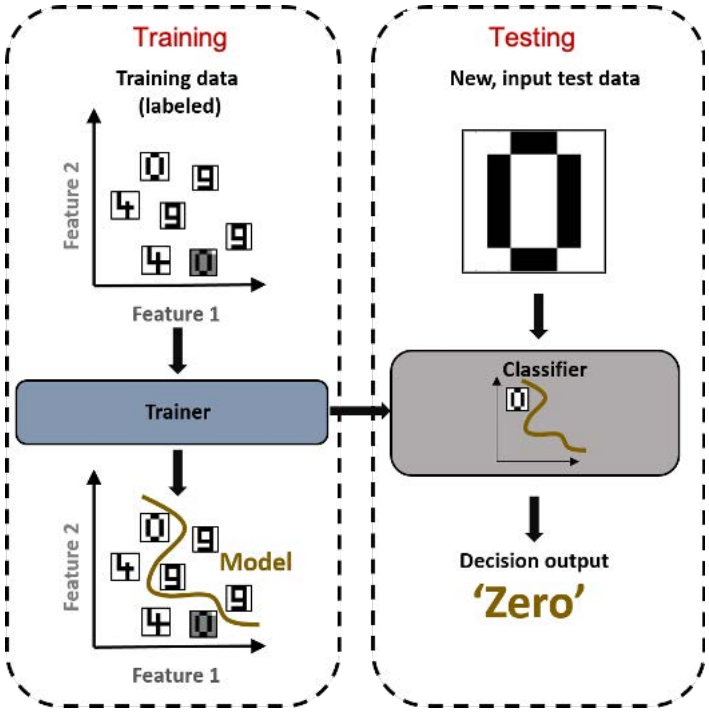

Figure 6.2: The structure of a classification system.

6.2 Classification

The process where we arrange data into specific categories with the intention to secure it and utilize its efficiently is known as data classification. A simplified structure of a classification system is depicted in Figure 6.2. Classification of data not only increases understanding of data but also makes it easier for us to process it by locating and retrieving in a convenient manner. The process includes tagging the data to enhance traceability and eliminate unnecessary storage and transmission costs which leads to higher speed while searching for the data and lower power when transmitting it. Classification can be done on the basis of content, context, and desired application for the users. In order to decrease the number of interconnections between CMOS and the Large Area Electronics domain, an SVM classifier is exploited to output a label corresponding to the input image. Therefore, a single analog output will summarize all of the raw data from the array which will minimize the number of interface connections mentioned previously. To confirm functionality, the model is trained on MNIST dataset with the goal of classifying a specific digit of the dataset from the rest of the numbers. Implementing SVM classification shown in Figure 6.3b on hardware requires implementation of the analog dot product of sensor voltages and the weight values using OTFTs. To address this, we propose a series combination of two OTFTs per each pixel value to accommodate the weights and sensor voltages used in the dot product. To further

improve accuracy, a strong classification algorithm is implemented using the same linear decision boundaries of SVM classifiers [144]. The following section gives a detailed description of implementing the analog multiplier, enhancing its linearity and the classification details of both of the weak and strong learner algorithms.

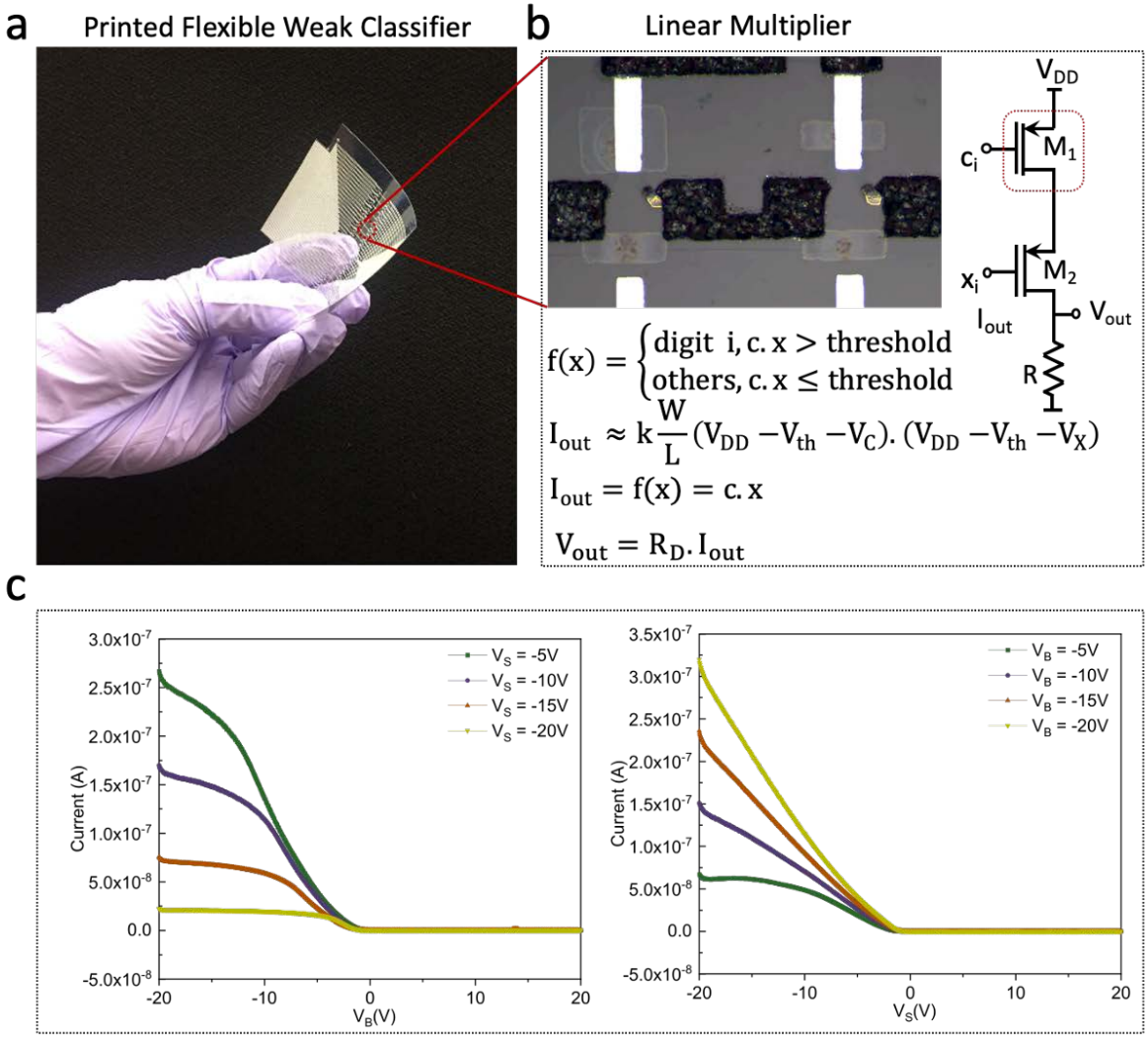

Figure 6.3: Linear multiplier implementation using OTFTs. (a) A printed flexible array of OTFTs.(b) Hardware implementation of the linear multiplier.(c) I-V characterization plots for each linear multiplier. The OTFT inputs V_B and V_S are c_i and x_i accordingly.

Linear Multiplier and Weak Classifier

The circuit shown in Figure 6.3b is implemented for a single series combination of OTFTs and the I-V characterisation plots are used for generating the data for classification which is discussed in the following sections. I-V characterization plots for the top and bottom transistors are shown in Figure 6.3c. For each transistor, the I-V plot is the result of a linear sweep of input voltages to each transistor for four distinctive voltages applied to the adjacent transistor. To generalize the results of Figure 6.3c, we use linear regression to fit a linear function to the output current for the linear operation range of voltages. As shown in Figure 6.3c, the output current demonstrates a more linear behaviour for the bottom transistor, making it a better candidate to support pixel values coming from the photodiodes to preserve linearity while weight voltages are applied to the top transistor. To ensure linear operation the sensor data and the weights are normalized and scaled before applying them to the multiplier circuit. The details of deriving the output current are shown in Figure 6.4. In Figure 6.4, V_X and V_C refer to the input and weight voltages respectively. G_m is the trans-conductance of OTFT devices and is defined as the ratio of changes in output current divided by changes in input voltage values and can be computed from the slope of the current characterization plots shown in Figure 6.3c.

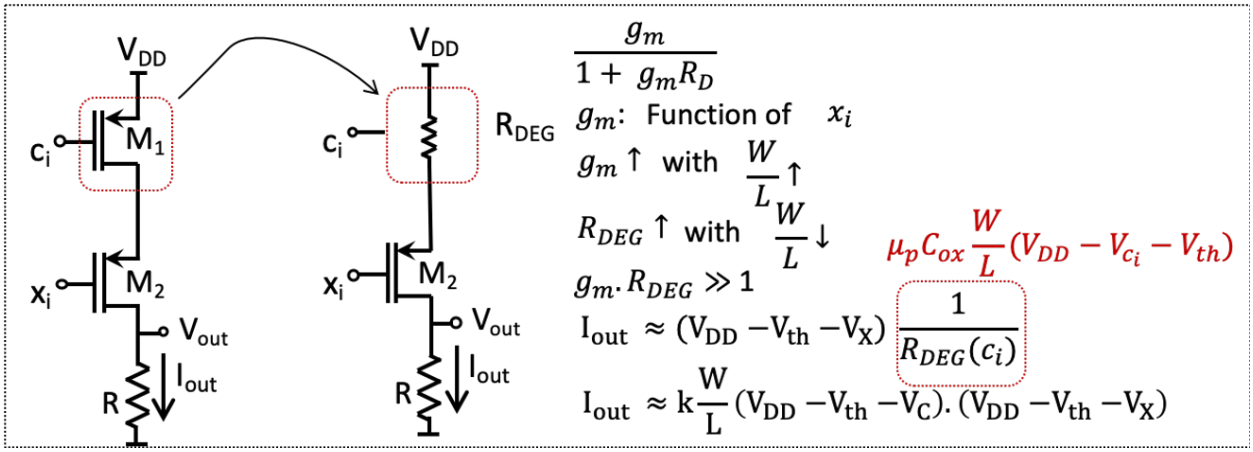

Figure 6.4: Output current derivation for the series combination of OTFTs

Linearity Enhancement of OTFT-Multiplier

Modeling the accuracy of the hardware implementation of SVM relies heavily on the quality of the linear fit. This requires operation of OTFT-M_2 (sensor input) and OTFT-M_1 (weight input) in saturation and linear region accordingly. Figure 6.4 describes the improvement of the linearity through the modulation of the scale ratios of the two transistors. Increasing the scale ratio of OTFT-M_2 results in increasing g_m which causes the gain to be proportional

to $1/R_{DEG}$. To increase $1/R_{DEG}$, OTFT-M_1 is kept at the smallest scale ratio, resulting in the linearity improvement. As explained in chapter 2, we introduced a method for scale ratio tuning of devices along with the large array. Figure 6.5 depicts the improvement of linearity by increasing OTFT-M_2(sensor input) scale ratio and keeping OTFT-M_1 (weight input) scale ratio constant.

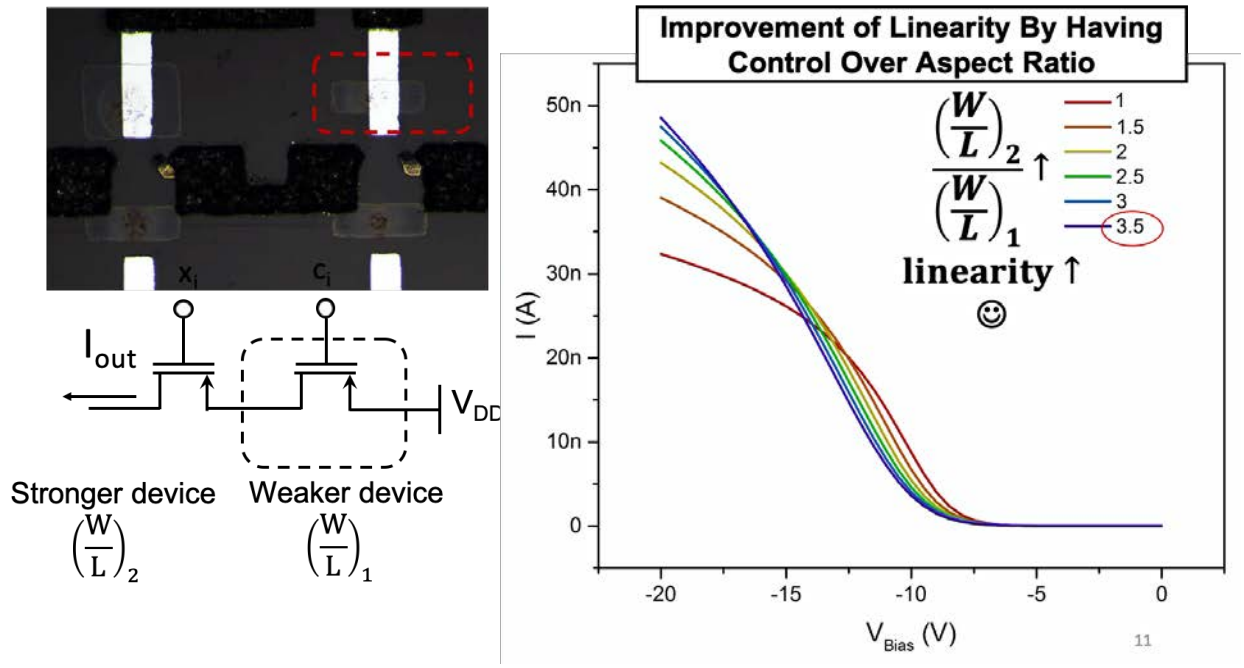

Figure 6.5: Improvement of linearity by controlling and changing the scale ratio of organic thin-film transistors in the linear multiplier.

Hardware Implementation of the Weak Classifier

The circuit shown in Figure 6.3b implements the dot product only for positive weights. To adjust the multiplier for accommodating negative weights the top OTFT device in Figure 6.3b is replaced by a differential pair with the input signal connected to both of the following cascade devices. This results in a differential output current with the same polarity as the classification weight for each OTFT pair.

Finally, an array of 28×28 multipliers each consisting of a series combination of OTFTs is simulated in python using the linear fit coefficients derived from the I-V characterization plots shown in Figure 6.6. The output currents from all of the differential pairs are summed up resulting in a single output voltage while passing through a linear resistor R. The details of circuit implementation of the array are shown in Figure 6.7.

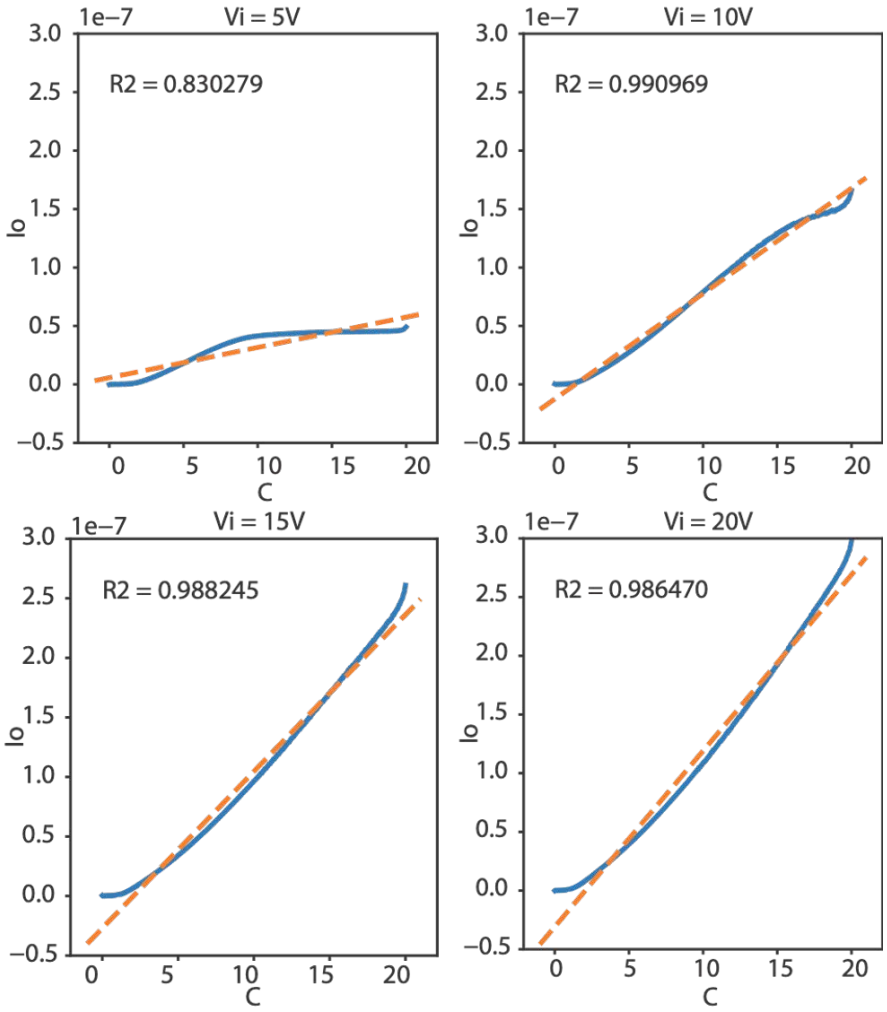

Figure 6.6: Linear Regression for I-V characterization plots

Weak Classification vs. Strong Classification

Generally, weak learners have either linear or nonlinear boundaries based on the specific application and available data. The proposed weak classifier's performance is limited due to the linear boundaries resulting from using the linear multipliers. Strong learners can further improve accuracy by exploiting ensembles of these weak learners without changing the core of the hardware implementation. Figure 6.8 compares the two models for classification of a two-class data. The yellow line in Figure 6.8a imposes a linear decision boundary which results in misclassification of many data points due to the high classification bias of the linear model for the data which is not linearly separable. As shown in Figure 6.8a, a nonlinear decision boundary results in a more accurate classification. However, Figure 6.8c shows a strong

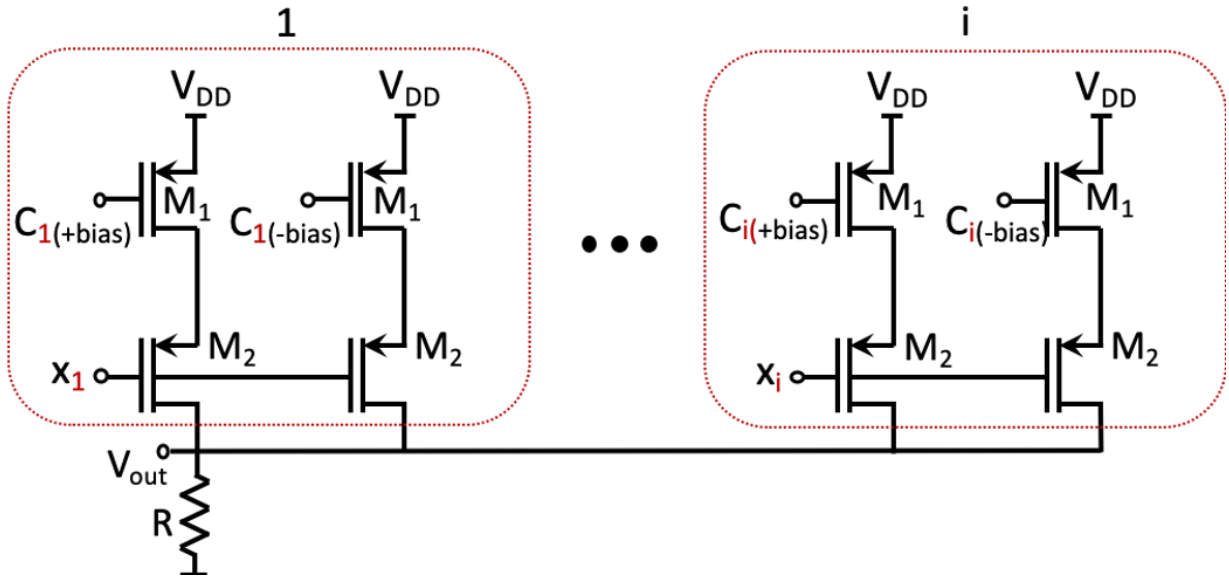

Figure 6.7: Hardware implementation of the array of multipliers

model that separates two classes by using ensembles of these weak learners. Strong learners achieve higher accuracies by combining predictions of the weak classifiers which might be restricted to the form of their decision boundaries. Another important advantage of an ensemble learner is lower sensitivity to data variations and outliers by averaging the outputs of different learners. It can be shown that a sufficiently large ensemble of weak learners leads to approximately 100% accuracy even for weak learners accuracies slightly higher than 50% resulting from random guessing. Considering binary classification, if a dataset consists of two classes with an equal split for the data points between each class, random labeling results in an accuracy of 50%. If a weak learner manages to perform better than 50% accuracy, a boosted learner can use a weighted sum of weak classifiers to perform efficiently with higher accuracy while having the ability to fit the data. Boosting is a process of transforming weak learners into strong classifiers using supervised learning by exploiting various weak learners and averaging them to reduce bias and variance. The motivation behind boosting is to create a strong classifier where predictions of many weak classifiers are combined to produce a stronger model to fit the data. Figure 6.8 shows the structure of the Adaptive Boosting algorithm where each of the weak classifiers votes for the final output of the meta-learner with a weight proportional to its performance in classifying the training data [26]. Feature vector x combines linearly with the weight vector c under linear classification after which the weighted sum of the feature is compared with a threshold leading to predictions in the form of binary output. Boosting is generally considered as a method with the ability to convert a broadly practiced principle into a rule of highly accurate predictions. The error

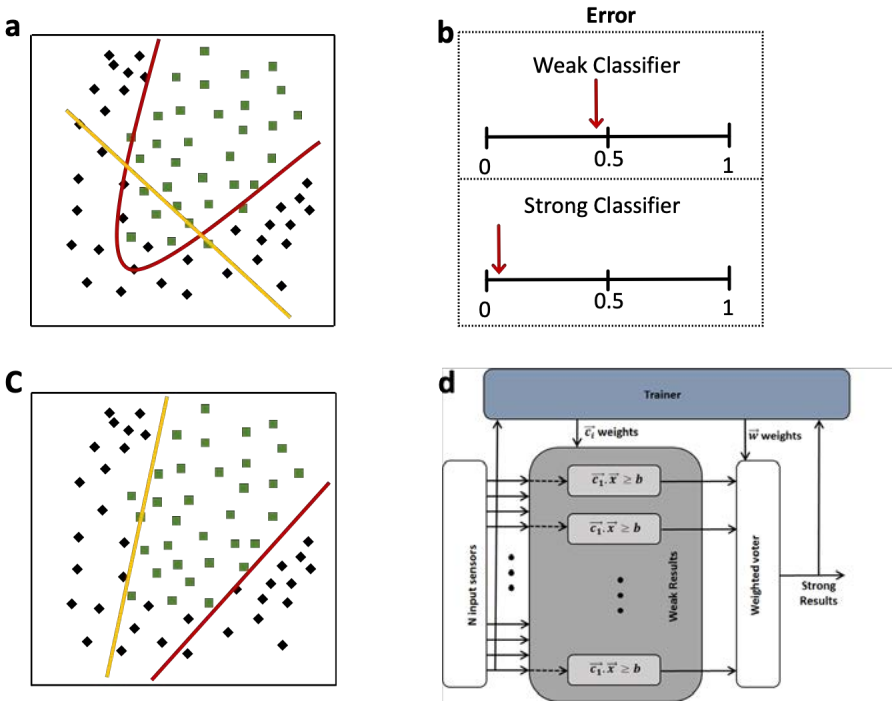

Figure 6.8: (a) Linear vs nonlinear decision boundary (b) error rate comparisons for the weak and strong classifier (c) Adaptive boosting for the linear classifiers and (d) algorithm structure resulting in strong classification by summation of the linear boundaries.

rate produced after applying boosting is extremely low due to the effect of averaging on variance for each weak model and it can be implemented on actual hardware even if the initial model does not result in high accuracies. Generally, adaptive boosting algorithms are applied to decision trees where they combine predictions of various classifiers iteratively by assigning larger weights to those classifiers that provide more accurate predictions. After every iteration, the algorithm increases the weights of misclassified sample points. At the end of training, more accurate learners get bigger votes for the final prediction. Error adaptive Classifier Boosting algorithm (EACB) has a similar structure to Adaboost with the additional capability of taking the hardware non-linearities of OTFTs into account. The original Adaboost algorithm trains multiple weak classifiers and combines them by taking a weighted sum of each weak-classifier's output. EACB is useful when the only available base algorithm is weak and not very accurate. This is necessary in this case, since the TFT hardware can only support a non-ideal dot product classifier [115, 147].

In EACB, the training data is divided into different segments. Each weak classifier is trained on its assigned weighted training tranche with weights corresponding to the importance based on how accurately the previous weak classifier would evaluate the data. The first weak classifier gives all input vectors equal weights while the subsequent classifiers adjust the

weights according to the prediction accuracies while the algorithm iterates over the number of weak classifiers.

Classification Results

To test SVM on our proposed hardware, digit seven is chosen as the classifier's preferred True output and the rest of MNIST dataset is associated with False labels. Due to non-idealities in linear approximation for the output current of OTFTs, hyperparameter tuning is required to specify the optimum threshold voltage in Figure 6.3b for assigning the predicted labels. The right plot in Figure 6.9b shows training and test accuracies for different threshold voltages for an output Resistance of $2K\Omega$. Increasing the value of R increases the magnitude of threshold voltages resulting in a more robust classifier to circuit variations. A maximum testing accuracy of 78% can be achieved using our proposed hardware implementation. To improve accuracy we employ a boosted classifier using EACB which was discussed in detail in the previous section [115, 147]. As shown in Fig.6.9a increasing the number of weak classifiers, improves the overall training and test accuracy of classification for a fixed threshold voltage used in predicting the output labels as discussed previously. According to the left plot in Figure 6.9b, employing EACB achieves training and test accuracies equal to 93% and 89% which is a more than 10% improvement over the weak linear classifiers. Applying a boosted SVM to the sensor data enables us to decrease the number of interconnections between CMOS and Large Area Electronics domains to only one output voltage corresponding to the label of the initial image instead of 28×28 raw pixel data from the sensors.

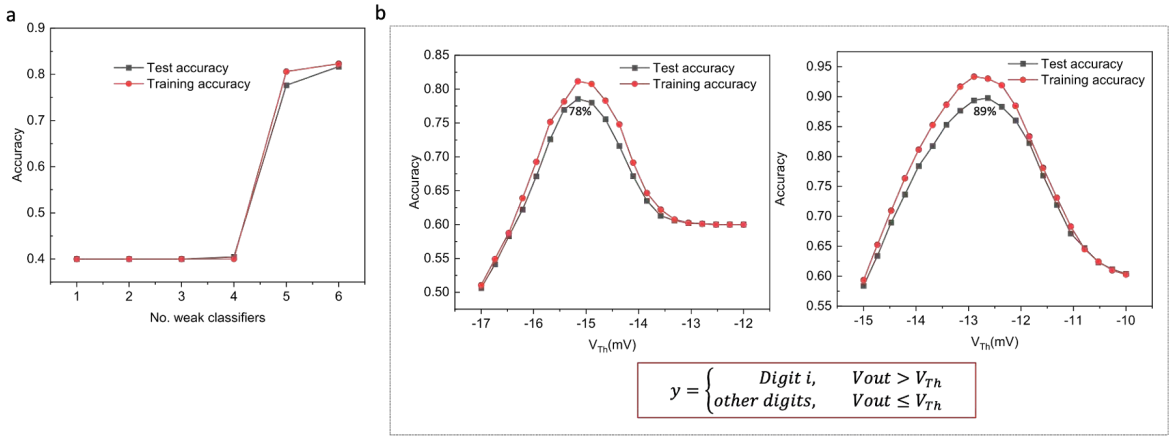

Figure 6.9: Training data and testing data accuracy for the weak and strong classifiers

6.3 Sensing System Using OPTs

Array Fabrication

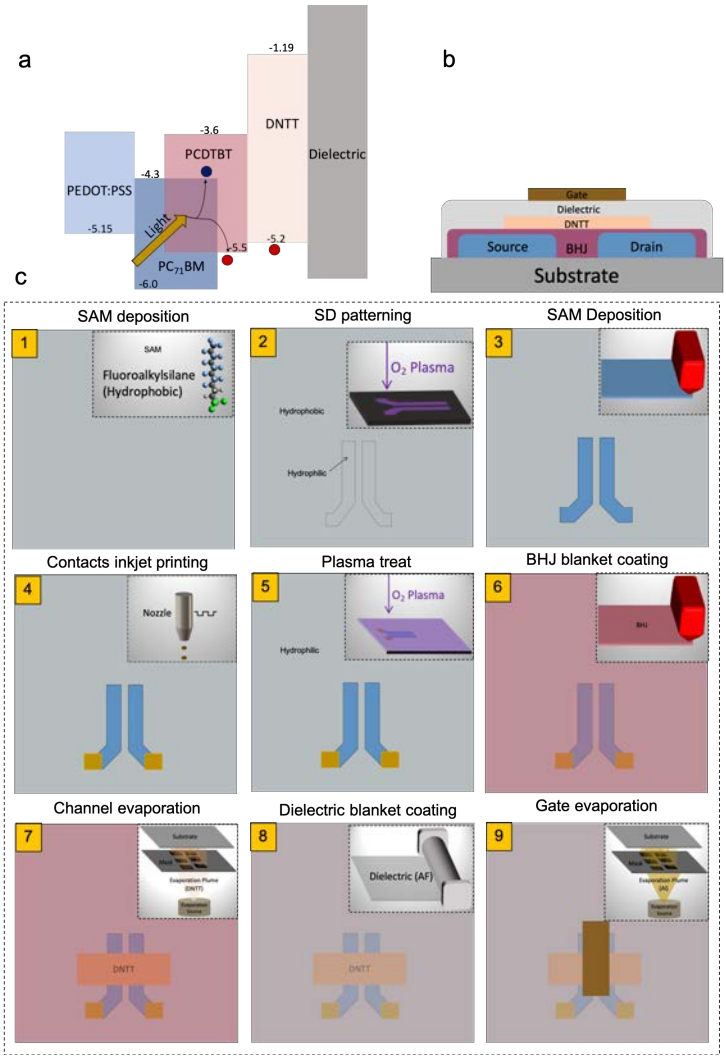

Figure 6.10: (a) Band diagram of the organic phototransistor (OPT) channel. (b) The cross section, and (c) fabrication process flow for the OPT device.

Figure 6.10c depicts the fabrication process flow of an array of OPTs using the same device design explained in previous chapters. The source and drain electrodes are surface energy patterned and blade coated on the flexible substrate following by inkjet printing of the contacts. The substrate is plasma treated to remove the former deposited hydrophobic to enable the blade coating of the $PCDTBT : PC_{71}BM$, which is a bulk-heterojunction

(BHJ) with a broad absorption and high internal quantum efficiency [110, 111]. The organic

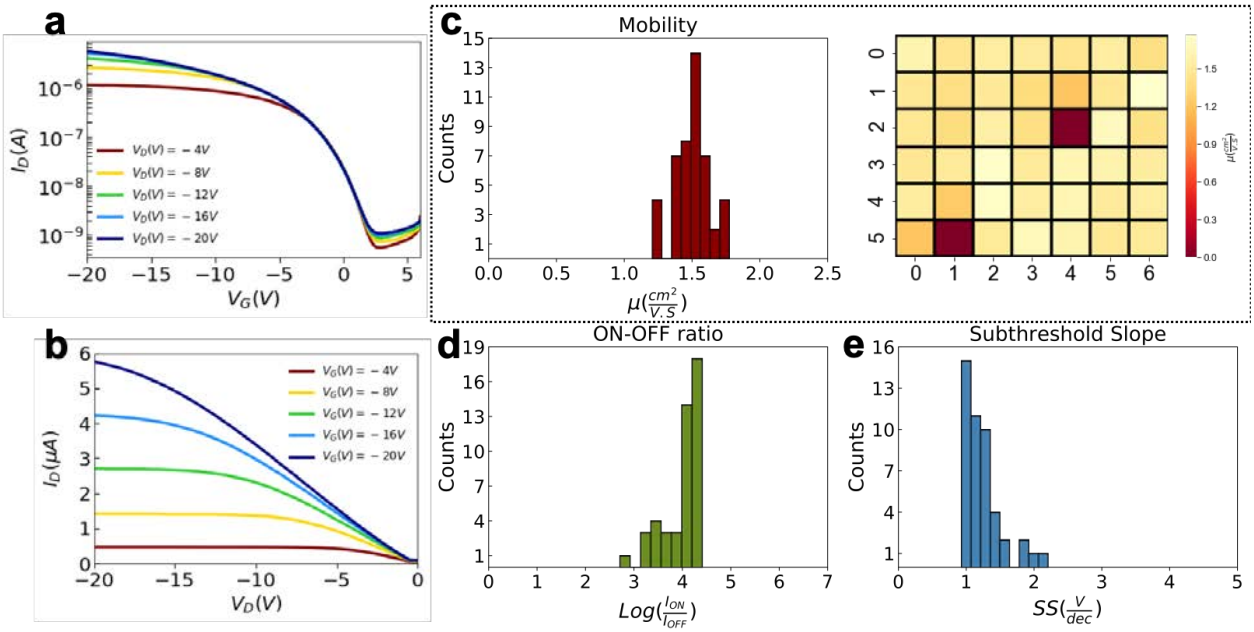

Figure 6.11: (a) Dark transfer characteristics, and (b) output character of an organic phototransistor device. Statistical distribution of (c) mobility, (d) ON-OFF ratio, and (e) SS of 42 devices.

semiconductor dinaphtho[2,3-b:2',3'- f]thieno[3,2-b]thiophene (DNTT) is thermally evaporated forming an heterojunction layer. The gate dielectric (AF) is coated on the whole array followed by Al gate evaporation. Figure 6.10b shows the corss-section view of the device structure. The heterostructure of the OPT channel consisting of the semiconductor DNTT and the $PCDTBT : PC_{71}BM$ is depicted in Figure 6.10a. The photo-generated hole in the HOMO (highest occupied molecular orbital) of the $PCDTBT$ level can get into the DNTT due to the energy matching of the two layers. However, the existing energy barrier in LUMO (lowest unoccupied molecular orbital of $PC_{71}BM$ and DNTT blocks the entrance of photo-generated electrons in to the semiconductor layer. The electrons are minority carriers with life time of τ_n and holes are majority carriers with transient time of τ_t. The charge carrier selectivity in these OPT devices results in high photo-conductive gain dependent to ratio of the τ_n to τ_t. [111].

Array Interconnection

This section investigates the employed methods and required optimizations for the interconnection of OPTs and OTFTs in a large array to form circuits (classifier and the FFC/FPC

connectors for connection to the PCB board). The conductive interconnection layer is fabricated and shown using two methods of screen printing and evaporation. The dielectric insulation layer between the two conductive interconnecting layers is done with screen printing. The interconnection printing method should be adaptable to the printed beneath layers and do not affect the device performances. The solvents of the printing method should be insoluble in the gate dielectric layer. The silver ink used in the screen printing method is adaptable with the amorphous fluropolymer (AF) used as the gate dielectric. In screen printing, the snap-off distance and the squeegee pressure are two critical parameters to consider. The squeegee pressure can result in gate leakage on the array of OTFTs due to the rough surface of the crystal channel (diF:TES:ADT) penetrating through the dielectric. The gate dielectric thickness was increased along with the optimization of the squeegee pressure to avoid shorting. In the OPT case, the shorting effect was not seen due to the smoother morphology of the DNTT film. In high squeegee pressures, the mesh pattern transfer is visible on the gate dielectric layer and the Al gate electrode. In larger snap-off distances, the gap between the screen and the substrate, the applied pressure from the squeegee is not sufficient and can result in incomplete patterns in the array. Also, screen tension is higher in the larger snap-off distance, which results in damaging and flaking the previous prints on the substrate. For lower snap-off distances, the screen adheres to the substrate due to the high surface tension of the ink after the ink transfer by the squeegee. The separation of the mask results in ink dispersion. For the screen printing of the array of OPTs and OTFTs, the optimum squeegee pressure to result in favorable print is 30N and 1.7mm accordingly. The print and flood speed are both set to 60 mm/s, applied in the printing of both the conduction (silver) and the insulating layer (dielectric). One of the main challenges confronted during screen printing is the fast ink solvent evaporation and clogging the openings. The blocked features prevent the transfer of the ink for the next prints. This effect occurs more often in masks with small feature sizes. If the time between the test prints for the alignment and the prints are not short enough, the ink dries, and the screen attached to the screen holder can be taken out of the screen printer for the cleaning and returned while keeping the alignment state. However, the detachment from the screen holder's mask changes the alignment, and the process should be initiated from the beginning. The drying issue can be improved by quickly flooding the screen after each print run. Figure 6.12 summarizes the interconnection procedure of devices. We fabricate the OPT classifier sensors with two different methods. In the first method using screen printing, the array of devices are exposed to 5 seconds of plasma before the start of the interconnection process. The air plasma improves the wettability of the silver ink on the gate dielectric (AF) layer. The deposition of interconnection layers requires a precise alignment due to the small feature sizes using the alignment marks. The insulating dielectric square (blue square in Figure 6.12a) is screen printed over the first conductive layer to prevent shorting. The square dielectrics are large enough with the safety margins to avoid possible shorting from misalignment imperfections. Finally, the last screen printing layer is screen printed which has some part of interconnection and the FFC/FPC connectors lines. In the second method, the interconnection lines are Al-evaporated with the same design. The first conductive layer, is merged and combined with the gate evaporation

step. The mask has the gates and partial interconnections. The insulating dielectric square is screen printed over the first layer, following by evaporation of the last conducting layer. However, the last layer evaporation should be done in three steps to achieve about a 300nm thickness to cover the shadowing effect in the edges of the screen-printed square patch and form a conductive line passing on top of the dielectric. The photograph of a fabricated flexible classifier is shown in Figure 6.12c. As was explained before and previous chapters, the gate dielectric layer is blanket-coated on the whole array after the deposition of source and drain Ag contacts. With thin contacts, there will be no connection between the contacts and the interconnecting layers. However, the Ag inkjet-printed contacts are thicker than the dielectric layer, penetrating through forming conductive vias to the interconnection layers. The classifier's OPTs were characterized by contacting the probes to the interconnection layers far away from the source, drain, and gate electrodes to check the fidelity of the fabricated interconnection layers. The characterization of the devices with the derived characteristics are depicted in the Figure 2.5.

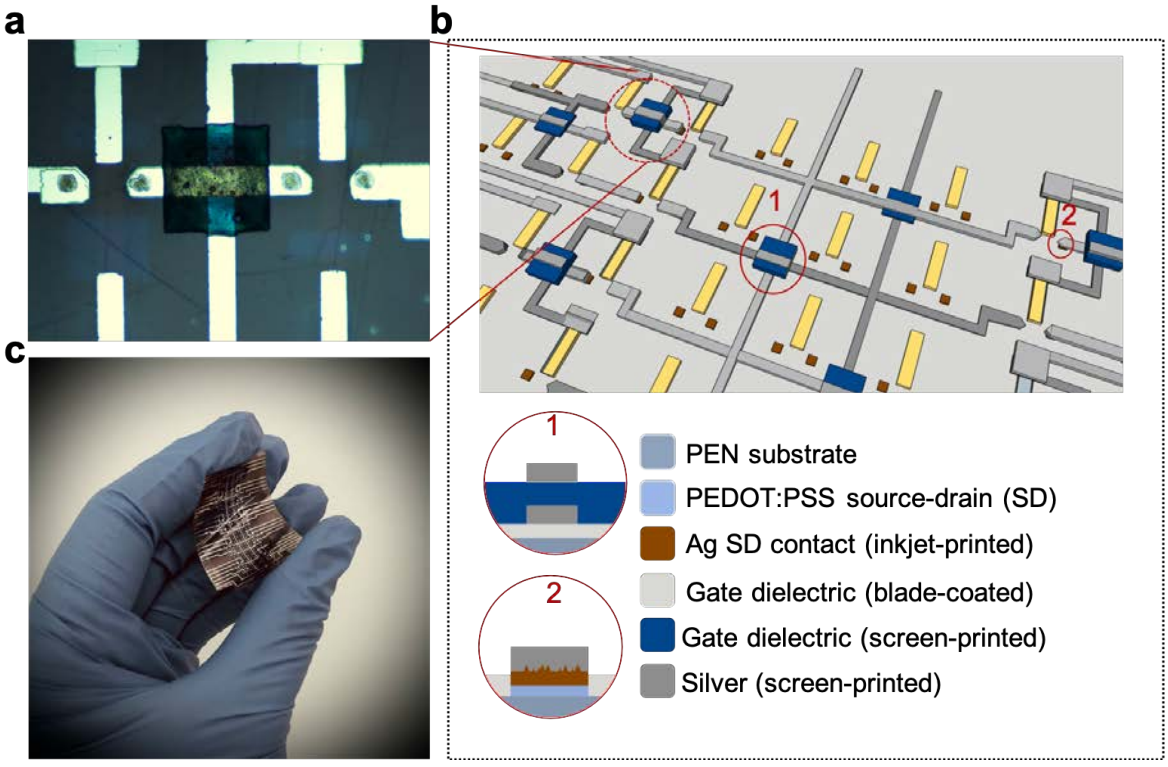

Figure 6.12: (a) Optical micrograph of a portion of interconnected devices with the two layers of conductive and an insulating layer in between . (b) Interconnection process of large array of organic devices. (c) Photograph of a flexible OPT sensor and classifier.

System Integration

On the main board, there are 2×5 column and row-addressable pixels, each as a separate controlling module associated with every unit in 2×5 linear multiplier in classifier and sensor array. As shown in Figure 6.15c, each pixel structure on the board contains potentiometers (POT-1 and POT-2), and selects for addressing each pixel in the array and digital potentiometer access. POT-1 is used for applying the multiplier coefficient-input voltages $V_{(b-)}$ and $V_{(b+)}$ to M1 and POT-2 for applying V_s to the OPT used as sensor (M2). For the final readout, all the outputs coming from all the pixels are combined in to one input to a transimpedence amplifier (TIA) converting the current to voltage and then feeding to ADC to digitize the signal. As shown in Figure 6.13, forcing the drain node of M2 in linear multipliers in series at the ground using TIA improves the linearity of the multiplier and as pixels are decoupled the classification algorithm can be more relaxed. This design was adopted over another design which is connecting the drain node of transistors in to a resistor [115] and the downside of this design is as the input voltage to M2 increases, the voltage at the drain node of M2 can decrease which results in pushing the M2 into triode region which is non-ideal.

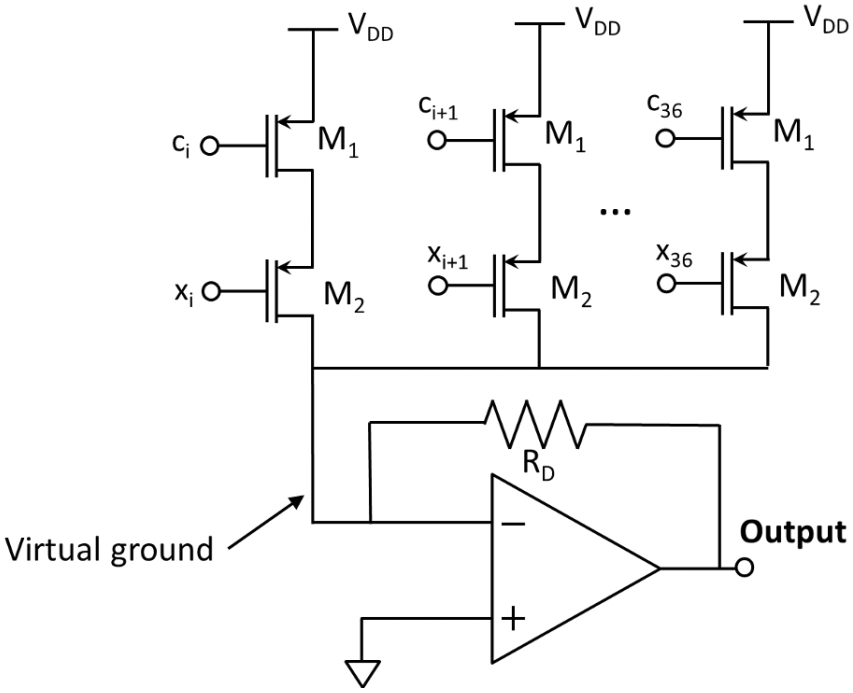

Figure 6.13: Use of Trans-Impedance (TIA) fixing the drain of M_2 to the ground and in saturation mode. In this case the pixels are decoupled and can help with reduction of complexity in algorithm.

The potentiometers in the board are controlled by a micro-controller which is the interface

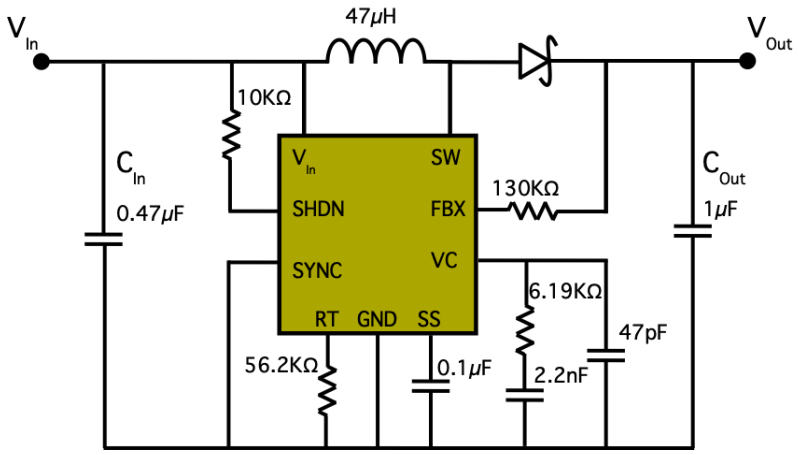

Figure 6.14: DC/DC boost converter, 5V to 12V

between the computer and the board. The whole board is powered by a USB using DC/DC converter (5V to 12V) in the board as shown in Figure 6.14. The flexible printed classifier is connected using FCC and FPC connectors as shown in the Figure 6.15a and b. We characterized the pixels in both dark (Figure 6.16(a)) and bright (Figure 6.16(b)) conditions. In each case, the gate voltage of M1 (V_B or the coefficients) and M2 (V_S or the sensor reading) were swept by setting the digitally-tuned potentiometers through the computer interface, and the output voltage was read through the ADC. These plots illustrate the linear behavior of the OPTs for 5 measurements per each dark and bright conditions. Note that in this case, the channel for both M1 and M2 were exposed to the light. However, in the actual use-case of a linear classifier, the coefficients are determined during the training phase and will stay constant afterwards. Therefore, a filter will be printed on the channel of M1 to protect it from the changes in light (Figure 6.16(c)).

6.4 Conclusion

Large-area organic electronics provide advantages such as cost and processing on various materials. While the devices suffer from variability and lower performances, they can be adopted in many rising applications for which the performance is sufficient, and flexibility and cost benefits are needed. For many large-area applications, only the high-end information is required. In this work, we fabricated a linear multiplier using OTFT and showed the classification of the numbers. This proved the sufficiency of OTFT performance for utilization in a large area system. A large array of OTFTs can be used as a processing section which receives the signals coming from the large area of sensors and passing the high-level information to the computer. This can result in the reduction of system complexity. We demonstrate techniques for the fabrication of printed organic classifiers and interfacing with

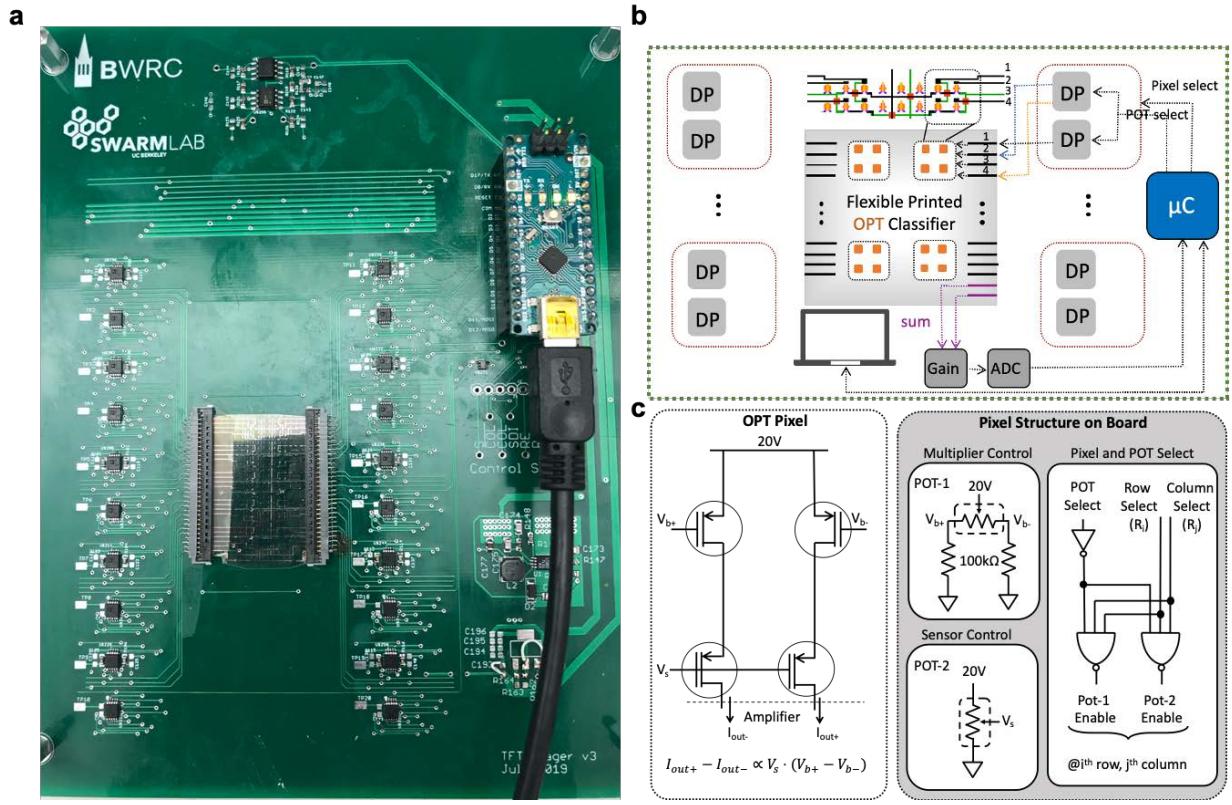

Figure 6.15: (a-b) classification set up: the flexible classifier is connected to a control board with column and row-addressable pixels. (c) The schematic of each pixel on the board.

a control board. We utilize and show a system for the reduction of system complexity by adopting the OPTs, which can combine the action of sensing and the function generation.

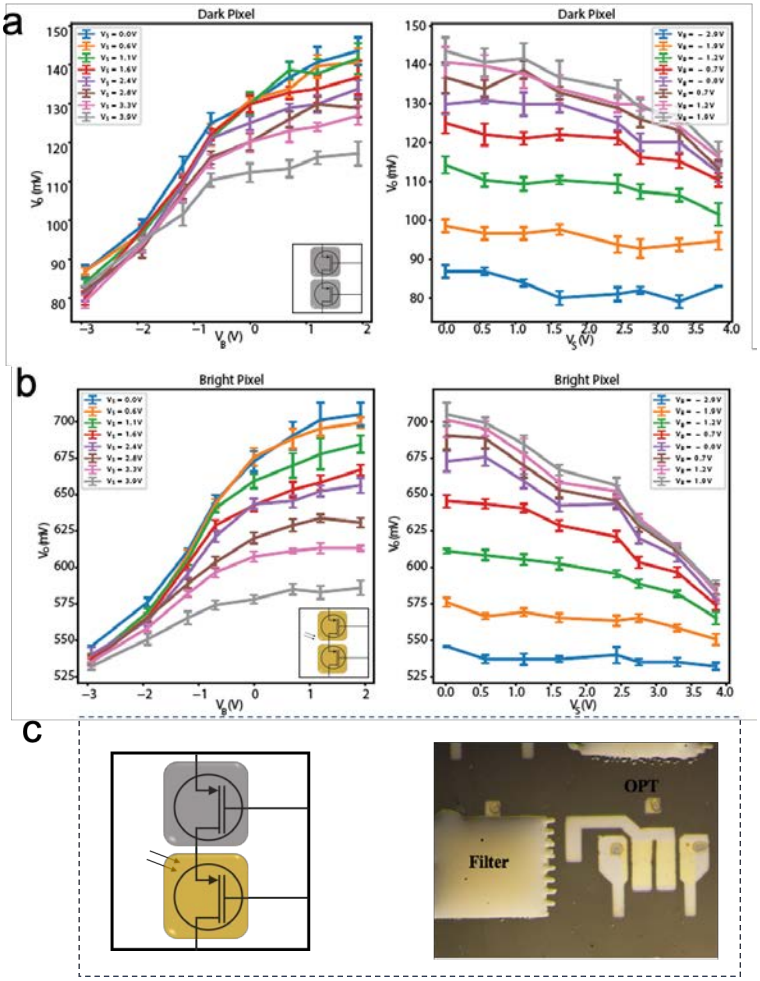

Figure 6.16: Combination of sensing and classification: linear multiplier characterization plots of (a) dark pixel and (b) bright pixel. (c) The optical microscopy for an inkjet-printed filter on the back of the substrate for the phototransistor to behave as a transistor and the adjacent phototransistor exposed to light to behave as a sensor.

Chapter 7

Conclusion and Future Work

This thesis primarily focuses on the fabrication and optimization of large-area organic thin-film transistors and phototransistors and using them for circuits and system levels. The low thermal budget printing methods on various substrate materials enable large-area manufacturing of devices at lower costs not possible by expensive microfabrication processing techniques. OTFT technology continues to advance, and the possibility of fabrication on a wide range of polymeric materials facilitate new applications with the vision of flexibility.
At the early stages, the focus was to establish methods for the development of flexible printed OTFTs, as shown in chapter 2. The large-area devices are fabricated using a novel printing method that combines surface energy-patterned (SEP) and doctor blade coating to form uniform thin films [109]. There was performed a significant study to optimize the source and drain geometry to maximize yield. The semiconductor blend of small-molecule and polymer show better results in better performance of OTFTs with no notable contact barrier, high on-off ratio, and high mobility. This method shows
The scale ratio of OTFTs is one of the crucial variables for circuit design. The control and change of this variable in a large array of devices can be challenging using printing techniques. Chapter 3 investigates a method for change of scale ratio by the increase of the source and drain width and change of the semiconductor channel on top. We also introduce a method for the interconnection of devices to form logic circuit designs in a large array.
Chapter 4 introduces a method for the digital tuning of the scale ratio of devices in the large array. The digital on-demand inkjet printing of contacts on the discrete source and drain electrodes enables the rapid change of scale ratio of devices based on the required circuit design.
One of the topics to investigate and improve for OTFTs is the reduction of the operating voltages and power consumption accordingly. The low operational power can be obtained by the use of materials with higher dielectric constants and reduction of the dielectric layer thickness. The reduction of thickness increases the risk of leakage, and the use of high-k dielectric directly on the semiconductor channel deteriorates carrier mobility. The mentioned issues can be resolved by the adoption of a bilayer gate dielectric structure, as investigated in chapter 5. The use of a thin layer of the low-k polymer at the interface of the semicon-

ductor channel eliminates the dipole effect, and reduction and addition of high-k results in an increase of the capacitance.

Chapter 6 concentrates on the utilization of the large array of OTFTs introduced in the previous chapters at a system level for data classification. The use of a large array of TFTs benefiting from lower costs of fabrication can result in the improvement of system complexity by the reduction of the number of interfaces from the sensors to the CMOS [115]. The large array of TFTs can only pass the higher level of information to CMOS with the help of machine learning. In this chapter, we use a large array of fully printed OTFT-classifier for data classification. We also introduce a method for further reduction of system complexity benefiting from the dual-performance of the phototransistor for both function generation and sensing.

It is important to investigate methods for further reduction of the channel length. The masks used in this thesis limited us for the improvement of the scale ratio of devices. The use of higher resolution masks can improve the channel length and the performance of devices. As small-molecules and polymers continue to advance, future works require the development of OTFTs using new materials. This applies to the gate dielectric materials as well for the power and speed improvements. One of the ways we considered was the use of laser for high-resolution patterning of the source and drain electrodes instead of plasma treatment to improve the channel length. System robustness is one of the concerns using fully printed flexible electronics. For the first time, we initiated using fully printed OTFTs at the system level. Organic electronics are beneficial for wearable and sensing applications, and the use of machine learning can both help with the prediction and improvement of the performance. In this thesis, we started using fully-printed OTFTs in a system as a proof of concept. OTFTs show sufficient performance for sensing applications integrated into a CMOS system. Phototransistors and sensor-based OTFTs, in general, can combine the performance and sensing and function generation, which is beneficial for system complexity reduction.

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