

# PCB-less Integration of a Robust Wireless MEMS Tactile Package

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PCB-less Integration of a Robust Wireless MEMS Tactile Package

by

Dillon Acker-James

A thesis submitted in partial satisfaction of the

requirements for the degree of

Masters

in

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in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Kris Pister, Chair

Professor Eric Paulos

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## Abstract

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Creating a wireless tactile actuator the size of an aspirin will allow for more precise physical stimulation. This will lead to a more immersive virtual reality (VR) experience and better convey information via touch. Making this wireless tactile actuator can be accomplished by further utilizing the existing Si on Insulator (SOI) structure. Currently, a printed circuit board (PCB) is used for the sole purpose of assembly, however, further utilization of the Micro Electromechanical Systems (MEMS) SOI structure can allow the chip to operate as both the actuator and housing package. In addition, the MEMS Si could replace circuitry previously incorporated in external components: lateral relays replacing high voltage buffers. The assembly of electronics into a MEMS housing was found to require finer assembly tools, lateral SOI relays to control the MEMS devices showed a need for a more durable contact material, and fabrication methods to enhance MEMS robustness are presented. These are meant to enable a durable aspirin-sized package to controllably stimulate the human skin.

Find what you enjoy doing and go do it.

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# Chapter 1

## Integration to Create a Wireless Tactile Stimulator

### 1.1 Vibration: The Most Common Tactile Stimulation Method

Our world is constantly vibrating. This is not a reference to the constant movement of atoms due to thermal energy, but rather the smartphones that are never too far away. Vibration motors are standard in all smartphones, in fact it would even be strange if one did not come with that feature. The first time tactile stimulation was widely used in electronic notification was in the 1950's with Motorola pagers to alert the wearer without disturbing others; the devices were everywhere, even used by emergency response, and the technology was borrowed by emerging electric toothbrushes [6]. Two decades later, Thomas Shannon was granted the first US patent for tactile telephones in 1973, and now they are not just standard in phones, but each smartphone has multiple vibration motors. But in 1995, Geir Jensen illustrated the idea of a haptic wristwatch, Tap-in, where the device had a unique poking pattern for defined callers. It could even facilitate the user to reply with a set of selected short messages. However, the project was not pursued or published until 2015 - the same year Apple started selling a wristwatch that included skin tap alerts to the user [17].

Though commonly used for notification, haptic devices are also used to immerse the user in other worlds. For decades, Disney has been using a combination of haptic actuators to create more immersive rides and shows. In conjunction with visual and audio stimulation, there are tactile simulators incorporated into the system to create more immersive experiences [7]. However, these actuators are still vibration-based, thus limiting the amount of sensations that are able to mimic due to the large location a vibration motor stimulates. With the prevalence of tactile stimulators based solely on vibration actuation, new methods, more precise methods, of touch actuators are needed.

## 1.2 A More Precise Method of Tactile Stimulation

Rather than a spinning weight causing vibrations, a more precise method of stimulation can add a different gadget to the to the toolbox of haptics engineers: creating a poking wireless tactile stimulator the size of an aspirin. Humans have five senses, of which only three are widely used for stimulation from electronics: sight, sound and touch. A variety of sights and sounds can be generated and programmed, not just by engineers who make them, but by the users themselves: phones, electronic watches, cars, etc. can all have customizable notifications. However, the only physical sensation electronics really use is vibration. Imagine all of the different physical surfaces touched in a single day. Mimicking those to create a more realistic virtual reality, for example, will require more precise stimulation than just vibration. Investigating other ways to electronically control tactile stimulation is critical to better communicate information via touch.

When operational, a wireless aspirin-sized poking device could be utilized in a myriad of ways, especially with arrays of them are linked to create more complex sensations. In virtual reality (VR) applications, the added functionality of a suit of wireless tactile stimulators has impactful possibilities. Used in conjunction with the widely-popular vibration motors, arrays of pokers could further add to linking the physical with virtual worlds. This potential, though extremely useful for, goes beyond the entertainment industry. With an overwhelming amount of sights and sounds sometimes overstimulating the daily senses, incorporating more precise tactile feedback can aid in the completion of more complex tasks. For example, remote operation of a surgical robot. With the development of robotics along with remote control, video game-like consoles can be used for more than just entertainment. In this situation, a vibrational notification, like getting too close to an artery, may increase the difficulty of the user to accomplish the task due to the large area vibration stimulated. Whereas a single poke, or multiple pokes, in defined patterns may relay the information in a more subtle and useful way.

One method to expand this haptic toolbox by stimulating the skin in a different way, is to use a Silicon on Insulator (SOI) Micro Electromechanical Systems (MEMS) device that physically pokes the user. Fig. 1.1 shows a goal of this work fixed to a user: to make a wireless tactile MEMS actuator the size of an aspirin. The inchworm motors in this work provide enough force to be detectable by the human skin when run with at least 30V. The small, 2 $\mu$ m minimum, feature size of microfabrication and large force, multi-mN, capability of inchworm motors allows for the potential creation of many more electronically controlled physical sensations. However, to wirelessly run an inchworm motor to accomplish this haptic goal, it currently needs to be integrated with two other chips that provide power and control.

## 1.3 Overview

To make a wireless MEMS device, three components are needed: Power, Control and the MEMS component. Previous work has shown three chips (Zappy for power, SCuM for

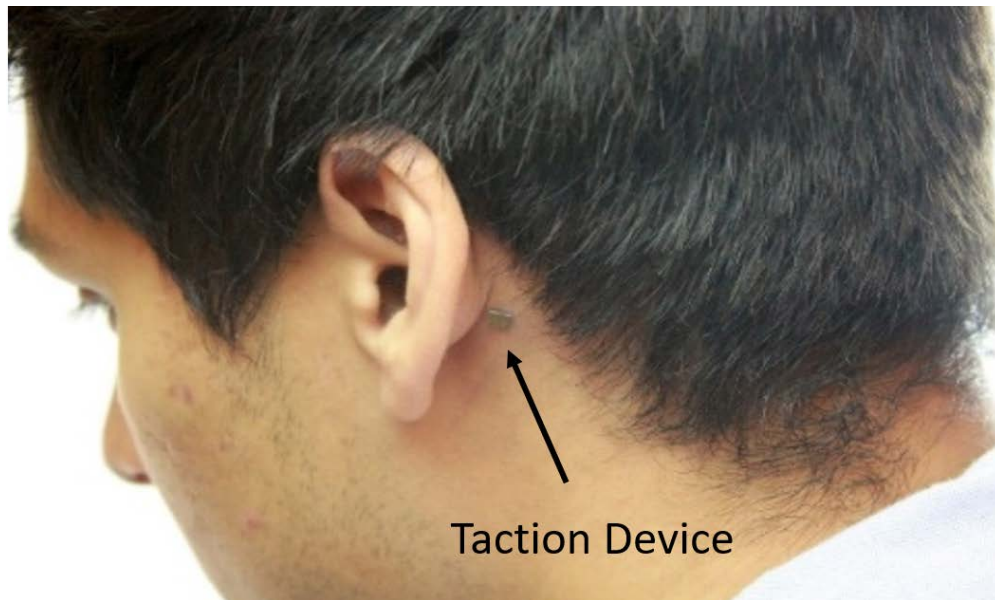


Figure 1.1: An image taken by the Paulos group showing a taction device placed by the ear of a user. Note, this is only the MEMS component and not the entire wearable system.

control and a Gripper as the MEMS component) working together [9]. Though this shows proof of concept, it is not practical for a wearable package. Zappy and SCuM are made in foundry processes with limited flexibility to aid in post-process assembly. However, the MEMS component is made by a graduate student in a SOI process in the UC Berkeley nanolab, which offers more design flexibility. Thus, instead of using a printed circuit board (PCB) as a housing to mechanically and electrically connect the three components shown in Fig. 1.3, the MEMS device can be designed based on the integrated circuits (ICs) layouts: integrate the two foundry ICs with the SOI chip as the hub rather than using a printed circuit board solely for integration like in Fig. 1.10. In addition, other MEMS components could replace the inchworm motor and other components could be added to increase the functionality further.

## 1.4 Power: Zappy

One of the limiting factors to microrobotics is a power source. The Stauth group developed an optically powered high-voltage drive circuit for microrobot applications [8]. This device is made in a 650V SOI CMOS process with 100umx100um pads with a 140um pitch. There is further work on improving the efficiency, flexibility and functionality of this chip, but this thesis will mainly consider the physical dimensions for integration purposes.



## 1.5 Control: SCuM

Another limiting factor to microrobots is communication and control. The Single Chip micro Mote (SCuM) allows optical and Bluetooth communication and its GPIOs can interface with Zappy's high-voltage buffers to control multiple inchworms motors simultaneously. The pads are  $40\mu\text{m} \times 70\mu\text{m}$  with an  $80\mu\text{m}$  pitch. Like with Zappy, there is further work on improving the efficiency, flexibility and functionality of this chip, but this thesis will mainly consider the physical dimensions for integration purposes.

## 1.6 MEMS Device Fabrication

A 3 mask SOI process shown in Fig. 1.2 has the capability to fabricate devices with wide ranging functions. Though, not an overly complex process, it is useful for quickly trying different designs for a faster design loop. This fabrication is done in the UCB nanolab. Furthermore, making process and design changes can be accomplished quickly; once a design need is determined, for example sidewall conductivity needs to increase, a researcher can simply sputter a conductive material onto devices. This flexibility in design and process allows for the MEMS component to be utilized as hub chip for IC assembly.

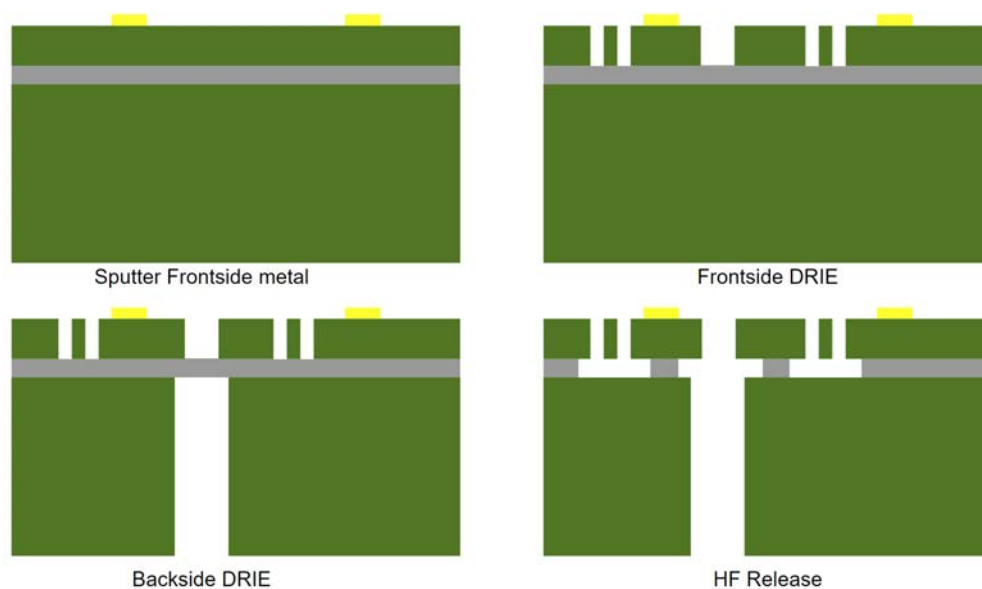


Figure 1.2: Top left: pattern sputtered metal stack - 50nm of Ti or Cr and  $0.5\mu\text{m}$  of Au. Top Right: DRIE frontside features,  $2\mu\text{m}$  minimum. Bottom Left: Backside DRIE  $40\mu\text{m}$  wide trenches. Bottom Right: HF release with  $6\mu\text{m}$  undercut.

## 1.7 Integration of the 3 Components

### Connections

How the chips are electrically and mechanically connected to each other is crucial. High resistance traces are lossy, which is detrimental to microrobots, and can even prevent the ICs from working properly. In addition, a weak physical connection is likely to lead to package failure. Ideally, the two ICs are bonded to the MEMS circuit board (MEMS-CB) with strong, low resistance connections.

### Wirebonding Connections and PCB Housing

In the previous integration work, the chips were mechanically fixed with silver epoxy and the electrical connections were made with wirebonds as shown in Fig 1.3, along with the three external capacitors 22  $\mu\text{F}$  0402 Capacitor, 100  $\mu\text{F}$  0805 Capacitor, and 100 nF 0805 Capacitor required to respectively to maintain voltages VDDIO, VBAT, and VDDH.

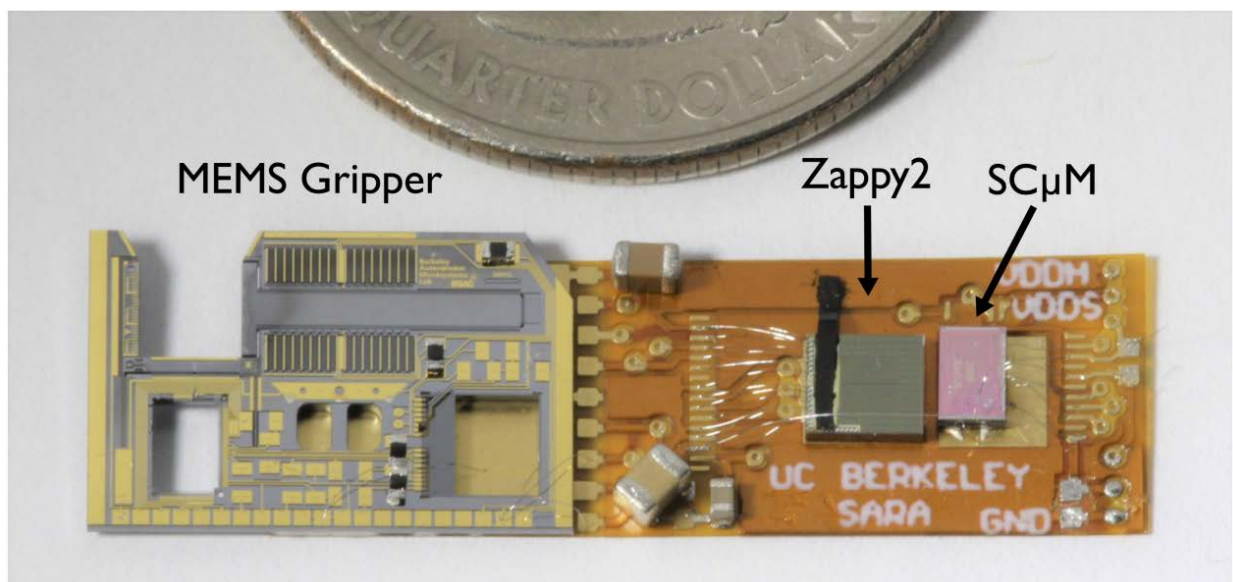


Figure 1.3: The proof of concept setup where the three chips are fixed to a PCB and then wirebonded together along with external capacitors soldered to the flexible PCB. Left to right, Gripper, Zappy, and SC $\mu$ M [10].

This proved that these three components could act as an independent system under 2 suns [10]. However, the size increased caused by the flexible PCB is not ideal, and the free-floating wirebonds are not robust enough for wearable applications. A smaller and more durable package was needed.

## MEMS Circuit Board (MEMS-CB)

The MEMS chip itself could be used as the circuit board to connect all of the electrical components of the system. The MEMS chip has the potential of very small features, such as 2  $\mu\text{m}$  wide Si beams. Even the wider beams required to support a Au trace are only 12  $\mu\text{m}$  wide, including a 2 micron wide Au trace down the middle. While these dimensions are quite large by integrated circuit standards, they are quite small compared to most PCB designs, which are typically at least 100  $\mu\text{m}$  wide. However, the MEMS chip provides only one layer of wiring, which is quite restrictive, but is mitigated by a lid chip described in chapter 3, or by  $0\Omega$  resistors used as jumpers to connect planar traces, both of which are seen in Fig. 1.10.

Using beams on the SOI layer like probes on a probe card, SCuM, Zappy or another IC can be inserted from the back side of the MEMS chip into an appropriately sized hole etched in the substrate, with all of the pads lined up under the SOI beams shown in Fig. 1.7.

Thus, small drops of epoxy deposited on Zappy and SCuM can serve as the mechanical and electrical connections. Currently, the resistivity of the SOI beams is  $15\text{-}25\Omega\cdot\text{cm}$ , and so traces of sputtered Au on the frontside, and Al sputtered to the bottom side of the device Si aid in decreasing the connection resistance. This resistance, defined from Al pad of IC to Au pad on the MEMS device, will be dominated by the resistance of the Si beam: roughly 40  $\mu\text{m}$  thick x 40  $\mu\text{m}$  wide x 70  $\mu\text{m}$  long with a resistivity of  $15\text{-}25\Omega\cdot\text{cm}$ . The resistivity and thickness are set by the wafer spec, but width and length are set by the IC pad dimensions. This is theoretically  $3\text{k}\Omega$ , which matches experimental data. A large drop (5 pads worth) of epoxy was deposited on a gold surface, which was then brought into contact with SOI beams of a MEMS-CB; adjacent SOI beams were purposely shorted. Then the resistance was measured between adjacent pads that were shorted together through the epoxied Au; the resistance path is then roughly 2x of the  $3\text{k}\Omega$  resistive path illustrated in Fig. 1.4.

After release (Fig. 1.2) the underside of the device Si was sputtered with Al to decrease the connection resistance, but when that was compared to a MEMS-CB that did not have backside material sputtered, the resistance was within 10%, which is within experimental variation. Thus, the resistance between IC pads and the SOI beams of the MEMS-CB is dominated by the resistance of the device Si. Since the pad dimensions are defined by the IC pad pitch, they cannot be greatly changed. Therefore, lowering the connection resistance has to be accomplished by lowering the resistivity of the Si. Wafers with a highly doped device Si have not yet been explored in this application.

## Alignment and Assembly

We use the same micromanipulator for assembly alignment and epoxy application, using the appropriate tip for each. The tool came with 2 different tips, but we taped on a third for epoxy application shown in Fig. 1.5. With the current tool, alignment at this scale is difficult. The best solution that we've found is to use the wirebond tip on the micromanipulator to

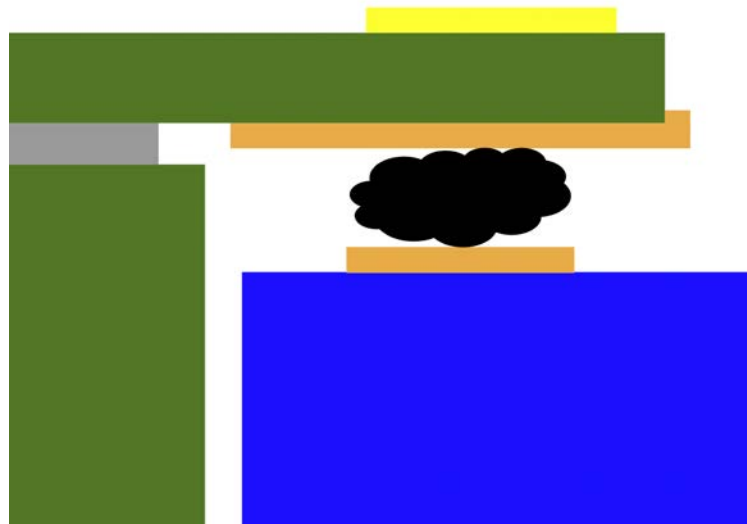


Figure 1.4: A cross section cartoon of an IC (blue) with its Al pad (orange) epoxied (black) to the Al (orange) that has been sputtered on the backside of the device Si (green).

apply epoxy to the pads of the IC chips, and then raise the aligned IC chips with the vacuum tip until the epoxied pads contact the SOI beams of the MEMS-CB as shown in Fig. 1.7.

### Epoxy Application

First, epoxy deposition was attempted by dipping the metal tip into epoxy and then controllably placing a blob onto a desired pad. However Fig. 1.6 shows that the epoxy deposited by the metal tip is nearly a millimeter and obviously far too large for the attempted microassembly. To apply a smaller amount of epoxy, a wirebond wire was taped to the tip of the micromanipulator. The wirebond's small gauge acts as a fine-tip to apply the epoxy; the micromanipulator is moved such that the wire is dipped into the epoxy and then onto the desired pad, leaving a droplet behind. Note, the epoxy deposited by the wirebond in Fig. 1.6 was left by touching down 3 times, despite the blob in the bottom left image of 1.6 looking larger than the IC pad. The amount of epoxy needed for each pad is significantly smaller than the blob picked up by the wirebond, but it is still recommended that the wirebond is redipped into the epoxy between each pad application to keep the epoxy blob uniform. If this is not done the amount of epoxy deposited with the same force changes and can lead to unintended mechanical and electrical connections.

### Alignment

The vacuum nozzle can be controlled in XYZ by moving the joystick of the micromanipulator; separately, the  $\theta$  of the vacuum nozzle is controlled with a dial on the joystick. The alignment

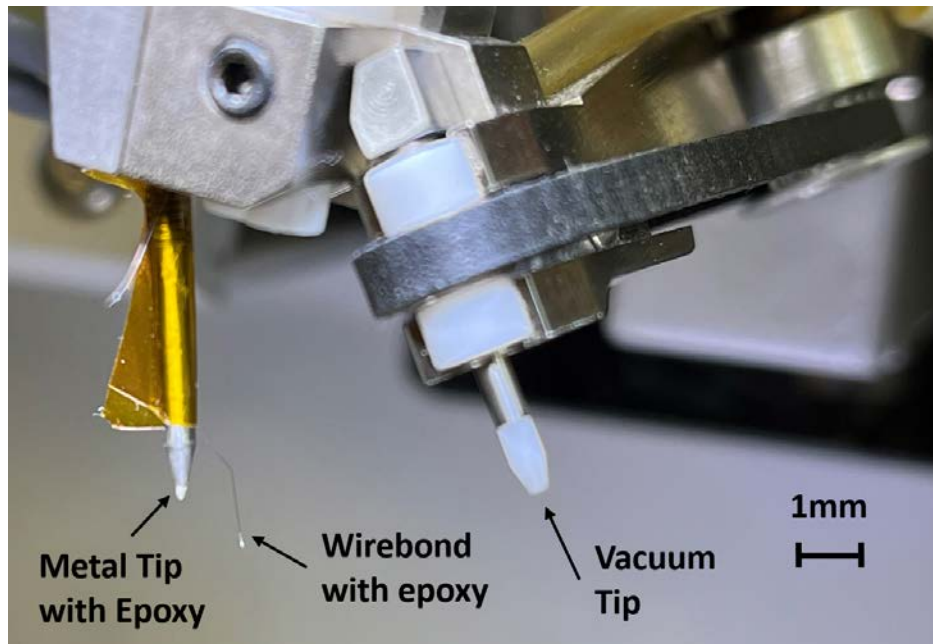


Figure 1.5: The three tips attached to the micromanipulator. The metal and vacuum tips came with the tool, but a wirebond wire was taped to the metal tip for epoxy application.

is then done by eye with the vacuum tip of the micromanipulator through a 1-5x microscope. After epoxy has been applied to the pads of the IC, it is placed below the raised MEMS-CB as shown in Fig. 1.7: the MEMS-CB remains fixed during alignment. Aligning and moving the IC pads into contact with the underside of the MEMS-CB SOI beam is accomplished by only moving the IC. The vacuum nozzle of the micromanipulator is used to pickup the IC and align it to the MEMS-CB shown in Fig. 1.8. Once aligned, the epoxy on the IC's Al pads comes into contact with the underside of their respective SOI beams to create mechanical and electrical connections between the two chips without the need for wirebonds nor a separate structural PCB.

## Full System Conclusions

With SCuM, Zappy and a MEMS-CB mechanically and electrically connected, an autonomous wearable tactile stimulator can be assembled as rendered in Fig. 1.10. Closer inspection shows ten circuit components mounted to MEMS-CB; the black  $0\Omega$  jumpers bridge planar traces due to the complex wiring needed on a single routing layer, and three voltage-maintaining capacitors shown in blue. In addition, adding a glass slide further discussed in chapter 3, increases the robustness of the MEMS device as well as potentially eliminating the need for the jumpers. The glass wafer is shown in conjunction with the jumpers to show

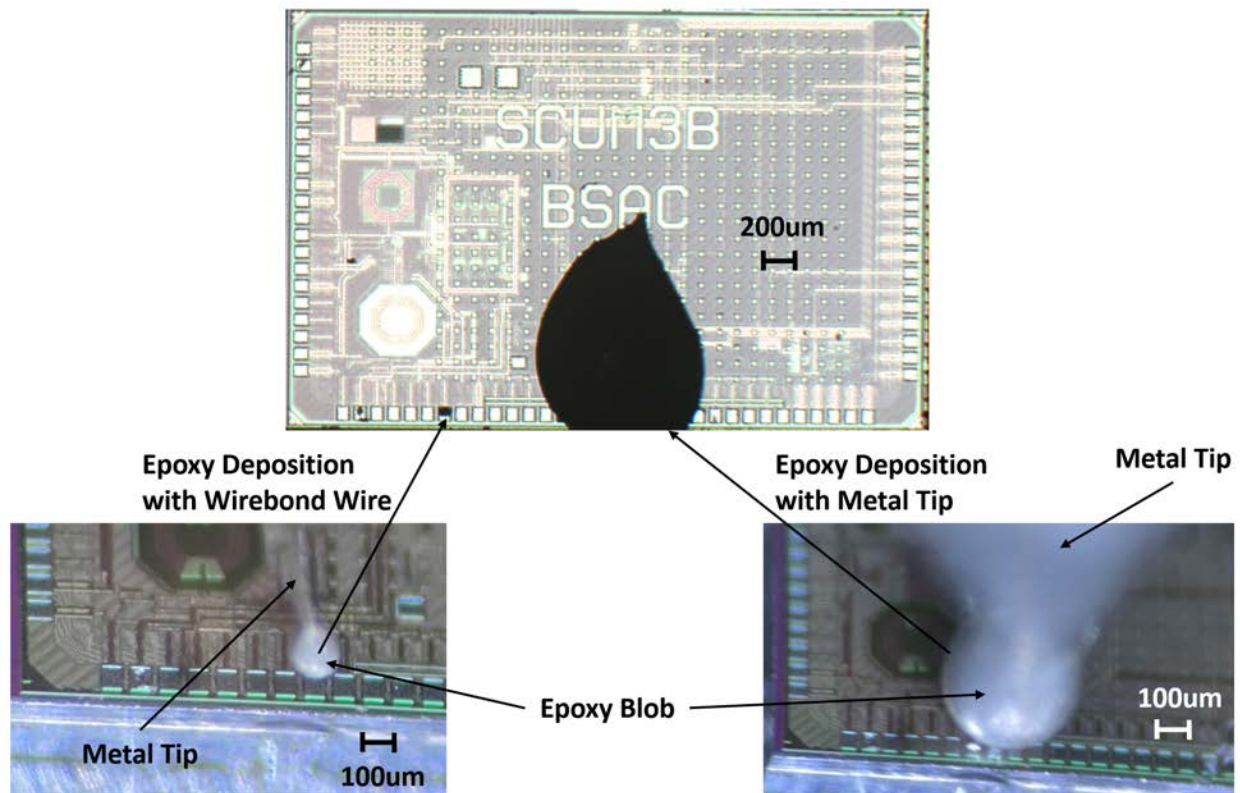


Figure 1.6: Three images of SCuM where the bottom left shows the application of epoxy with the wirebond, the right shows the application of epoxy with the metal tip and the top image shows the resulting epoxy droplets from each method.

different assembly options: the glass slide is not needed to integrate the wearable, but is a benefit to robustness and could also be used to simplify the MEMS-CB assembly. Whereas the jumpers are needed for the wearable assembly if the glass cover is not utilized due to the complexity of the necessary connections and limitations of a single routing layer. Regardless, the three capacitors are necessary components of the system.

The full integration was attempted multiple times but misalignment in conjunction with epoxy spreading was not solved. Aligning to the fine pad pitch of the SCuM chip is challenging and less than 100µm misalignment is difficult with the current micromanipulator and 5x microscope. However, proper alignment was achieved, but even with adequate alignment, epoxy spreading is difficult to control. Dispensing a blob of epoxy smaller than the pads is achievable utilizing the wirebond wire explained above. However, the proper amount of epoxy is challenging. Too much epoxy and nearby traces were shorted, and too little did not result in a measurable connection. These assembly issues are likely solved with a finer micromanipulator, high magnification microscope and a more viscous epoxy.

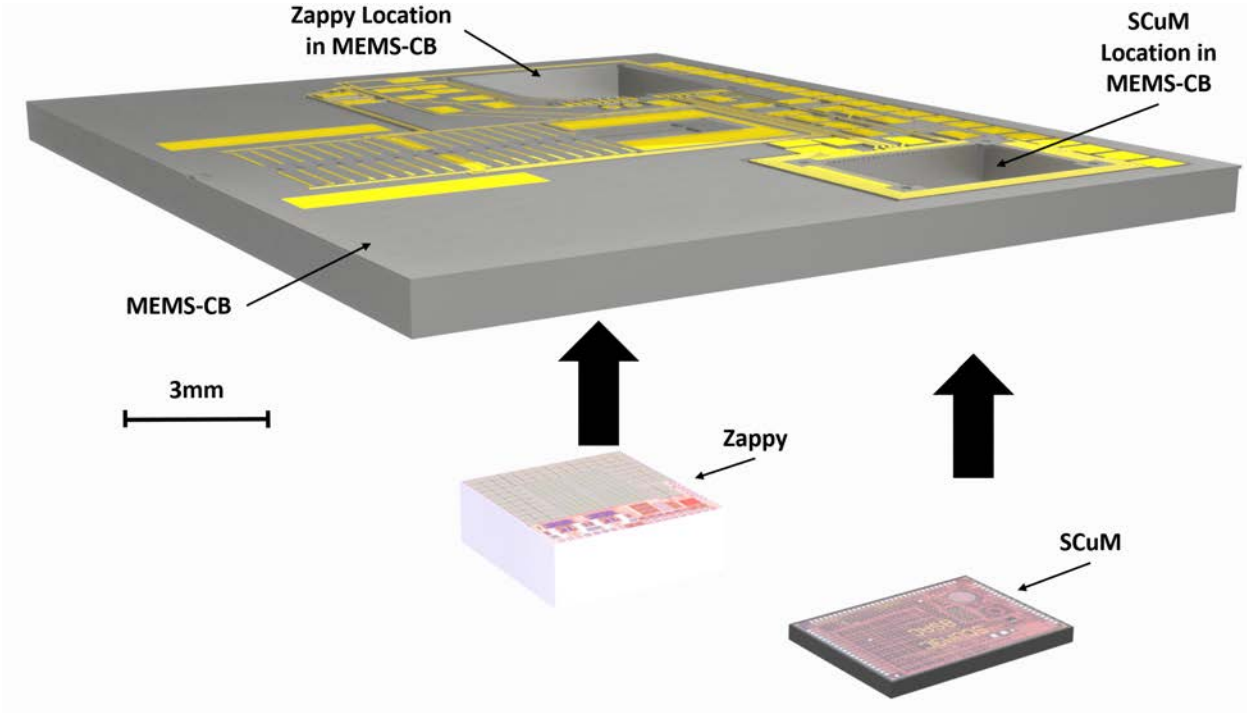


Figure 1.7: A 3D rendering of the integration step where the MEMS-CB is lowered onto the two ICs with conductivity epoxy on their pads.

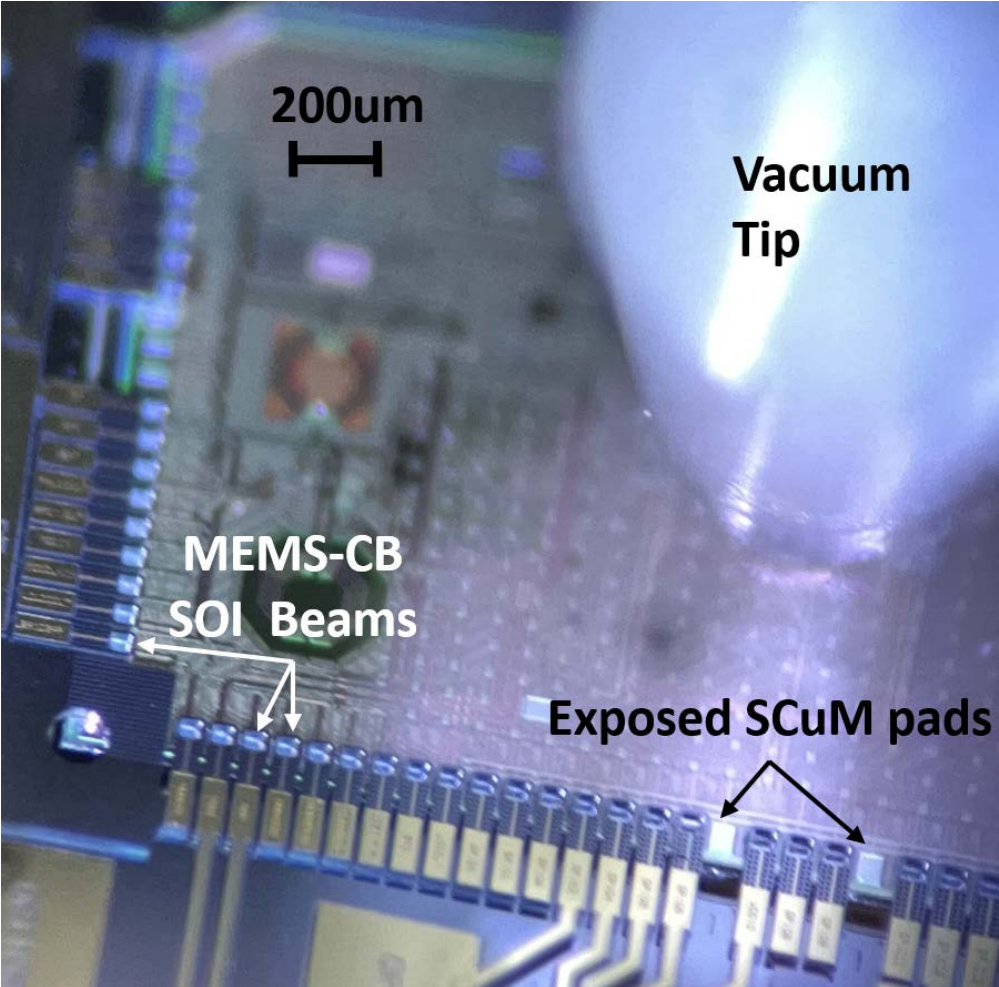


Figure 1.8: SCuM was raised and aligned to the SOI Beams of the MEMS-CB with the vacuum tip of the micromanipulator. Two SOI beams were purposely removed so that the Al IC pads could be seen.



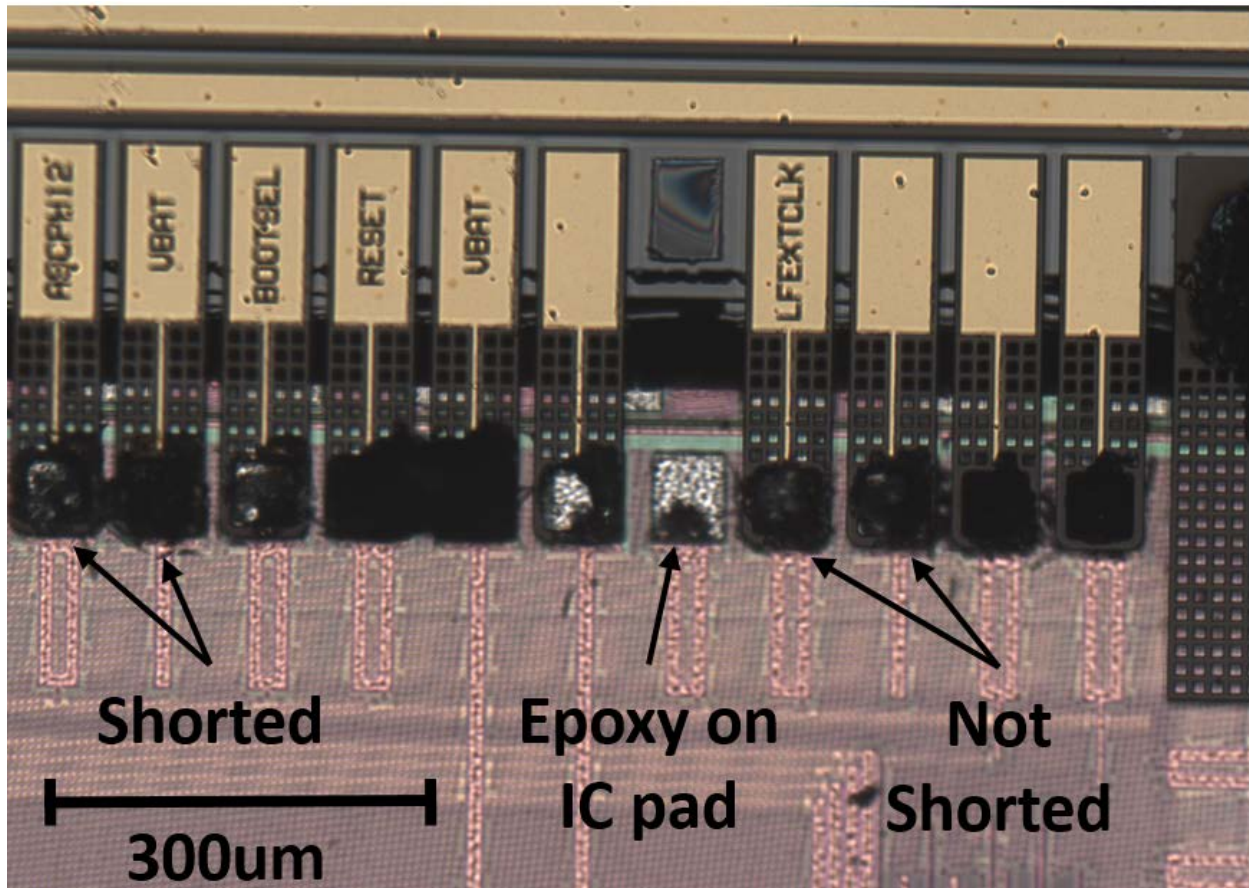


Figure 1.9: An image of an attempt to integrate SCuM into the MEMS-CB. Most adjacent SOI beams were shorted together, not all are labeled. One beam was intentionally removed to show the size of the epoxy blob on the IC pad that caused this shorting.

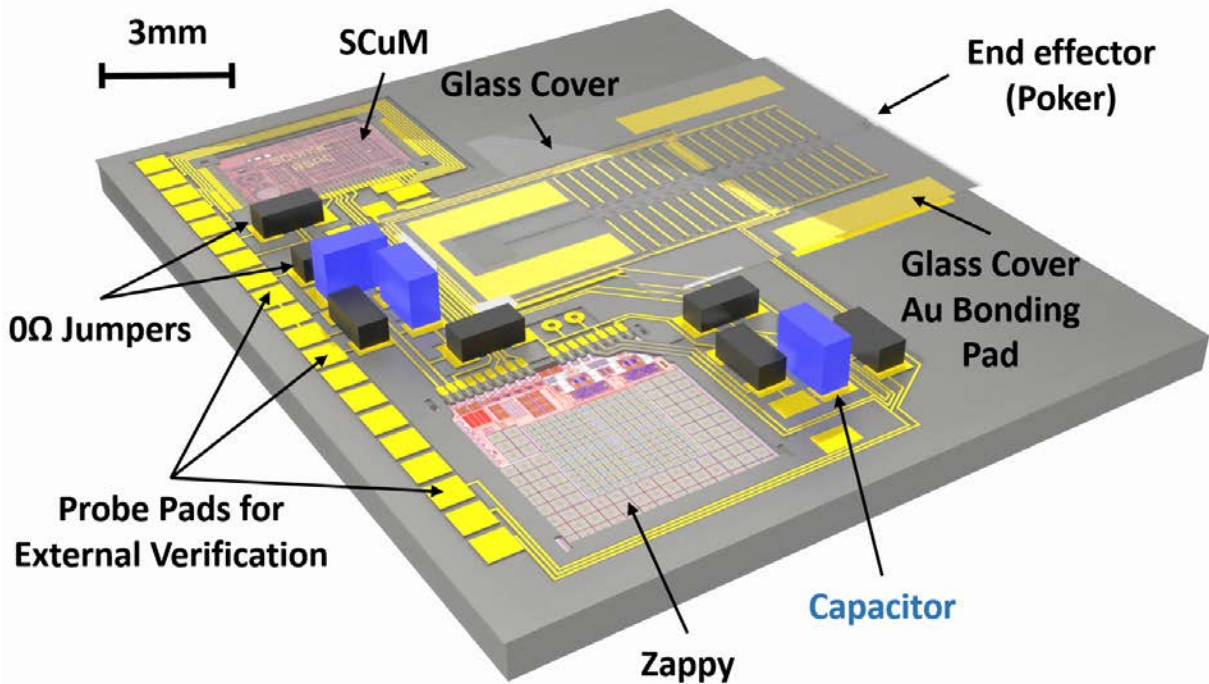


Figure 1.10: A 3D rendering of the full wearable where SCuM and Zappy are fixed to the MEMS-CB with glass only covering the MEMS components. The ten shown circuit components are needed for integration: jumpers in black and capacitors in blue. The remaining Au pads are for debugging during the assembly process and

## Chapter 2

# Simplifying Integration by Eliminating the Need for SCuM and Zappy

As explained in chapter 1, power and control are needed in conjunction with a MEMS component to make a wireless MEMS package. This chapter explores ways to eliminate the need for Zappy, and in some applications, SCuM. The first objective of this chapter is to ease integration by eliminating the need for IC assembly by including essential functions of the ICs within components that can be constructed in the MEMS fabrication process. The second is for microrobots to explore high temperature environments, for example the surface of Venus, where CMOS chips like SCuM cannot survive without extensive thermal protection.

To eliminate SCuM, the two square wave signals shown in Fig. 2.1 must be generated. However, if SCuM were to not be included, there could be no communication with the device. It could only be turned on and off by supplying enough power to run the inchworm motor, thus limiting its applications. However, the inchworm motors can be controllably run by illuminating the package: with Zappy's solar cells or others. To replace Zappy, not only does the power source need to be replaced, but high voltage buffers as well.

In the current operation with SCuM and Zappy running an inchworm motor, SCuM generates the square waves at a low voltage, which control Zappy's high voltage buffers that connect the solar cell high voltage output to the inchworm motor. To replace Zappy, high voltage hot-switchable relays and on-chip solar cells must be constructed; to replace SCuM, a method of generating the offset square waves must be constructed. This is proposed to be accomplished with a multifunctional solar skin, and an oscillator comprised of resistors and relays.

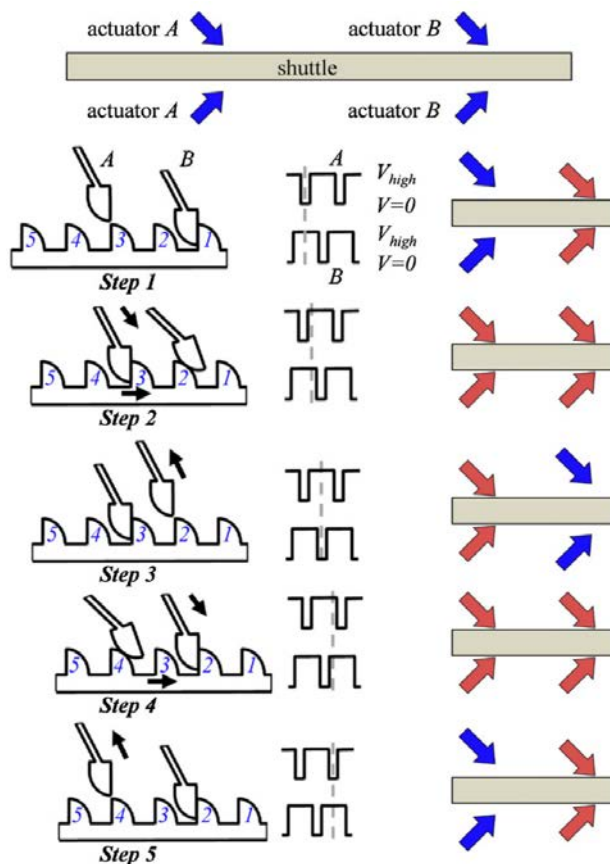


Figure 2.1: Overview of inchworm motor control and operation [12].

## 2.1 Powering Inchworm Motors with Structural Si

In the package outlined in chapter 1, the power comes from solar cells in the Zappy IC, and Fig. 1.10 shows a vast area of underutilized Si. It is there for structural purposes, but if doped, and wired, could potentially provided the needed energy to power an inchworm motor. Creating a solar skin from the device Si to power itself, like in Fig. 2.2 could be accomplished with the proposed flow shown in Fig. 2.3. In this flow, the N+ doping step along with the p- device Si makes the solar cell, and the Au pattern is used instead of a p+ region to conduct holes. This Au can also be used for wiring; as discussed in chapter 3, a glass or SOI chip with patterned Au can be bonded to the Au on the SOI wafer. This can simplify routing an array of solar cells, as well as increasing robustness. This MEMS device is a useful structures to achieve mN forces and cm displacements in a mm scale-package, however, to power it, with appreciable force, at least 30V is needed with an estimated few nanoamps of current Fig. 2.4.

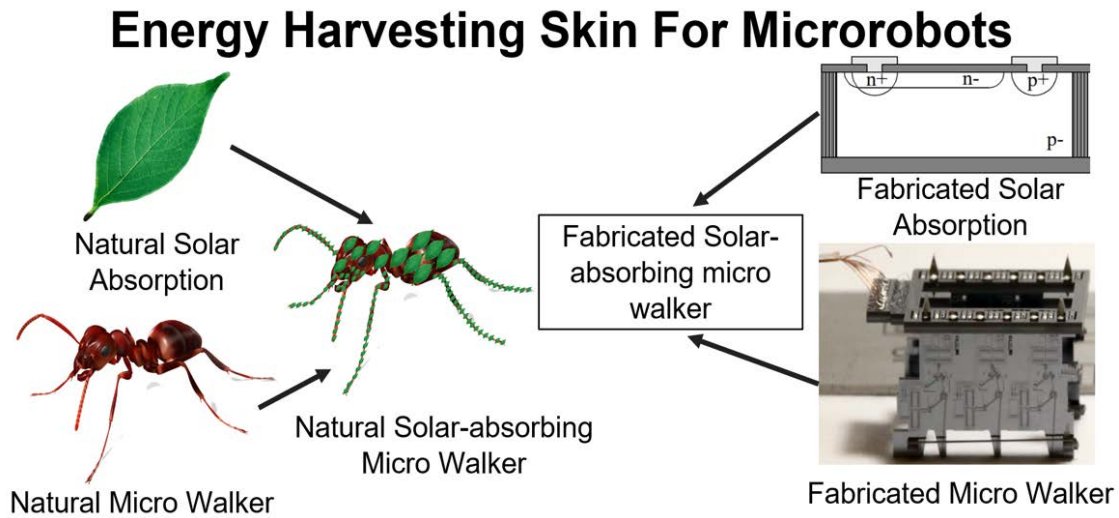


Figure 2.2: Cartoon illustrating the idea of solar skin on a MEMS device, which for this example, is a microwalker [3].

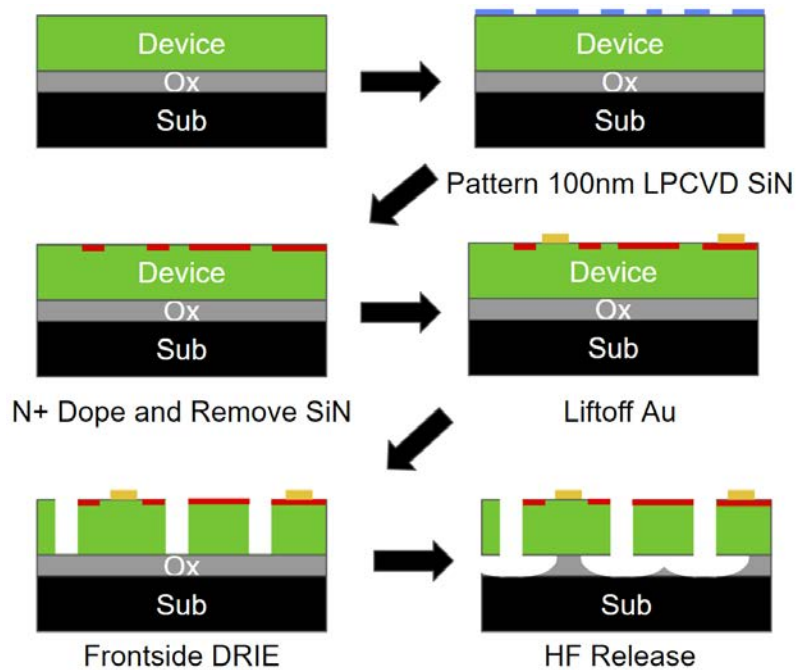


Figure 2.3: Process flow for solar skin MEMS structures.

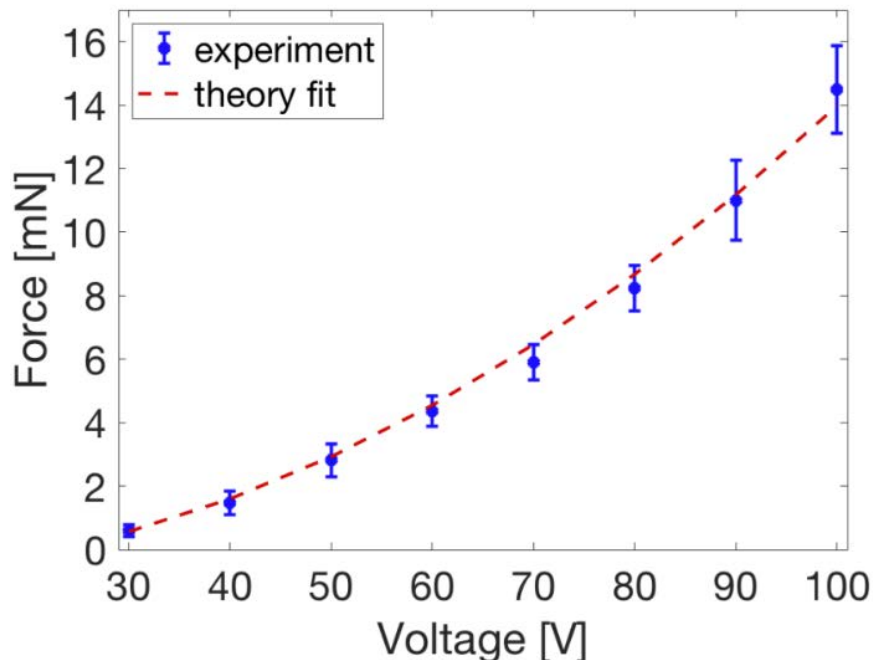


Figure 2.4: Plot of experimental and theoretical force [15].

## 2.2 Hot Switching

Hot switching is defined as two separate structures of different potential, physically coming into contact with one another. This is a major limitation with current micro-relays because hot switching, even at a few volts, leads to the contacts welding shut, thus destroying the device. Different theories exist on the exact physics that occur, but arcing and material transfer leading to contacts getting stuck closed with a higher potential differential is clear [2].

Making a high voltage hot-switchable relay is trivial for high resistance contacts: our Si-Si contacts range from 1 – 10M $\Omega$ s have survived over 100M hot switch cycles [3]. Stuck closure events are not currently seen in our SOI inchworm motors because the contact material is Si. Lower resistance contacts are achieved through metals, but suffer from hot switching failure; the contacts weld shut when the adhesion force is larger than the spring force, thus the relay remains closed. Our group has successfully hot switched lateral SOI relays with 60nm of sputtered TiN, but this was only done for a few cycles at 4V [14]. The purpose was to measure the time delay of a GCA opening and closing, not to have the device cycle more than a few times at a low voltage.

## 2.3 Mechanical Finite State Machine (MFSM) to Run an Inchworm Motor

For mechanical relays to drive an inchworm motor with appreciable force, they must be hot-switched at least at 30V, which is very limiting to the force/usefulness of the inchworm motor, yet still difficult for a relay to survive even a few cycles. Fig. 2.1 shows the phase-shifted square waves required to run an inchworm motor. Currently, these signals are made with CMOS circuits but can also be generated only with relays - thus, eliminating the need for CMOS to run an inchworm motor.

There was significant effort to create a system where the opening and closing of the inchworm's two gap-closing arrays (GCAs), Actuator A and Actuator B shown in Fig. 2.1, would cause the next step in the state diagram. Meaning, applying one DC voltage would allow the inchworm motor to operate as though the same 2 phase-shifted square waves were applied. Since, the state where both GCAs are closed has two possible subsequent states, Actuator A opening or Actuator B opening, the control system requires memory. However, its not that simple because the mechanical and electrical time constants for a relay and GCA all need to be taken into account. Actuator A cannot open until Actuator B closes, and vice versa, in addition both actuators must open enough to fully release the shuttle.

Thus, the test structures to measure the pull in and release times were repurposed to measure when the two actuators of the inchworm motors were open, closed or traveling between the two states [14]. When the relay is pulled out, Contact is VDD and PO is ground, and Contact is ground while PO is VDD when the relay is pulled out shown in Fig. 2.5. To avoid vertical pull in between movable SOI components and the substrate, they are both grounded. Thus pull up resistors to VDD were used to determine what state the Actuators were in, shown by the circuit in Fig. 2.5. However, this complex system of relays was never successfully fabricated; problems with relays intermittently sticking closed and syncing time delays of the physical structures with so many relays were not able to be overcome.

The easiest solution was found to simply create the two waveforms with oscillators constructed by relays. This is similar to the idea from Professor King Liu's group where simulated square waves were generated only from resistors and a mechanical relay [4]. The goal of this work was to run inchworm motors without the need for CMOS control, but never worked experimentally. Both the more complex MFSM and oscillator systems both use a relay as their basic unit, which is difficult to make hot-switchable at high voltages.

### Single Relay

Whether a more complicated MFSM, or oscillators, the building block of the control system is the same: a relay. With the current fabrication method, lateral SOI relays can be constructed with 3 terminals with the basic structure shown in Fig. 2.6. Once the Gate node is above

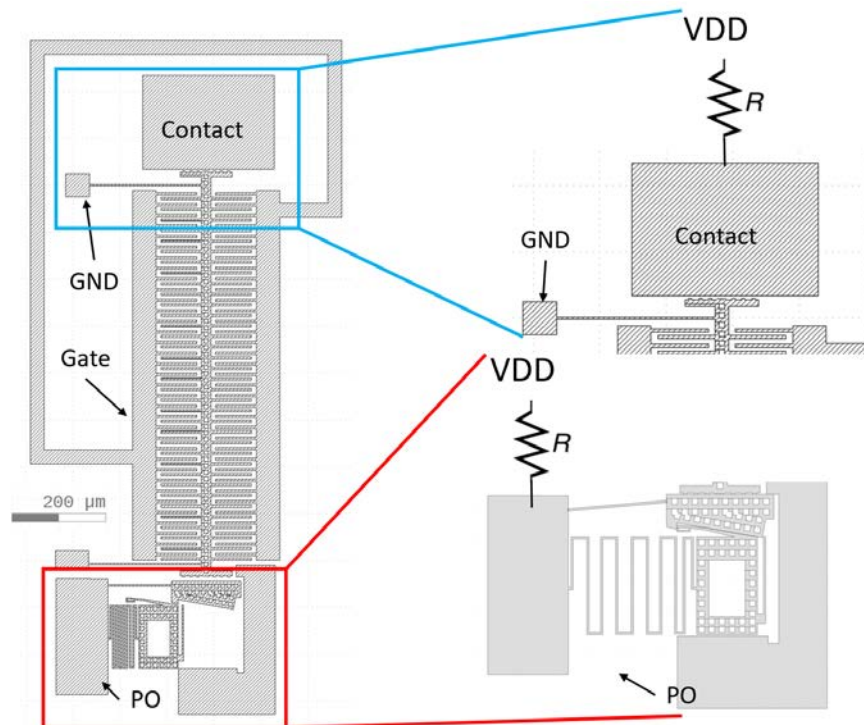


Figure 2.5: Layout and a schematics of the pull up network for a pull in and pull out sensor where  $R$  is  $1M\Omega$ . Left: layout of a relay with a pull in sensor Contact and a pull out sensor PO. Top Right: the schematic for the pull in sensor. Bottom Right: A zoomed in image of what the device looks like once its been setup - not its layout. The PO node must make contact to the GND node, but cannot be fabricated connected since they also must be separate physical parts. The large Si rectangle is dragged into contact with a probe - note the difference between the left and bottom right images.

the pull in voltage of the device, the relay will pull in and connect the GND node to the Contact node.

Table 2.1: Table of the 100x change in contact resistance with changing applied voltage. The 100nm Ru-sputtered relay was designed to pull in at 30V, but pulled in at 27V.

Applied Voltage	Contact Resistance
27V (VPI)	$33k\Omega$
100V	$241\Omega$

Making a low resistance lateral SOI relay in an SOI process is straightforward, and accomplished by sputtering a conductive material after the normal SOI process. The most



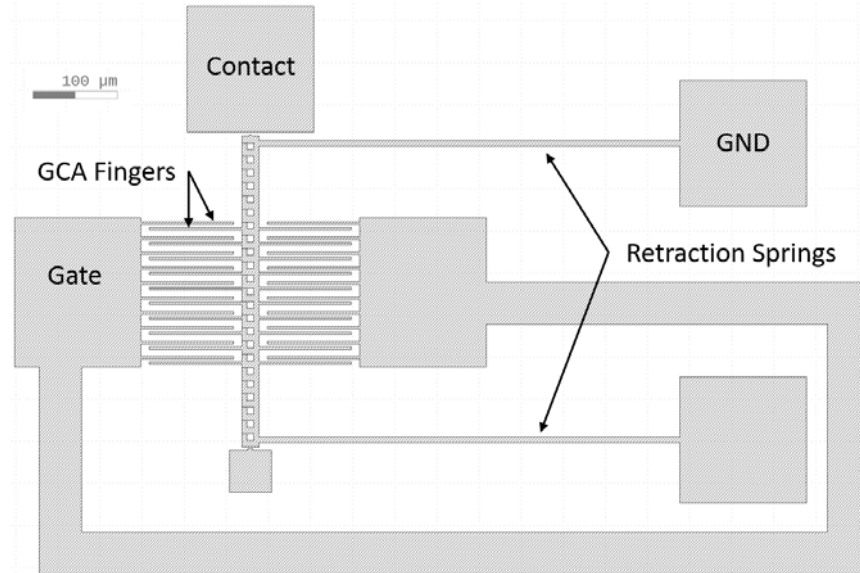


Figure 2.6: Layout of a single relay. Three nodes of this device are the Gate, GND, and Contact where the voltage between the Gate and GND node determine actuation of the device.

difficult aspect is what conductive material to use. Bare Si-Si contacts have a large resistance, 1-10M $\Omega$ , thus a more conductive contact material is needed. Sputtered Ruthenium, Chrome, and Titanium-nitride were used as contact materials, each with thicknesses of 30nm, 50nm, 100nm and 200nm: totaling 12 contact material variations. No appreciable change in resistance nor ability to survive hot switching was seen between these materials. The driving factor of change in contact resistance is applied voltage. Table 2.1 shows a 100x decrease in resistance by increasing the applied voltage across a relay.

The pull in voltage of this device was designed to be 30V, but was measured to be 27V. The Contact and GND nodes were grounded, while the voltage of the Gate node was increased until pull in occurred. Then, the resistance was measured between the Contact and GND nodes. This resistance was noted as the gate voltage was further increased. The purpose for shorting the Contact and GND node before opening or closing the relay, rather than measuring the contact resistance between the same nodes as the relay pulls in, is to avoid hot switching. Even minimal hot switching caused by measuring a resistance across soon-to-be contacting materials, or involving a floating node, can result in a stuck closure. Fig. 2.7 shows a relay that was closed but the Contact node was left floating. However, this was an extreme example and often relays get stuck closed without any visual change to the film.

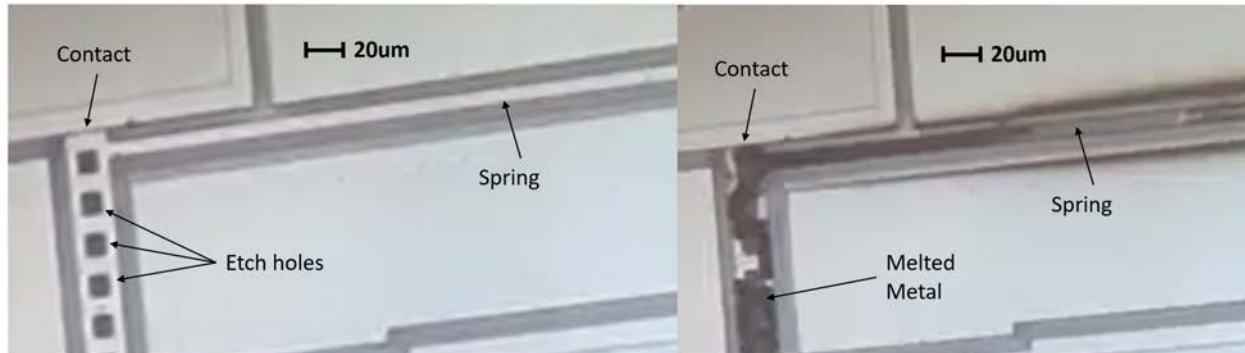


Figure 2.7: 100nm of sputtered Ru film underwent a visual change when the Contact node was left floating upon pull in. Left: the relay just before pull. Right: Just after pull in.

### High Voltage Experiments: 30V-100V

To show that these relays can be used to run inchworm motors, they were hot switched from 30-100V. The first test setup was identical to the one described above, except the contact Node was instead fixed at 100V instead of shorting to ground with the GND node. Thus, the Contact node was 100V, GND was grounded and Gate was increased from 0V to 100V with a step function. Fig. 2.9 shows the result where the retraction spring was blown away. This relay had the same Gate voltage vs. resistance that was shown in Table 2.1 When the relay pulled in, 100V was across the  $241\Omega$  contact resistance: over 400mA of current caused a loud popping noise and the retraction spring to vaporize. Thus, a current limiting resistor was included for the subsequent tests.

High current upon closure was thought to be the cause so a  $1M\Omega$  current limiting resistor was included as shown in Fig. 2.8. While open, the Contact node was VDD, GND was grounded and Gate stepped up from 0V to 30v. Again there was a popping sound and obvious destruction shown in Figures 2.10 and 2.11 with 100nm and 30nm of sputtered Ru respectively. These relays also had a similar 27V VPI and Gate voltage vs. resistance, so the current causing this was 30uA. No appreciable change was seen in material thickness nor element. For these explosive experiments, the three probes were even difficult to remove from the pads due to the redeposition of the contact material, which splattering over a hundred microns away.

## 2.4 Conclusions for Eliminating SCuM and Zappy

This work was unable to experimentally show the ability to eliminate SCuM nor Zappy. To replace Zappy, on-chip solar cells and low resistance 30V hot-switchable relays must be constructed, in addition to a power source. The solar cells process was never able to be properly run: fabrication errors prevented the testing of initial test structures.

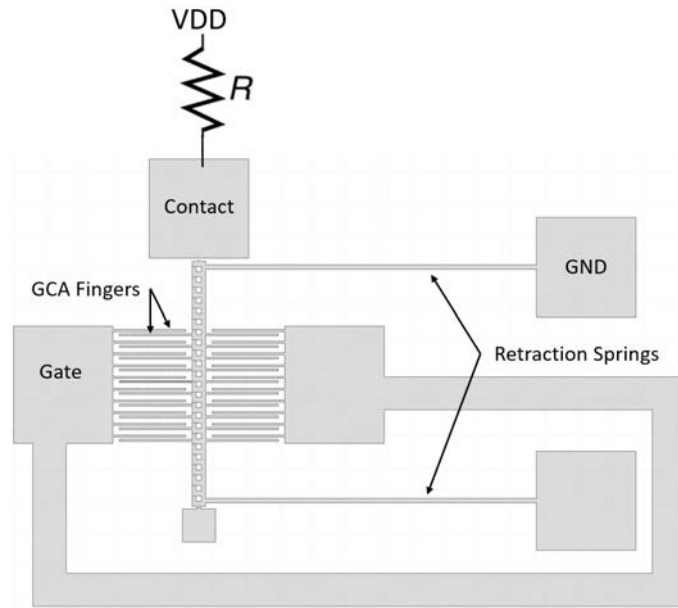


Figure 2.8: The circuit schematic of the hot switch test setup. VDD was 30V for Figures 2.10 and 2.11 and but R was constant at  $1M\Omega$ .

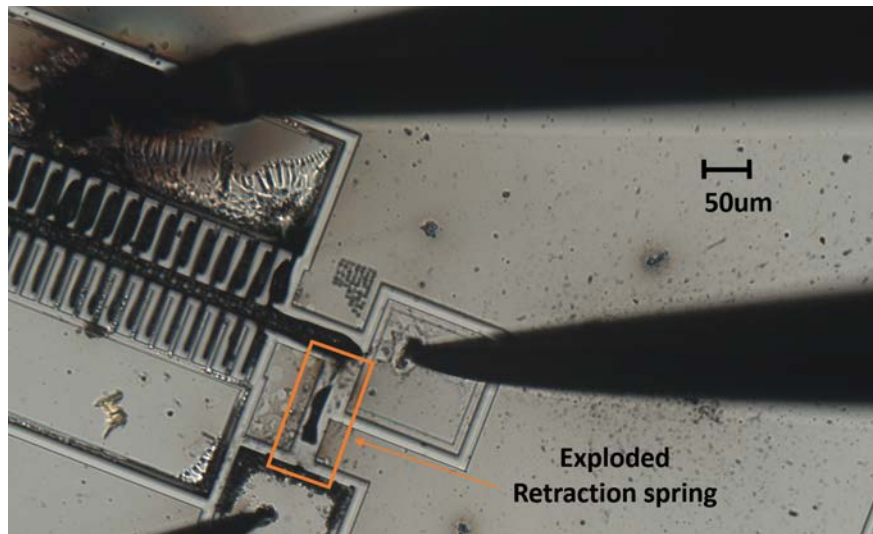


Figure 2.9: A relay sputtered with 30nm of Ru that underwent a violent change when hot switched at 100V with no current limiting resistor. The top probe was the Gate, left probe was GND, and the right was Contact.

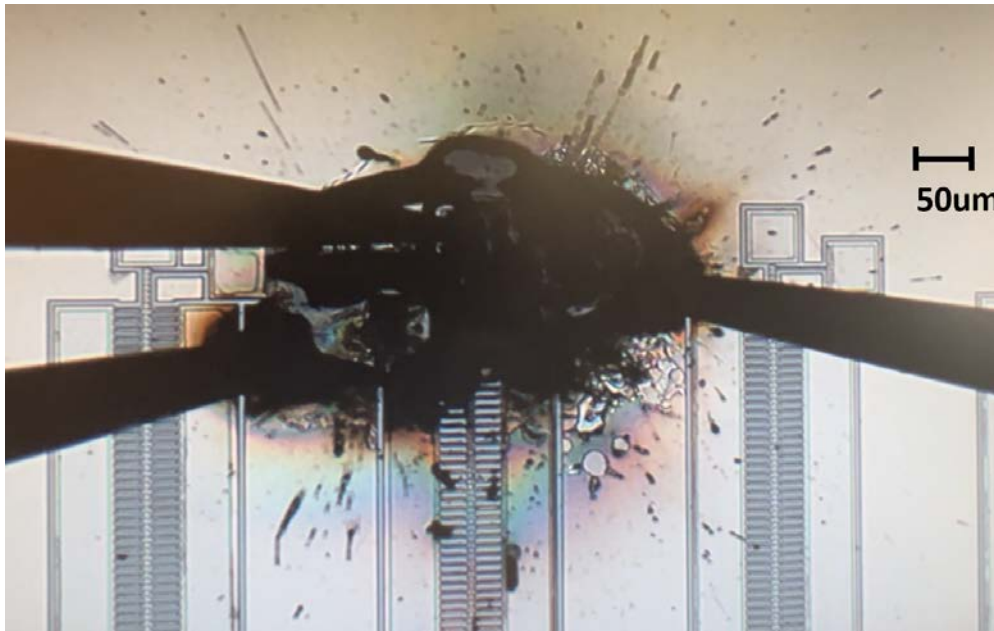


Figure 2.10: Relay sputtered with 100nm of Ru when hot switched at 30V with a 1M $\Omega$  resistor. The top probe was Contact, left probe was Gate, and the right was GND.

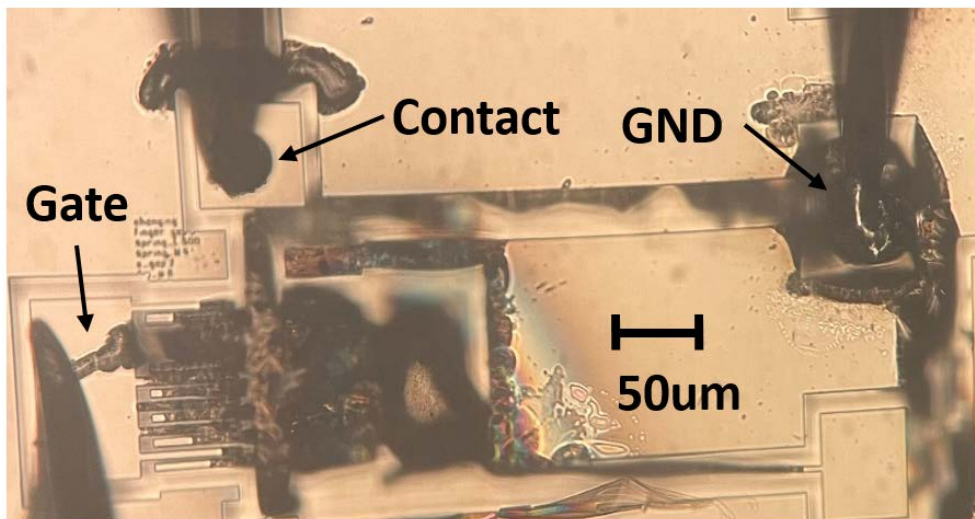


Figure 2.11: A relay sputtered with 30nm of Ru that underwent a violent change when hot switched at 30V, even with a 1M $\Omega$  resistor.

Zappy's high voltage buffers could also not be replaced with SOI relays due to lack of hot-switching capability. Si-Si relays can be hot switched over 100V, but their resistance is 1-10M $\Omega$ ; relays with resistances less than 30k $\Omega$  were unable to be hot switched above 5V. Low voltage (under 5V) lateral SOI relays can be fabricated and hot switched, however, inchworm motors force is proportional to the square of the applied voltage such that 30V is the minimum voltage to achieve a useful force for tactile applications. Twelve contact material variations were tried (three different materials each with different 4 thicknesses) but no change in hot switching capability was observed. In addition the the contact resistance depended on the force between contacts more than the thickness or material of the sputtered contact. This contact resistance did decrease from 1M $\Omega$ -10M $\Omega$  for the Si-Si contacts to 241 $\Omega$ -33k $\Omega$  for sputtered contacts, depending on the applied voltage. Further investigation into a conductive, hard and non-sticky contact material is required for these relays to be implemented in an system controlling inchworm motors.

To replace SCuM, a method of generating the offset square waves must be constructed. A complex design where the opening/closing of actuator A causes the opening/closing of actuator B that mimics the state diagram of 2.1 was attempted but never shown to work, even at low voltages where the relays could survive hot switching for limited cycles. Instead, a simpler solution is to create the square waves from relay oscillators. However, this was not shown experimentally. The best method found to create a wireless tactile wearable is to incorporate SCuM and Zappy into a MEMS-CB outlined in chapter 1.

## Chapter 3

# Taction Devices

The proof of concept design, V1, suffered from failure due to contamination, but proved that a 40um thick, 250um wide piece of Si could be felt by a human when pushed into contact with skin with 1mN of force. This V1 device is shown in Fig. 3.1 next to a finger, and it's layout is compared with an updated High Force version in Fig. 3.3. The High Force version addresses the contamination issue with post processing and layout changes, in addition it can provide 15x the force.

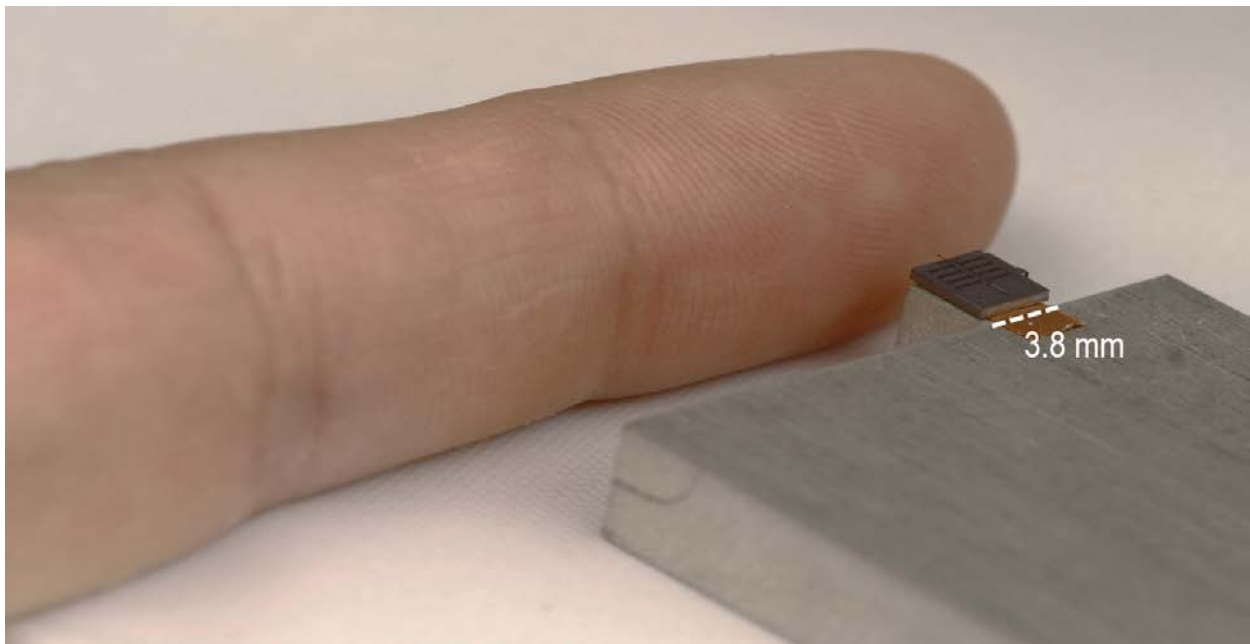


Figure 3.1: An image of the V1 taction device next to a finger provided by the Paulos group.

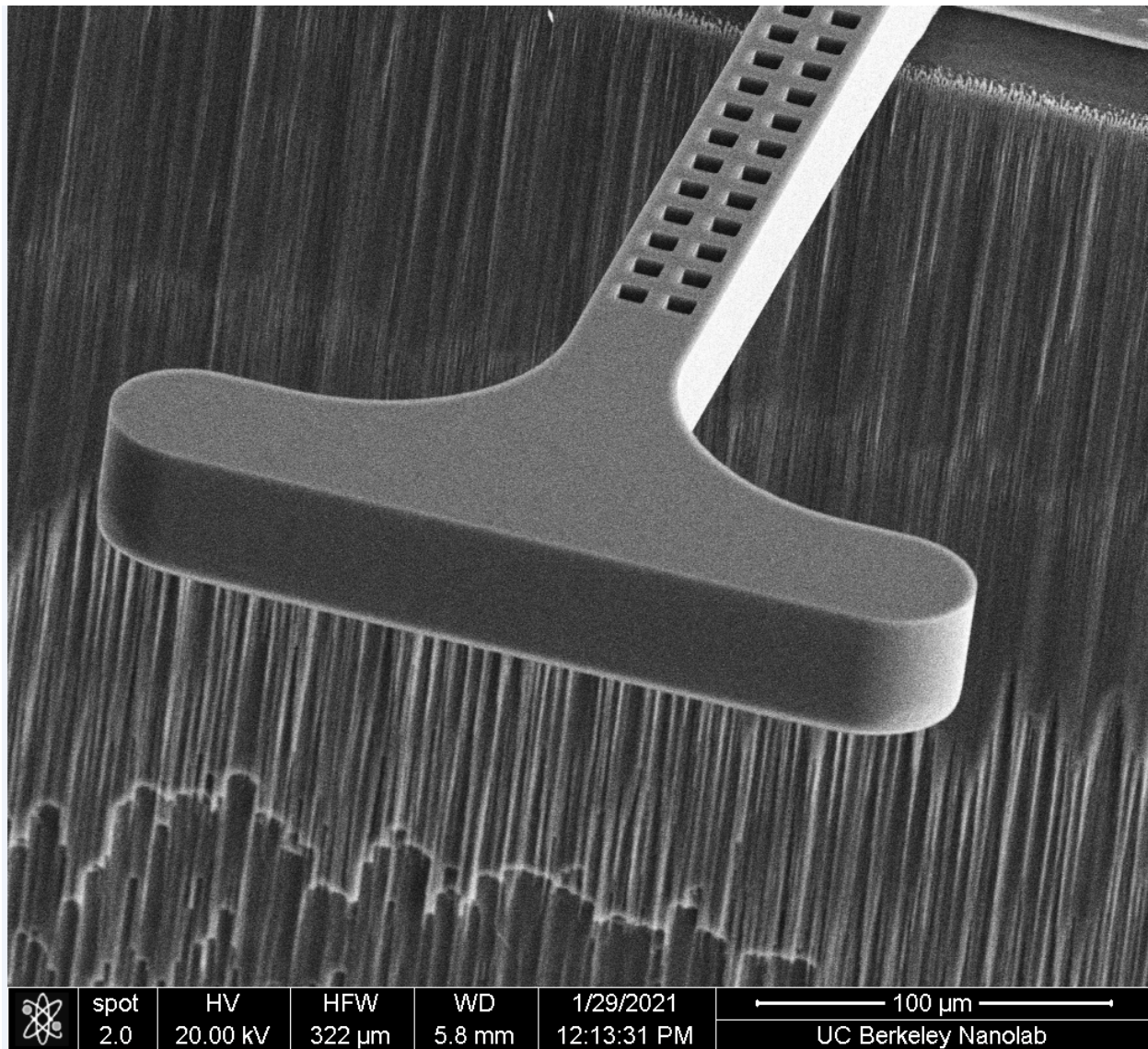


Figure 3.2: A SEM image of the V1 taction device’s end effector. This is the Si that makes contact with human skin.

### 3.1 Preventing Contamination

The main failure mode of V1 was condensation from human skin which caused the retraction springs of the device to stick: making the device inoperable. Partial encapsulation and layout redesign were explored to mitigate that failure.

Fig. 3.4 shows moisture and oils from human skin condensing onto the Si surface. These particles can cause failure of movable structures that they come into contact with. The

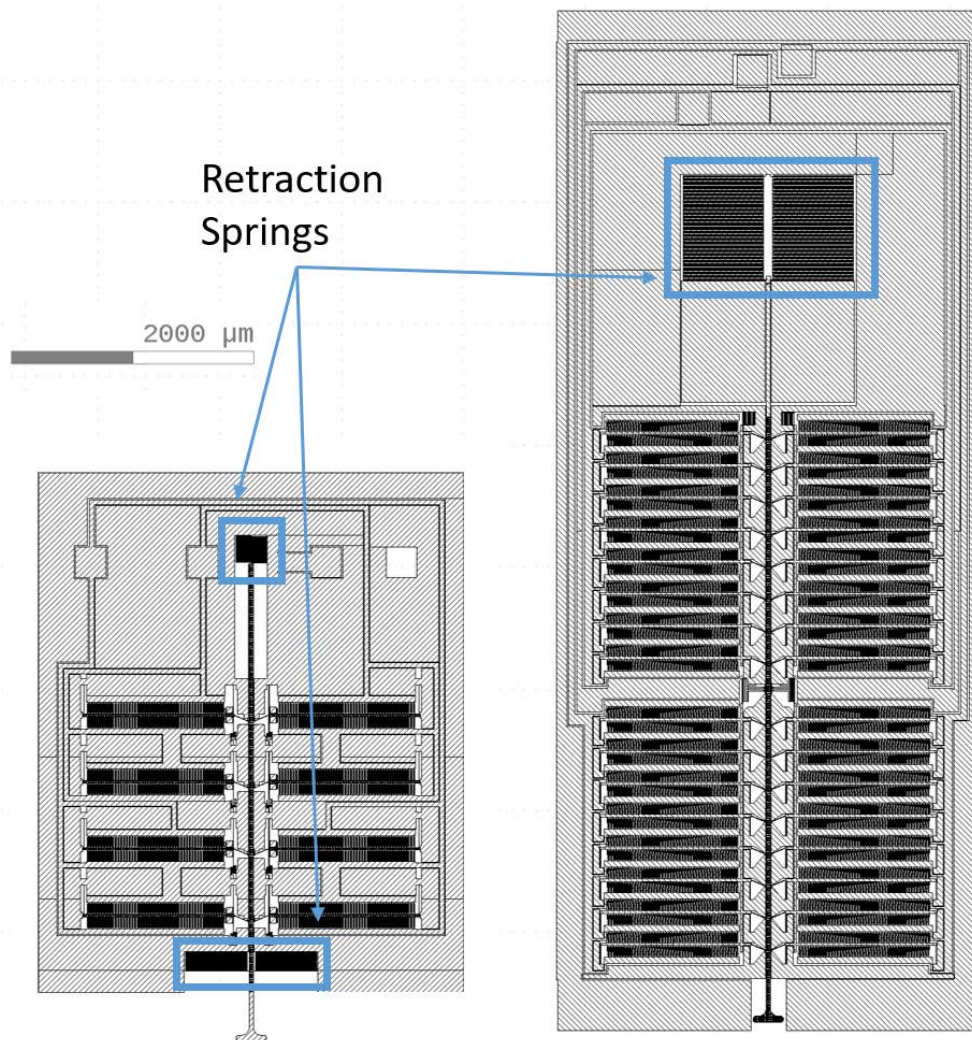


Figure 3.3: Left: V1 with 2 sets of retractions springs - one near the probe pads and the other close to the end effector highlighted in blue boxes. Right: The High Force redesign has only one set of retraction spring that are on the opposite end of the device from the end effector.

end-effector is the exception. Though it is 40 $\mu$ m thick Si with a 2 $\mu$ m gap to the substrate below, it did not get stuck due to repeated exposure to moisture by contact a finger. The failure mode was when the moisture reached the retraction springs or GCA of the inchworm motor. Those are the two types of features that need protection.



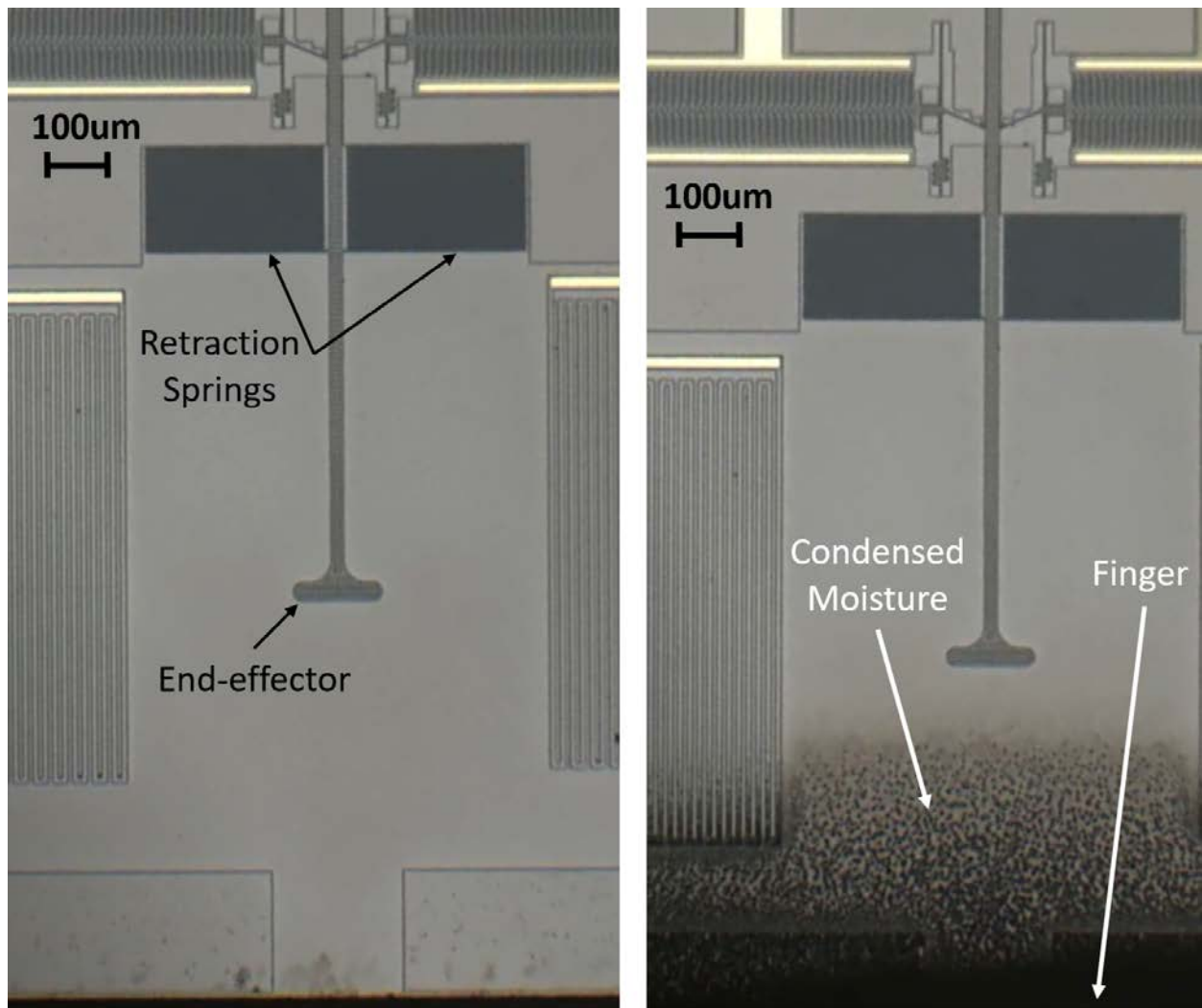


Figure 3.4: Left: a tactile device with no contamination (human skin) nearby. Right: a finger is placed at the bottom edge of the chip which causes particles to condense on the Si.

### Partial Encapsulation

The MEMS tactile device is designed to physically contact the human skin and is thus exposed to the moisture and oils of the human skin. Thus, it cannot be hermetically sealed as many MEMS devices are. It can however be partially encapsulated. Either on a wafer scale by wafer bonding, or on a chip-scale by adding a cover by hand post process.

Both methods are an effective way to protect the devices from moisture, and physical destruction. Additional process steps were explored where Au-Au thermocompression bonding a glass wafer with Au traces to the MEMS wafer was completed. In addition to providing

protection, this approach provides a second routing layer: simplifying traces and decreasing the need for costly post-process wirebonding.

### Wafer Bonding Glass to the SOI Wafer

Three challenges were overcome to successfully produce partially encapsulated chips from a wafer-bonded stack. The Au delaminated which decreased bond integrity, the wafer stack cracked after bond, and individual devices were difficult to remove from the wafer. These challenges were solved by adding a lift off resist, using a different glass wafer, and changing the dicing procedure respectively.

The first issue was the Au stack itself. The stack is 50nm Ti, 50nm of Pt, and 1 $\mu$ m of Au; the Titanium acts as an adhesion layer, while the Platinum acts as a barrier layer, and the Gold layer allows the bond. The tool manual, shown in Appendix A, recommends a Au layer 0.5-1 $\mu$ m thick and notes that thinner films drastically decrease in bond strength. All three films in the metal stack are critical for a successful thermocompression bond. The Ti layer is visible in Fig 3.5 because the bottom of the metal stack is seen through the quartz wafer. Also in this image, the Au on the SOI wafer is seen. This is due to misalignment. Bonding was done on an AML AWB-08-30 wafer bonder; 8 $\mu$ m of misalignment was achieved, but less than 2 $\mu$ m has been achieved by other tool users.

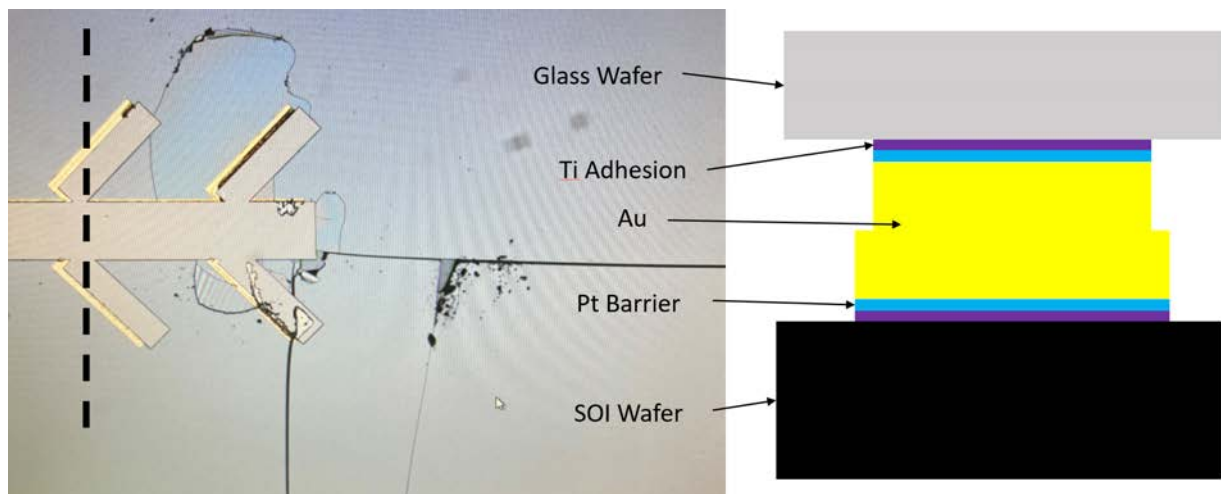


Figure 3.5: A zoomed in image of the bonded stack cracking and misalignment. On the image to the left, the gray is the Titanium (the bottom of the Au stack) shown through the quartz wafer and the yellow is the gold.

Thermocompression bonding is much less sensitive to defects as other types of bonds: the bonding surfaces do not need to be as clean and flat as fusion bonding. However, folds of



Figure 3.6: Au stack peeling after liftoff. The black strips are peeled back folds of the metal stack and the green is the glass wafer.

delaminated Au shown in Fig 3.6 are large enough to cause the thermocompression bond to fail. In this figure, the gold is supposed to be a solid strip, but much of the gold peeled back in the liftoff process and the black are folds of metal left behind when it ripped off. This delamination was caused by the Au on the Si being ripped up during the liftoff process. A thinner Au layer (which limits bond strength and success) or utilizing liftoff resist eliminates the issue. This is because less Au is deposited on the sidewalls of the photoresist (PR), so when the PR is removed, it does not peel back the Au designed to be left behind on the Si.

The next issue with thermocompression bonding was caused by thermal mismatch. The SOI wafer was bonded to a quartz wafer, but as the bonded pair cooled, the stack cracked and ripped itself apart shown in 3.5, Fig. 3.7, and 3.8. The bond took place at  $300^{\circ}\text{C}$ , thus as the stack cooled to room temperature, the stressed caused by the TCE differential between Si and Quartz caused the wafers to crack. This issue was fixed by using a borofloat wafer instead of quartz. This solved the issue because the borofloat's temperature coefficient of thermal expansion is matched to Si, while quartz's is roughly 6x highlighted in Table 3.1. Once this change was made, a SOI and Borofloat wafer, each with  $1\mu\text{m}$  thick Au traces, were successfully bonded with the given parameters in Table 3.2.

The final challenge to wafer bonding was how to get chips out of the wafer stack. Traditionally, the backside DRIE etch singulates the wafer, however, plasma dicing was not possible because of the bonded borofloat wafer; the SOI wafer was extremely fragile after the substrate DRIE and the glass wafer was not able to be controllably etched without

Table 3.1: Table of Si, Quartz and Borofloat TCE [1] [13] [11]

Material	Temperature Coefficient of Thermal Expansion
Si	$2.6 - 3.3 \mu K^{-1}$
Quartz	$0.5 \mu K^{-1}$
Borofloat	$3.25 \mu K^{-1}$

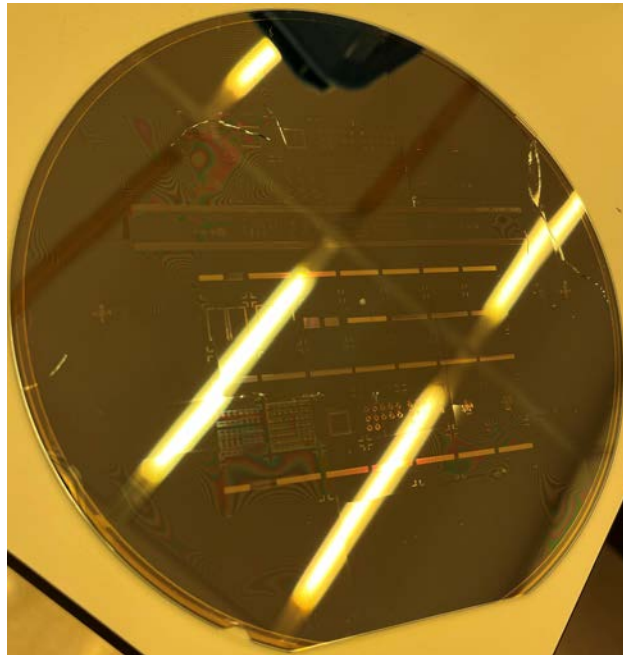


Figure 3.7: The quartz wafer cracking after the bonded stack cools.

Table 3.2: Manual Recommended Values Compared to Those of a Successfully Bonded Stack

Parameter	Manual Recommendation	Experimental Value Used
Temperature	$300 - 320^{\circ}C$	$300^{\circ}C$
Bond Pressure	1-7MPa	6.5MPa
Bond Time	2-15 minutes	15 minutes

breaking the SOI wafer. Therefore, the stack was diced. The whole stack could be diced into chips, but the pads were still inaccessible. A break in the SOI and Au trace is purposefully left such that the end effector can protrude from the stack, note the end effector in 3.4. However, a second opening is needed to contact the pads to control the device. Through glass vias (TGVs) could eliminate the need for the second opening, such that the entire structure is hermetically sealed except for the opening smaller than  $300\mu m \times 2\mu m$  that the end-effector

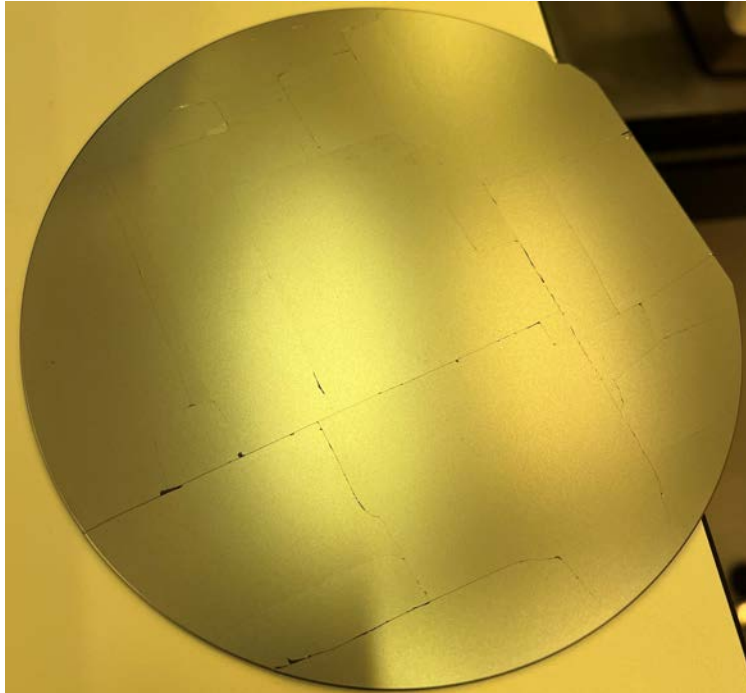


Figure 3.8: The SOI substrate cracking as the bonded stack cools.

protrudes from. However, a much simpler solution is to partially dice the glass wafer after fully dicing the bonded stack into chips shown in Fig. 3.9. The partial dice, 200 $\mu$ m deep, creates a stress concentration that is controllably broken with tweezers: providing a simple post-processing method to access the pads.

Initially, stress concentrations were made in the glass wafer and then the full-stack dices were made to singulate chips. However, the force of the full-stack dices caused the partially diced glass to break apart prematurely and the water jet of the dicing saw ruined all devices. Thus, the full-stack dicing must be done prior to the partial dices.

### **Post Process Bonding Glass to an SOI Chip**

The easiest solution to protect the MEMS device from physical and moisture failures is to attach a cover to each chip individually, rather than singulating a bonded wafer stack into chips. For example, run a typical SOI process with one added post processing step; frontside DRIE, backside DRIE, and HF release with an optional metallization step 1.2. Then, manually apply epoxy to a chip-sized piece of glass slide, and fix it to the SOI chip covering the fine features, while leaving the probe pads exposed. In addition, instead of using a glass slide, a micromachined SOI chip made in the same process could be bonded [16]. This is simpler than wafer bonding, because it is one extra step, and require no changes



Figure 3.9: Process flow showing how to create 2 chips and expose pads through a full and partial dice where grey is glass wafer and SiO<sub>2</sub>, yellow is Au, and green is Si.

to the fabrication process. However, it is not a wafer-scale solution. This can also provide an extra routing layer but requires larger bond pads because this alignment is dependent on the skill of the user: less than 100 $\mu$ m is achievable with the current micromanipulator.

### Changing Layout To Solve Contamination Failures

The simplest and most effective method to decrease failure due to contamination, without post processing nor changing the fabrication process, is to simply design for sufficient space between the fine movable components (springs and GCAs) and human skin.

Repeated exposure to human skin increases the distance that they moisture condenses, but after repeated trials they were never seen condensing more than 1mm from the skin that they originated from. The V1 design failed because 2 of the 4 retractions springs were placed less than 1mm from the edge of the chip. Redesigning such that there was more than 1mm was the easiest solution to solving the failure mode caused by moisture shown in the layout comparison of Fig. 3.3.

## 3.2 Conclusion for a Robust Tactile Stimulator

Ensuring a 1mm space is between the fine features of the device (retraction springs and GCAs) is the easiest way to prevent condensation failure. This was first fixed by removing

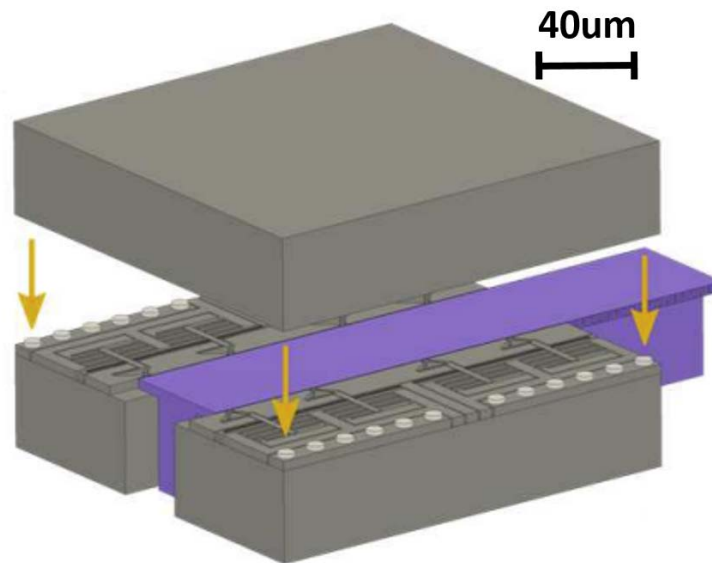


Figure 3.10: An 3D rendering from [16] showing simplified illustrations of the inchworm motor running after an SOI cap was bonded. The cover is bonded on top with dots of silver epoxy and the (purple) inchworm motor shuttle is still able to move after the bond.

the second pair of retraction springs from the V1 design that were closest to the end effector. However, fixing a cover to act as a physical and moisture barrier also protects against condensation. For small batches, this is best done by post processing single chips, but can be also accomplished by wafer bonding for higher volume manufacturing. Post process fixing a lid can be any material because the epoxy bonding is done at room temperature, but due to the elevated temperature in thermocompression bonding, a Si-matched TCE cover material must used for the wafer-scale solution. In addition, either chip or wafer scale bonding can provide an additional routing layer. This simplifies the wearable assembly by removing the need for jumpers between planar traces.

The main failure mode of the V1 device was contamination, which is mitigated by increasing the spacing around the edge of the chip in conjunction with a lid covering the MEMS components. This change in layout and process allowed for the tactile devices to be repeatedly used without failing due to condensation.

# Chapter 4

## Lessons Learned and Future Work

### 4.1 Integration

The keys to improving integration are connection and alignment. The current method is very labor intensive and difficult. It is possible to properly align an IC to the MEMS-CB, but is very difficult. In order to make it easier, and increase the yield, epoxy type and deposition method should be investigated along with a finer alignment tool and higher magnification microscope.

#### Connection Resistance and Reliability

##### Change the SOI Wafer

The easiest way to decrease resistance of connections is to use a lower resistivity SOI wafer. Experiments showed that with sufficient epoxy, the resistance from MEMS-CB SOI beam to IC pad was dominated by the resistance of the SOI beam. For example, if using an SOI wafer with a device layer doping of  $1e18$  instead of  $1e15$ , the connection resistance would be lowered to tens of Ohms, compared to thousands of Ohms, which would be suitable for this application.

##### Using Different Epoxies

In addition, different epoxies can be tested. Only 3 were tried and all had particle sizes in the same order of magnitude as the droplets: even highly conductive epoxies may not have many conductive particles in the applied droplet, due to the small amount of epoxy used. For example, if an epoxy particle size is  $30\mu\text{m}$ , but the epoxy droplet is  $40\mu\text{m}$  in diameter, it may still be a highly resistive connection. Therefore, nanoparticle epoxies should be explored. Other epoxies should also be considered on their viscosity. The alignment will become easier if the epoxies spread less when the IC and MEMS-CB come into contact, making sure that connections are only made where the alignment step dictates. This was a



major difficult in assembly as even when properly aligned, adjacent traces were shorting due to epoxy spreading.

## Alignment

The alignment can also be aided by including a fixture to the assembly setup. Making a structure where the alignment is not done by hand, but rather guided by a fixture would increase accuracy, speed and ease of assembly. Though it can be done by hand with the current micromanipulator, a finer micromanipulator, especially with a fixture to hold the two IC chips in place, would greatly increase the success of alignment. In addition a high magnification microscope would also increase the likely hood of successful assembly.

## 4.2 Simulation

The MEMS designs are based off of theoretical equations and working devices were found by making arrays of prototypes with varying parameters. Though this leads to a faster design cycle, it often takes more time due to dealing with unforeseen problems that could have been avoided through simulation, like the unaccounted moments shown in Fig. 4.1.

### Wafer Weighing Simulation

Though never fabricated, a cantilever with a Wheatstone bridge at its base designed for wafer weighing was simulated Fig. 4.3. The process could have been the same SOI process described above, but with two additional masks to pattern the oxide and doping layers in order to create the strain sensors 4.2. This was meant to precisely, 1ppm, weigh wafers while still in the etcher to accurately remove material. It's maximum force was designed to be 0.4N, and the minimum detectable force of 0.4uN simulated 63nV 4.4. This was never fabricated, but the simulation shows a measurable voltage with the set spec of 1ppm and 0.4N maximum force; the setup to simulate added time, but now there is more confidence in the design than if only theoretical equations were used. Further integrating simulation into the design flow is needed for more reliable design. In addition, the wafer-weighing cantilever should be fabricated based on the CoventorWare modeling.

## 4.3 SOI Wafers

### Lower Resistivity

As mentioned above, the current resistivity is 15-25 $\Omega$ \*cm; the fabrication process can remain the same but a different starting material can drastically decrease the connection resistance when assembling ICs into a MEMS-CB.

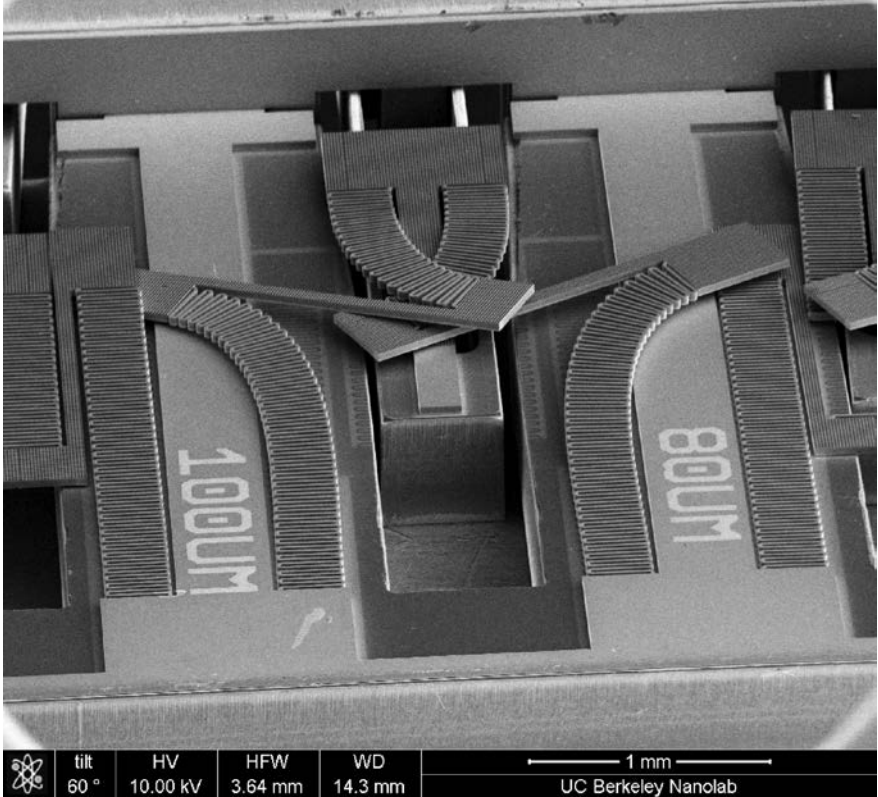


Figure 4.1: An image of Dr. Hani Gomez’s locking springs that became twisted due to an unaccounted moment [5].

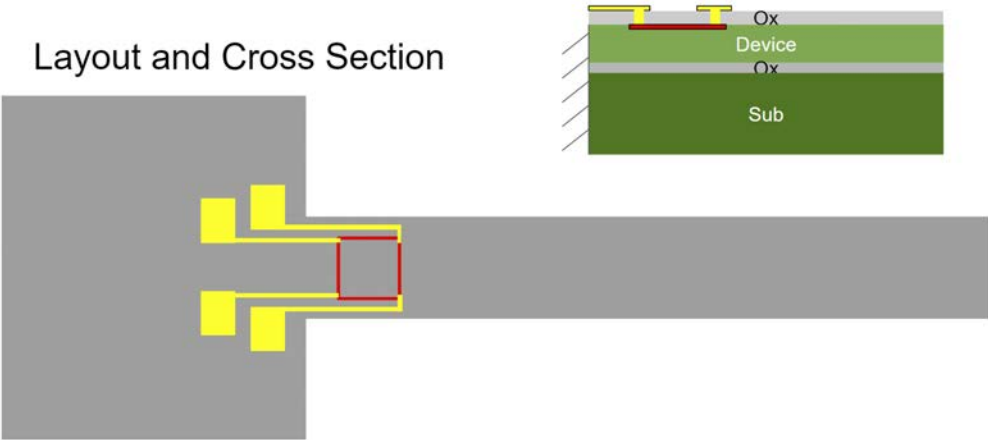


Figure 4.2: The layout and cross section of the device to be simulated.

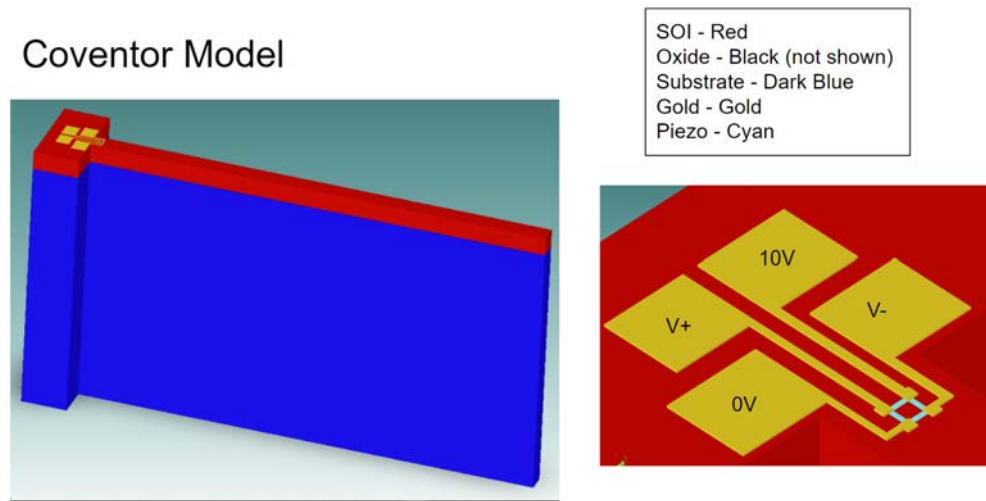


Figure 4.3: An overview of the cantilever’s design.

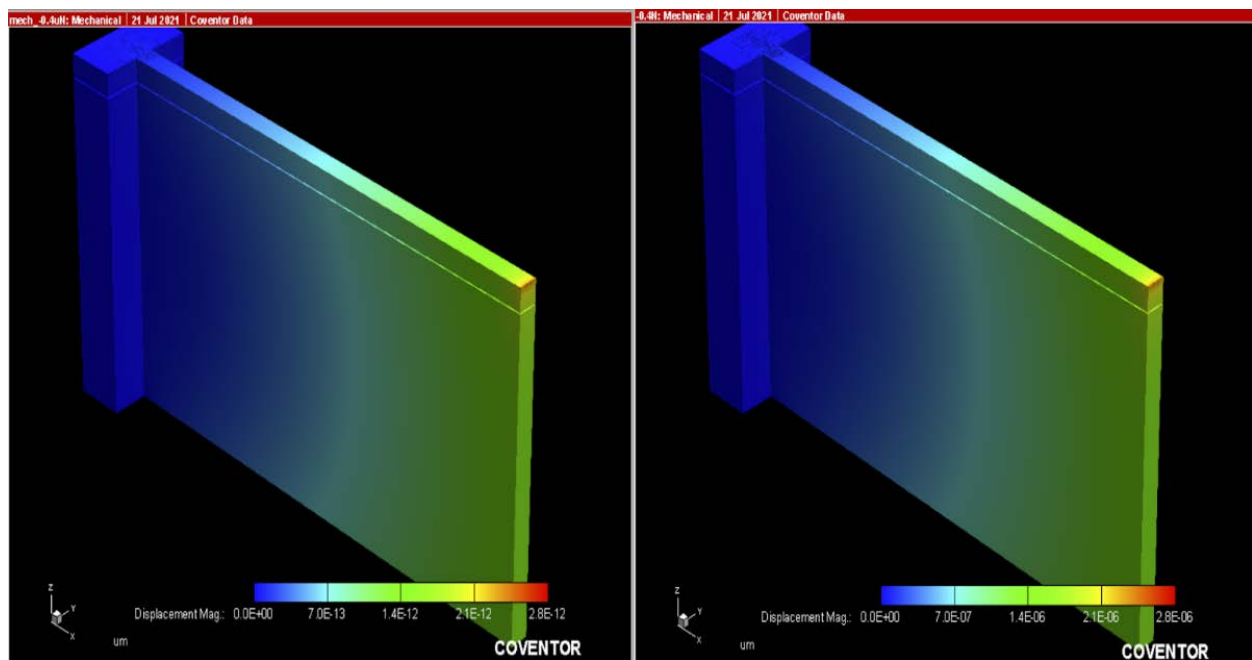


Figure 4.4: Two simulated displacements in CoventorWare. Left: designed minimum sensible force of 0.4 $\mu$ N. Right: designed maximum force of 0.4N.

## Annealing

Annealing all wafers upon receipt is not normally needed, as it should be done by the manufacturer, but can prove detrimental if skipped. In one fabrication run, after a 2 $\mu$ m HF

etch, many structures were free when they were designed to be stationary until a 6 $\mu\text{m}$  etch. This is was caused by the improper bonding of the Si to the SiO<sub>2</sub>. This is known by the anisotropic etch shown in Fig 4.5. HF etches SiO<sub>2</sub> isotropically, so the etch front should become more vertical as the etch progresses and the SiO<sub>2</sub> should etch laterally at the same rate as vertically. This image shows 30 $\mu\text{m}$  of lateral SiO<sub>2</sub> etching when it has yet to etch 2 $\mu\text{m}$  vertically.

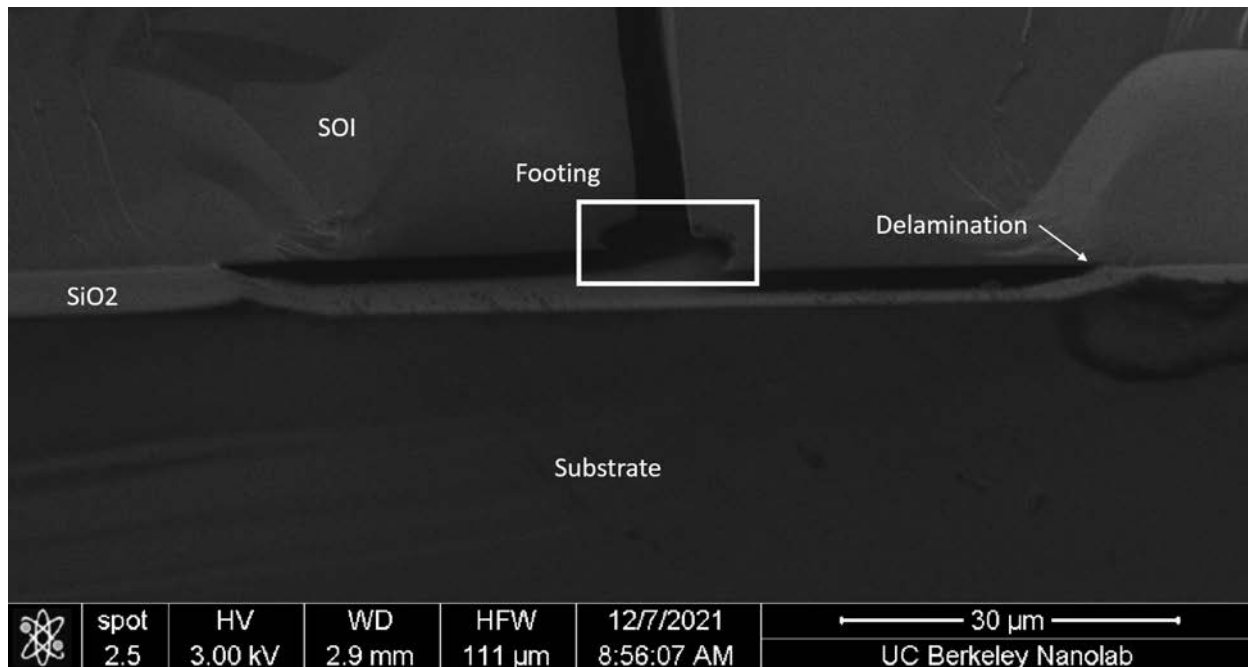


Figure 4.5: Cross section of an SOI wafer that shows footing of a DRIE trench and the delamination of Si from SiO<sub>2</sub>. The SiO<sub>2</sub> layer is 2 $\mu\text{m}$  and though some remains, it has been laterally etched 30 $\mu\text{m}$ .

## Problems with vapor HF

Vapor HF has been used to etch SiO<sub>2</sub> and release the Si structures, but has intermittently caused problems such as an inconsistent etch rate. Some features moved freely, while others of the same size remained fixed, and more moved erratically, like they were catching on something. The Si features were removed and imaged in the SEM showing unetched SiO<sub>2</sub>: Fig 4.6. This was not an isolated event and the tool has even had issues when it was raining because of how it measures pressure. A wet HF etch may result in stiction, but that has not been tested, and it will certainly etch more consistently. Also, if nitride is introduced into the process for more advanced anchoring, or other applications like CMOS integration, vapor HF should not be used as it will cause the nitride to swell because it is an anhydrous

reaction. Adding as much Si to the nitrogen mitigates this, but its best practice to avoid using vapor HF with SiN.

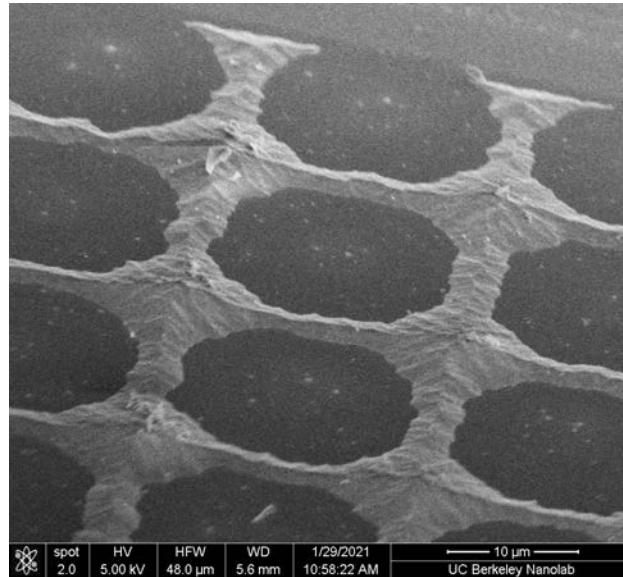


Figure 4.6: Unetched SiO<sub>2</sub> on the Si substrate that caused device Si, that was supposed to be released, to catch as it moved.

## DRIE Optimization

The current method of etching the front and backside Si of the SOI wafers relies heavily on the expertise of the operator, and can be optimized. Underetching is detrimental and leads to device failure. This is because if the Si is not etched down to the SiO<sub>2</sub>, the Si is not free to move Fig 4.7. It is difficult to measure whether or not the etch has completed in trenches smaller than 10μm without breaking the wafer. An optical imager Olympus has been somewhat successful, but as 4.9 shows, it struggles to measure the 8μm etch holes because of their size and the SiO<sub>2</sub>. Thus, it is better to overetch the Si; however, this is not without its drawbacks. Fig 4.10 the topside of a feature and appears as drawn in layout, however, Fig 4.11 is the bottom side of that feature - showing a large overetch. This overetch leads to undercutting features, which causes device performance further from simulation. In addition, thinner features, like springs, vaporize due to the heat caused when the undercut separates them from the SiO<sub>2</sub>: they are unable to cool through the substrate and the photoresist burns off resulting in what is shown in Fig. 4.8.

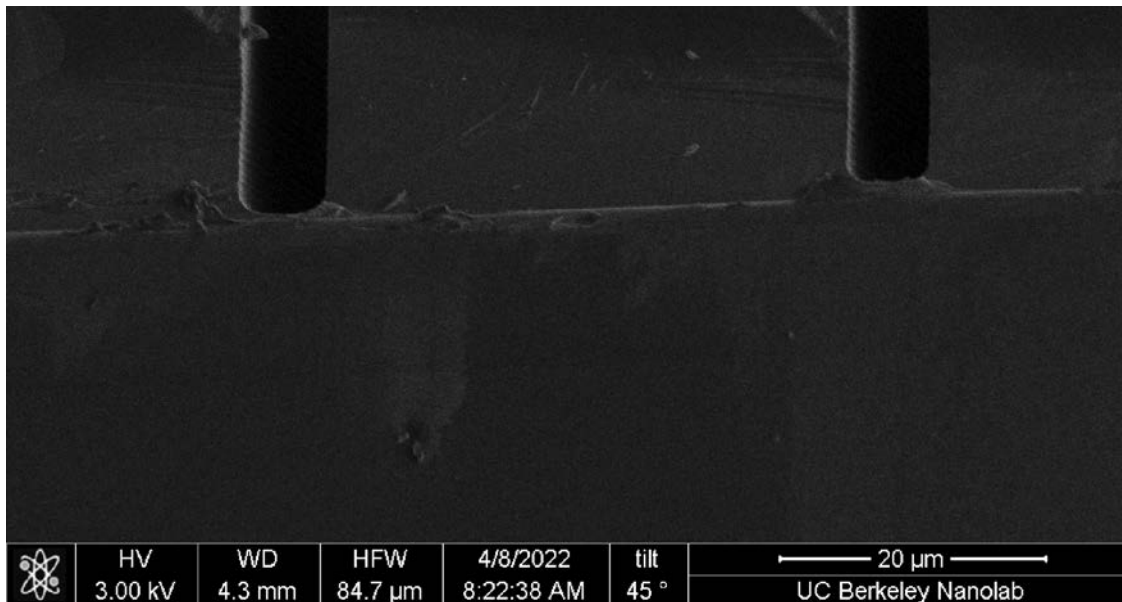


Figure 4.7: Two DRIE trenches that did not etch down to the SiO<sub>2</sub> layer, resulting in all devices on the wafer not functioning.

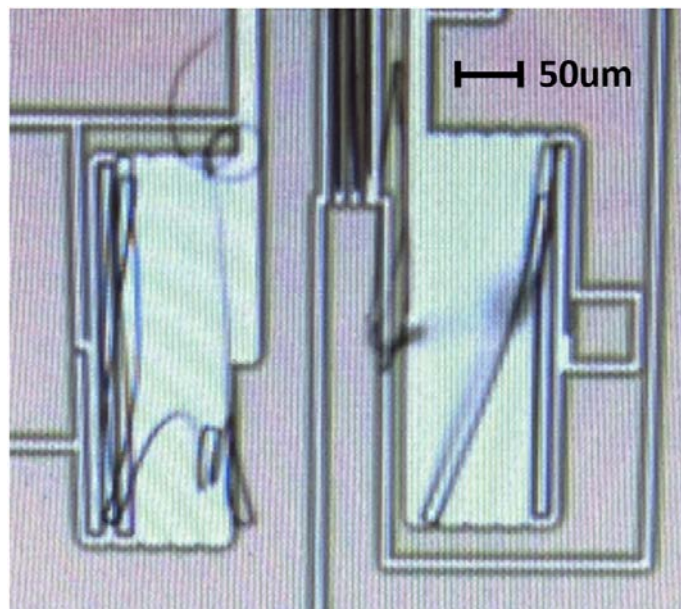


Figure 4.8: The serpentine springs after the overetch in the DRIE caused them to overheat and burn off the photoresist defining the structure.

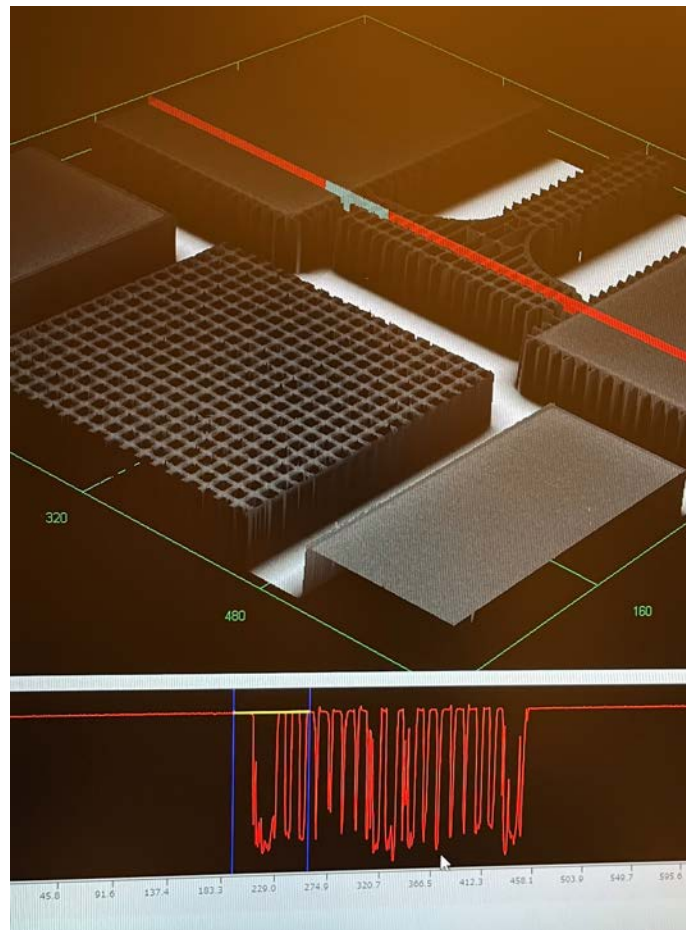


Figure 4.9: Screenshot of Olympus measuring SOI features that have not completed their etch. The top image is a 3D optical scan of the SOI features, where the red line shows the cross section plane of the etch holes shown below. It does not appear that etch holes completed their etch, but further etching does not change the clarity on this tool.

### **Avoid under- and overetching with a 3 wafer solution**

A better method of DRIE uses 3 SOI wafers, but yields more consistent results. First, DRIE the SOI wafer with high frequency (HF) cycles until the field clears. Cleave this wafer to find the remaining depth on the minimum sized feature. Next, etch a second SOI wafer the same number of HF cycles as the first, then low frequency (LF) etch 1/4 of the HF cycles. Again cleave and note the change in depth caused by the LF cycles. Linearly extrapolate this to get the exact number of needed cycles for the third SOI wafer. DRIE is dependent on the exposed pattern so this should be done each time the mask is changed.

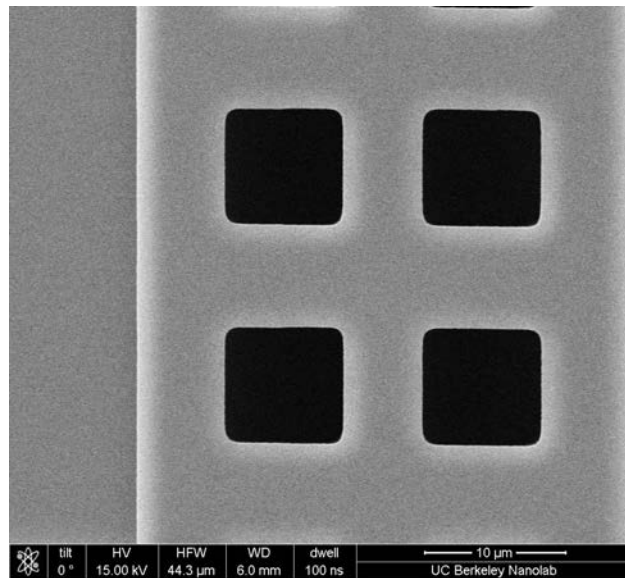


Figure 4.10: The topside of a feature, which looks as drawn.

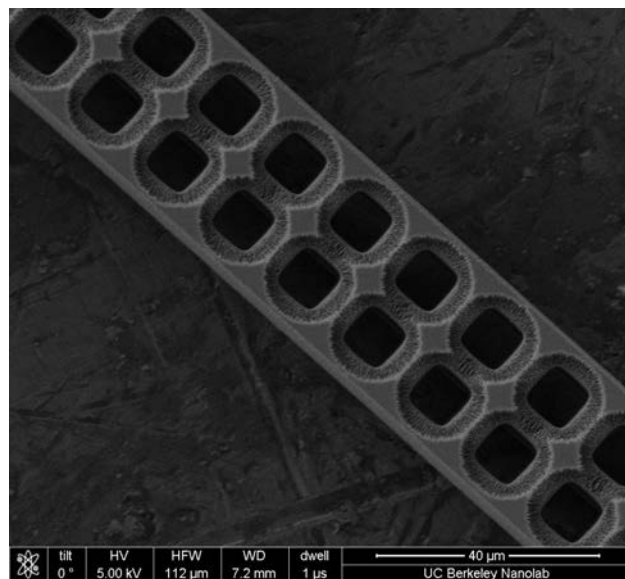


Figure 4.11: The bottom of the same feature, showing extreme footing. The circular shapes around the squares are where Si was etched due to ions bounding off of the SiO<sub>2</sub> and removing the Teflon passivation.



## 4.4 Conclusions

Making electronics is difficult. That difficulty only increases when multiple parts are integrated, especially when exposed to a harsh environment like the human skin. Though unsuccessful, many components to make a wireless tactile actuator the size of an aspirin are in this thesis.

To make the wearable, the assembly failures are likely solved with a finer micromanipulator, high magnification microscope and a more viscous epoxy. Experiments showed that alignment is possible with the current tools, but is labor intensive; the spreading of epoxy when pressing the IC and MEMS-CB into contact shorted adjacent traces or too little epoxy was deposited to make a measurable connection. In addition, more precise and automated epoxy depositions would aid in the ease of assembly. Also, replacing the device SOI with a high conductivity wafer would decrease resistance between integrated components. Experiments showed that with an excess of epoxy, the resistance from MEMS-CB SOI beam to IC pad was dominated by the resistance of the SOI beam. The current resistivity is  $15\text{-}25\Omega\cdot\text{cm}$ , but the process can remain the same when using a lower resistivity SOI wafer, which can drastically decrease the connection resistance.

To utilize on-chip relays to replace SCuM and Zappy, further investigation into a conductive, hard, and non-sticky contact material is required to be implemented in a system controlling inchworm motors. Sputtered Ruthenium, Chrome and Titanium-Nitride films of 30, 50, 100 and 200nm films were tested and a 100x decrease in resistance was seen, in a change in applied voltage, the capacity to be hot switched above 5v was not observed. Hot switching above 30v is needed to adequately provide force with an inchworm motor. Therefore, the best way to construct the wearable is to continue to use SCuM and Zappy.

After assembling a working wearable, it is critical to increase the robustness of the most sensitive component: the MEMS device. This can be done by increasing the spacing around the edge of the chip in conjunction with a lid covering the MEMS components, which best protects the device from failure cause by moisture and physical damage. Increasing the spacing between the edge of the chip and fine MEMS features is a layout change that minimally increases the chip size. Adding a cover is a simple process change that better protects the MEMS components because it also acts as a physical barrier. This cover can be applied at the wafer-scale, with less than 10um misalignment, but the process is more complex and the cover material is then limited to a material with a similar TCE to Si. An easier solution was found to cover the chips after singulation. Though not a high volume solution, it is easier than singulating a bonded wafer into chips, can still provide a second routing layer, and can be assembled with less than 100um of misalignment with current tools.

This information can be used to make a wearable device that is more than just a binary vibration sensation currently available; it could provide a precise tactile stimulation. Imagine all of the different physical surfaces touched in a single day. Mimicking those to create a more realistic virtual reality, for example, will require more precise stimulation than just vibration. Investigating other ways to electronically control tactile stimulation is critical to better communicate information via touch.

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## Appendix A

# AML AWB-08-30 Wafer Bonder Manual Chapter on Thermocompression Bonding

The the relevant pages regarding Au-Au thermocompression bonding in the 377 page manual bonder user manual are included below.



## 14.2 Gold to Gold Thermocompression Bonding

### Benefits

- No molten layers during the bond process.
- Keep integrity of structures in glass and Si
- Good thermal coupling between substrates
- Simple metallisation process

### Disadvantages

- Requires an intimate contact between gold layers – bond layer cannot accommodate surface topography or roughness
- Very high pressures / forces requires between the wafers
- Good surface finish required – needs smooth surface – low roughness – low particle density
- Not a very high strength bond

### Conditions

<b>Upper Wafer Temperature</b>	320°C
<b>Voltage</b>	N/A
<b>Lower wafer temperature</b>	300°C
<b>Bond mechanism</b>	Plastic flow of gold layer creates "cold weld" between the wafers.
<b>Bonding Environment</b>	Compatible with all pressure ranges. Inert gas.



**Design Rules**

<b>Material properties</b>	A "soft" Au coated layer is required on both wafers. Preferable that the Au is deposited with low stress and annealed to maximise grain size.		
	<b>Au thickness</b>	0.5 - 1µm Au layers below 500 nm strength decreases rapidly.	
	<b>Adhesion layer</b>	Titanium recommended	
	<b>Barrier layer</b>	Platinum recommended to prevent Si diffusion into gold layer	
<b>Min Wafer Thickness</b>	100µm	<b>Min Width</b>	50mm (75mm for alignment)
<b>Max Total Stack Thickness</b>	8mm	<b>Max Width</b>	200mm
<b>Number of wafers in a stack</b>	No limit, but two substrates per bond process		
<b>Suggested cleaning methods</b>	<ul style="list-style-type: none"> <li>• SC1</li> <li>• Propanol</li> </ul>		
<b>Do not Use</b>	Piranha solution if Chromium is used as adhesion layer		
<b>Effect of particles</b>	Severe		
<b>Alignment method / accuracy</b>	IR	± 1 µm for double side polished wafers	±10µm for single side polished wafers.
<b>Maximum permissible surface roughness</b>	R <sub>a</sub> (nm) 2	P-V (nm) 100	
<b>Preferred surface roughness</b>	R <sub>a</sub> (nm) 1		
<b>Wafer bow</b>	Upper wafer 200µm. Lower wafer no limit.		
<b>Temperature conditions</b>	~ 300-320°C		
<b>Pressure range required</b>	Pressures between 1MPa and 7MPa required. Higher pressure required for rougher surfaces / higher pressure may give more reliable bond / higher bond strength. <b>Note that the gold layer needs to be patterned to form bond frames with total area consistent with the max force capability of the bonder.</b>		
<b>Bonding time</b>	~2-15 min		
<b>Cycle Time</b>	~ 25-45 min		



<p><b>Presence of surface layers / layer type and thickness</b></p>	<p>Layer beneath Au is important – diffusion of Cr through the Au layer can interfere with Au properties – harden the layer. Also, diffusion of silicon into the gold layer may cause hardening.</p>
<p><b>Process Yield (High / Medium / Low)</b></p>	<p>Medium</p>
<p><b>Other information worth keeping note of: Compatible materials</b></p>	<p>Good force uniformity is needed. Large forces are required.</p>
<p><b>Any Safety concern (e.g. generation of toxic gas)</b></p>	<p>None</p>
<p><b>Other process notes</b></p>	<p>For a hermetic seal, a continuous bond frame of minimum width 100µm is required around the area to be sealed</p> <p>Figure 1: Active ASIC Area Surrounded by 100µm Air Gap and 100µm Bonded Area All active circuitry must be completely contained within the bond frame. A minimum 100µm is required between bond frame and the edge of active region (Fig 1). Feedthrough vias must be surrounded by a bond frame (ring) of min. width 100µm (Fig 2).</p> <p>Figure 2: ASIC Bond Pad Surrounded by 50µm Air Gap and 100µm Bonded Area If bond pads are accessed through cap wafer the only feature permitted within via is the ASIC bond pad. Minimum space between bond pad and via edge must be &gt;50µm (Fig 2). All areas to be bonded must be at the same height with respect to substrate. Hence bonds are made to the</p>



same layer within ASIC structure.

