Micro-Electro-Mechanical Relay Technology for Beyond-Von-Neumann Computer Architectures

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Technical Report No. UCB/EECS-2022-251
http://www2.eecs.berkeley.edu/Pubs/TechRpts/2022/EECS-2022-251.html

December 1, 2022

Micro-Electro-Mechanical Relay Technology for Beyond-Von-Neumann Computer Architectures

by

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A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

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Spring 2022

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Abstract

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The invention and development of complementary metal-oxide-semiconductor (CMOS) transistor technology for digital computing have led to a global information technology revolution and economic boom, which have shaped modern society. However, transistor leakage current (I_{OFF}) and limited subthreshold swing set a fundamental limit on the energy efficiency of digital computing today. Micro-electro-mechanical (MEM) switches (relays) previously have been shown to be promising for energy-efficient digital computing applications, due to their abrupt ON/OFF switching characteristics and negligible OFF-state leakage current.

This dissertation focuses on novel applications of MEM relays for facilitating new computer architectures that can be much more efficient than the classic von Neumann architecture. First, MEM relays are demonstrated to operate reliably with millivolt signals at cryogenic temperatures, due to much lower hysteresis voltage and more stable ON-state resistance. A sub-10 mV relay-based inverter circuit is demonstrated at a temperature of 4 K. Our experimental study indicates that MEM relays should be able to operate at temperatures as low as 1.8 K, making them promising candidates for ultra-low power cryogenic digital interface circuits for quantum computing.

Then superconducting MEM relays using niobium (Nb) as the contact material are investigated, in order to further reduce the operation power consumption for quantum computing applications at cryogenic temperatures. The detailed fabrication process flow is shown, and temperature-dependent measurements are conducted to check the superconductivity of the Nb electrodes.

Finally, DC-voltage-driven oscillatory behavior of MEM relays is investigated via experimental study and finite-element-method-based computer simulations. Sub-harmonic injection locking and coupled oscillation behaviors of MEM relays are demonstrated, indicating that MEM relay oscillators are promising for implementing Ising machines, which can solve large-

scale combinatorial optimization problems much more efficiently than conventional computer architectures.

To my grandparents and parents

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Acknowledgments

First and foremost, I am extremely grateful to my advisor, Professor Tsu-Jae King Liu, who provide me with inspiring guidance and constant encouragement throughout my graduate studies at UC Berkeley, and act as a role model for me not only in academic but also in life. Her knowledge and creativity in the semiconductor field, motivation and enthusiasm to push the technical boundary, and kind personality and thoughtfulness to people, are all precious lectures in my life. I hope one day I can become a person like her, and be able to make changes not only in the technical world, but also encourage younger generations to pursue their dreams.

I would also like to thank Professor Ming Wu and Professor Junqiao Wu for serving on my dissertation committee and qualifying examination committee, and providing me with invaluable feedback and guidance on my research projects. I would like to thank Professor Ana Claudia Arias for being the committee member for my qualifying examination and preliminary examination, and providing me with frequent guidance and encouragement. I am grateful to Prof. Vivek Subramanian for advising me on my Master's thesis and strengthening my ability to think and study independently as a graduate student. Additionally, I am grateful to Profs. Jeffrey Bokor, Sayeef Salahuddin, Chenming Hu, Ali Javey, Rikky Muller, Clark Nguyen, and Jaijeet Roychowdhury for their technical support, career advice, and excellent courses in the field of electrical engineering.

I also appreciate Professor Muhammad M. Hussain for giving me the opportunity to teach the semiconductor fabrication laboratory (EE 143), and helping me to better enhance my knowledge and experience in modern semiconductor process technology. I would also like to thank Dr. Arash Nourian and Dr. Ed Henrich for providing me with the opportunity to serve as a graduate student instructor for Data-X (IEOR 135) and get a better understanding of state-of-the-art data science and machine learning techniques while teaching.

Additionally, I would like to thank the entire King Liu research group. With the help, discussion, and encouragement from Dr. Sergio Almeida, Dr. Zhixin Alice Ye, Dr. Benjamin Osoba, Dr. Urmita Sikder, Tsegereda Esatu, Lars Tatum, Dr. Xi (Robin) Zhang, Dr. Fei Ding, Dr. Thomas Rembert, Dr. Hei Kam, and Dr. Min-Wu Kim, I had a lovely journey at Berkeley. I would also like to thank Qianyi Xie for being a reliable nanolab buddy for me, discussing the process difficulties with me, and providing me with help for my experiments. I would like to thank Dr. Siqi Wang, for helping me with cryogenic measurements. I also would like to thank friends that I met in nanolab, including Yichi Zhang, Junjie Hu, Zeying Ren, Xiangli Jia, and Jason Wu, for spending time in the amazing world of nanofabrication together.

In particular, I would like to appreciate UC Berkeley Marvell Nanofabrication Laboratory staff – including Dave Taosaka, Allison Dove, Richelieu Hemphill, Ryan Rivers, Sam Tsitrin,

Jay Morford, Jason Chukes, Joanna Bettinger, and Bill Flounders – for helping me to learn the fabrication equipment, analyze the process problems in the fabrication, and maintain the working status of the equipment. I especially appreciate the rapid help from Greg Mullins, Danny Pestal, and Ming Wong for EE 143 labs.

I am sincerely grateful to the EECS administrative staff. In particular, I would like to thank Shirley Salanio, for supporting me with different petitions, personal questions, useful information, and positive encouragements.

In addition to the above, I want to thank my friends, classmates, and colleagues for providing me with ideas, help, creativity, and friendship on my course projects, teaching experience, and graduate life, including Dr. Xiaosheng Zhang, Dr. Danqing Wang, Yu Sun, Andrew Aikawa, Wanwoo Noh, Dr. Yu-Hung Liao, Mahan Tajrobehkar, Dr. Ming-Yen Kao, Shikun Shen, Kevin Zheng, Xintian Liu, Ziyu Xiang, and Zheyu Lu. I would also like to thank Harikrishnan Rajagopal, Minal Shettigar, Isabel Li, and Arvind Shankar from Applied Materials, Inc., for teaching me a lot during my internship in Summer 2020. I appreciate the help from Dr. Yuxuan Cosmi Lin, Dr. Danping Peng, Thomas Li, Josh Maher, Dr. Milind Gadre, Dr. Dejiu Fan, and Qinyue He during my job hunting time.

I would also like to thank my favorite video/mobile games: Genshin Impact, Counter-Strike: Global Offensive, and Pokémon GO. I enjoyed the beautiful scenery I saw, the sweat and practice I spent on leveling/ranking up, and the interesting people I met in these games.

Finally, I am tremendously grateful to my family for their unconditional love and ceaseless support. I want to thank my grandparents for all the efforts and sacrifices they provided when I was young, and also during this Ph.D. study. Thanks must also go to my parents. Although they don't have an electrical engineering background, they tried their best to understand the semiconductor fabrications that I was doing, and encourage me to chase my dream. Without their understanding, encouragement, and support, I would never have had a chance to complete this Ph.D. journey. I want to thank Guanglong Huang, for emboldening me to overcome all the obstacles and get through all the dark moments during these years. His accompanying helps me to realize how beautiful and sweet my world is.

Chapter 1

Introduction

1.1 Introduction: Digital Integrated Circuits and Next-Generation Computing

Integrated circuit "chips" are the electronic brains used in all computing devices today, and Complementary Metal Oxide Semiconductor (CMOS) Field Effect Transistors (FETs) are the predominant type of transistors utilized in all computing chips. Steady advancement in CMOS manufacturing technology has resulted in a global information technology revolution that has shaped modern society [1]. In 1967, Gordon Moore observed that the number of CMOS transistors on the leading microprocessor chip doubles every 18 months [2]; in 1975, he revised this to a more realistic two years [3]. This observation has since become known as Moore's law, and the exponential pace of increasing transistor count per chip has been sustained for more than five decades by the semiconductor industry; as a result, microprocessor chips have become more functional and energy efficient over the past half-century. The first commercially produced microprocessor chip, the Intel 4004, was released in 1971 and fabricated using a 10 µm generation process; it comprised approximately 2000 transistors [4–6]. More than 50 years later, the Apple M1 Ultra, unveiled in March 2022, comprises 114 billion transistors and is fabricated using a 5 nm generation process at Taiwan Semiconductor Manufacturing Company [7, 8].

The end of Moore's law will herald a new era of information technology advancement, as the emphasis of research and development shifts away from scaling down transistor dimensions and toward innovation of new devices, new device integration approaches, and new computing architectures, to sustain the exponential pace of improvement in computational ability [9, 10].

Quantum computers have the potential to effectively solve problems that are intractable for classical computers [11–13]. For example, in 1994, Peter Shor demonstrated that quan-

tum computers are capable of effectively factoring numbers in polynomial time [11], posing a severe threat to the RSA public-key cryptosystem that is widely used for secure data transmission, which relies on the fact that classical computers, even when equipped with the most efficient algorithms, are incapable of factoring integers with a length of 1000 decimal digits [14]. Quantum computers would also have a significant impact on fields such as quantum simulation [15] and machine learning [16–18].

In a classical computer, information is encoded as a binary number or string of binary digits (bits). The state of each bit is represented as a voltage level: a high voltage corresponds to a bit value of '1' and a low voltage corresponds to a bit value of '0'. A bit can only take a single value at a time [19]. Quantum computers manipulate qubits, which leverage quantum mechanical effects to store more than one state in a single qubit via the principle of **superposition**. That is, a qubit has the ability to superpose multiple states with varying probabilities (for example, 40% 0 and 60% 1) like Schrödinger's cat [19, 20], and we cannot predict which state it is in. But the instant when we measure it, it collapses into one of the definite states.

For a classical computer, for example, if there are 4 bits, there are 16 possible combinations of bit values, and only one of them can be utilized at a time, as seen in Figure 1.1 (a). In contrast, 4 qubits in superposition can each be in any of those 16 combinations simultaneously, as illustrated in Figure 1.1 (b). Moreover, this number grows exponentially with each additional qubit, so 20 qubits can store 2^{20} (more than one million) values in parallel [21]. Therefore, a quantum computer with N qubits can be 2^N times more efficient than a classical computer with N bits.

Figure 1.1: Comparison of (a) 4 bits in classical computers that each can only represent 1 possible value at a time, and (b) 4 qubits in quantum computers that each can represent all 16 combinations at the same time.

There are several approaches to implementing quantum computers, including superconducting qubits [13,22–25], polarized photons [26–30], trapped ions [31–34], and electron spins in silicon [35,36]. Among all the different approaches, superconducting qubits, in particular, are considered as the most promising candidate for achieving a scalable quantum processor architecture, due to high designability, scalability, fast and reliable operation, and ability to be coupled and controlled easily [13,37].

A CMOS-based digital integrated circuit can be used to control and read information out of quantum processor, but typically is designed for room temperature operation. The number of interconnections between the refrigerated quantum processor and the external CMOS controller constrain the number of qubits that can be used [38, 39]. The CMOS controller circuitry can be located in the refrigerator together with the quantum processor at cryogenic temperatures, but may dissipate heat that detrimentally affects qubit operations.

Previous studies have shown that micro/nano-electro-mechanical (M/NEM) relays can operate at much lower voltages (50 mV and below) than required for CMOS transistors, and have negligible OFF-state leakage current (in contrast with CMOS transistors), so that they are a promising candidate for Internet of Things (IoT) applications which require ultra-low-power consumption [40–46]. Therefore, MEM relays can also be an attractive candidate to build logic controllers for quantum computing, if they can be operated reliably at cryogenic temperatures.

Another attractive non-von Neumann computing architecture is the Ising model, which can efficiently solve a large number of discrete optimization problems across a wide range of fields: very-large-scale integrated circuit design, drug discovery, capacity planning, sensing, and manufacturing [47]. Many of these combinatorial optimization problems are so-called nondeterministic polynomial time (NP)–hard or NP-complete problems [48]. NP-hard or NP-complete problems are challenging for conventional digital computers to solve efficiently with heuristic or "greedy" algorithms [49, 50]. As Figure 1.2 (a) shows, von Neumann computers use programs to solve problems in a step-by-step repeated manner; as a result, the number of computing steps and the total computing time will drastically increase when the problem size becomes large. On the other hand, these problems can be mapped onto Ising models (Figure 1.2 (b)) and solved by finding the ground (minimum energy) state of the corresponding Ising Hamiltonian (Figure 1.2 (c)) [51, 52]. As a result, Ising machines have attracted increasing interest as physical solvers for this type of minimization problem, due to their high calculation speed and energy efficiency.

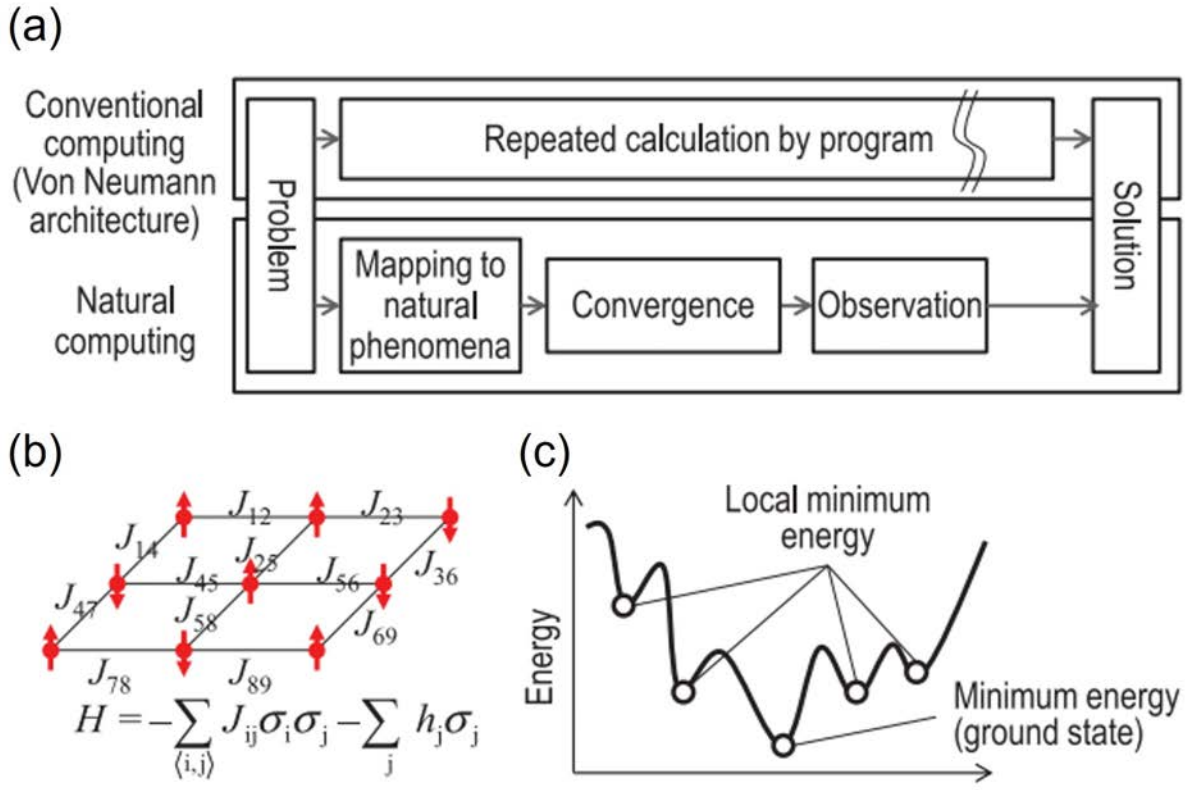


Figure 1.2: Computing paradigms: (a) Procedure-based approach to solving problem in conventional computing architectures and "natural" computing architectures. (b) A 9-spin Ising model. (c) The energy profile of an Ising model. Adapted from [50].

An Ising machine comprises a set of 'spins' - each of which can take one of two values - that are coupled together. The 'spins' can take many forms, including optical parametric oscillators [49, 53], qubits [54–57], CMOS circuits [50], and electronic oscillators [58–60]. A micro-electro-mechanical (MEM) relay can be made to function as an oscillator, and therefore can potentially be used to implement Ising machines for solving complicated combinatorial optimization problems.

1.2 Why Micro-Electro-Mechanical (MEM) Relays?

Figure 1.3 (a) shows the drain current vs. gate voltage semi-log plot of two n-channel MOSFETs with different threshold voltages (V_{th}), and for an "ideal switch". The subthreshold swing (SS) of conventional CMOS transistors is fundamentally limited by Boltzmann statistics to be no steeper than 60 mV/dec at room temperature. The OFF-state leakage current of a MOSFET, I_{OFF}, is the drain current when $V_{GS} = 0$ V and $V_{DS} = V_{DD}$, where V_{DD} is the power-supply voltage. I_{OFF} increases exponentially with a reduction in V_{th}:

$$I_{OFF} = I_O \times 10^{-\frac{V_{th}}{SS}} \tag{1.1}$$

where I_O is defined as the current when $V_{GS} = V_{th}$.

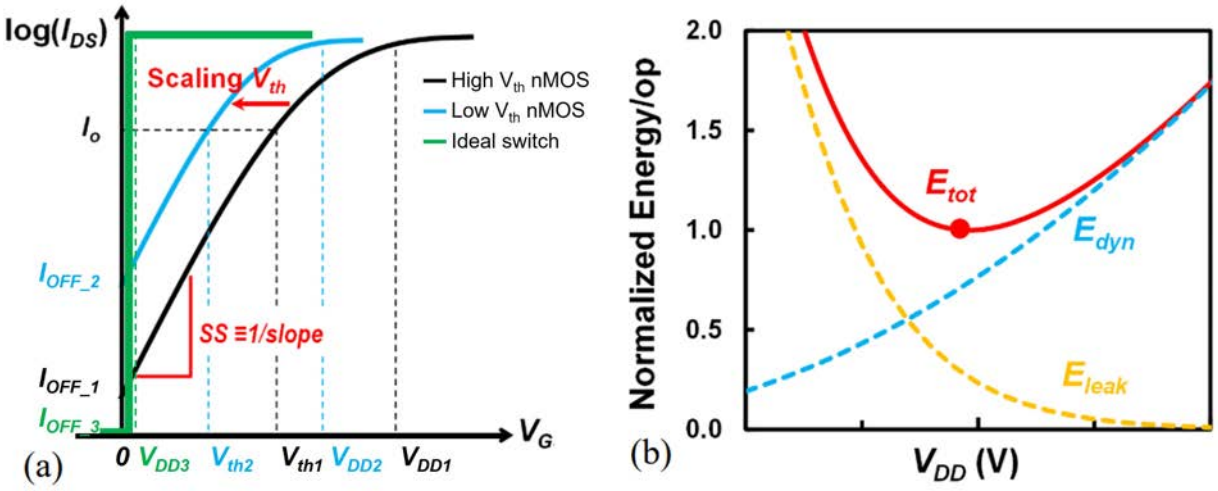


Figure 1.3: Conceptual illustrations of (a) transfer I-V characteristics of a high V_{th} n-channel MOSFET, a low V_{th} n-channel MOSFET, and an ideal switch; (b) normalized dynamic, static, and total energy consumed by a CMOS digital logic circuit to perform a digital operation, as a function of the supply voltage V_{DD}, showing the tradeoff between dynamic energy and static energy resulting in a minimum for total energy consumed. Reproduced from [40].

From Figure 1.3 (a), it can be seen that a reduction in V_{DD} to reduce the dynamic power consumption of a CMOS digital circuit would result in lower ON-state current (which is undesirable because it results in slower digital circuit operation) unless V_{th} is also reduced - but this would result in higher I_{OFF} (cf. Equation 1.1) which undesirably increases static power dissipation. Thus, energy wasted due to static power dissipation (defined as E_{leak}) increases as V_{DD} is reduced, as illustrated by the yellow curve in Figure 1.3 (b), while energy consumed to perform a digital operation (E_{dyn}, illustrated by the blue curve in Figure 1.3 (b)) is reduced. Therefore, the total energy consumed (E_{tot}) by a CMOS digital logic circuit has a fundamental lower limit. This limit exists due to transistor OFF-state leakage and limited SS. Therefore, an ideal digital logic switch should have zero I_{OFF} and a steep switching characteristic like the green curve shown in Figure 1.3 (a), which enables ultra-low voltage operation.

A MEM relay has abrupt switching characteristics (enabling lower V_{DD} and therefore lower E_{dyn}) and negligible OFF-state leakage current (eliminating E_{leak}). This is because an air gap physically separates the conducting electrodes (source electrode and drain electrode) in the OFF state, as illustrated in Figure 1.4 (a), so that no leakage current can flow between these electrodes. To turn ON the relay, a voltage is applied between the gate and body

electrodes, which induces an electrostatic force (F_{elec}) that actuates the movable conducting electrode into physical contact with a fixed conducting electrode, as illustrated in Figure 1.4 (b). Therefore, the relay current increases abruptly when the gate voltage reaches the turn-ON voltage, V_{ON}. This process is marked with the green arrow in Figure 1.5. To turn OFF the relay, the gate voltage is reduced so that the spring restoring force (F_{spring}) of the deformed movable electrode actuates it out of contact. Due to the existence of contact adhesive force, F_{adh}, the turn-OFF voltage (V_{OFF}) is smaller than the turn-ON voltage. This turn-OFF process is marked with the orange arrow in Figure 1.5. The minimum gate voltage swing to switch a relay ON/OFF is the difference between V_{ON} and V_{OFF}, which is defined as hysteresis voltage, V_H.

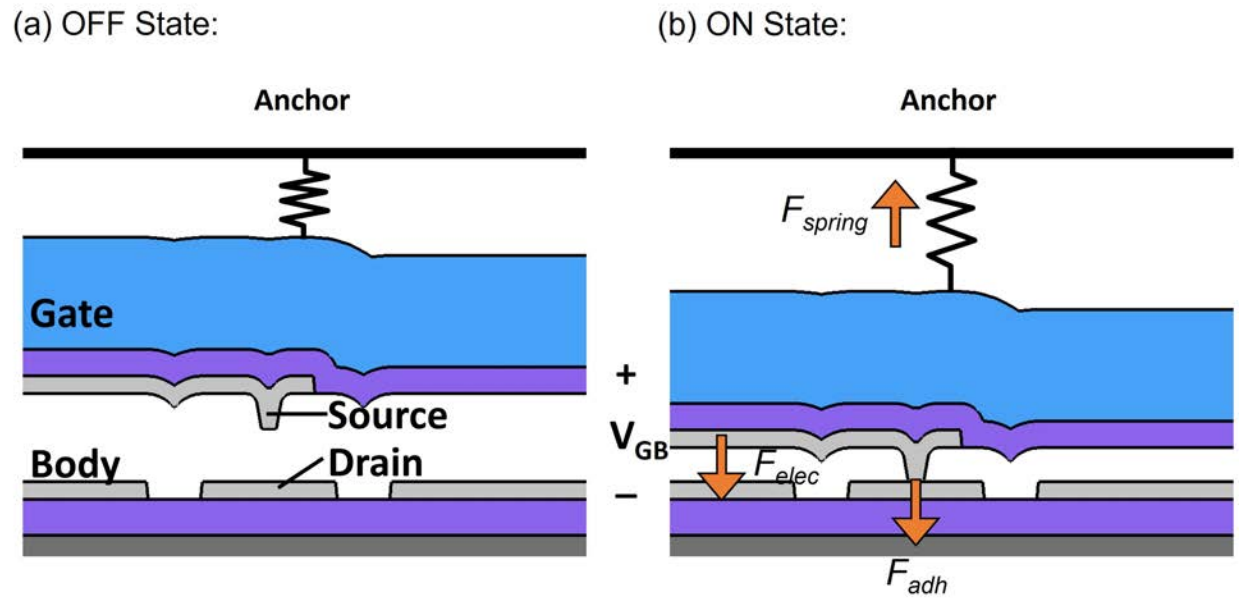


Figure 1.4: A simplified illustration of MEM relay working mechanisms in (a) OFF-state and (b) ON-state.

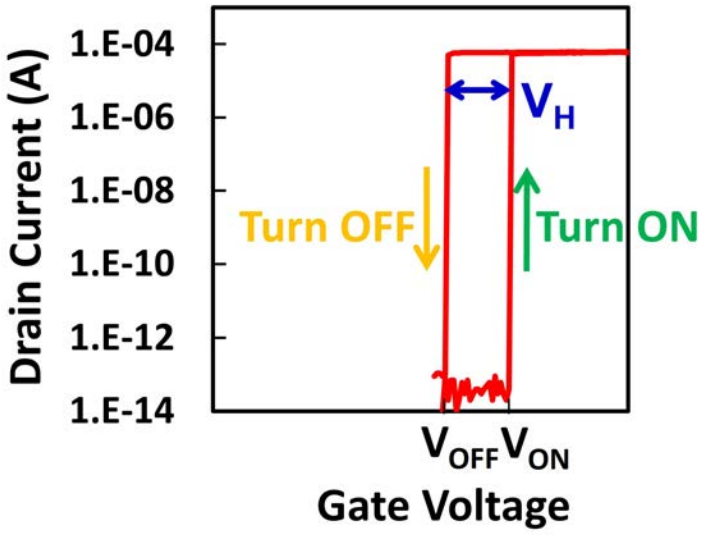


Figure 1.5: A typical I_{DS} -vs.-V_G characteristic of a MEM relay, with immeasurably low I_{OFF} and abrupt switching behavior.

1.3 MEM Relay Design and Operation

The simplified parallel capacitor model of a MEM relay is shown in Figure 1.6. The distance between the top plate and the bottom plate is labeled as g_o. The air gap between the source electrode and drain electrode is marked as g_d. The top plate is mechanically suspended through a spring with an effective spring constant of k_{eff}.

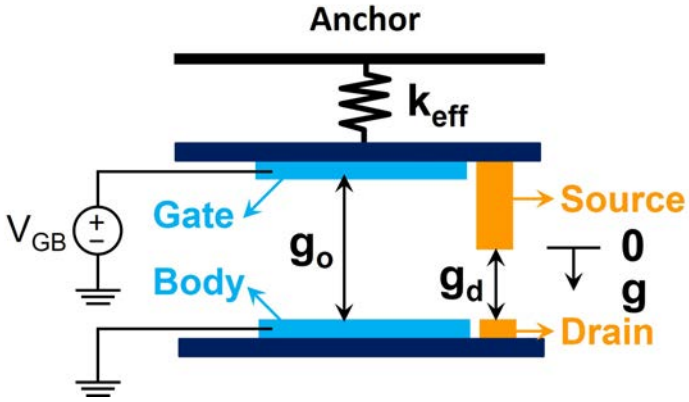


Figure 1.6: A simplified parallel capacitor model of a MEM relay.

When the top plate moves downwards by a distance g toward the bottom fixed plate, the spring restoring force F_{spring} can be written as:

$$F_{spring} = -k_{eff} \times g \tag{1.2}$$

The minus sign in Equation 1.2 indicates the spring restoring force is upward, as shown also in Figure 1.4 (b). The range of g is between 0 (when the top plate is in its as-fabricated position) and g_d (when the source and drain electrodes make contact with each other). With V_{GB} applied, the electrostatic force that actuates the top plate moving towards the bottom plate can be modeled based on the properties of parallel plate capacitors as:

$$F_{elec} = \frac{1}{2}\frac{\epsilon_0 A_{ACT} V_{GB}^2}{(g_o - g)^2} \tag{1.3}$$

where ϵ_0 is the vacuum permittivity, A_{ACT} is the effective actuation area (the overlap area of the parallel plates), and V_{GB} is the potential difference between the gate and body electrodes. The direction of this electrostatic force F_{elec} is downward, as indicated in Figure 1.4 (b). Therefore, the net force F_{total} (positive direction is downward) can be written as:

$$\begin{aligned} F_{total} &= F_{spring} + F_{elec} \\ &= -k_{eff} \times g + \frac{1}{2}\frac{\epsilon_0 A_{ACT} V_{GB}^2}{(g_o - g)^2} \end{aligned} \tag{1.4}$$

The derivative of F_{total} over g can be written as:

$$\frac{dF_{total}}{dg} = -k_{eff} + \frac{\epsilon_0 A_{ACT} V_{GB}^2}{(g_o - g)^3} \tag{1.5}$$

When the suspended top plate moves down, g becomes larger. From Equations 1.2 and 1.3, the upward F_{spring} is proportional to g, and the downward F_{elec} is inversely proportional to the square of $(g_o - g)$. Therefore, when $(g_o - g)$ gets small, it is possible that both F_{total} and $\frac{dF_{total}}{dg}$ are larger than 0, resulting in non-linear positive feedback. This phenomenon is called the pull-in (PI) effect [40]. By setting both F_{total} and $\frac{dF_{total}}{dg}$ to 0:

$$\begin{cases} 0 = -k_{eff} \times g + \dfrac{1}{2}\dfrac{\epsilon_0 A_{ACT} V_{GB}^2}{(g_o - g)^2} \\ \\ 0 = -k_{eff} + \dfrac{\epsilon_0 A_{ACT} V_{GB}^2}{(g_o - g)^3} \end{cases} \tag{1.6}$$

we can obtain the pull-in voltage V_{PI} and the corresponding displacement of the top plate g at pull-in:

$$\begin{cases} V_{PI} = \sqrt{\dfrac{8 k_{eff} g_o^3}{27 \epsilon_0 A_{ACT}}} \\ \\ g = \dfrac{g_o}{3} \end{cases} \tag{1.7}$$

From Equation 1.7, if g is less than 1/3 of g_o, the MEM relay turns ON before it enters the PI region of operation. That is to say, g_d should be designed to be less than 1/3 of g_o, since g_d is the maximum value that g can take. In this case, the relay is considered to operate in non-pull-in (NPI) mode. The turn-ON voltage V_{ON} can therefore be calculated by setting Equation 1.4 to be 0 and $g = g_d$:

$$\begin{cases} 0 = -k_{eff} \times g + \dfrac{1}{2}\dfrac{\epsilon_0 A_{ACT} V_{ON}^2}{(g_o - g)^2} \\ \\ g = g_d \end{cases} \tag{1.8}$$

and the solution to Equation 1.8 is:

$$V_{ON} = \sqrt{\frac{2 k_{eff} g_d (g_o - g_d)^2}{\epsilon_0 A_{ACT}}} \tag{1.9}$$

As noted in Figure 1.4 (b), when the relay is ON, there is an additional adhesive force F_{adh} between the two contacting electrodes primarily due to van der Waals forces [61]. The total force becomes:

$$\begin{aligned} F_{total\_ON} &= F_{spring} + F_{elec} + F_{adh} \\ &= -k_{eff} \times g_d + \frac{1}{2}\frac{\epsilon_0 A_{ACT} V_{GB}^2}{(g_o - g_d)^2} + F_{adh} \end{aligned} \tag{1.10}$$

Therefore, in order to turn OFF the relay, the magnitude of the spring restoring force must be at least the sum of F_{elec} and F_{adh}:

$$\begin{aligned} k_{eff}g &= F_{elec} + F_{adh} \\ &= \frac{1}{2}\frac{\epsilon_0 A_{ACT} V_{OFF}^2}{(g_o - g_d)^2} + F_{adh} \end{aligned} \tag{1.11}$$

By solving Equation 1.11, we can obtain the turn-OFF voltage V_{OFF}:

$$V_{OFF} = \sqrt{\frac{2(k_{eff}g_d - F_{adh})(g_o - g_d)^2}{\epsilon_0 A_{ACT}}} \tag{1.12}$$

The hysteresis voltage V_H is the minimum switching voltage needed for relay-based digital integrated circuits, and it is defined by the difference between V_{ON} and V_{OFF}. V_H can be written and simplified as:

$$\begin{aligned} V_H &= V_{ON} - V_{OFF} \\ &= \sqrt{\frac{2k_{eff}g_d(g_o - g_d)^2}{\epsilon_0 A_{ACT}}} - \sqrt{\frac{2(k_{eff}g_d - F_{adh})(g_o - g_d)^2}{\epsilon_0 A_{ACT}}} \\ &= \sqrt{\frac{2(g_o - g_d)^2}{\epsilon_0 A_{ACT}}} \times (\sqrt{k_{eff}g_d} - \sqrt{k_{eff}g_d - F_{adh}}) \\ &= \sqrt{\frac{2(g_o - g_d)^2}{\epsilon_0 A_{ACT}}} \times (\frac{F_{adh}}{\sqrt{k_{eff}g_d} + \sqrt{k_{eff}g_d - F_{adh}}}) \\ &\approx F_{adh}\sqrt{\frac{(g_o - g_d)^2}{2\epsilon_0 A_{ACT}k_{eff}g_d}} \qquad \big) \text{ if } k_{eff}g_d \gg F_{adh} \\ &\geq F_{adh}\sqrt{\frac{2g_d}{\epsilon_0 A_{ACT}k_{eff}}} \qquad \big) \text{ if } g_d \leq \tfrac{g_o}{3} \end{aligned} \tag{1.13}$$

From Equation 1.13, it can be seen that if g_o is smaller, V_H can be smaller. But g_o has to be at least $3g_d$ for the relay to operate in NPI mode; otherwise the device is prone to failure to turn OFF [40]. It is also worth noting that the equality in Equation 1.13 holds when

$g_d = \frac{g_o}{3}$. Therefore, the ideal design is to make the relay operate at the boundary of PI mode and NPI mode. Moreover, decreasing F_{adh} is a crucial research topic to lower the operating voltage and thereby improve the energy efficiency of MEM relays. Methods investigated to date include self-assembled molecular coating [62–64], ion beam induced oxide formation [65], contact dimple size reduction [61], and lower temperature operation [66].

1.4 Dissertation Overview

In order to address the challenges of data-centric computation and the limitations of present computing systems, it is necessary to explore alternatives to the conventional von Neumann computer architecture [10].

This dissertation aims to explore micro-electro-mechanical switch technology for novel applications that facilitate implementation of non-von-Neumann computing. Operation of relays with voltage signals as small as 10 mV at cryogenic temperatures is demonstrated, for quantum computing application, and superconducting materials are considered for MEM relay contact electrodes. The use of relays as DC-voltage-driven oscillators for implementation of Ising machines is also explored.

Chapter 2 presents the ultra-low voltage operation of MEM relays at cryogenic temperatures. First, an overview of quantum computing requirements and MEM relay benefits is presented. Then the MEM relay fabrication process flow is presented, followed by a study of the temperature dependence of relay properties. Millivolt operation of relay-based integrated circuits is demonstrated at 77 K and 4 K. The results indicate that MEM relays are intriguing candidates for monolithic integration of digital control circuitry with qubits, due to their suitability for ultra-low-power and cryogenic operation.

Chapter 3 describes the requirements for relay contacting electrode material, and investigates the possibility of using a superconducting material (niobium) to further reduce relay ON-state resistance at cryogenic temperatures. A detailed integrated process flow for fabricating Nb-contact relays is presented, followed by electrical characterizations and comparisons with W-contact relays.

Chapter 4 investigates the novel application of MEM relays as DC-driven non-linear oscillators to implement Ising machines for solving combinatorial optimization problems. The effects of applied voltages on the frequency and amplitude of MEM relay oscillators are studied. Furthermore, sub-harmonic injection locking and coupling of MEM relays are demonstrated experimentally, representing a significant milestone toward networked arrays of MEM relay oscillators for building Ising machines.

Chapter 5 outlines the major results and contributions of this dissertation. Additionally, suggestions for future work are provided.

Chapter 2

Ultra-Low-Voltage Operation of MEM Relays for Cryogenic Logic Applications

2.1 Quantum Computing Benefits and Requirements

Quantum computing has gained much attention recently, because it has the potential to solve computational problems that are intractable for traditional computing paradigms [38, 67]. Promising applications for quantum computing include: machine learning [17, 18, 68, 69], database searching [70, 71], financial modeling [72–76], and cryptography [77–79].

A quantum computer comprises a quantum processor and a classical electronic controller [39]. The quantum processor consists of a set of quantum bits (qubits) operating at a few tens of milli-Kelvin (mK), while the classical electronic controller that is used to read out and control the quantum processor is operated at room temperature [80], as illustrated in Figure 2.1. This approach becomes increasingly challenging and less cost-effective as the number of qubits (hence the number of interconnections between the processor and controller) grows.

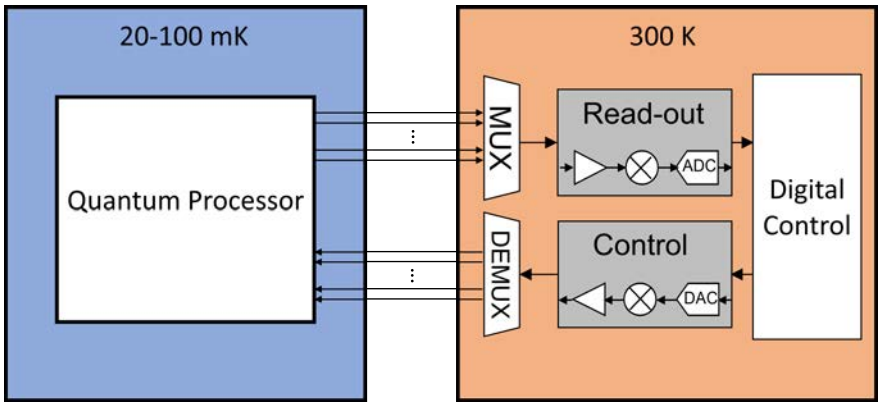


Figure 2.1: Quantum processor with classical controller.

To allow for a reduction in the number of interconnections between the cryogenic chamber and the room-temperature electronics, operation of digital logic circuitry at cryogenic temperatures is of growing interest [81]. As shown in Figure 2.2, ideally the electronic control circuitry should be monolithically integrated with the qubits, at least for the multiplexer (MUX) and demultiplexer (DEMUX). These circuits should dissipate as little energy as possible in order to maintain the computer at mK temperatures [82, 83]. Otherwise qubit operation can be detrimentally impacted [84].

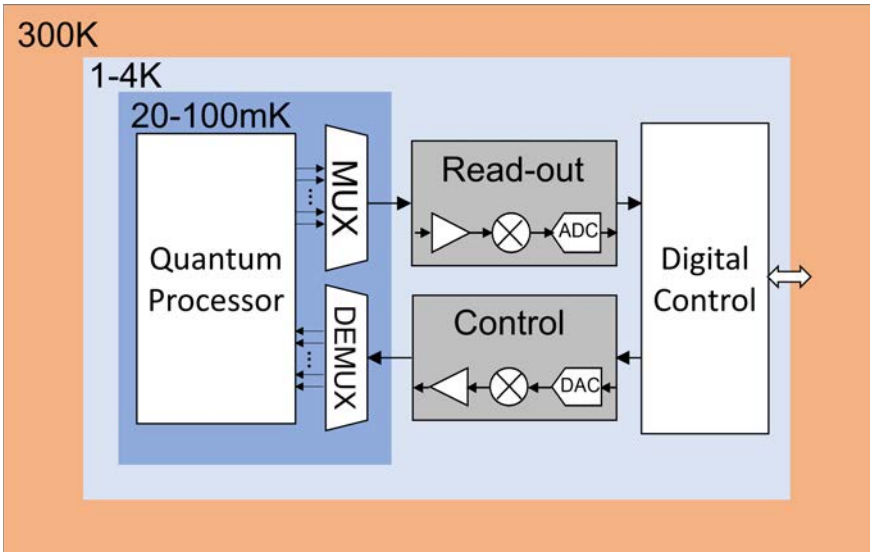


Figure 2.2: Monolithic integration of quantum processor with electronic control circuitry.

Therefore, improvements in energy efficiency of CMOS-based digital integrated circuits are needed for quantum computing; these generally require reductions in the circuit operating voltage, V_{DD}. In principle, MOSFETs can operate at cryogenic temperatures with very small subthreshold swing (SS). However, due to temperature-dependent oxide-interface trap density, SS for conventional bulk-silicon MOSFETs operated at 4 K is at least 10 mV/dec, which is well above the lower limit set by Boltzmann statistics [85,86]. Therefore, the supply voltage required to operate CMOS digital circuits at cryogenic temperatures is still more than 0.25 V.

Micrometer-scale electro-mechanical (MEM) relays have been experimentally demonstrated to operate with zero off-state leakage current (I_{OFF}) and ultra-low switching voltage signals, enabling the demonstration of sub-50 mV digital integrated circuits at room temperature [63, 64, 87]. In this chapter, the operation of MEM relays and relay-based integrated circuits at temperatures down to 4 K is experimentally investigated for the first time [66].

2.2 Relay Structure and Fabrication Process

Figure 2.3 is a 30° tilted scanning electron micrograph (SEM) image of a fabricated MEM relay, which comprises a movable gate electrode suspended by four folded-flexure beams over a fixed body electrode, and two pairs of source/drain electrodes.

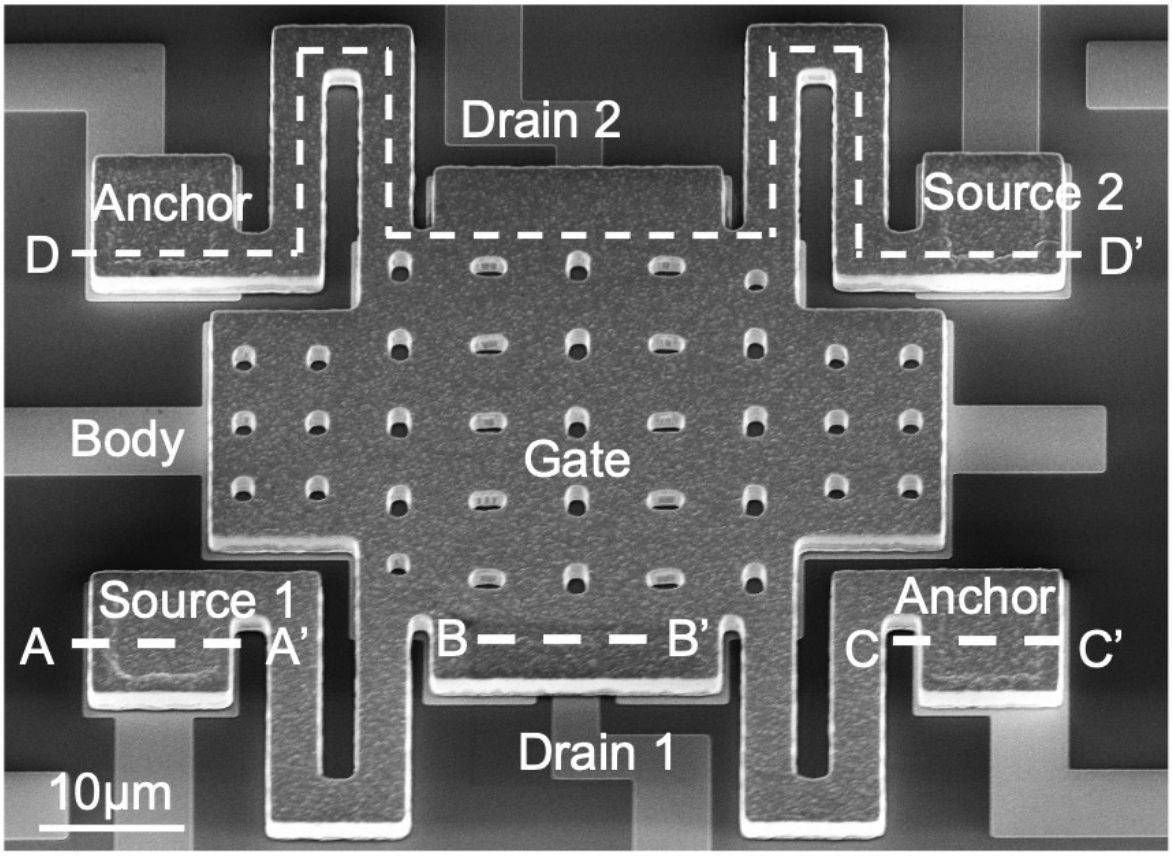


Figure 2.3: 30° tilted SEM image of a MEM logic relay.

The schematic cross-sectional views in Figure 2.4 show the as-fabricated air gap between the two metal conductive (source and drain) electrodes, g_d, as well as the as-fabricated actuation gap, g_o. When a voltage difference is applied between the gate and body, the electrostatic force due to the applied voltage (V_{GB}) will actuate the movable gate towards the body. This force is opposed by the spring restoring force of the folded flexure beams. The air gap g_o is designed to be larger than three times g_d so that the relay operates in non-pull-in mode [40]. When the structure is actuated sufficiently to cause the source electrode to come into physical contact with the underlying drain electrode, current (I_{DS}) can flow between the source and drain under the influence of an applied voltage between drain and source (V_{DS}); this is defined as the ON-state. The minimum value of V_{GB} that causes the relay to turn ON is referred to herein as the turn-ON voltage, V_{ON}. In the ON-state, adhesive force exists between the source and drain electrodes. Therefore, to turn OFF the relay, the spring restoring force needs to exceed the sum of the adhesive force and the electrostatic force due to V_{GB}. The value of V_{GB} that is just small enough to cause the relay to turn OFF is referred to herein as the release voltage, V_{RL}. The difference between V_{ON} and V_{RL} is referred to as

the hysteresis voltage, V_H. By applying a DC bias (V_B) to the body electrode such that $V_B = -V_{RL}$, the relay can be switched ON and OFF by swinging the gate voltage (V_G) between 0 V and V_H. Therefore, decreasing V_H enables lower-voltage relay operation.

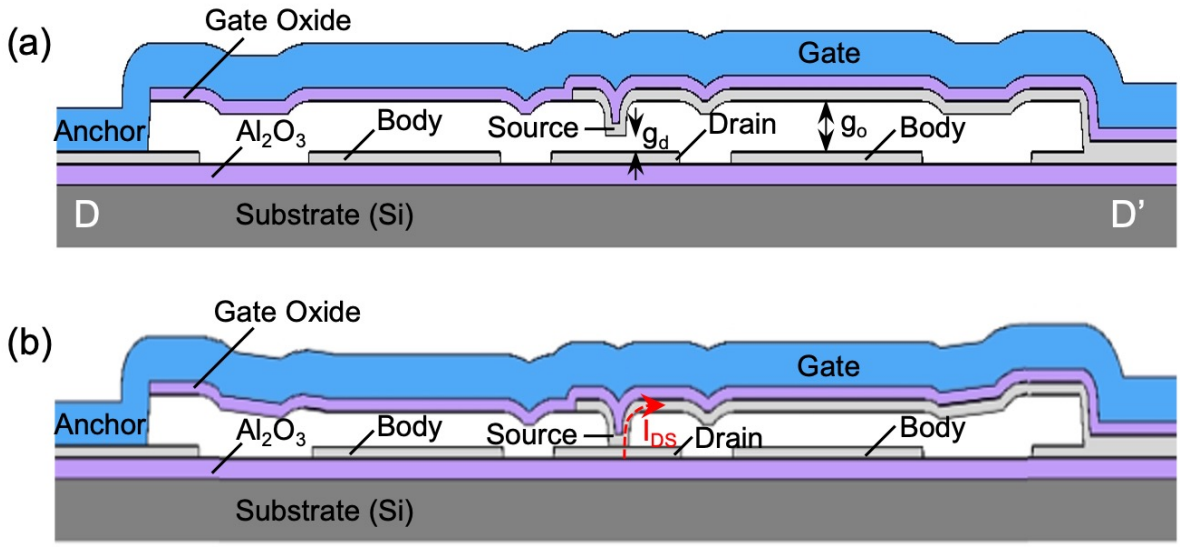


Figure 2.4: Schematic cross-sectional views along D-D' of Figure 2.3: (a) OFF-state (b) ON-state.

Conventional planar processing techniques are used to fabricate MEM relays, with a maximum substrate temperature below 450 °C for compatibility with post-CMOS (and post-qubit) integration. Figure 2.5 illustrates the key steps in the MEM relay fabrication process, with isometric and cross-sectional views along the A-A', B-B', and C-C' cutlines defined in Figure 2.3. The starting substrate is a silicon wafer, and alignment marks are patterned on the wafer to allow subsequent deposited layers of material to be patterned in alignment with each other.

First an 80 nm-thick electrically insulating Al_2O_3 layer is deposited by atomic layer deposition using a Picosun ALD system (Figure 2.5(a)). The precursor gases used are trimethylaluminum (TMA) and water vapor (H_2O). The substrate temperature is set to be 300 °C. The flow of TMA from source A is set to be 150 sccm, and the H_2O flow from source C is 200 sccm. The number of deposition cycles is approximately 900, which usually takes around 2 hours. An ellipsometer (Gaetner Stokes Ellipsometer) is used to check the thickness of the deposited Al_2O_3 film.

Then a 60 nm-thick tungsten (W) layer is deposited by pulsed-DC sputtering using the MRC944 (MRC Sputtering System with Sputter-Etch), as shown in Figure 2.5(b). The DC source power is set to be 1 kW and the sputtering pressure is 8 mTorr; 6 sputtering cycles are required. The sheet resistance should be approximately $3.5\,\Omega/\square$.

Lithography and reactive ion etching (RIE) processes are performed to pattern the W layer to form fixed electrodes, including body electrodes, drain electrodes, and source electrodes, shown in Figure 2.5(c). Hexamethyldisilazane (HMDS) pre-treatment should not be used when coating the 0.43 μm UV210 photoresist, and a hard bake step should not be used after the photoresist is developed; otherwise, it will be hard to remove the photoresist from the underlying W. An ASML DUV Stepper Model 5500/300 (ASML300) is used to expose the photoresist through a mask, with an energy dosage of 22 mJ/cm^2. After the photoresist is developed, a SF_6 plasma in a Lam Metal TCP Etcher (Lam7) is used to remove the W in regions not protected by photoresist. The flow of SF_6 is 50 sccm, the upper electrode power (TCP RF) is set to be 300 W, and the lower electrode power (bias RF) is 80 W; the etching time is around 15 seconds. The photoresist is then removed by soaking in MICROPOSIT Remover 1165 at 80 °C in Msink1 (Pre-Furnace Metal Clean Sink) for at least 30 minutes, followed by ashing in oxygen plasma at 250 °C for 1 minute in Matrix (Matrix 106 Resist Removal System). The wafer needs to be cleaned in a SVC-14 bath, also in Msink1, at 80 °C for 10 minutes before entering a furnace.

Subsequently a 160 nm-thick low-temperature deposited silicon dioxide (LTO) layer is deposited as a first sacrificial layer by low pressure chemical vapor deposition (LPCVD) at 400 °C with 135 sccm O_2 flow rate and 90 sccm SiH_4 flow rate for about 16.5 minutes, in the Tystar12 (Tystar12 Non-MOS Clean LTO LPCVD) furnace (Figure 2.5(d)). An ellipsometer is used to check the thickness of this LTO1 layer, which can be slightly greater than 160 nm.

The contact dimples are then defined by lithography and RIE processes to remove the LTO in regions over the drain electrodes (Figure 2.5(e)). HMDS pre-treatment should be used when coating the 0.43 μm UV210 photoresist, to promote adhesion to LTO. The ASML300 is then used to expose the photoresist with an energy dosage of 20 mJ/cm^2. After the photoresist is developed, the Technics-c (Technics C Plasma Etching System) is used to descum the photoresist in the small dimple regions at 50 W power for 30 seconds. Then UV bake is performed in the Axcelis (Axcelis Fusion M200PCU Photostabilizer System) using recipe U. Afterwards the Lam6 (Lam6 Oxide Rainbow Etcher) is used to etch the LTO1 film using 150 sccm Ar, 25 sccm CHF_3, and 25 sccm CF4 with the TCP RF power set at 750 W for an etch rate of approximately 700 nm/min. Afterwards the wafer is soaked in MICROPOSIT Remover 1165 at 80 °C in Msink1 for 30 minutes, and processed in the Matrix for 2.5 minutes to remove any remaining photoresist. Similarly as before, a pre-furnace metal cleaning process in a SVC-14 bath at 80 °C for 10 minutes is necessary before the wafer enters a furnace.

Next, a second sacrificial layer of 60 nm-thick LTO (called LTO2) is deposited using the same LPCVD recipe in Tystar12 for about 4.5 minutes, as shown in Figure 2.5(f). Note that the thickness of the second LTO layer corresponds to g_d, while the sum of the thicknesses of the two LTO layers corresponds to g_o.

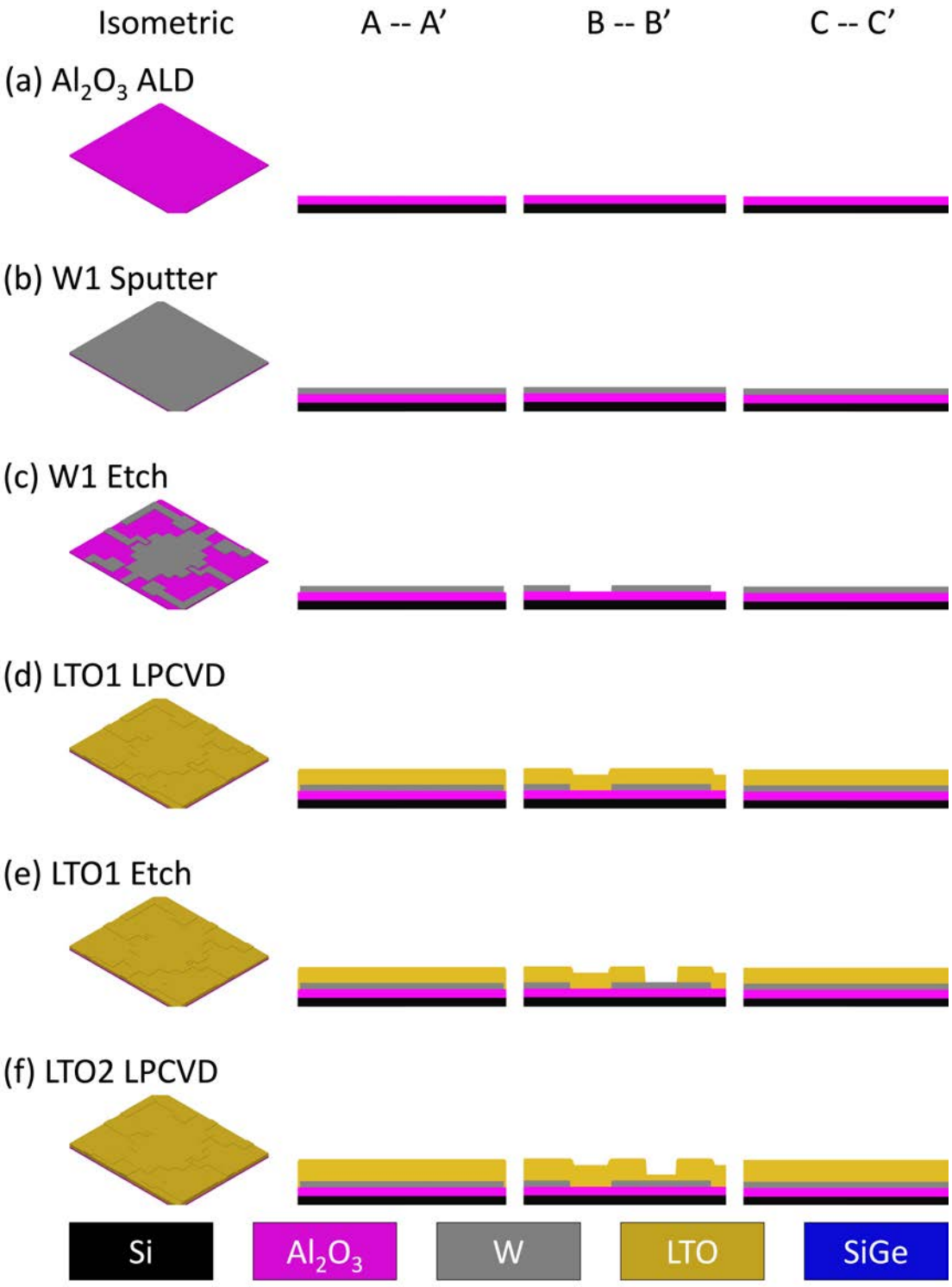


Figure 2.5: Fabrication process of tungsten-contact MEM relays, showing isometric views on the left and cross-sectional views along A-A', B-B', and C-C' cutlines on the right.

As shown in Figure 2.5(g), lithography and RIE processes are then applied to remove the LTO in regions over the fixed source electrodes. The coated photoresist is 0.87 μm-thick UV210, exposed in AMSL300 with an energy dosage of 18 mJ/cm^2. After the photoresist is developed, the same descum and UV bake steps are performed prior to etching in Lam6 for about 22 seconds to remove the LTO1 and LTO2 layers in the source anchor regions. Then the same photoresist removal and cleaning processes as before are used.

Next, a second layer of 60 nm-thick tungsten is deposited in the MRC944 using the same recipe as before (Figure 2.5(h)). This layer is patterned to form dimpled source electrodes, each extending over its corresponding drain electrode and anchored to its fixed source electrode (formed in the first W layer), as shown in Figure 2.5(i). The lithography, etching, and cleaning processes for this second W layer are the same as for the first W layer.

Next, a 55 nm-thick insulating layer of Al_2O_3 is deposited by ALD using the Picosun, with approximately 550 deposition cycles (Figure 2.5(j)). Lithography and RIE processes are then used to remove this second layer of Al_2O_3 and the LTO in regions over the fixed body electrodes. The UV210 photoresist is coated to be 0.87 μm thick and is exposed with a dosage of 18 mJ/cm^2, followed by developing and UV bake. A gas mixture of 30 sccm Cl_2 and 60 sccm BCl_3 with TCP RF power = 700 W and bias RF power = 80 W was used to etch the Al_2O_3 in the Lam7 etcher for about 75 seconds (Figure 2.5(k)). Then a gas mixture of 150 sccm Ar, 25 sccm CHF_3, and 25 sccm CF_4 was used to etch LTO in the Lam6 etcher for about 28 seconds (Figure 2.5(l)). Afterwards the wafer is soaked in 1165 photoresist remover for 30 minutes, followed by a standard Matrix photoresist ashing process for 2.5 minutes, and then soaked in the SVC-14 bath for 10 minutes for pre-furnace cleaning.

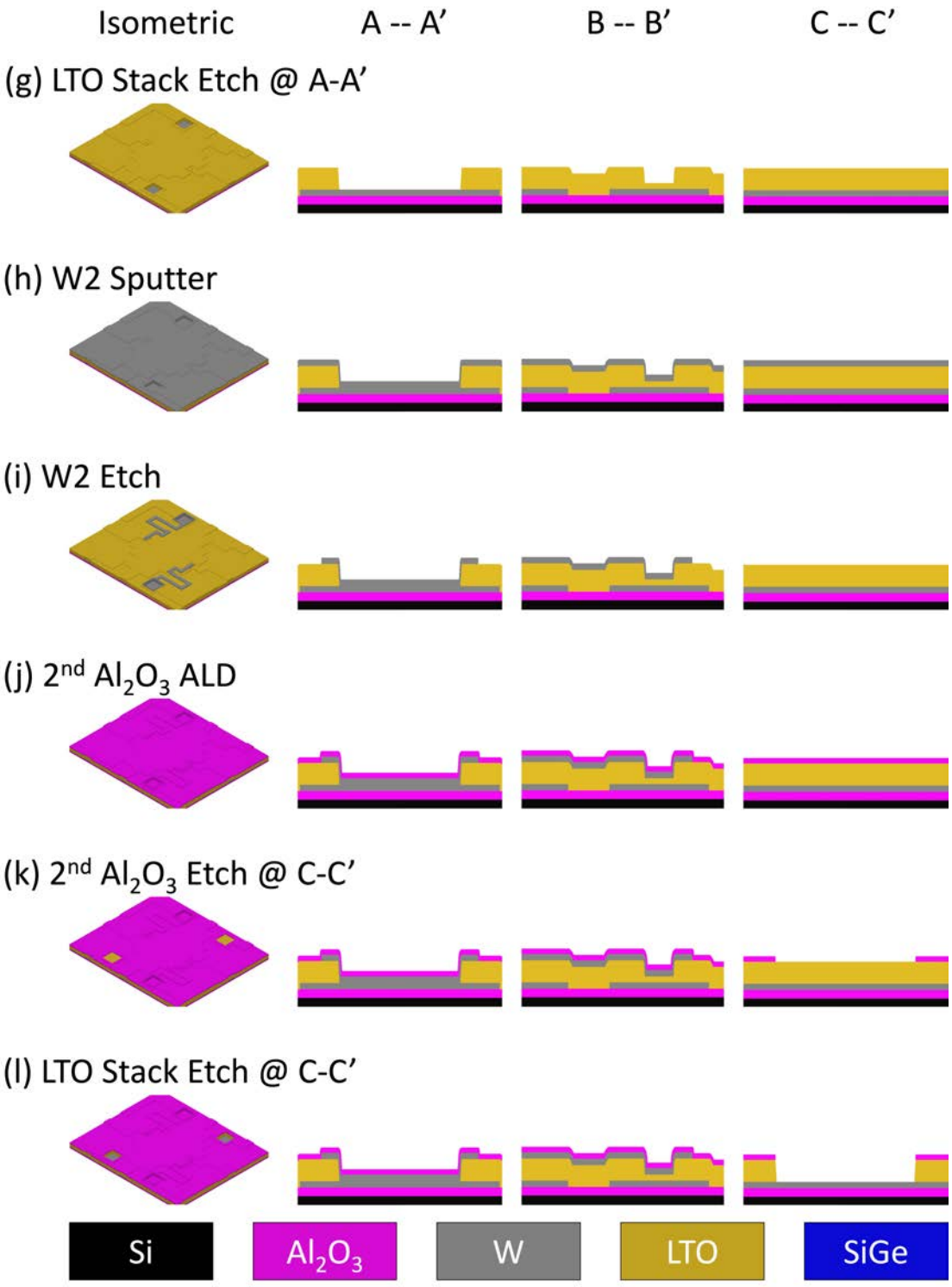


Figure 2.5: Fabrication process of tungsten-contact MEM relays, showing isometric views on the left and cross-sectional views along A-A', B-B', and C-C' cutlines on the right *(cont.)*

Next a structural layer consisting of 1.9 μm-thick p-type heavily in-situ doped polycrystalline-$Si_{0.4}Ge_{0.6}$ (poly-SiGe) is deposited via LPCVD at 410 °C for approximately 4 hours in the Tystar20 (Tystar20 Non-MOS Clean Si-Ge LPCVD), as shown in Figure 2.5(m). The deposition process comprises a nucleation layer deposition step (5 minutes, 100 sccm Si_2H_6, 300 mTorr) followed by the poly-SiGe deposition step using 140 sccm SiH_4, 60 sccm GeH_4, and 45 sccm dopant gas (1% BCl_3 and 99% He) at 600 mTorr. These deposition conditions provide for the lowest stain gradient poly-SiGe film [88].

Lastly a 400 nm-thick LTO hard-mask layer is deposited to facilitate patterning of the thick structural layer (Figure 2.5(n)); it is deposited by LPCVD at 400 °C using the same recipe as for the LTO1 and LTO2 layers. The hard mask is patterned by coating 0.87 μm photoresist, exposing it with an energy dosage of 18 mJ/cm^2 followed by developing, descum, UV bake, and etching in Lam6 for 30 seconds + 35 seconds (to avoid photoresist burning during one long etch in Lam6), as shown in Figure 2.5(o). The poly-SiGe layer is subsequently etched in Lam8 (Lam8 Poly-Si TCP Etcher) for about 310 seconds with 50 sccm Cl_2 and 150 sccm HBr at 12 mTorr chamber pressure, 300 W TCP RF power, and 150 W bias RF power, as shown in Figure 2.5(p). (The poly-SiGe etch rate is approximately 0.4 μm/min.) The Al_2O_3 layer is then etched away in the resulting exposed regions, using Lam7 with 30 sccm Cl_2 and 60 sccm BCl_3 at 700 W TCP RF and 80 W Bias RF, for about 60 seconds; this exposes the second LTO layer (Figure 2.5(q)).

Finally, vapor hydrofluoric acid (HF) is used to selectively remove the sacrificial LTO layers while avoiding capillary-force-induced stiction, as shown in Figure 2.5(r). 350 sccm of ethanol is used to desorb the H_2O reaction product from the surface of the wafer, and 310 sccm of HF at 45 °C is used to remove the LTO at an etch rate of about 36 nm/min. Inert gas (1250 sccm of N_2) is used to dampen the effects of changes in vapor pressures of the active gases, and to prevent ethanol saturation/condensation in the vaporizer.

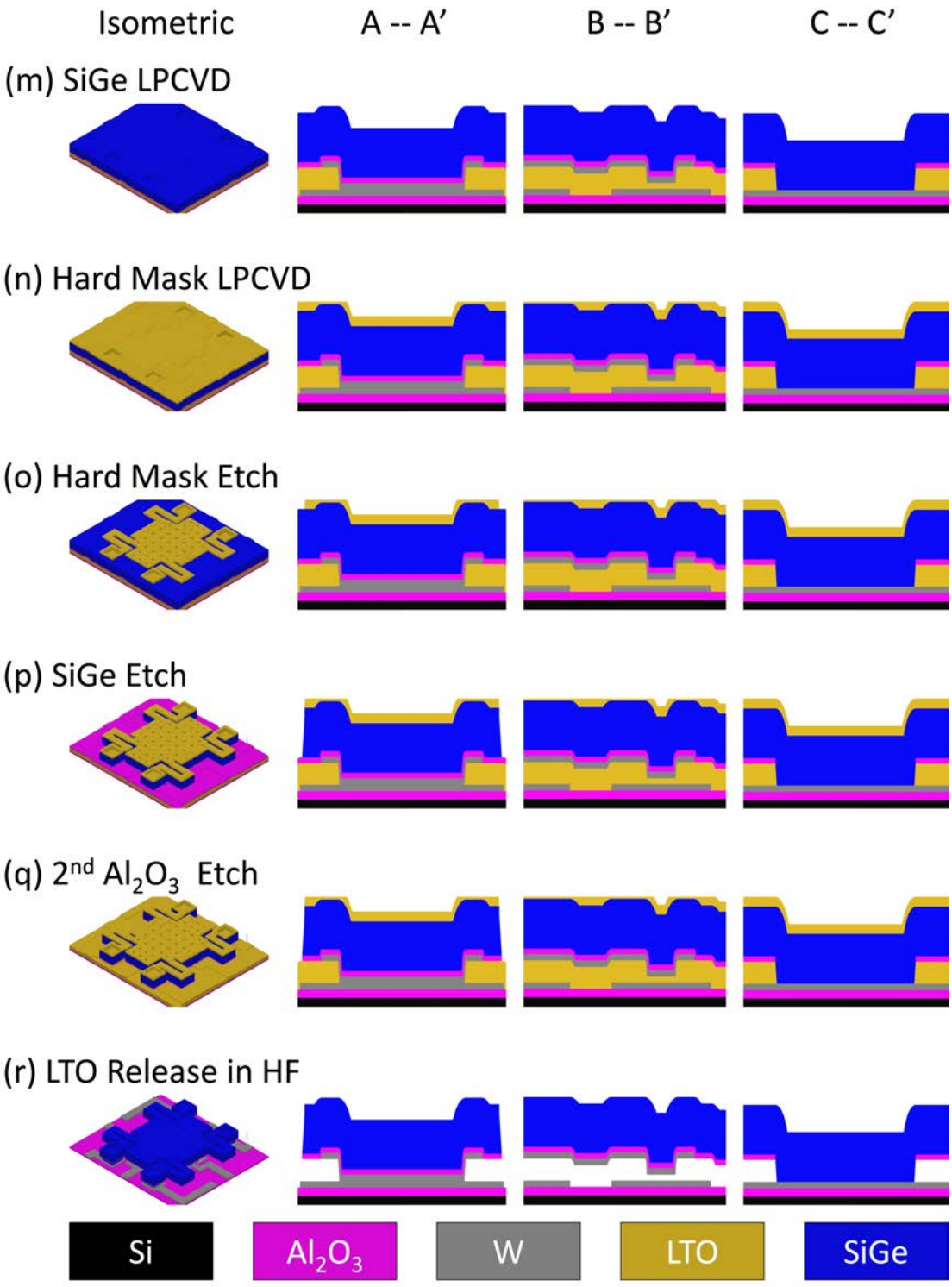


Figure 2.5: Fabrication process of tungsten-contact MEM relays, showing isometric views on the left and cross-sectional views along A-A', B-B', and C-C' cutlines on the right *(cont.)*

2.3 Complementary Relay Operation with Body Biasing

Complementary relay operation is achieved simply by applying body biases of different polarity [64], as shown in Figure 2.6. With a negative body bias, the electrostatic field increases with increasing gate voltage, so that the relay turns ON with increasing gate voltage; this switching behavior is similar to that of an n-channel MOSFET (NMOS transistor), so a relay with negative body bias is referred to heretofore as an N-relay. With a positive body bias, the electrostatic field decreases with increasing gate voltage, so that the relay turns OFF with increasing gate voltage; this switching behavior is similar to that of a p-channel MOSFET (PMOS transistor); so a relay with positive body bias is referred to heretofore as a P-relay.

The N-Relay and P-Relay circuit symbols used herein are similar to those for NMOS and PMOS transistors, respectively. Note that for a P-relay, if V_G is zero, the device is in the ON-state. Ideally, in a complementary relay circuit, the body bias voltages should be adjusted such that the N-relays and P-relays are never both ON for the same applied gate voltage, as shown in Figure 2.6.

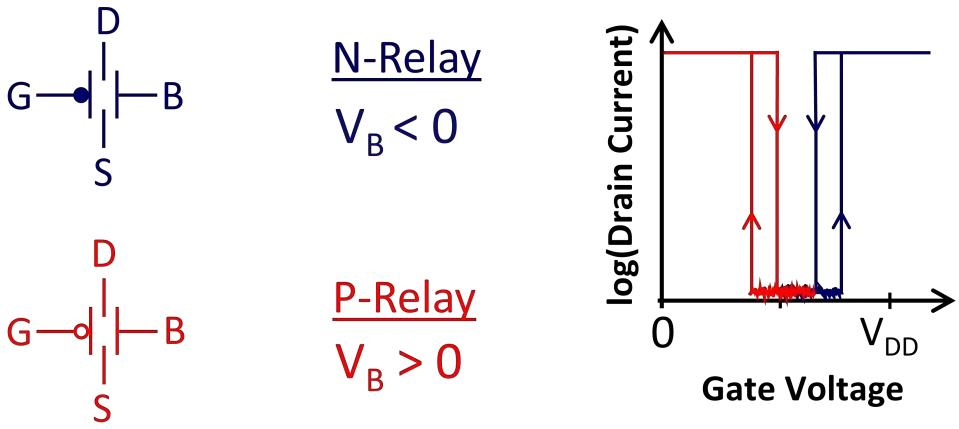


Figure 2.6: Complementary relay circuit symbols and I-V characteristics.

2.4 Temperature Dependence of Relay Properties

Changes in the electrical conductivity of the relay electrode materials are gauged by sheet resistance measurements of the contacting electrode layer (60 nm-thick W) and the structural gate electrode layer (1.9 μm-thick p-type poly-SiGe), as shown in Figure 2.7. The poly-SiGe

does not show dopant freeze-out effects down to 1.8 K, and the resistance of W also remains low, indicating that MEM relays can operate at temperatures as low as 1.8 K. Note that the sheet resistance of the poly-SiGe layer is lower than that of the W layer; this is because the poly-SiGe layer is much thicker than the W layer.

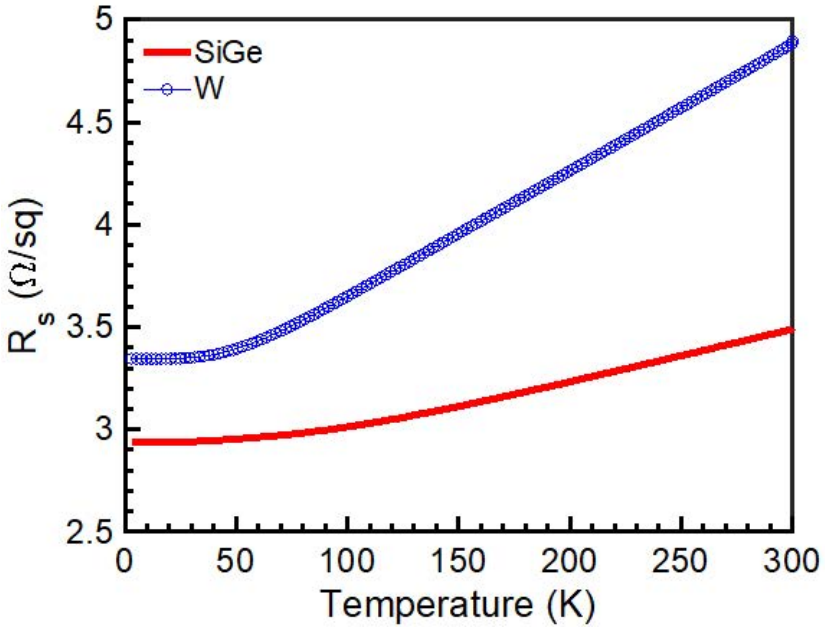


Figure 2.7: Temperature dependence of sheet resistance for the W electrode layer and poly-SiGe structural layer.

As can be seen from Figure 2.8, the relay turn-on voltage (V_{ON}) is stable over a wide range of temperatures. From the zoomed-in figure on the right, it can be seen that V_{ON} decreases slightly with decreasing temperature. This can be explained by an increase in structural stiffness, that is, an increase in the Young's modulus of the poly-SiGe film with decreasing temperature.

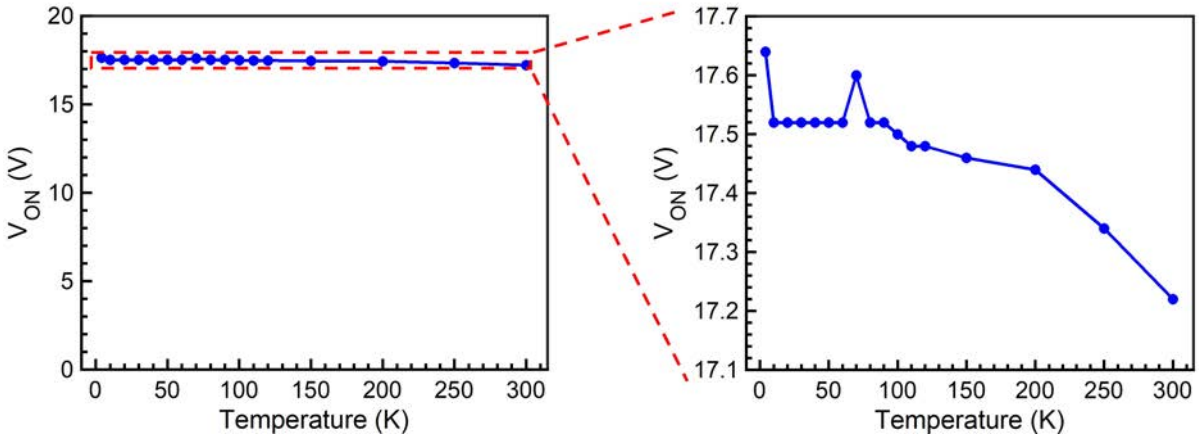


Figure 2.8: Temperature dependence of relay turn-ON voltage.

The relay self-oscillation frequency is used to gauge this change in Young's modulus with decreasing temperature. A DC voltage that is slightly less than V_{ON} is applied between the gate and body electrodes, while an applied V_{DS} is used to induce additional electrostatic force (in the contact dimple region) to turn on the relay (Figure 2.9). When the drain and source electrodes come into contact, the voltage difference between them decreases so the total electrostatic force decreases, causing the relay to turn off. When the source and drain electrodes are separated the voltage difference returns to the applied V_{DS}, causing the relay to turn on, and so on. Thus the relay can be made to oscillate with only DC voltages applied.

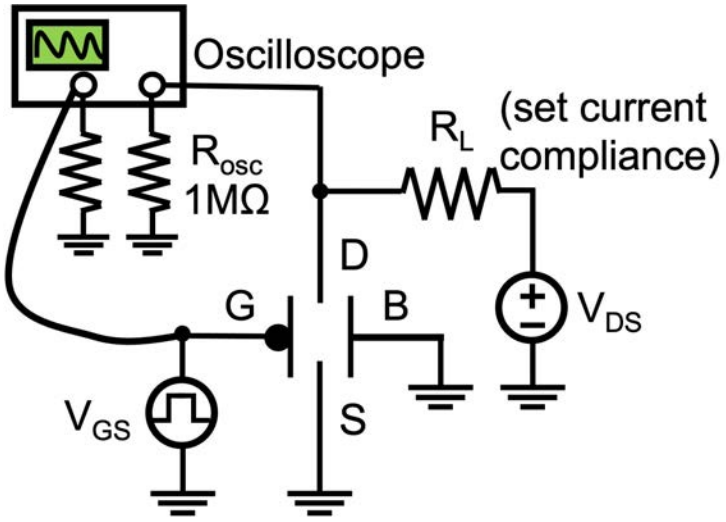


Figure 2.9: Circuit schematic for relay self-oscillation test setup.

The self-oscillation frequency (ω_0) of the MEM relay structure is measured at 300 K, 77 K, and 4 K respectively, as shown in Figure 2.10. Since $\omega_0 \propto \sqrt{k} \propto \sqrt{E}$ (where k is the composite stiffness of the folded-flexure suspension beams and E is the Young's modulus), it can be qualitatively deduced that a decrease in temperature increases the Young's modulus of the structural material.

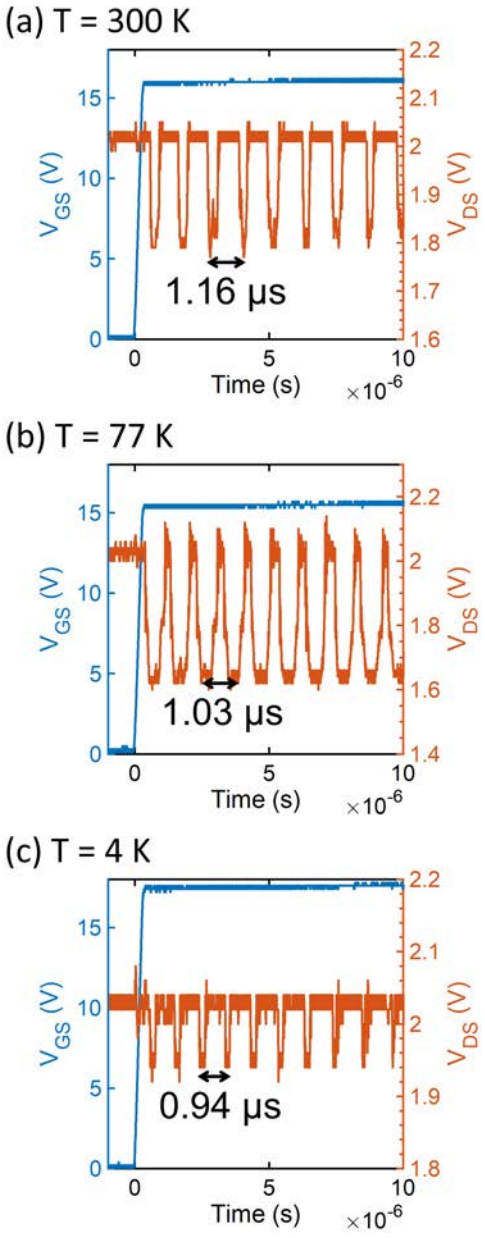


Figure 2.10: Relay self-oscillation measurements taken at different temperatures: (a) 300 K, (b) 77 K, and (c) 4 K.

The temperature dependence of the hysteresis voltage for a MEM relay is shown in Figure 2.11. It can be seen that V_H decreases dramatically with decreasing temperature, indicating that the contact adhesive force diminishes with decreasing temperature [89].

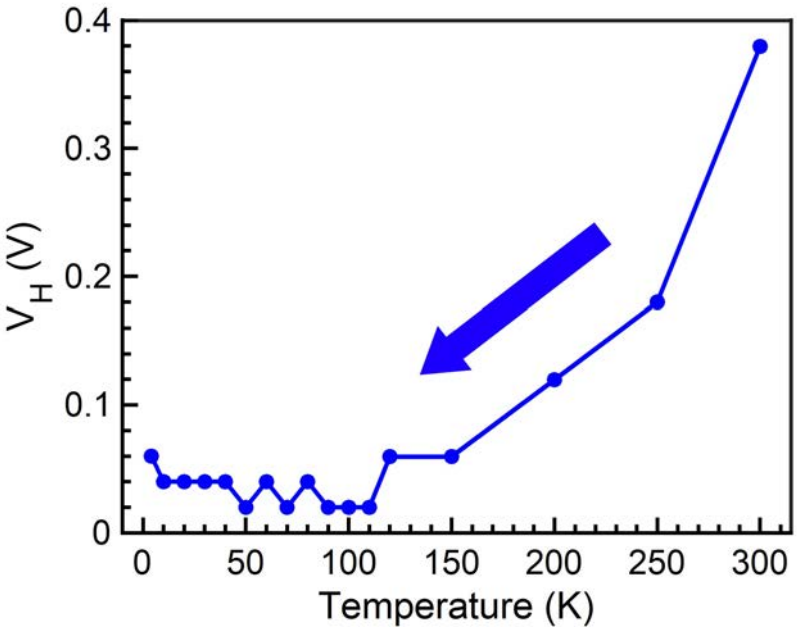


Figure 2.11: Temperature dependence of relay switching hysteresis voltage.

The average turn-ON voltage (V_{ON}) and hysteresis voltage (V_H) values across 5 MEM relays are compared for room temperature vs. cryogenic temperature operation, in Figure 2.12. The average V_{ON} at 4 K (16.43 V) is similar to that at 300 K (16.23 V). A much more significant change with temperature is seen for average V_H, dropping from 120 mV at 300 K to 30 mV at 4 K.

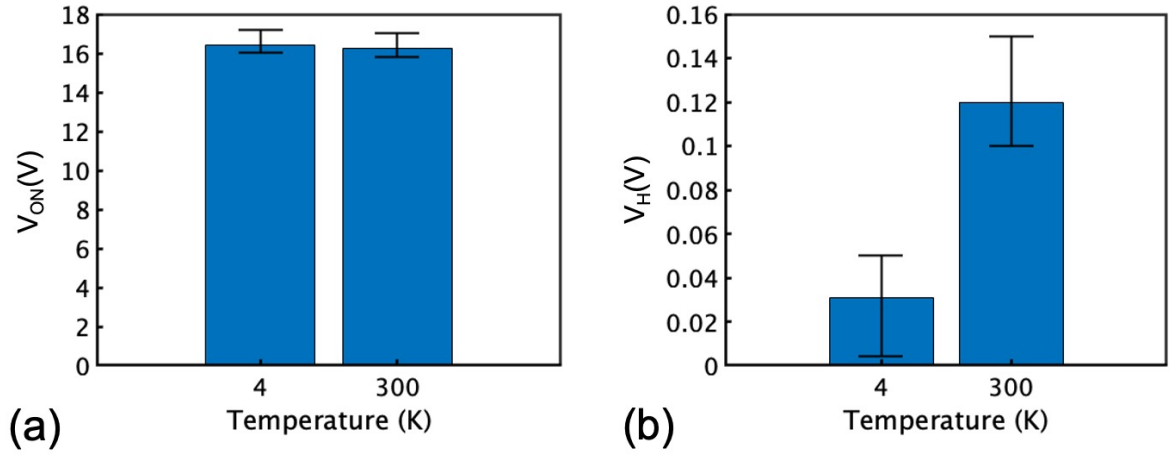


Figure 2.12: Measured values for 5 MEM relays: (a) Average V_{ON} at 4 K and 300 K, (b) Average V_H at 4 K and 300 K.

Measured relay I_{DS}-vs.-V_G characteristics are shown in Figure 2.13. As expected, the relay switches on and off abruptly as the gate voltage is swept up and down, respectively; an applied body bias voltage (V_B) allows for low gate voltage operation. The smaller hysteresis voltage at 4 K allows MEM relay circuits to be operated with sub-10 mV voltage signals – which are roughly two orders of magnitude smaller than for MOSFETs.

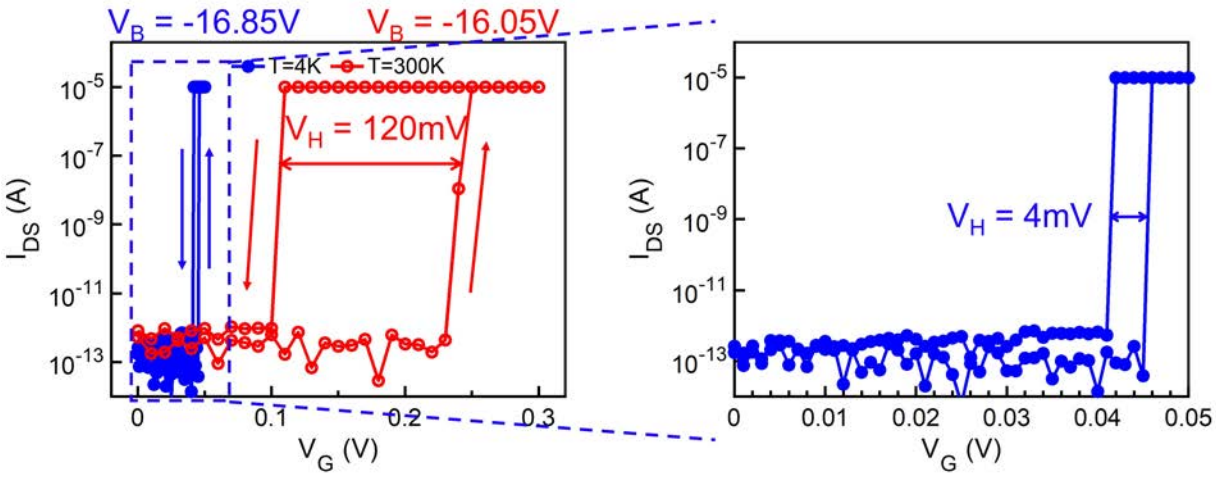


Figure 2.13: Body-biased relay I_{DS}-vs.-V_G characteristics at 300 K and 4 K.

In addition to low V_H, low R_{ON} is desirable for digital circuit operation for reduced RC (electrical charging/discharging) delay. It is difficult to maintain low R_{ON} for W-contact MEM relays operating at room temperature, due to contact oxidation [46, 90, 91]. Even in a vacuum environment with 1 μTorr pressure, trace amounts of O_2 can lead to native oxide formation on the surfaces of the W electrodes. Figure 2.14 shows that R_{ON} decreases dramatically for temperatures below 90 K. Since this is the boiling point of oxygen gas (O_2), sub-90 K operation inhibits the formation of native oxide on the electrode surfaces and thereby allows low R_{ON} to be maintained.

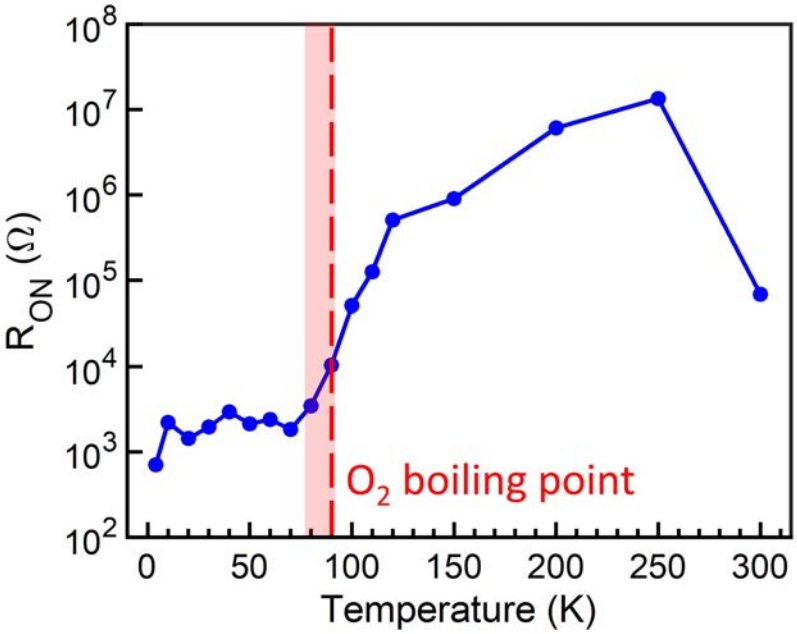


Figure 2.14: Temperature dependence of relay R_{ON}.

Relays used for implementing digital logic must operate properly over many switching cycles to be of practical use. Figure 2.15 compares how R_{ON} evolves over many ON/OFF switching cycles using 5 kHz square-wave gate voltage signals with 2 V gate overdrive and V_{DS} = 0.5 V, at various temperatures. Considering that R_{ON} should not exceed 10 kΩ for acceptable relay-based integrated circuit performance [92], the (hot) switching endurance of a MEM relay operating at 300 K is roughly 10^6 cycles. For relays operated at liquid nitrogen temperature (77 K) or liquid helium temperature (4 K), however, the endurance of a relay exceeds 10^8 cycles, since there is no O_2 to oxidize the W electrodes.

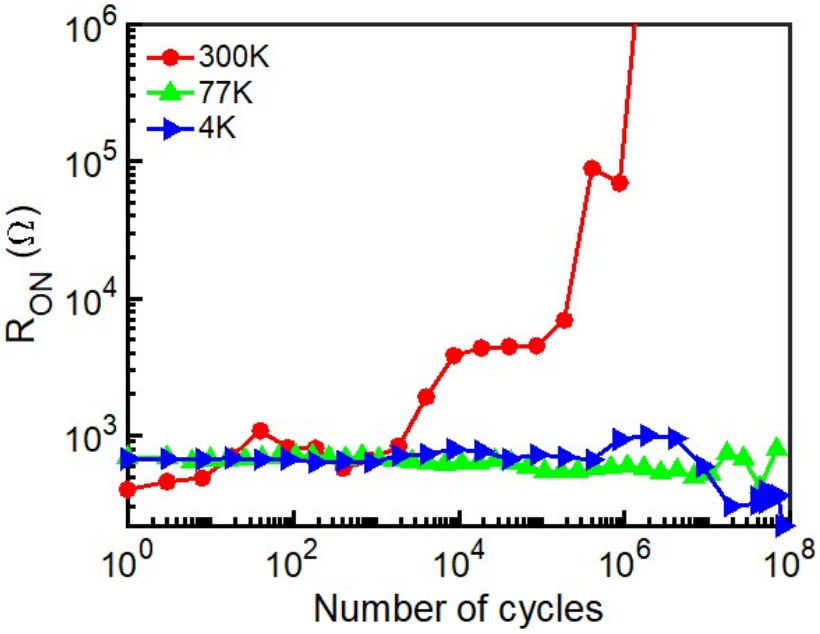


Figure 2.15: Relay endurance testing at various temperatures.

Figure 2.16 shows measurements of relay turn-ON delay at 300 K and 4 K. With a preset current compliance, the voltage across the source and drain decreases when the relay turns ON; therefore, the time when the output voltage starts to drop corresponds to the time that the relay is turned ON. The mechanical turn-ON delay at 4 K (0.22 μs) is slightly worse than that at 300 K (0.19 μs), possibly due to lower gate overdrive ratio (V_{GB}/V_{ON}).

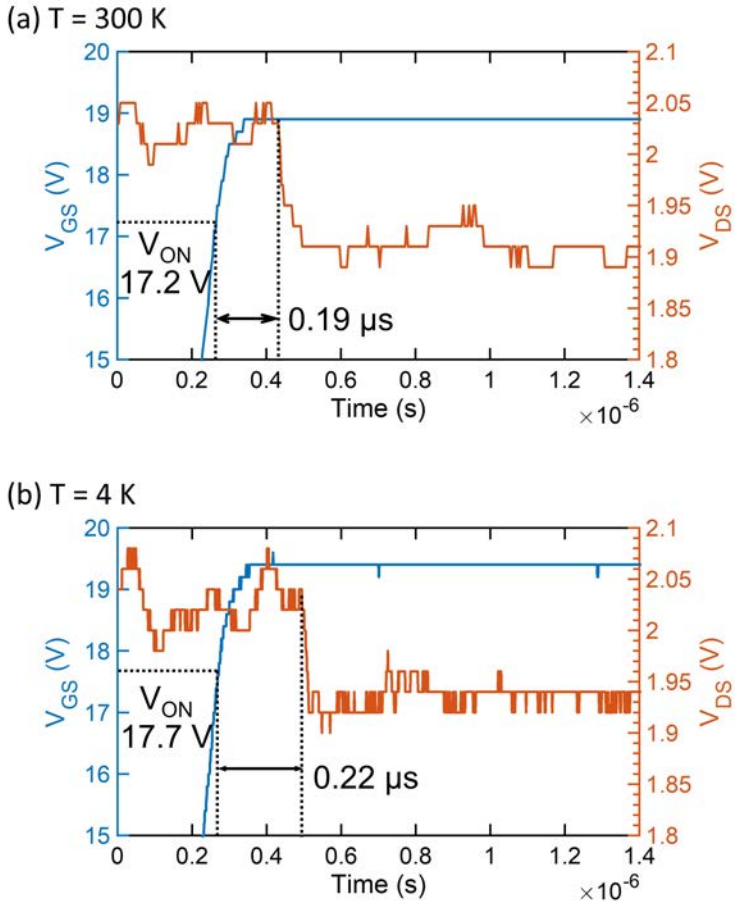


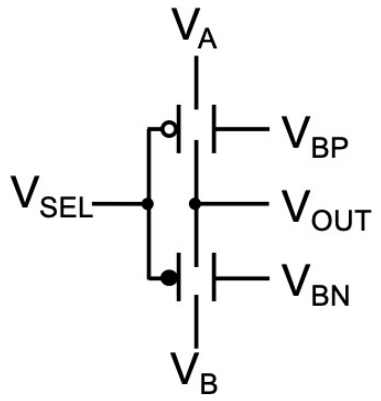
Figure 2.16: Relay turn-ON delay measurements with $V_B = 0$ V (a) at 300 K, and (b) at 4 K.

2.5 Millivolt Operation of Relay Integrated Circuits

The circuit diagram and truth table for a relay-based 2:1 multiplexer integrated circuit are shown in Figure 2.17). Note that it comprises only two relays, whereas a CMOS implementation requires at least 4 transistors. The upper relay has positive body bias (V_{BP}) so that it turns ON when the select voltage signal (V_{SEL}) is low, while the lower relay has negative body bias (V_{BN}) so that it turns ON in a complementary manner when V_{SEL} is high. Thus, the upper relay will pass the voltage signal V_A to the output (i.e., $V_{OUT} = V_A$) when V_{SEL} is low (logic '0'), and the lower relay will pass the voltage signal V_B to the output (i.e., $V_{OUT} = V_B$) when V_{SEL} is high (logic '1'). The waveforms in Figure 2.18(a) show proper circuit operation at 300 K with 100 mV signals, while the waveforms in Figure 2.18(b) show proper circuit operation at 77 K with sub-25 mV signals, made possible by smaller V_H values. (It

should be noted that V_{OUT} was monitored by an oscilloscope with an internal impedance of 1 MΩ. If a relay has high on-state resistance (R_{ON}) – due to electrode surface oxide formation – the input voltage signal will not be fully passed to V_{OUT} due to the voltage divider effect.)

(a)



(b)

V_{SEL}	V_{OUT}
0	V_A
1	V_B

Figure 2.17: (a) schematic circuit diagram and (b) truth table of a relay-based 2:1 multiplexer integrated circuit.

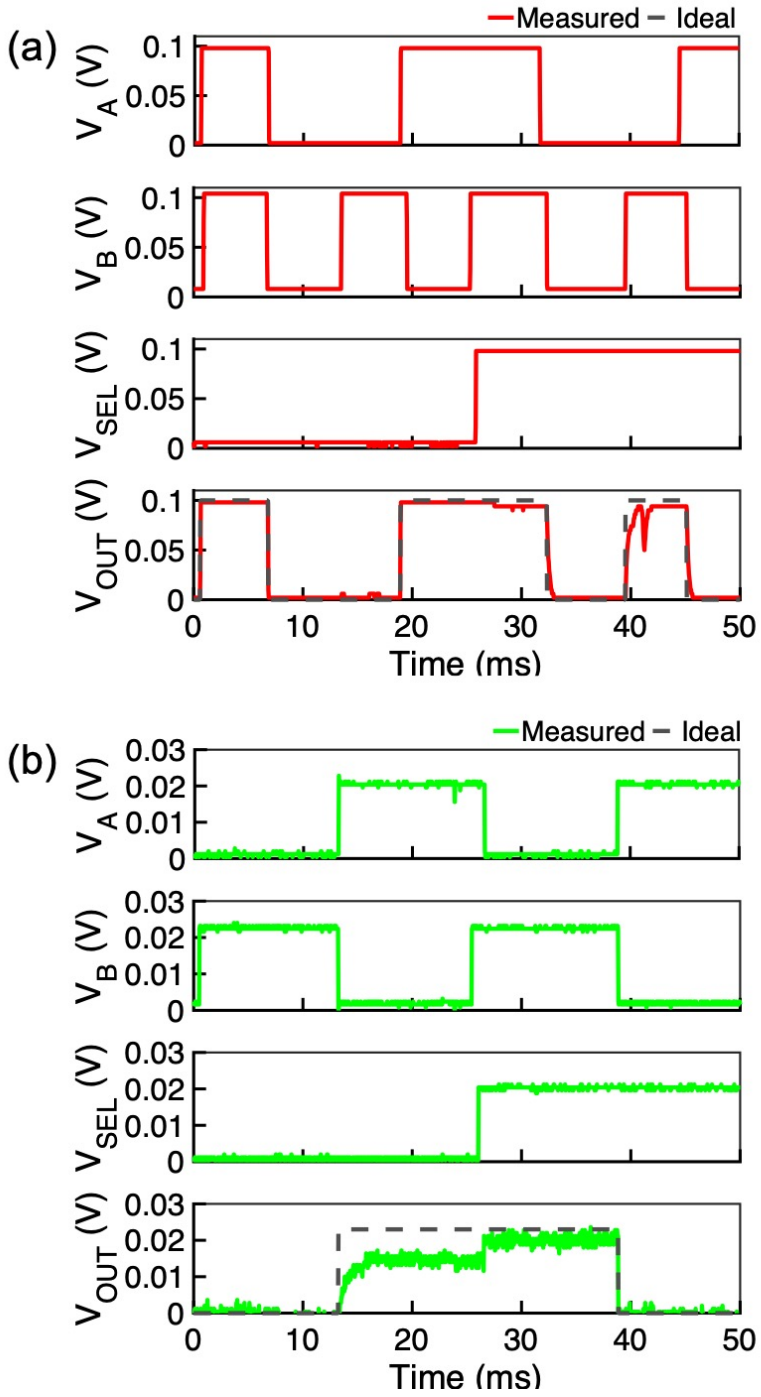


Figure 2.18: Measured voltage waveforms demonstrating operation of a relay-based 2:1 multiplexer (a) at 300 K (V_{BP} = 15.5 V, V_{BN} = -14.6 V), and (b) at 77 K (V_{BP} = 17.07 V, V_{BN} = -14.71 V).

A MEM relay can be used as a "pull-up" device or as a "pull-down" device in an inverter circuit, as shown in Figure 2.19. Similarly as a PMOS transistor, a relay with positive body bias can be used to pass a high voltage, V_{DD}, from source to drain when the input voltage is low (Figure 2.19(a)). Similarly as a NMOS transistor, a relay with a negative body bias can be used to pass a low voltage, 0 V, from the source to the drain when the input voltage is high (Figure 2.19(b)).

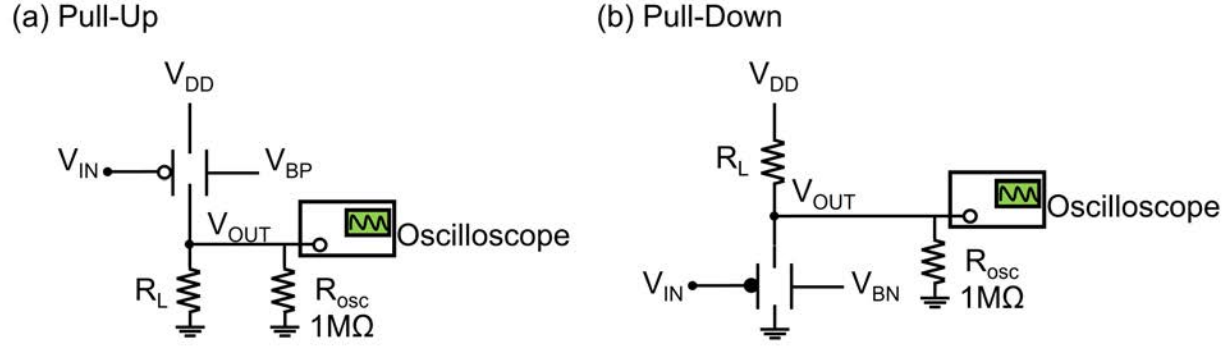


Figure 2.19: Inverter circuits: (a) MEM relay operating as a pull-up device and (b) MEM relay operating as a pull-down device.

A MEM relay can operate with sub-100 mV voltage swing at room temperature [87], as shown in Figure 2.20. With self-assembled molecular coating to reduce contact adhesive force, a MEM relay-based inverter circuit can operate with sub-50 mV voltage swing at room temperature [63], as shown in Figure 2.21

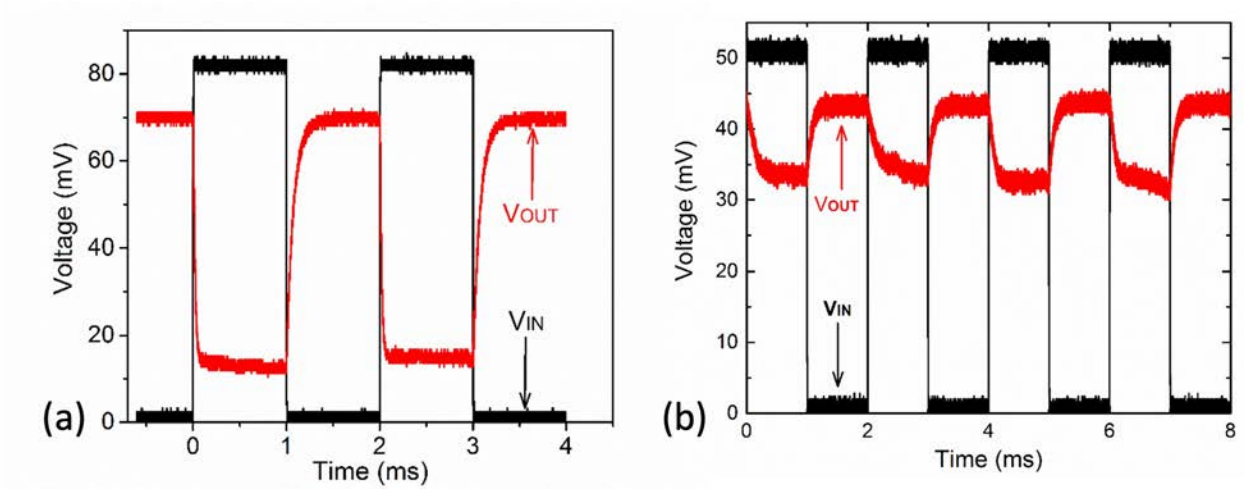


Figure 2.20: Demonstration of sub-100 mV inverter circuit operation at 300 K: (a) relay as pull-down device with V_{DD} = 80 mV, and (b) relay as pull-up device with V_{DD} = 50 mV. Adapted from [87].

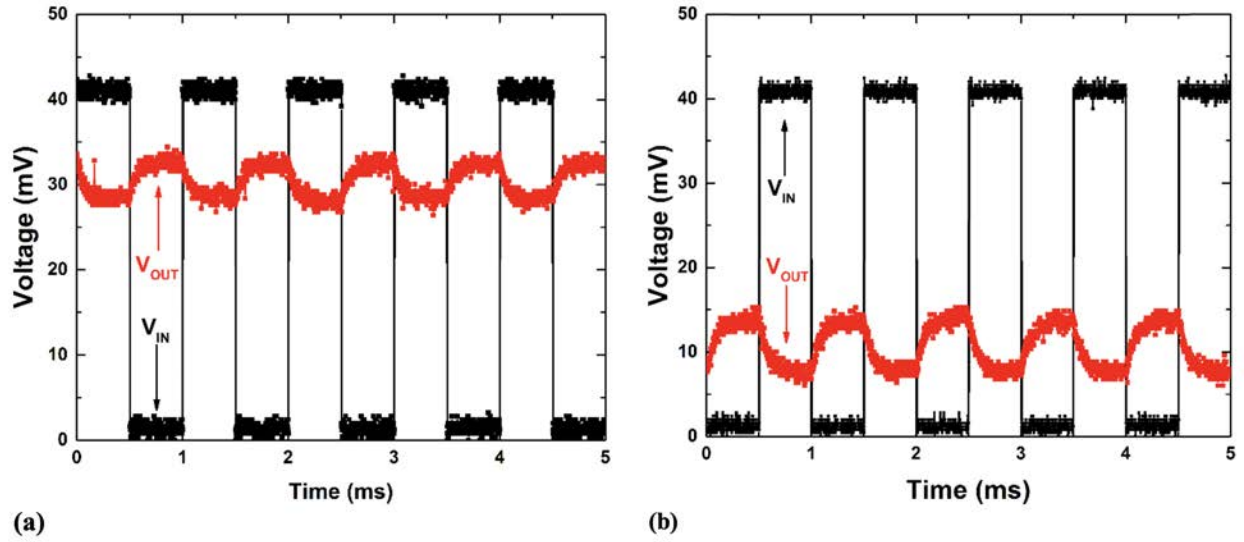


Figure 2.21: Demonstration of sub-50 mV inverter circuit operation, enabled by self-assembled molecular coating, at 300 K: (a) relay as pull-down device, and (b) relay as pull-up device. Adapted from [63].

When MEM relays are operated at 4 K, they have much smaller hysteresis voltage and hence can be operated with sub-10 mV gate voltage swings, as shown in Figure 2.22. Note

that the 10 mV input voltage waveform (in black) is a bit noisy because it is generated using a voltage divider.

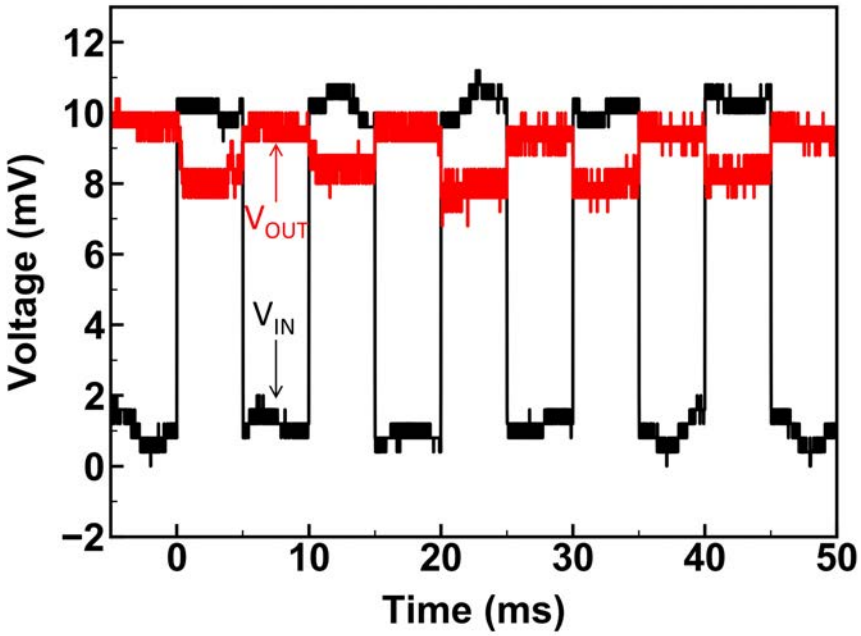


Figure 2.22: Measured voltage waveforms of a sub-10 mV relay-based inverter circuit in which a MEM relay is configured as a pull-down device at 4 K.

2.6 Summary

In this chapter, we demonstrated that MEM relays can operate reliably with millivolt signals at cryogenic temperatures, due to much lower hysteresis voltage (V_H) and more stable ON-state resistance (R_{ON}) with endurance exceeding 10^8 switching cycles. Relay digital ICs are demonstrated to function with sub-25 mV voltage signals, providing for more than 10 times lower V_{DD} than for CMOS technology. A sub-10 mV relay-based inverter circuit is demonstrated at 4 K. Our experimental study indicates that MEM relays should be able to operate at temperatures as low as 1.8 K, making them promising candidates for ultra-low-power cryogenic digital interface circuits for quantum computing.

Chapter 3

Contact Material Exploration for Cryogenic MEM Relays

3.1 Introduction: Why Superconducting Relays?

Cryogenic operation of digital logic circuitry is gaining increasing attention with the advent of quantum computers, which require electronic switches to interface with quantum bits (qubits) [82]. As explained in the previous chapter, digital logic electronic control circuitry ideally should be monolithically integrated with the qubits and dissipate as little energy as possible in order to keep the quantum computer operating at mK temperatures. In contrast with CMOS transistors, MEM relays can function with negligible OFF-state leakage current and ultra-low-voltage signals, enabling sub-50 mV operation at room temperature [64, 87] and sub-25 mV operation at 77 K [66]. Also, relay operating characteristics are improved for cryogenic temperature operation compared to room temperature operation: the switching hysteresis voltage decreases due to reduced contact adhesive force – enabling ON/OFF switching with voltage signals below 5 mV (Figure 2.13) [66] – and the contact resistance is very stable due to the absence of contact oxidation (Figure 2.14). Electrical conductivity measurements of the electrode layers indicate that MEM relays should function properly down to 1.8 K (Figure 2.7).

Superconductive electrodes would be advantageous for achieving the lowest possible ON-state resistance in MEM relays operating at cryogenic temperatures. Tungsten (W) thin films generally comprise crystalline grains of two phases: the alpha phase becomes superconductive at 15 mK, while the beta phase has a superconducting transition temperature between 1 K and 4 K. Tungsten films comprising both alpha and beta phases usually have superconducting transition temperature around 100 mK [93, 94]. The sputtered W films used in the MEM relays in this work are not superconductive at 1.8 K, as shown in Figure 2.7. Therefore, to achieve superconductivity across a wide range of cryogenic temperatures, an alternative electrode material that has a higher transition temperature is desirable. Pure niobium (Nb)

is a candidate, as it has a higher transition temperature of 9.29 K [95]. In general, any potential relay electrode material should satisfy the following requirements:

1. The material should have a high melting point to avoid contact micro-welding issues. Figure 3.1 shows a simulated temperature contour plot due to Joule heating for a 10 nm contact asperity with 1 V contact voltage applied. The peak local temperature must be lower than the contact material's melting point. Since the melting temperature of niobium (Nb) is about 2750 K [95], a MEM relay with Nb electrodes should function reliably without contact welding.

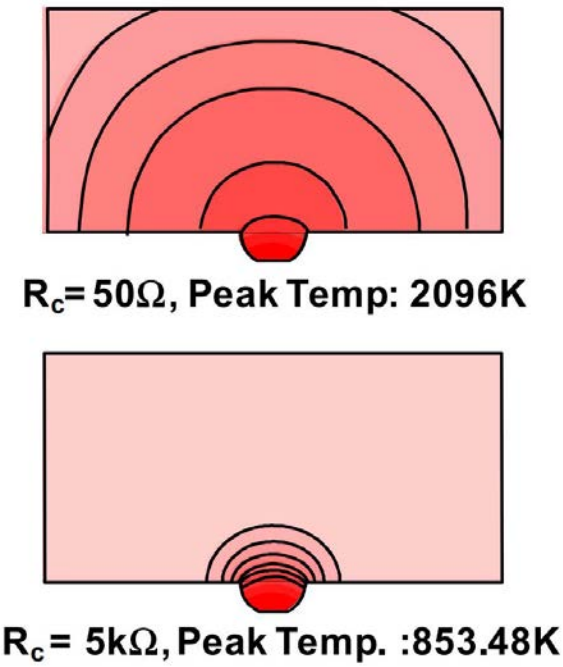


Figure 3.1: ANSYS-simulated temperature contours at a contacting electrode asperity under Joule heating. For simplicity, all the contacting asperities are lumped into one, and the asperity radius is set to be 10 nm. The simulated voltage drop across the contact is 1 V. Adapted from [96].

2. The material should be resistant to mechanical wear [91, 97]. W was originally chosen as the electrode material for our MEM relays because of its high hardness; after 10^{10} ON/OFF switching cycles, the root-mean-square surface roughness (R_q) of the W surface only decreased slightly, as shown in Figure 3.2 [91]. The Brinell Hardness of W is 392-4560 MPa [98], while the Brinell Hardness of Nb is 736-2450 MPa [98]. Therefore, electrode wear should not be an issue if Nb is used as the contact material for MEM relays.

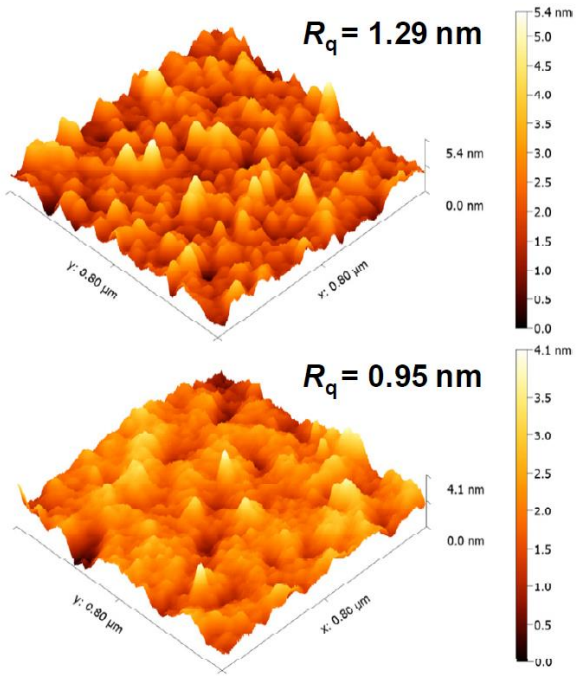


Figure 3.2: Atomic force microscopy images of tungsten electrode surfaces from a fresh relay (R_q = 1.29 nm) vs. a cycled relay (R_q = 0.95 nm). Adapted from [91].

3. The material should not require high processing temperatures, so that it can be easily monolithically integrated with qubits using a modular (post-qubit) fabrication process. Assuming that qubits have similar thermal budget tolerance as CMOS circuitry, this means that the superconducting material deposition temperature should be less than 410 °C. Nb can be deposited at room temperature by ion beam assisted sputtering [99] or by magnetron sputtering [100]. Besides, Nb can be patterned by dry etching using CH_4 and O_2 plasma [101], as well as Ar/Cl_2 plasma [102].

4. The material should be compatible with vapor-phase hydrofluoric acid (HF). To avoid stiction-induced failure, which occurs when attractive capillary forces overwhelm the spring restoring force of a MEM switch causing the switch to close permanently, it is necessary to utilize vapor-phase hydrofluoric acid (HF) to release the fabricated MEM relays. As a result, the electrodes are exposed to HF vapor. Vapor-HF cycling tests were performed on Nb films, and the results show that Nb is compatible with HF vapor.

Since Niobium has similar mechanical and electrical properties as tungsten, and is also

compatible with the MEM relay fabrication process, it is a promising electrode material for cryogenic relays due to its higher superconducting transition temperature.

3.2 Niobium-Contact Relay Fabrication Process Development

The fabrication process for niobium-contact MEM relays is very similar to that of tungsten-contact MEM relays (cf. Figure 2.5). The main differences are in the Nb deposition, Nb etching, and photoresist coating/removal steps, described in detail below.

First, after an insulating Al_2O_3 film is deposited onto the Si wafer substrate by ALD, the Nb electrode layer is deposited by sputter deposition using the Ast-sputter tool. (The Ast-sputter is a multi-target sputtering tool; the sputtering target has to be loaded manually before use. Overnight pump-down is preferred for better sputtered material quality.) For Nb sputtering, the process pressure is set to be 1.5 mTorr, the DC power is set to be 150 W, the Ar flow rate is set at 56 sccm, the substrate temperature is 300 °C. A sputtering time of 10 minutes yields a 140 nm-thick Nb film with sheet resistance approximately $4\,\Omega/\square$, which is similar to that of the W electrodes used for W-contact relays.

Figure 3.3 (a) shows how the sheet resistance of the sputtered Nb film varies with temperature across the range from 1.8 K to 300 K. It can be seen that the sheet resistance of the Nb film drops significantly at temperatures below 10 K. Figure 3.3 (b) plots the Nb sheet resistance for temperatures below 10 K, measured slowly with 0.5 K/min changing rate. It can be seen that the superconducting transition temperature of the deposited Nb film is approximately 5.4 K.

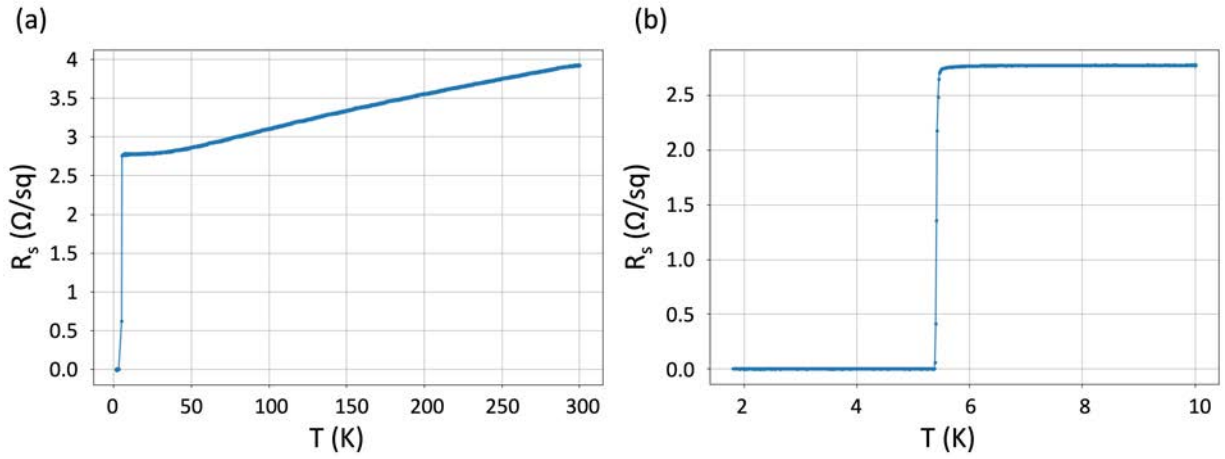


Figure 3.3: Sheet resistance vs. temperature of sputtered Nb thin film: (a) measurement with a temperature ramp rate of 5 K/min, and (b) measurement with a temperature ramp rate of 0.5 K/min. The superconducting transition temperature is approximately 5.4 K.

Lithography and etching steps are used to pattern the sputtered Nb film. Different from the W-contact relay fabrication process, hexamethyldisilazane (HMDS) pre-treatment is used to passivate the Nb thin film surface before coating it with 0.43 μm UV210 photoresist. This is to prevent the formation of NbO when positive photoresist comes into contact with Nb [103].

In this work the Nb film is etched using the Lam 7 tool, using the same mask as described in Figure 2.5(c). The chamber pressure is 8 mTorr, the flow of Cl_2 is 130 sccm, the upper electrode power (TCP RF) is set to be 400 W, and the lower electrode power (bias RF) is set to be 100 W; the etch rate is approximately 12 nm/s and the etching time used was approximately 15 seconds. Immediately after etching, a DI water rinse in an atmospheric passivation module (APM) supplemented with DI water pour is needed to prevent chlorine corrosion of Nb upon exposure to the atmosphere.

After etching, the photoresist needs to be removed. In order to reduce the ashing time in oxygen plasma, wafers are first soaked in MICROPOSIT Remover 1165 at 80 °C in Msink1. After 2 hours of soaking, it was found that photoresist residue remains on the wafer, as shown in Figure 3.4 (a). After 1-minute ashing in the Matrix tool, the photoresist is fully removed, as shown in Figure 3.4 (b).

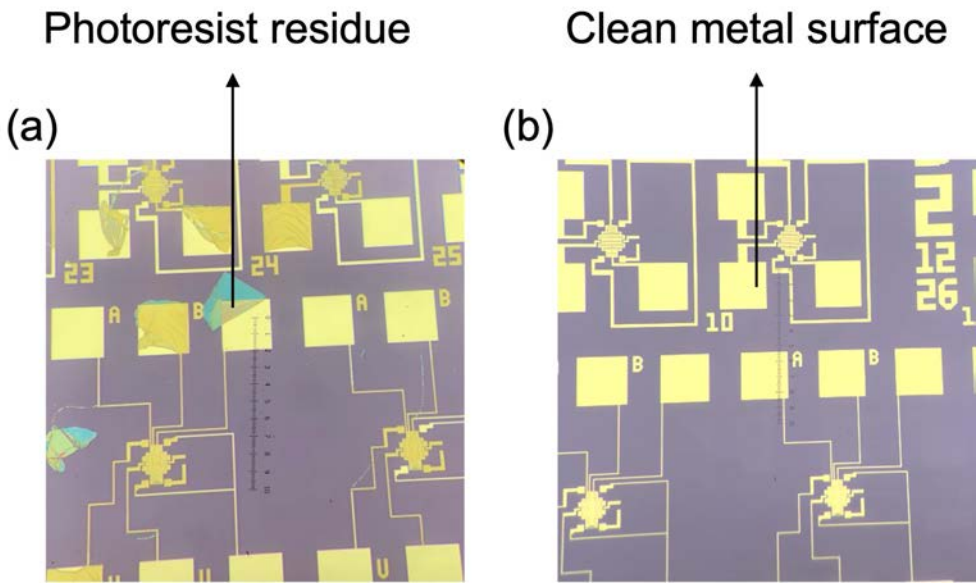


Figure 3.4: Microscopic images of a relay wafer surface after Nb etching: (a) after soaking for 2 hours in MICROPOSIT Remover 1165 bath, and (b) after additional oxygen plasma ashing for 1 minute at 250 °C.

The same cleaning process and sacrificial LTO layer deposition and patterning steps are used for Nb-relays as for W-relays (cf. Figure 2.5(d)-(g)). Afterwards the second Nb electrode layer is sputtered on top of the second LTO layer using the same recipe in Ast-sputter as described above. It is worthwhile to note here that ruthenium-contact MEM relays were previously developed and that it was found that ruthenium films crack and delaminate from LTO surfaces upon being exposed to atmosphere, due to moisture present in air [97, 104]; in contrast with ruthenium, a thin film of Nb does not delaminate from the LTO surface. Although under the microscope some tiny crack lines were observed near the edge of the wafer and some test structures (Figure 3.5(a)), the device area looks clean with no crack lines (Figure 3.5(b)). This is presumably due to larger stress in a thicker metal film near the edge of the wafer. The same lithography and etching processes used to pattern the first Nb layer were used to pattern the second Nb electrode layer.

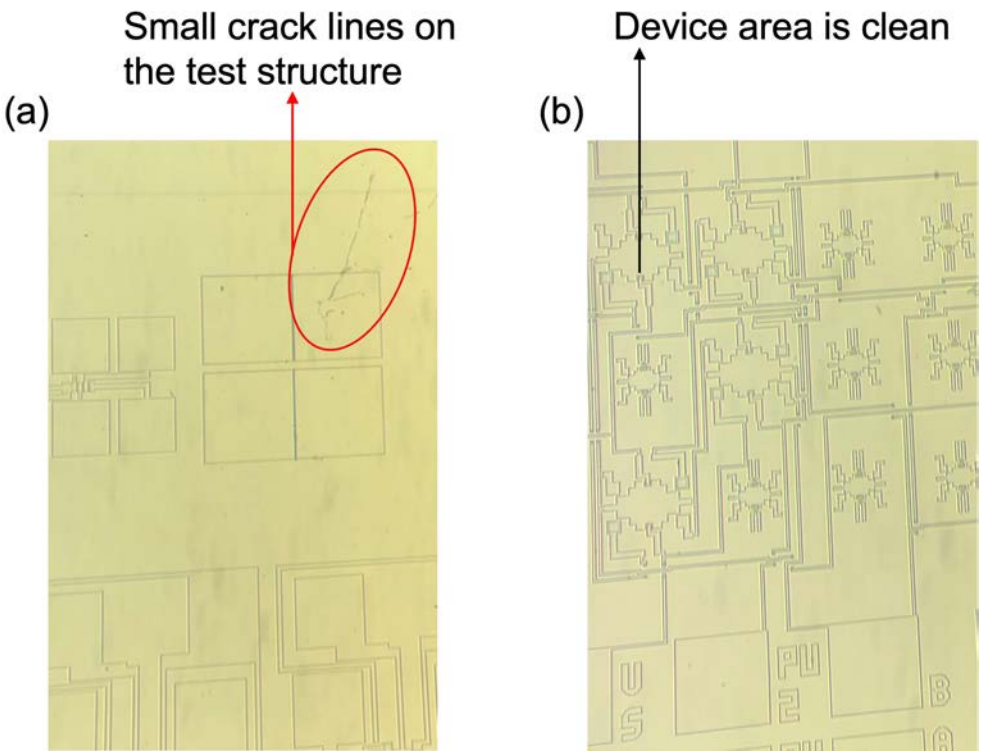


Figure 3.5: Microscope images of a relay wafer surface after the second Nb film is sputtered on top of LTO, showing: (a) small crack lines on a test structure, and (b) no cracking issues in the device area.

The remaining Nb-contact MEM relay fabrication process steps are the same as described in Figure 2.5(j)-(r).

3.3 Niobium-Contact Relay Operating Characteristics

Since the native oxide of niobium is not conductive, niobium-contact MEM relays also require an oxide breakdown process to achieve lower ON-state resistance. The hot-switching oxide-breakdown method used in this work is illustrated in Figure 3.6: first, 3 to 5 V is applied across the source and drain contact (V_{DS}) before the relay is turned ON, and then the gate voltage is stepped from 0 V to V_{ON} + 2V; at each step the current flowing between the source and drain electrodes is measured before proceeding to the next voltage step, and the current compliance is set to be 1 μA. This hot-switching oxide-breakdown method is implemented using a Keithley 4200A Device Parameter Analyzer and was found to be effectively for lowering ON-state resistance.

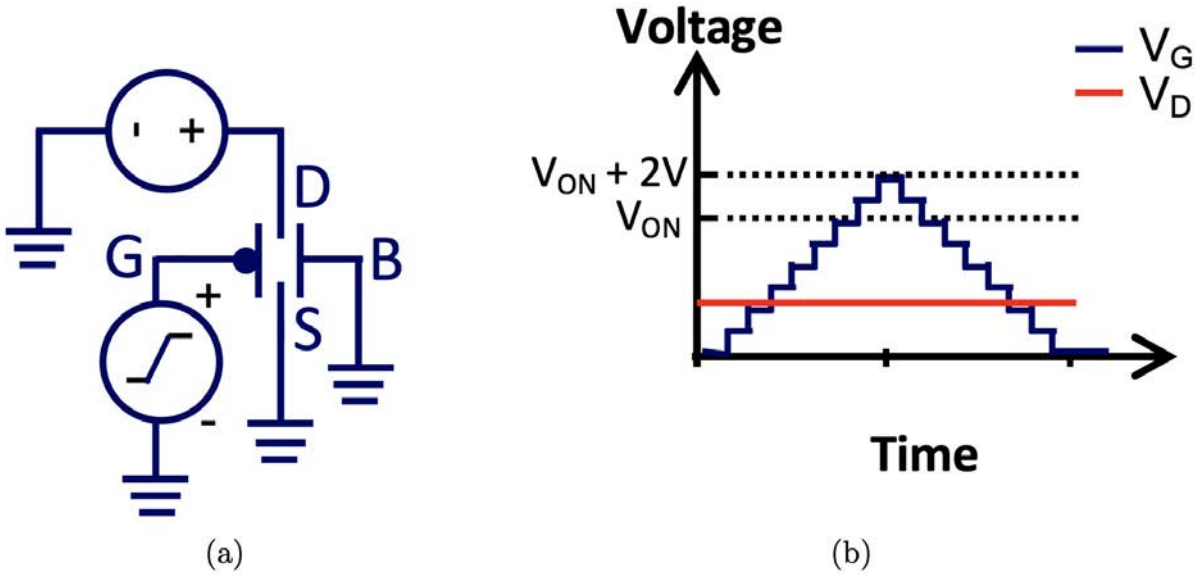


Figure 3.6: The hot-switching oxide-breakdown method (a) circuit schematic and (b) voltage timing waveforms (not to scale). Adapted from [42].

I_{DS} -vs.- V_{GB} characteristics were measured for relays of the dual-bridge source/drain contact design (Figure 3.7(a)) and dual-direct source/drain contact design (Figure 3.7(b)). The measured results are shown in Figure 3.8.

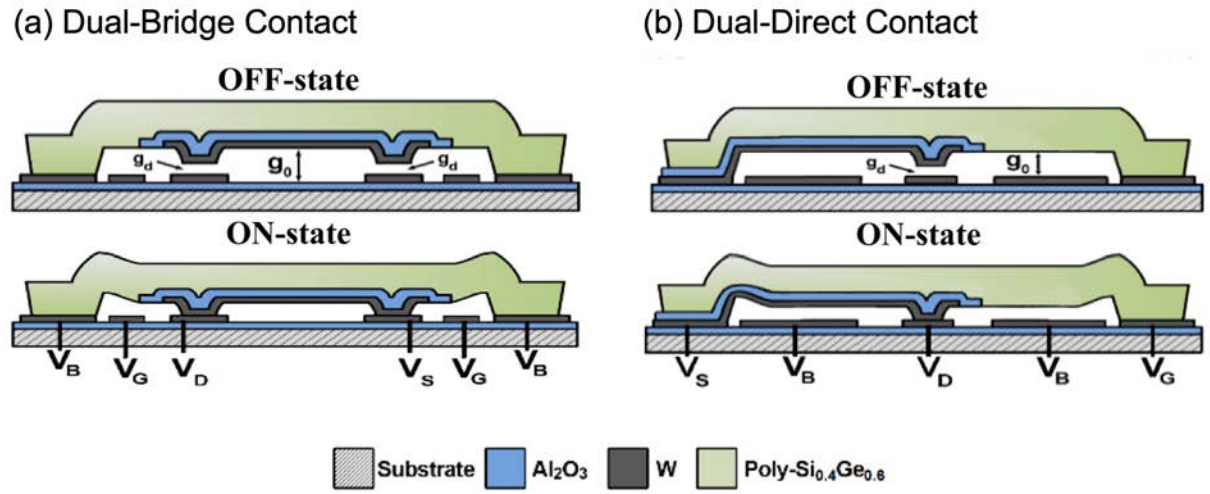


Figure 3.7: Schematic cross-sections of MEM relays with different contacting electrode designs, in the OFF-state and in the ON-state: (a) dual-bridge source/drain contact design, and (b) dual-direct source/drain contact design. Adapted from [46, 64, 105].

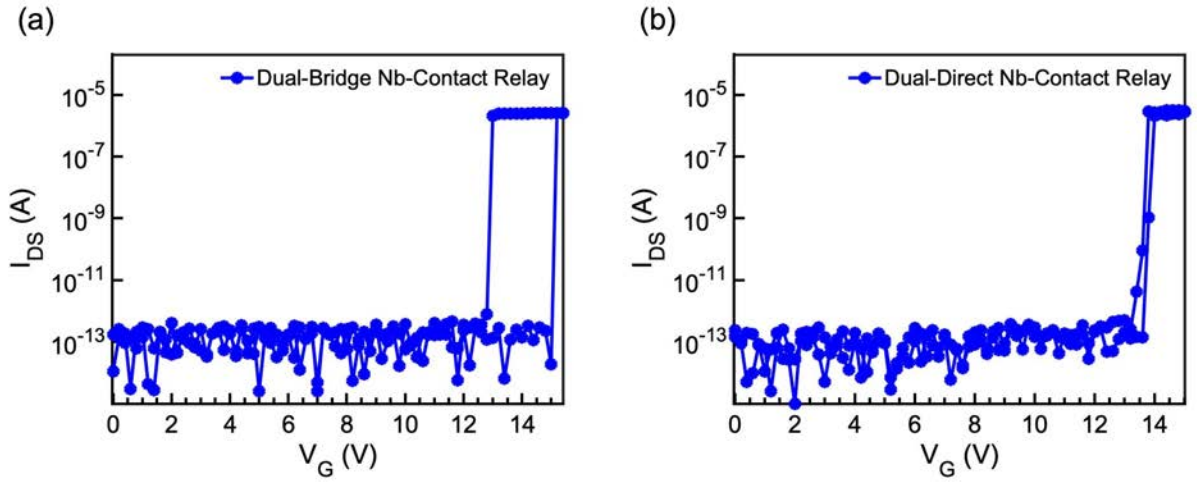


Figure 3.8: Measured I_{DS} -vs.- V_{GB} characteristics of Nb-contact relays. (a) dual-bridge contact design, (b) dual-direct contact design.

It can be seen from Figure 3.8 that the dual-bridge contact relay has larger V_H than the dual-direct contact relay; this is the same as for tungsten-contact MEM relays as reported in [64, 105], and is due to the larger total contact area (hence larger contact adhesive force)

for the dual-bridge contact design. Statistical data for V_H and R_{ON} across 10 different relays, for each of the two different contact designs, are shown in Figure 3.9. It can be seen that the dual-bridge design generally has larger associated hysteresis voltage and smaller ON-state resistance than the dual-direct design. The larger ON-state resistance of the dual-direct contact design can be explained by the larger sheet resistance of the second deposited Nb layer: the second Nb layer has a sheet resistance that is two times larger than the first Nb layer, as shown in Table 3.1, possibly due to contamination in this Nb layer during the fabrication process, as discussed below.

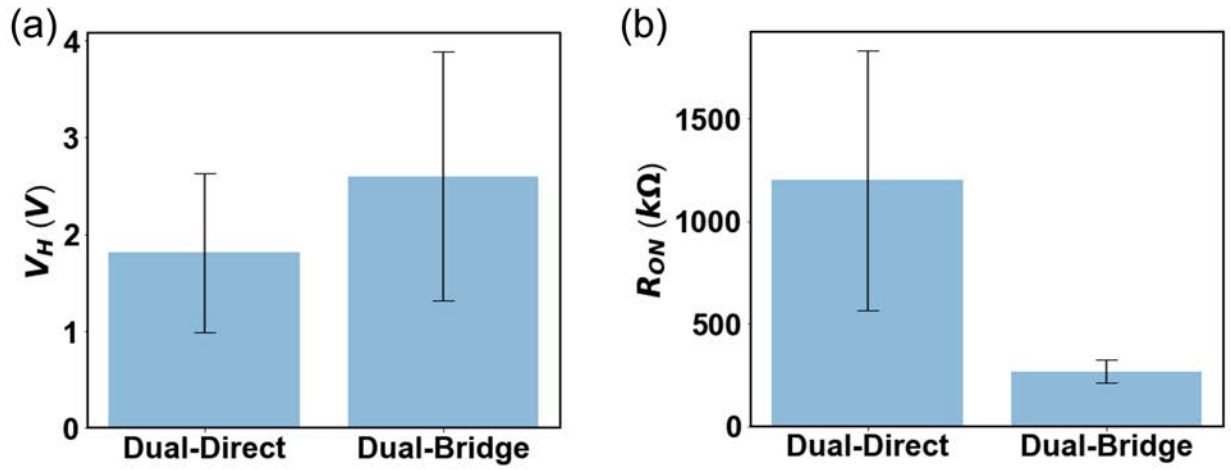


Figure 3.9: Average measured values of (a) V_H and (b) R_{ON} for 10 Nb-contact relays of each contact design. The error bars indicate the ranges of standard deviation.

Table 3.1: Comparison of sheet resistance values for the electrode and structural layers in W-contact and Nb-contact relays (unit: Ω/□)

Relay Type	First Metal Layer	Second Metal Layer	Structural SiGe
W-contact	3.0	3.1	2.5
Nb-contact	4.0	8.0	2.4

Unfortunately the Nb-contact relays were found to not exhibit superconductivity at 1.8 K: Measured sheet resistance vs. temperature behavior for a niobium thin-film test structure on the fabricated chip is shown in Figure 3.10. No abrupt drop in resistance to 0 Ω/□ is observed.

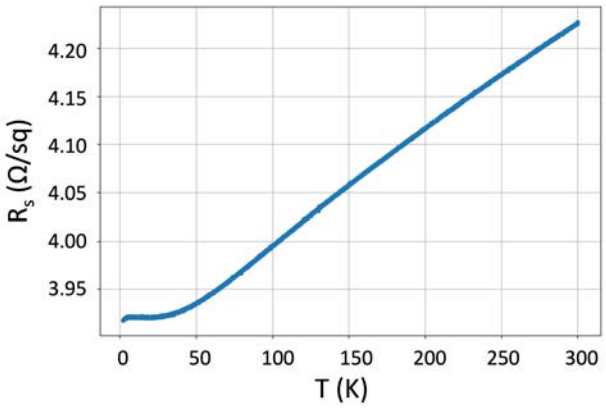


Figure 3.10: Measured sheet resistance vs. temperature of a niobium test structure on the fabricated chip. The temperature was ramped from 1.8 K to 300 K, at 1 K/min.

3.4 Discussion

The sheet resistance of the test structure on a fully processed chip, shown in Figure 3.10, is higher than that for a blanket film, shown in Figure 3.3. This might be due to reaction of the Nb film during the fabrication process; for example, the Nb electrode surface may have been oxidized by exposure to O_2 at 400 °C during the LTO film deposition process.

Since the Ast-sputter tool is shared equipment that is used to deposit multiple materials, the purity of the sputtered thin film may have been compromised: Even though a dedicated deposition chimney and shield dome (for covering the metal target) was used, the deposited Nb film might have been contaminated with other metal elements since the deposition chamber is dirty. Figure 3.11 shows a measured energy-dispersive X-ray (EDX) spectrum for a blanket deposited Nb film that is not superconducting at 1.8 K. (This film did not undergo lithography, etching, and LTO deposition processes.) In addition to Nb, the detected metals include iron (Fe), aluminum (Al), and chromium (Cr), which are all targets available for use in the Ast-sputter tool. The rubidium (Rb) peaks might be a fake signal, as there is no Rb target available for the Ast-sputter tool.

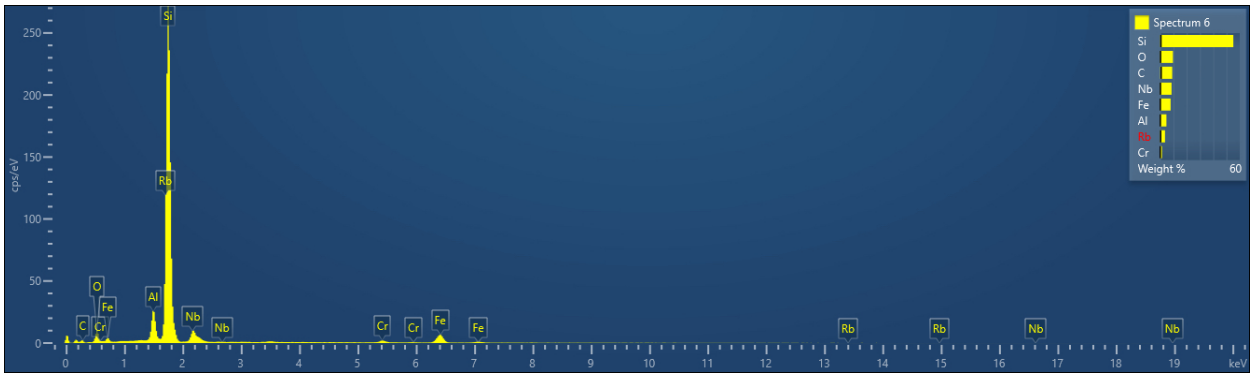


Figure 3.11: Measured EDX spectrum of a deposited Nb film that is not superconducting at 1.8 K, showing the presence of Fe, Al, and Cr in the Nb film.

MRC943, also an MRC Sputtering System that is similar to the MRC944 tool (used for tungsten thin film sputter deposition, described in Chapter 2.2), can also be used to deposit Nb. Compared with Ast-sputter, MRC943 is much cleaner since it has a chamber for Nb sputtering only. The DC source power is set to be 1.5 kW and the sputtering pressure is 8 mTorr. After 3 sputtering cycles, the Nb film is about 60 nm, and the sheet resistance is approximately 4.3 $\Omega/\square$. A sheet resistance vs. temperature measurement was performed to check the superconductivity of the Nb film deposited by MRC943. It can be seen from Figure 3.12 that this film has a superconducting transition temperature of 8.58 K.

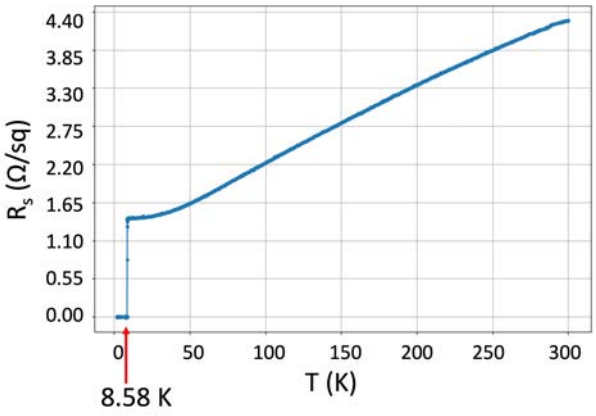


Figure 3.12: Measured sheet resistance vs. temperature of a niobium film deposited in the MRC943 tool. The temperature was ramped from 1.8 K to 300 K at a rate of 1 K/min. The superconducting transition temperature is 8.58 K.

In order to protect the Nb film from exposure to O_2 during the LTO deposition step, a 10 nm TiO_2 was deposited by ALD using the Picosun tool. However, after patterning the TiO_2 and Nb stack and subsequently depositing LTO and then removing the LTO and TiO_2 in vapor HF, the Nb film was found to be non-superconductive at cryogenic temperatures. Moreover, if the TiO_2 and Nb stack is not patterned, then after LTO is deposited and removed in vapor HF the Nb film cracks due to stress, as shown in Figure 3.13. Although patterning of the Nb film helps to relieve the stress, cracks could still be observed in regions near the edge of the wafer.

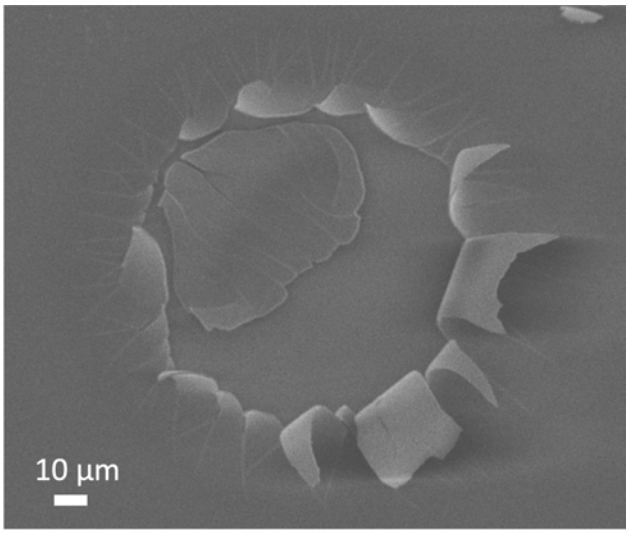


Figure 3.13: Scanning electron micrograph image of a Nb film after TiO_2 and LTO deposition, and vapor HF removal of the oxide layers.

Other superconductive materials could be explored in the future for achieving superconducting relays. For example, TiN can be superconducting [106, 107]; however, TiN cannot withstand HF vapor [97], so an alternative sacrificial material would be required.

3.5 Summary

In this chapter the possibility of using niobium as the contacting electrode material to achieve superconducting MEM relays was investigated. The conductivity of a sputter-deposited Nb film was measured to confirm superconductivity at cryogenic temperatures, and Nb-contact relays were successfully fabricated. The fabricated relays were found to not have superconductive behavior, however, and attempts to protect the Nb from oxidation during the fabrication process were found to be ineffective to solve this issue.

Chapter 4

Study of DC-Driven MEM Relay Oscillators for Implementation of Ising Machines

4.1 Ising Machine Background

The proliferation of Big Data and machine learning in recent years has greatly increased the need for computing resources. Today, leading-edge computing technologies are struggling to keep pace with the energy efficiency and performance requirements for computationally intensive applications. To address this issue, alternative approaches are needed to solve large computational problems much more efficiently than conventional digital computers that are based on the traditional von Neumann computing architecture. The Ising model is considered a promising non-von Neumann computing architecture for solving many combinatorial optimization problems [108, 109].

An Ising machine is a physical system to which a combinatorial problem can be mapped, whose absolute or approximate ground (lowest energy) state corresponds to the solution of the combinatorial problem [53]. An Ising machine comprises a network of discrete variables s_i, referred to as spins. Each spin takes a binary value ± 1 to minimize the "energy function" expressed mathematically as the Ising Hamiltonian shown in Equation 4.1. Combinatorial optimization problems are mapped onto Ising machines by assigning appropriate values to the coefficients J, which correspond to the coupling strength between spins, as shown in Figure 4.1. The combinatorial optimization problems then can be solved efficiently due to the inherent convergence property of the Ising physical system towards its ground state [110].

$$H = -\sum_{i,j,\, i<j} J_{ij} s_i s_j$$
$$s_i \in \{-1, +1\} \tag{4.1}$$

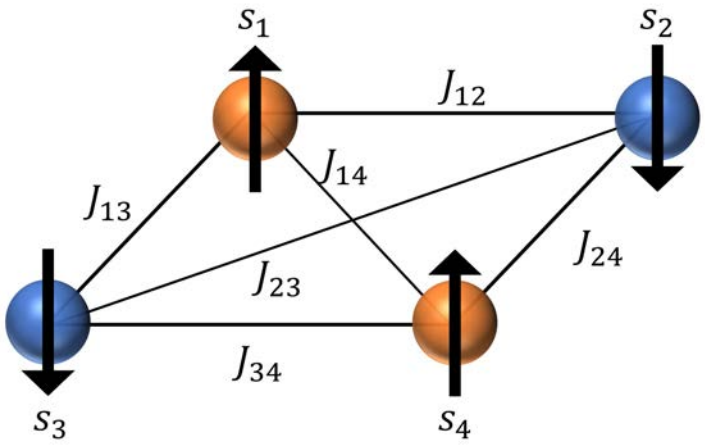


Figure 4.1: Illustration of a four-spin Ising model. Each spin can be either up or down, and the coupling strength between spin s_i and s_j is J_{ij}.

One practical example of a combinatorial optimization problem is the optimization of a very large scale integrated (VLSI) circuit chip layout. Floorplanning of functional blocks in VLSI design automation can be formulated as a "rectangle packing problem" which is an NP-hard problem. Given N rectangles with fixed sizes as shown on the left, the design goal is to minimize the boundary box area, $W \times H$, without overlapping of the rectangles, as shown in Figure 4.2. A brute-force search can be used to solve this problem, but it requires large computational resources and time when N becomes very large. Instead, this problem can be mapped onto an Ising machine with $3N^3$ spins and solved within several oscillation cycles, for a much faster time and lower energy to reach the solution [111].

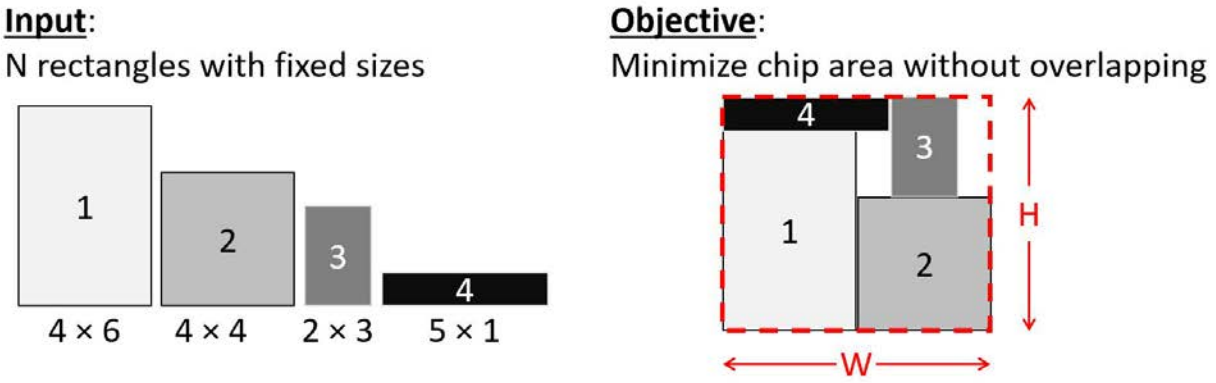


Figure 4.2: The combinatorial optimization problem in VLSI floorplanning design can be formulated as the "rectangle packing problem." Reproduced from [111].

Another interesting example is the "graph coloring problem" which is one of the most famous nondeterministic polynomial time (NP)-complete problems [109]. For example, with a set of 4 colors, the task is to assign colors to all the 51 states of the US so that every two adjacent states have different colors, as shown in Figure 4.3 [58]. This problem can be solved by an Ising machine with $4 \times 51 = 204$ spins. Generally, the graph coloring problem can be solved by an Ising machine with nN spins, where n is the number of available colors and N is the problem size [109]. For each state (or vertices in a general graph coloring problem), there are n spins associated with it to represent the coloring scheme, and only one of them can be in the $+1$ state.

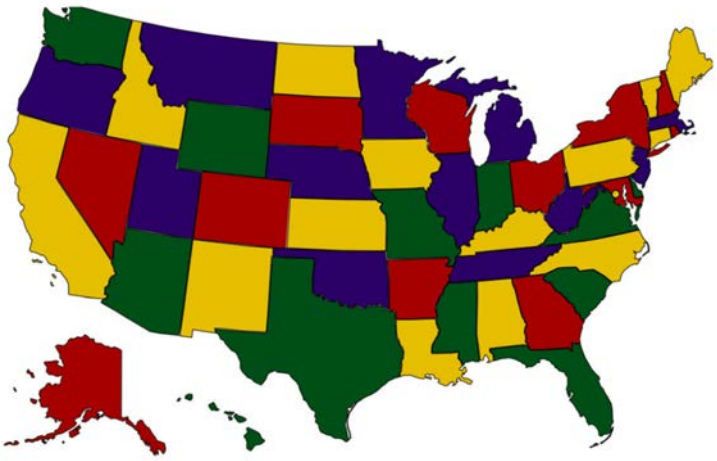


Figure 4.3: The result of the U.S. map coloring problem solved by an Ising machine. Adapted from [58].

There are many different ways to implement an Ising machine. For example, D-Wave Systems built adiabatic quantum annealers which have 2000 spins and operate at a temperature of about 15 mK [112, 113]. Such quantum Ising machines have a large footprint for the necessary cooling system, and cost about $15 million [114]. Another approach is to use non-quantum devices as "spins" to enable room temperature operation. The most notable example is the coherent Ising machine (CIM), which uses laser pulses traveling through a multi-kilometer-long optical fiber, or degenerate optical parametric oscillators, as Ising spins, so that an Ising machine is implemented as a network of coherent optical oscillators [49,115]. Although this approach does not require a cooling system, it needs sophisticated manual fabrication and assembly processes [116]. Besides, it is difficult to miniaturize the CIM due to its kilometer-long optical fibers.

Compared with the above approaches, an ideal Ising machine should have the advantages including lower cost, lower power consumption, higher scalability to more spins, higher speed, and easier fabrication process. It has been shown that Ising machines can be realized using a network of coupled nonlinear self-sustaining oscillators [58,117,118]. In an oscillator-based Ising machine (OIM), the phase of each variable oscillator takes a binary value of 0° or 180°, as shown in Figure 4.4 (a). This is achieved through sub-harmonic injection locking (SHIL) by applying to each oscillator a perturbation signal whose frequency is roughly double the oscillators' natural frequency, as illustrated in Figure 4.4 (b) [118]. The lowest energy configuration is determined by the coupling network, and corresponds to the minimum of the Ising Hamiltonian.

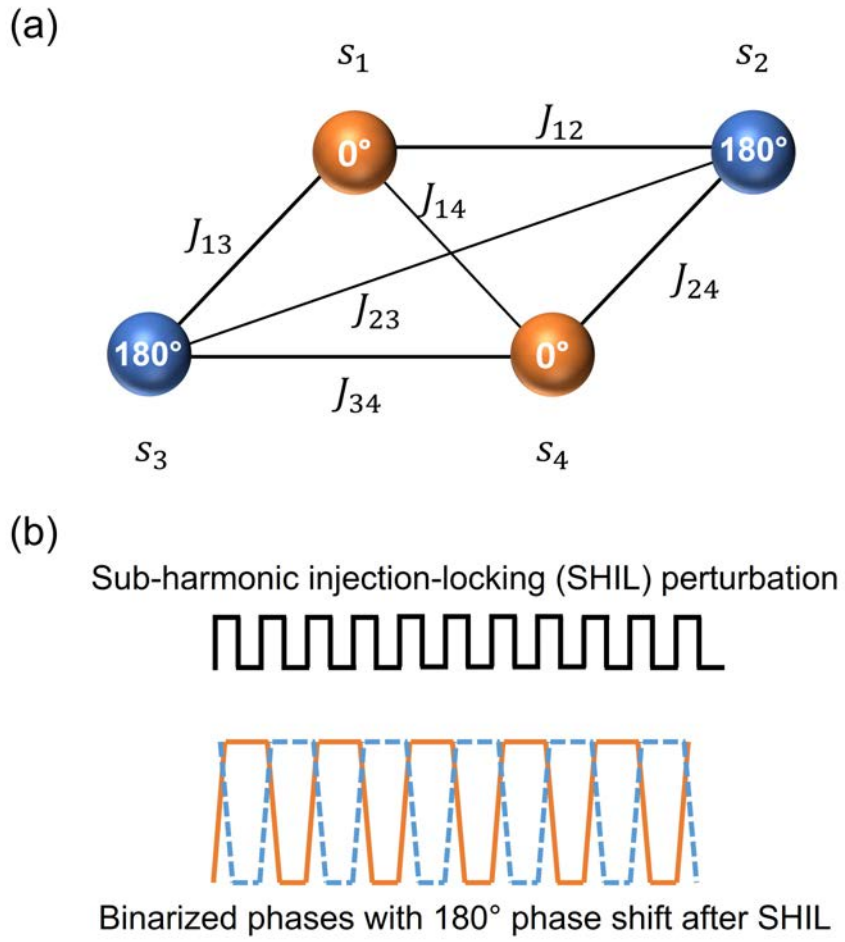


Figure 4.4: Oscillator-based Ising Machine (OIM) concept: (a) Illustration of a 4-spin Ising model implemented using oscillators. (b) A perturbing sub-harmonic injection signal causes the oscillators to settle into one of two phase states (0° and 180° phase shift).

In this chapter, the self-sustaining oscillation behavior of micro-electro-mechanical (MEM) relays is systematically investigated via experiments and computer simulations. The effects of DC bias voltages on oscillation frequency and amplitude are studied, and sub-harmonic injection locking is demonstrated to enable phase-based bit encoding. The locked-in phases of coupled MEM relay oscillators are demonstrated to be optimized for minimal energy consumption, which is dependent on the coupling configuration. Finally, the benefits of using MEM relays than other oscillators to implement Ising machines are summarized.

4.2 DC-Driven MEM Relay Oscillation

Figure 4.5 shows a scanning electron micrograph (SEM) image of a fabricated MEM relay, along with corresponding schematic cross-sectional views. The relay comprises a movable body electrode suspended by four folded-flexure beams over a fixed gate electrode, and two pairs of source/drain electrodes. The fixed drain electrodes are co-planar with the gate electrode. Each source electrode extends underneath the body electrode and is attached to it via an insulating dielectric layer. In the OFF state, an air gap physically separates each source electrode from its underlying drain electrode, so that no current (I_{DS}) flows. In the ON state, the movable body is actuated downward by electrostatic force such that each source electrode comes into contact with its underlying drain electrode to allow current to flow if there is a voltage difference (i.e., if $V_{DS} \neq 0$ V). The dimpled regions of source-drain contact are defined by lithographic patterning of a first sacrificial layer prior to the deposition of a second sacrificial layer.

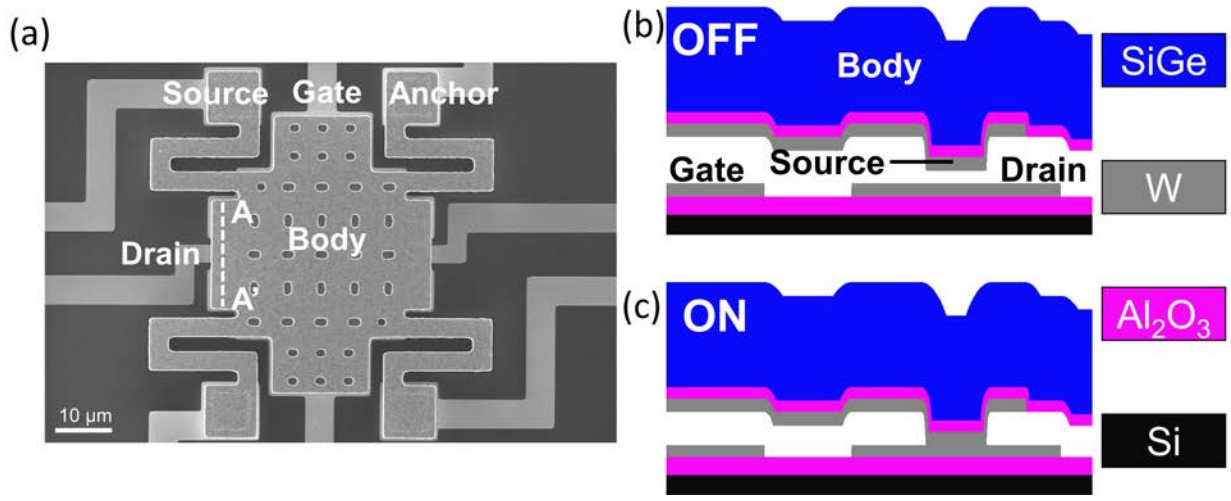


Figure 4.5: (a). Plan-view SEM image of a MEM relay, and cross-sectional views along the A-A' cutline: (b) OFF state (c) ON state.

The MEM relays were fabricated using conventional planar processing techniques with a maximum substrate temperature of 410 °C so as to be suitable for monolithic integration with CMOS circuitry, as described in Chapter 2.2 with more details [66]. The insulating dielectric layers are formed of Al_2O_3 deposited by atomic layer deposition (ALD) at 300 °C. The gate and source/drain conducting electrodes are formed of DC-sputtered tungsten (W), while the structural (body electrode) layer is formed of boron-doped polycrystalline $Si_{0.4}Ge_{0.6}$ deposited via low pressure chemical vapor deposition (LPCVD) at 410 °C. The sacrificial material used was low-temperature-deposited silicon dioxide (LTO) deposited at

400 °C using O_2 and SiH_4 as precursor gases. Vapor HF was used to selectively remove the LTO to "release" the movable structure while avoiding capillary-force-induced stiction.

Figure 4.6 shows the relay operation circuit and measured I_{DS} vs.-V_{GB} characteristics. To turn ON the relay, a voltage is applied to the gate electrode, inducing an electrostatic force that actuates the body electrode downward. The relay current increases abruptly when the gate voltage reaches the turn-ON voltage (V_{ON}) at which the source electrodes come into contact with their underlying drain electrodes. (The ON-state current is artificially limited to 1 μA to avoid contact welding due to Joule heating.) V_{ON} is defined as the turn-ON voltage when the drain voltage is close to 0 V. To turn OFF the relay, the gate voltage is reduced so that the spring restoring force of the deformed suspension beams overcomes the electrostatic force plus contact adhesive forces to actuate the body electrode upward, breaking contact between source and drain electrodes.

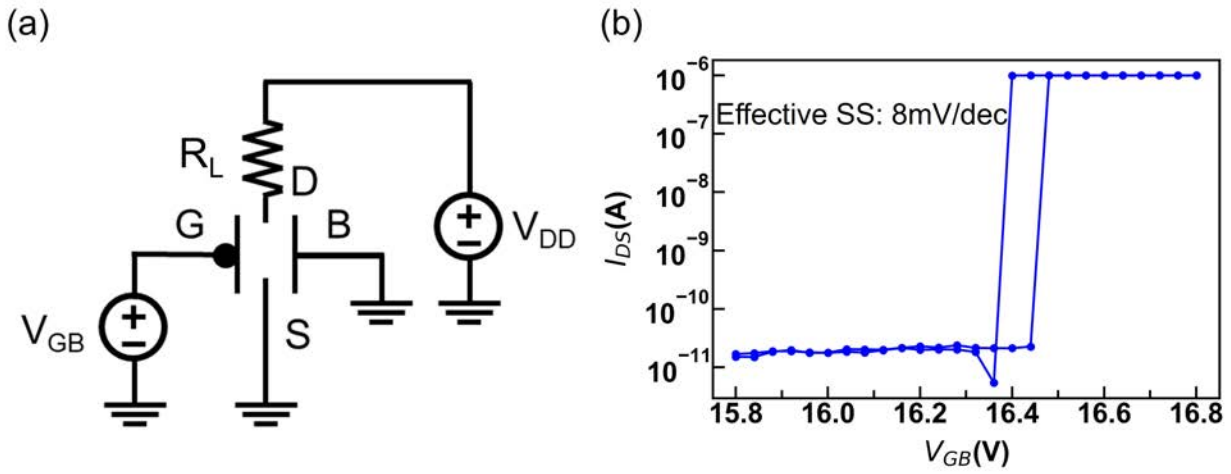


Figure 4.6: (a) MEM relay operation circuit diagram. Here, R_L is used to set the current compliance. (b) Typical measured relay I_{DS}-V_{GB} characteristic. It is worthwhile to note here that the effective subthreshold swing is only 8 mV/dec.

A four-terminal MEM relay can be made to oscillate between ON and OFF states with only DC voltages applied, as follows:

1. A voltage slightly less than V_{ON} is applied to the gate.
2. A voltage V_{DD} is applied to the drain electrode through a load resistor to induce additional electrostatic force (in the contact dimple region between the drain and source electrodes) to turn ON the device.

3. After the drain and source electrodes come into contact, their electrostatic potentials equilibrate so that the electrostatic force between them disappears, causing the relay to turn OFF.

4. When the drain electrode is separated from the source electrode, the drain voltage charges back up toward V_{DD}, inducing electrostatic force once again to turn ON the relay and discharge the drain voltage.

5. Thus, the drain voltage oscillates as the relay turns ON and OFF repeatedly.

With the gate electrode biased at a voltage slightly smaller than V_{ON}, the relay starts to oscillate when the drain voltage (connected via a load resistor to the power supply V_{DD}) is sufficiently large, as shown in Figure 4.7 (a). The drain voltage oscillates at approximately 1 MHz, which is close to the fundamental resonant frequency (ω_o) of the movable electrode calculated by Equation 4.2. The parameters used for the resonant frequency are listed in Table 4.1. Note that here the effective stiffness, k_{eff}, is calculated using experimental results for fabricated relays and Equation 1.8. Figure 4.7 (b) indicates that the oscillation frequency is stable over many cycles.

$$\omega_o = \frac{1}{2\pi}\sqrt{\frac{k_{eff}}{m}} \tag{4.2}$$

Table 4.1: Design parameters of a MEM relay for resonant frequency (ω_o) calculation

Parameter	Value	Unit
Effective stiffness, k_{eff}	540	N/m
Density, ρ [119]	4126	kg/m^3
Actuation Area, A [46]	1062	μm^2
Poly $Si_{0.4}Ge_{0.6}$ thickness, H	1.9	μm

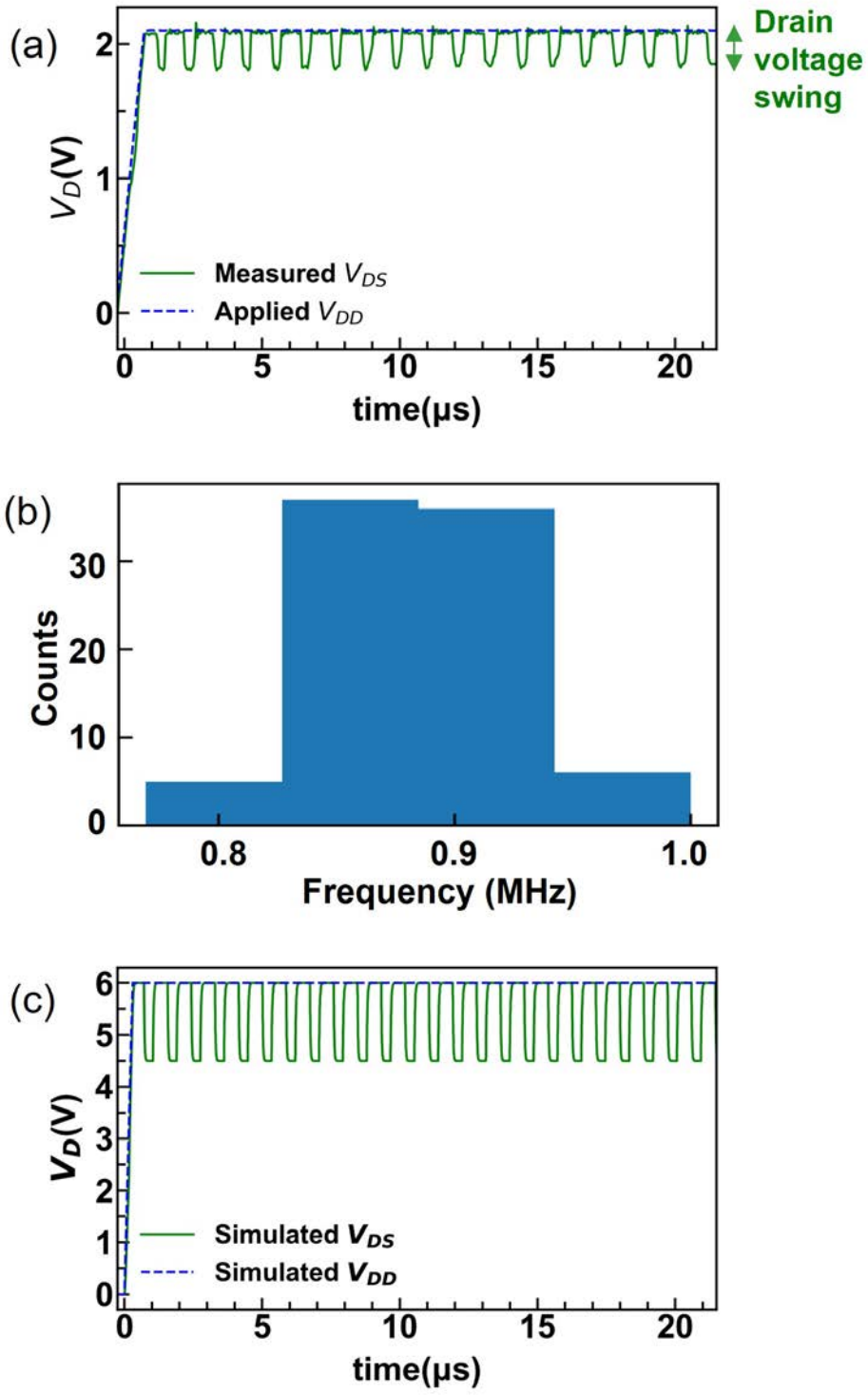


Figure 4.7: DC-bias-driven MEM relay oscillation: (a) measured voltage waveforms with applied DC voltages of $V_{GB} = V_{ON} - 0.5$ V and $V_{DD} = 2.1$ V; (b) relay oscillation frequency distribution over 100 cycles; (c) simulated MEM relay oscillation behavior for $V_{GB} = V_{ON} - 1.8$ V.

To facilitate the study of coupled MEM relay oscillators, Coventor MEMS+ [120] finite element method simulation software was used to model the MEM relay. Figure 4.7 (c) shows simulated relay oscillation behavior for constant applied V_{GB} and V_{DD}. It should be noted that this model is not an exact replica of the experimental device; it comprises a stiffer structure, which results in larger V_{ON} and higher resonant frequency. The drain voltage swing is defined by the difference between the highest and the lowest drain voltages during oscillatory operation.

In order for a DC-driven MEM relay oscillator to be used as a spin in an Ising machine, its oscillatory behavior must be influenced by a perturbing SHIL voltage signal. Therefore, the dependencies of MEM relay oscillation frequency and voltage swing on the applied DC voltages were investigated. Figure 4.8 shows how the oscillation frequency depends on the gate voltage V_G and drain supply voltage V_{DD}. The relay oscillation frequency increases with gate voltage at a rate of approximately +60 kHz/V. This is because the source and drain electrodes are brought closer to each other in the OFF state when V_{GB} increases to be closer to V_{ON}, reducing the distance of oscillatory motion, so that the relay turns ON more quickly when additional electrostatic force is induced by V_D.

The different curves in Figure 4.8 correspond to different values of V_{DD}, showing stronger and opposite dependence of the oscillation frequency on V_{DD} (-250 kHz/V). The larger the attractive electrostatic force between the source and drain electrodes, the greater the contact adhesive force and therefore the longer it takes for the relay to turn OFF.

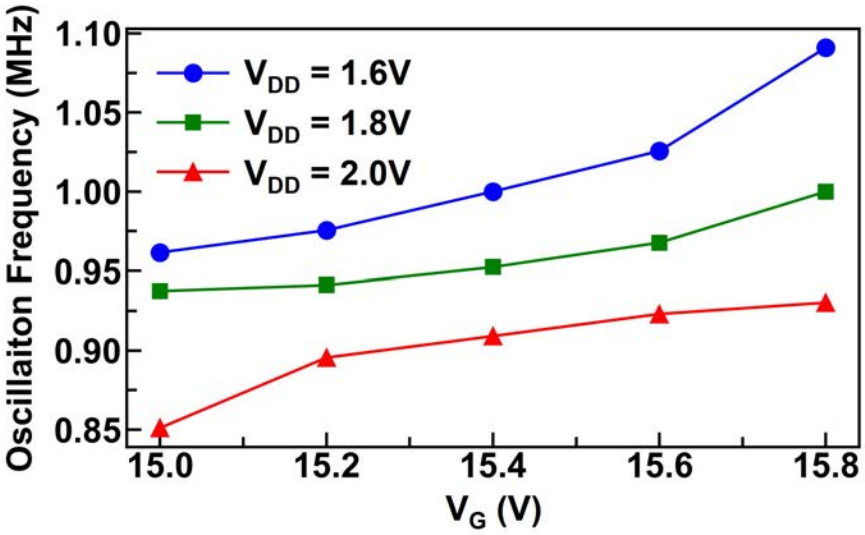


Figure 4.8: Relay oscillation frequency dependence on V_G for different values of V_{DD}.

As V_{GB} increases, the drain voltage swing required to turn OFF the relay increases; this is because the electrostatic force induced by V_D must decrease to a lower level in order to cause the relay to turn OFF when V_{GB} is larger. Measured data presented in Figure 4.9 confirm that the drain voltage swing increases with V_{GB}, at a rate $\sim$ 200 mV/V.

The different curves in Figure 4.9 correspond to different values of V_{DD}, showing similar dependence of the drain voltage swing on V_{DD}, at $\sim$ 200 mV/V). The greater the contact adhesive force, the lower the contact resistance R_{ON} and hence the lower value of V_D reached when the relay is ON, due to the voltage-divider effect (cf. Figure 4.6 (a)).

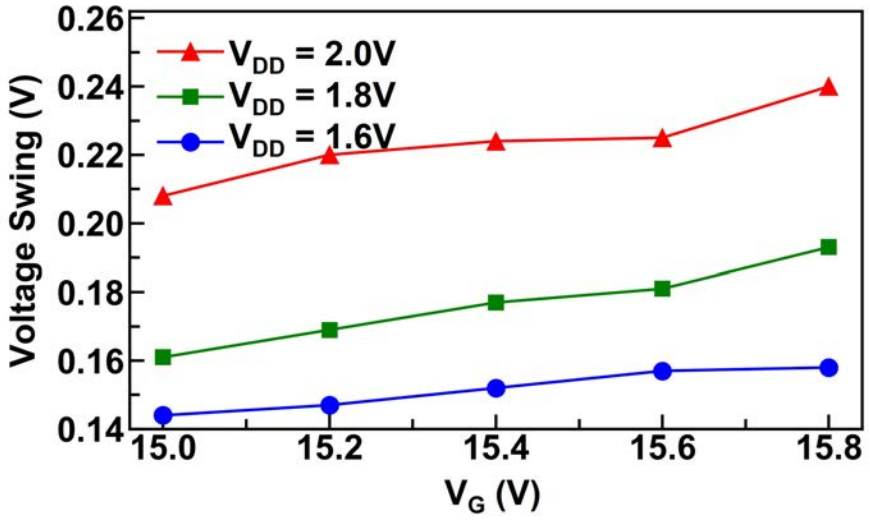


Figure 4.9: Relay oscillation drain voltage swing dependence on V_G for different values of V_{DD}.

Simulated MEM relay oscillation frequency and drain voltage swing dependencies on applied DC bias voltages showed the same trends as experimentally observed (as described above).

4.3 Demonstration of Relay SHIL Behavior

The voltage-dependent self-oscillating behavior of a MEM relay makes it possible to adjust the phase of oscillation by coupling the gate or body and the drain to other voltage signals. Specifically, a sub-harmonic injection locking (SHIL) signal can be used to cause it to settle into one of two phase states [118, 121]. In this section, a SHIL "sync" signal with a frequency approximately twice that of the relay self-oscillation frequency is superimposed on

V_{GB} through the body electrode, as shown in Figure 4.10, so that the drain voltage (V_D) locks into one of two phases with this synchronization signal.

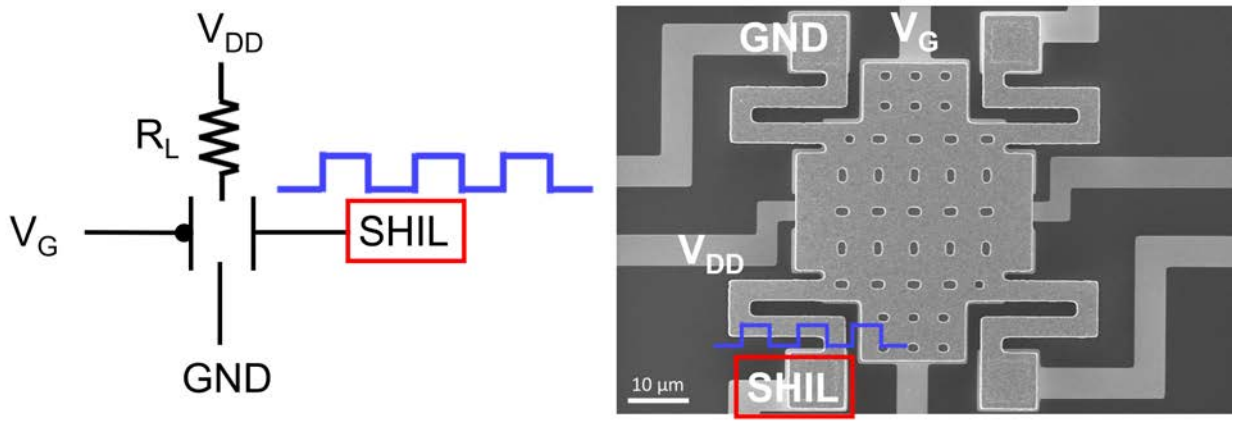


Figure 4.10: A Sub-Harmonic Injection Locking (SHIL) signal is applied via the body electrode of a MEM relay.

Shown in Figure 4.11 (a) are simulated voltage waveforms showing how the oscillation of V_D locks into phase with that of a 1 V, 2.3 MHz SHIL signal within 40 oscillation cycles. The upper blue waveform is the SHIL perturbation signal, and the lower red waveform is the resulting V_D waveform. Figure 4.11 (b) shows how the relay oscillation frequency changes over time after the SHIL signal is applied. It shows that the frequency stabilizes after about 40 μs.

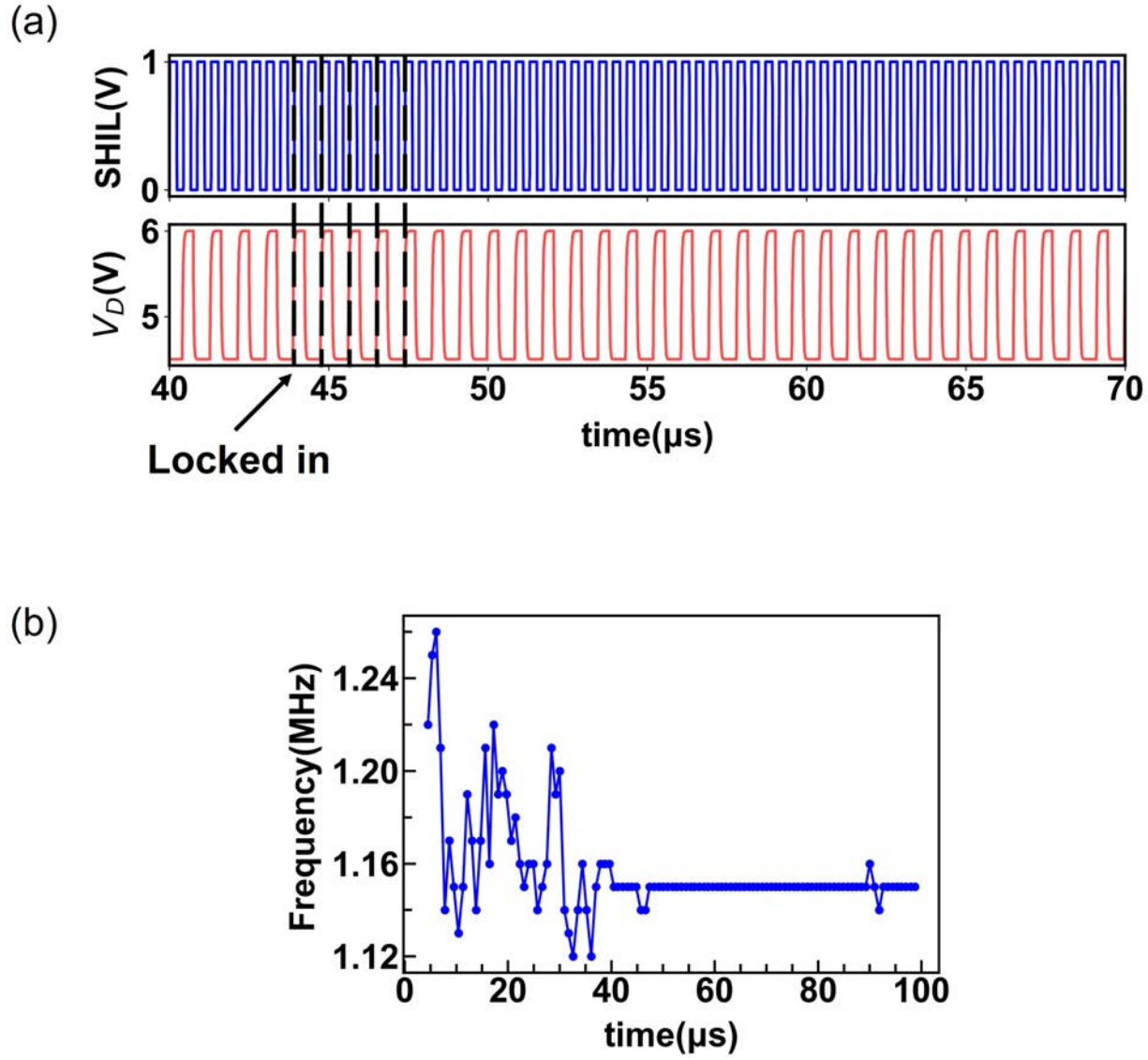


Figure 4.11: MEM relay oscillation simulation results: (a) simulated voltage waveforms showing phase lock with a 1 V, 2.3 MHz SHIL signal within approximately 40 cycles, and (b) oscillation frequency vs. time, showing frequency stabilization after approximately 40 μs.

Experimental SHIL results are shown in Figure 4.12. The sync SHIL signal is applied to the body electrodes of two different MEM relays. Their V_D responses are plotted in red and green curves, respectively. Figure 4.12 (a) shows that 0-25 μs after the DC bias voltages are applied, the two relays are oscillating independently and are not synchronized with the

SHIL signal. Later, 75-100 μs after start of oscillation as shown in Figure 4.12 (b), the two relays are oscillating at the same frequency but with 180° phase difference; both oscillations are locked in with the perturbation SHIL signal.

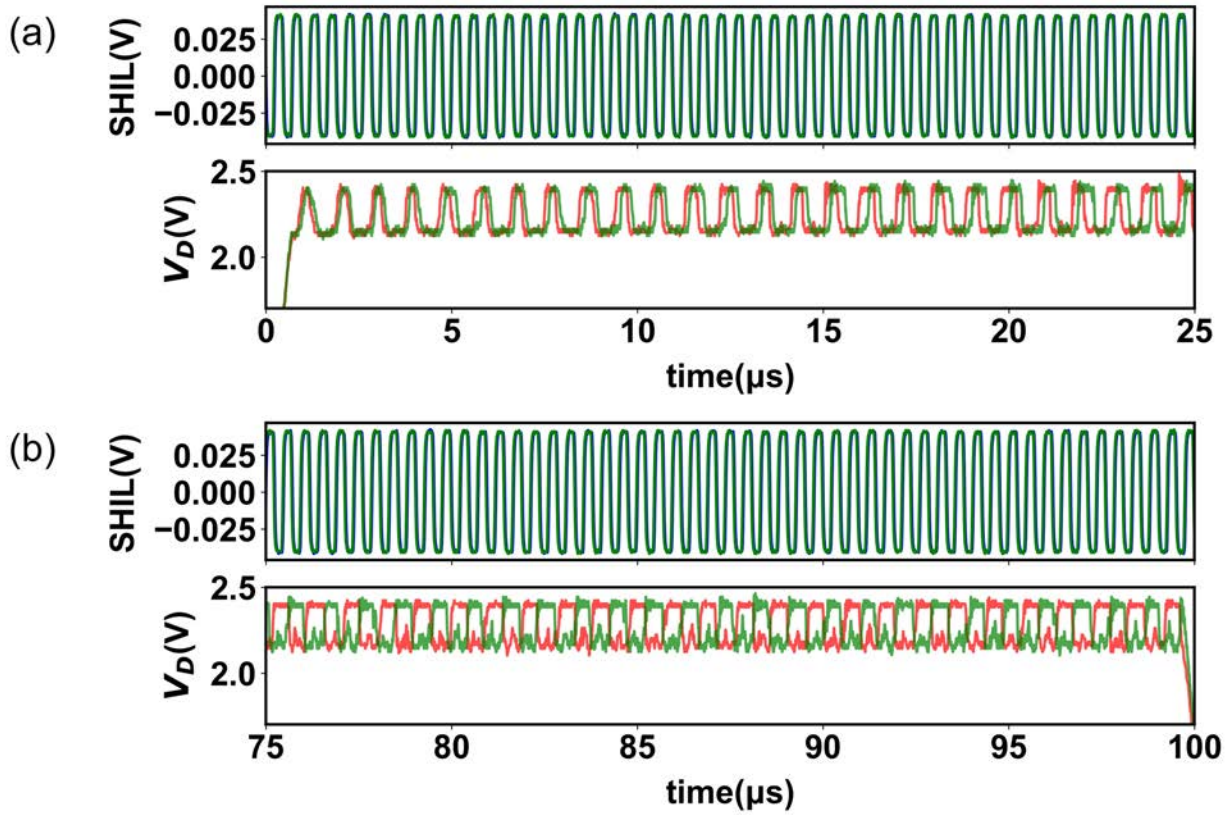


Figure 4.12: Experimental SHIL results. The perturbation 60 mV peak-to-peak SHIL signals applied to the two MEM relays are synchronized. (a) Initial independent oscillation of the two MEM relays. (The V_D responses of the two MEM relays are not locked in with their respective SHIL signals.) (b) 75-100 μs after start-up, oscillations locked in with the SHIL signals are observed, with 180° phase difference.

4.4 Coupling of MEM Relay Oscillators

Figure 4.13 is a circuit diagram for relays coupled in a parallel configuration; that is, the coupling coefficients between their sources and their drains are positive. To demonstrate SHIL for minimizing the energy dissipation of this relay oscillator network, supply signals V_{DD} are applied to each relay, DC bias voltages V_{G1} and V_{G2} are applied to the gate electrodes, and a common SHIL signal is applied to the body electrodes. The two relays are turned ON at staggered times so that they can oscillate initially with random relative phases. In

this circuit, the use of both "pull-up" (PU) and "pull-down" (PD) load resistors ensures low current flow, which is desirable for low power consumption. It should be noted that the electrical (RC) delay should be smaller than the mechanical switching delay of the relay to ensure stable oscillation.

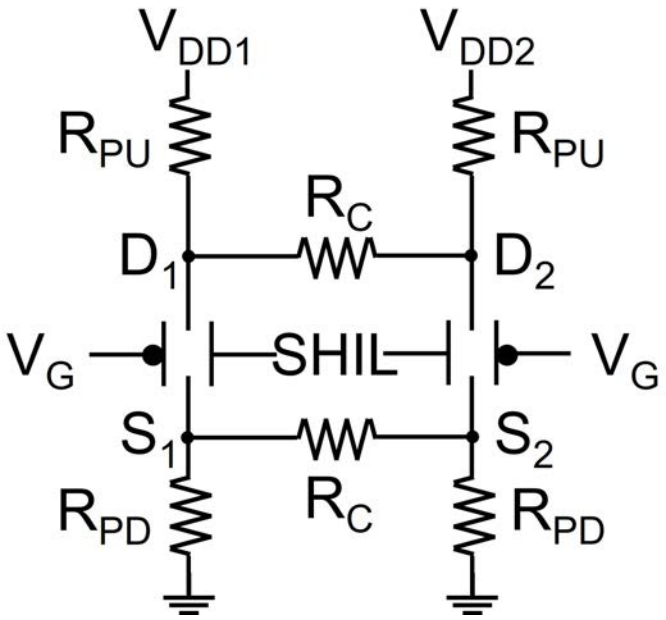


Figure 4.13: Circuit diagram for two relays coupled together in a parallel configuration.

The simulated voltage waveforms in Figure 4.14 show how the relay drain voltage oscillations lock into phase with each other after the devices are turned ON in sequence while a SHIL signal is applied to their body electrodes. The blue curve is V_{D1} (the V_D response of relay 1) and the red waveform is V_{D2} (the V_D response of relay 2). It can be seen that, after several cycles, the two relays oscillate with the same phase.

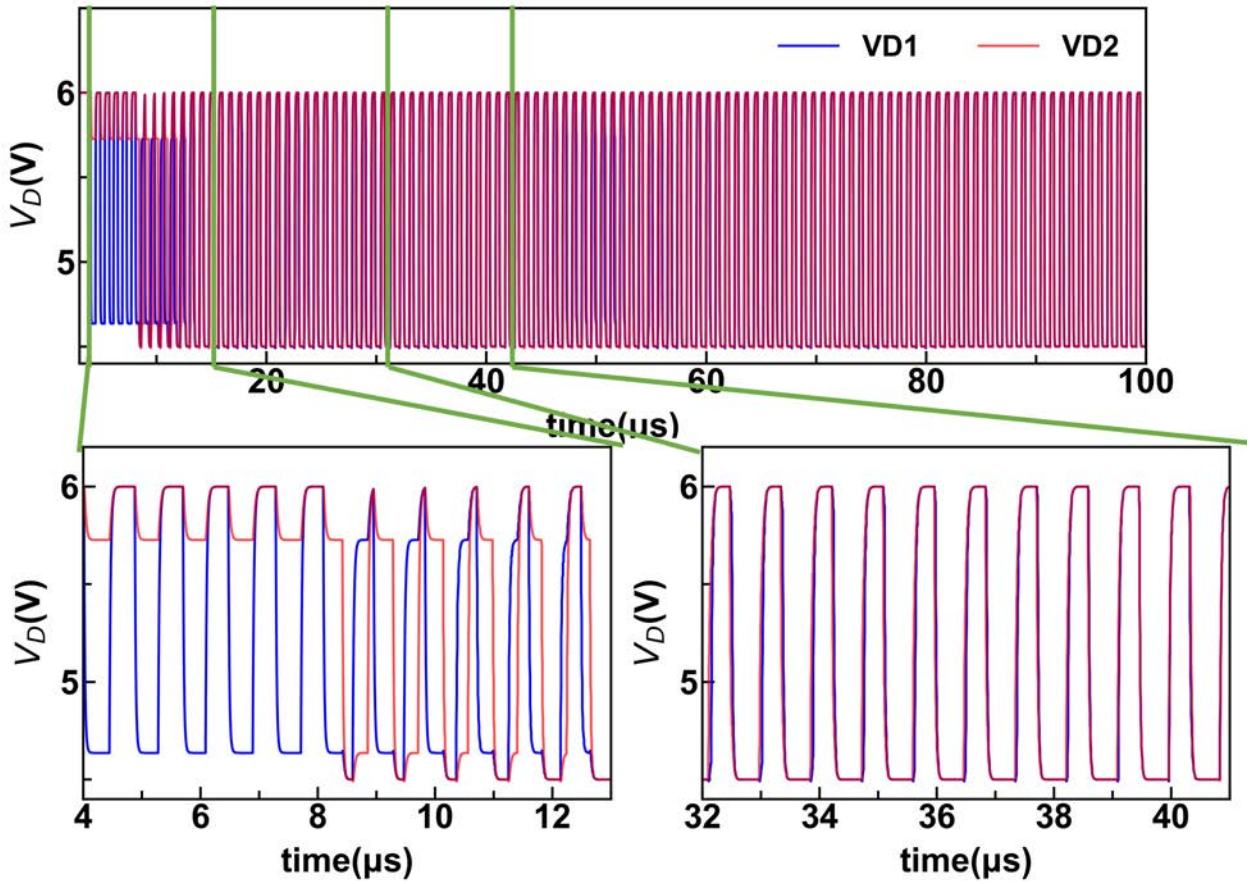


Figure 4.14: Simulated voltage waveforms of relay oscillators coupled together in a parallel configuration.

Figure 4.15 is a circuit diagram for relays coupled in an anti-parallel configuration; that is, the coupling coefficients between their sources and their drains are negative. Again a DC bias voltage V_{DD} is applied to each relay, DC bias voltages V_{G1} and V_{G2} are applied to the gate electrodes, and a common SHIL signal is applied to the body electrodes. The two relays are turned ON at staggered times so that they oscillate initially with random relative phases.

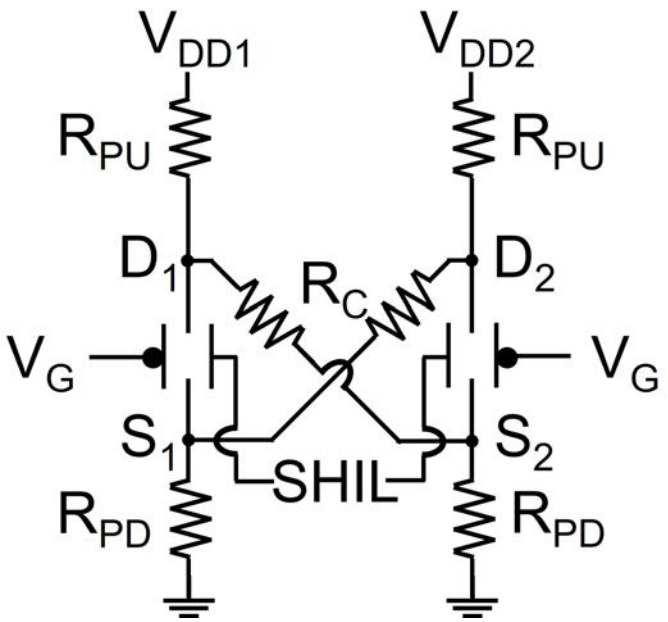


Figure 4.15: Circuit diagram for two relays coupled together in an anti-parallel configuration.

Similarly as before, shown in Figure 4.16 are simulated voltage waveforms showing how the relay drain voltage oscillations lock out of phase with each other after they are turned ON in sequence while a SHIL signal is applied to their body electrodes, to minimize the total energy dissipation.

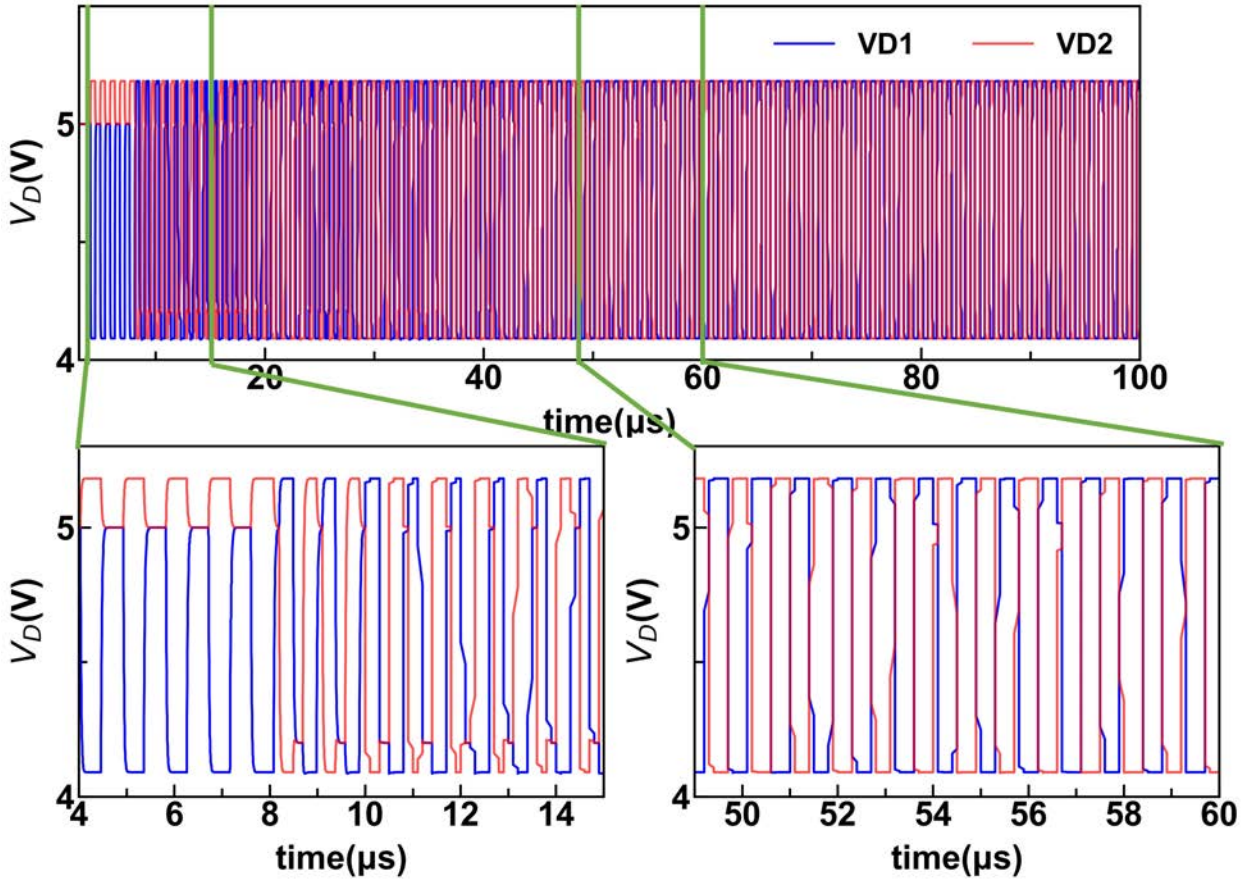


Figure 4.16: Simulated voltage waveforms of relay oscillators coupled together in an anti-parallel configuration.

Figure 4.17 shows experimental results for two relays coupled together in a parallel configuration (cf. Figure 4.13). The experiment was performed with the relays in a Lakeshore TTPX cryogenic vacuum probe station, at $\sim$ 5 μTorr and at room temperature. Since this probe station only has 6 probes for measurement, the body electrodes of the two relays were connected by wire-bonding, and the gate electrodes were also connected by wire-bonding. The experimental results indicate that, even though the two relays initially oscillate at different frequencies and phases, with a 1 V, 2 MHz SHIL signal applied, after approximately 10 cycles, the two relays start to couple in phase, and synchronicity is maintained as long as the SHIL signal does not change.

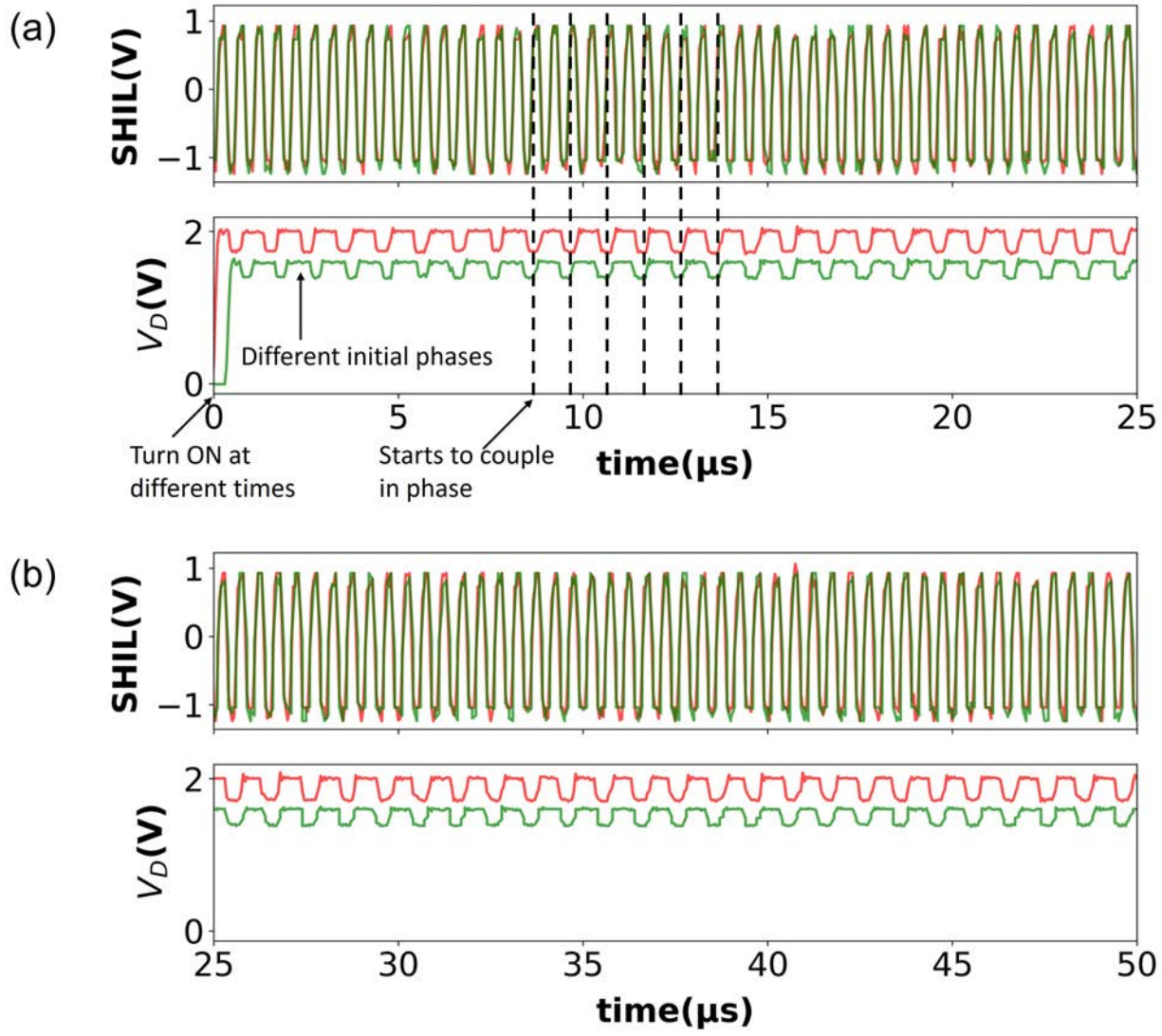


Figure 4.17: Experimental parallel-coupled relay oscillation voltage waveforms: (a) 0 - 25 μs, and (b) 25 - 50 μs after application of DC voltage signals. The red and green curves correspond to each of the two different relay oscillators.

To implement a larger Ising machine, an additional relay oscillator (with PU and PD resistors) would be added for each node, and coupling elements would be added to connect it with the other oscillators.

4.5 Discussion

Endurance

From previous studies [91, 122], the hot-switching endurance of a tungsten-contact MEM relay increases exponentially with decreasing contact voltage (that is, the source-drain voltage difference) and is projected to exceed 10^{16} cycles for contact voltage below 1 V. Therefore, for tungsten-contact MEM relay operation as an oscillator with an oscillation frequency of approximately 1 MHz, endurance is expected to exceed 300 years.

Size of the Relay Oscillators

Vertically oriented nano-electro-mechanical (NEM) switches can be implemented utilizing standard interconnect layers formed in the back-end-of-line (BEOL) steps of a conventional CMOS fabrication process, to achieve smaller footprint (chip layout area) and monolithic integration with CMOS integrated circuits [43, 44, 123]. The working mechanism of vertical NEM switches is similar to that of the MEM relays discussed above in Section 4.2, so vertical NEM switches can also be used as non-linear oscillators, in principle. The footprint of vertical BEOL NEM switches scales with the Minimum Metal Pitch (MMP) of the fabrication process. Vertical BEOL NEM switches have been successfully fabricated using a standard 16 nm-generation CMOS manufacturing process by TSMC [44]. In the future, BEOL NEM switch oscillators can be scaled down even further.

Speed of Calculation

From the results in Section 4.3 and Section 4.4, it takes 10 to 50 oscillation cycles for a two-relay MEM oscillator system to reach its minimum energy state. Since relay oscillation frequency scales up while the relay switching voltage scales down with miniaturization (cf. Equation 4.2), the time and energy required to reach the solution (minimum energy state) can be expected to improve dramatically with relay scaling.

As the size of a NP problem increases, traditional computing architectures require geometrically increasing computing time [50, 124]. In contrast, the Ising machine architecture is expected to require at most a proportionately larger number of oscillation cycles [112, 125].

Other Advantages of Relays as Oscillators

Compared with other oscillators, relay oscillators have unique benefits. First, they can be fabricated monolithically with CMOS circuitry [66]. Also, they can work reliably across a wide temperature range and also endure irradiation. This is especially advantageous for edge computing devices (in the Internet of Things), which must work dependably under harsher environmental circumstances than cloud computing devices (in data centers). In previous

work, MEM relay integrated circuits (2:1 MUX, OR, and inverter) were proven to function properly at temperatures down to 77 K and up to 400 K with V_{DD} as low as 25 mV [42,66]. Besides, MEM relays were demonstrated to function well at 4 K with sub-10 mV hysteresis voltage in Chapter 2.

Additionally, as mentioned above, relays can be scaled down to relatively small size. CMOS oscillators can also be used to implement Ising machines [58, 116, 118], but they require several inverters (each comprising two transistors) and hence would consume more chip area than a single BEOL NEM relay oscillator. Also, the power consumption of a NEM relay [40, 126] can be expected to be smaller that that of a CMOS ring oscillator.

4.6 Summary

In this chapter, MEM relays are experimentally demonstrated to be capable of being operated as DC-voltage-driven non-linear oscillators. The applied voltages can impact the oscillation frequency and amplitude; therefore, sub-harmonic injection locking (SHIL) of MEM relay oscillation is possible and is successfully demonstrated. Coupling-dependent relay oscillation phases are also verified via simulations and experiments. Adequate endurance, fast computing speed, scalable device design, wide-range operating temperature range, and compatibility with CMOS process technology make relay-based Ising machines a promising approach for solving complex combinatorial optimization problems efficiently.

Chapter 5

Conclusions and Future Work

5.1 Contributions of This Work

Moore's law sets the pace for increasing the number of CMOS transistors on a chip [2, 3] which provides for improvements in computation speed and energy efficiency. Over the last five decades, the industry has successfully followed Moore's law. As fundamental limits of transistor scaling approach, alternative devices and computing chip architectures must be developed to improve computational performance. This dissertation aims to explore novel applications of micro-electro-mechanical (MEM) relays for beyond-von-Neumann computing chip architectures.

MEM relays have the potential to be superior to CMOS transistors for interfacing with quantum computers, because they can be operated with much lower switching voltage and have zero OFF-state leakage current. This lower power consumption makes it easier to maintain the milli-Kelvin temperature environment required by the quantum computer, while reducing the number of interconnections between the electronic controller and qubits. In Chapter 2, the temperature dependence of several relay properties has been studied; these include the sheet resistances (R_S) of the contact material and of the structural material, turn-ON voltage (V_{ON}), self-oscillation frequency, switching hysteresis voltage (V_H), ON-state resistance (R_{ON}) and stability, and turn-ON delay. Moreover, sub-25 mV voltage operation of relay digital ICs is demonstrated at 77 K, and sub-10 mV relay-based inverter circuits are demonstrated at 4 K. These results indicate that MEM relays are promising for implementing ultra-low-power cryogenic digital interface circuits for quantum computing.

In Chapter 3 superconductive contacting electrode materials have been considered for cryogenic MEM relays, for electrical performance (RC delay) improvement. Niobium (Nb) is a promising candidate because its superconducting transition temperature is 9.29 K, and it satisfies the electrical and mechanical requirements for a relay contact material. The integrated process flow for fabricating Nb-contact MEM relays is described. Then the electrical

characteristics of Nb-contact MEM relays are measured, for different relay contact designs, and key performance characteristics of Nb-contact relays are compared against those of W-contact relays.

The Ising model is a promising non-von-Neumann computing architecture for efficiently solving large combinatorial optimization problems, by mapping the problems into Ising Hamiltonians of physical systems which naturally reach their ground state. Nonlinear self-sustaining oscillators have been proven to work as artificial Ising spins [58]. In Chapter 4, MEM relays are designed to oscillate between ON and OFF states with only DC biases applied. The gate voltage and drain voltage impacts on the oscillation frequency and drain voltage swing have been studied and analyzed, indicating the feasibility of sub-harmonic injection locking (SHIL) and coupled relay interaction. SHIL is experimentally demonstrated to lock MEM relay oscillation into one of two phase states (with 180° phase difference). Coupled relay oscillation is also demonstrated through both simulation and experiment, indicating that networked MEM relay oscillators are appealing for building Ising machines that have low power consumption. Finally, the benefits of MEM relay-based Ising machines are discussed in terms of endurance, size (cost), and speed.

5.2 Suggestions for Future Work

While this dissertation has explored new applications for MEM relays, there is still room for further improvement and exploration:

Milli-Kelvin Relay Operation. Demonstration of MEM relay digital circuits (MUX, inverters, etc.) at milli-Kevin temperatures can be done in the future with sub-10 mV or even lower voltages, for cryogenic computing applications. Additionally, superconducting contact material integration can be further investigated. For example, additional protection methods can be researched to maintain the superconductivity of the niobium contacts; alternative sacrificial materials and the associated release-etch steps can be investigated to further reduce the relay fabrication process temperature when the contact materials are exposed; or a more stable metallic material with a high superconducting transition temperature can be used to form the contacting electrodes.

Contact Exploration with Machine Learning Algorithms. More stable contact materials for MEM relays can be explored in the future, both for room temperature and cryogenic temperature applications. Machine learning is one of the most interesting new methods in the material science research toolkit in recent years. With the increasing availability of experimental and simulated databases for material science such as the Materials Project [127–129], Crystallography Open Database [130–132], and Materials Data Facility [133–135], the ability of machine learning-assisted algorithms and frameworks for novel material design [136–138] and material property prediction [139–142] has been significantly improved. Therefore, the material databases and machine learning algorithms might be able to expand

the contact material selection pool, as previous research mainly focused on refractory metals, but there are also a large number of alloys and ceramic materials available that might be able to satisfy all the requirements for relay contacting electrode materials.

Oscillation Analytical Model and Vertical BEOL NEM Relay Oscillators. Further work can also be done to create an accurate analytical model for relay oscillations, in order to better understand the benefit of device scaling for relay oscillators, as well as to systematically study the influence of different relay designs (for example, dual-bridge contact, dual-direct contact, and single-direct contact designs [46]) on oscillation behavior. Moreover, the oscillation behavior of vertical back-end-of-line (BEOL) Nano-Electro-Mechanical (NEM) switches [143] can be studied, for compact implementation of relay oscillator based Ising machines.

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