Hybrid Switched-Capacitor Converters for High-Performance Power Conversions

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by

Wen Chuen Liu

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Abstract

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High-performance power conversions are essential in many applications, especially in the fast-growing computing industries as well as the wireless sensor networks. A common example in mobile devices is the dc-dc converter that converts the energy from a 4 V Li-ion battery to 1 V CPU / GPU chips, where efficiency and form factor are of the most important concerns. Meanwhile, the source voltage increases with the processed power to reduce wire conduction loss, e.g. 48 V DC grid for data centers. In particular, a hybrid approach has shown great potential in achieving high efficiency, high power density and high conversion ratio, due to its efficient passives and switch utilization compared to the conventional buck and switched capacitor (SC) converters.

In this work, the development of a hybrid or resonant SC (ReSC) converter, along with its soft-charging feature, is illustrated to address the fundamental limits of conventional SC converters and efficiently utilize the high energy density of capacitors. On top of that, various SC topologies are synthesized from a single unit cell for obtaining higher conversion ratios. While several optimization approaches for switch utilizations have been established in recent studies, they mainly focus on the ideal switch model but with the absence of practical considerations. Therefore, a more comprehensive design and comparison framework for commercially available switches and passive components with various voltage domains will be elaborated throughout this work, in conjunction with the analysis and experimental results. The proposed framework serves as a selection guideline for topologies, and it is further solidified through various power converters with optimized switch employment, i.e. an on-chip 4-to-1 V Dickson converter and an on-chip three-level boost converter implemented using the custom switch sizing and voltage rating in 65 nm CMOS process; a 48-to-4 V two-stage ReSC and a 4-to-1 bi-lateral energy resonant converter (BERC) built using ultra-low on-resistance discrete silicon switches.

One of the most critical challenges for all hybrid SC converters is the flying capacitor balancing issues. Any occurrence of imbalance in the flying capacitor voltage leads to increased

voltage stress on the switching transistors; meanwhile, the inductor current ripple is increased leading to higher conduction loss. An auto-capacitor-compensation pulse frequency modulation (ACC-PFM) controller for three-level converters is proposed to address it by inherent negative feedback between unbalanced voltage and injected charge. The hybrid approach employed in ACC-PFM, i.e. peak current-mode control with constant-off time and valley current-mode with constant-on time, establishes not only a balanced flying capacitor voltage but also a full-range output voltage regulation.

To further improve the efficiency and power density, two main types of floating supplies, i.e. voltage borrowing technique (employ an existing voltage) and bootstrap circuit (generate a new voltage), are introduced, compared and implemented in different situations. It is found that the capacitance density ratio between the transistor gate capacitance and available capacitors determines which type of floating supplies provides a more area-efficient solution. On the other hand, the gate driving of a power MOSFET is investigated. A segmented gate driver with multiple driving strengths is proposed, which is dedicated to reducing the ringing issue by a low-strength driver and maintaining a low conduction loss by a high-strength gate driver after the ringing-sensitive region. Gate driving techniques including floating supplies and segmented gate drivers are also required by other classes of power converters, particularly when dealing with high voltage using low-voltage devices.

Lastly, passive reduction techniques are developed to further enhance the energy utilization of the passive components, along with the quantitative analysis of multiphase interleaving in hybrid SC converters. A novel BERC concept merges the resonant inductors for the multi-stage approach, by simultaneously using voltage- and current-type hybrid SC converters. Both passive reduction techniques not only significantly reduce the converter size, but they are also beneficial for high-current applications since lower inductance with higher saturation current can be employed. Therefore, an excellent high power density can be achieved.

Several on-chip and discrete hardware prototypes for hybrid SC converters have been implemented, measured and showing promising performance in ***efficiency***, ***power density*** and ***conversion ratios*** compared to prior arts, which are suitable for applications ranging from point-of-load (PoL), data center power deliveries and energy harvesting. Meanwhile, the hybrid approach offers a lot more design freedom in optimizing the switches and passives utilization, providing more opportunities in further improvement and research topics for high-performance power converters.

To my family

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Chapter 1

Introduction

Over the past decades, the ever-growing computing industry has been one of the major driving forces for high-performance power conversion. Owing to the high electricity demand in data centers and telecommunication systems, improving their energy efficiency is critical for reduced cost and less environmental impact. This demand has stimulated high-performance power deliveries, such as the intermediate bus architecture (IBA) moving from a 12 V legacy voltage to a higher backplane voltage, ranging from 40 V to 60 V, to reduce the wire conduction losses associated with the source current. On the other side, as Moore's law advances, the voltage of computing loads is lowered for less switching loss, usually below 1 V for the core devices or 3.3 V for I/O devices. As a result, the dc-dc interface between the DC grid and the current-starving loads should sustain high input voltage and high output current together with output regulation capability. This poses challenges to achieve high efficiency and high power density in the conventional dc-dc regulators. Similar situations occur in lithium-ion (Li-ion) battery-powered portable and wearable electronics since they may operate at even lower voltages in near- and sub-threshold operation resulting in voltages down to 0.3-0.5 V [1], [2].

Apart from voltage step-down applications, step-up converters are also essential in many power conversion systems. For instance, in the application of Internet of Things (IoT), power converters with high output voltage and high conversion ratio are demanded to interface between energy harvesters (below 1 V) and lithium-ion batteries (around 3 to $4.2V$) for wireless sensor network (WSN) devices as shown in Fig. 1.1. Applications such as bio-implantable devices [3], high-speed non-volatile low-power memories (e.g. ReRAM [4]) and display drivers also require highly efficient voltage step-up conversion for better performance. Undoubtedly, a low-voltage process technology is favored for these integrated systems, considering its high integration density that offers a lower cost solution; yet, the device rating has become a challenge due to the desired high output voltage in these systems.

Switched-capacitor (SC) converters [5]–[12] appear to be an enticing alternative for the aforementioned applications. The presence of flying capacitors conduces to the voltage stack-up capability in SC, which aids in providing high voltage with low-voltage devices. Moreover, capacitors generally have significantly higher energy density than that of inductors [13], [14],

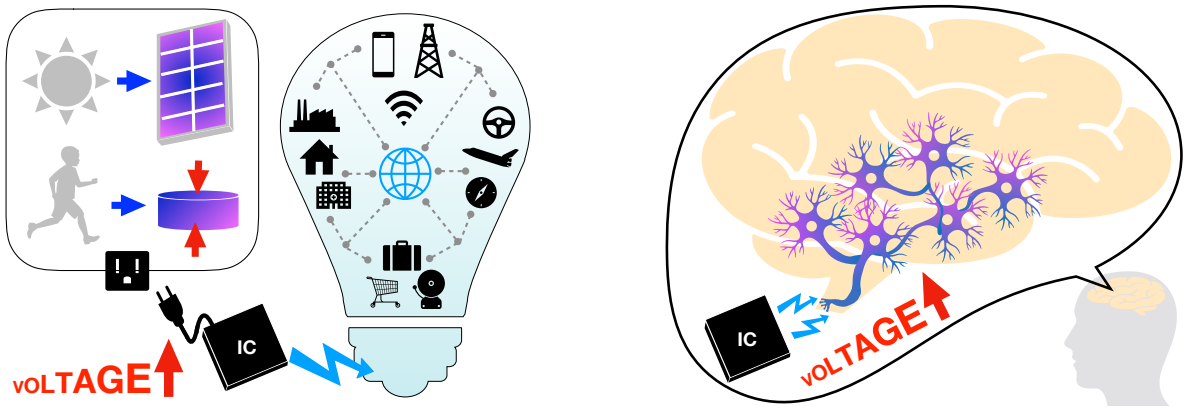


Figure 1.1: Applications that requested high-performance voltage step-up power conversion.

yielding reduced overall size and a path to further integration. However, the relatively low current capability and efficiency across wide conversion ratios have limited their use to primarily low conversion, fixed-ratio applications. Contrarily, conventional magnetic-based converters [4], [15]–[24] are able to sustain high efficiency across wide load ranges, but with the compromise of further integration owing to the large inductor size.

Hybrid or resonant SC converters incorporate the advantages of both capacitor- and magnetic-based converters. This class of converters preserves the ability to employ low-voltage devices, along with passive reduction; thus, achieving high power density. The inductor in hybrid SC mitigates the charge redistribution loss of SC converters (referred to "soft charging", as first identified in [25]), establishing an efficient power conversion across wide conversion ratios. Many prior arts have demonstrated the promising performance of hybrid SCs either in discrete [26]–[37] or on-chip [38]–[53] implementations. The trend shows that the high-level theories are becoming maturer in discrete designs, and the majority of the designs can be found in the 48-to-12 V power conversion [27]–[31] and some efforts are currently moving toward direct point-of-load (PoL) [35]–[37]. Contrary to the top-down voltage design in discrete implementations, researches in power management integrated circuit (IC), which are on the phase transitioning from pure SC and buck converters to hybrid SC converters, are looking for opportunities in extension to high-voltage domains with high performance. This can be seen not only from a whole new dedicated session in ISSCC but also from commercial products by major IC design houses. This work explores the hybrid SC from the perspectives of both discrete and integrated implementations, with an emphasis on efficient integration on power converters and all essential peripheral circuits for high efficiency, high power density and high conversion ratio. Topological efforts are made to evaluate how switches and passives can be efficiently utilized. Also, critical circuit design and techniques are investigated and implemented to maintain high reliability and performance. The dissertation is outlined as follows.

Chapter 2 provides an overview for conventional power converters including low-dropout

(LDO), SC and buck regulators, in terms of their applications and limitations. Chapter 3 then investigates into the charge sharing loss in SC by revisiting the two-capacitor problem, and soft-charging techniques are introduced to turn a pure SC into a hybrid SC with a more efficient energy utilization in the capacitors. Based on the fundamental SC cell, more SC topologies with higher conversion ratios are synthesized in Chapter 4. A metric - output impedance [5], [54] that models conduction loss and part of the switching loss is used to indicate the switch utilization. Combing the output impedance and converter volume, a novel figure of merit (FoM) - output conductance density, is proposed to characterize the tradeoff between efficiency and power density. Higher output conductance density means better switch and passive utilizations, or a higher efficiency with smaller form factor. A comprehensive and comparative framework shows that advantages of each topology depend on the applications and the available devices. Based on the comparison results, Chapter 4 paves the roadmap for the rest of the chapters. For instance, the Dickson topology is the most suitable for chip implementation as illustrated in Chapter 5, while the series-parallel topology is excellent for low-voltage discrete designs in Chapter 7. On the other hand, with moderate switch utilization, the flying-capacitor multilevel topology is employed for its wide-range regulation capability in Chapter 6 and the cascaded topology for its area-efficient conversion ratio extension in Chapter 8.

Chapter 5 demonstrates the high switch utilization of a hybrid Dickson converter [38] together with the highlight on the packaging and small form factor using voltage borrowing technique on floating gate drivers. The core converter is implemented using 65 nm bulk CMOS process, which integrates power MOSFETs, level shifters, gate drivers and digital controller. The wafer-level flip-chipped 4 mm^2 die is co-packaged with 3D stacked passives on a fine-pitch interposer for high power density. A wide and continuous conversion range between 4:1 and 15:1 is achieved from a 3-4.5 V input, with a peak output current of 1.53 A. Peak efficiency is 94.2% and peak power density 0.24 W/mm^2.

Chapter 6 covers flying capacitor balancing issues, which have been one of the most critical challenges for all hybrid SC converters. An auto-capacitor-compensation pulse frequency modulation (ACC-PFM) controller [52], [53], combining peak and valley current-mode controls, is proposed to resolve the issue of unbalanced flying capacitor voltage, as well as to regulate the output voltage. The capacitor balance is further strengthened through a delay-equalized level shifter that generates duty ratios with only sub-ns deviations. The step-up power conversion from the input voltage of $0.3-3.0V$ to the output voltage of $2.4-5.0V$ is demonstrated through a three-level boost converter implemented in a 65 nm CMOS process with 0.28 mm^2 active area. This converter achieves 96.8% peak efficiency and an $83mA$ peak output current, with an $8X$ peak step-up conversion ratio.

Chapter 7 shows the design for a multi-stage approach [26] for very high conversion ratios, with an emphasis on addressing the requirement in data center applications. Each stage can be optimally designed based on their voltage domains and associated available devices, which improves the overall performance. A 48 V-to- 4V two-stage hybrid SC converter, cascading a 2-to-1 resonant SC converter (high-voltage stage, using 40 V switches) and a 6-to-1 hybrid series-parallel SC converter (high-current stage, using 25 V switches), is designed, built and

tested. The hardware prototype achieves 97% peak system efficiency (including gate driver losses) with the use of zero voltage switching (ZVS) control techniques for both stages. A peak current density of 308 A/in^3 or a peak power density of 1154 W/in^3 is achieved. An output conductance density of 1200 S/in^3 at the conversion ratio of 12-to-1, which is even better than that of the state-of-the-art 4-to-1 converter.

Chapter 8 discusses more diverse and potential approaches to increase power density. The focuses are filter capacitance reduction and equivalent inductance enhancement for hybrid SC converters, through multiphase interleaving techniques and bi-lateral energy resonant conversion (BERC). In particular, the proposed BERC concept can easily be validated and demonstrated by a 48-to-12 V converter prototype, which merges the inductors in two adjacent cascaded stages by relocating the output inductor of the second stage to its input. This enables improved passive utilization, yielding a very compact size of 0.184 in^3, along with high efficiency of 98.9% using a zero voltage switching technique designed for BERC. The prototype is tested up to 50 A, thus achieving an excellent power density of 3200 W/in^3.

Finally, the conclusions are given in Chapter 9.

Chapter 2

Fundamentals of Power Converters

A power converter transfers electrical energy from the form supplied by a source to the form required by a load [55]–[57]. Take mobile phone as an example, a dc-dc power converter is required to converter energy from a 4 V Li-ion battery to 1 V CPU and GPU chips. Meanwhile, there are many power quality requirements, and high efficiency is of the most essential ones for any power processing application. Not only the efficiency is related to the electricity cost, but also the unpleasant heat dissipation issue that determines the power density of a converter: higher efficiency means lower power loss, which may enable a more compact converter with smaller size and weight without hitting the thermal limits. Some other applications may require higher conversion ratio and better regulation capability. As shown in Fig. 2.1, achieving these requirement involves the smart use of electronic devices, analog and digital circuit, topology, system feedback control and mechanical packaging, which will be covered to different extent in this dissertation. This chapter provides a brief introduction to the basic electronic elements and their combinations in synthesizing power converters.

2.1 Basic Elements - Passives and Actives

Like any other electronic systems, power converters are built up with passive and active components. The passives primarily include resistors, R, magnetics (including inductors and transformers, but inductors are mainly focused throughout this dissertation), L, and capacitors, C. Fig. 2.2 shows the some combinations featuring low-pass filters in order to cut off high-frequency noise. Their step responses can be analyzed in either frequency or time domain through the following fundamental characteristics:

$$Z_L = j\omega L, \quad v_L = L\frac{di_L}{dt} \tag{2.1a}$$

$$Z_C = \frac{1}{j\omega C}, \quad i_C = C\frac{dv_C}{dt}. \tag{2.1b}$$

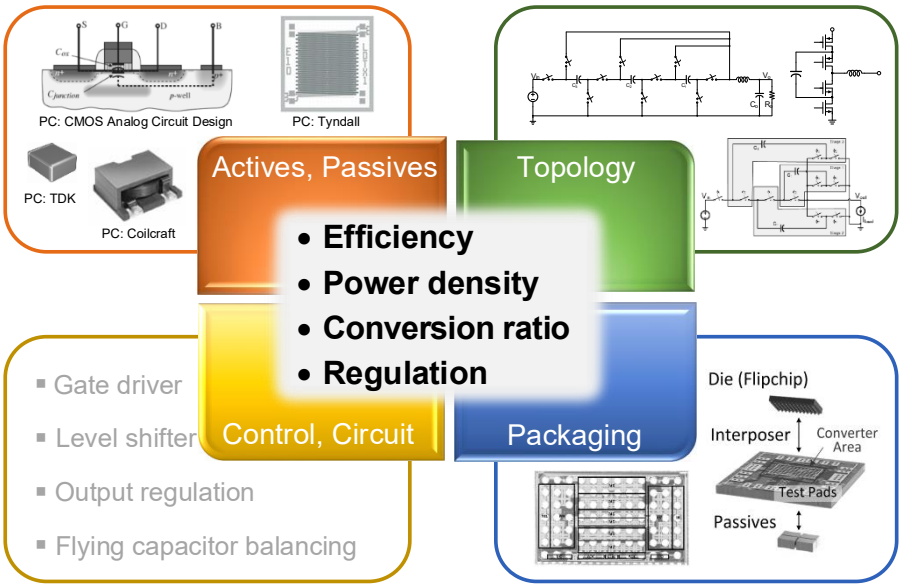
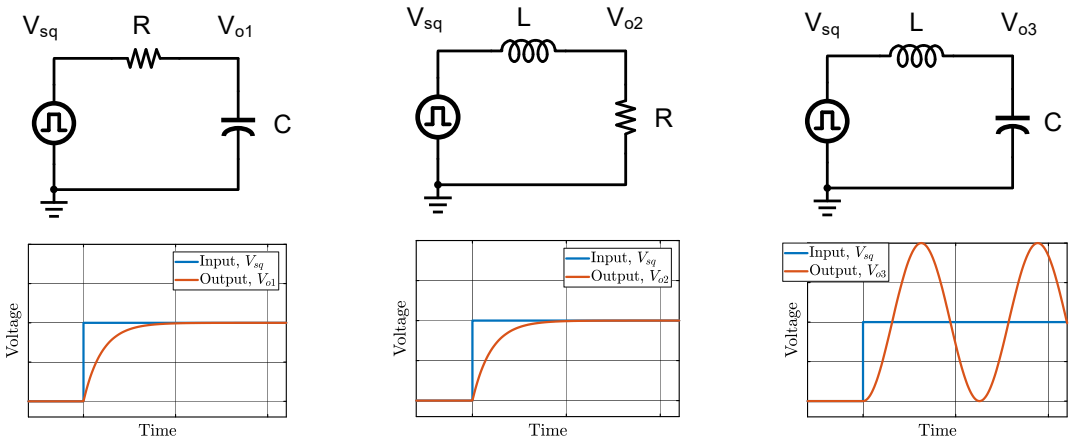


Figure 2.1: Design requirement and framework for power converters.



(a) *RC* circuit (b) *LR* circuit (c) *LC* circuit

Figure 2.2: Step response of various low-pass filters.

For example, in the *RC* circuit, the capacitor impedance, Z_C, is zero at the switching instance due to high-frequency components, leading to low output voltage at V_{o1}; after that, Z_C increases with the DC input, allowing V_{o1} to increase from 0. While in time domain, the capacitor "resists" to have much voltage change, dv_C, with its current, i_C, limited by R, causing a slow rise on output voltage. Similarly, the output voltage, V_{o2}, of the *LR* circuit can be predicted through the duality of voltage and current. Both *RC* and *LR* circuits have the same step response with time constants of *RC* and L/R, respectively. Different from

RC and LR circuits, the LC circuit in Fig. 2.2 (c) shows a resonant frequency of

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}, \tag{2.2}$$

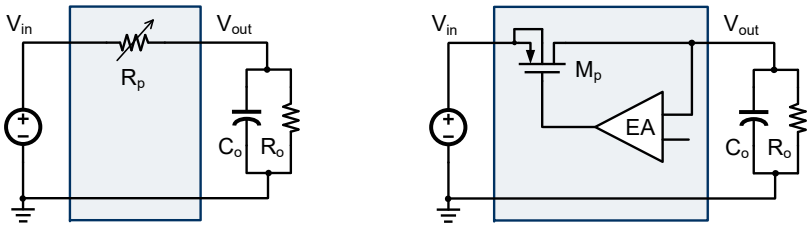
where the mutual "resist" between inductor current and capacitor voltage leads to the oscillation when the circuit is lack of damping resistance. Note the low-pass feature of LC circuit is easier to observe through frequency domain. In practical applications, a load is hooked up at the output of the low pass filters, and active components are added to condition their output voltage.

Active components include switches and diodes, and metal-oxide-semiconductor field-effect transistor (MOSFET) is the most commonly used in the field of power electronics due to its high reliability and cost effectiveness. A MOSFET switch has three useful operational regions: saturation, cut-off and linear (ohmic) regions. In linear regulators, the saturation region with a tunable R_{on} is used. In the switching converter, including magnetic-based and capacitor-based converters, the cut-off and linear (ohmic) regions providing the highest off-resistance, R_{off}, and the least possible on-resistance, R_{on}, respectively, are used. The switches of switching regulators control the energy flow through C and L by replenishing and releasing their energy in a certain rate — switching frequency, f_{sw}. Higher f_{sw} provides lower capacitor voltage (inductor current) ripple, when $f_{sw} \gg \frac{1}{2\pi RC}$ ($f_{sw} \gg \frac{R}{2\pi L}$) in Fig. 2.2 (a) and (b); meanwhile, we can assume the capacitor (inductor) as a voltage (current) source while doing quick qualitative analysis. In the case of Fig. 2.2 (c), the switching period should be much smaller than one-fourth of the resonant period, i.e. $f_{sw} \gg 4f_{res}$ to fulfill the assumptions for voltage or current approximation. While capacitor voltage (inductor current) is assumed relatively constant, the inductor current (capacitor voltage) can simply be linear.

In a power converter, passives are used to store and transfer the energy, and actives control the energy flow. Different configurations of passive and active devices lead to linear regulator, capacitor-based and magnetic-based converters, and a brief overview for these power converter will be discussed in terms of their components, integration level, power losses and conversion ratios.

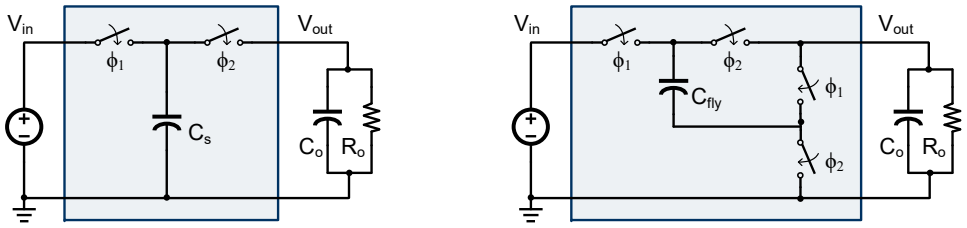
2.2 Linear Regulator, Capacitor- and Magnetic-based Converters

An intuitive way to obtain a specific output voltage is through a resistive divider as shown in Fig. 2.3 (a). By tuning the equivalent resistance, R_p, of the converter, the output voltage can be regulated within a certain allowable load range. The linear regulator or low-dropout (LDO) voltage regulator as shown in Fig. 2.3 (b) demonstrates the idea with the pass transistor resistance tuned by changing the gate-to-source voltage, V_{gs} of M_p. Similarly, switched-capacitor (SC) converters adjust their internal resistance by changing f_{sw}, e.g. the 1:1 SC as shown in Fig. 2.4 (a) has an equivalent resistance of $\frac{1}{f_{sw}C_{\text{fly}}}$. Compared to LDO, SC can



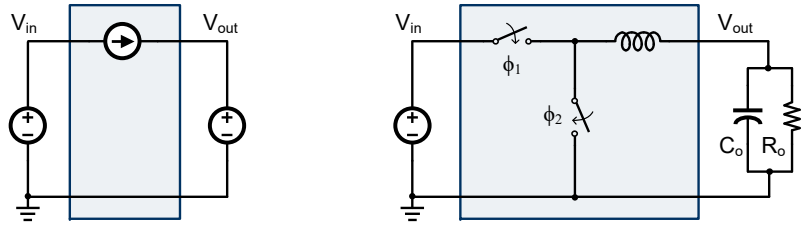
(a) resistive divider (b) linear regulator

Figure 2.3: Operating principle and schematic of a linear regulator.



(a) 1:1 native conversion ratio (b) 2:1 native conversion ratio

Figure 2.4: Schematics of capacitor-based converters.



(a) VIV-energy flow (b) buck converter

Figure 2.5: Operating principle and schematic of a magnetic-based converter.

provide conversion ratios other than 1:1 by adding more switches and capacitors, such as the 2:1 example shown in Fig. 2.4 (b). However, both LDO and SC have the efficiency of

$$\eta = \frac{V_{out}}{V_{in}}, \tag{2.3}$$

which drops significantly when their output voltage deviates too much from input voltage, due to their dissipative nature. Note the 2:1 SC has the same efficiency profile, except V_{in} is replaced by $\frac{V_{in}}{2}$ in (2.3).

To improve the efficiency for wide conversion ratio, the VIV-energy flow as shown in Fig. 2.5 (a) can be used, which ideally does not incur any intrinsic power loss during the

Table 2.1: Comparison between conventional power converters.

	Linear Regulator, LDO	**Capacitor-based Converter, SC**	**Magnetic-based Converter**
Regulation speed	High	Medium	Low
Integration level	High	Medium	Low
Efficiency for wide CRs	Low	Low	High
Step-up possibility	No	Yes	Yes
Current rating	Medium (5 mA to 7.5 A)	Low (10 mA to 300 mA)	High (50 mA to 40 A)

voltage conversion. In practical circuit, the current source is implemented by an inductor, and switches are added to control the voltage across the inductor. Fig. 2.5 (a) shows the most basic magnetic-based converter — buck converter. The switching signals, ϕ_1 and ϕ_2, of a buck converter are operated in a complementary way, controlling the average voltage seen by the inductor. As the converter reaches steady state, there is no energy change across the inductor or no inductor current ripple change after every switching period, or it is called *volt-sec* balance:

$$(V_{in} - V_o) \cdot DT_{sw} = V_o \cdot (1 - D)T_{sw} \quad \Rightarrow \quad D = \frac{V_{out}}{V_{in}}, \tag{2.4}$$

where D is the turn-on duty ratio of ϕ_1. Accordingly, the output voltage can be regulated by tuning D. Compared to the dissipative conversion shown in Fig. 2.3 (a), the magnetic-based converter can sustain more current without generating much power loss. Note the power loss coming from switch R_{on}, capacitor equivalent series resistance (ESR), inductor DC resistance (DCR), etc are not considered yet and they are unavoidable in all converters.

2.3 Advantages, Applications and Motivations

A simplified guideline for conventional power converters is shown in Table 2.1, with the current rating range extracted based on the available parts from Texas Instruments as of year 2020. Among various converters, the LDO has the simplest structure and it is easy to be fully integrated. With only one passing transistor between its input and output, the LDO is beneficial in achieving the fastest regulation and highest accuracy. Therefore, LDO is extensively used in applications with critical voltage requirement, such as accurate sensor and analog blocks. Other than LDO, SC can also be fully integrated due to the intrinsically available on-chip capacitors, providing small form factor with the extra benefits on step-up conversion or polarity reversal, especially useful in tiny-scale energy harvesting. Both

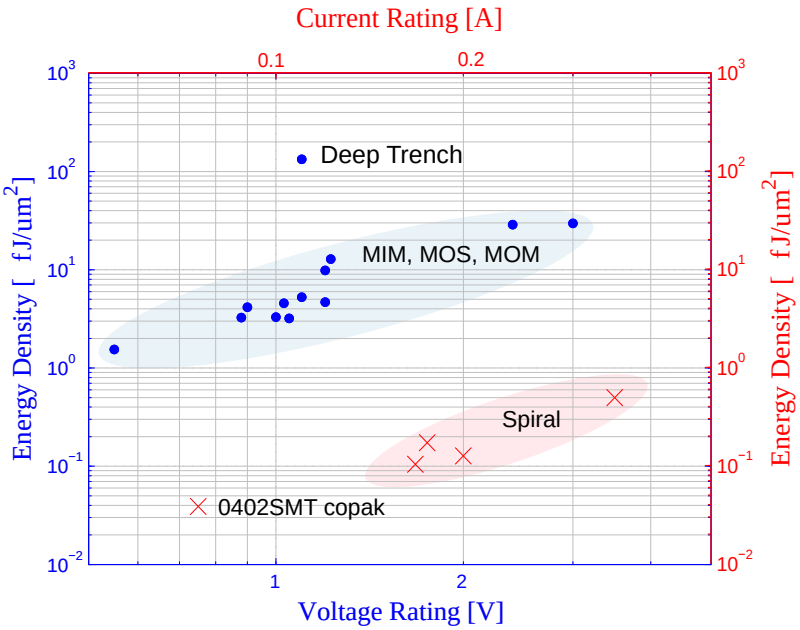


Figure 2.6: Energy density of on-chip inductors and capacitors. Data points are collected from integrated solutions with different fabrication processes in literature review.

LDO and SC have very limited efficiency when it comes down to the wide-range output regulation. As a result, the buck converter is usually considered when efficiency is of the greatest concerns, e.g. it is widely employed as the voltage regulator for current-starving computing loads [19]. Given various advantages, combinations of different types of power converters might also be considered. For example, when a critical voltage domain obtains energy from a higher voltage level, one would suggest to have a buck converter as the front stage for high step-down ratio with high efficiency, and an LDO as the second stage for very clean output voltage.

Switching converters are potential in providing higher efficiency and more flexibility, since the energy is transferred between non-dissipative elements. Apparently, the conventional SC is an exception, which is operated in a dissipative fashion showing poor efficiency when operating other than the native conversion ratio. However, the energy density of capacitors $\left(\frac{1}{2}CV^2/\text{Size}\right)$ is indeed much higher than that of inductors $\left(\frac{1}{2}LI^2/\text{Size}\right)$, because of the simple planar and stack-up structure of capacitors in a typical IC fabrication process. The on-chip capacitor can be 100X energy denser than inductor as shown in Fig. 2.6, or even 1000X denser in discrete components [13], [14]. The contradiction between limited SC performance and excellent capacitor energy density motivate this work. Questions left unanswered:

1. *Why do the SC designs have the lowest current rating?*
2. *How to utilize the high energy density advantage of the capacitor?*

Chapter 3

Soft-Charging Techniques

This chapter begins with the popular two-capacitor problem to understand the fundamental loss mechanism in conventional SC. It is found that the energy loss comes from the charge sharing process between capacitors (or voltage sources), and this loss can be reduced by multi-step charging as compared two-step charging in the two-capacitor problem. To further eliminate the charge sharing loss, a soft-charging technique is introduced by adding inductors into a conventional SC structure, ensuring a VIV-type energy transfer. As a result, a new class of power converter — hybrid or resonant SC converter is developed.

3.1 Two-Capacitor Problem — Hard Charging

A simplified energy transfer between two capacitors is shown in Fig. 3.1 (a), where the left capacitance is assumed much larger, i.e. $C_1 \gg C_2$, and it can be approximated as a voltage source to C_2. Initially, C_1 and C_2 have voltage of V_1 and V_2, respectively, and it is assumed that $V_1 > V_2$. As the switch turns on, C_2 will be charged from V_2 to V_1, and C_1 needs to provide a charge of $Q_1 = C_2(V_1 - V_2)$. By comparing the output energy from C_1 and the stored energy in C_2, there is an energy loss of

$$E_{loss,hard} = Q_1 V_1 - \left(\frac{1}{2}C_2 V_1^2 - \frac{1}{2}C_2 V_2^2\right) = \frac{1}{2}C_2 \Delta V^2, \tag{3.1}$$

dissipated in R_{on}, where $\Delta V = V_1 - V_2$. Fig. 3.1 (c) shows the capacitor current and voltage waveform with various R_{on}. Even though reducing R_{on} decreases the settling time, it meanwhile increases the current spike. By solely observing the energy loss on the resistor using $E_R = \int_0^\infty i_R^2 R_{on} dt$, we can reach the same result as (3.1). Similar process happens in all digital circuits, including gate drivers commonly used in power electronics, where V_{dd} is the supply voltage and C_2 is the gate capacitance. Fig. 3.1 (a) only shows one half part of a switching process (switched on), the other half is to short the capacitance (switched off). This leads to a total energy loss of CV_{dd}^2 every switching period, and therefore the digital

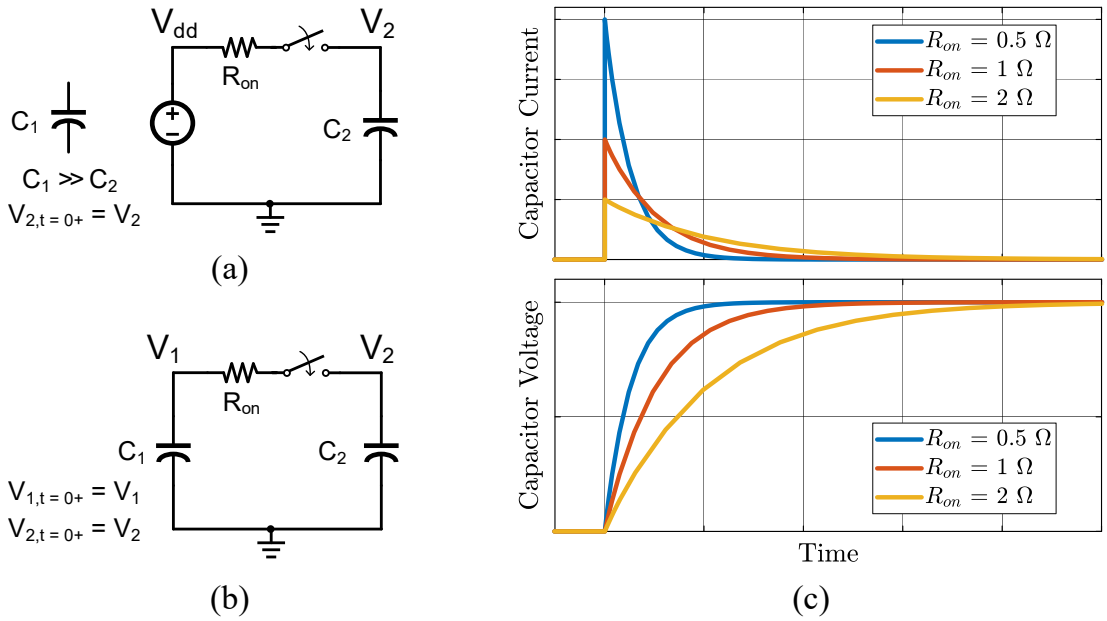


Figure 3.1: Capacitor charging by (a) a voltage source and (b) another capacitor, along with the (c) capacitor voltage and current waveform.

circuit switching loss or the gate driver loss can be estimated through

$$P_{driver} = CV_{dd}^2 f_{sw}. \tag{3.2}$$

A more general case of capacitor charging is shown in Fig. 3.1 (b), where C_1 and C_2 have different voltage level before the switch is closed. When the switch turns on, the voltage across the parallel capacitors becomes $\frac{V_1+V_2}{2}$, given C_1 and C_2 have the same capacitance, C. Similar to the case in Fig. 3.1 (a), there is an energy loss[1] of

$$\begin{aligned} E_{loss,hard2} &= E_{sw,open} - E_{sw,closed} \\ &= \left(\frac{1}{2}CV_1^2 + \frac{1}{2}CV_2^2\right) - \frac{1}{2}C\left(\frac{V_1+V_2}{2}\right)^2 \cdot 2 = \frac{1}{4}C\Delta V^2 \end{aligned} \tag{3.3}$$

to the hard charging process — an energy transfer from one capacitor (or a voltage source) to another. This loss happens after the charge distribution process, and hence it is called charge redistribution loss or charge sharing loss. Note the charge sharing loss increases quadratically with the voltage difference, ΔV, between the capacitors, which contradicts to allowing more voltage ripple and utilizing the high energy density in the capacitors. This explains why conventional SC has lower current rating, since higher processed current leads to higher ΔV and the power loss increases accordingly. In most cases, the switching frequency is designed much higher to avoid charge sharing loss and that further incurs undesired switching loss.

[1]Although the energy loss is regardless of the value of R_{on}, we can always assume $R_{on} > 0$ in practical applications. Therefore, we will not run into two-capacitor paradox for zero R_{on}

3.2 Staircase Charge Transfer — Quasi-Soft Charging

Instead of charging the capacitor directly to a target voltage, one or several intermediate values, V_m, can be inserted between the initial and the target voltage. In the case of one V_m inserted, C_2 is first charged from V_2 to V_m, and then from V_m to V_1. For simplicity, C_2 is assumed being charged by a large capacitance or a voltage source. By using (3.1), the total energy loss of the two-step charge transfer can be calculated as

$$\begin{aligned} E_{loss,quasi} &= E_{loss,V_2\to V_m} + E_{loss,V_m\to V_1} \\ &= \frac{1}{2}C\left(V_m - V_2\right)^2 + \frac{1}{2}C\left(V_1 - V_m\right)^2. \end{aligned} \tag{3.4}$$

As compared to the hard charging, one intermediate voltage helps reduce an energy of

$$\begin{aligned} \Delta E_{loss} &= E_{loss,quasi} - E_{loss,hard} \\ &= C\cdot\left[-V_1V_2 + V_m(V_1 + V_2 - V_m)\right]. \end{aligned} \tag{3.5}$$

If V_m is selected to be the mid point of V_1 and V_2, i.e. $\frac{V_1+V_2}{2}$, the stair-case transfer reduces the energy loss by

$$\Delta E_{loss,N=1} = \frac{1}{4}C\left(V_1 - V_2\right)^2, \tag{3.6}$$

as compared to the hard charging process, where N is the number of inserted values. From (3.6), it is now more obvious that E_{gain} is always greater than 0. To generalize the idea and extend it to multiple intermediate values, the energy gain then becomes

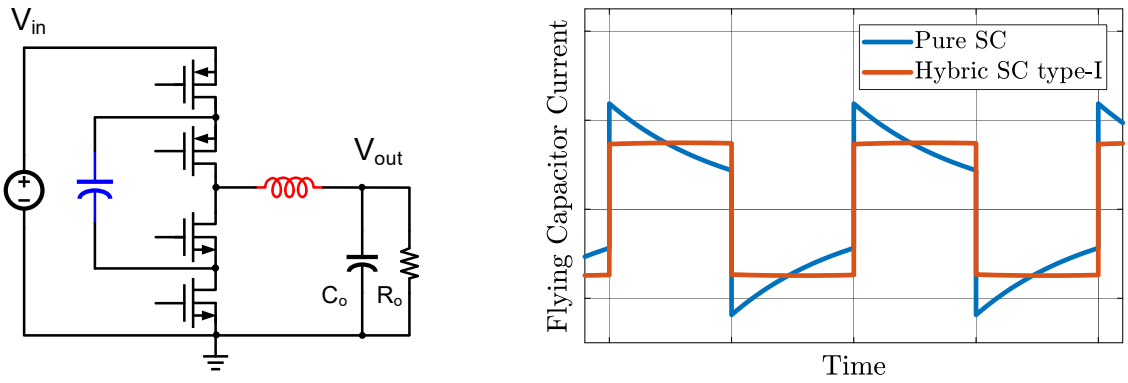
$$E_{loss} = \sum_{i=1}^{N}\left(\frac{1}{2}CV_m^2\right) = \frac{1}{2}C\frac{\Delta V^2}{N}, \tag{3.7}$$

As can be seen, the charge sharing loss can be reduced with an increasing N.

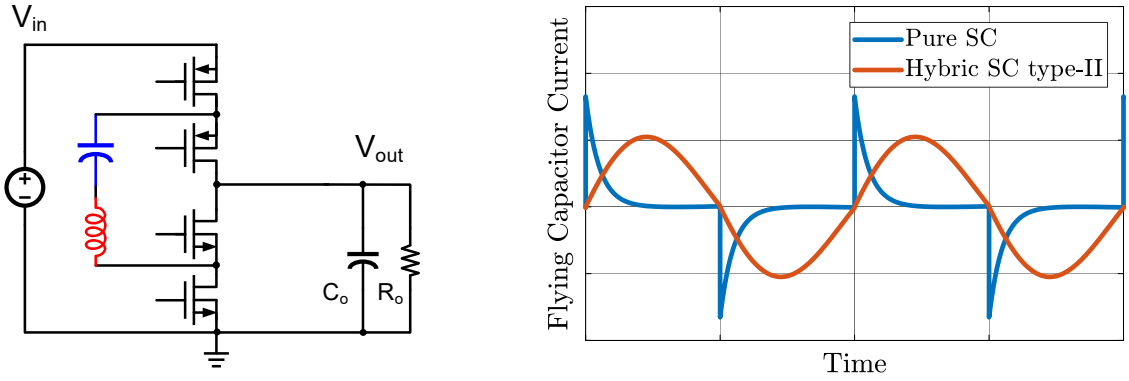
The staircase charge transfer technique was used [10] in reducing switching loss in bottom plate capacitance — an undesired parasitic capacitance to on-chip capacitor contributing to the major power loss for SC. However, this is not suitable and applicable to the main power conversion, as it requires a much more complicated switch and capacitor matrix along with floating gate driver is needed, lowering power density.

3.3 Smooth Charge Transfer — Soft Charging

The charge sharing loss can be eliminated as N approaches infinitely large according to (3.7), and the staircase voltage becomes smoothly linear. To achieve that, a current source can be added in series with the capacitor, enabling infinitely smooth charge transfer — soft-charging operation. The current source can be implemented by inductors and added to the conventional SC, generating a new class of power converters - hybrid SC or resonant



(a) Hybrid SC type-I: single inductor at the output, $f_{sw} > f_{res}$



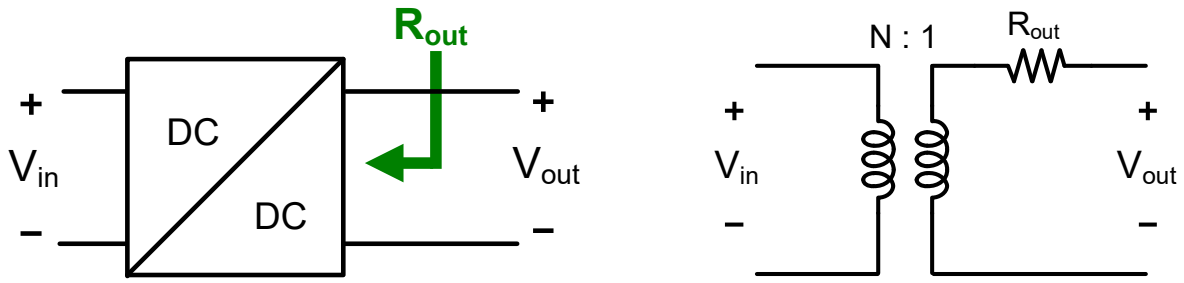
(b) Hybrid SC type-II: distributed inductors in series with the capacitor, $f_{sw} = f_{res}$

Figure 3.2: Smooth capacitor current in hybrid switched-capacitor converters.

SC converter [25]. As shown in Fig. 3.2, there are primarily two methods in achieving soft-charging operations: (i). hybrid SC type-I — single inductor at the output [54], [58] and (ii). hybrid SC type-II - distributed inductors in series with each flying capacitor [28], [59]. As compared to pure SC, both hybrid SC types with soft-charging operations have much smoother capacitor current, beneficial in obtaining low switch RMS current. From another perspective, the soft-charging operation transforms the pure SC from VVV-type energy transfer to VIV-type, which is ideally lossless similar to magnetic-based converters but now with high-energy capacitors processed part of the power.

Output impedance

To better characterize and compare different types of power converters, the output impedance, R_{out}, as shown in Fig. 3.3 (a) can be employed. Specially, a generic SC model applicable to pure and hybrid SCs is shown in Fig. 3.3 (b), which consists of an ideal fixed-conversion-



(a) (b) Generic SC model

Figure 3.3: Output impedance for characterizing power converters.

ratio, N, transformer[2] with an output referred impedance, R_{out}. The parameter R_{out} reflects the conduction loss, which incorporates losses from physical resistances in the circuit (e.g. switch on-resistance, R_{on}, and capacitor equivalent series resistance, ESR), capacitor charge sharing loss and VI-overlap loss. Generally, the switch on-state resistance, R_{on}, is more dominant [60], and only the impact of switch on-resistance is considered to focus on comparing the switch performances. As a result, R_{out} can be represented by [5]

$$R_{out} = \frac{P_{cond}}{{I_{out}}^2} = \sum_{i=1}^{N_b}\sum_{j=1}^{N_p} \frac{\left(a_{r,i}^{j}\right)^2}{D_j G_i} = \sum_{i=1}^{N_b}\sum_{j=1}^{N_p} \frac{\left(a_{sw,i,RMS}^{j}\right)^2}{G_i}, \tag{3.8}$$

where $a_{r,i}^{j}$ is the charge multiplier through switches, $a_{sw,i,RMS}^{j}$ is the switch RMS current multiplier, N_b is the number of switches, N_p is the number of phases (or circuit states), G_i is the i-th switch conductance and D_j is the duty ratio of the j-th phase. Note that the multipliers are values that are normalized to the average output current, I_{out}.

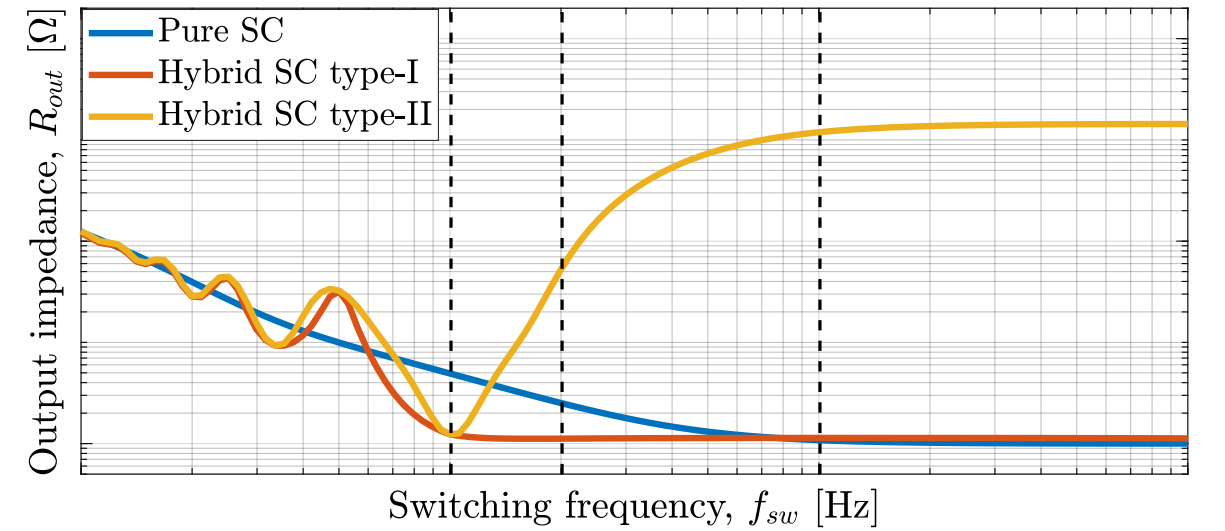
The output impedance versus switching frequency for pure and hybrid SC converters is shown in Fig. 3.4 (a)[3]. During simulation, all of the tested converters are attached to the same output load resistance, and R_{out} for SC converters is obtained using the model in Fig. 3.3 (b):

$$R_{out} = \frac{V_{out} - \frac{V_{in}}{N}}{I_{out}}. \tag{3.9}$$

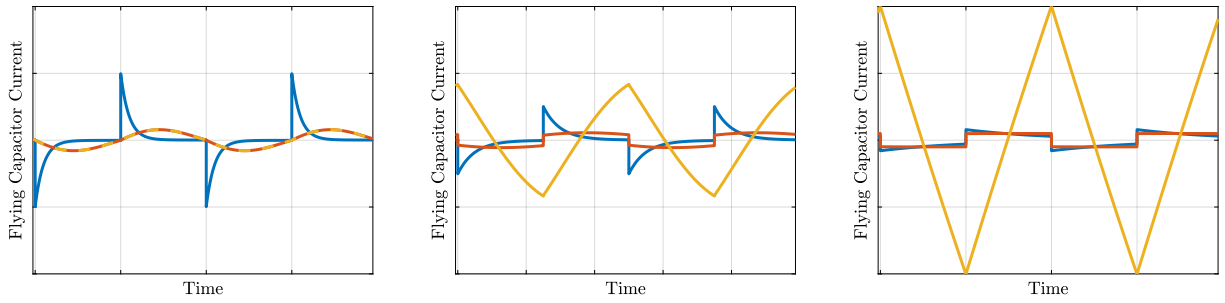
A lower R_{out} means a better switch utilization, and it has lower conduction loss according to (3.8), or a smaller switch size can be achieved for the same conduction loss. On the other side, a lower f_{sw} means a better passive utilization, and it has lower switching and gate driver losses, or a smaller passive size can be achieved. The $R_{out} - f_{sw}$ plot helps locate the optimal f_{sw} and achieve the lowest overall power loss.

[2]This model only applies to unregulated conversion, and the transformer represents the voltage ratio between its primary and secondary sides with the assumption of accepting any forms of input.

[3]Note the deadtime is also another crucial parameter at high f_{sw}, and Fig. 3.4 (a) assumes the deadtime proportionally decreases with increasing f_{sw}, otherwise R_{out} would increase with higher conduction loss associated with the body diodes.



(a)



(b) $f_{sw} = f_{res}$ (c) $f_{sw} = 2f_{res}$ (d) $f_{sw} = 10f_{res}$

Figure 3.4: Output impedance and time-domain waveforms for pure SC, hybrid SC type-I and hybrid SC type-II.

For pure SC, there are mainly two operational regions: the slow switching limit (SSL) for $f_{sw} < f_{crit}$ and the fast switching limit (FSL) for $f_{sw} > f_{crit}$, where $f_{crit} \approx \frac{1}{RC}$. While the pure SC is operating within SSL, R_{out} is dominated by $\frac{1}{sC}$, which corresponds to those hard-charging process mentioned in tunable resistance in section 2.2 and the two-capacitor problem in section 3.1. As can be observed, higher RMS current of the pure SC in Fig. 3.4 (b) and (c) leads to higher R_{out} in the SSL regions. As f_{sw} further increases and the pure SC enters into the FSL region, R_{out} is determined solely by switch R_{on} since the capacitor current ripple is much smaller (hence the voltage difference between capacitors is also smaller) and charge sharing loss is not as obvious as in the SSL region. However, the FSL region does not provide any output regulation, even though it has lower R_{out}. To obtain different output voltage, a lower switching frequency is needed to drive the pure SC back into the SSL region with a variable and higher R_{out}. Better efficiency in wide-range regulation might be addressed by multi-gear SC techniques [7], which obtains multiple conversion ratios by

reconfiguring a more complicated matrix of switches and capacitors. Nevertheless, it is still performance limited with large size required[4], and will not be covered in this dissertation.

Single Inductor at the Output

As compared to pure SC, this type of hybrid SC features the lowest R_{out} at lower switching frequency, which enables lower switching loss. There are mainly two operational states for the hybrid SC type-I shown in Fig. 3.2 (a): either ϕ_1 is on or ϕ_2 is on, where the inductor sees $\{V_{in} - V_{cfly}, V_o\}$ or $\{V_{cfly}, V_o\}$. At steady state, the flying capacitor voltage is maintained around $V_{in}/2$, and the output voltage is also around $V_{in}/2$ given the duty ratio is 0.5. The inductor in this hybrid SC works similar to the one in buck converter, except the voltage seen by the inductor is greatly reduced and the inductor current ripple decreases with increasing switching frequency. The inductor current is unidirectional and it points toward the output. At higher switching frequency, the inductor current becomes flat and it can be approximated as a current source. For $f_{sw} \gg f_{crit}$, the RMS current of pure SC and hybrid SC type-I approaches the same, which leading to similar R_{out} as it is now dominated by switch R_{on}.

Distributed Inductors in Series with Flying Capacitor(s)

The hybrid SC type-II shares the same characteristic with type-I at f_{res}, except the inductor current is bidirectional to keep the charge balance on the flying capacitor. As the switching frequency increases, the inductor current becomes more linear rather than sinusoidal. In order to meet the charge balance on the capacitor and obtain the required output current, the magnitude of the capacitor current becomes larger[5] as shown in Fig. 3.4 (c) and (d), which also means more reactive power flowing internally and causes higher power loss. Therefore, lower V_{out} and higher R_{out} are expected with increasing switching frequency. In another perspective, the series LC circuit or the flying tank acts as a bandpass filter, providing only low impedance when $f_{sw} = f_{res}$. It can also be observed that the output impedance of the hybrid SC type-II saturates after 10 times of f_{res}, showing that the phase of LC circuit reaches 180deg and very few current is going to the output. Due to the narrow available f_{sw} range, this type of hybrid SC is susceptible to parameter variations and it requires more complicated controller to achieve an accurate f_{sw}.

[4]Multigear SC converter is mostly assumed operated at SSL due to the limited on-chip capacitance density. Even when the capacitance density is improved, the converter has higher R_{FSL} due to its complicated switch matrix, leading to poor efficiency at heavy load condition.

[5]This characteristic should not be confused with the case in a buck converter, where higher switching frequency leads to lower inductor current ripple. The LC configurations of a buck converter and a hybrid SC type-II are different, i.e. band-pass filter vs. low-pass filter.

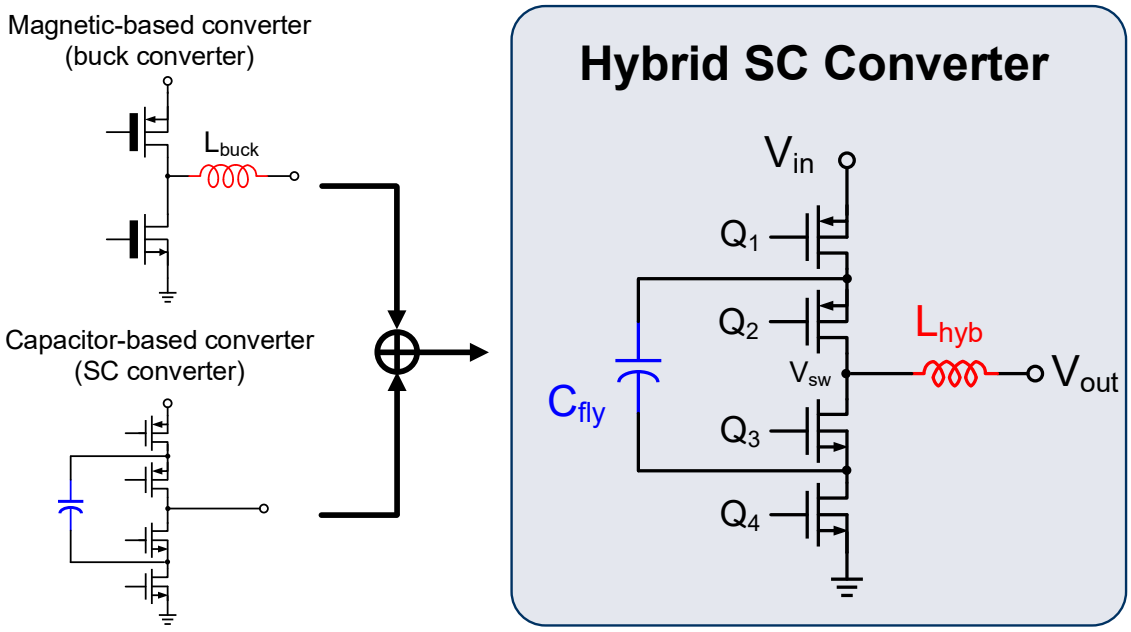


Figure 3.5: Hybrid SC converter — a merged combination of magnetic-based and capacitor-based converters.

3.4 Hybrid Switched-Capacitor Converter vs. Magnetic-based Converter

The hybrid SC using soft-charging technique eliminates the fundamental charge sharing loss in the conventional SC, providing an opportunity of utilizing the high energy density of capacitors. In particular, the hybrid SC type-I, which is indeed the merged combination of conventional capacitor-based (2-to-1 SC converter) and magnetic-based (buck converter) converters as illustrated in Fig. 3.5, shows similar operating principle as buck converters, shedding light upon the efficient output regulation using SC structures. While the hybrid SC is already compared to the pure SC, it is also essential to quantitatively compare it with magnetic-based converters in terms of their actives, passives and output regulation. The schematic shown in Fig. 3.5 (a) is also called three-level buck converter, which is served as the basic hybrid SC and compared to the buck converter.

Switch Requirement

There is always a confusion on the conduction loss in a hybrid SC converter; it looks as if the additional stacked-up switches require larger switch size than the buck converter. It is clarified here by comparing the conduction loss with the assumption of the same switch area

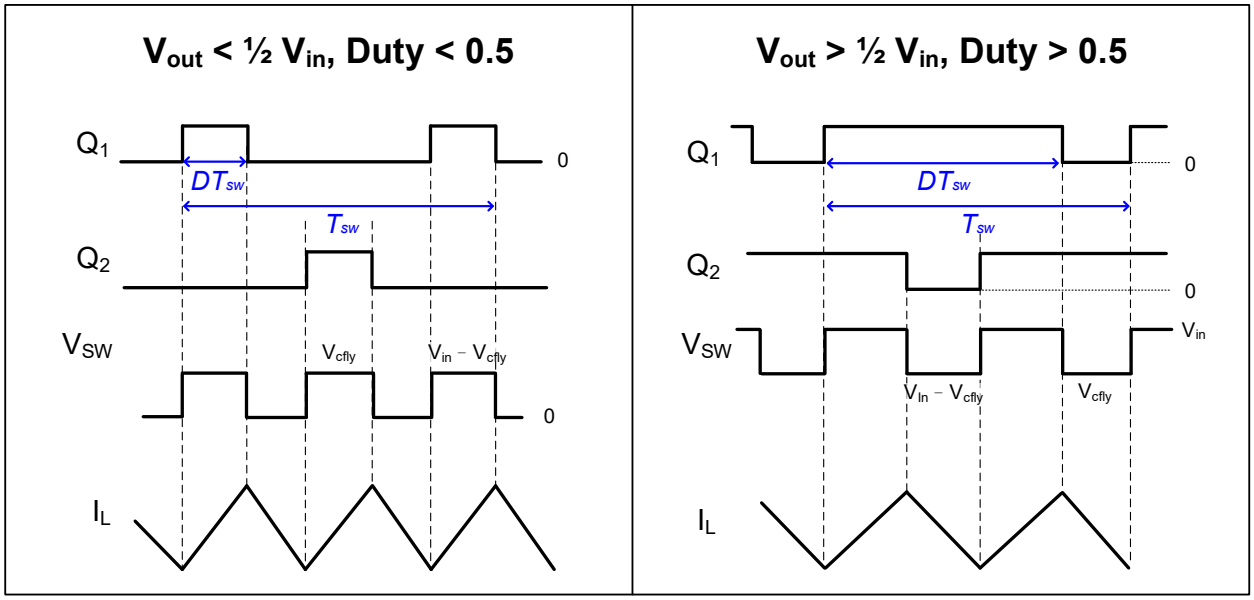


Figure 3.6: Operational waveforms of a three-level buck converter.

constraints or the total $G_{on}V_{rated}^2$ product [5], [61] for both converters,

$$\sum_{i=1}^{4} G_{on}V_{rated}^2\Big|_{\text{Three-level buck}} = \sum_{i=1}^{2} G_{on}V_{rated}^2\Big|_{\text{Conv. buck}}, \tag{3.10}$$

where G_{on} and V_{rated} represent the switch conductance and the rated blocking voltage, respectively. The flying capacitor in hybrid SC handles the voltage distribution across all the switches, the voltage stress on each switch is therefore only $V_{in}/2$ as compared to V_{in} in conventional buck converters. This allows the use of low blocking voltage switch with a better figure of merit on $R_{on}C_{gg}$, where C_{gg} is the switch gate capacitance. Given the constraint in (3.10), it can be deduced that the conductance of each switch in three-level boost converter can be $2X$ higher, i.e. $G_{on}|_{\text{Three-level buck}} = 2G_{on}|_{\text{Conv. buck}}$, revealing that the conduction loss contributed by each individual switch in the three-level buck converter is smaller. In other words, given the same switch area, the total conduction losses of the stacked-up devices in a three-level buck converter is equivalent to a conventional buck converter, since smaller low-voltage devices are employed. Meanwhile the gate driver loss for both converters is also the same, since the total gate capacitance is mainly determined by the switch size.

Conversion Ratio

Unlike pure SC, the hybrid SC or the three-level buck converter is able to operate with different conversion ratios through the *volt-sec* balance on the inductor. In a pure SC converter, changing the duty ratio does not give too much flexibility on conversion ratio, since

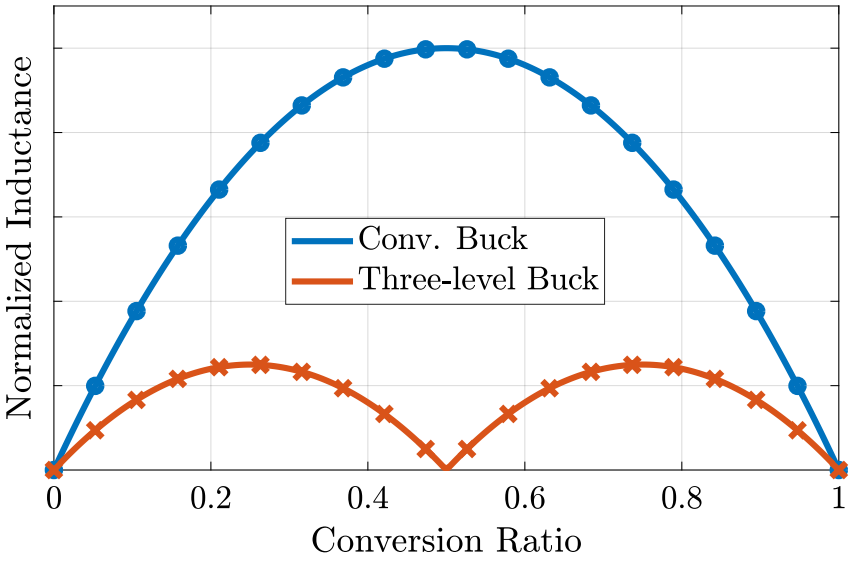


Figure 3.7: Inductance requirement reduction in a hybrid SC converter.

it is mainly determined by the conservation of charge or charge balance between capacitors; therefore, the duty ratio is usually set to 0.5 for more even heat spread and higher possible output power. In a three-level buck converter, four switches can be controlled by two sets of complementary signals with duty ratios other than 0.5. For the hybrid SC shown in Fig. 3.5, two complementary pairs are $Q_1 - Q_4$ and $Q_2 - Q_3$ with Q_2 (Q_3) being the 180° phase-shift version of Q_1 (Q_4). Depending on the operating regions, as shown in Fig. 3.6, the switching node voltage, V_{sw}, pulsates with a level of $V_{in}/2$, that is between $V_{in}/2$ and ground for $D < 0.5$ or V_{in} and $V_{in}/2$ for $D > 0.5$, assuming $V_{cfly} \approx V_{in}/2$. The case of $D < 0.5$ is used to compute the desired operating conversion ratio:

$$\Delta I_L = \frac{\left(\frac{V_{in}}{2} - V_o\right) \cdot DT_{sw}}{L_{3lvl}} = \frac{V_o \cdot \left(\frac{1}{2} - D\right) T_{sw}}{L_{3lvl}}. \tag{3.11}$$

With some manipulations, the conversion ratio can be expressed as follow:

$$\left.\frac{V_o}{V_{in}}\right|_{\text{Three-level buck}} = \left.\frac{V_o}{V_{in}}\right|_{\text{Conv. buck}} = D. \tag{3.12}$$

Note that the other operating region, $D > 0.5$, will arrive at the same derivation results. From (3.12), the three-level buck converter exhibits the similar characteristics as a conventional buck converter, achieving variable conversion ratios with a tunable D.

Inductance Requirement

As shown in Fig. 3.6, the inductor of a three-level buck converter is magnetized and demagnetized twice within a switching period, T_{sw}, leading to inductor current ripple reduction.

Take $D < 0.5$ as an example, the inductance required by the three-level buck converter can be derived from (3.11) and (3.12), which can be further expressed as

$$L_{3lvl} = \frac{(1-2D) \cdot V_{in} \cdot D}{2\Delta I_L f_{sw}}. \tag{3.13}$$

As compared to the inductance required in a buck converter:

$$L_{buck} = \frac{(1-D) \cdot V_{in}}{\Delta I_L f_{sw}}, \tag{3.14}$$

the equivalent frequency seen by the inductor of the three-level buck converter is doubled and the voltage across it is reduced. Given the same requirement on input voltage and inductor current ripple for both converters, the three-level buck convert requires much smaller inductance than the buck converter[6], as shown in Fig. 3.7. This is mainly contributed by the energy processing involvement of the flying capacitor in the three-level buck converter [14]. Given the higher energy density in capacitors than inductors as shown in Fig. 2.6, the power density of the three-level buck converter can be improved significantly with the inductance being scaled down.

[6]Note the flying capacitor in this figure is assumed relatively large. Ideally, in the special case of $D = 0.5$, there is no inductor current ripple or the least inductance required, where all the energy is processed by the flying capacitor and the three-level buck converter behaves like a pure SC when $D = 0.5$. In practice, the inductor current ripple increases or the required inductance increases as the flying capacitance decreases to a relatively small value.

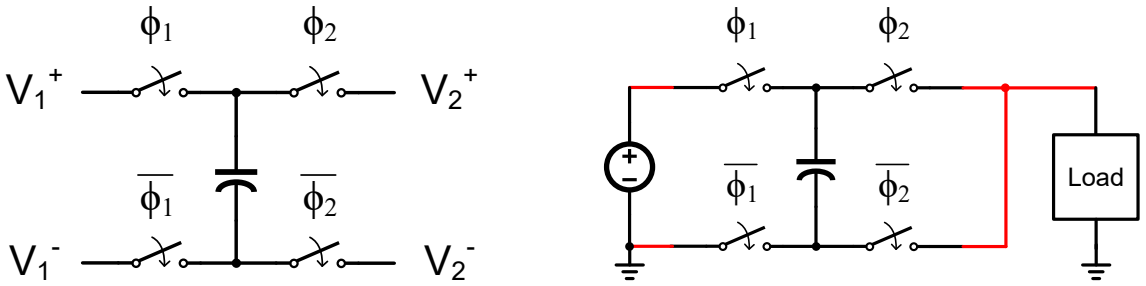
Chapter 4

Topologies of Hybrid SC Converter

Several SC topologies with higher conversion ratios can be synthesized through connecting fundamental SC cells in different patterns. The soft-charging techniques introduced in Chapter 3 can turn these SC topologies into hybrid SC topologies by adding inductor(s) at different placements, eliminating the charge sharing loss. In particular, for hybrid SC type-I with an inductor placed at the output of SC topologies, it is able to provide wider conversion ratios without operating into high output impedance region, hence beneficial in more applications and becoming the primary focus of this work. Through the quantitative analysis on output impedance and required capacitor energy, the switch and passive utilization of each topologies can be compared. While there are many excellent prior arts [14], [58] working in topology comparison, practical consideration including commercially available devices and layout constraints were not covered. In this chapter, a more complete and practical selection guideline for both discrete and integrated implementations is therefore suggested, revealing the difficulties encountered by some of the popular topologies. A comparison framework is developed based on a new metric — output conductance density, which merges the performance index of power density and efficiency. The new metric reflects both switch and passive utilization, providing clear implementation goals for power converters. Meanwhile, it also helps visualize and predict the developing trend of power converters, when extending toward higher conversion ratios. Based on a comparison result, various excellent topologies are suggested depending on the device availability.

4.1 Generation and Synthesis of SC Topologies

The most basic hybrid SCs, achieving providing a 2-to-1 native conversion ratio, were shown in Fig. 3.2. It is found that there is a fundamental SC cell: a combination of four switches and one capacitor as shown in Fig. 4.1, which can be employed for extensions to higher conversion ratios. For simplicity, two sets of complimentary control signals, ϕ_1 and ϕ_2, are assumed for two-phase operations. For example, a simple 2-to-1 SC converter can be generated by connecting the primary side of an SC cell to a input voltage source along with



(a) fundamental SC cell (b) 2-to-1 SC converter using one SC unit

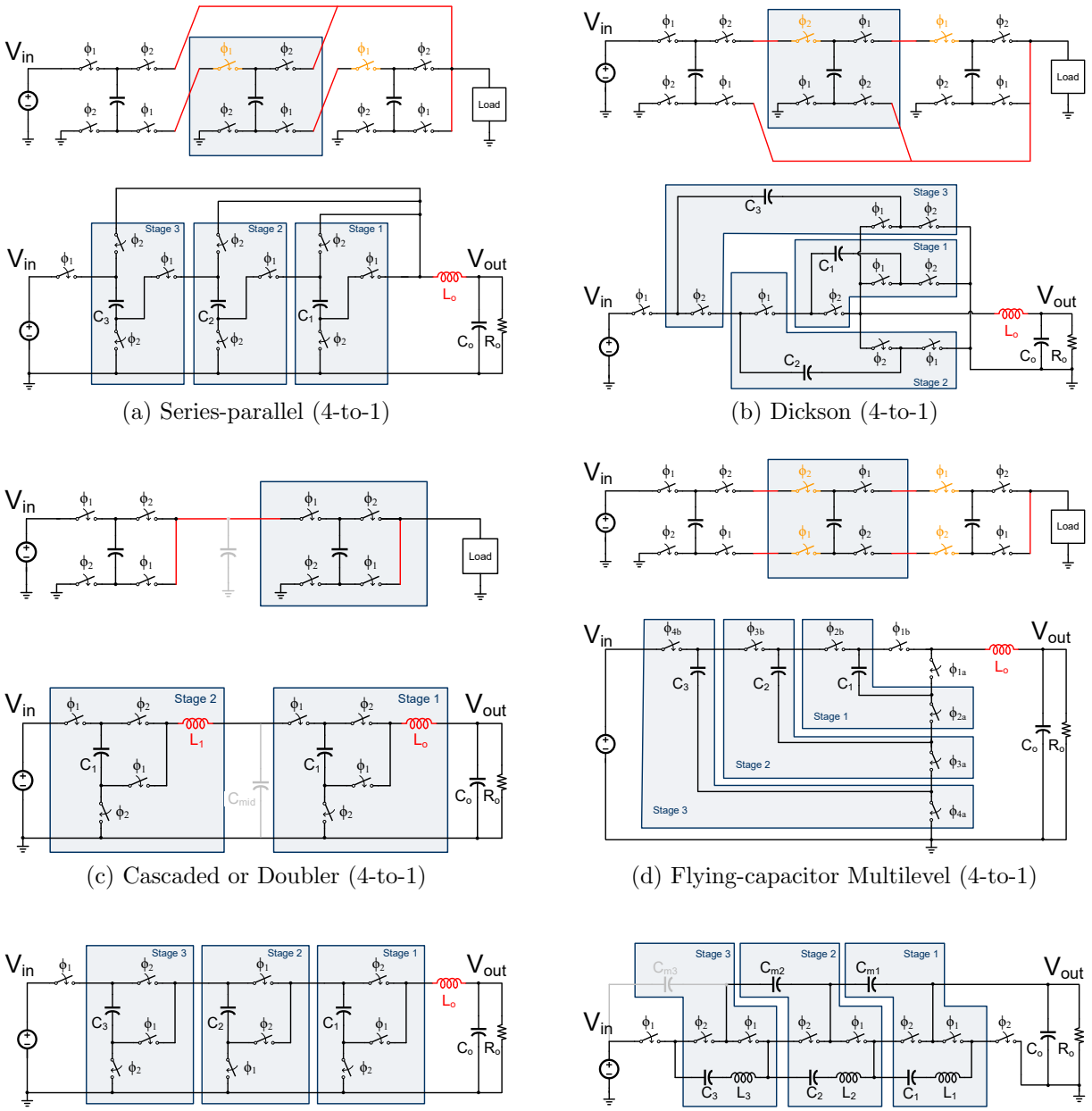
Figure 4.1: Fundamental SC cell and 2-to-1 converter.

the secondary side shorted to the load as shown in as shown in Fig. 4.1 (b).

More SC cells can be duplicated and connected for conversion ratio higher than 2. The first step is to arrange duplicated cells in a row with a certain pattern. While placing the cells, the SC cell can be rotated, twisted and mirrored due to its symmetric structure. As a result, the switching signals for the SC cells can be in the same order or in an interleaved fashion. The second step is to make connections for each cell, which can be categorized into to two: (i) connection to another SC cell or (ii) connection to a dc voltage, e.g. input voltage, output voltage or ground. Note the load voltage will be the switching node for hybrid SC, which is assumed relatively stable as capacitors are usually selected large enough to maintain low voltage ripple. By different ways of connection, multiple SC topologies can be synthesized as shown in Fig. 4.2, where 2 to 3 SC cells are used to exemplify. The third step is to merge adjacent switches with the same switching function. Finally, inductor(s) can be added to the SC topologies to achieve soft-charging operations. After some rearrangement, it is clear that how each SC topology can be further extended with their own characteristic recursive stages (highlighted by blue boxes) as shown in Fig. 4.2.

Take the series-parallel topology as an example, multiple SC cells with the same sequence for switching signals are first placed in a row, ready for connections. The start cell (the leftmost) is connected to a input voltage source, and the end cell (closest to the load) does not have the next cell to be connected with and is usually tied to the load similar to the basic 2-to-1 SC. All middle SC cells have their one terminal, V_2^+, at the secondary side **parallel** connected to the load, and the other terminal, V_2^-, connected in **series** with the primary side of their next adjacent cell. After merging the series switches with the same switching signals, it can be observed that the series-parallel topology is essentially composed of repetitive cells (three switches and one capacitor) together with a starting switch (closest to the input source). Similar idea on SC cells connection can be applied to generate Dickson topology, and the primary difference between them is the interleaved switching signal sequence of the SC cell in the Dickson topology. Accordingly, other topologies including cascaded, flying capacitor multi-level (FCML), Fibonacci and ladder can be generated through connections of the SC cells in various patterns.

As of now, a number of SC topologies can be made to operate in soft-charging and



(a) Series-parallel (4-to-1)

(b) Dickson (4-to-1)

(c) Cascaded or Doubler (4-to-1)

(d) Flying-capacitor Multilevel (4-to-1)

(e) Fibonacci (5-to-1)

(f) Ladder (4-to-1)

Figure 4.2: SC topologies generation through recursively added fundamental SC cells.

resonant mode with a single inductor at the output, including series-parallel, Dickson, FCML and Fibonacci, have been proved that they can be soft-charged with single inductor at the output [54]. The series-parallel and Fibonacci topologies can achieve complete soft charging with same flying capacitance throughout their structures, while the Dickson and Doubler topologies require a highly skewed flying capacitance ratio. In the Dickson topology, the

Table 4.1: Switch requirement for SC topologies.

	Number of Switches	**Switch Voltage Rating**	**Total Switch Stress, V_oI_o**
Series-parallel	$3N-2$	$(N-1)V_o \ldots 2V_o,\ V_o$	$\frac{(N-1)(N+2)}{N}$
Dickson	$3N-2$	$2V_o, V_o$	$\frac{4(N-1)}{N}$
Cascaded	$4\log_2 N$	$\frac{N}{2}V_o \ldots 2V_o,\ V_o$	$2\log_2 N$
FCML	$2N$	V_o	N
Fibonacci†	$3k+1$	$F(k+1) \ldots 2V_o,\ V_o$	Note‡
Ladder	$2N$	V_o	$\frac{4(N-1)}{N}$

† k is the number of stages in Fibonacci topology, and $N = F(k+2)$.
$F(\cdot)$ is the Fibonacci series, where $F(1) = 1$, $F(2) = 1$, $F(3) = 2$, ..., $F(n) = F(n-1) + F(n-2)$.

‡ if $k = 2m, \forall m \in \mathbb{Z}^+$,

$$\frac{1}{N}\sum_{m=1}^{k/2}\{F(2m+1)\left[F(k-2m+4)+F(k-2m+2)\right]+F(k-2m+1)F(2m)\}+\frac{1}{N}F(k)F(1)$$

if $k = 2m+1, \forall m \in \mathbb{Z}^+$,

$$\frac{1}{N}\sum_{m=1}^{k/2}\{F(2m+1)\left[F(k-2m+4)+F(k-2m+2)\right]+F(k-2m+1)F(2m)\}+\frac{1}{N}\left[F(k+2)+2F(k)\right]$$

skewed ratio can be addressed by additional operational phases (known as split-phase in [62]), so that all the flying capacitance can be the same. On the other hand, all of the SC topologies can be turned into hybrid SC with distributed inductors in series with the flying capacitors. Specially, for the cascaded topology, the inductor of each stage can either be placed at the output (as shown in Fig. 4.2 (c)) or in series with the flying capacitor of each 2-to-1 SC stage. Note that both cascaded and ladder topologies require middle or bypass capacitance, C_m, between stages, which can be reduced by multi-phase solution or implemented using same LC tank in the case of hybrid SC type-II. Other topologies like Dickson can be re-modified by replacing some of the flying capacitance (even numbered in Fig. 4.2) to bypass capacitance (relatively large capacitance so that it is not involved in the resonant operation), which then becomes the switched tank converter [28].

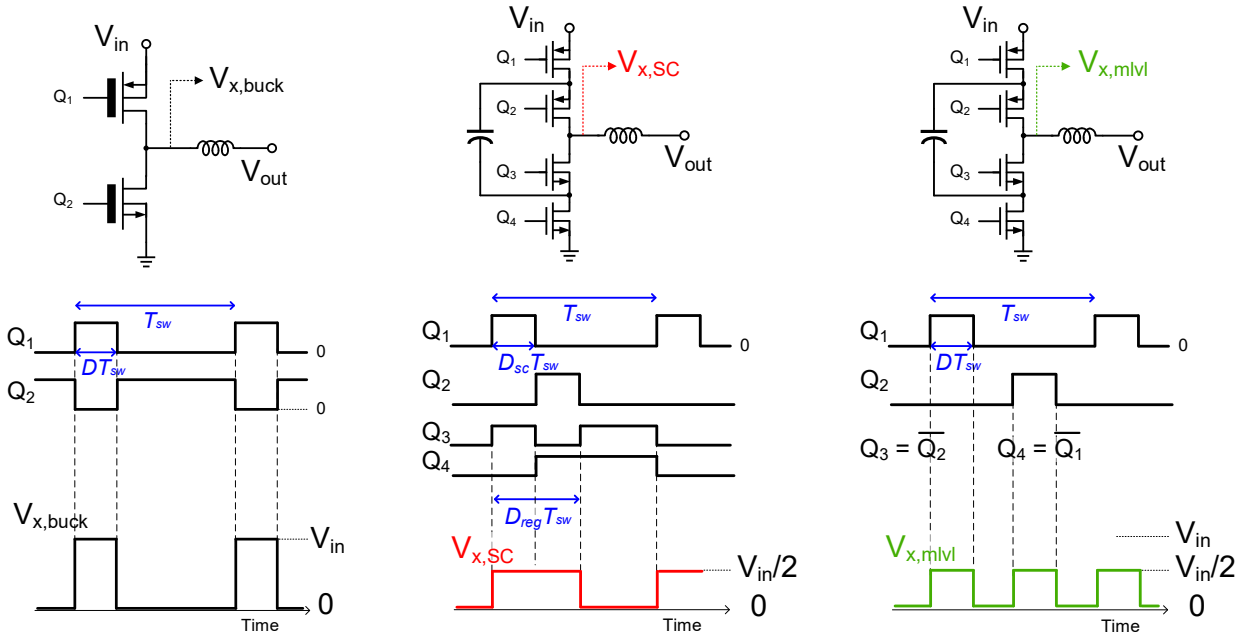
Table 4.1 and 4.2 summarize the switch and capacitor requirement, respectively, providing a quick overview when designing a specific topology. In these tables, N represents the conversion ratio, and all of the topologies will be reduced to the same structure as shown

Table 4.2: Capacitor requirement for SC topologies.

	Number of Capacitors	**Capacitor Voltage Rating**	**Total Capacitor Energy, $\frac{1}{2}CV_o^2$**
Series-parallel	$N-1$	V_o	$N-1$
Dickson	$N-1$	$(N-1)V_o \ldots 2V_o,\ V_o$	$\frac{N(N-1)(2N-1)}{6}$
Cascaded‡	$\log_2 N$	$\frac{N}{2}V_o \ldots 2V_o,\ V_o$	$\frac{N^2-1}{3}$
FCML	$N-1$	$(N-1)V_o \ldots 2V_o,\ V_o$	$\frac{N(N-1)(2N-1)}{6}$
Fibonacci†	k	$F(k+1)V_o \ldots 2V_o,\ V_o$	$\sum_{m=1}^{k}[F(m+1)]^2$
Ladder‡	$N-1$	V_o	$N-1$

† k is the number of stages in Fibonacci topology, and its conversion ratio
‡ bypass capacitors are not included.

in Fig. 4.1 (b) when $N = 2$. While most of the topologies have their number of stages increased linearly with the conversion ratio, the cascaded topology has it quadratically and the Fibonacci topology has it associated with the two previous values (or increased with golden ratio for large numbers). As a result, both cascaded and Fibonacci topologies are advantageous with less components for higher conversion ratios, especially in discrete implementations. The voltage ratings in switches and capacitors are very important, since they determine the selection of the devices or the fabrication process. When scaling the switches, the average total switch stress is needed to evaluation the switch utilization, which is calculated by the total of average power processed by the switches and it simultaneously considers voltage and current ratings. For passive components, the total capacitor energy can be used to approximate the capacitor size of each topology. By comparing the switch and capacitor requirement in Table 4.1 and 4.2, it can be seen that there are trade-offs between the switch and passive utilization: the advantages in better switch utilization are usually at the expenses of worse passive utilization, or vice versa. For example, the Dickson topology has the best switch utilization, but it has the worst passive utilization. Similarly, the series-parallel topology has the best passive utilization, but it has the worst switch utilization. To better compare different topologies, both switches and passives should be factored in, details of which will be provided in Section 4.3.



(a) Buck converter (b) All Hybrid SC Type-I (c) FCML

Figure 4.3: Switching scheme to achieve output voltage regulation for a buck converter and hybrid SC topologies.

4.2 Output Voltage Regulation

Hybrid SC type-I provides an efficient output voltage regulation through the *volt-sec balance* across its output inductor. An example using a 2-to-1 SC was demonstrated in Section 3.4. Here, a more general method extends the regulation capability to more hybrid SC topologies.

In a buck converter, the output voltage can be changed by tuning the duty ratio of the pulse voltage seen by the output inductor at its switching node, $V_{x,buck}$, which is shown in Fig. 4.3 (a). Similarly, the duty ratio of the pulse voltage at switching node voltage, $V_{x,SC}$, of the hybrid SC type-I topologies can be adjusted. The only difference between $V_{x,buck}$ and $V_{x,SC}$ is their amplitudes: V_{in} vs. V_{in}/N — a reduced voltage source. To achieve output regulation for hybrid SC type-I, an additional phase is added after the original operational phases (normally two) in order to ground the output inductor and generate a zero voltage level at $V_{x,SC}$, which was not feasible in the pure SC. For example in Fig. 4.3 (b), the ratio between the original two phases are maintained the same, i.e. $D_{sc1} = D_{sc2}$, and the total time of the two phases over the whole switching cycle, T_{sw}, becomes a new regulation duty ratio, D_{reg}, for regulating the output voltage:

$$\left.\frac{V_{out}}{V_{in}}\right|_{hybSC-I} = \frac{D_{reg}}{N}. \tag{4.1}$$

Specially, the buck converter has $N = 1$ and it does not do any amplitude scaling to the input

voltage. Furthermore, a different switching scheme as shown in Fig. 4.3 (c) is feasible to the FCML topology, which has three levels (0, $V_{in}/2$, V_{in}) available at $V_{x,mlvl}$ and it is controlled by two sets of complementary signals with 180^o phase shift with each other. A general N-level FCML topology will require $N-1$ sets of complementary signals with $360^o/(N-1)$ phase shift between each set. The wide-range levels available at the switching node allows more output regulation flexibility for the FCML topology, and it is able to provide the same conversion ratio as the buck converter.

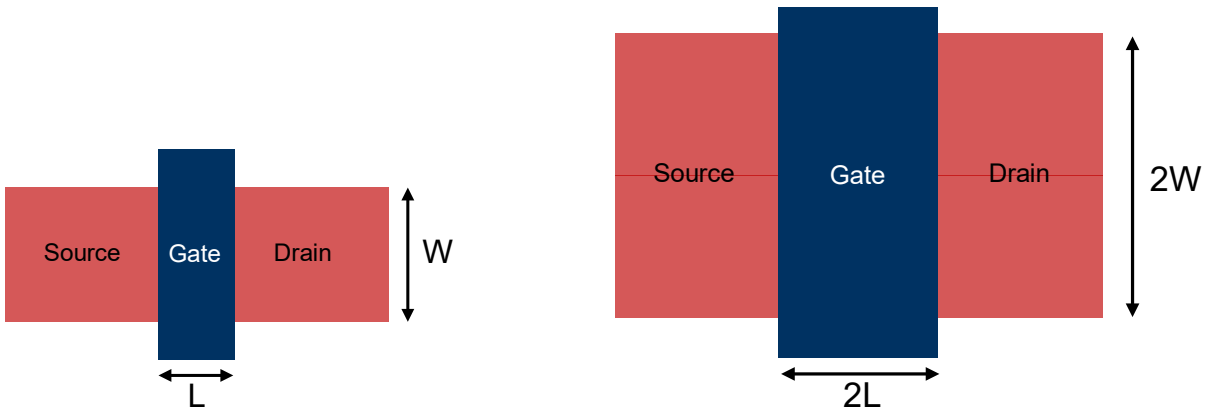
Compared to the conventional buck converter, all hybrid SCs are beneficial in having reduced inductance requirement due to lower inductor voltage and increased effective switching frequency. Depending on the topologies, different extent of conversion ratios can be achieved and applied to various situations. For example, the very wide-range conversion ratio featured by the FCML topologies enable its efficient implementation in ac power conversions [63]. On the other hand, some applications, such as 1 V for PoL, have a more specific output voltage within a relatively narrow range, other concerns might be prioritized. For instance, a 4-to-1 Dickson with the highest switch utilization along with some range of output regulation is suitable for the PoL application. Other than the regulation range, parameters including the switch and passive utilization are necessary to take into account before making the decision on topologies.

4.3 Optimal Switch Utilization

Better switch utilization usually means higher heavy-load efficiency (conduction loss dominated) or smaller switch size. One way to characterize the switch utilization is by analyzing the converter output impedance. Therefore, to compare topologies, the output impedance of each topology can be optimized given all topologies are assumed the same switch sizes. The most important thing to the optimization process is the modeling of switch size, which is closely related to the transistor scaling trend based on the practical device availability. This section discusses the switch utilization for two extreme cases — fully customized and uniform switches based on fabrication process, voltage domains and applications. A comparison framework, combining the switch and passive utilization, is then proposed to provide a more comprehensive understanding on different topologies.

Transistor Scaling

Key parameters in modeling a switch for a power converter are the switch size, conductance, G_{on}, and the rated voltage, V_{rated}, and the purpose of transistor scaling is to understand their relationship. For example, Fig. 4.4 shows the basic layout for a typical MOSFET switch with a channel area of WL and specifications of G_{on} and V_{rated}, and a model for transistor scaling is desired to predict the size for switches with different specifications. As shown in Fig. 4.4 (b), doubling V_{rated} requires increasing the length to $2L$ for longer buffering region. However, in order to maintain the same G_{on}, the MOSFET with $2V_{rated}$ should also



(a) Conductance G with one rated V (b) Conductance G with two rated V

Figure 4.4: MOSFET transistor scaling.

have a wider channel, leading to a total area of the new MOSFET 4 times as before. To analyze that, the crucial part is the switch channel, which is the overlapped region of the blue polysilicon gate terminal and red ion-implantation source-drain pads. A wider and shorter channel provides lower on-resistance or higher G_{on}: $G_{on} \propto \frac{W}{L}$; whereas a longer channel sustains higher V_{rated}: $V_{rated} \propto L$. As a result, the switch area[1] can be approximated as

$$A_{tot} = W \cdot L = \frac{W}{L} \cdot L^2 \ \propto G_{on} V_{rated}^2. \tag{4.2}$$

For the same fabrication process, it is reasonable to assume the same depth. As a result, the switch size factor of the whole converter can be expressed by

$$X_{tot} = \sum_{i=1}^{N_b} G_i V_{i,rated}^2 \propto \mathrm{Vol}_{sw,tot}, \tag{4.3}$$

where N_b is the number of switches. Note that (4.3) is associated to the gate-channel area, which further reflects the switch gate capacitance and indicates the gate driver loss.

In reality, the relation suggested by (4.3) might deviate from the square low of V_{rated} due to the rough approximation using $V_{rated} \propto L$. However, the switch scaling through (4.3) serves its purpose to some extent. Fig. 4.5 (a) shows a survey[2] for commercial silicon

[1]Total area of the switches should also take into account the contacts, spacings and metal 1 routing. However, the transistor channel provides good enough first-order estimation. A linear correction factor can be added to predict the actual switch size, e.g. $A_{tot} = k_{size} \cdot W \cdot L$, where k_{size} is around 4 empirically and it depends on fabrication process.

[2]In fact, there are discrete switches with lower V_{rated} available from other providers like Texas Instruments and Vishay. However, their performance on G_{on}/Vol_{sw} is not as good as those 25 V switches from Infineon. As a result, they are not considered in this survey, which is also reasonable since they do not use the same fabrication process. The example of discrete switches represents the vertical switches, whereas more details about the planar integrated switches will be provided in section 5.2.

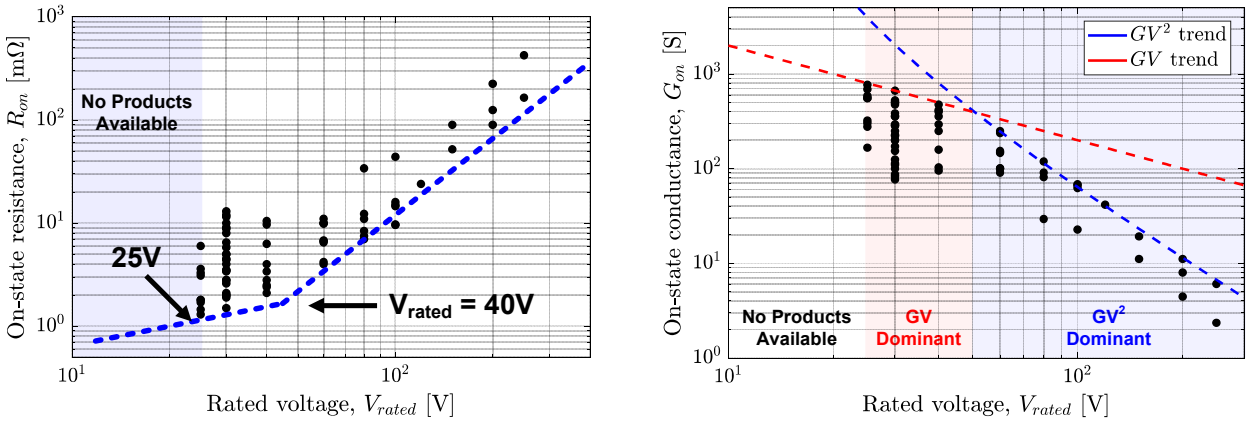


Figure 4.5: Survey of high-performance discrete silicon transistors. Data points are from active Infineon Optimos^{TM} products in S3O8 package (3.3 mm x 3.3 mm x 1 mm). [64]

transistors with excellent switch R_{on} and small form factor, Vol_{sw}. Given the same footprint (or area constraint), a trend line is plotted for minimum available switch R_{on} against V_{rated}. By turning R_{on} into G_{on}, Fig. 4.5 (b) is generated to clearly show switch G_{on}'s dependency on V_{rated}. The aforementioned transistor scaling trend is fulfilled by transistors with higher V_{rated}. However, the scaling trend gets weaker as V_{rated} goes below 40 V, and a disruption happens below 25V. Generally, the switch rated voltage, V_{rated}, is customized or selected slightly above the blocking voltage, in order to maximize $G_{on}/\text{Volume}_{sw}$, based on (4.3). While lower blocking voltage is still desired to allow better switch performance with smaller switch volume, the device availability leads to different results on optimal output impedance depending on the voltage domains.

Operating Conditions for Optimal Output Impedance

Table 4.3 summarizes the operating conditions required for achieving the minimum output impedance, R_{min}, in pure and hybrid SCs, where all flying capacitance are assumed the same as C. For the pure SC, R_{min} occurs at FSL region when operating at high f_{sw}, where the converter performance is mainly dominated by the switch R_{on}. In addition, the duty ratio for pure SC is usually set around 50% to ease the controller implementation, given the charge balance of flying capacitors is irrelevant to the duty ratio. Hybrid SC type-I achieves R_{min} when operating higher than the resonant frequency, i.e. $f_{sw} > f_{crit}$; sometimes, it is designed operated around the resonant frequency to lower the switching loss with some compromise on conduction loss. Rather than commonly seen 50% in pure SC, the duty ratio of hybrid SC type-I is set according to the ratio of equivalent capacitance seen by the

Table 4.3: Operating conditions of achieving minimum output impedance, $R_{\min}$.

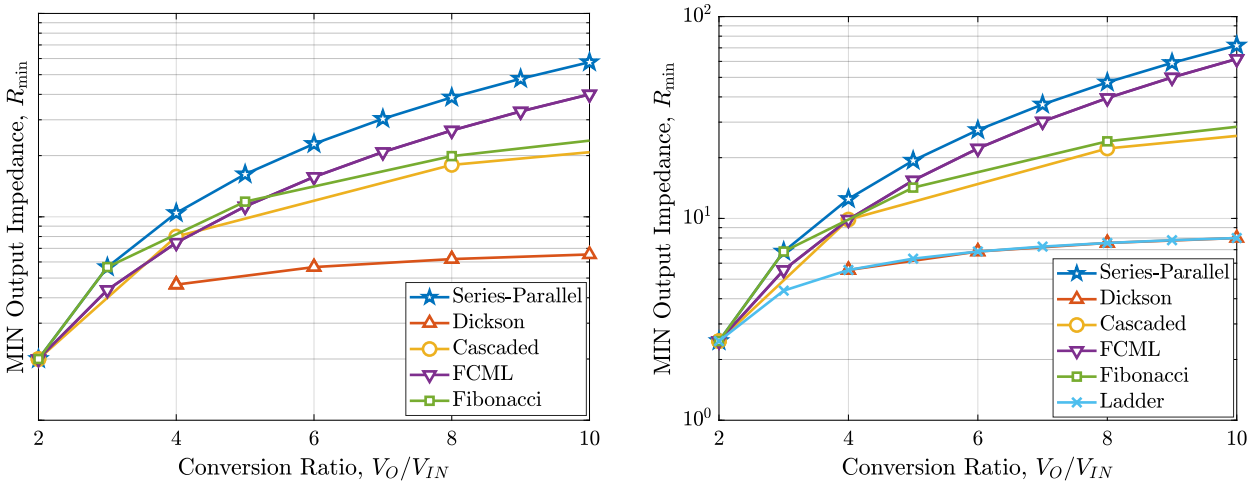
	Pure SC	**Hybrid SC type-I (single inductor)**	**Hybrid SC type-II (distributed inductors)**
Critical frequency, f_{crit}	$\frac{1}{R_{\min}C_{eq,sc}}$	$\frac{1}{2\pi\cdot\sqrt{LC_{eq,HybSC1}}}$	$\frac{1}{2\pi\cdot\sqrt{LC}}$
Operating frequency, f_{sw}	$f_{sw} > f_{crit}$	$f_{sw} > f_{crit}$	$f_{sw} = f_{crit}$
Switch RMS Current, $I_{sw,RMS}$	$\frac{\overline{I_{sw,t\in[0,DT_{sw}]}}}{\sqrt{D}}$	$\frac{\overline{I_{sw,t\in[0,DT_{sw}]}}}{\sqrt{D}}$	$\frac{\overline{I_{sw,t\in[0,DT_{sw}]}}}{\sqrt{D}}\cdot\frac{\pi}{2\sqrt{2}}$
Typical Duty Ratio, D	50%	Topology dependent	50%

inductor every operational phase, since the charging and discharging of the flying capacitors are determined by its inductor current.[3] The skewed capacitance ratio seen by the inductor also leads to different equivalent capacitance, $C_{eq,HybSC1}$, or resonant frequency. Unlike pure SC and hybrid SC type-I allow low R_{out} for wider switching frequency, hybrid SC type-II achieves lower R_{out} only at a few operating frequencies, with the optimal R_{min} occurs at f_{crit}. In that case, its duty ratio should always be 50% to maintain complete resonant cycles of a sinusoidal current waveform, which has a RMS value $\frac{\pi}{2\sqrt{2}}$ times the flat current. However, its resonant frequency is simply determined by each LC tank, and all tanks are usually set the same for synchronized current and the lowest impedance. As a result, hybrid SC type-II has the same patterns of switch charge multiplier as its pure SC companion operating at FSL, except that it has higher current amplitude. Its equivalent R_{out} can simply be derived from the pure SC, which is $R_{eq,HybSC-II} = \frac{\pi^2}{8}\cdot R_{pc}$.

Optimal Output Impedance for Fully Customized Switches

The primary focus of the optimal output impedance is on the switch performance, whereas the passives determined the operating frequency will later be taken into consideration in a more comprehensive comparison framework. Given the definition of R_{out} expressed in (3.8) as well as the general constraint of a total switch area, X_{tot}, suggested by (4.3), $R_{\min}$ of a

[3]There is one exception from the FCML topology. To maintain the charge balance between flying capacitors, the duty ratio is set as $\frac{1}{N}$ at very high switching frequency. However, the capacitance ratio seen by the inductor is $\begin{bmatrix} C & \frac{C}{2} & \frac{C}{2} & \cdots & \frac{C}{2} & \frac{C}{2} & C \end{bmatrix}$, which implies the duty ratio for each switching signals becomes $\begin{bmatrix} 1 & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \cdots & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 1 \end{bmatrix}$ at resonant frequency. Note this set the boundaries for the range of duty ratio when operating from resonant frequency to very high switching frequency.



(a) Hybrid SC type-I: single inductor

(b) Hybrid SC type-II: disctributed inductors

Figure 4.6: Optimal output impedance given fully customized switches, and the switch area constraint is $\sum G_{on} V_{rated}^2$.

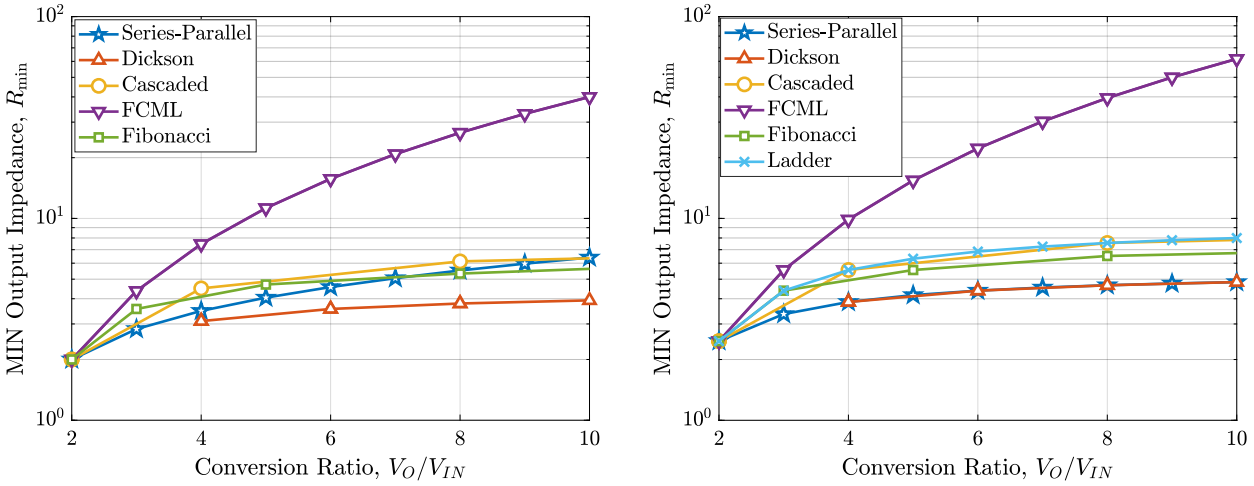
topology can be obtained as

$$\begin{aligned} R_{\min} = \min\left(R_{out}\right) &= \frac{1}{X_{tot}} \left[\sum_{i=1}^{N_b} \left(\sqrt{\sum_{j=1}^{N_p} \frac{\left(a_{r,i}^{j}\right)^2}{D_j}} \cdot V_{i,rated} \right) \right]^2 \\ &= \frac{1}{X_{tot}} \left[\sum_{i=1}^{N_b} \left(\sqrt{\sum_{j=1}^{N_p} \left(a_{sw,i,RMS}^{j}\right)^2} \cdot V_{i,rated} \right) \right]^2 \end{aligned} \tag{4.4}$$

through the Lagrangian optimization function [5]. Note the optimization process provided by (4.4) assumes all switches can be fully customized according to their RMS current and voltage rating. For instance, a switch has to be larger if its current and/or voltage rating is higher. In a special case where a two-phase operation and $D = 50\%$ are assumed, (4.4) can be simplified as

$$R_{\min}\Big|_{D=50\%} = \frac{1}{X_{tot}} \left[\sum_{i=1}^{N_b} \left(a_{r,i} V_{i,rated} \right) \right]^2, \tag{4.5}$$

which implies that the total average switch stress listed in Table 4.1 directly reflects $R_{\min}$ of each topology for both pure SC and hybrid SC type-II. For hybrid SC type-I, the general expression as (4.4) should be used due to the topology-dependent duty ratios. The topology comparisons of hybrid SC type-I and type-II are shown in Fig. 4.6 (a) and (b), respectively. It can be seen that these two cases have shown similar trend for all topologies, except that the ladder topology is only available to hybrid SC type-II. In particular, the Dickson topology always features the least R_{min} due to its low blocking voltage requirement and



(a) Hybrid SC type-I: single inductor

(b) Hybrid SC type-II: disctributed inductors

Figure 4.7: Optimal output impedance given the uniform V_{rated} switches, and the switch area constraint is $\sum G_{on}$ (V_{rated} is not considered due to unavailable voltage selection).

always-guaranteed multiple parallel paths (lower switch RMS current). The excellent switch utilization brought by Dickson topology is beneficial in on-chip integration, which not only saves die area for the same power loss but also accommodates for very high input voltage using low-V_{rated} devices.

Optimal Output Impedance for Uniform Switches

In high-power applications, solutions using discrete components are necessary as they not only provide switches with much higher VA rating and lower cost, but it is also attractive for its short time-to-market development. However, unlike full custom design provided by application-specific integrated circuit (ASIC), the discrete components do not support very fine-scale voltage and conductance selection, due to the limitations of commercially available packages as well as product strategies. An example is shown in Fig. 4.5: there is a design discontinuity for $V_{rated} < 25V$. Instead of having the switch area scaling with V_{rated}^2, the designs fell in that voltage domain are only able to employ uniform V_{rated} switches, and $R_{\min}$ can be optimized with a new area constraint for switches: $X_{tot,G} = \sum G_i$ with V_{rated} ignored. As a result, the topology performance considering only switch conductance is shown in Fig. 4.7, and it generates different results as compared to Fig. 4.6. While the Dickson topology is still showing the lowest R_{min} at high conversion ratios, others are emerging to show promising switch utilization. Fig. 4.7 implies that there are more selections available when dealing with low-voltage domain using discrete switches.

In most discrete implementations, minimal number of switches is primarily considered for the concerns of smaller and practical PCB, instead of accommodating with different current stress and achieving the optimal conductance ratio by fine tuning the number of parallel

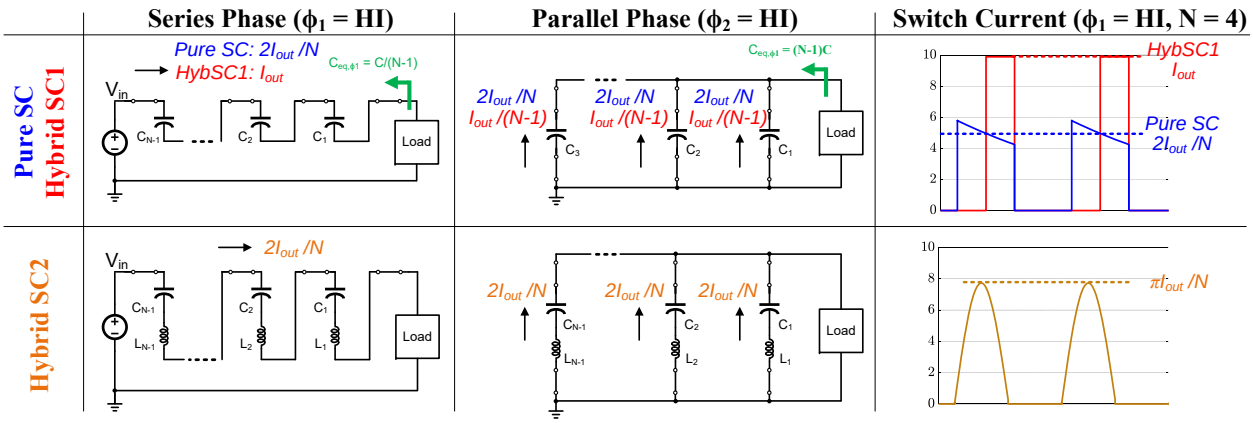


Figure 4.8: Switch current of an N-to-1 series-parallel topology.

Table 4.4: Conduction loss breakdown in an N-to-1 series-parallel topology.

	Pure SC	**Hybrid SC type-I (single L)**	**Hybrid SC type-II (distributed L)**
Critical Frequency	$\frac{1}{R_{\min,sc} \cdot NC}$	$\frac{\sqrt{N-1}}{\pi \cdot N\sqrt{LC}}$	$\frac{1}{2\pi \cdot \sqrt{LC}}$
Series Phase duty ratio	50%	$\frac{1}{N}$	50%
Series Phase, P_{cond} per switch (total switches $= N$)	$\frac{2}{N^2} {I_{out}}^2 R_{on}$	$\frac{1}{N} {I_{out}}^2 R_{on}$	$\frac{\pi^2}{4N^2} {I_{out}}^2 R_{on}$
Parallel Phase duty ratio	50%	$\frac{N-1}{N}$	50%
Parallel Phase, P_{cond} per switch (total switches $= 2N-2$)	$\frac{2}{N^2} {I_{out}}^2 R_{on}$	$\frac{1}{N(N-1)} {I_{out}}^2 R_{on}$	$\frac{\pi^2}{4N^2} {I_{out}}^2 R_{on}$
Minimum Output Impedance, $R_{\min}$	$\frac{2 \cdot (3N-2)}{N^2} R_{on}$	$\frac{N+2}{N} R_{on}$	$\frac{\pi^2}{8} \cdot R_{\min,sc}$

connected switches. Consequently, the switch area constraint degenerates and it is only related to the number of switches, $X_{tot,1} = \sum 1$. When comparing R_{out} between topologies, minimal number of uniform V_{rated} switches are applied throughout the whole converter and the number of switches for each topology is forced the same for fair comparison. For example, both series-parallel and Dickson topologies require $(3N-2)$ switches; rest of the topologies will also be implemented with $(3N-2)$ switches with some paralleled at higher RMS current paths, even though they originally require less switches.

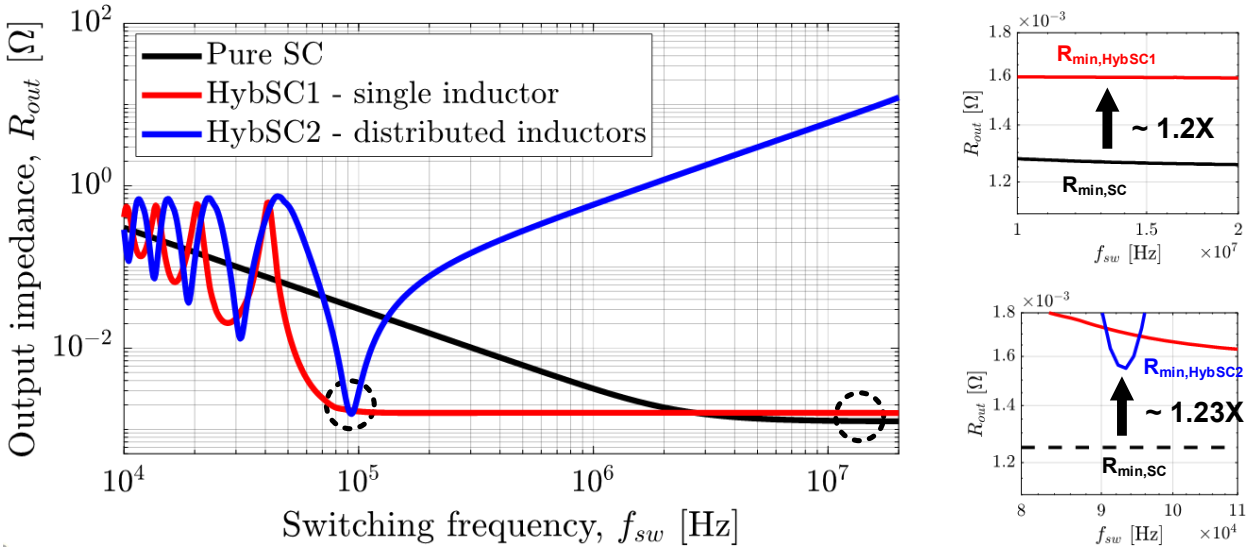


Figure 4.9: Output impedance of a 4-to-1 series-parallel SC topology with various soft-charging techniques.

To calculate R_{min} for the case of uniform-V_{rated} switches, the series-parallel topology is used as an example due to its simple operation. This topology either operates at series or parallel phase, and the switch current of an N-to-1 series-parallel topology for each phase is shown in Fig. 4.8. Both pure SC and hybrid SC type-II have an equal average current at all switches and phases, allowing $D = 50\%$ to maintain a balanced charge to the flying capacitors. In hybrid SC type-I, the output inductor behaves like a current source when operating at very high switching frequency, forcing the peak current flowing out from the switching node to be the same in both series and parallel phases. As a result, the switch current is forced to I_{out} in the series phase; while I_{out} is distributed to $(N-1)$ parallel branches in the parallel phase. To keep all flying capacitors balanced, a duty ratio of $\frac{1}{N}$ is needed for series phase. Table 4.4 provides a detailed conduction loss breakdown for an N-to-1 series-parallel topology, where all switches are uniform with R_{on}. Both pure SC and hybrid SC type-II has higher order in the denominator of their R_{min}, which means the conduction loss can be reduced as the conversion ratio increases because more parallel paths are added. As compared to that, $R_{\text{min},HybSC1}$ has equal order for its numerator and denominator, due to the higher power loss during its series phase. In hybrid SC type-I, even though the current through switches in the series phase only appears for an interval of $\frac{T_{sw}}{N}$, the current magnitude is meanwhile increased by $\frac{N}{2}$ as compared to the pure SC, leading to $\frac{N^2}{4}$ times increase in the loss. In the case of $N = 4$, $\frac{R_{\text{min},HybSC1}}{R_{\text{min},sc}}$ and $\frac{R_{\text{min},HybSC2}}{R_{\text{min},sc}}$ are respectively $\frac{6}{5}$ and $\frac{\pi^2}{8}$, matching the simulation result in Fig. 4.9. Following the same procedure as shown in Fig. 4.4, R_{min} for other topologies can be obtained. Note the duty ratios for other hybrid SC type 1 are as follows: Dickson — $\frac{N+2}{4N}$ and $\frac{N-2}{4N}$ for each main and auxiliary phases; FCML

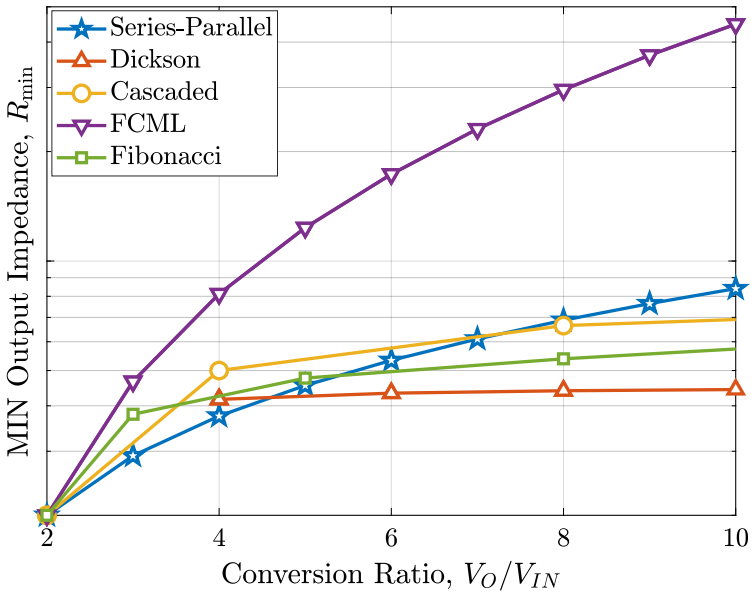


Figure 4.10: Optimal output impedance given the uniform V_{rated} switches, and the switch area constraint is $\sum 1$.

— $\frac{1}{N}$ with phase shift of $\frac{2\pi}{N}$ between switching signals; Fibonacci — $\frac{F_k}{F_{k+2}}$ or $\frac{F_{k+1}}{F_{k+2}}$.[4]

The optimal output impedance of various hybrid SC type-I using minimal amount of uniform switches throughout the converters is first shown in Fig. 4.10, with all derived $R_{\min}$ using the switch area when $N = 2$ (where $X_{tot} = 4G_{on}V_{out}$ or $4G_{on}$). As compared to Fig. 4.7, the switch utilization of all topologies, except FCML, becomes even closer to each other. In particular, the series-parallel topology shows low $R_{\min}$ at lower N. Even though the Dickson topology is still showing very good switch utilization, it can be observed the crossover point is around $N = 6$ for Dickson to have lower $R_{\min}$ than the series-parallel topology. Meanwhile, the series-parallel topology features the best capacitor utilization when considering the voltage derating factor of the flying capacitors, which can further reduce the passive requirement. As a result, it is potential that the series-parallel topology has excellent overall performance. A more general comparison considering both switch and passives utilization will be detailed in section 4.5.

[4]It is found that the deviation of duty ratio from 50% yields differences in minimum output impedance between conventional SCs and those hybrid SCs with a single inductor at their outputs. Note that higher R_{min} in hybrid SC does not necessarily suggest they have worse performance than the pure SC. Factors including operating frequency, passive selection and overall convert size should be considered. Therefore, a new figure of merit in section 4.4 and a comparison framework are proposed to compare different approaches.

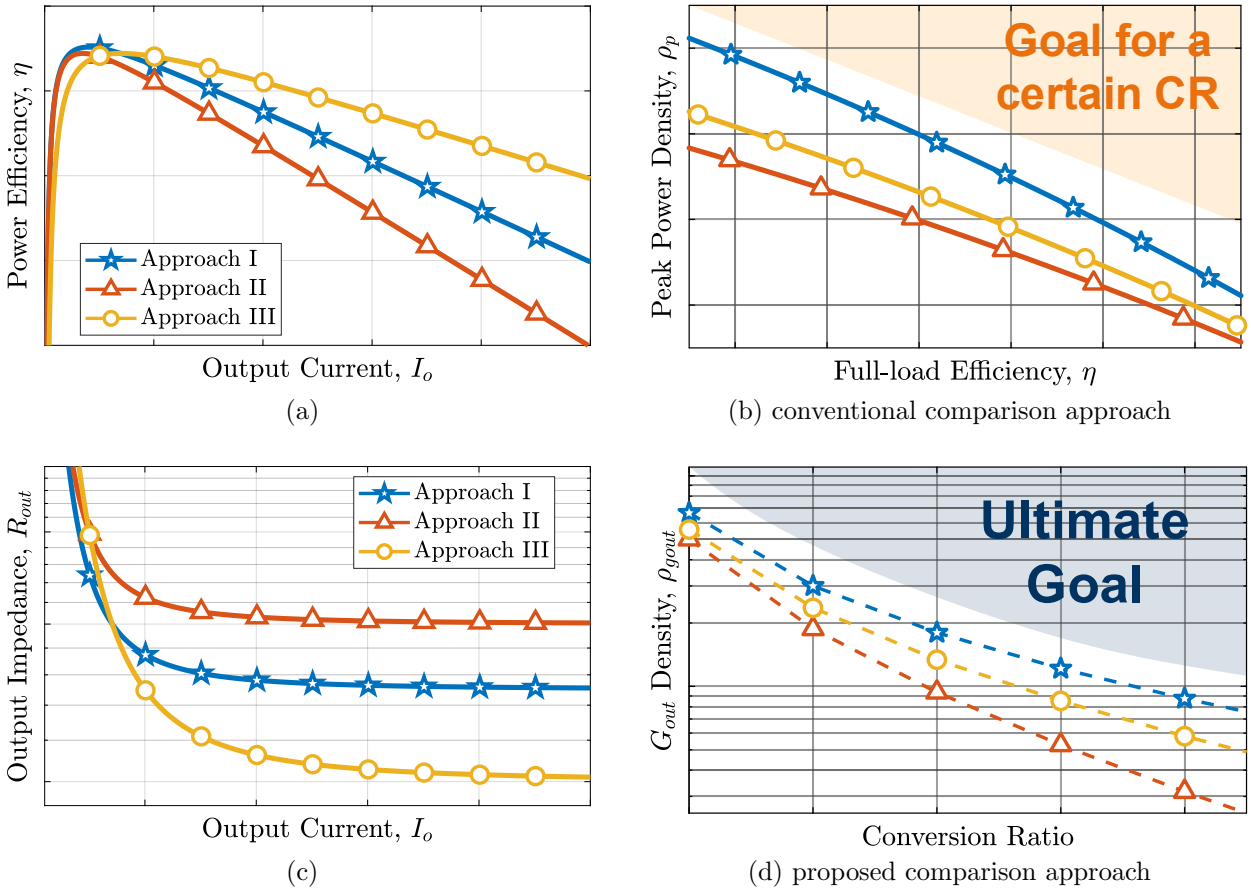


Figure 4.11: Development of the proposed figure of merit (FoM): (a) efficiency vs. output current, (b) conventional comparison approach - peak power density vs. full-load current, (c) output impedance vs. output current and (d) proposed comparison approach. Three different cases are exemplified, with the scenario as follows: i) Topology I and II have the same form factor but different performance, ii) dual-phase interleaved topology II has some advantage in passive reduction. All of the compared cases have the same input voltage and conversion ratio unless otherwise stated.

4.4 Output Conductance Density — Figure of Merit (FoM)

In this section, an FoM, combining efficiency and power density, is proposed and introduced to provide a simple selection guideline and design direction for converters. To illustrate how the proposed FoM is developed, three cases, including two topologies together with different interleaved phase numbers, are exemplified. For simplicity, single-phase Topology I and II are assumed the same volume with different efficiency performance at heavy load region. A dual-phase interleaved Topology II has lower conduction loss and more merged components,

hence improving the efficiency and power density as compared to its single-phase version. Based on these settings, the three cases are then evaluated and compared.

Conventionally, the most intuitive way to compare converters is by plotting their efficiency over output current, and higher efficiency is usually sought for the concerns of more energy saving and less thermal issues. A typical efficiency plot is shown in Fig. 4.11 (a), where the dual-phase Topology II seems having the best performance. However, when converter volume is concerned, this comparison is unclear until the power density is calculated. As a result, plots of peak power density versus full-load efficiency is suggested [29]. As shown in Fig. 4.11 (b), the dots for each compared case are mapped here from their heavy-load regions in Fig. 4.11 (a), where the output current is far beyond their peak efficiency points. Fig. 4.11 (b) shows that the top-right direction is where we want to pursue, and Topology I is superior than Topology II since it is able to achieve high power density and high efficiency simultaneously. For a given topology, it can be observed that there is a tradeoff between the two performance index, where a lower full-load efficiency is expected when pushing towards higher peak power density, and vice versa. It is usually up to designers' discretion to show their favorite converter performance by picking up one of the power density - efficiency pairs, even though the full-load condition is usually determined based on device specifications. Therefore, this comparison approach remains unclear if the trendline for each topology is not shown, especially for novel converters with only few numbers reported. In addition to that, the plot in Fig. 4.11 (b) does not have enough space for dealing with different conversion ratios.

In fact, the output impedance, which is the most intrinsic feature of a power converter, can help combine various performance index and fundamentally characterize a converter. First of all, the efficiency can be derived as

$$\eta = \frac{P_o}{P_o + P_{loss}} \approx \frac{V_o I_o}{V_o I_o + I_o^2 R_{out}}, \tag{4.6}$$

when operating at heavy load regions, including the full-load condition. With some manipulations of (4.6), the output impedance, R_{out}, can be represented by

$$R_{out} = \left(\frac{1}{\eta} - 1\right) \cdot \frac{V_o}{I_o}, \tag{4.7}$$

which is general to any case including non-regulated and regulated converters. By applying (4.7), R_{out} for different compared cases are shown in Fig. 4.11 (c). Focusing on heavy load region, R_{out} is almost constant attributed to the fact that the power loss is mainly dominated by the conduction loss, $I_o^2 R_{out}$. The reciprocal of R_{out} is the output conductance,

$$G_{out} = \frac{1}{R_{out}} = \frac{\eta}{1-\eta} \cdot \frac{P_o}{V_o^2}, \tag{4.8}$$

which better describe the performance, e.g. higher G_{out} is targeted. Normalizing G_{out} with the converter volume (including active semiconductor and passive components) gives us a

new FoM - the output conductance density

$$\rho_{gout} = \frac{G_{out}}{\text{Volume}} = \frac{\eta}{1-\eta} \cdot \frac{\rho_p}{V_o^2}, \tag{4.9}$$

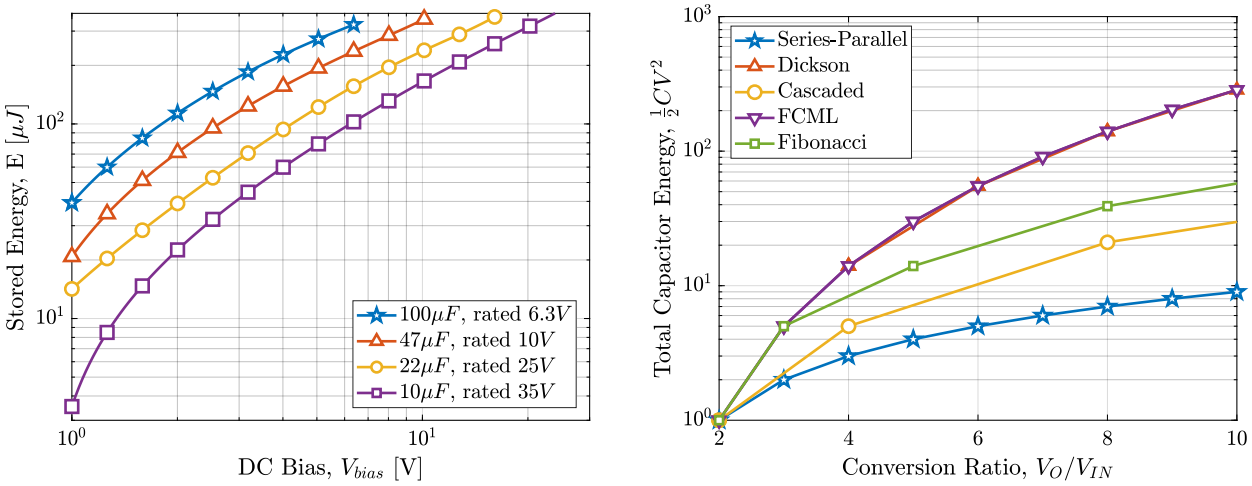
where ρ_p is the power density. As suggested by (4.9), ρ_{gout} intrinsically describes both efficiency and power density, and higher ρ_{gout} means better performance. Note that it is practical to assume the inductor current is not saturated and the device temperature coefficient can be ignored without hitting the thermal limit, since both of which decreases G_{out} and therefore lower ρ_{gout} can be expected.

With the assistance of ρ_{gout}, the information in Fig. 4.11 (b) can be shrunk and mapped to a more general plot shown in Fig. 4.11 (d). Therefore, a clearer roadmap is then laid out for the development of power converters. For a given topology, extending with more stages adds volume overhead, hence the conductance density decreases for increasing conversion ratios. This sets a performance limit for a certain topology moving toward high conversion ratios. Meanwhile, given a certain input voltage, the commercial device availability does not follow the common device scaling, e.g. $G_{on}V_{rated}^2$ for switches, as the conversion ratio goes up, aggregating the decreasing rate of ρ_{gout} trendline. This encourages a better strategy to extend to a higher conversion ratio with high ρ_{gout}, which will be discussed in section 7.

4.5 Topological Comparison Framework

To achieve the best output conductance density, we are looking for the optimal combination of switch and passive utilization. With the switch scaling trend shown in Fig. 4.5, the switch utilization for two extreme cases were investigated in section 4.3. On the other hand, the passive utilization considering the energy processed by inductors and capacitors was comprehensively analyzed in [14]. Unlike the switches, the capacitor scaling trend, $\text{Volume}_{cap} \propto CV_{bias}^2$, for low voltage (even down to around 0 V) can easily be supported by a survey like the one shown in Fig. 4.12 (a). Meanwhile, with the passives survey done in Fig. 2.6 and [13], it is reasonable to assume that the capacitor has much more energy density than the inductor. When $\rho_C \gg \rho_L$, the passive utilization considering both capacitors and inductors in [14] reaches the same results as the pure SC performance at SSL region, M_{SSL} dominated by the capacitor[5]. Without running into a complicated analysis, the passive utilization here is approximated by the total capacitor energy requirement shown in Fig. 4.12 (b) for a quick comparison. As can be seen, there is a tradeoff between switch and capacitor utilization, and it shows an opposite trend to the switch utilization with full switch customization shown in Fig. 4.6. Designing solely based on either switch or passive utilization may result in suboptimal overall performance. For instance, the Dickson topology has the

[5]The concept of passive utilization is the allowable capacitor voltage ripple as well as the inductor current ripple. The general analysis for hybrid SC in [14] was from the energy point of view, while the specific case for pure SC in [5] was based on power consumption. Both [14] and [5] provide the optimization with respect to the volume and with the capacitor volume proportional to their stored energy.



(a) Survey of discrete multilayer ceramic capacitors (MLCC).

(b) capacitor energy requirement

Figure 4.12: Capacitor scaling (Data points are from active Murata products in 0805 SMD package (2 mm x 1.25 mm x 1.25 mm) [65]. Same package is selected for fixed capacitor volume and fair comparison.) and capacitor energy requirement.

best switch utilization, but worse passive utilization. The overall performance is unclear until both switches and passives are considered. Therefore, the output conductance density is used to provide a more holistic view for the whole converter.

A comparison framework based on the output conductance density shown in Fig. 4.5 is developed. Per the model in [14], all topologies can be simply assumed the same resonant frequency with different passive volume requirement by each topology. In a practical PCB layout, the optimal passive volume will be attempted, meaning the inductor and the capacitor will have similar volumes, assuming the energy density of capacitors is 100 times better than that of inductors. For the switches, same switching frequency is applied for their minimum output impedance, given the same resonant frequency. Meanwhile, all topologies are using the same area of switches, generating the same switching and gate driver loss which are not captured by the output impedance are equalize. However, there is a missing link between the passive and switch volumes. This will not be understood until the practical PCB layout is considered. As a result, the best layout of three popular topologies, series-parallel, Dickson and cascaded with the same conversion ration are considered as the examples in the next section. Finally their output conductance density is calculated and compared.

4.6 Practical Layout Consideration

In this section, three topologies with a native conversion ratio of 4-to-1 are implemented using uniform switches. Fig. 4.14 shows the top view of PCB layout for each topology. For all layout, high power components are placed on the top layers for immediate heat transfer, and

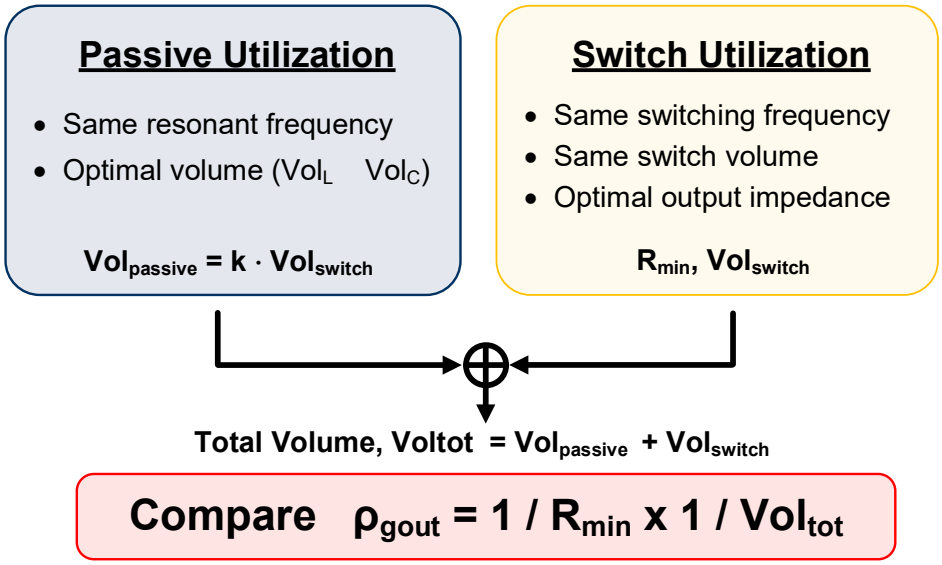
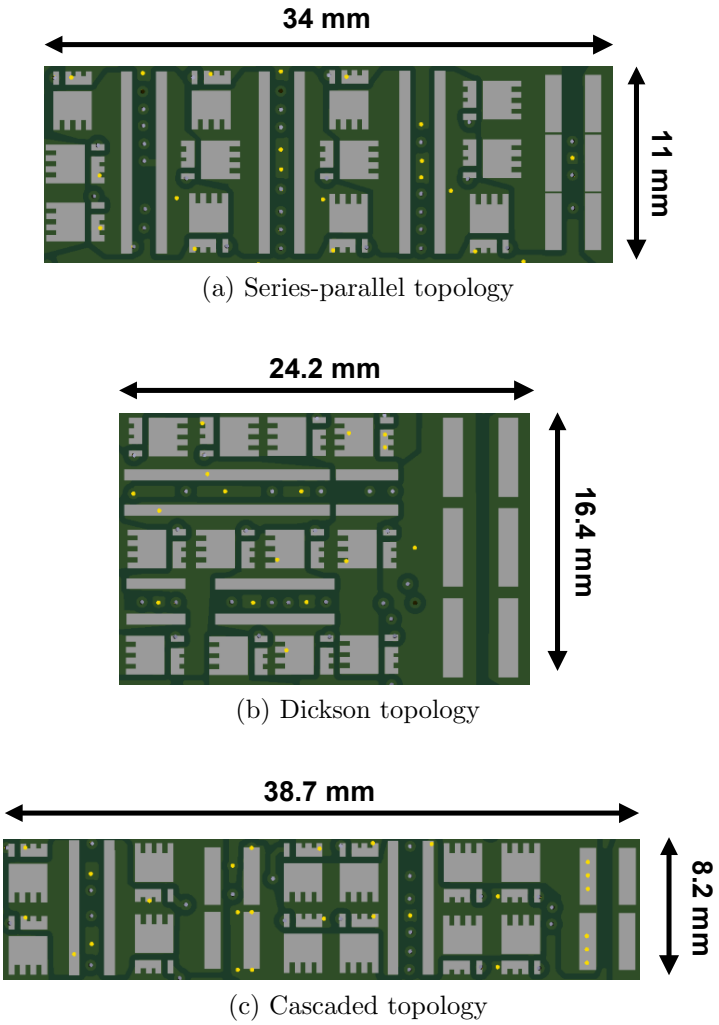


Figure 4.13: Comparison framework using output conductance density.

auxiliary circuit including gate drivers is right beneath the power components for maximal use of prototype volume. All topologies have the same 12 total power switches, together with soft-charging technique of using inductor at the output. Based on the topological comparison framework shown in Fig. 4.13, the selection of the passive components is listed in Table 4.5. Before selecting the flying capacitance, the equivalent capacitance, C_{eq}, is first calculated as that determines the actual resonant frequency. The selection criteria for passive component also includes the output inductor DC resistance as well as saturation current. The rated current of each topology is set high enough to show their switch utilization at heavy load region. Altogether, the passives size is determined based on the practical layout consideration of each topology.

Series-Parallel Topology

This topology has the best passive utilization, thanks to its high C_{eq} and the low voltage stress to all the flying capacitors. Since all capacitors have the same voltage stress, they can have the same size without considering voltage derating factor, allowing this topology to have very symmetric and tight layout for the capacitors and therefore a very compact size. In addition, the high passive utilization also enables low profile output inductor with lower inductance but higher saturation current. In the case of uniform switches, the layout for the switches can be very organized together with the flying capacitors. The power path is direct from input to output with no vias required, significantly reducing the conduction loss on PCB connection. The only downside is the higher current path of the series-phase switches, which requires more attention as it causes not only parasitic inductance but also resistance. The series-phase switches have $(N-1)$ times the conduction loss as compared



(a) Series-parallel topology

(b) Dickson topology

(c) Cascaded topology

Figure 4.14: PCB layout of 4-to-1 hybrid SC type-I topologies.

to the parallel-phase switches. As a result, after placing the 10 necessary switches in series-parallel topology, the two empty spaces can be filled up with switches in parallel with the series-phase switches. For even higher current application where thermal issues are more critical, a simple way to address it is by extending the middle parts with more series-phase switches in parallel to evenly spread out the heat. The layout of the series-parallel can be extended easily by adding more columns for higher conversion ratios, together with more rows for the middle series switches. Overall, the layout can be compact with high output current rating.

Table 4.5: Passive component selection for each topology when $V_{in} = 24V$ and $V_{out} = 6V$.

	Series-Parallel	**Dickson**	**Cascaded**
C_{eq} seen by output inductor	$\frac{N^2}{4(N-1)} \cdot C$	$< \frac{(N+2)^3+(N-2)^3+2(N-4)^{\frac{3}{2}}}{16N^2}$	C
Flying Capacitor	GRM21BR61A476 @ 6 V $C_{fly1,2,3} = 11.98\mu F \times 9$ $C_{eq} = \frac{4}{3}C = 144\mu F$	GRM21BR61E226 @ 18 V $C_{fly3} = 2.49uF \times 28 = 70\mu F$ GRM21BR61E226 @ 12 V $C_{fly2} = 3.94\mu F \times 18 = 71\mu F$ GRM21BR61A476 @ 6 V $C_{fly1} = 11.98uF \times 6 = 72\mu F$ $C_{eq} < 1.2C = 85\mu F$	**Stage II** GRM21BR61E226 @ 12 V $C_{fly2} = 3.94\mu F \times 12 = 47\mu F$ **Stage I** GRM21BR61A476 @ 6 V $C_{fly1} = 11.98uF \times 12 = 144\mu F$
Output Inductor	XAL 4014-331 330 nH / 3 in parallel $L_{eq} = 110nH$ $DCR_{eq} = 3.3m\Omega$ $I_{sat} = 43.8A$	XAL 5020-801 800 nH / 3 in parallel $L_{eq} = 267nH$ $DCR_{eq} = 3.4m\Omega$ $I_{sat} = 36A$	**Stage II** XAL 4020-601 600 nH / 2 in parallel $L_{eq2} = 300nH$ $DCR_{eq} = 4.75m\Omega$ $I_{sat} = 20.8A$ **Stage I** XAL 4020-201 200 nH / 2 in parallel $L_{eq1} = 100nH$ $DCR_{eq} = 1.52m\Omega$ $I_{sat} = 39.4A$
Resonant Frequency	40 kHz	35 kHz	42 kHz

† Capacitors are selected from Murata Manufacturing Co., Ltd. and inductors are from Coilcraft, Inc.
‡ Note that C_{eq} of Dickson is around $1.1C$ from the simulation result, depending on the output current.

Dickson Topology

As opposed to the series-parallel topology, the Dickson topology has the best switch utilization with more evenly distributed current in each switch. Even though a higher current path happens at those switches operating in only main phases for split-phase control, the conduction loss ratio between highest and lowest current path is only $\frac{2(N-2)}{N}$ with a boundary between 1 and 2 as the conversion ratio increases. Meanwhile, the topology can sustain a very high input voltage with low rating devices, which is especially good for high voltage

applications when the device selection is limited to low-voltage domain, such as chip integration. However, the excessive voltage stress is indeed transferred to the capacitors, and each flying capacitor sustains different voltage derating factors, complicating the layout since the number of capacitors for each branch varies significantly. Meanwhile, it is hard to predict the resonant frequency as well as the suitable duty ratio in achieving complete soft charging through split-phase control. Therefore, while selecting the passive components and comparing topologies, the resonant frequency is set lower for the Dickson to avoid incomplete soft charging. Even though capacitors with low derating factor like C0G and NP0 can be used, they require a lot more space and that lowers the converter power density. In short, this topology can be very useful when the cost of switches are critical. However, the overall layout is mainly dominated by the highly skewed capacitor size ratio, resulting the power path routing in a less organized or modular fashion; therefore, lower power density is expected.

Cascaded Topology

The cascaded topology has the most modular layout as long as the devices follow the general scaling trends of GV^2, CV^2 and LI^2 for switches, capacitors and inductors, respectively. For example, when stepping up one more stage in the cascaded topology, the inductance can be increased by 4 times and the capacitance can be decreased by 4 times, giving the same LC size since the inductor current is halved and the capacitor voltage is doubled at the same time. When the general scaling trends are closely followed, the cascaded topology does not only have the same size for each stage, but also features the same resonant frequency for each stage due to the same LC constant. Similarly, the switch conductance of each stage can be scaled down by 4 times, as the voltage rating doubles at the higher voltage stage, resulting in the same size of switches as well as the same conduction loss for all stages. For higher conversion ratio, the module can be simply extended without changing the layout but the replacement of devices with various ratings. Also the conversion ratio increases quadratically with the number of stages, providing a very size-efficient way. However, as the switch is not scaled as GV^2, e.g. discrete switches at low-voltage domain, the layout of the cascaded topology using 2-to-1 ReSC becomes non-modular. Given the uniform-V_{rated} switches, more switches have to be in parallel for the lower voltage stage, making more difficult to achieve compact and rectangular converter prototype. Consequently, suboptimal overall performance is expected in the low-voltage applications.

4.7 Chapter Summary

Various SC topologies, including series-parallel, Dickson, cascaded, flying-capacitor multilevel (FCML), ladder and Fibonacci, with higher conversion ratios are generated and synthesized through a fundamental SC cell. The synthesized SC topologies can be turned into hybrid SC by using soft-charging techniques; particularly, the output regulation capability is found available to the soft-charging technique with inductor at the output. A quantita-

Table 4.6: Topologies employed in the rest of the chapters.

Chapter	Topology	Application	Advantage	Challenge addressed
5	4-to-1 Hybrid Dickson (regulated output)	Li-ion battery to computing loads in mobile devices	Best switch utilization	Off-chip capacitor are co-packaged with a FCBGA
6	3-level Boost (output regulated)	Energy harvesting in wireless sensor network	Wide voltage regulation	Flying capacitor voltage balancing by ACC-PFM technique
7	Two-stage ReSC (non-regulated output)	Direct point of load in data center	High performance for very high conversion ratio	Optimal selection of topology based on voltage domains
8	Interleaved Cascaded (non-regulated output)	Intermediate bus voltage in data centers	Extremely high efficiency and high power density	Passive component reduction

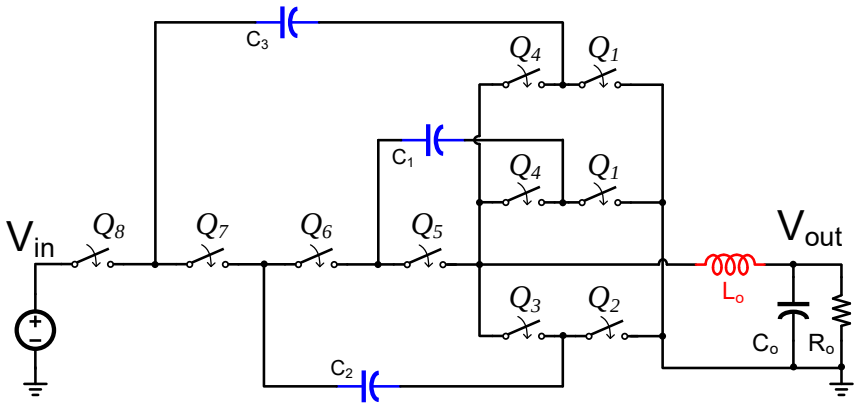
tive method is built up to analyze the switch utilization, which is by calculating the exact minimum output impedance, R_{min}. The distinctions in R_{min} between pure SC and hybrid SC converters are found related to the deviations in their duty ratios and current amplitudes. Given the survey of available devices, three progressive optimization results for R_{min} are derived, which include area constraint of $\sum G_i V_{i,rated}^2$ when very fine-scale switch rated voltage and conductance can be selected, together with $\sum G_i$ and $\sum 1$ in low-voltage domain applications where switches do not scale with V_{rated}. The comparison shows that each topology serves their purpose in different applications. When the full switch customization is available, the Dickson topology has the lowest minimum output impedance. Yet, when only the switch conductance or only the minimal number of switches is considered , other topologies demonstrate promising results. A comprehensive comparison framework is developed, considering both passive and switch utilization, to analyze the overall performance of each topology. Recommended layouts, creating links between switch and passive volumes, provide the shortest power paths for switches and passives and they can be easily extend to a more general case where switch is scaled with voltage. In the case of uniform switches, the series-parallel has the highest output conductance density due to its excellent switch and passive utilization as well as symmetric layout. As listed in Table 4.6, several different topologies are designed, fabricated and measured in each chapter with their specific advantages for different applications. In addition, Table 4.6 also lists their challenges, which will later be addressed.

Chapter 5

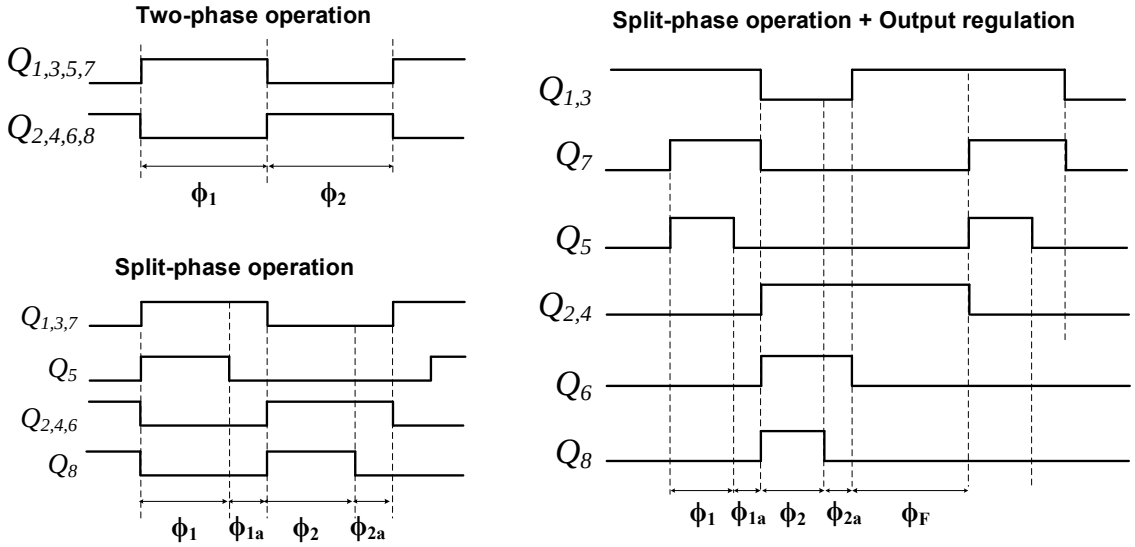
On-Chip Hybrid Dickson for High Switch Utilization

Owing to the need for low power consumption, portable and wearable electronics operate at low voltages, typically below 1 V, with recent designs in near- and sub-threshold operation down to 0.3-0.5 V. Meanwhile, voltage range of the most common energy source, the Li-ion battery, is 3 - 4.2 V. Likewise, a common bus voltage on motherboard is 12 V, which needs to be converted to 3.3 V or 1.8V before supplying the power to the point-of-load regulator for processors. These applications motivate the need for compact power converters capable of large conversion ratio with wide and efficient voltage regulation. Meanwhile, as the CMOS technology node advances, the voltage ratings of available switches are also decreased down to 1 V for core devices and up to 2.5 V or 3.3 V for I/O devices. To interface between the source and the load, cascoded switches are unavoidable for power converters, e.g. stacked-switch buck converter, SC as well as hybrid SC. The Dickson topology with an inductor at its output is an excellent candidate due to its superior switch utilization.

In this chapter, a 4-to-1 hybrid Dickson converter is proposed and implemented. Its soft-charging operations by two-phase and split-phase controls are investigated, along with its extended regulation capability; the duty ratio variation in the split-phase control is also discussed in terms of operating frequency, output current and capacitance variations. The converter is implemented using 65 nm CMOS process with careful selection on the voltage rating and sizing of all power MOSFETs. In addition, The specifications for die bumping in the IC fab as well as the interposer fabrication in the back-end service are covered for a prototype co-packaging a flip-chip ball grid array (FCBGA) converter die, an interposer and passive components. Other than the packaging, to operate the converter in a more reliable, area-efficient and power efficient, several key circuit techniques including floating supplies and gate driver techniques are evaluated and developed, which are also common technical issues and applicable to other power converters. As compared to prior arts, the proposed converter outperforms in efficiency, power density and conversion ratio.



(a) a 4-to-1 hybrid Dickson converter by adding an inductor at the output



(b) switching signals

Figure 5.1: A 4-to-1 hybrid Dickson converter and its switching signals.

5.1 Operating Principle

A hybrid Dickson converter can be either operated with two or split phases, with a 4-to-1 example shown in Fig. 5.1. These two types of operations can also be added with an output inductor freewheeling phase to obtain flexible regulation capability. As shown in Fig. 5.2, there are five operational states given the switching signals in Fig. 5.1: ϕ_1 and ϕ_2 are the main states shared by the two-phase and split-phase operations; ϕ_{1a} and ϕ_{2a} are the additional states only in split-phase operations; ϕ_F is the freewheeling state where the bottom switches controlled by Q_{1-4} are turned on and grounded. Note the current branches are always guaranteed as many as possible (two in the 4-to-1 case) in the main phases,

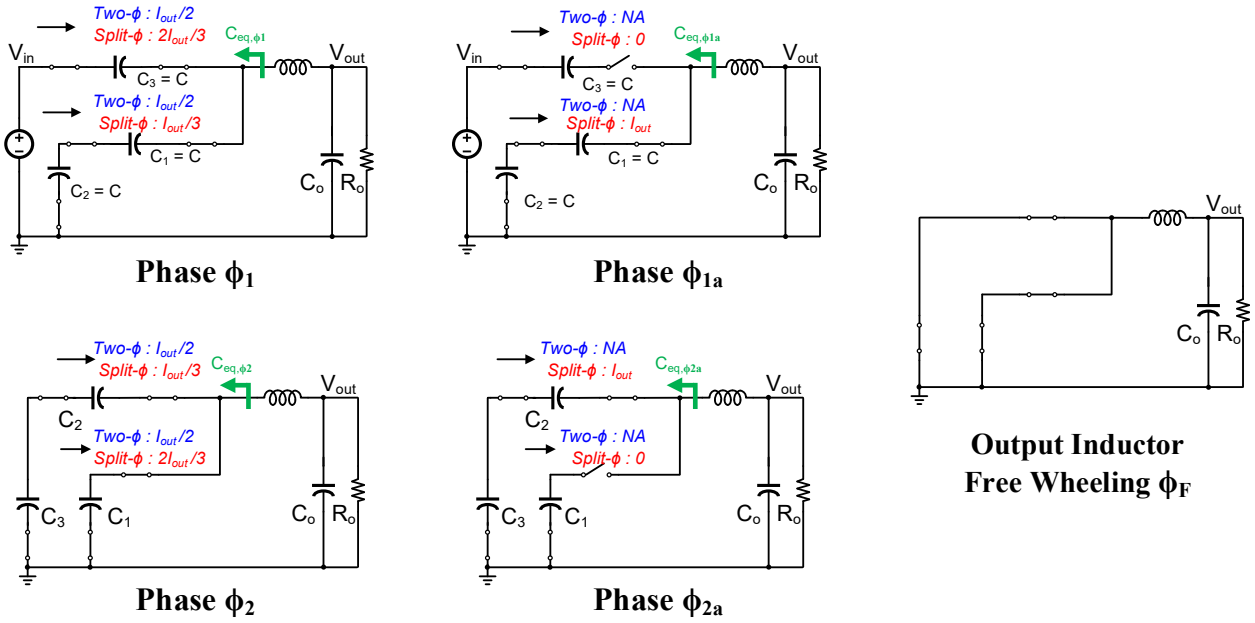
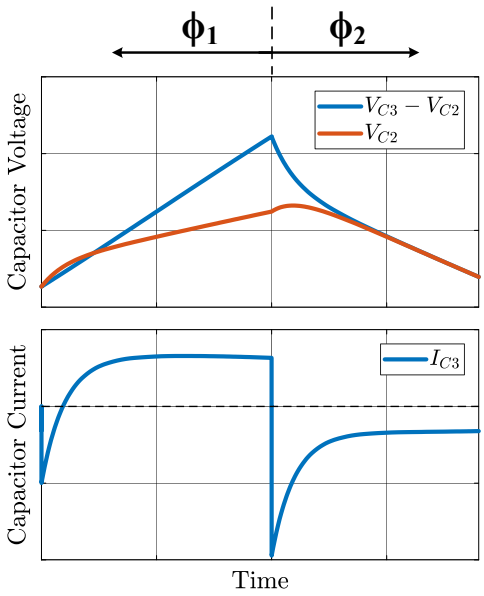


Figure 5.2: Operational states of a 4-to-1 hybrid Dickson converter.

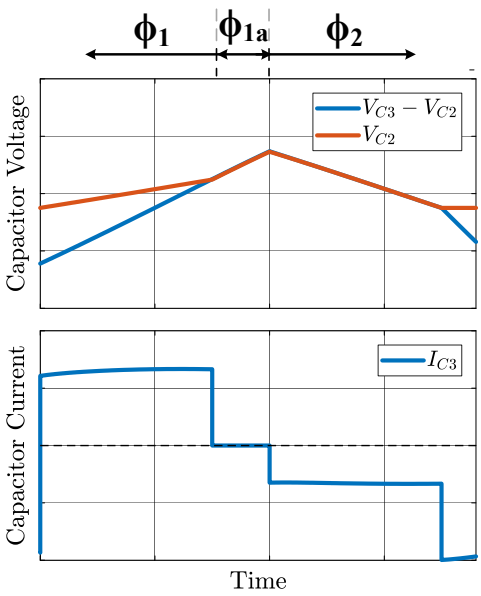
reducing the switch RMS current and benefiting the Dickson converter from excellent switch utilization.

In the two-phase operation, the duty ratio is usually set as 50%, which is similar to the conventional pure SC. However, given uniform capacitance for all flying capacitors[1], there is voltage difference between capacitor branches when they are connected, leading to a high spiky current due to the residual charge sharing loss. Fig. 5.3 (a) shows the example when the Dickson converter transitions from ϕ_1 to ϕ_2, and the voltage of capacitor branches for ϕ_2 is monitored. It can be seen the voltage difference between $(V_{C3} - V_{C2})$ and V_{C1} when ϕ_2 is on leads to the spiky current in all flying capacitors (I_{C3} is shown as an example). To address that, The split-phase control adds two auxiliary phases before transitioning into the main phases, allowing the voltage difference between capacitor branches to be eliminated before they are connected. With the auxiliary phases, the capacitor current becomes smooth as shown in Fig. 5.3 (b). The output impedance in Fig. 5.3 (c) clearly shows the difference between the split-phase and the two-phase operation, where the split-phase control has a lower critical frequency and a lower switching frequency is allowed to achieve the minimum output impedance. However, there is a tradeoff: the split-phase operation has higher R_{min} than that of two-phase operation, since there are less parallel branches involved in the auxiliary states. The ratio between switching and conduction loss determines whether split-phase operation is worth implementing; the answer is yes when the converter efficiency

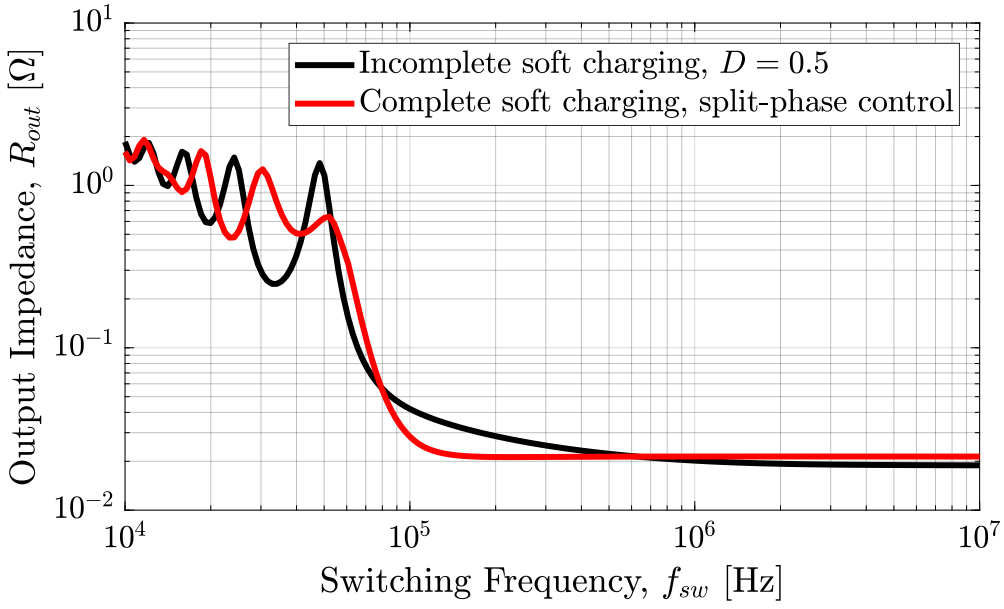
[1]The flying capacitance ratio can also be set highly skewed to approximately achieve soft-charging operation according to [54], which is to set the even numbered flying capacitance to be much higher.



(a) Two-phase: incomplete soft charging



(b) Split-phase: complete soft charging

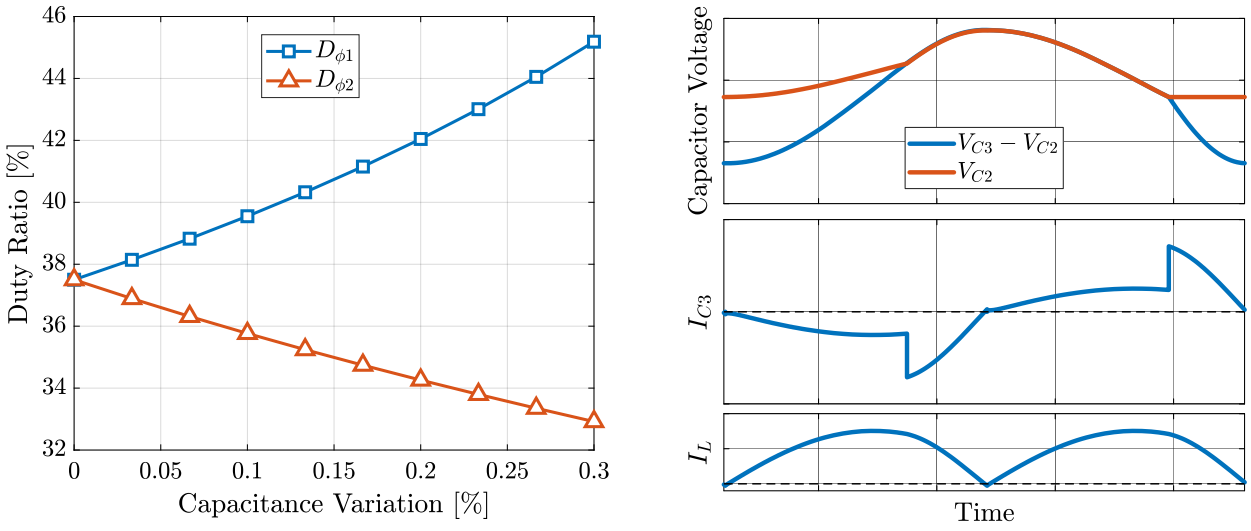


(c) Output impedance of two-phase and split-phase operations.

Figure 5.3: Comparison between two-phase and split-phase operations.

is dominated by switching loss.

For the output regulation, the split-phase control together with the freewheeling phase is illustrated in Fig. 5.1 (b). The duty ratios of main and auxiliary phases are combined into D_{reg}, i.e. $D_{reg} = D_{\phi_1} + D_{\phi_{1a}} + D_{\phi_2} + D_{\phi_{2a}}$, which determines the output voltage by $V_o = D_{reg} \cdot V_{in}/4$. The required inductance in the 4-to-1 hybrid Dickson converter can be



(a) Duty ratio versus capacitance variation

(b) Resonant operation

Figure 5.4: (i) Duty ratio variation and (ii) resonant operation of split-phase control when complete soft-charging operation is achieved.

derived by:

$$L_{\text{4-to-1 Dickson}} = \frac{V_o \cdot (1 - D_{reg})}{\Delta I_L \cdot f_{sw}}, \tag{5.1}$$

which has similar form as the inductance for the buck converter except that D_{reg} is now four times bigger since the switching node voltage is approximately $V_{in}/4$. As a result, the inductance requirement is greatly reduced for the same inductor current ripple. Note adding the freewheeling state does not change the switching frequency for all control signals, since it is generated by extending the switching signals, Q_{1-4}.

For split-phase control, the ϕ_1 duty ratio to achieve complete soft charging is 37.5% (4-to-1 case) in the split-phase operation when the inductor current is relatively flat at high switching frequency. The duty ratio varies with the flying capacitance ratio as well as the switching frequency. Fig. 5.4 (a) shows how the duty ratio varies with the capacitance ratio, where the variation of flying capacitance is defined as the increasing rate of C_1 and the decreasing rate of C_3. Note that $D_{\phi_1} + D_{\phi_{1a}} = D_{\phi_2} + D_{\phi_{2a}} = 50\%$ is always true since the equivalent circuit for $\phi_1 - \phi_{1a}$ and $\phi_2 - \phi_{2a}$ are the same. On the other hand, the duty ratio decreases with lower switching frequency since the current amplitude going through each capacitor is not flat any more. Fig. 5.4 (b) shows one example of low switching frequency, which requires a duty ratio of 34.7% for a complete soft-charging given all flying capacitances are the same. Note that there is only one duty ratio at a specific operating frequency and current for simultaneously achieving resonant and complete soft charging operation. In other words, there are still more design margins to optimize the performance of the Dickson topology, requiring further research in simplified modeling and control. However, in this

Table 5.1: Characterization of n-channel devices in 65 nm CMOS process.

Device†	Channel Length	Voltage Rating	Channel Resistance $R_{ds} \cdot W$ $[\Omega \cdot \mu m]$	Parasitic Capacitance C_{gg}/W $[fF/\mu m]$	Leakage current	Layout Area‡
Core 1 V	1X	1X	1X	1X	1X	1X
I/O 1.8 V	1.8X	1.8X	3.2X	1.7X	0.02X	4.5X
I/O 2.5 V	1.9X	2.5X	3.0X	1.9X	0.02X	6.5X
I/O 3.3 V	2.6X	3.3X	4.9X	3.8X	0.02X	12.5X

† Corresponding p-channel devices have 3X higher resistance and 2X smaller leakage current.
‡ The actual layout includes spacing between the poly gate and metal contact. The actual layout length ratio deviates from the channel length, which should be corrected as [1X, 2X, 2.1X, 2.5X]. For the same conductance. All are tested with the same width. The difference is based on the number of multipliers.

chapter, the hybrid Dickson converter is operated at higher switching frequency where a more ideal situation of flat current can be assumed.

5.2 Power MOSFET Selection

The switch device ratings for Dickson topology are V_o and $2V_o$. Given the input voltage of 4 V and a the conversion ratio of 4-to-1, the nominal switch blocking voltage is either 1 V or 2 V. As listed in Table 5.1, there are mainly four regular-V_{th} devices in a 65 nm CMOS process. The most important design parameter is the voltage rating, which is usually selected 50% higher than their nominal blocking voltage for better reliability. Meanwhile, the characterization of the channel resistance as well as the parasitic capacitance are crucial for efficiency evaluation. For instance, a power converter processing higher current requires larger switches for lower resistance, but they are not able to switch too fast due to high parasitic capacitance. In order to quickly calculate the device widths and lengths, the channel resistance and parasitic capacitance are normalized to the channel width, assuming the minimum length is used for the lowest overhead on size and capacitance. While extracting the parasitic capacitance through gate driver loss, both the gate capacitance, C_{gg}, and the leakage current, $I_{gg,leak}$, should be considered:

$$P_{gate} = C_{gg} V_{DD}^2 f_{sw} + D \cdot I_{gg,leak} V_{DD}. \tag{5.2}$$

As can be seen from Table 5.1, the leakage current increases significantly as the gate length shrinks down to sub-100 nm regime. Literature also shows that the leakage current becomes a serious concern for the gate oxide thickness below 20Å in advanced CMOS processes [66]. Considering high leakage current for large power MOSFET and narrow allowable gate swing

range for driving (limited margin between the breakdown voltage and V_{th}) in core devices, the I/O devices are chosen for power MOSFET, especially for floating switches.

The chip area can be estimated through the channel area. Empirically, the actual chip area is about 3 to 4 times the total channel area depending on the design rules for each device. After considering the area overhead including M1-to-diffusion contacts, contact spacings, metal wires, and guard rings[2], the layout area ratio between different is approximately proportional to V_{rated}^2 given the same conductance, echoing the scaling trend for discrete switches at their higher voltage domain, $V_{rated} > 40V$. Other than designing the channel for power MOSFET, its fanout to the upper metal layers is critical as well since the lowest metal layer, M1, being the thinnest and narrowest, can contribute a large portion of resistance. The area ratio between the channel and the interconnection in a power switch unit should also be taken into consideration. For example, the switch channel occupies only a proportion, k, of a power switch unit area, and an empirical k value is from 0.2 to 0.3 for a balance between switch conductance density and gate capacitance density; otherwise, the switch resistance may be dominated by the metal resistance, e.g. more than 50% conduction loss coming from outside the gate channel was found when only one contact column is employed between the gate channels. Increasing the channel width without considering its ratio between M1 width and contact results in low conductance density as well as large gate capacitance. To further improve the quality of power MOSFET, not only the layout for M1 and contact is important, but also the number of vias on the higher metal layers. A grid-style layout of every metal layer perpendicular to its adjacent layer is usually employed, with the number of vias added as many as possible. Last but not least, the thickest top metal or redistribution layer is a great resource to reduce interconnection resistance.

5.3 High-Density Packaging

The form factor of a power converter is very crucial to power density, and the target is to package switches and passives into an optimal box volume. While the fully integrated switches have been mature enough for their high conductance density and wide variety of voltage scaling, the passives size is still the bottleneck preventing the power converter from achieving high power density. In most cases, the profile of the inductor determines the height of the whole package, resulting in a larger box volume. Several solutions were developed including the on-chip air-core spiral inductors [15], [49], off-chip air-core wirebond inductors [18] and co-packaged magnetic-core inductor [17], [38], [48], [67]. The co-packaged inductors can be full custom inductors like racetrack [17] and self-rolled up membrane (S-RuM) [68], or commercial ones [38], [48]. Nevertheless, the final goal is to integrate the inductor device into commercial IC fabrication processes, so that the inductor can be part of the "printing" functional layers. While the bottleneck of the inductor might be the expensive

[2]Guard rings are crucial for power switches to avoid latch-up issues. For hybrid SC, most of the power switches are floating and the deep N-well layer is needed to form an isolated P-well for NMOS, leading to some layout area overhead.

magnetic material in forming the core, the price is expected to be reduced significantly as the demand of high performance converter increases. This momentum of pushing inductor into nominal process does not only exist in the academics, commercial products are also moving their system in package (SiP) [69] from requiring an additional small substrate (fabricated by a back-end company) to the fully integrated solutions (all fabrication done in IC fab) [22]. All approaches are to find a balance between the fabrication cost, efficiency and form factor. There were also many ways to reduce the inductance requirement such as resonant operations, multi-phase interleaved converters and coupled inductors. In this chapter, the introduced hybrid Dickson converter has the advantage of very low inductance required, and it is chosen to have the inductor co-packaged with the power switches in FCBGA package through a high density interposer. The details of the whole packaging are provided as follows.

Power Switches packaged in FCBGA

The connection between the chip and the outside world is usually done by bond wire. However, the length of the bond wire can easily go more than 5 mm, leading to high parasitic inductance of 5 nH given the empirical 1 nH/mm for wire with a diameter of 1 mil. This causes significant ringing and reliability issues, which is especially serious when dealing with high switching frequency and high current. To address the issue of long interconnection, the developed chip can be flipped and directly connected to the outside world with small die bumps. As shown in Fig. 5.5 (a), an interposer is used to transfer the electrical connections from die bumps to the larger pads of the capacitors. In some cases, the capacitor can be directly soldered to the die bumps to achieve an even smaller height for the whole converter, as long as the bumps are large and distant enough [48]. A typical analysis of package parasitic inductance is shown in Fig. 5.5 (b), and Table 5.2 provides an estimation for the values based on the dimensions for each layer. It can be seen the parasitic inductance using FCBGA package can be reduced by 10 times as compared to packages using wirebond. The FCBGA package does not only help reduce parasitics including inductance and resistance, but it also reduces the converter size; beneficial in achieving high efficiency and high power density.

For the implemented hybrid Dickson converter chip, the die bumping was done in Taiwan Semiconductor Manufacturing Company (TSMC). While the bump pitch and size available in the TSMC process are very wide range, it is highly suggested to have larger bumps and spacings in order to ease fabrication constraints on the interposer. Larger bumps also help component assembly, avoiding annoying shorts between pins. For the implemented chip, the bumping process at the IC fab requires an incremental fee of \$10,000++ for production of the solder-bump mask and additional \$8,500++ shared cost of purchasing the flip-chip wafer. These fees are independent of the die area as it is an additional service upon request. Therefore, it could be cheaper if more projects shared the cost for the additional masks in the whole wafer. Even though several other back-end services provide bumping process, they require un-diced wafer or mass production. Another cost-effective way is cutting a shallower bond wire so that the bump associated with bonding action is then formed on top of the pad, which can be a very good alternative to the TSMC bumping service. This bumping

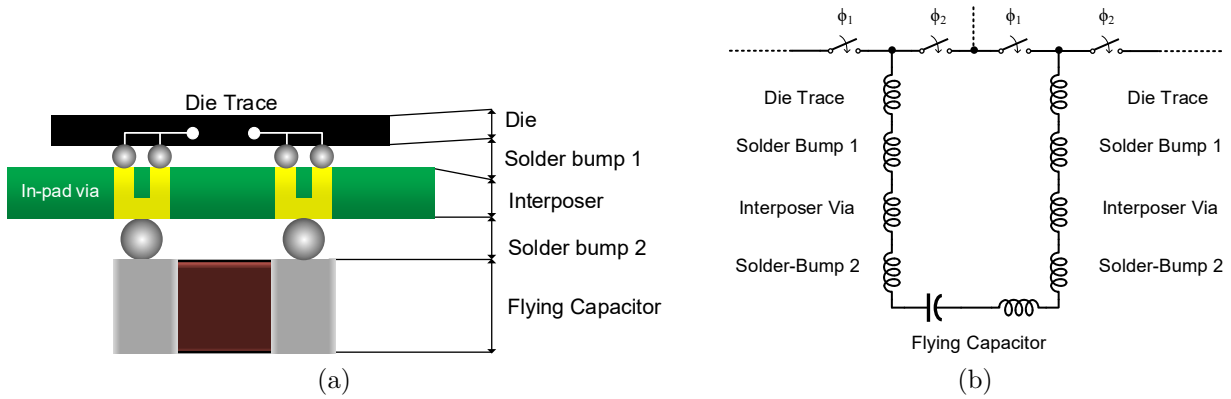


Figure 5.5: Parasitic inductance of a power converter using flip-chip ball grid array (FCBGA).

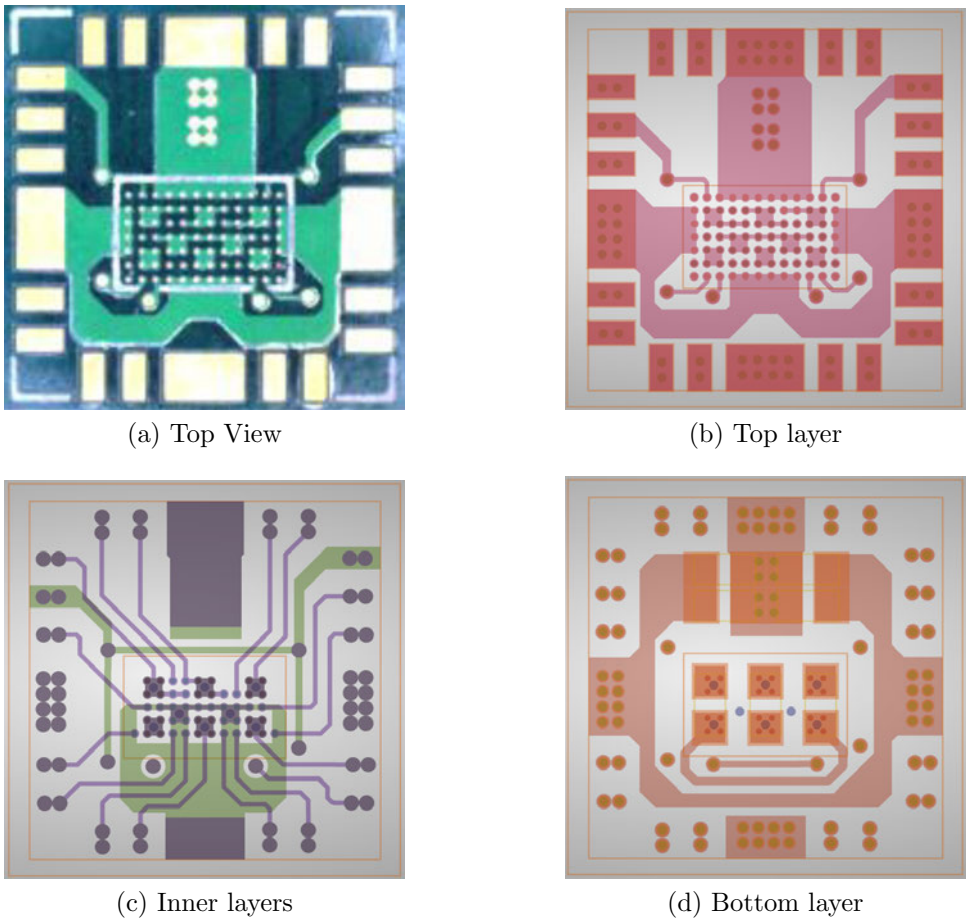
Table 5.2: Parasitic inductance estimation in FCBGA package.

Element	**Characteristics**	**Parasitic Inductance**
0402 SMD capacitor	1.0 mm x 0.5 mm x 0.5 mm	370 pH
Solder Bump 1	Diameter = 100 μm Thickness = 50 μm (max.)	2 x 10pH / 2 = 10 pH
Interposer Via (4 layers, 1 oz Cu)	Diameter = 100 μm Thickness = 460 μm	2 x 200 pH / 4 = 100 pH
Solder-bump 2	Diameter = 200 μm Thickness = 80 μm (max.)	2 x 8.5 pH = 17 pH
Die Trace	Length = 200 μm (max.) Width = 100 μm (min.) Thickness = 3.4 μm (UTM)	2 x 70 pH / 2 = 140 pH
	Total	637 pH

technique can done by smaller assembly house, but at the potential risk of possible damage for the circuit under the pads.

High Density Interposer (HDI)

An interposer is basically another substrate or an external interconnection for a chip, which functions as a regular fan-out board but in a much smaller scale. A more cost-effective way is to implement it through regular PCB vendors with their advanced capability. A prototype



(a) Top View (b) Top layer

(c) Inner layers (d) Bottom layer

Figure 5.6: Chip interposer and its each layer.

interposer board shown in Fig. 5.6 is realized by FlexPCB in California, and the specifications are listed in Table 5.3. The interposer has four layers together with blind and buried vias for more flexibility in fanning out the smaller pins. Note the blind via allows smaller drill than the buried and through vias, which further allows the die bumps to be connected with the via-in-pad for shorter connection. There are many challenges to have fully working power converters, and the challenges associated to the interposer can be categorized into three aspects as follows.

- Cost: it was about USD 4000 for 10 working interposers made in FlexPCB. Although it was cheaper if more boards were ordered, the fixed cost highly depends on the fabrication specifications and it increases exponentially with any tighter constraints. Die bumps with a pitch of 220 μm is indeed very challenging to the back-end process, and that left not enough space for routing out more internal pads from the die using the top layer of the interposer given the constraint of 3 mil minimum trace width.

Table 5.3: Layout specifications of the chip interposer.

Layout Items	**Specifications**
Min. trace width and clearance	3 mil
Via-in-pad	6 mil landing pad and soldermask
Pad-to-pad clearance	2 mil
Blind via	6 mil landing pad, 4mil drill
Buried via	10 mil landing pad, 6mil drill
Through via	10 mil landing pad, 6mil drill
Board thickness	18 mil (4 layers, 1 oz copper)

Therefore, most of the bumps are connected through via-in-pad and use the inner layers for more signal routing, which turns out to be a high cost factor. Meanwhile, in this prototype interposer, the via is plugged with conductive material to avoid the solder from draining out of the vias, which also adds more to the overall cost.

- Assembly: the flip chip is soldered using hot air gun handled by hands, and the alignment between the flip chip and the interposer is done using a Finetech BGA rework station. To improve the alignment and the contact between solder balls and interposer pads, suitable amount of soldering flux was applied on the interposer board before the chip placement. The amount of the flux is critical: underfilled flux results in cold joints and poor connections; overfilled flux along with high-intensity hot air flow can easily drifts the chip away from the right position. Other than that, the successful connection of all pins is mainly determined by the flatness consistency of the interposer, since most of the failure boards are found tilted.

- Yield: it was about 10% to 20% claimed by the connection test at manufacturing side, where they have some equipments to verify the board connection based on the schematic. There is another 80% failure rate while assembling the components in the lab. The via-in-pad for die bump soldering needs a tremendous attention, since the fabrication process of via-in-pad bent the interposer in different angles. This then further causes misalignment between the interposer and die when soldering. Even worse, the vias filled with copper are usually not even, leading to a tilted FCBGA before PCB rework. The connection failure can be found after removing the chip from the interposer, either the pads of the interposer still shine with the exposed copper or the solder balls of the die not melted to flat. However, after several practice and weeding out the bad interposers, the yield of the component assembly was improved to around 80%.

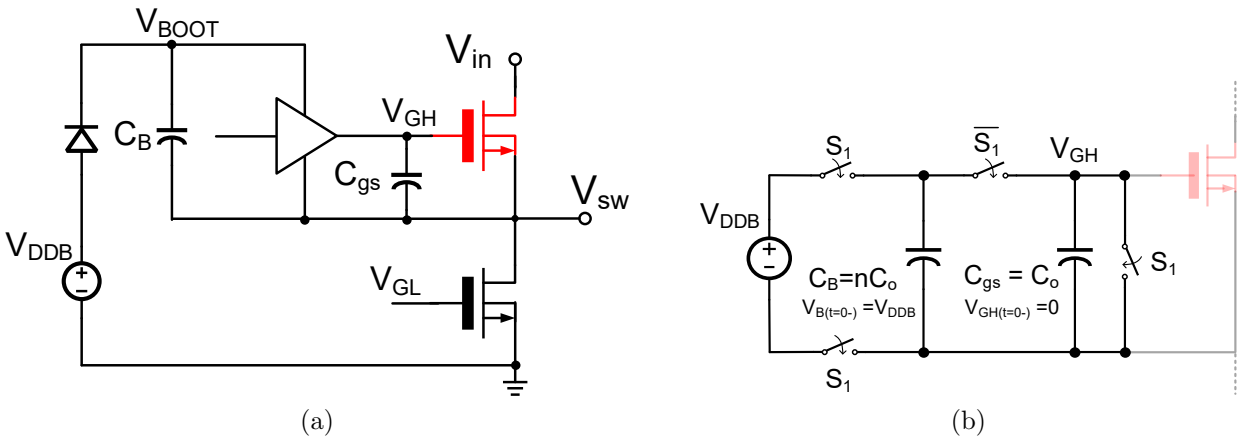


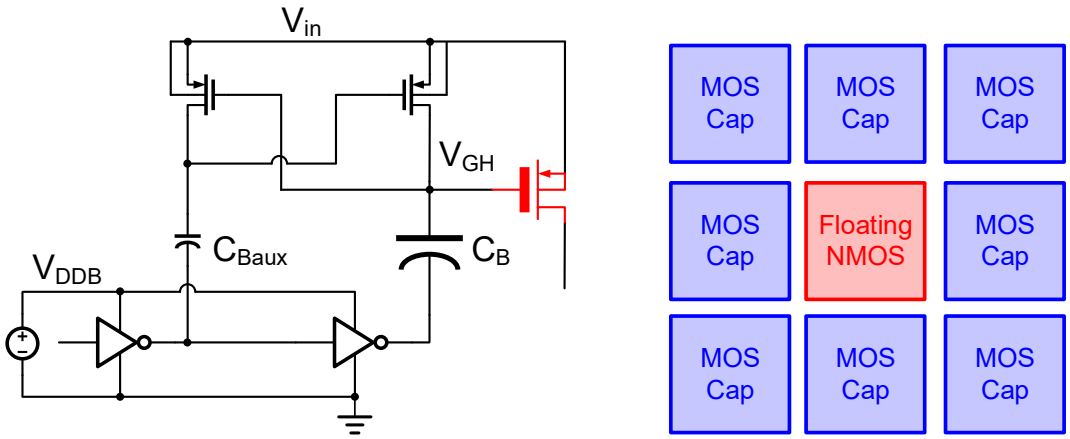
Figure 5.7: (a) Schematic and (b) simplified circuit of a conventional bootstrap circuit for driving high-side NMOS.

5.4 Floating Supply for Gate Drivers

Floating supplies are essential to any power converters with high-side switches. In particular, the SC topologies, composed of many high-side switches, require area-efficient floating supplies to leverage its advantage of high switch utilization. Similar to level translators or shifters, floating supplies transfer electrical signals between different voltage domains except that they are used to drive power MOSFETs with much heavier capacitive load. There are two main requirements for the supply voltage of floating supplies: (i). it should always be high enough to achieve low turn on-resistance and (ii) it should be lower than the breakdown voltage. To implement that, there are several approaches, including capacitor-based technique [8], [9], [70], [71], voltage borrowing technique[6], [72] and transformer-based [73] technique. This section primarily focuses on the previous two approaches, since they are more potential in providing a higher integration level.

Conventional Bootstrap Circuit

The circuit shown in Fig. 5.7 (a) is one of the capacitor-based approaches, which is also called the n-type charge pump. The fabrication of diodes might not be always available in IC processes, the p-type charge pump circuit [70] as shown in Fig. 5.8 (a) can be employed in together with PMOS, which can be turned on with a lower node voltage available within the power converter instead of generating a higher voltage. Focusing on the n-type charge pump, assuming the NMOS can be turned on with $V_{gs} = V_{DDB} \gg V_{th}$, the voltage difference between V_{BOOT} and V_{sw} needs to be V_{DDB} to turn on the high-side NMOS. To ensure that, it is necessary to tie the negative terminal of C_B or the switching node, V_{sw}, to the ground reference of the bootstrap supply voltage, V_{DDB}. Also, the bootstrap capacitor, C_B, must be charged and updated frequently to ensure V_{BOOT} is high enough to turn on the high-side switch. In other words, the high-side switch cannot be fully on or the duty ratio of



(a) (b)

Figure 5.8: (a) Latch and charge pump circuit for driving PMOS and the (b) area allocation of a power switch unit with its bootstrap capacitor using the conventional bootstrap circuit.

Table 5.4: Capacitance density comparison between different processes.

	65 nm CMOS [38]	65 nm CMOS [74]	XFAB 180 nm CMOS
MOSCAP	$2.3fF/\mu m^2$ @ $2.5V$	$1.89fF/\mu m^2$ @ $1.0V$	$2.1-8.3fF/\mu m^2$ @ $1.8V$ $0.9-2.7fF/\mu m^2$ @ $5.0V$
MIMCAP	$2.0fF/\ \mu m^2$	$1.85fF/\ \mu m^2$	$6.6fF/\ \mu m^2$ for Triple MIM
MOMCAP	$1.6fF/\ \mu m^2$	$2.42fF/\ \mu m^2$	Provided but no density shown

V_{GH} cannot be 100%. It is commonly seen that never-grounded V_{sw} leads to not switching V_{GH}, especially when individually testing floating switches. Consequently, the application of the conventional bootstrap circuit is only limited to buck converters, and a modified bootstrap circuit and several cascaded bootstrap circuits are developed later to address more complicated floating issues.

The conventional bootstrap circuit is commonly seen in discrete implementations. To design the bootstrap capacitance required by the conventional bootstrap circuit, a simplified circuit as shown in Fig. 5.7 (b) can be employed, which assumes very low bootstrap diode voltage drop. Before turning on the high-side switch (S_1 is high), C_B is charged to V_{DDB} through a bootstrap diode and C_{gs} is discharged to ground. As the high-side switch is turning on (S_1 is low), C_B is in parallel with C_{gs} through the gate driver. During this charging process, C_{gs} is supposed to be charged to V_{DDB} so that V_{gs} is high enough to reduce the switch turn-on resistance. However, after charge redistribution between C_B and

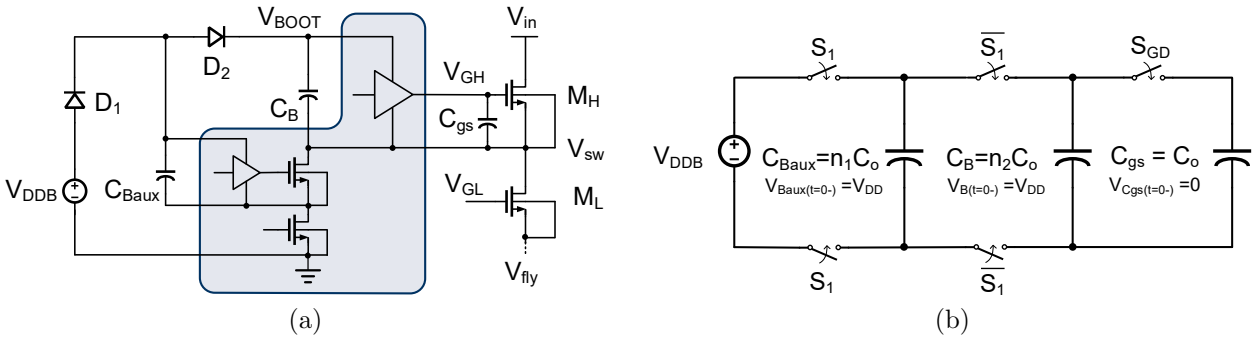


Figure 5.9: (a) Schematic and (b) simplified circuit of a modified bootstrap circuit for driving high-side NMOS.

C_{gs}, the final voltage becomes:

$$V_{gs} = \left(\frac{n}{n+1}\right) V_{DDB}, \tag{5.3}$$

which is different from V_{DDB}. In discrete implementations, the capacitance density ratio between capacitors, such as SMD MLCC, and switches C_{gs} can easily go more than 10,000 times, lending itself to a good use of conventional bootstrap circuit. To implement C_B on chip, there are mainly three kinds of capacitors: MOSCAP, MOMCAP and MIMCAP as listed in Table 5.4. In some advanced CMOS processes, either only MIMCAP or a combination of MOSCAP and MOMCAP is allowed on the same vertical plane, instead of having all three of them in parallel. In general, the MOSCAP is available and it has higher capacitance density. While the combination of MOSCAP and MOMCAP may provide more capacitance density, full integration of capacitors significantly increases the chip size given low on-chip capacitance density. An example of a unit switch cell is shown in Fig. 5.8 (b), the size of a combination of power switches and bootstrap capacitors has to be more than 9 times the original power switches in order to maintain high V_{gs} according to (5.3). However, the MOSCAP also experiences lower breakdown voltage and higher voltage derating factor than other capacitors, complicating the on-chip integration of conventional bootstrap circuit. Some exotic capacitor process might provide higher capacitance density [72], [75], which however is not cost-effective.

General-Purpose Bootstrap Circuit

The schematic of a general-purpose bootstrap circuit [76] is shown in Fig. 5.9, which can be placed at any floating domains without pre-knowledge of the converter operations. The modified bootstrap circuit generates the floating voltage of $V_{in} + V_{DDB}$ by duplicating the whole system shown in Fig. 5.7 (a) including the power switches for the buck converter, which is then coupled to a high-side driver through an additional diode, D_2. As compared to the conventional bootstrap circuit, the general-purpose bootstrap circuit decouples the

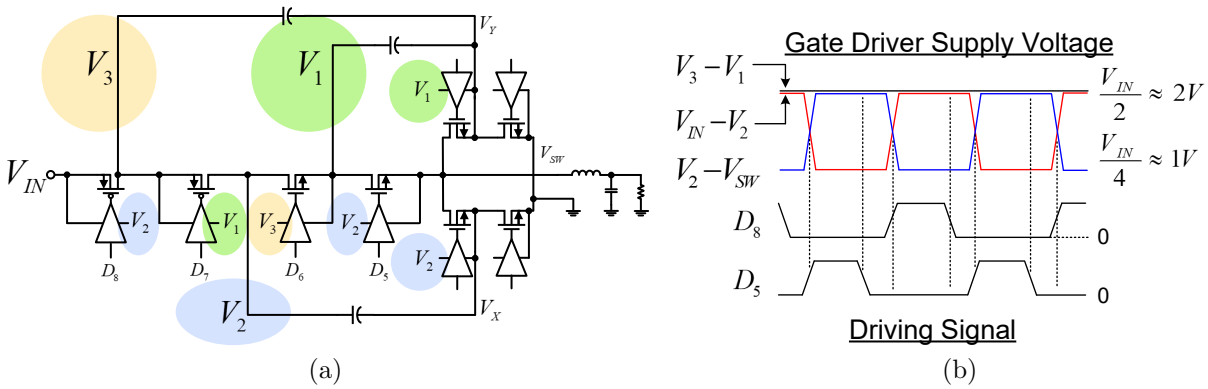


Figure 5.10: Voltage borrowing technique in a 4-to-1 Dickson converter.

charging of C_{Baux} and C_B, offering the benefits of turning on high-side switches with 100% duty ratio. This circuit can be very useful in power converters like non-inverting buck-boost converter when it is either operated at buck or boost mode and one of the switches is fully on. Unlike cascaded bootstrap technique [77], the voltage drop of the gate driver circuit is guaranteed $2V_D$, which can be easily compensated by increasing V_{DDB} to $V_{DDB} + 2V_D$.

The design consideration on C_B and C_{Baux} is similar to the conventional bootstrap converter, and a simplified schematic shown in Fig. 5.9 (b) is used to analyze the modified bootstrap circuit. The target is to maintain high enough V_{BOOT}, otherwise low V_{BOOT} triggers metastability condition in the gate drivers, drawing more current from C_B and deteriorating the voltage drop issue. The most efficient charge transfer between capacitors is from a much larger capacitance to a smaller capacitance, and $n_1 = 81$ and $n_2 = 9$ are selected intuitively according to (5.3) so that V_{BOOT} can be charged to a high enough voltage. Other than that, since the switching frequency, f_{sw}, of the power switch and updating frequency, f_{update}, of C_B can be different ($f_{sw} = f_{update}$ in conventional bootstrap circuits), there might be a more optimal design on all C_B, C_{Baux}, f_{sw} and f_{update} in terms of size and efficiency. For example, f_{update} can be designed faster to reduce C_{Baux}.

Given the inductor-free and topology-independent advantages, this circuit can be very compact and powerful if the shaded area as shown in Fig. 5.9 (a) can be further integrated. Most of the components are low-voltage and associated with V_{DDB}, and the highest blocking voltage is V_{in} on D_1, D_2 and the two switches (one grounded and one connected to V_{sw}). The voltage rating of the general-purpose bootstrap circuit is simply determined by available fabrication process, and the switching performance can be tuned by the size of the two additional switches. Unlike transformer-based approach, it has high stability and reliability, since there is no extra regulation loop needed.

Voltage Borrowing Techniques

This technique directly retrieves the energy from an internal node of a power converter. It can also be understood as sharing or borrowing the capacitance from the existing flying

capacitors, or the SC structure itself can be seemed as a provider of multiple floating voltage sources. The key step is to match the voltage requirement of the gate drivers to the closest floating voltage sources. There are two situations when the node voltage is not close enough to the required level: (i). the supply voltage is too high and linear regulators serve the simplest and smallest way to step the supply voltage down to a safe level; (ii). the supply voltage is too low and a larger-size switch (either NMOS or PMOS) is then required to compensate the lower conductance density. While both situations may degrade some efficiency or power density, the voltage borrowing technique may be still more beneficial than on-chip bootstrap circuit given the condition of low on-chip capacitance density. Also, in some critical applications like GaN-power converters, a series or shunt regulator is already hooked up in front of the gate terminal to prevent it from punch through, and that can serve as part of the voltage borrowing technique.

Fig. 5.10 shows the voltage borrowing technique employed in a 4-to-1 Dickson converter. In the final prototype, all GDs and LSs are powered by flying capacitor nodes of the power stage. Note that those power MOSFETs, Q_8 and Q_7, close to the high input voltage are implemented using PMOS with larger size, other lower switches are implemented by NMOS. Usually, PMOS is preferred for high-side switches so that the driving voltage can be easily found within the power converter and the use of bootstrap circuit can be avoided. As shown in Fig. 5.10 (b), the waveforms of the supply voltages (V_{HIGH}–V_{LOW}) to the LSs and GDs, V_3–V_1, V_{in}–V_2 and V_2–V_{sw} are all sufficiently high to turn on switches with low on-resistance, and within the switch voltage ratings. For driver D_8, it can be supplied by $V_{in} - V_2$, instead of generating a higher voltage. Although $V_{in} - V_2$ can be sometimes decreased to V_o, it is back to $2V_o$ when Q_8 needs to be turned on. Similarly, $V_2 - V_{sw}$ for the driver D_5 is also ready when Q_5 is turning on. Other middle drivers including D_7, D_6 and D_3 can easily find their right floating source, since $V_3 - V_1$ and $V_2 - V_X$ are always $2V_o$. In the case where $V_o = 1V$, the common 2.5 V I/O devices are good enough for building up these gate drivers. The only bottleneck is the supply voltage for D_4, since it only has stable V_o or $3V_o$ available in its voltage domain with reference of V_Y. In the proposed chip, $V_1 - V_Y$ is selected with a larger switch size assigned to Q_4 (2.5 V devices), since $3V_o$ would leave less margin to 3.3V I/O devices.

Comparison between floating supplies

Both bootstrap circuit and voltage borrowing technique have their own advocates. For example, while voltage borrowing technique is more commonly seen in pure SC converters [6], [72], implementing bootstrap capacitors using either external capacitors [70], [71] or large-area on-chip capacitors [8], [9] can also be found in synchronous buck converters, a folded Dickson converter and an 11-to-1 SC converter. In this section, more general floating supplies are provided for converters with higher conversion ratios, which were mostly limited to 3:1 or below in prior designs. For instance, the general-purpose bootstrap circuit can be plugged in any voltage domains without topological limitation, and the voltage borrowing technique is extended to higher levels like Fig. 5.10 (a).

Table 5.5: Area comparison for on-chip floating supplies.

	JSSC 2011 Le [6]	**JSSC 2015 Biswas [11]**	**JSSC 2015 Sarafianos [8]**	**PE 2017 Andersen [72]**
Technology Node	32 nm	28 nm	90 nm	32 nm
Gate Driving	Mostly BRW from V_i and V_o, others BTS to $V_i - V_o$ and $2V_o$	Mostly BRW from V_i and V_o, others BTS to $V_i - V_o$ and $2V_o$	Full BTS	Full BRW from V_i and V_o
Max. Output Power	0.61 W w/ 79.8%	0.0017 W w/ 83%	0.0032 W w/ 76.6%	10 W w/ 84%
Capacitance Density	MOSCAP NA	MOS+MOMCAP $5fF/\mu m^2$	MIMCAP $2fF/\mu m^2$	TrenchCAP $220fF/\mu m^2$
Chip Area (SW + GD)	$0.38mm^2$	$0.05mm^2$	$0.24mm^2$	$1.97mm^2$

† BRW: voltage borrowing, BTS: bootstrap circuit
‡ SW: switch, GD: gate driver

The bootstrap circuit generates a non-existing and usually higher voltage, while the voltage borrowing technique is by carefully selecting the existing node voltage. Generally speaking, the capacitance density ratio, X_{GD}, between the bootstrap capacitance density and the switch C_{gg} density

$$X_{GD} = \frac{C_{BOOT}}{\text{Volume}_{C_{BOOT}}} \div \frac{C_{gg}}{\text{Volume}_{sw}} \tag{5.4}$$

can be a selection guideline choosing between different floating supply techniques. High power density is ensured as long as X_{GD} is much higher than 1. When the available capacitance density for bootstrap capacitor is higher, such as trench capacitor in [72] or off-chip capacitors, the bootstrap circuit is preferable since it has high X_{GD} and it can be used to drive NMOS (around 2 to 3 times better conductance density than PMOS). Otherwise, the power density is greatly reduced, such as [11] and [8], since it consumes considerable on-die capacitance using commercially available processes. For designing an on-chip power converter, the voltage borrowing technique is usually suggested for low-voltage process ($V_{rated} < 5V$), which means similar ratings on V_{DS} and V_{GS}. The voltage borrowing technique can be understood as improving X_{GD} by using the existing large flying capacitance. Table 5.5 compares the on-chip floating supplied employed in prior arts, which shows that on-chip bootstrap circuit

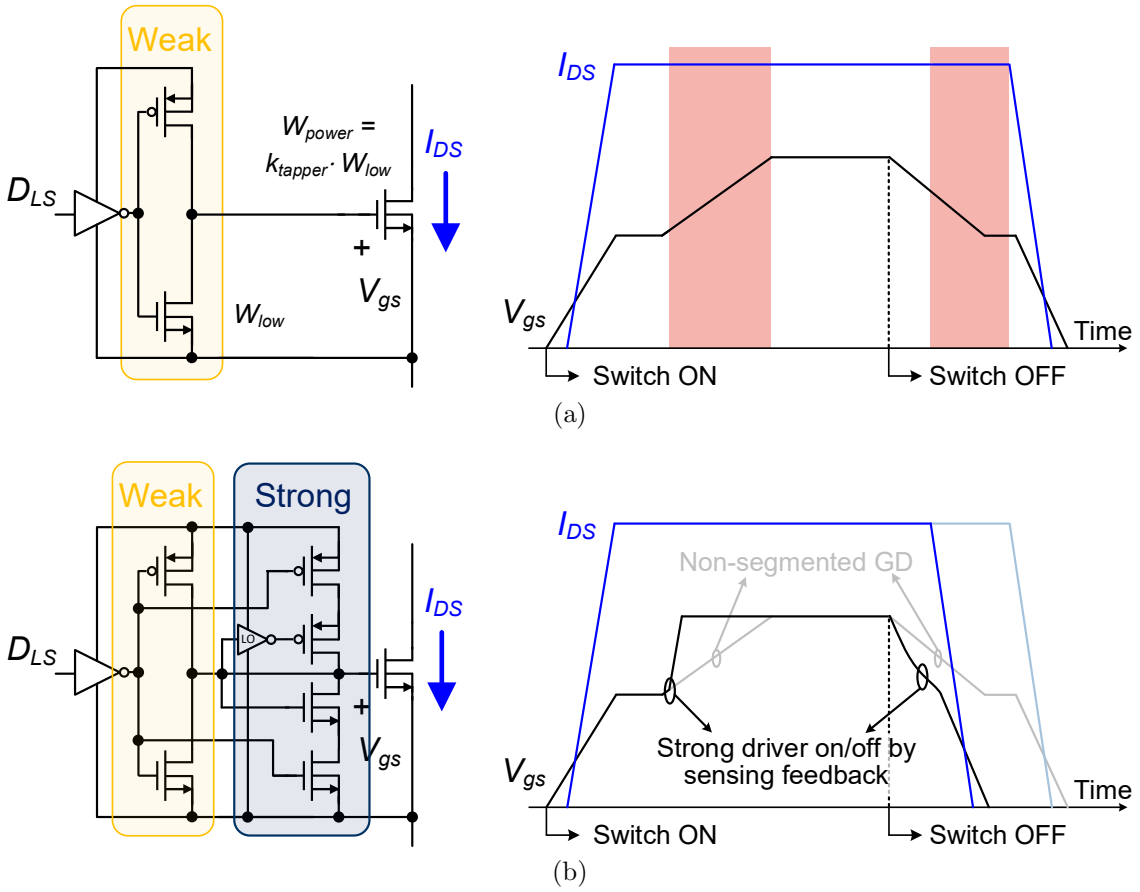


Figure 5.11: (a) weak gate driver and (b) segmented gate driver in reducing the ringing issue.

suffers from low power density when high capacitance density is not available and X_{GD} is low.

5.5 Segmented Gate Driver

Ringing is the primary reason for device failure and it worsens as parasitic inductance and output current increase. Although the ringing can be addressed by selecting a higher voltage rating device, the power density is greatly reduced and the device might not be available in most processes. As shown in Fig. 5.11 (a), the most intuitive way is to increase the gate resistance between gate driver and power MOSFET, so that the switching transition can be slowed down and the ringing is reduced. However, this leads to high on-resistance as well as VI -overlap loss during the switching transition due to low V_{gs}. Therefore, there is a tradeoff between voltage ringing and efficiency while designing the gate driver strengths: weaker gate driver has less ringing issue, but the switching transition time as well the associated switching loss increases, preventing the power converter from operating at high switching

frequency.

Higher ringing voltage is expected with a faster current transition in a larger parasitic inductance, according to $V_L = ESL \cdot \frac{di}{dt}$. While investigating the detailed mechanism between I_{ds} and V_{gs} during power MOSFET switching transition for inductive loads, it is found that the largest current transition occurs during the plateau region, where V_{gs} stays flat due to the miller capacitance seen by the gate driver and the power MOSFET is operated at its saturation region with an intrinsic gain. During the plateau region, the driving current from the gate driver is flowing through C_{gd} of the power MOSFET instead of C_{gs}. Consequently, the driving current is injected into the switching node of the power converter, ramping it up to a higher voltage. The stored energy at the switching node is then swapped between the parasitic inductance and capacitance, leading to the ringing issue. Therefore, a longer transition dampens the ringing voltage more, or vice versa. To reduce the ringing without sacrifice of efficiency, the technique of segmented gate driver is developed, which is by combining both drivers with different strengths and triggering them at different time of the switching transition. Fig. 5.11 (b) shows an example of two segments: weak and strong drivers. At the beginning of the gate driving waveform, the segmented GD turns on the power MOSFET using the weak driver to slow down the transition and reduce voltage ringing. After I_{DS} has fully transitioned, the strong driver is engaged by a LO-skew inverter with threshold voltage higher than $V_{plateau}$. This raises V_{GS} at a faster rate so that the switch reaches the low on-resistance state sooner and the conduction loss is reduced.

To control the strengths of gate drivers, the additional gate drivers, except the default set (weak driver in this case), should be tristate inverters[3], otherwise shoot-through events would occur. Another concern is the trigger timing of the strong driver, which has to be on beyond $V_{plateau}$ to avoid strong gate drivers from being always dominant. The plateau voltage can be estimated as

$$V_{plateau} = V_{th} + \sqrt{\frac{I_{ds}}{k_{sw}}} \tag{5.5a}$$

$$I_{ds} = k_{sw} \cdot (V_{gs} - V_{th})^2, \tag{5.5b}$$

where k_{sw} is the MOSFET parameter covering the information of channel dimension as well as oxide capacitance. Given $I_{load} = 2A$, it is estimated that $V_{plateau} \approx 0.7V$ with some variations depending on V_{ds}. Without adding too much area and power consumption overhead, an inverter serves as a simple and quick comparator for sensing $V_{plateau}$, which can be done by setting the inverter threshold, V_m, to around $V_{plateau}$. The value of V_m is determined by the ratio of pulling strengths between PMOS and NMOS. Nominally, $V_m \approx V_{dd}/2$ when PMOS and NMOS have equal pulling strengths, i.e. when the width ratio is 3:1. In order to achieve $V_m \approx 0.7V$, LO-skew inverter is chosen with $P : N = 3 : 9$ through the simulation result shown in Fig. 5.12 (b).

Fig. 5.12 (c) and (d) show the simulation results under the conditions of $I_{load} = 1.82A$ and $V_{in} = 4V$. The parasitic inductance in each flying capacitor is set 1 nH, which is 30%

[3]The pull-down transistors of the strong gate driver may not need to be tristate or controlled since most power switches can be turned off with intrinsic zero-voltage switching.

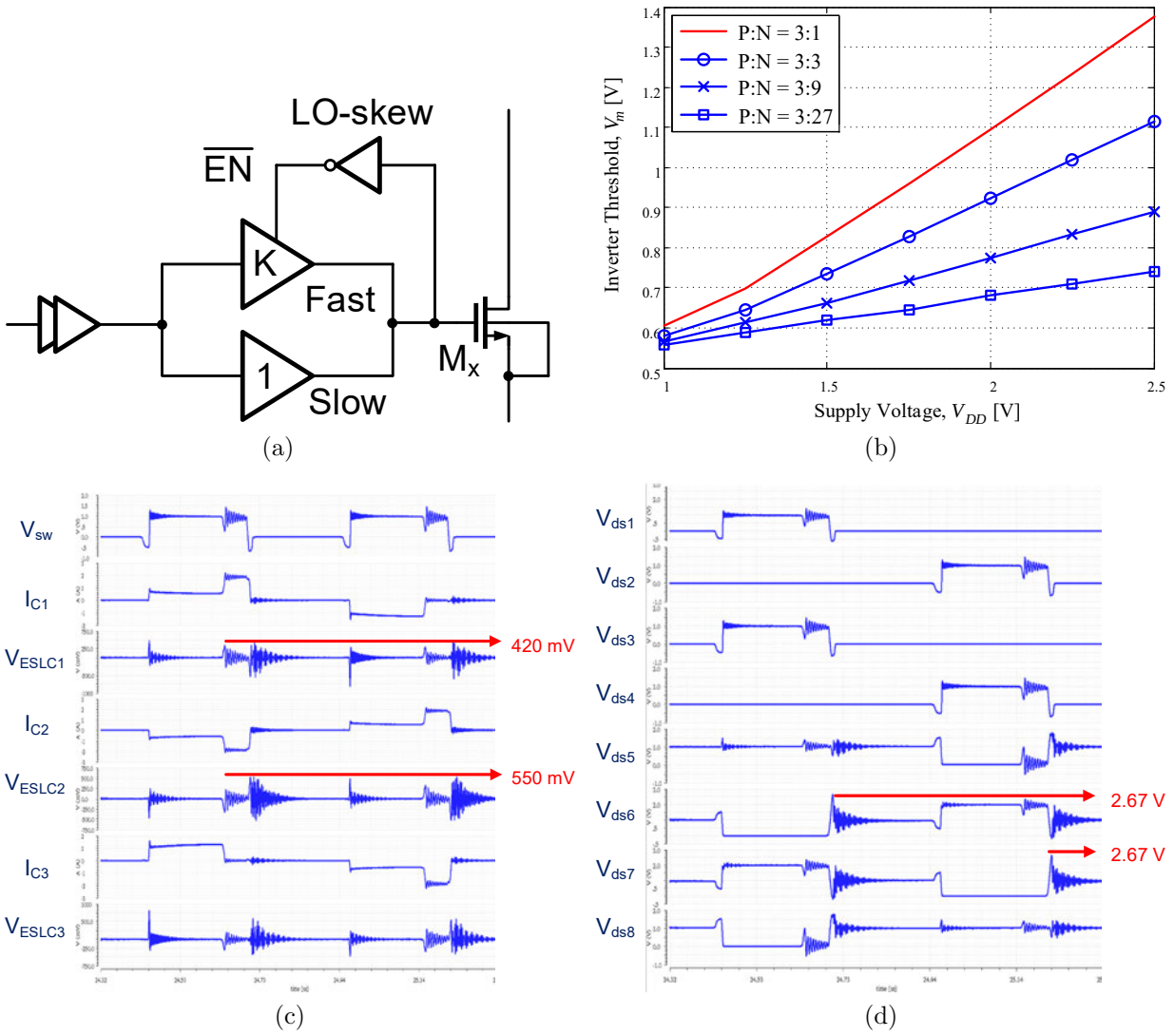


Figure 5.12: (a) Simplified schematic of segmented gate drivers, (b) inverter threshold design of the $V_{plateau}$-sensing inverter, (c) current and voltage across the parasitic inductance and (d) switch blocking voltgae when applying with the segmented gate driver.

more than the estimated inductance for design margin for the co-package situation shown in Fig. 5.5. By using the segmented gate driver, the ringing voltage on each parasitic inductance is limited to around 500 mV, which then adds to the blocking voltage of each power switch. Due to higher nominal blocking voltage ($2V_o$) and current transition, the worse case happens in Q_6 and Q_7, which have blocking voltage more than their nominal rated voltage (2.5 V). Given that this happens for a short interval and there is a 20% margin for the switch devices, the converter is still within the safe operating region.

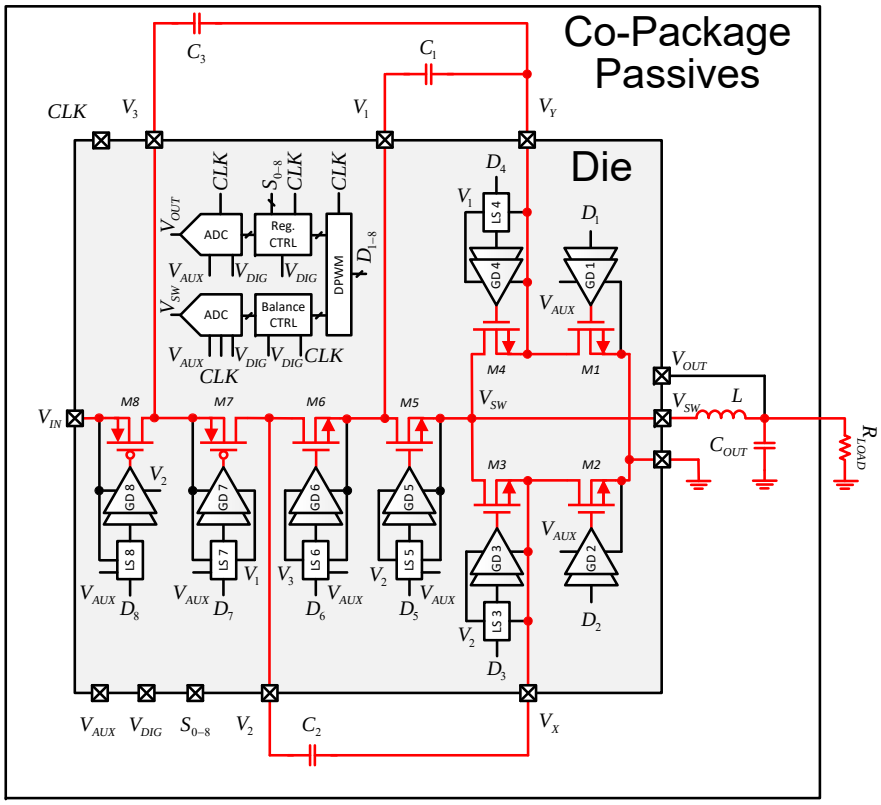


Figure 5.13: Block Diagram and Packaging of a 4-to-1 Dickson Converter.

5.6 Measurement Results

The schematic of the hybrid Dickson converter is presented in Fig. 5.13. The power MOSFETs, level shifters (LS), gate drivers (GD) and digital controller are integrated on the die with a wafer-level flip-chip package, while the passive components are co-packaged on the opposite side of a fine-pitch interposer in the annotated whole testing system as shown in Fig. 5.14. The FCBGA die has a total of 80 working bumps, with 4 at the corner to avoid DRC violation and fabrication issues. The external signals, $S_{1\text{–}8}$, are used to program the internal digital controller and to preset the duty ratios for gate driving signals, $D_{1\text{–}8}$, during start-up. The supply V_{DIG} is provided externally to power the digital controller blocks consisting of the ADCs, output voltage regulator, capacitor voltage balancing and DPWM generation circuitries. To better experimentally characterize gate driving power consumption, $V_{AUX} = V_{in}/2$ is externally supplied, but included in all efficiency measurements. The SC stage is a 4-to-1 Dickson topology, with 3 flying capacitors and inherently low voltage stress on the switches, allowing for the use of advanced CMOS process and transistors with better figure-of-merit. In this work, 2.5 V devices are used for an input voltage of 4.2 V without the cascode transistor need. The testing board shown in Fig. 5.14 was showcased in

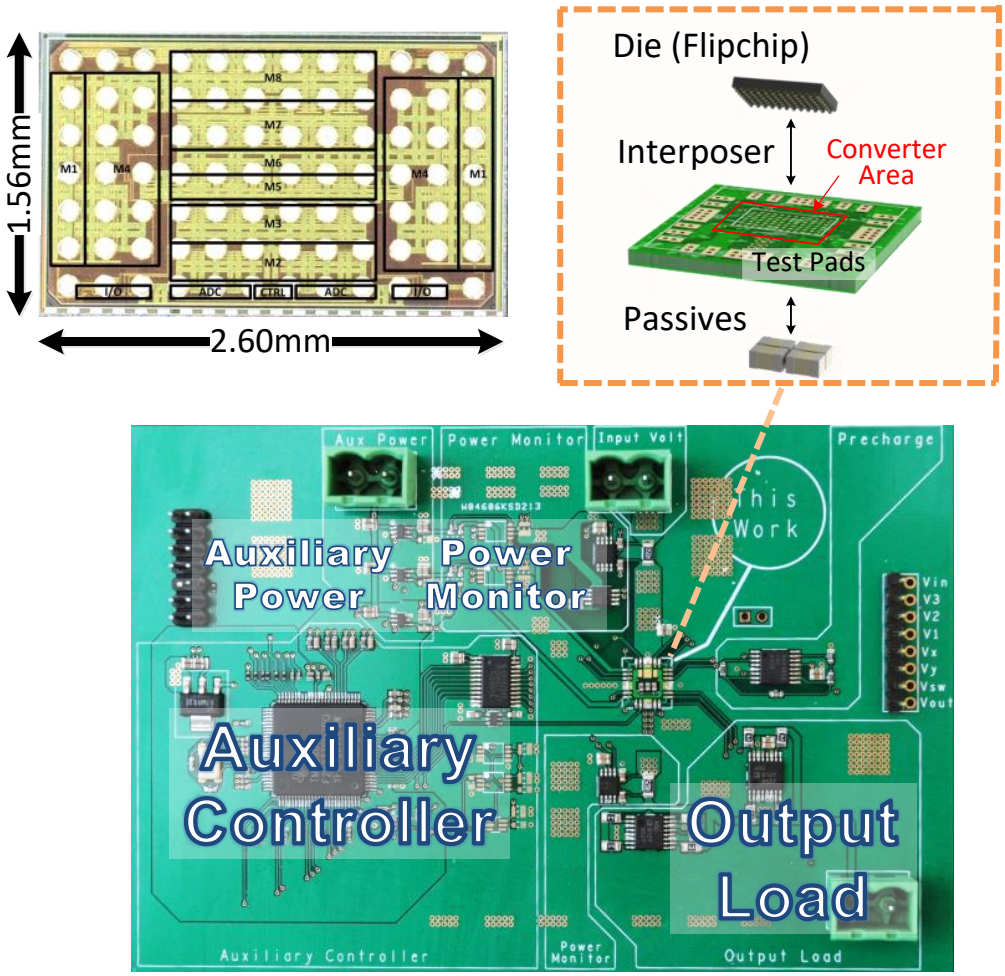


Figure 5.14: Whole testing system with the die photo, converter packaging and testing board.

ISSCC Demo 2017. On the same board, multiple peripheral and monitoring circuits are also implemented. The regulation of the proposed converter can be either internally controlled by an on-chip synthesized controller for showcasing full integration or externally controlled by a microcontroller for exploring more functions. The output load, composed of several switches and resistor, can be reconfigured to simulate light to heavy load condition. The input power, output power and consumption of the IC are all monitored on board, which are then sent back to the microcontroller for a GUI display.

A converter prototype using 65 nm bulk CMOS process has been implemented with a die area of 4 mm^2 as shown in Fig. 5.14, with a symmetric layout and gate drivers to greatly reduce the delays in driving signals. All capacitors are in imperial 0402 packages with nominal capacitance of 22 μF (@ 0 V), which will be derated to approximately 60%, 40% and 15% for blocking voltage of 3 V, 2 V and 1 V, respectively. Fig. 5.15 shows measured

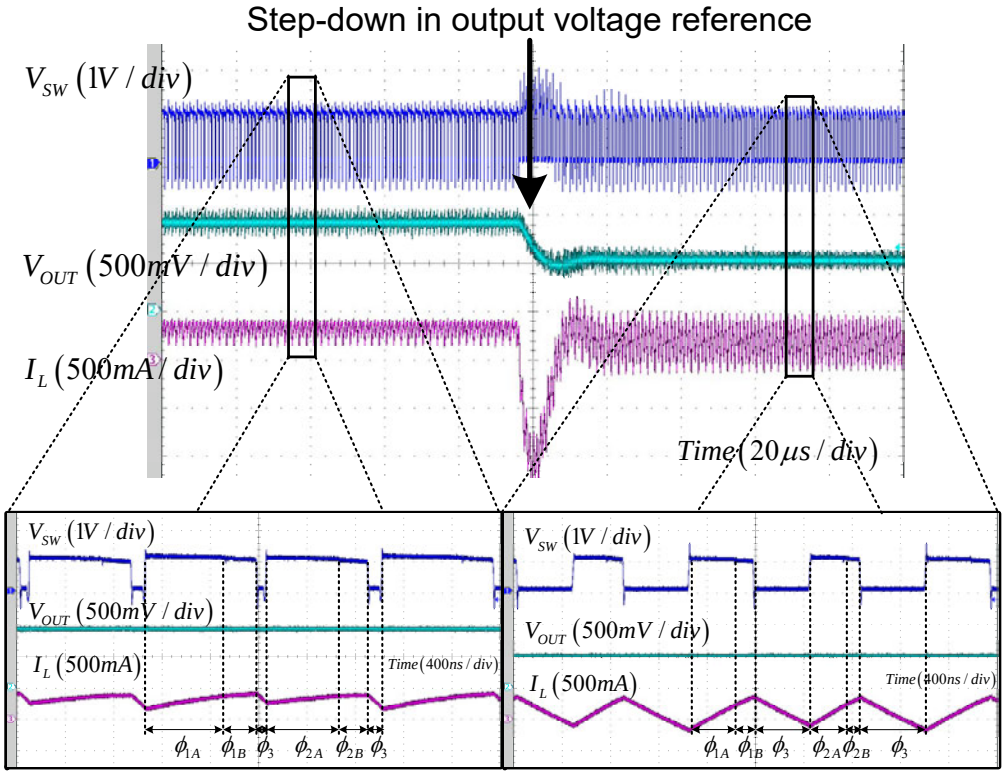


Figure 5.15: Key waveforms of the proposed 4-to-1 Dickson converter.

waveforms of V_{sw}, I_L, and V_{out} for a step-change in commanded duty cycle D, illustrating the PWM operation and corresponding output voltage regulation. It can be observed that the consecutive pulses in V_{sw} have similar levels, which means all flying capacitors are balanced with their nominal voltage, i.e. $3V_o$, $2V_o$ and V_o. The converter has been tested at PWM frequencies ranging from 200 kHz to 5 MHz, with excellent flying capacitor voltage balancing and gate drive functionality. Fig. 5.16 (a) and (b) show the measured efficiency versus output current at different input voltages and conversion ratios for two different frequencies. The peak output current is 1.53 A, while the efficiency peaks at 94.2%. The comparisons in Fig. 5.16 (c) and (d) between this work and other recently published comparable designs show this work achieves excellent power density and efficiency for the large voltage conversion required in direct battery applications. For this comparison we report the lower efficiency associated with 1 MHz operation for our prototype, where the inductor footprint is smaller than the die area in our 3D stacked prototype. Moreover, excellent power density is achieved despite the relatively low PWM frequency, owing to the reduced inductor amplitude and effective frequency doubling associated with the Dickson topology. Table 5.6 summarizes the performance of our prototype, along with comparison to prior designs. Along with the widest input and output voltage regulation range, this work achieves similar or higher efficiency and power density as other best-in-class prototypes, but at a significantly higher voltage conversion ratio (up to 15:1).

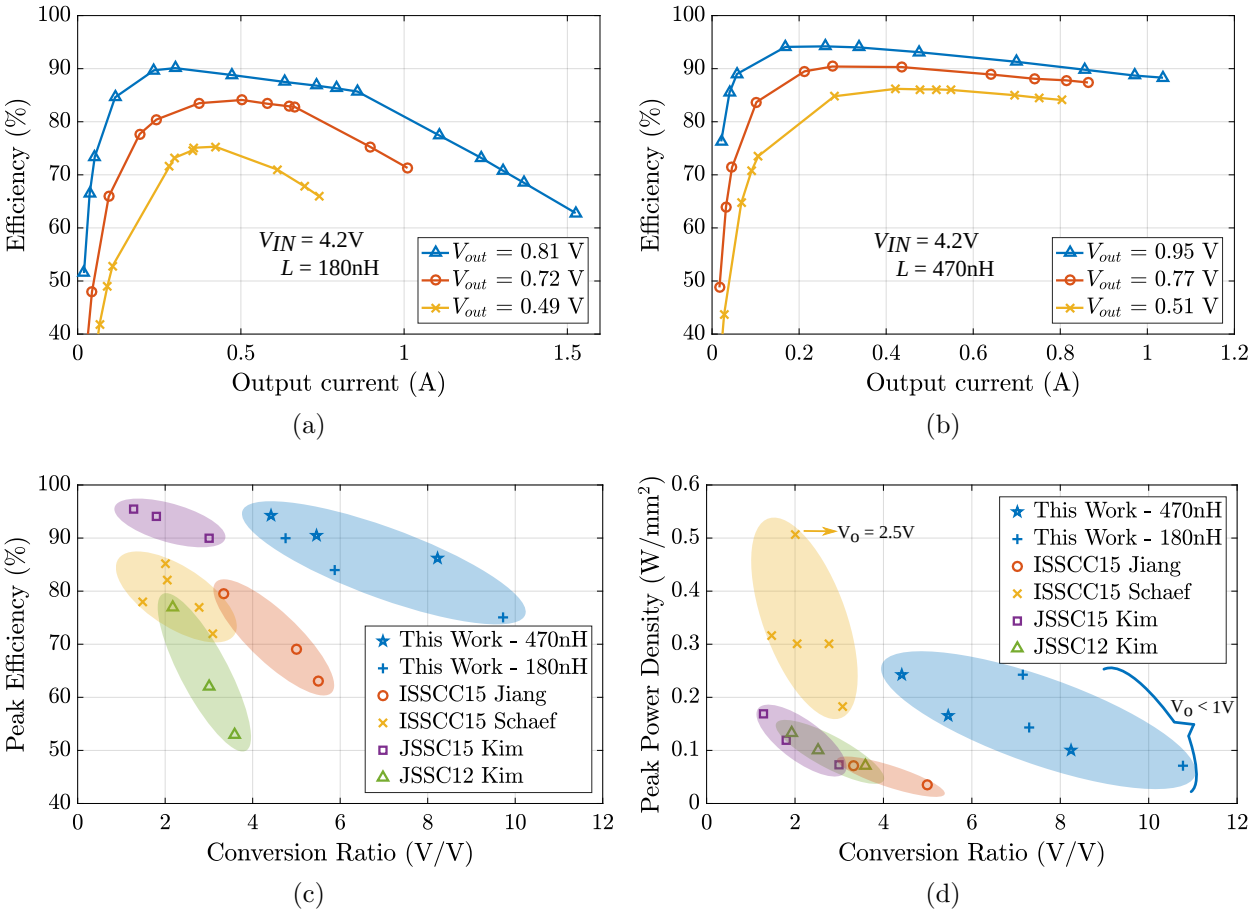


Figure 5.16: Efficiency measurement and performance comparison.

5.7 Chapter Summary

This chapter leverages the high switch utilization advantage of hybrid Dickson converters through dedicated control schemes, packaging and gate driving techniques. It is found that the split-phase control can achieve complete soft charging operation by fully removing the charge sharing loss in the two-phase control. As compared to the incomplete soft charging operation, the split-phase control achieves its minimum output impedance at even lower switching frequency, improving the light load efficiency. Additionally, the split-phase control allows equal capacitance for all flying capacitors, together with a significant inductance reduction by hybrid SC topology, enabling compact packing of passive components. Low form factor is further solidified through the employment of the voltage borrowing technique for floating power supplies, which improves the capacitance density ratio by getting the floating voltage from flying capacitors. To ensure high power density, the capacitance density ratio provides a general selection guideline between bootstrap circuit and voltage borrowing techniques: if bootstrap capacitor has higher capacitance density the bootstrap circuit technique

Table 5.6: Performance comparison with prior arts.

	This Work Liu [38]	**ISSCC 2015 Jiang [78]**	**JSSC 2015 Schaef [48]**	**JSSC 2015 Kim [20]**	**JSSC 2012 Kim [40]**
Structure	Hybrid SC	SC	ReSC	Buck	3-level Buck
Input Voltage $[V]$	3.0 - 4.5	1.5 - 2.5	6, 3	1.8	2.4
Peak Output Current $[A]$	1.53	0.05	2	0.6	0.8
Overall Peak Efficiency @ Conversion Ratio	94.2% @ 4.4	79.5% @ 3.3	85.1%† @ 2.0	95.5% @ 1.3	77%† @ 2.2
Peak Efficiency @ Max. Conversion Ratio	86% @ 8.2	63%† @ 5.5	72%† @ 3.1	90%† @ 3.0	53%† @ 3.6
Peak Power Density, ρ_p @ Conversion Ratio $[W/mm^2]$	0.24 @ 4.4	0.07† @ 3.3	0.51† @ 2.0	0.17 @ 1.3	0.13† @ 1.9
Efficiency @ ρ_p	88.3%	68%†	83%†	88%†	63%†
Process	CMOS 65 nm	CMOS 65 nm	CMOS 180 nm	CMOS 65 nm	CMOS 130 nm

† Estimated from measurement result

is preferred, otherwise voltage borrowing technique is chosen.

A 4-to-1 hybrid Dickson converter is measured with peak efficiency of 94.2% and peak current of 1.53 A. It is the first CMOS implementation of a hybrid Dickson SC converter, with innovative segmented floating gate driver and level shifter designs that are directly powered by the flying capacitors themselves, saving significant die area compared to bootstrap solutions. A significant improvement in power density and efficiency is achieved for high-voltage step-down (up to 15:1) applications compared to conventional SC- and inductor-based power converters, of great practical importance for low-voltage CMOS loads powered by Li-ion batteries. As high-efficiency, high step-down conversion is difficult to achieve in low-voltage CMOS power conversion, this work illustrates that hybrid SC topologies and control methods can yield significant performance improvements compared to conventional solutions.

Chapter 6

On-Chip Flying Capacitor Balancing Techniques

Unlike pure SC, the charge balance between flying capacitors in hybrid SC type-I (SC topologies with soft-charging operations through an output inductor) is not only defined by voltage sources (input and output voltage), but also highly associated with the inductor current and charging intervals. For further investigation into the mechanism of flying capacitor balancing, this chapter uses three-level converter as an example.

The challenges are addressed by using an auto-capacitor-compensation pulse frequency modulation (ACC-PFM) controller together with delay-equalized level shifters (Deq-LS) [52]. Rather than employing a preset strength for duty ratio calibration through direct V_{CFLY} monitoring [44], [45], [79] that is susceptible to the aforementioned variations, this proposed technique achieves auto-adjustable balancing strength through regulation of the inductor current, I_L, or equivalently the net current, ΔI_C, to the flying capacitor, C_{FLY}. As shown in Fig. 6.1, the ACC-PFM controller builds on earlier work, which achieved voltage balancing, albeit over a limited operating range [46], [80], [81] working as a three-level converter with the auto-capacitor-compensation functionality. In [46], the four power switches only operate as a three-level converter for $D < 0.5$ with the valley current mode control employed to obtain auto-capacitor-compensation. In order to maintain the advantage of inductor current ripple reduction over the entire duty ratio range, it is proposed to employ a peak current mode control for $D > 0.5$ and a valley current mode control for $D < 0.5$. Therefore, a three-level converter is demonstrated working at a full-range duty ratio, with a method to simultaneously alleviate V_{CFLY} unbalance issue and efficiently regulate the output voltage. The Deq-LS circuit ensures the accuracy of C_{FLY} charging and discharging intervals; the rising and falling delays of the level shifted gate drive signals for the converter are then equalized, resolving the issue of skewed delays in conventional stack-up level shifters. This characteristic allows the three-level boost converter to operate at high switching frequencies with maximum feasible duty ratio.

This chapter first describes the fundamental operating principles of a three-level boost converter, along with the charge flow and impacts of the unbalanced flying capacitor voltage.

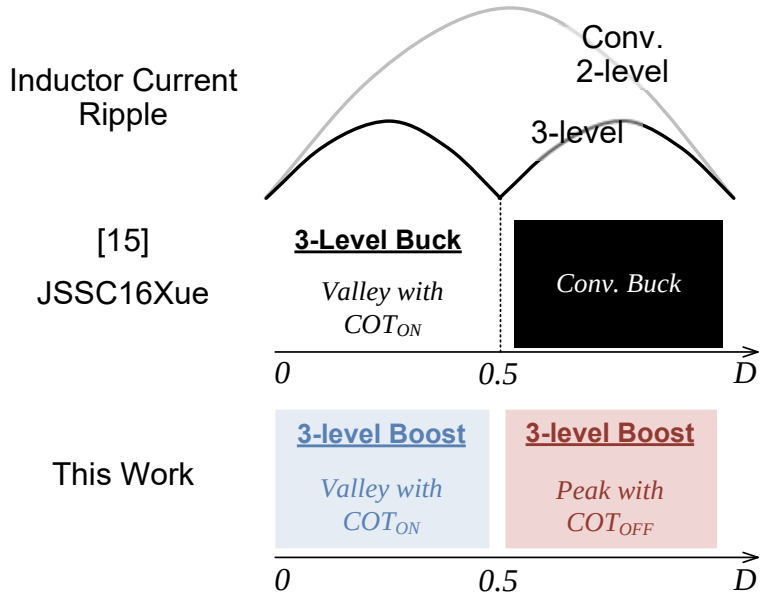


Figure 6.1: Full-duty-ratio region capacitor compensation for three-level converters.

The mechanism of the proposed ACC-PFM controller in ensuring balance is then illustrated. The functionalities and designs of key building blocks in the system, including timing control and level shifter circuits, are also explained. Finally, the performance of the proposed three-level boost converter is validated through a prototype fabricated in 65 nm CMOS process technology.

6.1 Charge Flows of Flying Capacitors

The schematic of a three-level boost converter is shown in Fig. 6.2. Two complementary signal pairs, Q_{1-4}, are generated to drive the power MOSFETs, with Q_4 complementary with Q_1, and Q_3 complementary with Q_2. Both signal pairs are operated 180^o out of phase (e.g. Q_1 and Q_2) and their duty ratio, D, is referred to the on-time of Q_1 and Q_2. The three-level boost converter operates in four switching states as shown at the bottom left of Fig. 6.2. During states 1 and 2, the inductor is magnetized and de-magnetized, respectively, analogous to the conventional boost converter. While in states 3 and 4, the flying capacitor, C_{FLY}, is introduced into the circuit. The three-level boost converter will go through different switching states based on the D values, i.e states 1, 3 and 4 for $D > 0.5$, and states 2, 3 and 4 for $D < 0.5$. The relation between the conversion ratio, V_O/V_{IN}, and D can be expressed as

$$\frac{V_O}{V_{IN}} = \frac{1}{1-D} \tag{6.1}$$

for both regions of $D > 0.5$ and $D < 0.5$, by applying the *volt-sec* balance across the inductor during steady state. From (6.1), the three-level boost converter exhibits variable conversion

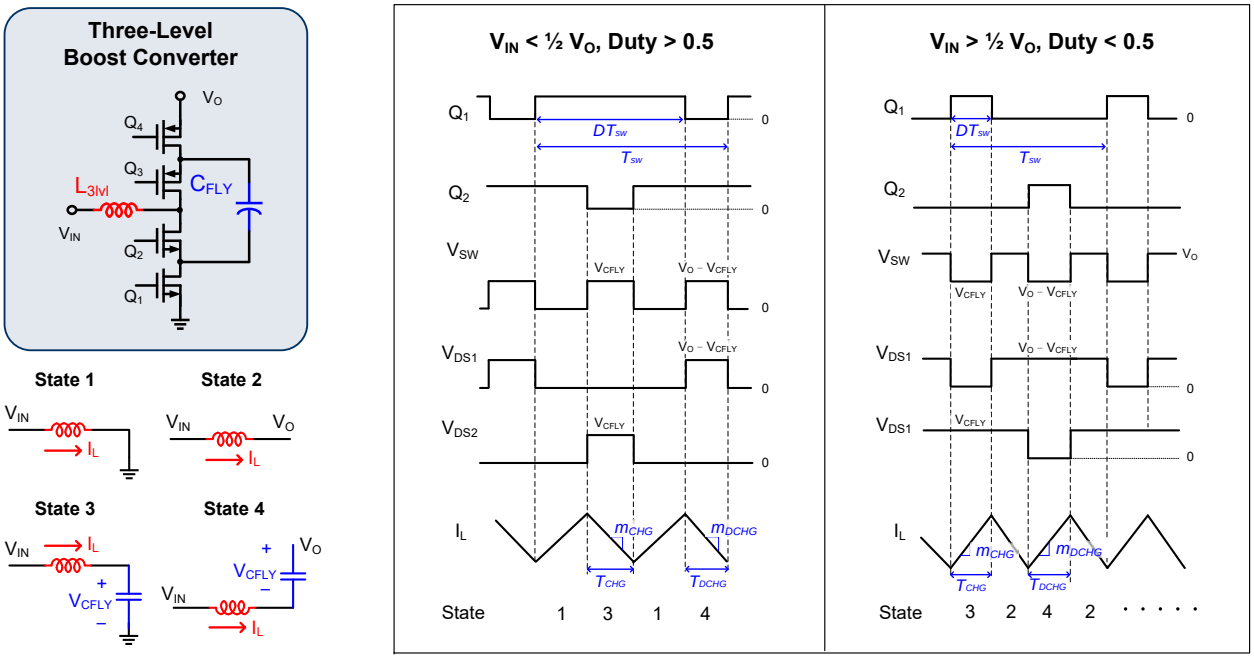


Figure 6.2: Circuit configurations and operational waveforms of a three-level boost converter.

ratios with a tunable D, where $V_{IN} < V_O/2$ for $D > 0.5$ and $V_{IN} > V_O/2$ for $D < 0.5$. As can be seen in Fig. 6.2 (right), no matter what duty ratio regions, the blocking voltage required by the switches are around $V_O/2$ in the three-level boost converter, as compared to V_O in conventional boost converters. Meanwhile, the equivalent frequency seen by the inductor is doubled and the voltage across it is reduced, leading to inductor current ripple reduction in a three-level boost converter.

However, the aforementioned advantages of three-level boost converters depend on the voltage across the flying capacitor remaining balanced throughout the operations, i.e $V_{CFLY} = V_O/2$. Any occurrence of imbalance in the average flying capacitor voltage leads to uneven V_{sw} pulses, which further leads to increased voltage stress on the switching transistors. An example of $V_{CLY} > V_O/2$ for $D > 0.5$ is shown in Fig. 6.3 to unveil the influence of unbalanced V_{CLY} on the power converter. In this case, not only that the power MOSFETs would degrade due to the fact that V_{DS2} and V_{DS3} may exceed their breakdown voltage, the gate drivers that are powered by the flying capacitor would also be damaged. Contrarily, when $V_{CLY} < V_O/2$, V_{DS1} and V_{DS4} may also see higher blocking voltage. Regardless of the operating region, an unbalanced V_{CFLY} causes higher inductor current ripple, which leads to increased conduction loss on inductor. Therefore, it is critical to address flying capacitor balancing issue since that determines the performance and the reliability of the three-level boost converter, or any multilevel converters in general. In this work, a control mechanism to ensure balanced V_{CFLY} is proposed and will be discussed in the next section.

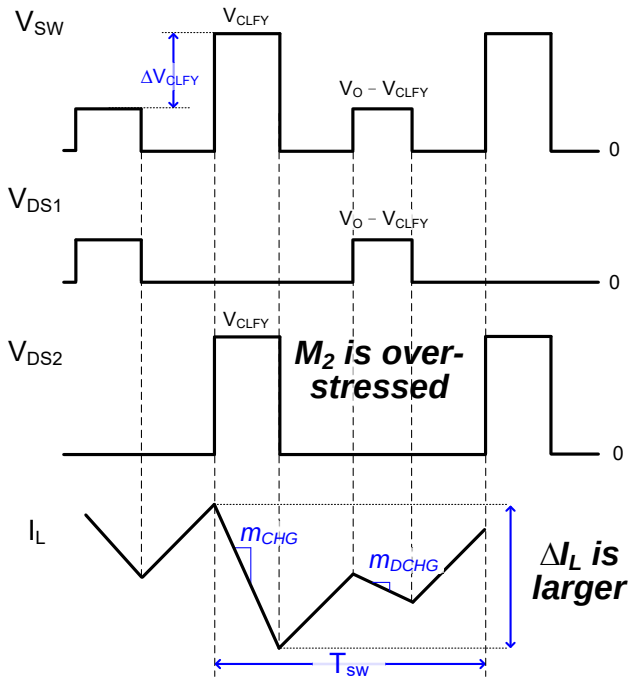
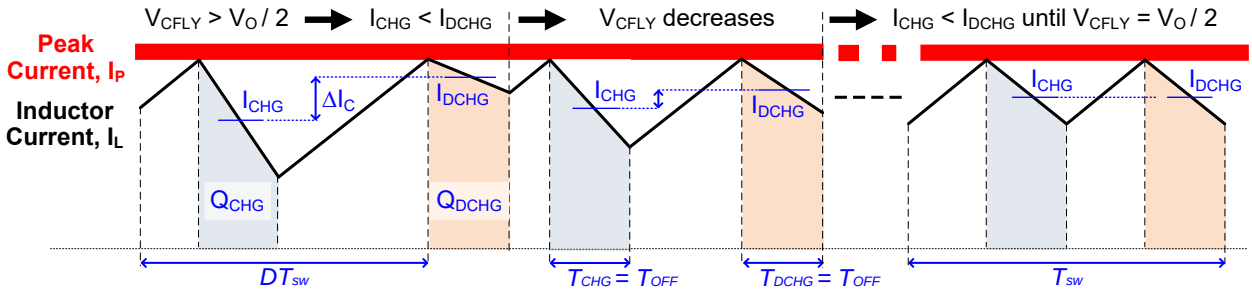


Figure 6.3: Flying capacitor unbalance along with the issues in switch blocking voltage and inductor ripple, under the condition of $V_{CFLY} > V_O/2$ when $D > 0.5$.

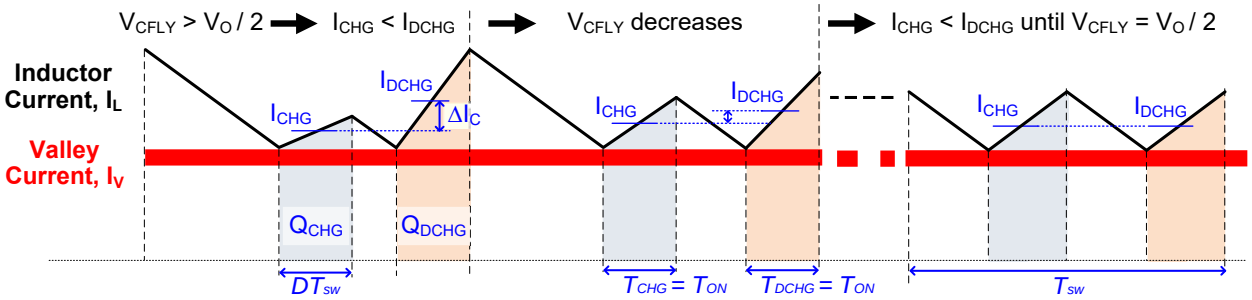
6.2 Auto-Capacitor-Compensation Pulse Frequency Modulation (ACC-PFM)

The ACC-PFM controller is a hybrid current control architecture; it comprises a peak current-mode control with constant-off time for $D > 0.5$ and a valley current-mode control with constant-on time for $D < 0.5$. Unlike constant-frequency current mode control [57], the constant on-time and constant off-time (T_{ON} and T_{OFF}) utilized in ACC-PFM suppresses the subharmonic oscillation for the entire duty ratio region without any slope compensation, simplifying the design complexity and circuit area for the controller. The developed controller not only supports output voltage regulation, but also facilitates capacitor balancing — the key objective of this work. The prerequisite for a balanced V_{CFLY} is that a dynamic capacitor charge equilibrium must have been achieved. In other words, the charges going into the flying capacitor should be equal to the charges going out, $\Delta Q_C = 0$, and this fundamental requirement can be satisfied in the ACC-PFM controller over the entire operating range ($D > 0.5$ and $D < 0.5$). The controller has an inherent negative feedback mechanism to compensate any variation in C_{FLY}, ΔV_{CFLY}, by adjusting the duty ratios and the phases of the switching signals to either remove or introduce excessive charge from / into the capacitor.

In a three-level boost converter, the charging and discharging process, states 3 and 4



(a) Duty ratio > 0.5: peak current-mode control with constant-off time



(b) Duty ratio < 0.5: valley current-mode control with constant-on time

Figure 6.4: Capacitor-compensation mechanism of the ACC-PFM controller over the entire operating range.

in Fig 6.2, of the flying capacitor are defined by the inductor current. The slopes of the inductor current, defined as m_{CHG} and m_{DCHG} in this work, characterize the capacitor charging and discharging rate. The charging and discharging current are obtained with a specific reference level based on the controller operating region. A complete illustration of the ACC-PFM control mechanism is shown in Fig. 6.4, and the mathematical derivations are further discussed in the following subsections.

Operating Region: Duty Ratio > 0.5

Fig. 6.4 (a) shows the peak current-mode operation of the controller with constant-off time for $D > 0.5$ region. The V_{CFLY} regulation is monitored through the total capacitor charge, i.e. the integration of capacitor current over time, which is indicated as the shaded regions under the inductor current waveforms. In this operating region, the capacitor charging and discharging intervals (T_{CHG} and T_{DCHG}) occur when one of the bottom MOSFETs are turned off and are represented as T_{OFF}. To investigate the regulation process, V_{CFLY} is initially assumed to be unbalanced, i.e. $V_{CFLY} > V_O/2$. The slopes of the inductor current ripple

can be expressed as

$$m_{CHG} = \frac{V_{CFLY} - V_{IN}}{L} \tag{6.2a}$$

$$m_{DCHG} = \frac{V_O - V_{CFLY} - V_{IN}}{L}, \tag{6.2b}$$

for intervals T_{CHG} and T_{DCHG}, respectively. Given the unbalanced condition, a higher voltage drop is generated across the inductor during T_{CHG}. As a result, m_{CHG} is steeper than m_{DCHG}, i.e. $|m_{CHG}| > |m_{DCHG}|$. When the inductor current, I_L, reaches the reference level for a peak current, I_P, the charging process is triggered with a constant-off time, T_{OFF}. Here, the average capacitor charging current over the charging interval is computed as

$$I_{CHG} = I_P - \frac{m_{CHG} \cdot T_{CHG}}{2}. \tag{6.3}$$

The discharging process occurs when the increasing I_L reaches I_P again, and the average capacitor discharging current is obtained as:

$$I_{DCHG} = I_P - \frac{m_{DCHG} \cdot T_{DCHG}}{2}. \tag{6.4}$$

Equations (6.3) and (6.4) highlight that the slope of inductor current is a determining factor for capacitor charging and discharging current. Thus, with $|m_{CHG}| > |m_{DCHG}|$ and the fact that $T_{CHG} = T_{DCHG} = T_{OFF}$, the average charging current is less than the average discharging current, $I_{CHG} < I_{DCHG}$. Consequently, the net charge into the capacitor, Q_{CHG}, is less than the net charge out of the capacitor, Q_{DCHG}, i.e. the area of shaded region in T_{DCHG} is larger than that in T_{CHG}. Excessive charges are therefore removed from the flying capacitor, eventually decreasing V_{CFLY} back to the desired value, $V_{CFLY} = V_O/2$. The inherent capacitor balancing mechanism can alternatively be expressed as the capacitor, ΔI_C, which can be computed by subtracting (6.4) from (6.3):

$$\Delta I_C = I_{CHG} - I_{DCHG} = \frac{(V_O - 2V_{CFLY}) \cdot T_{OFF}}{2L}. \tag{6.5}$$

For a perturbation, ΔV_{CFLY}, around the nominal voltage $V_O/2$, the net current can similarly be expressed as:

$$\begin{aligned} \Delta I_C &= \frac{\left[V_O - 2 \cdot \left(\frac{V_O}{2} + \Delta V_{CFLY}\right)\right] \cdot T_{OFF}}{2L} \\ &= \frac{-\Delta V_{CFLY} \cdot T_{OFF}}{2L}. \end{aligned} \tag{6.6}$$

The equation above implies that ΔI_C is proportional to negative ΔV_{CFLY}. This relationship demonstrates that the capacitor voltage can be balanced through a compensation net charge whenever there is an unbalanced condition.

Operating Region: Duty Ratio < 0.5

The valley current-mode control with constant-on time for $D < 0.5$ is illustrated in Fig. 6.4 (b). The similar approach used in $D > 0.5$ can be applied, but with the reference level replaced as the valley of the inductor current, I_V. Now, the capacitor charging and discharging intervals (T_{CHG} and T_{DCHG}) occur when one of the bottom MOSFETs are turned on, which defines T_{ON}. For the operating region of $D < 0.5$, the slopes of the inductor current can be expressed as

$$m_{CHG} = \frac{V_{IN} - V_{CFLY}}{L} \tag{6.7a}$$

$$m_{DCHG} = \frac{V_{IN} - V_O + V_{CFLY}}{L}. \tag{6.7b}$$

It can be observed that these slopes are the negation of (6.2), and the inductor is now magnetized during T_{CHG} and T_{DCHG}. With the reference level defined by I_V, the charging and discharging currents are derived as

$$I_{CHG} = I_V + \frac{m_{CHG} \cdot T_{CHG}}{2} \tag{6.8a}$$

$$I_{DCHG} = I_V + \frac{m_{DCHG} \cdot T_{DCHG}}{2}. \tag{6.8b}$$

Following the same procedures as (6.5) and (6.6), the net current to the capacitor can be expressed as

$$\Delta I_C = \frac{-\Delta V_{CFLY} \cdot T_{ON}}{2L}, \tag{6.9}$$

with $T_{CHG} = T_{DCHG} = T_{ON}$, the same relation between ΔI_C and ΔV_{CFLY} holds.

From (6.6) and (6.9), an intrinsic negative feedback loop between ΔQ_C and V_{CFLY} is established for the entire operating region. This feedback loop adaptively determines the amount of charge to compensate the flying capacitor, without the knowledge of input voltage and inductance. The ACC-PFM controller ensures that m_{CHG} and m_{DCHG} will eventually be self-aligned and maintain the flying capacitor voltage at around $V_O/2$. Note that even though only the case of $\Delta V_{CFLY} > 0$ is demonstrated, the derivations above also hold for $\Delta V_{CFLY} < 0$. In addition to the capacitor balancing, the proposed current-mode control algorithm for a three-level boost converter presumably has excellent rejection capability to line disturbance, with the help of input feedforward gain through the inductor current in the current mode control [82]. This is especially beneficial for energy harvesting applications, where the harvester output or the converter input varies depending on the environmental conditions.

Transient Time

The transient time, T_{tr}, for the proposed ACC-PFM algorithm can be estimated by the number of switching periods, N_{tr}, required to achieve the flying capacitor balancing:

$$T_{tr} = N_{tr} \cdot T_{sw}, \tag{6.10}$$

where N_{tr} can be further expressed as

$$N_{tr} = \frac{\Delta V_{CFLY}}{\delta V_C}. \tag{6.11}$$

The small change, δV_C, which can be expressed as

$$\delta V_C = \frac{Q_C}{C_{FLY}} = \frac{\Delta I_C \cdot T_{CONST}}{C_{FLY}}, \tag{6.12}$$

is brought by the negative feedback current, ΔI_C, of the proposed ACC-PFM controller, intending to reduce ΔV_{CFLY}.

Substituting either (6.6) or (6.9) into (6.12) and then (6.10) gives the expression for transient time:

$$T_{tr} = \frac{2LC_{FLY}}{T_{CONST}^2} \cdot T_{sw}, \tag{6.13}$$

which implies that the transient time for capacitor balancing can be further improved by smaller passives values or decreasing the constant on/off time [21] during a transient interval.

Feasibility in DCM Operations

Although Fig. 6.4 (a) and (b) mainly focus on continuous conduction mode (CCM), the three-level boost converter as well as the ACC-PFM are able to operate at discontinuous conduction mode (DCM), with the reverse inductor current prevented by zero current detection (ZCD) circuits. The switching schemes for the valley and peak current mode control are shown in Fig. 6.5, which demonstrates that the capacitor voltage can be balanced through a compensation net charge whenever there is an unbalanced condition.

- For $D < 0.5$, as shown in Fig. 6.5 (left), the valley current mode control with constant-on time, T_{ON}, at DCM works with the reference current, I_V, maintained at zero, meaning all switches are commanded off when the inductor current hits zero. The T_{ON} pulse is initiated as long as the output voltage goes below a reference voltage, $V_O < V_{ref}$. The capacitor compensation for $D < 0.5$ is still supported by (6.9). Given the constant T_{ON}, the example situation of $V_{CFLY} > V_O/2$ leads to higher discharging than charging current, thus the flying capacitor is auto-balanced.

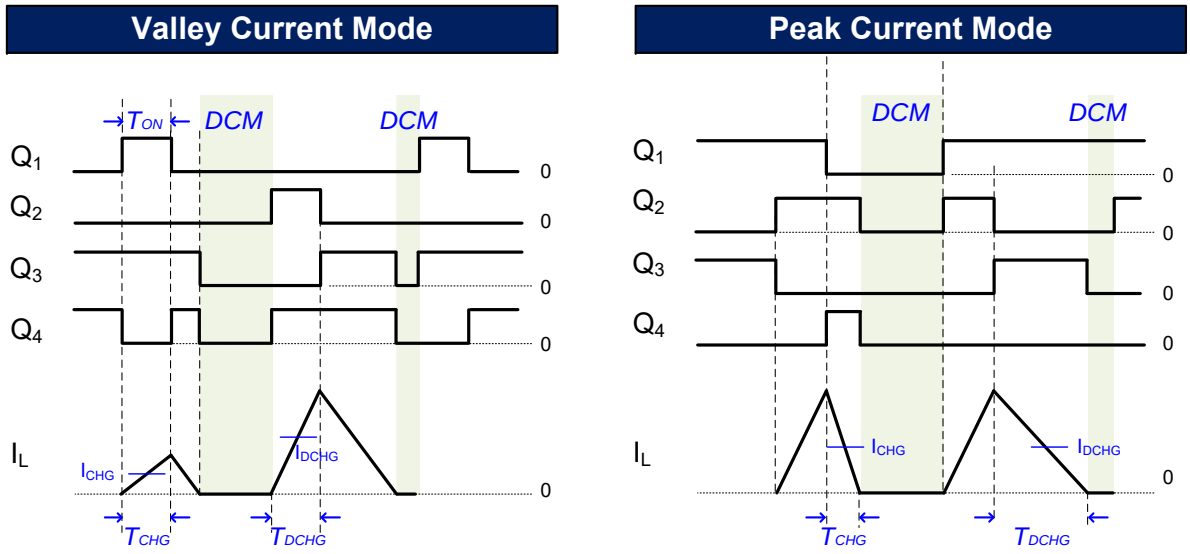


Figure 6.5: Auto-capacitor-compensation mechanisms of the ACC-PFM controller over the entire operating range during discontinuous conduction mode (DCM), where an unbalance is added to the flying capacitor: $V_{CFLY} > V_O/2$ for functionality illustration.

- For $D > 0.5$, the peak current mode control is still capable of doing auto-capacitor-compensation, but the off-time is determined by the zero inductor current instead of a constant value. As shown in Fig. 6.5 (right), the peak inductor current is still regulated by a reference current, I_P, but all switches are commanded off when the inductor current hits zero, irrelevant to a constant T_{OFF}. Due to the same boundaries set by I_P and 0, the charging and discharging current are the same, i.e. $I_{CHG} = I_{DCHG}$. Note that the charge, which is the product of current and time, determines the balance of the capacitor. For the case of $V_{CFLY} > V_O/2$, the slope m_{CHG} is steeper than m_{DCHG}, i.e. $|m_{CHG}| > |m_{DCHG}|$, and the charging time is thus shorter than the discharging time, i.e. $T_{CHG} < T_{DCHG}$, leading to more charge leaving from the flying capacitor.

6.3 Delay-Equalized Level Shifter (D-Eq LS)

Delay mismatch between driving signals for power MOSFETs has been identified as a major source of V_{CFLY} imbalance in hybrid SC converters [83]. This mismatch normally originates from uneven pull-up and pull-down strengths of the conventional level shifters (LS) [38].

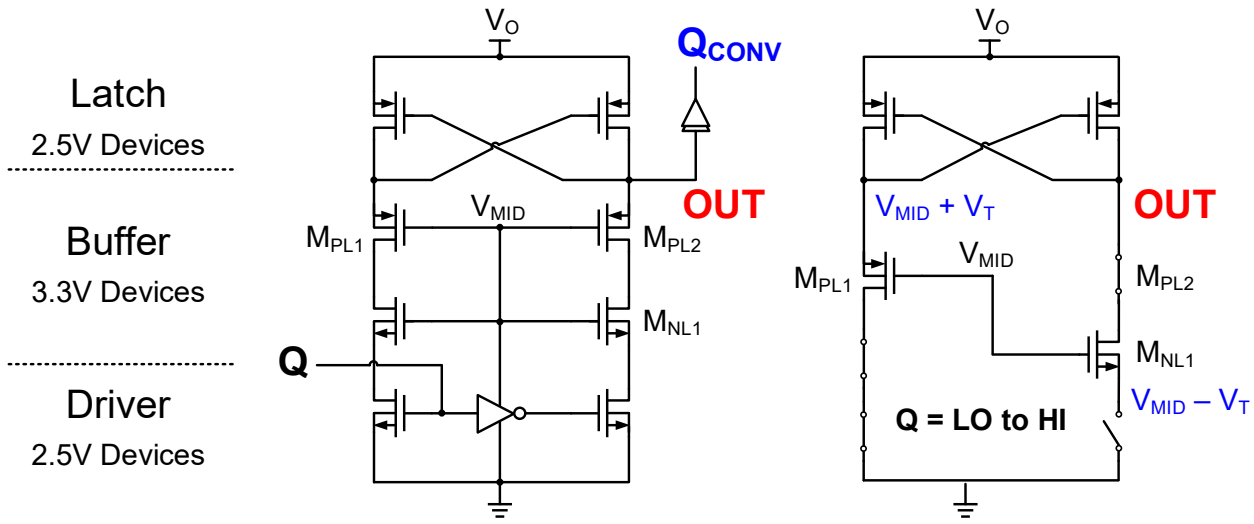


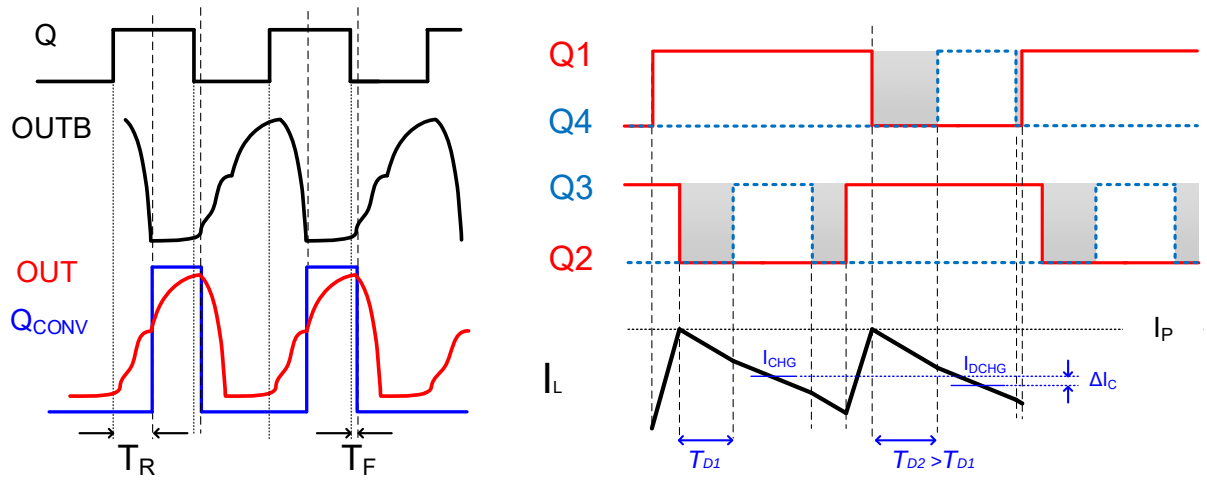
Figure 6.6: Long falling delays in a conventional stacked up level shifter.

Conventional Level Shifter

The schematic is shown in Fig. 6.6, and the pull-up strength is usually designed weaker to ensure that the PMOS will latch at the top without operating into metastability, resulting in a longer rising delay, T_R, than falling delay, T_F, and leading to deviations in duty ratio as shown in Fig. 6.7. The target specification for maximum V_O is 5V, while the available devices are with breakdown voltage of 2.5V and 3.3V. In the case of three-level converter, the 2.5V devices seem the best fit for all MOSFETs needed. However, as detailed operations of the level shifter shown in Fig. 6.6 (right), the blocking voltage for the middle buffer stage might get up to $V_O/2 + V_T$ ($V_{MID} \approx V_O/2$) due to the MOSFET clamping effect (MOSFET is cut off when $|V_{gs}| < V_T$), where V_T is the device threshold voltage. The 3.3V devices are thus selected for the buffer stage to protect the level shifter circuit from overstressed. Consequently, the rising delay increases when the middle stage is implemented using 3.3V devices with higher threshold voltage and higher RC constant (as compared to 2.5 V devices for the top and bottom switches), which worsens when the supply voltage, i.e. V_O, of the level shifter gets lower. The worst rising delay of 11 ns is obtained at the lowest supply voltage, i.e. $V_O = 2.5$V. The delays are longer and the feasible duty cycle region is narrower, becoming a limiting factor for high switching frequency operations.

Effects of Unequal Delays

Usually, the level shifters are employed for only floating power MOSFETs, i.e. M_{2-4} in the three-level boost converter; whereas the bottom power MOSFET, M_1, is grounded with no level shifter attached to its driving signal, Q_1. Hence, the rising and falling delays of Q_1 are shorter than that of Q_2, leading to a longer deadtime between Q_1 and Q_4 than that between



(a) Unequal delays of a conventional LS

(b) Adverse effect on converter operations

Figure 6.7: Effects of unequal delays by conventional level shifters.

Q_2 and Q_3, i.e. $T_{D1} < T_{D2}$. Fig. 6.7 (b) illustrates the effect of the unequal delays for the case of $D > 0.5$. Note that the inductor current is still going down during deadtime, since $V_O/2 + V_D (> V_{IN})$ appears at V_{SW}. As can be seen from Fig. 6.7, the rising/falling delay mismatch between Q_1 and Q_2 leads to a net charging current, $\Delta I_C = |I_{CHG} - I_{DCHG}|$, even though Q_3 and Q_4 have the same rising delays and the same falling delays. Similar case can be seen for $D < 0.5$. While a conventional level shifter can still be added and attached with Q_1 so that it has the same delays as Q_2, a long and redundant deadtime is unavoidable between Q_1 and Q_4; likewise, Q_2 and Q_3. This causes efficiency loss, especially when operating at high switching frequency. Therefore, to achieve the same duty ratios for all switching signals with higher frequency capability as well as to maintain full-range flying capacitor balancing, a delay-equalized level shifter is proposed, implemented and recommended for all four driving signals.

Modified Level Shifter

The D-Eq LS implemented in this chapter resolves unavoidable skewed delays in a conventional LS by an additional delay-equalizing (D-Eq) unit. This unit consists of inverter chains, one-shot generators and an SR-latch, and it is added at each output, OUT and $OUTB$, of the conventional LS. The inverter chains are designed identically, allowing the MOSFETs branches at OUT and $OUTB$ of the conventional LS to be sized symmetrically. With this matching load connected at each end, the possible discrepancy in driving strength between OUT and $OUTB$ in a conventional LS is minimized; as a result, the delays for resulting signals will be equal. Each of these signals is then sent into its corresponding one-shot generator. The negative edges generated by the one-shot circuitry will be utilized by the SR-latch differentially. Symmetric and shorter delays, new T_R and T_F, between Q_{LS} and

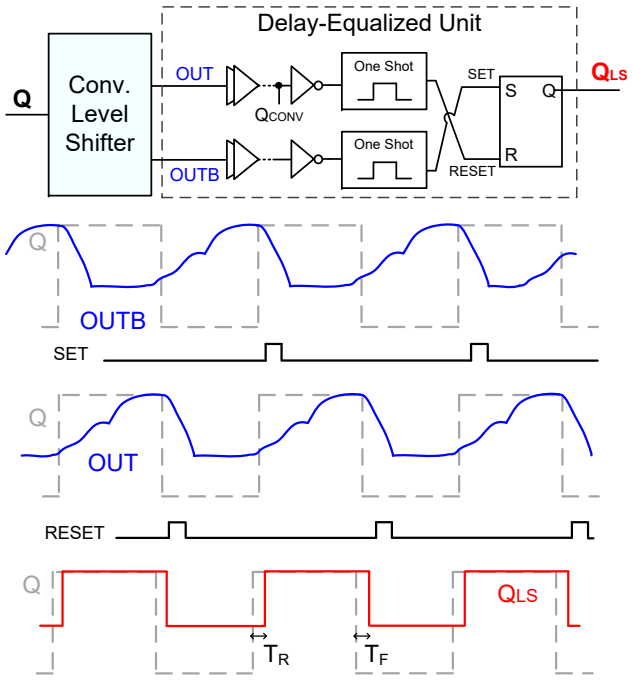


Figure 6.8: Delay equalized level shifter.

requested Q are eventually generated, as shown in Fig. 6.8. Thus, the complementary pairs $Q_{1,4}$ and $Q_{2,3}$ will have de-skewed delays with the least deadtime required without the issue of shoothrough. This ensures high frequency operation with only a few logic delays. The small discrepancy between new T_R and T_F achieved by Deq-LS reduces the inductor current ripple. Moreover, the area penalty by including this design is smaller than 5%. Thus, the D-Eq LS circuit is beneficial for any hybrid SC converters without a significant cost. It should be noted that as this converter topology requires well matched delays for good capacitor voltage balancing, the main focus was on matching the delay of the level shifters, not necessarily on obtaining the lowest possible delay.

6.4 Dual-Mode Timing Controller (DMTC)

The DMTC circuit shown in Fig. 6.9 manages the timing between the gate driving commands, Q_{1-4}, for both peak and valley current-mode controls. Several common circuits including two one-shot generators, an SR latch, a deadtime generator and a ramp generator, are shared between two different current-mode controls to save the die area. The configuration between current-mode controls is governed by digital multiplexors, with small area overhead, placed at the inputs of the SR latch and the ramp generator.

With $PV_{SEL} = 0$ for the peak current-mode control, the signals $COTSET\_RST$ from the ramp generator and RST_SET from the D-flip-flop (shown in Fig. 6.11 (a)) are connected to the S(et) and R(eset) inputs of the SR latch, respectively. The positive edges of RST_SET_1

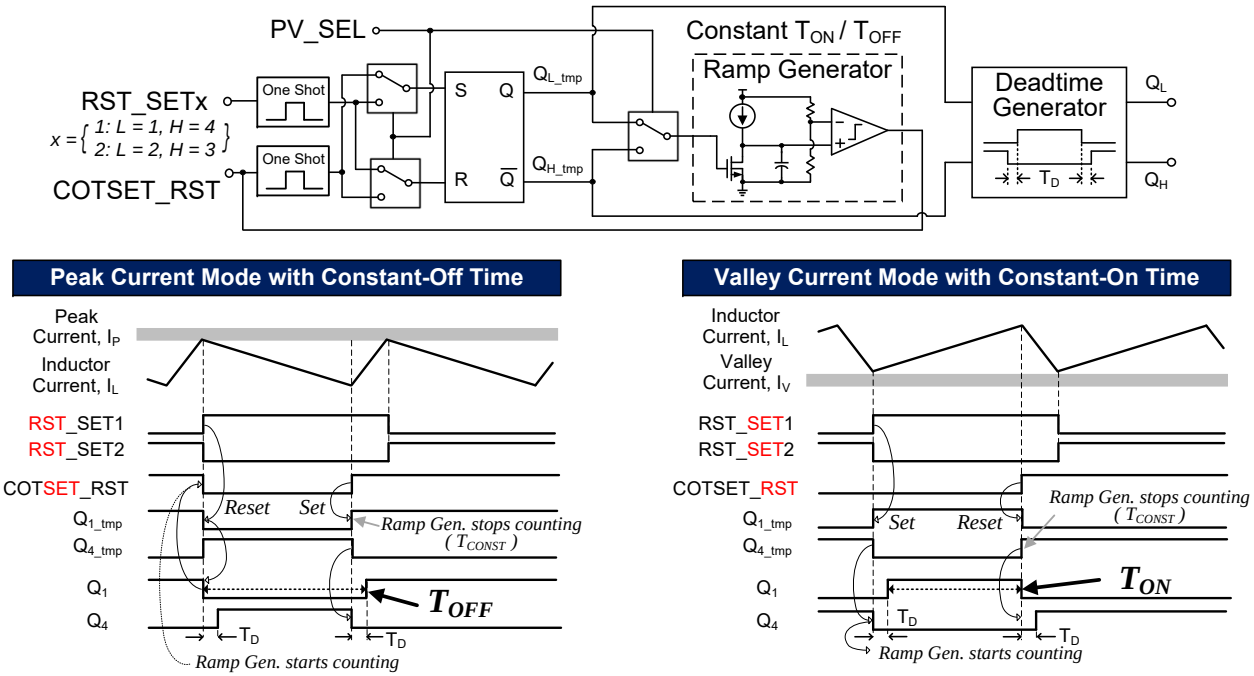


Figure 6.9: Dual-mode timing controller (DMTC).

resets Q_{1_tmp} as well as Q_1, but the immediate raise of signal Q_4 is suppressed until the deadtime, T_D, is reached. Meanwhile, the low level of Q_{1_tmp} kick starts the charging of the capacitor in the ramp generator. When the capacitor voltage is higher than a certain reference value, the output of the comparator, $COTSET\_RST$, is pulled high and Q_{1_tmp} is set high again, which defines the Q_{1_tmp}'s off-time by T_{CONST}. Similarly, the immediate raise of signal Q_1 is suppressed until the deadtime, T_D, is inserted after Q_4's falling edge. As a result, a constant-off time, $T_{OFF} = T_{CONST} + T_D$, for Q_1 and deadtime between $Q_{1,4}$ are generated. The state changes of another complementary pair, $Q_{2,3}$, is activated at the positive edge of RST_SET_2, following the same mechanism as for $Q_{1,4}$. In valley current-mode control, the condition of $PV_{SEL} = 1$ flips the inputs of the SR latch as well as the kick-start signal for the comparator of the ramp generator. The ramp generator starts counting at the low level of Q_{4_tmp}, which defines the turn-off time of Q_{4_tmp}. With the complementary feature between Q_{1_tmp} and Q_{4_tmp}, the off-time in Q_{4_tmp} is converted into the on-time in Q_{1_tmp}. Again, the on-time of Q_{1_tmp} is defined by T_{CONST} of the ramp generator. After the inclusion of deadtime, the actual constant-on time, T_{ON}, of Q_1 is $T_{CONST} - T_D$, as shown in 6.11 (b). Therefore, the DMTC circuit is capable of managing the timing of Q_{1-4} for both current-mode controls. Generated Q_{1-4} signals are then shifted up to drive the floating switches by D-Eq LS.

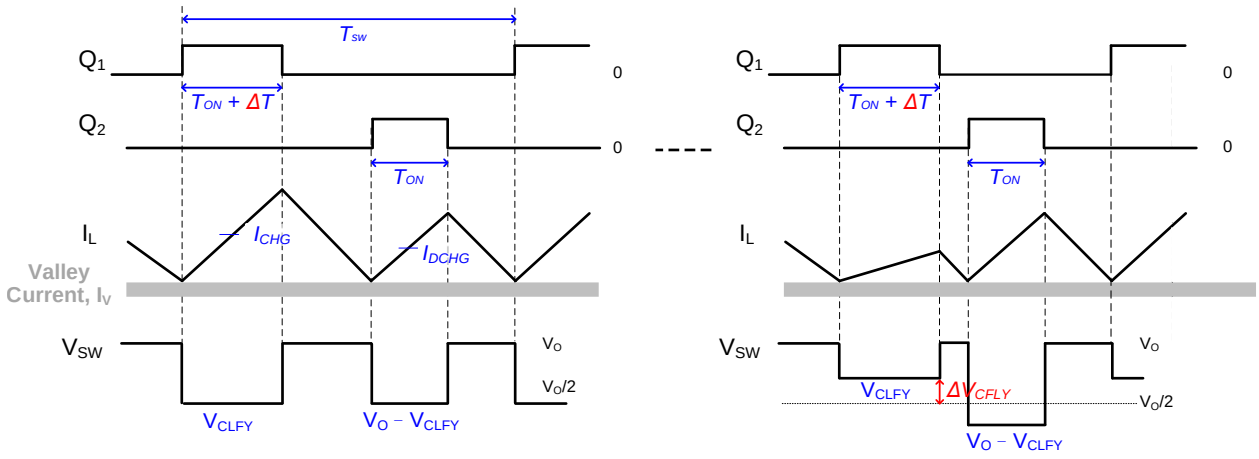


Figure 6.10: Possible inaccuracy of ACC-PFM controller at high switching frequency operations.

Accuracy and Balancing Error

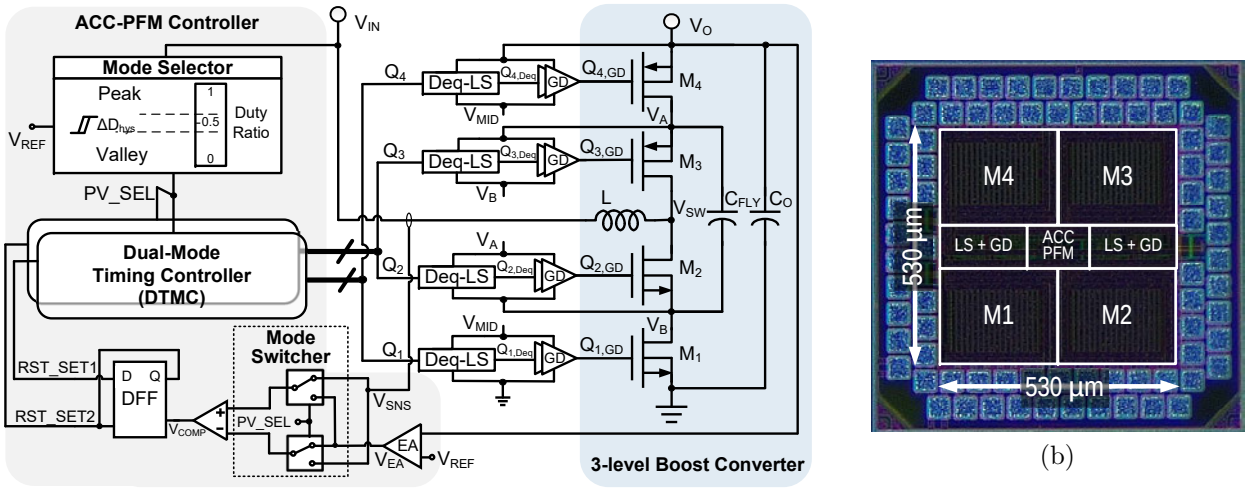
There are two types of errors that may exist in two sets of the timing controllers (DMTCs) while generating the constant time, T_{CONST}, for T_{ON} / T_{OFF}: (i) the two generated constant times are the same, but they are different from an expected value, i.e. $T_{CONST1} = T_{CONST2} \neq T_{CONST}$; (ii) the mismatch error between two constant times, i.e. $\Delta T = T_{CONST1} - T_{CONST2}$.

The first error will not lead to improper auto-capacitor-compensation mechanism, but the variation on the converter switching frequency. For the case of valley current mode control, the generated T_{ON} that is smaller than the expected will lead to a shorter switching period or a higher switching frequency, since $T_{sw} = T_{ON}/D$ with D maintained for the same input-output operating voltage. For the implemented chip, there is a certain tunable range for T_{CONST}, which can be calibrated to help maintain a more reasonable converter switching frequency.

The second error may lead to an inaccuracy in flying capacitor compensation, i.e. $\Delta V_{CFLY} = V_{CLY,new} - V_O/2$. The error or time mismatch, ΔT, might come from the process variations in the charging capacitance or the input offsets of the ramp generator in DMTC. Fig. 6.10 shows the effect of ΔT on the flying capacitor balancing error, ΔV_{CFLY}, while the converter is controlled by valley current mode for $D < 0.5$. To characterize the effect of ΔV_{CFLY}, it is helpful to look at the charge balance across the flying capacitor:

$$I_{CHG} \cdot (T_{ON} + \Delta T) = I_{DCHG} \cdot T_{ON}. \tag{6.14}$$

Substituting the expressions of charging, I_{CHG}, and discharging, I_{DCHG}, current for valley current mode control as expressed in (6.8) into (6.14) obtains an updated flying capacitor



(a) (b)

Figure 6.11: (a) Block diagram and (b) die micrograph of an ACC-PFM controlled three-level boost converter.

voltage, $V_{CFLY,new}$:

$$V_{CFLY,new} = \frac{V_O \cdot T_{ON}^2 + 2L \cdot I_V \cdot \Delta T + V_{IN} \cdot \Delta T \cdot (T_{ON} + \Delta T)}{T_{ON}^2 + (T_{ON} + \Delta T)^2}. \tag{6.15}$$

To observe the effect of ΔT at higher switching frequencies, the equation (6.15) is further normalized by T_{sw}, and can be derived as

$$V_{CFLY,new} = \frac{V_O \cdot D^2 + 2L \cdot I_v \cdot \Delta D + V_{IN} \cdot \Delta D \cdot (D + \Delta D)}{D^2 + (D + \Delta D)^2}. \tag{6.16}$$

The inaccuracy of the capacitor compensation algorithm can then be evaluated through $\Delta V_{CFLY} = \left|V_{CFLY,new} - \frac{V_O}{2}\right|$. In the most ideal case where very low ΔT is achieved or a lower switching frequency is applied, $\Delta D = \frac{\Delta T}{T_{SW}} \approx 0$ and $V_{CFLY,new}$ is calibrated to around $V_O/2$. As the switching frequency gets higher, the duty ratio variation, ΔD, becomes larger for a certain ΔT, leading to a higher ΔV_{CFLY} according to (6.16). The variation, ΔD, can be reduced by careful and symmetric layout or on-line trimming. Note that the case of valley current mode control is derived here; likewise, the derivations for the case of peak current mode control can be done.

6.5 Key Functional Blocks

The schematic of the three-level boost converter with ACC-PFM controller is illustrated in Fig. 6.11 (a). The four power MOSFETs are driven by $Q_{1-4,GD}$ through delay-equalized level shifters (Deq-LS) and gate drivers (GD). The ACC-PFM controller comprises three main

blocks: a mode selector, a mode switcher and two dual-mode timing controllers (DMTC) which generate the gate drive commands, Q_{1-4}. The mode selector generates a selection signal, PV_{SEL}, to assign the algorithm for the entire ACC-PFM controller: $PV_{SEL} = 0$ for employing the peak current-mode control with constant-off time and $PV_{SEL} = 1$ for valley current-mode control with constant-on time. The signal PV_{SEL} is generated based on the relations between the input voltage, V_{IN} and a reference voltage, V_{REF}: $PV_{SEL} = 0$ for $D > 0.5 + \Delta D_{hys}/2$, and $PV_{SEL} = 1$ for $D < 0.5 - \Delta D_{hys}/2$. Near $D = 0.5$, note that a hysteresis window, ΔD_{hys} is added to stabilize PV_{SEL} and prevent erratic mode transitions. For the case that duty ratio falls within $0.5 \pm \Delta D_{hys}/2$, the command D can be governed by voltage mode [57]. The mode switcher then determines the input polarities of the comparator for signals from V_{EA} and V_{SNS}, depending on PV_{SEL}. For instance, when $PV_{SEL} = 0$, the positive input of the comparator is connected to V_{SNS} and the negative input to V_{EA}, generating a logic-high pulse at V_{COMP} when the increasing inductor current, represented by V_{SNS}, reaches the programmed peak current, represented by V_{EA}. The positive edge of V_{COMP} triggers a D-flip-flop, leading to the state changes in signals RST_SET_1 and RST_SET_2. The result of RST_SET_1 is sent to the first set of DMTC circuit for the generations of the complementary switching signal pair of Q_1 and Q_4, while RST_SET_2 is used by the second DMTC set for the pair of Q_2 and Q_3. Within each complementary pair, a deadtime is also added between switching transitions to prevent the switch shoot-through.

Flying Capacitor Selection

When choosing the capacitor value, there are three main concerns: the efficiency, the package and the switch tolerance. Firstly, to achieve a lower conduction loss in a three-level boost converter, the switching frequency should be greater than the critical frequency [84]

$$f_{sw} > f_{crit} = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{FLY}}}. \tag{6.17}$$

Lower f_{sw} (hence lower switching loss) is possible for a larger product of $L \cdot C_{FLY}$, which however is limited by the whole package size. Many prior arts [9], [48] have shown that the co-package discrete capacitors are preferable for their better performance metrics as well as higher capacitance density over cost, especially for more advanced technology nodes. Considering the fabricated chip area (including pads) is around 0.85 mm x 0.85 mm, the best capacitor for co-package can be in 0402 package. Lastly, the capacitance along with the switching frequency determines the capacitor voltage ripple, $V_{FLY,ripple}$, which can be expressed as

$$V_{FLY,ripple} = \max\left[\frac{I_O \cdot D \cdot (1-D)}{f_{sw} \cdot C_{FLY}}\right] \tag{6.18}$$

The maximum $V_{FLY,ripple}$ happens when $D = 0.5$. The output voltage range of the power converter benefits from lower $V_{FLY,ripple}$ and therefore lower blocking voltage across power switches. While the highest capacitance available on the market is 22 μF for the 0402

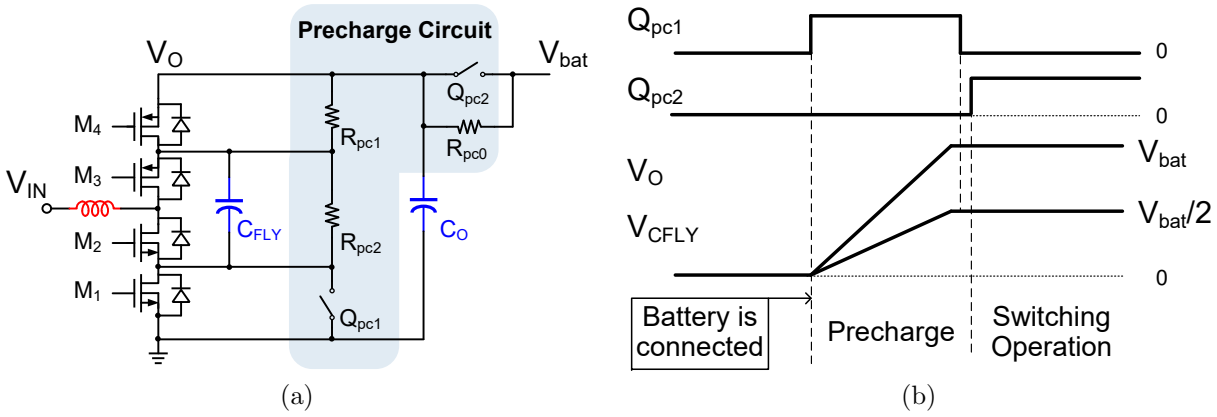


Figure 6.12: Precharge circuit for three-level boost converters.

package, the value for C_{FLY} be chosen to be lower, with very minor decreases in efficiency. In this work, we are focusing to demonstrate a high-efficiency and high-output-voltage three-level boost converter, as well as the full-range flying capacitor balancing algorithms.

Precharge and Start-up

Startup is a concern for all multi-level and switched-capacitor power converter, and although not a specific focus of this work, an off-chip assisted startup technique was implemented. All four power MOSFETs ($M_1 - M_4$) are nominally rated 2.5 V, with 10-20% tolerance to their absolute ratings. To ensure a smooth start-up for a three-level boost converter, as shown in Fig. 6.12 (a), a precharge circuit, composed of two auxiliary switches (Q_{pc1} and Q_{pc2}) and three auxiliary resistors (R_{pc0}, R_{pc1} and R_{pc2}), is implemented externally. In the measurement, both R_{PC1} and R_{PC2} are chosen to be 100 kΩ, so that the relevant power consumption, P_{pc}, is maintained below 1 % of the total output power at the worst-case scenario, i.e. the highest output V_O, the largest D and the lightest load. The switching scheme for the auxiliary switches and the key waveforms are shown in Fig. 6.12 (b). The precharge process begins once the battery, V_{bat}, is connected to the circuit and Q_{pc1} is turned on. The slew rates of V_{CFLY} and V_O are intentionally set to around 1-to-2, same for the final values. This ensures similar lower blocking voltage, i.e. $\approx V_O/2$, for all power switches, M_{1-4}. As long as V_O is close enough to V_{bat}, Q_{pc2} turns on and the three-level boost converter is ready for switching operation. In steady state, each power switch will nominally sustain around $V_O/2$ and up to $V_O/2 + V_D$ if body diode voltage drop is considered.

Several other precharging ways can be considered. One of that is connecting the converter to the input voltage before the output voltage comes in; meanwhile, turning on M_1 and M_3 prechargs the flying capacitor to the input voltage. However, this will require the input voltage to be higher than $V_O - V_{MOS,block}$. Last but not least, reconsidering the case of direct battery connection, the switches might survive if the top and bottom switch (M_4 and M_1) have some certain ratio of output capacitance, C_{oss}. While all switches are turned-off and

in high impedance, a step voltage change at V_O of the power converter will induce charge sharing between C_{oss1-4} and C_{FLY}. Those charge will mainly go through C_{oss1}, C_{oss4} and C_{FLY}, since C_{FLY} is much larger than the series impedance of C_{oss2} and C_{oss3}. Regarding the capacitive voltage divider mainly formed by C_{oss1}, C_{oss4} and C_{FLY}, the voltage at V_A and V_B can be expressed as

$$V_A = \frac{\frac{1}{sC_{oss1}} + \frac{1}{sC_{FLY}}}{\frac{1}{sC_{oss1}} + \frac{1}{sC_{oss4}} + \frac{1}{sC_{FLY}}} \cdot V_O \approx \frac{V_O}{2} \tag{6.19a}$$

$$V_B = \frac{\frac{1}{sC_{oss1}}}{\frac{1}{sC_{oss1}} + \frac{1}{sC_{oss4}} + \frac{1}{sC_{FLY}}} \cdot V_O \approx \frac{V_O}{2}, \tag{6.19b}$$

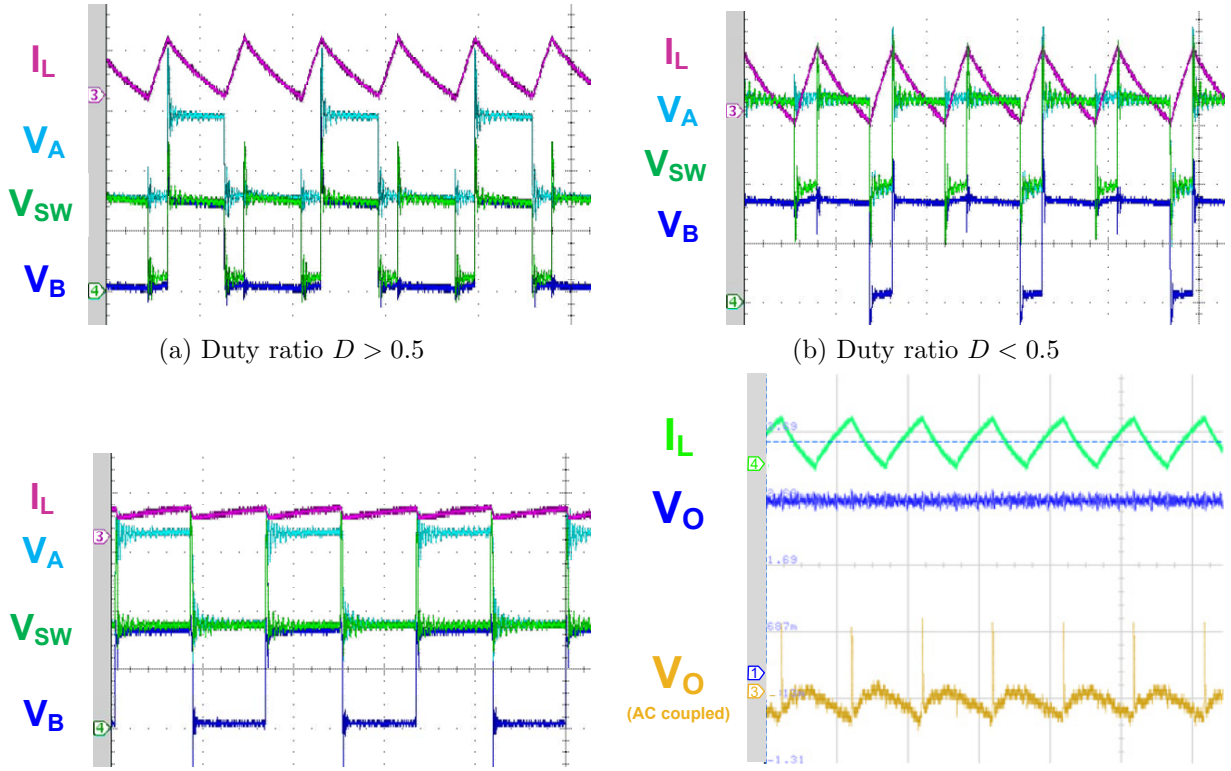
where reasonable assumptions of $C_{FLY} \gg C_{oss1}, C_{oss4}$ and $C_{oss1} \approx C_{oss4}$ are made. Therefore, the blocking voltage across each switch is still within rated voltage and survived from the direct battery connection.

Feasibility of Digital Implementation

A fully digital implementation is possible for this converter, and its programmability and flexibility would bring in features like adaptive on-time for on-line optimization in efficiency performance and dynamic response [16], [85]. However, turning the proposed controller into its digital version requires ADCs for converting three analog signals (V_{IN}, V_{OUT} and I_L) into digital forms, and oscillators or pulse generators are necessary for implementing the sampling-and-hold function in those ADCs. To evaluate the efficiency for the power converter using a full digital controller, the power loss overhead brought by the ADCs should be taken into consideration, as well as their performance index including number of bits (resolutions) and conversion rate (speed). For example, the power loss can be a few mW per SAR ADC with 8 to 10 bits and more than 100 MSPS sampling rate [86], [87], which may contribute significant efficiency loss during light load condition. In general, a fully digital implementation would be more feasible for higher output power with more aggressive frequency scaling at light load condition.

6.6 Measurement Results

A converter prototype is implemented using 65 nm bulk CMOS process with an active die area of 0.28 mm^2, as shown in Fig. 6.11 (b). The passives used in the converter include two 22 μF capacitor (0402 package, for C_{FLY} and C_O) and a 1 μH inductor. The converter has been tested at various duty ratios in ranges including $D < 0.5$ and $D > 0.5$, with excellent flying-capacitor voltage balancing and gate-drive functionality. The measurement results of steady-state waveforms are shown in Fig. 6.13: V_A indicates the top-plate flying capacitor voltage, V_B is the bottom-plate flying capacitor voltage, V_{SW} is the switching node voltage, and I_L is the inductor current. The V_{SW} pulses are observed to be twice the frequency of



(a) Duty ratio $D > 0.5$

(b) Duty ratio $D < 0.5$

(c) Duty ratio $D \approx 0.5$

(d) Duty ratio $D \approx 0.5$

Figure 6.13: Steady-state waveforms when (a) duty ratio > 0.5, (b) duty ratio < 0.5, and (c) duty ratio ≈ 0.5. (d) Output voltage ripple when duty ratio > 0.5. The scales for waveforms are as follows, time: $1\mu s$/div, I_L: 200 mA/div, V_A: 1 V/div, V_B: 1 V/div, V_{SW}: 1 V/div, V_O (AC coupled): 20 mV/div.

V_A and V_B, along with a $2X$ effective frequency of the inductor current ripple. The output voltage ripple for the case of $D > 0.5$ is also shown in Fig. 6.13(d), with an amplitude of 10 mV. In addition to the capacitor ripple voltage, there is a ringing voltage caused by the parasitic inductance between the chip's output node and the external output capacitor, which can be reduced by more compact packaging or on-chip passives integrations [38], [47], [49].

Ringing Issues

The ringing of the implemented chip is mainly caused by the parasitic inductance in the connection between the flying capacitor. As compared to conventional boost converters, the three-level boost converter has two more high-frequency switching nodes, i.e. V_A and V_B, in addition to V_{SW}. In our case, the most available package is 1cm x 1cm QFN, leading to a parasitic inductance around 2 nH on both sides of the flying capacitor and thus higher ringing voltage between switching transitions can be expected. Even though the ringing

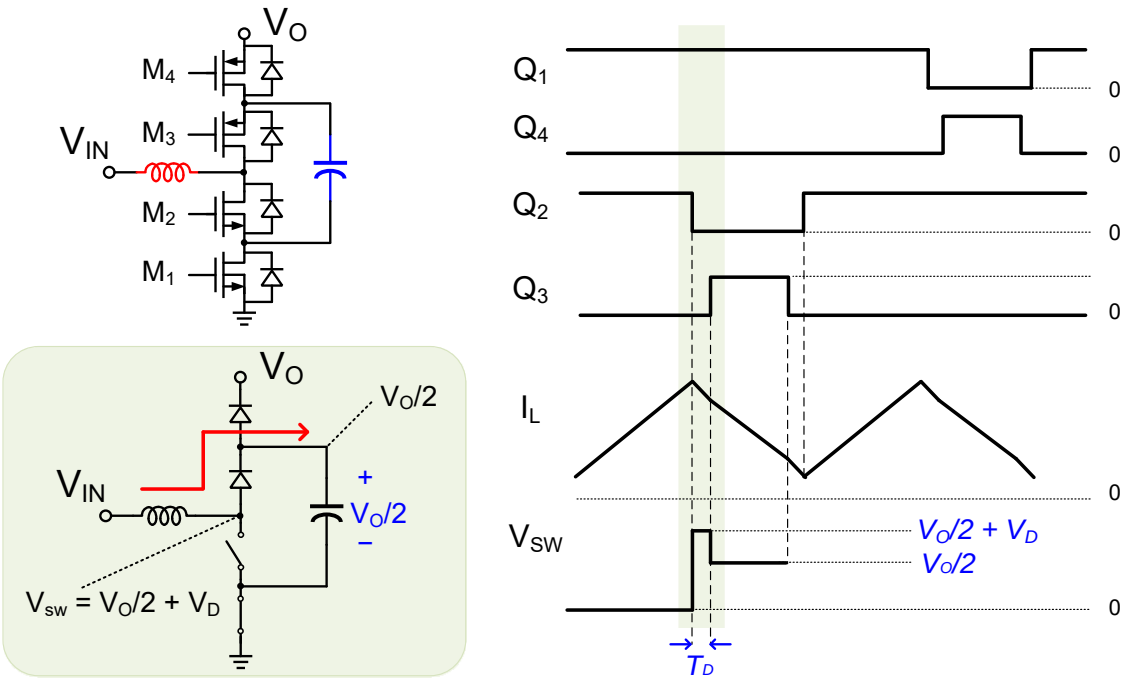


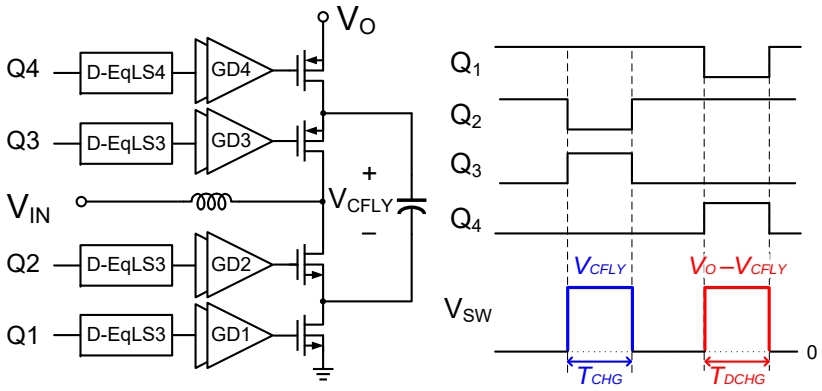
Figure 6.14: Body diode conduction and overshoot at V_{SW} of a three-level boost converter.

can be damped by less aggressive design in the gate driver strength, the efficiency would be compromised as well as the high-frequency operation capability. The best way of reducing the ringing voltage is shortening any connection to the flying capacitor. Many solutions including compact packages or fully integrated chips [38], [47], [49] have showcased significant parasitics reduction.

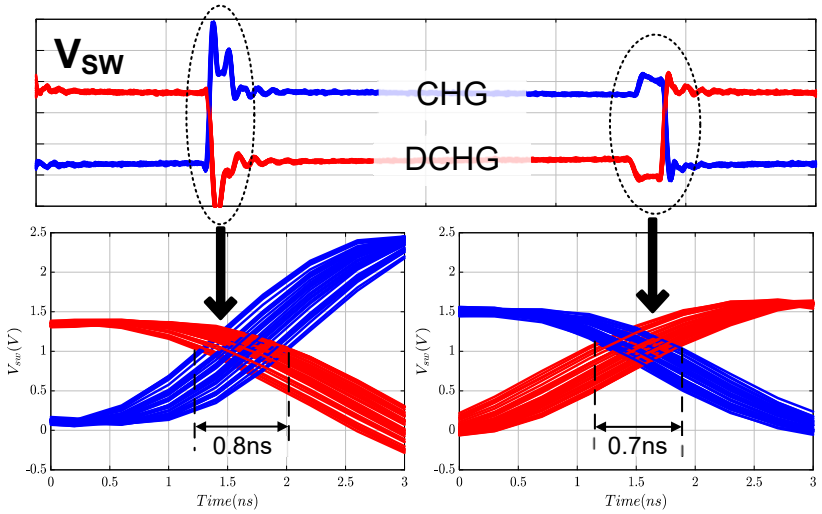
Apart from the parasitics ringing, another element that determines the amplitude of the overshoot is the conducted body diode voltage (V_D). In an ideal case without any parasitics, upper body diode of M_3 or M_4 is conducted with a positive inductor current. The equivalent circuit and operational waveforms are shown in Fig. 6.14. During the deadtime between Q_2 and Q_3, the three power MOSFETs (M_2, M_3 and M_4) are turned-off with blocking voltage of $V_O/2 + V_D$, V_D and $V_O/2$, respectively. Similarly, M_1 will also see $V_O/2 + V_D$ during the deadtime between Q_1 and Q_4, given a positive inductor current. The same phenomenon happens in conventional boost converters, where the lower switch experiences a blocking voltage of $V_O + V_D$.

Validation of D-Eq LS

An example of the switching schemes, when $D > 0.5$ as shown in Fig. 6.15 (a), is employed to investigate the rising and falling delays of the proposed D-Eq LS circuit. The switching transitions between Q_2 and Q_3 lead to the charging state, i.e. state 3, of C_{FLY} while the



(a)



(b)

Figure 6.15: (a) Switching scheme for (b) measured V_{SW} eye diagram showing duty ratio deviation between CHG and DCHG states (i.e. states 3 and 4) given the same duty ratio for Q_1 and Q_2.

transitions between Q_1 and Q_4 lead to the discharging state, i.e. state 4; the V_{SW} pulse during T_{CHG} and T_{DCHG} can therefore be used as an alignment indication of those level-shifted gate driving signals. With this information, cycles of V_{SW} pulses at T_{CHG} are overlapped with the inverted, 180° phased shifted V_{SW} pulse at T_{DCHG} to generate an eye diagram shown in Fig. 6.15 (b). Since Q_1 and Q_2 are 180° out of phase and their duty ratio are commanded to be same, the transitions overlapped regions imply the duty ratio deviation between charging and discharging states. This deviation is normally dominated by the long rising delays; with D-Eq LS, it is measured to be within sub-ns regions even in the worst case of operating at the lowest working voltage (i.e. $2.5V$), as compared to the delays in conventional LS ($\approx 11ns$ in post-layout simulation).

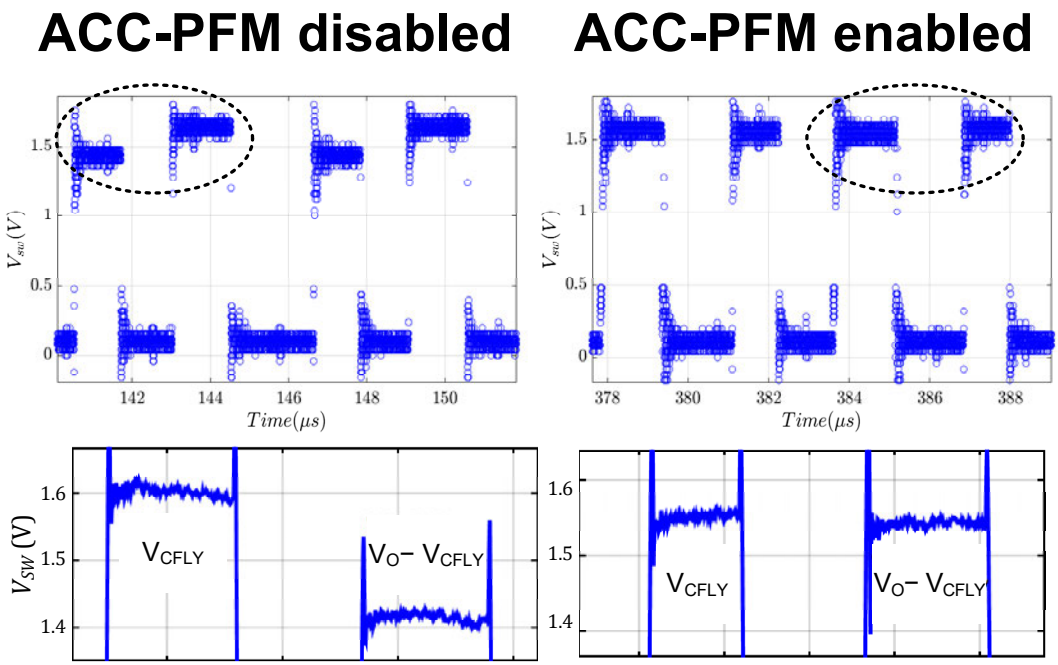


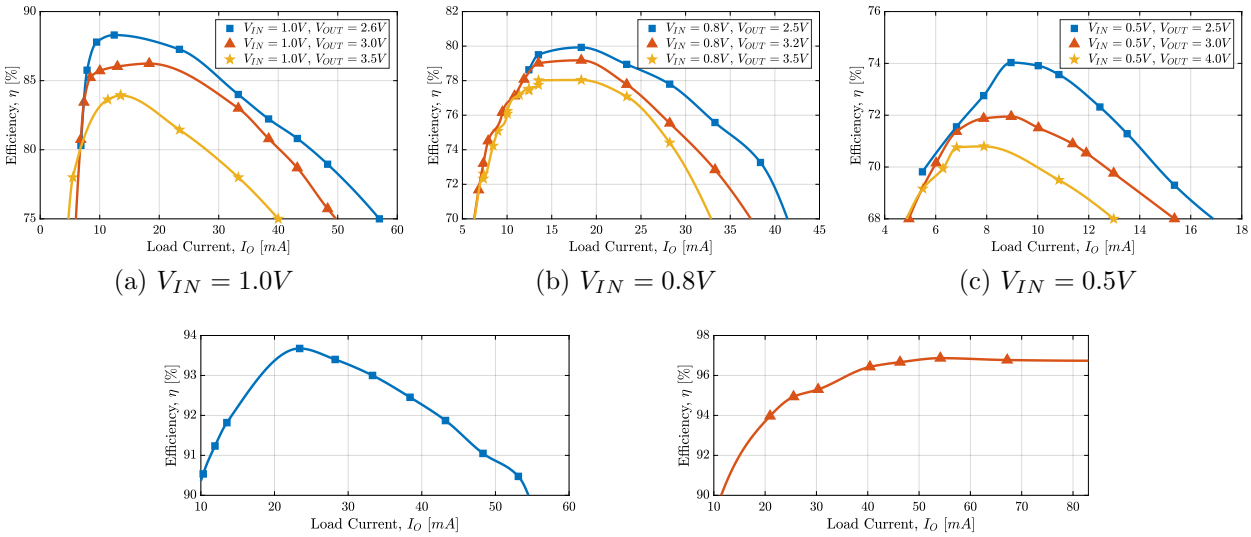
Figure 6.16: Validation of the ACC-PFM's capacitor balancing mechanism. Measured pulse-heights that are even demonstrate effective balancing.

Validation of ACC-PFM Controller

The ACC-PFM mechanism is validated by initially introducing a positive ΔV_{CFLY} disturbance to the flying capacitor, i.e. $V_{CFLY} > V_O/2$. It is observed that when the three-level boost converter operates with a constant duty ratio, i.e. the ACC-PFM controller is disabled, the V_{CFLY} will stay unbalanced; however, as can be seen from the experimental measurements shown in Fig. 6.16, the V_{SW} pulses, representing V_{CFLY} and $V_O - V_{CFLY}$, converges to $V_O/2$ after the ACC-PFM controller is enabled. This demonstrates that more discharging current is generated to remove excessive charge from the flying capacitor, supporting the theoretical analysis in Section III. It is measured that ΔV_{CFLY} can be eliminated within $250\mu s$ transient time and 1% balancing error, both of which can be reduced through an adaptive on/off-time scheme [21] and a more symmetric layout for two sets of DMTCs, respectively. Further derivations and clarifications for the transient time and the balanced error of the ACC-PFM algorithm are provided in Appendix.

Efficiency Measurement

The switching frequency and switch sizing are design parameters that reflects the trade-off between conduction loss and switching loss. To better understand the efficiency, the power



(a) $V_{IN} = 1.0V$ (b) $V_{IN} = 0.8V$ (c) $V_{IN} = 0.5V$

(d) $V_{IN} = 2.0V$ and $V_O = 4.7V$ (e) $V_{IN} = 3.0V$ and $V_O = 4.0V$

Figure 6.17: Measured efficiency versus load current with various $V_{IN} - V_O$ conditions.

losses of this converter can be expressed as follows:

$$\begin{aligned} P_{loss} &= \text{① DC conduction loss } (\propto R_{on} \text{ and DCR}) \\ &= \text{② Ripple conduction loss } (\propto 1/f_{sw},\ R_{on} \text{ and DCR}) \\ &= \text{③ Gate driver loss } (\propto C_g V_g^2 \cdot f_{sw}) \\ &= \text{④ VI overlap loss } (\propto I_{ds} V_{ds} t_{on/off} \cdot f_{sw}). \end{aligned} \tag{6.20}$$

High switching frequency (f_{sw}) helps decrease ②, while increasing ③ and ④. To achieve a better efficiency at a certain f_{sw}, the optimization between ①-④ needs to be done when sizing the power MOSFETs. For example, a narrower power MOSFET is selected for lower ③ and ④ considering a lower gate capacitance, C_g, and lower turn-on/off time, $t_{on/off}$ (mainly caused by the MOSFET output capacitance C_{oss}). However, the current capability is limited since ① increases with the power MOSFET on-resistance, R_{on}. Given the tradeoff between different sources of power losses, an efficiency optimization is mainly done around 1 MHz to 2 MHz in our chip. For achieving better performance, any advanced control techniques like segmented power MOSFETs and phase-shedding scheme [88] can be applied to maintain higher efficiency at wider load range.

The efficiency has been tested up to 45 MHz with operational functionality. The switching frequency also varies to lower values at light load condition to reduce the gate driver loss and increase the efficiency. Various efficiency plots are shown in Fig. 6.17 to demonstrate the performance of the converter prototype in wide conversion ratios, ranging from 1.3 to 8.0. Fig. 6.17 (a)-(c) show that the implemented three-level boost converter is able to regulate to different output voltages, given a constant input voltage, while maintaining its efficiency. Fig. 6.17 (d)-(e) show that this prototype has the ability to achieve an efficiency of more

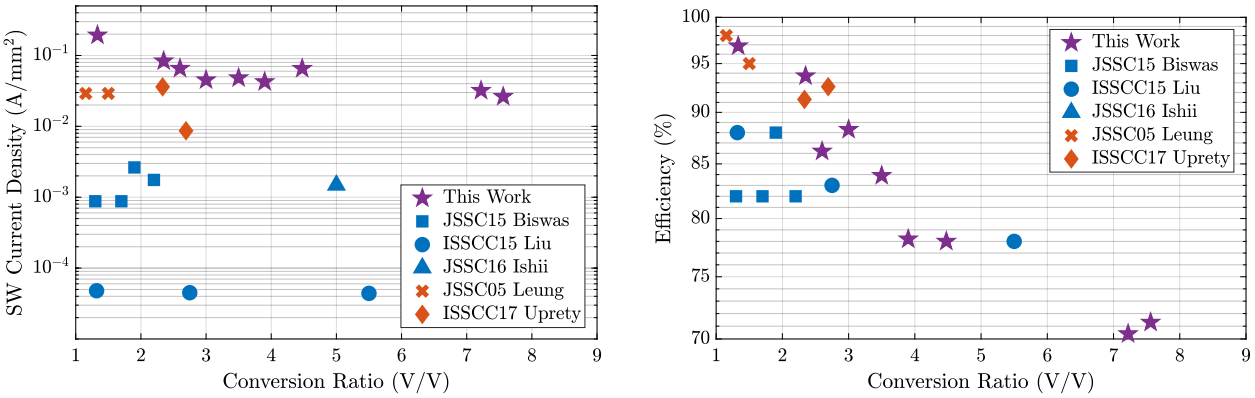


Figure 6.18: Efficiency versus conversion ratio compared to prior arts. Color code: purple - this work (three-level boost converter), red - conventional boost converter, blue - switched capacitor converter.

than 90% at various load conditions. The peak conversion ratio is measured to be 8, when $V_{IN} = 0.5V$ and $V_O = 4.0V$, with its highest efficiency of 74%. The overall peak efficiency and peak current of the converter are measured to be 96.8% and $83mA$, respectively, when $V_{IN} = 3.0V$ and $V_O = 4.0V$. Note that the measured output voltage in Fig. 6.17 ranges from 2.5 V to 4.7 V, which shows that the designed chip is not only suitable for a typical Li-ion battery, i.e. 3 to 4.2 V operating voltage, but also allows more margins for possible voltage spikes or batteries with very low or very high state of charge (SOC).

Electro-Magnetic Interference (EMI) Issue

Regarding the wide frequency range brought by PFM and the relevant EMI issue, the target design frequency in this work was 1-2 MHz, while it is desired to demonstrate that the key components and concepts could operate all the way up to 45 MHz. In a commercial implementation, one would likely choose to operate in a more narrow frequency range, or utilize any of the many EMI mitigation techniques that have been developed to handle the relatively wide range associated with light-load control. One of them is an adaptive on/off time with selective and discrete frequency hopping [89], which simplifies the EMI filter design. The spectrum of the switching noise tone can be further spread out and lowered by dithering the switching frequency [90]. Last but not least, a growing research in active EMI filter [91] have potential in minimizing the EMI issue by a pre-known frequency signal from the converter with variable frequency operations.

Comparison with Prior Arts

Table 6.1 summarizes the performance of our prototype and state-of-the-art on-chip conventional boost converters and SCs. Fig. 6.18 further compares prior designs with the focus on

Table 6.1: Performance Comparison with the State of the Arts.

	This Work	**ISSCC17 Uprety [24]**	**JSSC16 Ishii [4]**	**JSSC05 Leung [23]**	**JSSC16 Liu [12]**	**JSSC15 Biswas [11]**
Topology	3-level Boost	Boost	Boost	Boost	SC	SC
Input Voltage $[V]$	$0.3-3$	$0.5-2.4$	$0.6-1.0$	$1-1.3$	$0.45-3$	1
Output Voltage $[V]$	$2.4-5.0$	3.5	3	1.5	3.3	$1-2.4$
Peak Meas. Conversion Ratio $[V/V]$	8	2.7	5	1.5	5.5	2.2
Peak Output Current $[A]$	$83m$	$294m$	$0.4m$	$150m$	$0.015m$	$1m$
Peak Efficiency	96.8%	91.3%	52.5%	95.5%	89%	88%
Switching Freq. [Hz]	$0.5M-45M$	$1M$	$800k^{\dagger}$	$100k$	$20k-1M$	$0.5M-200.5M$
Active Area [mm^2]	0.28	$1.98^{\dagger}$	0.27	$3.09^{\dagger}$	$0.31^{\dagger}$	0.114
Process	CMOS $65nm$	CMOS $0.35\mu m$	CMOS $0.18\mu m$	CMOS $0.6\mu m$	CMOS $0.18\mu m$	FDSOI $28nm$

† Estimated from measurement results or die photo

efficiency and conversion ratio. It can be noticed that the three-level boost converter achieves excellent switch current density and high efficiency across various voltage and load conditions. The main advantage of a three-level boost converter is the elimination of the charge sharing loss in SC approaches, hence lower switching frequency is possible in achieving higher efficiency over wide-range output regulation. While the switched-capacitor approaches can be made to achieve multiple conversion ratios [11], [12], the switch current density as well as the heavy-load efficiency (dominated by switch on-resistance) are significantly reduced since many more switches are needed for different circuit configurations. At low conversion ratios, both this work and conventional boost converters have higher efficiency than that of SC; yet, this work accomplishes a higher current density than that of conventional boost converters due to inductor current ripple reduction. In addition to that, this work further extends the feasible conversion ratio to 8, which is a wider operating region compared to SC. With its achievements in both power density and efficiency, the three-level boost converter has the potential to push its wider applications for step-up power conversions.

6.7 Chapter Summary

The unique challenges associated with the step-up operation and the balanced flying capaitor voltage, V_{CFLY}, across input voltage, output voltage, and inductance variations are addressed in this work by an implementation of a three-level boost converter. Additionally, the flying capacitor balancing mechanism in the proposed ACC-PFM controller is analyzed with mathematical derivations in this work. The inherent negative feedback between ΔV_{CFLY} and ΔQ_C in the ACC-PFM controller is established. The hybrid approach employed in ACC-PFM, i.e. peak current-mode control with constant-off time when $D > 0.5$ and valley current-mode with constant-on time when $D < 0.5$ for a three-level boost converter, establishes a balanced V_{CFLY} together with a full-range output voltage regulation. The duty ratio deviation caused by level shifting, which is also one of the root causes for unbalanced V_{CFLY}, is reduced to sub-nanoseconds through the D-Eq LS. This ensures a balanced V_{CFLY} for converter operation, especially in higher switching frequencies. As high-efficiency and high step-up voltage are difficult to achieve using low-voltage CMOS process, this work illustrates a robust, wide load-range and self-balanced three-level boost converter that demonstrates significant performance improvement.

Chapter 7

Multi-stage Approach for High Conversion Ratios

Power converters with high conversion ratios are unavoidable owing to the efficiency pushes from perspectives of both power delivery and digital circuit. An example for the power converters in data-center applications is shown in Fig. 7.1 (a), where the input voltage is increased to lower source connection conduction loss (more than 48 V) and the output voltage is decreased to lower switching loss (down to 1 V or even below).

In order to extend to higher conversion ratios, several SC topologies were recursively generated in Chapter 4. Many of them are implemented and published, e.g. series-parallel [92], Dickson [28], [33], [35], cascaded [27], FCML [36], ladder [93], demonstrated excellent performance for non-isolated, non-regulated applications with soft-charging or resonant operations. While there are single-stage power conversions addressing the high conversion ratios through direct point-of-load (PoL) conversion (from 48 V to below 1 V) [35]–[37], multi-stage approaches [26], [32]–[34] are also attractive with its divide-and-conquer strategy. As shown in Fig. 7.1 (b), by cascading bus converter and POL converter, multiple stringent specifications can be achieved by individual stages: (i). the bus converter focuses on improving the conversion ratio and efficiency, and (ii). the PoL converter provides stable output regulation. Many of the bus converters [27]–[31] have shown excellent performance for 48-to-12 V conversion. However, high switch VI stress and large inductance required by the PoL converter sets a limit to the overall performance. To address that, a bus converter with higher conversion ratios can ease the stress on the PoL converter. Meanwhile, to maintain high output conductance density, the multi-stage approach can be re-applied to the bus converter with its promise for lower total component counts.

In this work, an example of two-stage ReSC is implemented: as shown in Fig. 7.1 (b), the first stage is responsible for high input voltage, and the second stage for high output current. The first stage employs a 2-to-1 ReSC converter, which shows high performance as demonstrated in [27]. However, as the voltage domain goes lower, more cascaded stages of 2-to-1 ReSC converters leads to low output conductance density considering the atypical scaling trend of commercial power transistors in low voltage domain, i.e. $\text{Volume}_{sw} \not\propto G_{on}V_{rated}^2$,

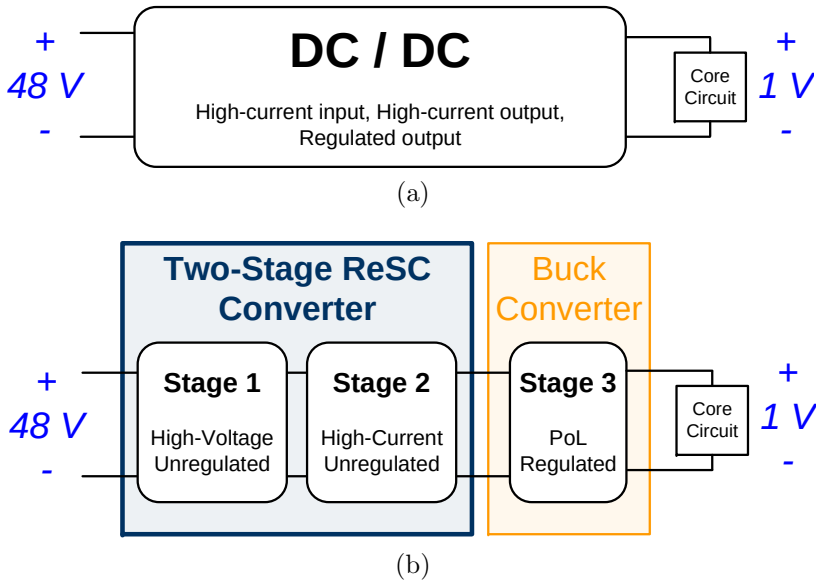


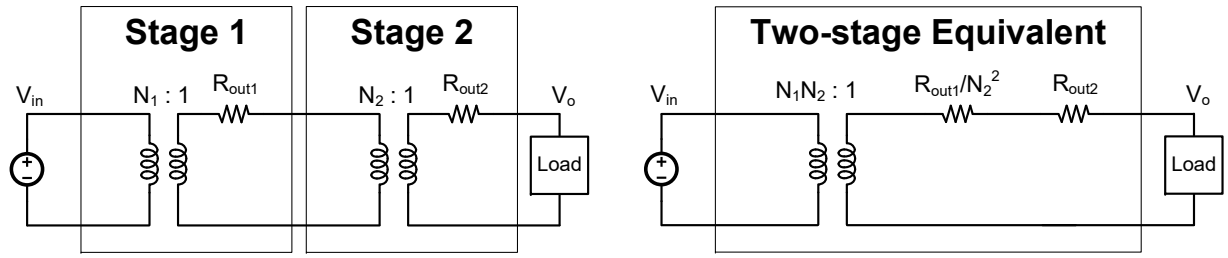
Figure 7.1: Dc/dc interface structures and requirements for data center applications using (a) single-stage and (b) multi-stage power conversions.

where G_{on} and V_{rated} are the switch conductance and rated blocking voltage, respectively. Therefore, as suggested by Fig. 4.10 and Fig. 4.12 (b), the series-parallel topology is selected for the second stage due to its high output conductance density. In addition to eliminating the charge sharing loss associated with conventional SC converters (i.e., achieving "soft charging" [25], [39]), ReSC converters have the ability to operate with soft switching. The intrinsic zero current switching (ZCS) operation by two-phase control will be introduced, together with a proposed zero voltage switching (ZVS) technique for light load efficiency improvement. Several capacitor-based floating supplies are developed to provide area-efficient and power-efficient gate driving techniques.

7.1 Output Impedance for Multi-stage Approaches

The multi-stage approach can significantly reduce the number of components and control signals in achieving higher conversion ratios with a smaller volume, as compared to the single-stage approach. Meanwhile, it is also important to characterize their output impedance in order to evaluate ρ_{gout}. In the multi-stage approach, multiple stages are cascaded together and each of them can be modeled using Fig. 3.3 (b). Fig. 7.2 (a) shows an example for the output impedance model of two stages, and its equivalent circuit as shown in Fig. 7.2 (b) can be achieved after some manipulations and simplifications. It can be seen that the overall native conversion ratio is $N = N_1 \cdot N_2$ and the output impedance can be derived as

$$R_{out} = R_{out2} + \frac{R_{out1}}{N_2^2}, \tag{7.1}$$



(a) Ouput impedance of a two-stage circuit (b) Equivalent single-stage circuit

Figure 7.2: Output impedance model of a two-stage power converter.

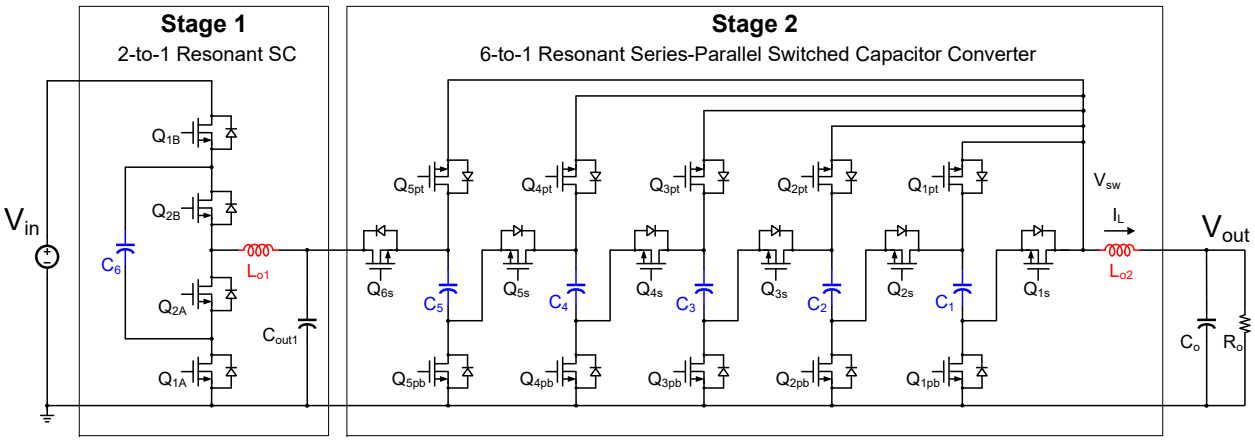
where N_1 and R_{out1} are the native conversion ratio and the output impedance for stage 1, respectively; while N_2 and R_{out2} are for stage 2. According to (7.1), there are combinations in selecting topologies as well as conversion ratios for each stage in order to achieve minimum R_{out}. By collecting more data on available devices and substituting it into the optimal layout templates like Fig. 4.14, it is potential to show a Pareto front with output conductance density versus output voltage, providing a holistic view in optimally allocating the resources for each stage. Given that R_{out1} is usually larger with the use of high-voltage switches, one of the combinations can be lowering R_{out2} as well as increasing N_2 so that the effect of R_{out1} can be reduced and low R_{out} can be achieved. The comparison result in Chapter 4 serves as a design guideline for each stage, through the switch and passive utilizations for different topologies, ranging from low to high voltage domains. In particular, it is found that the series-parallel topology serves as an suitable candidate for the second stage at low-voltage domain, with its excellent switch utilization and the best passive utilization.

7.2 Two-Stage Resonant SC Converter

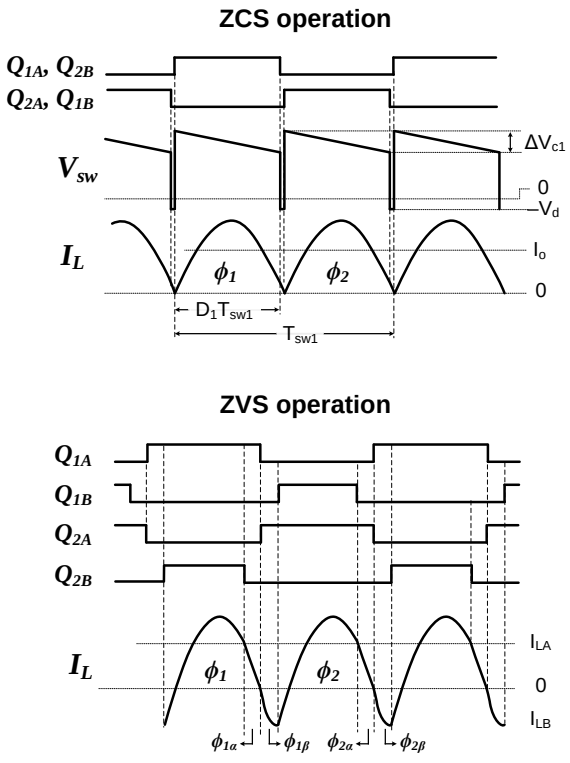
In this work, a two-stage ReSC converter, cascading a 2-to-1 ReSC converter and a 6-to-1 series-parallel ReSC converter, is proposed as shown in Fig. 7.3 (a). As suggested by (7.1), a 6-to-1 series-parallel ReSC converter provides not only low R_{out2} but also high enough N_2. Thanks to $N_2 = 6$, the effect of R_{out1} onto R_{out} is reduced by 36 times. Meanwhile, small form factor is presented by both selected topologies together with the two-stage structure, which is advantageous in achieving high ρ_{gout} for high conversion ratio. The fundamental operating principle for each stage is illustrated as follows.

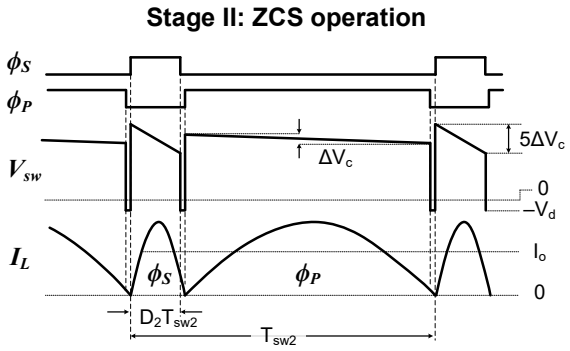
Stage I: 2-to-1 ReSC Converter

The four switches, Q_{1A}, Q_{1B}, Q_{2A}, Q_{2B}, can be controlled by two signal pairs, with Q_{1A} complementary with Q_{1B}, and Q_{2A} complementary with Q_{2B}. Both signal pairs are 180^o out of phase with each other, e.g. Q_{1A} and Q_{2A}, Q_{1B} and Q_{2B}. All control signals are operated

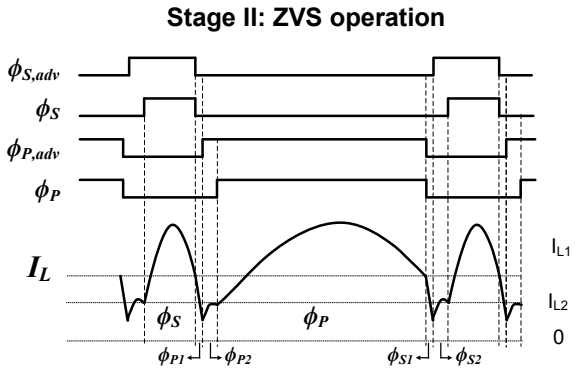


(a)





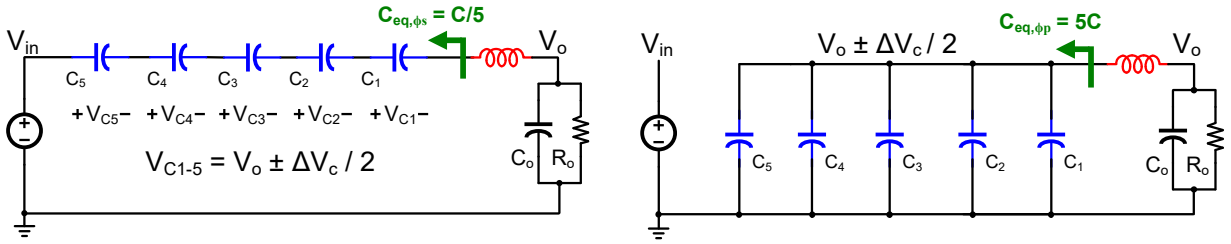
(b) Stage I: 2-to1 ReSC



(c) Stage II: 6-to1 Series-Parallel ReSC

Figure 7.3: Circuit schematic and control signals for the two-stage ReSC converter.

with a fixed duty ratio of $D_1 = 50\%$. As shown in Fig. 7.3 (b), the converter can either be operated with ZCS when $f_{sw1} = f_{crit1}$ or with ZVS when $f_{sw1} > f_{crit1}$, where f_{sw1} and f_{crit1} are the switching frequency and resonant frequency for the first stage, respectively. The steps to achieve ZVS operation are: i) Q_{2B} (Q_{1B}) turns off when the inductor current is positive, i.e. $I_{LA} > 0$, ii) Q_{1A} and Q_{2A} are then toggled at the same time when the inductor



(a) ϕ_S = high (b) ϕ_P = high

Figure 7.4: Equivalent circuit of a 6-to-1 series-parallel ReSC when (i) ϕ_S = high and (ii) ϕ_P = high.

current is around 0, and finally iii) Q_{1B} (Q_{2B}) turns on when $I_{LB} < 0$. The ZVS switching scheme enables the inductor current to flow through the body diodes of the switches before turning them on, eliminating the switching loss and improving the light load efficiency. More details about the ZVS operation for a 2-to-1 ReSC converter can be referred to [27].

This stage only processes an average current of $\frac{I_o}{6}$ or a peak current of $\frac{I_o}{3\pi}$ for the worse case (operated at the resonant frequency, f_{crit1}), thanks to the high conversion ratio provided by the stage II. The low processing current decreases the voltage ripple, $\Delta V_{c6} = \frac{I_o}{12 f_{sw1} C_6}$, across the flying capacitor, C_6. With the nominal voltage rating for all switches and flying capacitor, C_6, being $\frac{V_{in}}{2}$ or 24 V for an intermediate 48-to-24 V voltage conversion, $\frac{\Delta V_{c6}}{V_{c6}}$ is maintained low, beneficial in leaving more voltage margin to the switches and capacitor. On top of that, the low output current for this stage allows the inductor, L_{o1}, to have higher inductance with lower saturation current rating, given the same inductor size. Higher L_{o1} brings down the resonant frequency of this stage,

$$f_{crit1} = \frac{1}{2\pi\sqrt{L_{o1} C_6}}. \tag{7.2}$$

Therefore, a lower switching frequency, f_{sw1}, can be adopted to simultaneously achieve low conduction and switching losses.

Stage II: 6-to-1 Series-Parallel ReSC converter

Similar to the first stage, this converter can either be operated with ZCS or with ZVS, in order to reduce the switching loss. For ZCS operation, the converter can be controlled by the two-phase complementary signals, ϕ_S and ϕ_P, while operating at resonant frequency, $f_{sw2} = f_{crit2}$. For ZVS operation, two additional control signals, $\phi_{S,adv}$ and $\phi_{P,adv}$, are proposed and introduced, which will be illustrated in details in the next section. The equivalent circuit for the two-phase operation is shown in Fig. 7.4 (a) and (b): during ϕ_S = high, six switches, Q_{1s-6s}, are turned on and all flying capacitors, C_{1-5}, are connected in series with the input voltage, V_{in}, and switching node voltage, V_{sw}; while during ϕ_p = high, another ten parallel

switches, $Q_{1pt-5pt}$ and $Q_{1pb-5pb}$, are conducting and C_{1-5} are in parallel with V_{sw}. As a result, the voltage ripple across V_{sw} is $5\Delta V_c$ and ΔV_c during ϕ_S and ϕ_P, respectively, where ΔV_{c2} can be estimated by $\Delta V_c = \frac{I_{L,pk}}{6 f_{sw2} C_{fly}}$, given that $C_1 = C_2 = \cdots = C_5 = C_{fly}$. Depending on the capacitor configurations, the equivalent capacitance seen by the output inductor, L_{o2}, is different: $\frac{C_{fly}}{5}$ for ϕ_S versus $5C_{fly}$ for ϕ_P. To keep charge balance in C_{1-5}, meaning the same voltage ripple, ΔV_c, for all flying capacitors for both phases, the duty ratio, D_2, for ϕ_S is set around $\frac{1}{6}$. The switching frequency required to achieve resonant operation can be derived as

$$f_{crit2} = \frac{2}{T_{S,crit} + T_{P,crit}} = \frac{1}{2\pi\sqrt{L_{o2} C_{fly}}} \cdot \frac{\sqrt{5}}{3}, \tag{7.3}$$

where $T_{S,crit}$ and $T_{P,crit}$ are the resonant periods during ϕ_S and ϕ_P, respectively. Note the equivalent capacitance is 1.8 times C_{fly}, allowing smaller capacitors or lower switching frequency.

In this converter, each switch sustains different blocking voltage, e.g. $5V_o$ for Q_{6s} as compared to V_o for Q_{1s}. Given the practical availability shown in Fig. 4.5, switches with uniform V_{rated} are applied throughout the converter for low-voltage domain. For a 6-to-1 series-parallel topology, the input voltage can go up to 30 V when employing 25 V switches. Contrarily, unlike the scaling disruption in discrete transistors, the capacitors closely follow CV^2 for wide operating range, including voltage domain below 25 V. As a result, it is valid that series-parallel topology having the least passive volume, when CV^2 is used as a capacitor volumetric parameter [14]. The low passive requirement is mainly because all flying capacitors sustain only V_o - the lowest voltage in the converter, as can be seen in Fig. 7.4 (a) and (b), enabling the use of capacitors with higher capacitance density. Together with the high equivalent capacitance seen by the output inductor, the series-parallel topology is advantageous in excellent passive utilization. Meanwhile, all flying capacitors are experiencing the same voltage derating factors, providing an easily predictable resonant frequency and ensuring low output impedance at low switching frequency.

7.3 Zero Voltage Switching (ZVS) Techniques

Large-swing inductor current while operating at resonant frequency gives a design freedom in achieving soft switching operation. While the ZCS turn-on mechanism developed in the previous section reduces the VI overlap loss during switching transitions, there is a strong need to implement ZVS turn-on techniques for further improvement in light-load efficiency. The ZVS operation [94] is able to eliminate not only the VI overlap loss but also the switching loss, $P_{oss} = C_{oss} V_{block}^2 f_{sw}$, correlated with the transistor output referred capacitance, C_{oss}. The origin of P_{oss} can be twofold: i) hard charging C_{oss} with charge sharing loss, and ii) resistively discharging C_{oss} through the transistor on-resistance. To eliminate the switching losses, the ZVS operation charges and discharges C_{oss} through an inductive current, by an output inductor in this work. Through the inductor current, the energy stored in C_{oss} of

turning on switches can be brought down to zero (practically, a body diode voltage drop, V_d) before the turn-on event, and the blocking voltage required by turning off switches C_{oss} can be built up before their neighboring switches are about to turn on, eliminating the voltage difference between capacitors and so the switching losses. These two conditions coexist, serving as important indicators of the ZVS completeness, e.g. a complete ZVS operation has all correct blocking voltage ready before the turn-on event.

To analyze the ZVS operations of the series-parallel topology shown in Fig. 7.3 (a), the switches are divided into four sections: upper series switches (Q_{6s}), lower series switches (Q_{5s-1s}), upper parallel switches ($Q_{5pt-1pt}$) and lower parallel switches ($Q_{5pb-1pb}$); with their body diodes represented by D_x, parasitic capacitance by C_x and blocking voltage by V_x, e.g. C_{6s}, D_{6s} and V_{6s} for the switch Q_{6s}. Aligning the inductor current with body diodes helps creating low voltage across C_{oss} before turning on the corresponding switches. Depending on the conducting directions of body diodes and the inductor current, I_L, all switches can be divided into two groups: i) upper series and upper parallel switches (D_{6s} and $D_{1pt-5pt}$) for negative I_L, ii) lower series and lower parallel switches (D_{1s-5s} and $D_{1pb-5pb}$) for positive I_L. There are trade-offs in the selections of I_L polarity in terms of switch ratings and power loss reduction. For example, a negative I_L during deadtime is potential in achieving complete ZVS operation, but it also leads to a higher voltage at V_{sw}, i.e. $V_{in}+2V_d$ or $5V_o+2V_d$, raising the blocking voltage of all lower parallel switches to be $5V_o + V_d$ as compared to $\{5V_o, 4V_o \cdots V_o\}$ in the case of positive I_L.

The proposed switching scheme to achieve ZVS operation is shown in Fig. 7.3 (c). Four more auxiliary phases are added on top of the original series and parallel phases, which are ϕ_{S1}, ϕ_{S2}, ϕ_{P1} and ϕ_{P2}. The control for the switch Q_{6s} is now replaced by $\phi_{S,adv}$, and the switches $Q_{1pt-5pt}$ by $\phi_{P,adv}$; and the control for other switches remains the same. Both $\phi_{P,adv}$ and $\phi_{S,adv}$ are the time-advanced versions of ϕ_P and ϕ_S, respectively; they will be turned on depending on the polarity of the inductor current. To fully remove the charge on parasitic capacitance, the stored inductor energy should satisfy

$$\frac{1}{2}L_o I_L^2 > \frac{1}{2}\sum C_{oss}V_{ds}^2, \tag{7.4}$$

implying that a complete ZVS operation requires either larger inductance or inductor current. However, I_L is usually maintained low to avoid too much conduction loss; meanwhile, a lower inductance is required for smaller size and higher saturation current. As a result, a negative inductor current during deadtime is suggested when higher inductance available since it is capable of achieving full ZVS operation and the inductor current does not need to go very negative to fulfill (7.4); otherwise, a positive inductor current is better to balance the conduction and switching loss with incomplete ZVS operation. As compared to the ZVS operations in the first stage, the 6-to-1 series-parallel topology has much more complicated parasitic capacitor network. Therefore, all auxiliary phases with equivalent circuit and operational waveform will be illustrated in details.

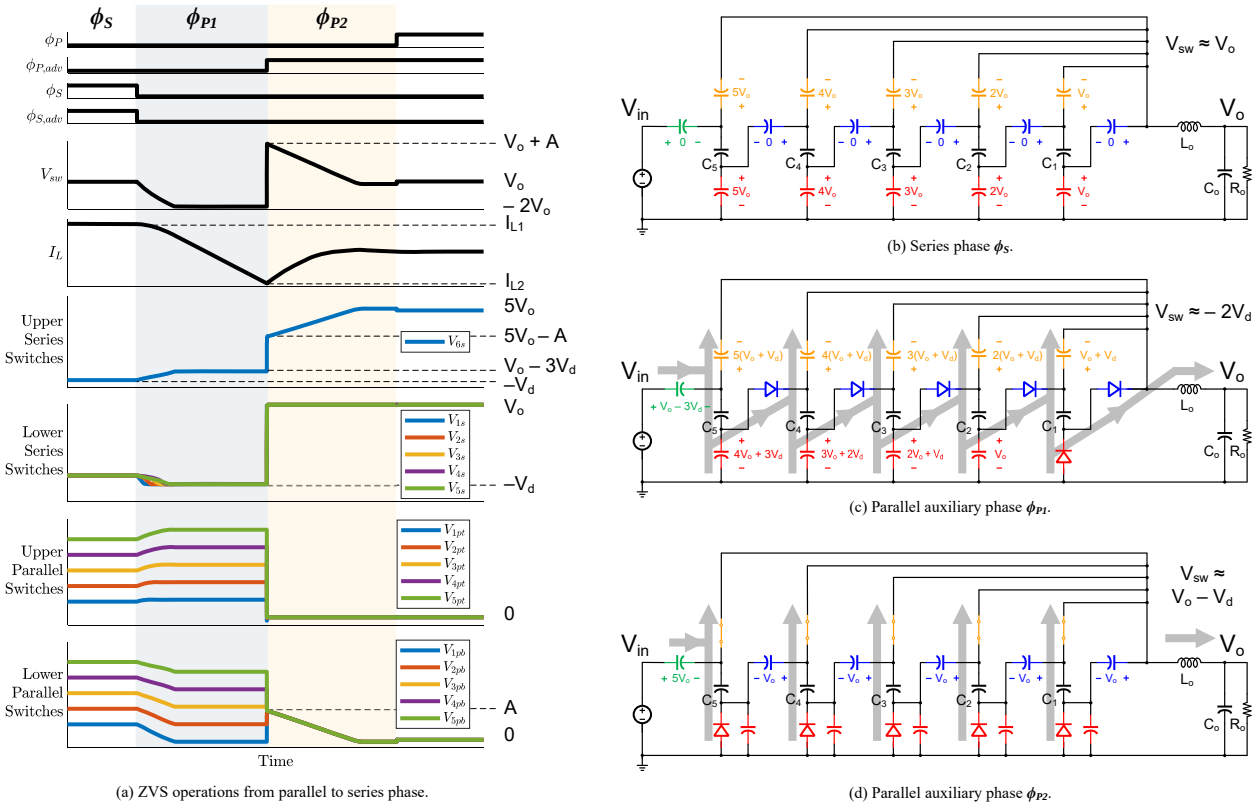
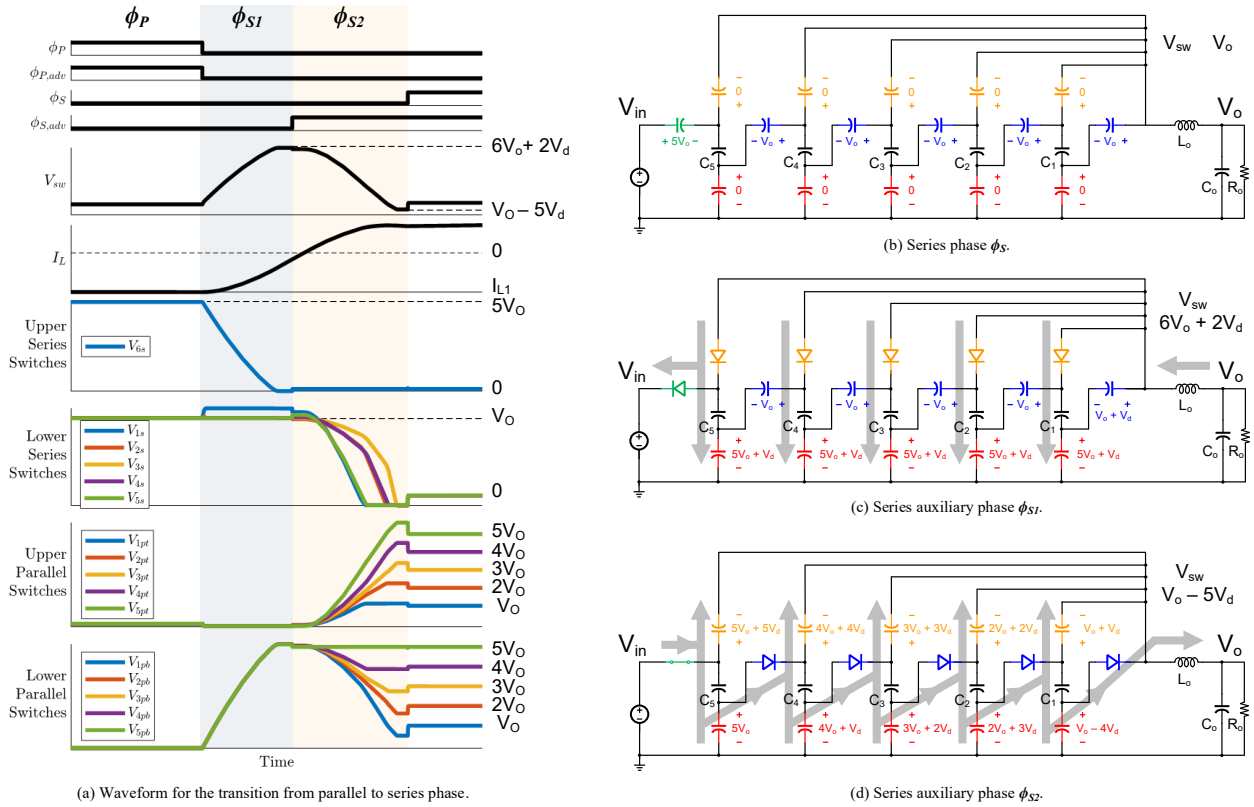


Figure 7.5: Zero voltage switching (ZVS) operations from series to parallel phase in a 6-to-1 series-parallel ReSC converter, when inductor current is positive during deadtime.

Positive Inductor Current during Deadtime

The ZVS operations for the transition from series to parallel phase is shown in Fig. 7.5. The goal is to remove the capacitive energy stored at all parallel switches, and to get the series switches prepared and charged to their blocking voltage. First, the series-parallel converter enters deadtime, i.e. phase ϕ_{P1}, when $I_L > 0$. The positive inductor current quickly turns on the body diodes of lower series switches, since all series switches were with zero energy across their parasitic capacitance during series phase. Note that D_{1pb} is also turned on for the continuous flow of I_L, lowering V_{sw} to $-2V_d$ at the end of ϕ_{P1} and further changing the blocking voltage across all C_{oss} except lower series switches. The converter then enters ϕ_{P2} once $\phi_{P,adv}$ turns the upper parallel switches on, when I_L is still positive. Once ϕ_{P2} goes high, the different blocking voltage across lower parallel switches raises V_{sw} to $V_o + A$, where A is the charge sharing result between $C_{1pb-5pb}$. The positive inductor current the soft discharges $C_{1pb-5pb}$ from A to $-V_d$, until their body diodes conduct; meanwhile, Q_{6s} is being soft charged to around $5V_o$. As compared to ZCS, the converter with the proposed ZVS transitions from parallel to series phase, with less switching loss on C_{6s} and $C_{1pb-5pb}$.



(a) Waveform for the transition from parallel to series phase.

(b) Series phase ϕ_S.

(c) Series auxiliary phase ϕ_{S1}.

(d) Series auxiliary phase ϕ_{S2}.

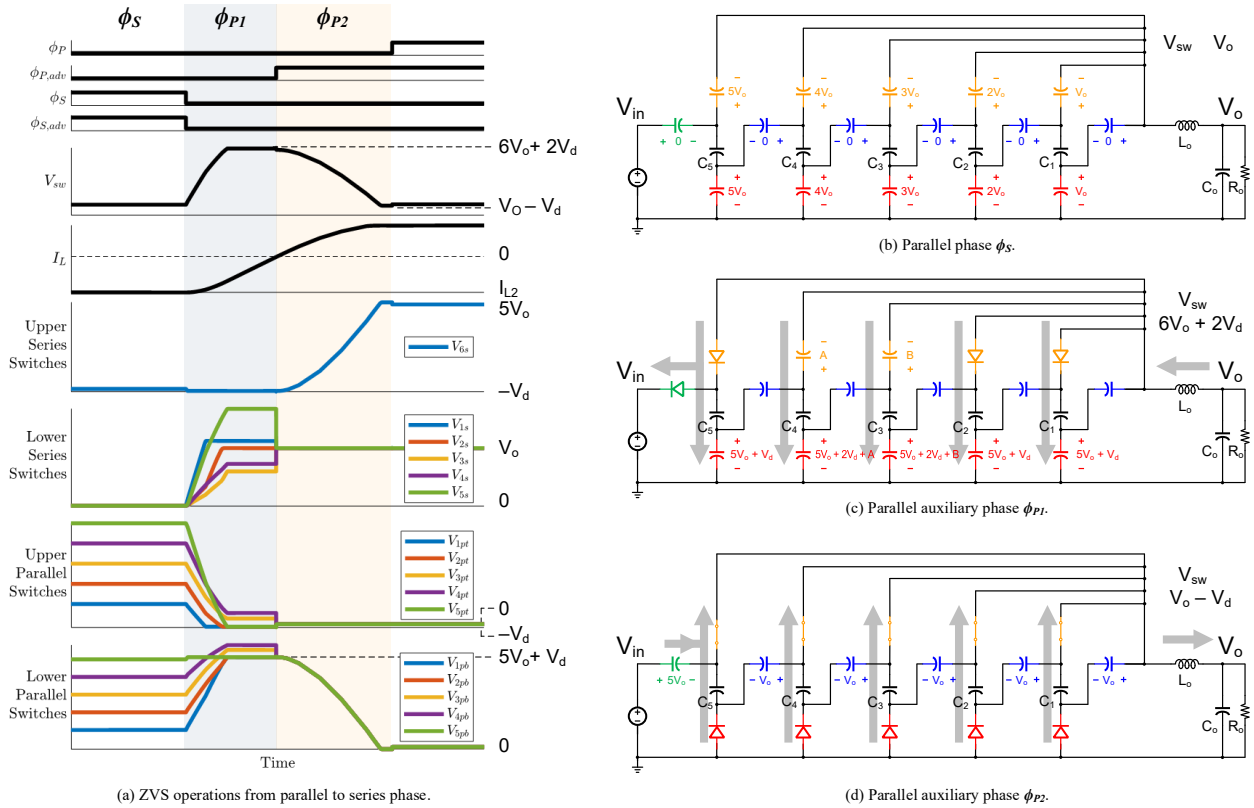
Figure 7.6: Zero voltage switching (ZVS) operations from parallel to series phase in a 6-to-1 series-parallel ReSC converter, when inductor current is negative during deadtime.

Similarly, the analysis for the transition from series to parallel phase can be done.

Negative Inductor Current during Deadtime

Fig. 7.6 shows the transition from parallel to series phase when $I_L < 0$. When entering ϕ_{S1}, the negative inductor current turns on D_{6s} and $D_{1pt-5pt}$, raising V_{sw} to $6V_o + 2V_d$ at the end of ϕ_{S1} and charging $C_{1pb-5pb}$ to $5V_o + V_d$. Meanwhile, I_L increases so that it is ready to bring the energy away from $C_{1pb-5pb}$ in the upcoming phase. To prevent the positive I_L from undermining the soft switching operation done during ϕ_{S1}, the best time to turn on Q_{6s} is when I_{L2} is around and below 0. Once Q_{6s} is turned on, the converter then enters ϕ_{S2} with $C_{1pb-5pb}$ being discharged from V_o to $-V_d$ until $D_{1pb-5pb}$ conduct. At the end of ϕ_{S2}, both $C_{1pt-5pt}$ and $C_{1pb-5pb}$ are charged to their blocking voltage, i.e. $\{5V_o, 4V_o \cdots, V_o\}$. Both conditions, including (i). D_{1s-5s} turned on with low voltage drops and (ii). $C_{1pb-5pb}$ and $C_{1pt-5pt}$ charged to their blocking voltage, are arrived. This suggests that Q_{1s-5s} are ready for ZVS turn on; therefore, the converter smoothly transitions from parallel to series phase.

The circuit operations for the transition from series to parallel phase is shown in Fig. 7.7.



(a) ZVS operations from parallel to series phase.

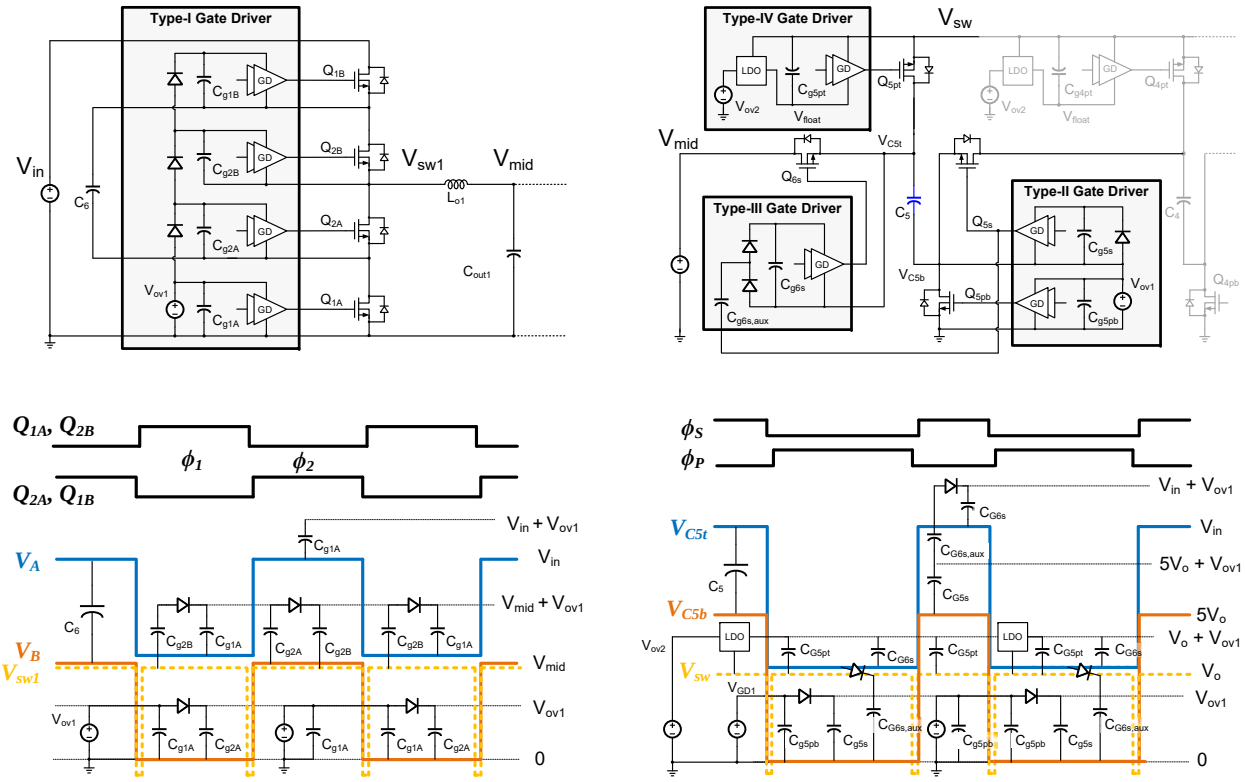
(b) Parallel phase ϕ_S.

(c) Parallel auxiliary phase ϕ_{P1}.

(d) Parallel auxiliary phase ϕ_{P2}.

Figure 7.7: Zero voltage switching (ZVS) operations from series to parallel phase in a 6-to-1 series-parallel ReSC converter, when inductor current is negative during deadtime.

Similar to $\phi_S \rightarrow \phi_{P1}$, the converter enters ϕ_{P1} when $I_{L2} < 0$. Still, the negative inductor current will eventually go through D_{6s} and D_{5pt}. However, the blocking voltages between $C_{1pb-5pb}$ or $C_{1pt-5pt}$ are clamped to different values. For instance, C_{4pb} and C_{3pb} are clamped at a voltage higher than $5V_o + V_d$, and the charge transfer halts as V_{sw} hits $6V_o + 2V_d$. On the other hand, V_{2pt} and V_{1pt} during the previous phase ϕ_{P1} are closer to $-V_d$, quickly clamped by their body diodes as well as ensured V_{2pb} and V_{1pb} being charged to $5V_o + V_d$. The discrepancy between $V_{1pb-5pb}$ or $V_{1pt-5pt}$ happens in the middle branches due to their complicated neighboring capacitive netrwork, leading to some charge sharing loss when the converter goes to ϕ_{P2}. Fortunately, the voltage discrepancy is small enough that ZVS benefits are largely maintained. When the inductor current goes up to around 0, $Q_{1pt-5pt}$ are turned on. At the end of ϕ_{P2}, $C_{1pb-5pb}$ are discharged to $-V_d$ and $D_{1pb-5pb}$ are turned on by the positive inductor current; meanwhile, V_{1s-5s} are maintained at V_o and V_{6s} is brought up to $-V_d$. The conditions, including turned-on body diodes and charged blocking voltage, are met, and $Q_{1pb-5pb}$ are ready to turn on. Going through the auxiliary ϕ_{P1} and ϕ_{P2}, the series-parallel topology achieves ZVS operations from series to parallel phase.



(a) Stage I– 2-to-1 ReSC converter

(b) Stage II– 6-to-1 series-parallel ReSC converter

Figure 7.8: Floating gate driver designs and driving waveforms for (a) stage I – 2-to-1 ReSC and (b) stage II – 6-to-1 series-parallel ReSC, with all diodes assumed ideal without voltage drops.

7.4 Floating Gate Driver Techniques

N-type transistors are preferred for their better $R_{on} \cdot C_{ds}$ performance than p-type transistors, when designing the power MOSFETs in discrete implementations (as covered in Chapter 5, the MLCC bootstrap capacitor has high capacitance density). However, turning on high-side n-type transistors requires floating supplies with higher voltage generated. For instance, $V_{in}+V_{ov}$ is required to drive the high-side NMOS of a buck converter, where V_{in} is the highest available voltage within the converter and V_{ov} is an overdrive voltage for the gate-to-source voltage, V_{gs}. The overdrive voltage is chosen as high as possible to obtain low on-resistance; meanwhile, it should be low enough to keep gate driver loss down and stay within the safety operating region. To make sure the overdrive voltage is steadily provided on top of varying source voltage of high-side switches, several techniques are developed to generate stable and safe floating supplies for V_{gs} [77]. In this work, four types of gate driving techniques are employed, which are basically derived from the conventional bootstrap circuit as shown in Fig. 5.7.

Fig. 7.8 (a) shows the cascaded bootsrapped technique for stage I, where the floating supplies are successively generated from low to high sides. The lowest gate diver as well as its bypass capacitance, C_{g1A}, is always charged to the supply voltage, V_{ov1}. As Q_{1A} is turned on during phase 1, the source voltage of Q_{2A}, V_B, is tied to ground, giving C_{g2A} a chance to be charged to V_{ov1}. In the next phase or phase 2, Q_{2A} can be turned on with enough supply voltage across C_{g2A}; meanwhile, C_{g2A} and C_{g2B} are able to be connected since their bottom plates share the same voltage level, V_{mid}. When the converter operation is again back to phase 1, C_{g1B} at the top can be charged by C_{g2B}. Eventually, all bootstrap capacitors are replenished to around V_{ov1} every switching cycle, providing sufficient charge reservoir for stable floating supplies. Note the diode voltage drop is not considered here, which slightly affects the driving capability for switches at higher levels.

Fig. 7.8 (b) shows three different gate driving techniques for stage II. Firstly, as shown by the type-II gate driver, adjacent lower series and parallel switches, $Q_{ns} - Q_{npb}$ $n \in [1, 5]$, can be driven in pair using half bridge gate drivers, just like the switches in regular buck converters. Secondly, the double charge pump technique represented by the type-III gate driver is used for driving Q_{6s}, which is capable of generating a floating voltage higher than V_{in}. In the type-III gate driver, $C_{g6s,aux}$ is first charged by the top plate of C_5, V_{C5t}, to V_o during ϕ_P, and C_{g6s} is then charged by the total voltage of $C_{g6s,aux}$ in series with C_{g5s} during ϕ_S. As can be seen in the driving waveforms of Fig. 7.8 (b), during ϕ_S, the top plate of C_{g5s} can be raised to $5V_o + V_{ov2}$ when Q_{5s} is turned on. With the assistance of V_o across $C_{g6s,aux}$, the top plate of C_{g6s} is increased to $V_{in} + V_{ov2}$, which is high enough to turn on Q_{6s} during ϕ_S. Finally, the type-IV gate driver is used for $Q_{1pt-5pt}$, where an LDO is employed to stabilize the floating supply referenced to V_{sw}. The LDO requires an input voltage of at least $V_o + V_{ov2} + V_{dropout}$, and its output is clamped to V_{ov1} with its reference voltage, V_{sw}, swinging between $-V_d$ and V_o.

7.5 Measurement Results

A quality PCB layout has short interconnection, strong signal integrity and evenly distributed heat generation, which often links to the converter performance in efficiency and power density. For example, a PCB with shorter interconnection, with reduced parasitic resistance and inductance, has higher efficiency and power density due to lower conduction loss and less ringing issue. While there are many components to consider when designing the layout for a power converter, the first priority is looking into the high-current paths for switches and the high-dv/dt paths for gate drivers. First of all, a direct path on the same copper layer is preferred for high-current paths since it gives the shortest possible connection. In other words, changing layers through vias should be reduced to the minimum to ensure more direct paths and avoid additional resistance. For the vias, note that there is a tradeoff in its sizing and converter performance: a larger hole with less resistance has larger spacing required; whereas multiple tiny holes given tight area constraint significantly increase the cost. When routing the connections between components, there is a tradeoff between wider

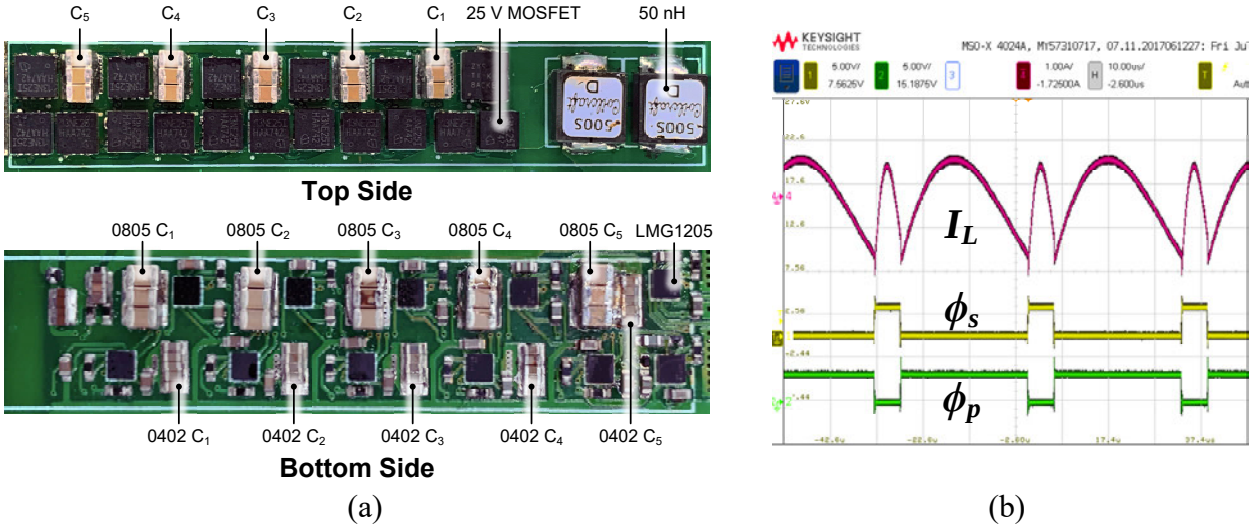
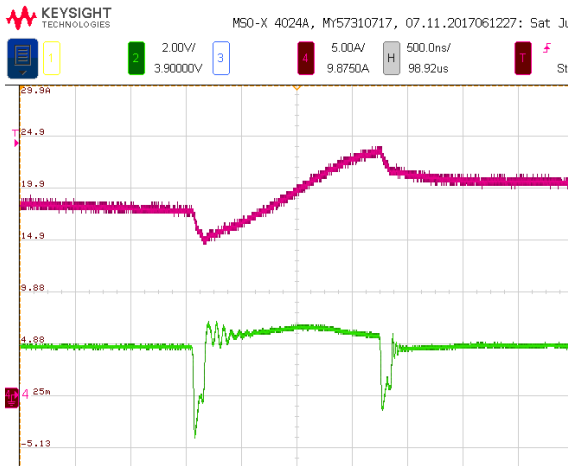


Figure 7.9: (a) Photograph with a box dimension of 0.39 in x 2.36 in x 0.23 in (or 1 cm x 6 cm x 0.585 cm) and (b) key steady state waveforms of the prototype 6-to-1 series-parallel ReSC.

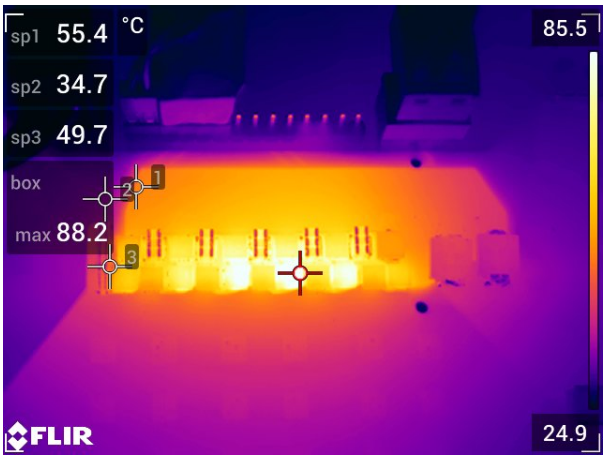
traces and smaller power converter, and there is some effort to find a balance considering both sizing and heat generation. Other than the short interconnection, thicker copper is another option in reducing the parasitics. However, more concerns in layout constraints should be taken into account, e.g. the trace width / spacing increases from 6 mil using 1-oz copper to 12 mil using 4-oz copper. Therefore, to implement a 4-oz copper PCB, the floorplan with relaxed layout constraints should be done in a very early stage.

A strong gate driver reduces the switching transition time, and so the switching loss. However, it also raises a serious concern in signal integrity as it induces higher dv/dt in the circuit. In particular, the high impedance input of the gate driver is susceptible to the interference, leading the gate driver to falsely turn on the switch as well as shoot-through issues. To address that, the first step is to shorten the gate driving paths in order to reduce the loop parasitic inductance and the opportunity to couple with other circuits. In addition to that, simple *RC* filters right in front of the gate driver can be very useful in reducing the high frequency noise going into the gate driver. Furthermore, an optimal solution is to combine the *RC* filters with a careful signal routing by avoiding direct overlap between vulnerable control signals and strong power switching planes. For example, a ground plane serves as a nice shielding layer that can be inserted between control signal and power switching layers to prevent the control signals from getting interfered by the high-current and noisy paths. The ground or supply planes can also serve as an integrated heat sink to spread the heat out, which is especially needed in thermal spots – the bottleneck that prevents the board from pushing to higher power. Usually, the thermal spot can be a good starting point for debugging, as that may indicate loose interconnection and/or inferior signal integrity.

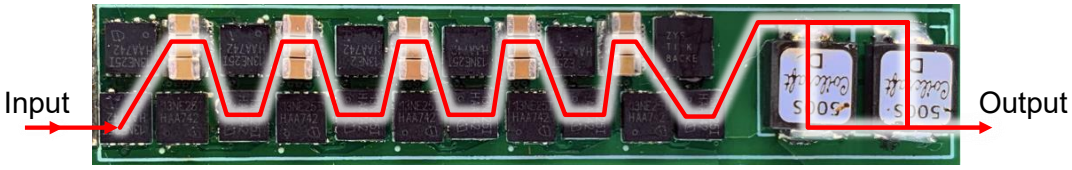
In this section, the layout of the second stage – a 6-to-1 series-parallel ReSC is primarily



(a) Top (red): I_L, bottom (green): V_{sw}



(b) Fan cooling only @ 50 A output current



(c) Long current path during series phase

Figure 7.10: Measurement results of the first prototype 6-to-1 series-parallel ReSC converter.

focused, which was fabricated and measured several times before arriving at its optimal design. The very first and last prototype board are shown in this section to demonstrate the PCB design consideration in detail.

First PCB Prototype

The annotated photograph of the first prototype is shown in Fig. 7.9 (a), which was successful in laying out all the high-power switches and passives on the top layer by following the component arrangement shown in the schematic of Fig. 7.3 (a). This PCB prototype has a compact layout with direct current path from input to output. All gate drivers and auxiliary floating supply circuits, except added LDO, are laid out on the bottom layer. Due to the use of gate drivers with very small BGA package (TI LMG 1205), the space left on the bottom layer are filled up with more parallel flying capacitors. This prototype worked nicely as shown in Fig. 7.9 (b), where the converter is operated at its resonant frequency. However, a further measurement result shows that the measured converter output impedance (5.8 mΩ) is twice the theoretical analysis, excluding the gate driver loss. Also, the temperature of the board rises to more than 88°C at 50 A output current, preventing the power converter from getting higher power density even though the current rating of the whole power converter

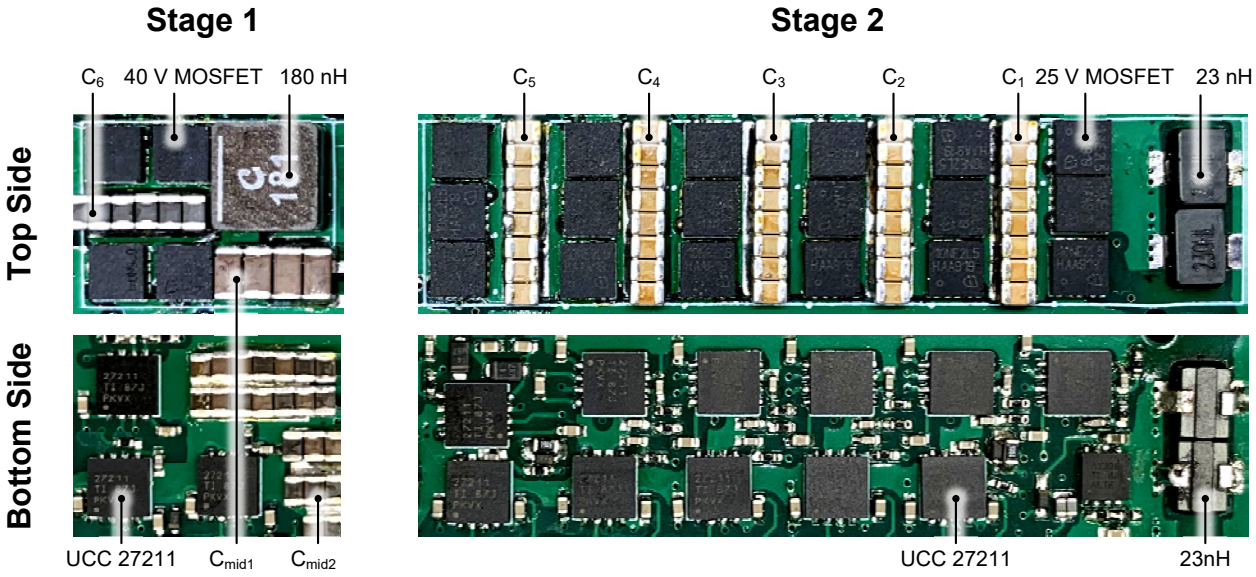


Figure 7.11: Photograph with box dimensions of the two-stage ReSC converter – stage I: 0.44 in x 0.6 in x 0.22 in (or 1.12 cm x 1.52 cm x 0.56 cm); and stage II: 0.44 in x 1.96 in x 0.16 in (or 1.12 cm x 4.99 cm x 0.4 cm).

should be more than 80 A (limited by saturation current).

Fig. 7.10 shows the inductor current and switching node voltage when the converter has the phase transitions of parallel-series-parallel. The switching node voltage, V_{sw}, contains the most information of the power converter, showing that there is more ringing voltage at the beginning of the series phase than that of the parallel phase. In addition to the ringing amplitude, it can be seen that the ringing frequency is much smaller in the series phase, implying that the series-connected flying capacitors see different amount of inductance. To analyze the ringing at V_{sw}, the current path during series phase shown in Fig. 7.10 (c) can be handy, which was found that the long current path leads to high parasitic inductance and resistance. Even worse, as analyzed in chapter 4, the series switches sustain higher RMS current than the parallel switches, which can also be observed by the hot spots in Fig. 7.10 (b). To reduce the ringing issue and balance the heat generation, an updated PCB layout should first consider having the shortest path and more ground plane for switches involved in the series phase.

Final PCB Prototype

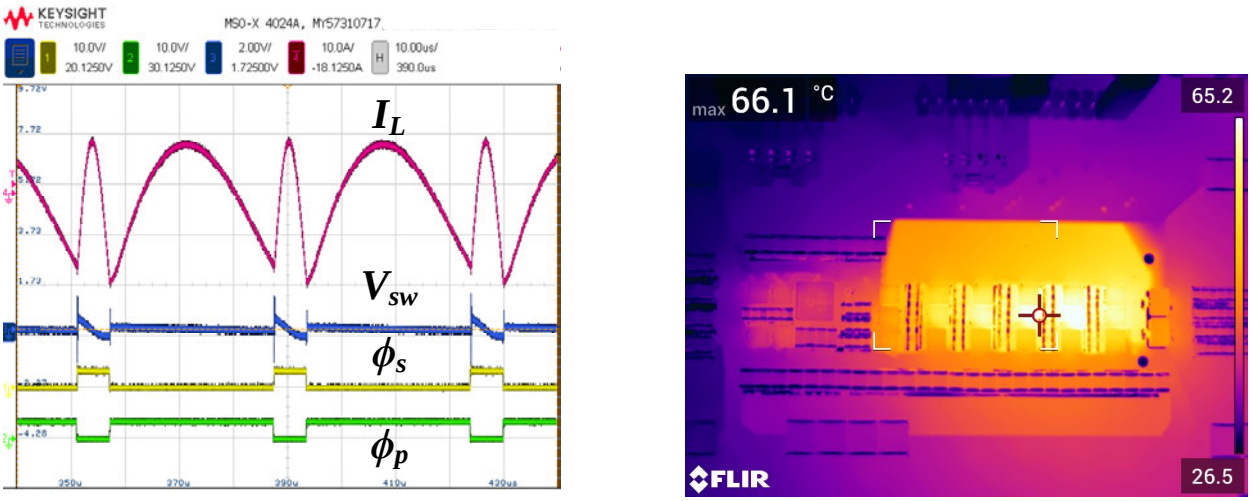
The photograph of the final hardware prototype is shown in Fig. 7.11, with main components highlighted and detailed in Table 7.1. The fabricated PCB has four layers, with 4-oz copper for the outer layers and 3-oz copper for the inner layers. The thick copper layers significantly reduces the trace resistance and serves as an effective heat sink. High-current components

Table 7.1: Main components for the PCB and their specifications.

Component	Part Number	Specification
Stage-1 MOSFET Switch	Infineon BSZ025N04LS	40 V, 40 A, 2.5 $m\Omega_{max}$ @ 10 V_{GS}
Stage-1 Gate Driver	Texas Instruments UCC 27211	Half bridge, 3.7 A_{sink}, 4.5 A_{source}
Stage-1 Flying Capacitor, C_6	C2012X5R1V226M125AC	Rated 35 V, 22 μF x 12
Stage-1 Output Capacitor, C_{mid1}	C3216X5R1V226M160AC	Rated 35 V, 22 μF x 4
Stage-1 Output Capacitor, C_{mid2}	C2012X5R1V226M125AC	Rated 35 V, 22 μF x 22
Stage-1 Inductor, L_{o1}	XAL6030-181MEL	180 nH, 39A_{sat}, 1.59 $m\Omega_{nom}$
Stage-2 MOSFET Switch	Infineon BSZ010NE2LS5	25 V, 40 A, 1 $m\Omega_{max}$ @ 10 V_{GS}
Stage-2 Gate Driver	Texas Instruments UCC 27211	Half bridge, 3.7 A_{sink}, 4.5 A_{source}
Stage-2 Flying Capacitor, C_{1-5}	GRM21BR60J107ME15L	Rated 6.3 V, 100 μF x 8 for each
Stage-2 Inductor, L_{o2}	Pulse PA2983.230HL	23 nH, 75A_{sat}, 0.33 $m\Omega_{nom}$ x 2

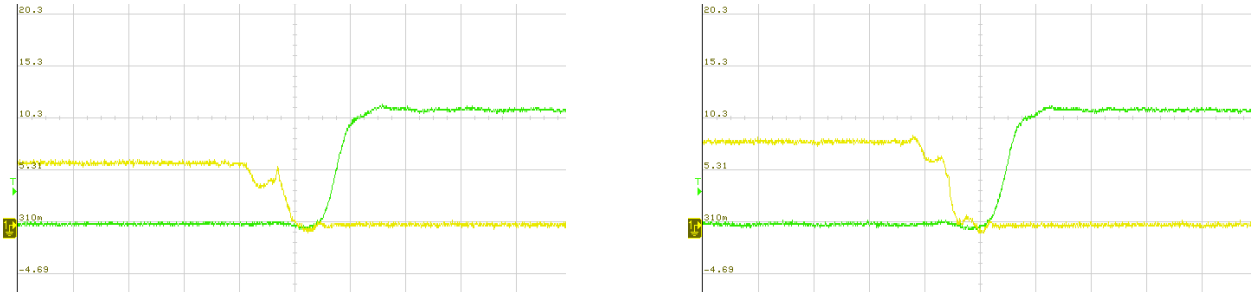
and paths are all laid out on the top layer of the PCB in order to avoid any high-resistance vias and reduce conduction loss. Both active and passive components are arranged in the most symmetric and compact way, thanks to the identical footprint for all flying capacitors. The output inductor of the second stage is embedded in a dedicated slot, greatly reducing the profile of the converter. Each stage utilizes uniform power MOSFETs, which are 40 V for the first stage and 25 V for the second stage. All switches are driven by high-voltage and high-driving-current gate drivers (i.e. TI UCC 27211), in order to reduce the switching VI overlap loss. Together with compact and efficient bootstrap techniques using auxiliary capacitors and diodes, all gate drivers as illustrated in section 7.4 are placed on the bottom layer. Note that there are two additional switches in stage II, each in parallel with the top and bottom series switches (Q_{6s} and Q_{1s}), reducing the switch RMS current during series phase and filling up the spaces left after the essential 16 switches are placed. Several careful routings, including ground shielding plane through the inner layers, are done to avoid interference on high-impedance node.

The key operating waveforms of the 6-to-1 series-parallel ReSC converter are shown in Fig. 7.12 (a). The highest output current tested is 60 A with the overall system temperature monitored as shown in Fig. 7.12 (b), where the peak temperature is 66.1°C with fan cooling only, thanks to the low output impedance (3.83 mΩ in total) in the series-parallel topology. This output impedance is composed of topology-dependent switch utilization ($\approx$1.5 mΩ), PCB trace ($\approx$2 mΩ), the rest of it are gate driver loss and switching losses. After adding a 2-to-1 ReSC converter as the first stage, the total equivalent output impedance of the two-stage ReSC converter is 4.28 mΩ, which has only an 11% increase thanks to the conversion ratio of 6 at the second stage. Also, due to the low processing current in the first stage, it can be seen operating with cooler temperature as shown in Fig. 7.12 (b). The ZVS operation of the second stage is validated through Fig. 7.13, which shows the transition from series to parallel phase. It can be observed that V_{ds} goes to zero before V_{gs} turns on, reducing the



(a) (b)

Figure 7.12: (a) Key waveforms of the 6-to-1 series-parallel ReSC converter and (b) thermal monitor at 60 A output current with fan cooling only.

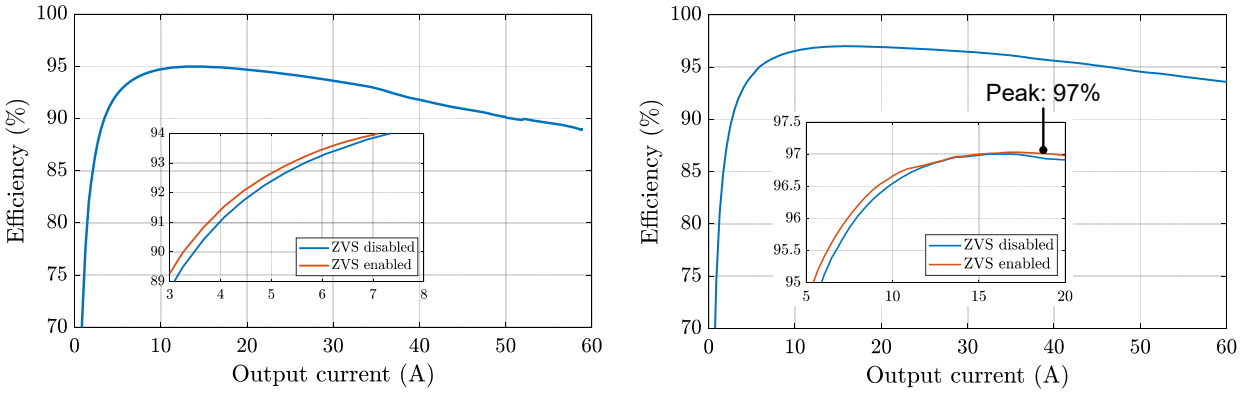


(a) Q_{3pb} (b) Q_{4pb}

Figure 7.13: Drain-to-source (yellow) and gate-source voltage (green) of (a) Q_{3pb} and (b) Q_{4pb} when the 6-to-1 series-parallel ReSC converter transitions from parallel to series phase. Scale: vertical 5 V/div and horizontal 50 ns/div.

switching loss.

The efficiency plots for various input voltage are shown in Fig. 7.14 (a) and (b), where the efficiency peaks at 97% for 48-to-4V power conversion with ZVS technique enabled. The efficiency was measured with a Yokogawa WT3000 precision power analyzer, and includes all gate driving losses. In addition, the capacitor voltage of the second stage is balanced with only ±2.5 mV deviations. As summarized in Table 7.2, both stage I and stage II are implemented in a very small total box volume of 0.195 in^3, hence achieving a peak current density of 308 A/in^3 or a peak power density of 1154 W/in^3 for 48 V input voltage. The comparison with the state-of-the-art designs is shown in Fig. 7.15 using the FoM



(a) V_{in} = 24 V, V_o = 2 V, f_{sw} = 60 kHz (b) V_{in} = 48 V, V_o = 4 V, f_{sw} = 72 kHz

Figure 7.14: Measured efficiency over input voltages of (a) 24 V and (b) 48 V for the two-stage ReSC converter, with the insets showing the improved efficiency by ZVS operations. Note that all gate drivers are included for efficiency calculation.

Table 7.2: Performance summary of the two-stage ReSC converter.

Stage	Input	Output	Peak Efficiency	Full-load Efficiency	Volume
Stage 1: 2-to-1 ReSC	48 V	24 V	99.30% @ I_{o1} = 3 A	99% @ I_{o1} = 10 A	0.058 in^3
Stage 2: 6-to-1 SP-ReSC	24 V	4 V	97.49% @ I_{o2} = 16 A	94.24% @ I_{o2} = 60 A	0.137 in^3
Two-Stage ReSC	48 V	4 V	97.04% @ I_{o2} = 16.8 A	93.57% @ I_{o2} = 60 A	0.195 in^3

"G_{out}/Volume" over different conversion ratios, and this work shows promising performance pushing towards higher current density and higher efficiency for high conversion ratios.

7.6 Chapter Summary

This chapter validates that the multi-stage approach is feasible in achieving high output conductance density for high conversion ratios, by optimally designing each stage based on their voltage domains and available devices. An example of a two-stage ReSC converter, optimally cascading a 2-to-1 ReSC converter for high-voltage domain and a 6-to-1 series-parallel ReSC converter for low-voltage domain, successfully showcases an efficient 48-to-4 V power conversion in a very small box volume of 0.195 in^3, thanks to the symmetric power switch layout and th area-efficient floating gate driving techniques. The whole converter is tested up to 60 A and the full-load efficiency is maintained 93.6%, thanks to the efficient

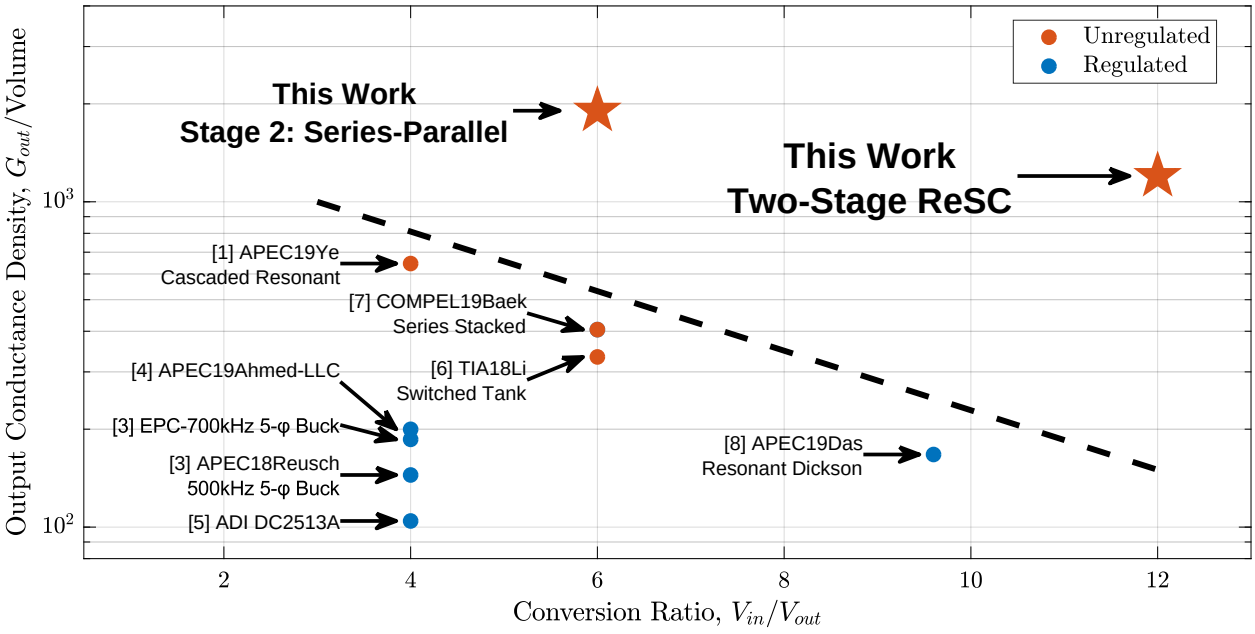


Figure 7.15: Performance comparison with the state-of-the-art designs. The metric of G_{out}/Volume is used to capture both the current density and efficiency at heavy load condition, where the efficiency is mainly dominated by the converter output impedance or the reciprocal of the output conductance, G_{out}. Higher G_{out}/Volume represents higher current density and higher efficiency are simultaneously achieved.

switch utilization of both stages. The two-stage ReSC converter achieves a very high current density of 308 A/in^3 or a power density more than 1000 W/in^3. Meanwhile, the peak efficiency is 97% (considering the gate driver losses) with the proposed ZVS techniques enabled. The experimental results demonstrate the great potential of the multi-stage approach in interfacing both high input voltage and high output current for PoL applications, particular in high-speed computing industries and data centers.

Chapter 8

Passives Reduction Techniques

Hybrid or resonant switched capacitor converters (ReSC) have shown superior efficiency and power density in fixed- and high-conversion-ratio applications, due to their efficient utilization on active and passive components. Other than the power converter itself, the input and output capacitor filters are also essential elements, which, however, are usually assumed fairly large and not included in the ReSC design. Even worse, when operating around resonant frequency, the inductor current has a larger swing that leads to more current going to the filter capacitor, and larger voltage ripple is expected as compared to higher-frequency operations. Also, the ReSC performance is highly associated with the stability of the input and output voltage, and high performance requires predictable resonant operation without the involvement of filter capacitors. As a result, the filter capacitors have to be large enough, e.g. $C_{filter} \gg C_{eq}$ for a single-phase ReSC, which compromises the power density. To reduce the filter capacitor size, multiphase interleaving technique that is broadly used in conventional power converters can be applied to ReSC, since it reduces the current flowing to the capacitor and increasing the equivalent filter capacitance. However, the analysis and implementation for multi-phase ReSC were not fully discussed.

This chapter first analyzes the efficaciousness of multiphase interleaving technique when operating around resonant frequency. It is found that the multi-phase ReSC shows promising results in reducing the filter capacitance requirement, though different behaviors are also found as compared to high-frequency operations. On top of that, the **Bi-lateral Energy Resonance Converter (BERC)** is introduced to aggressively reduce the size of the resonant inductor, which are especially beneficial when dealing with high output current at low-voltage domain. This technique, which is applicable to hybrid SC type I that employs single inductor at the output, merges passives of adjacent stages in multi-stage approach. For the existing designs, several independent stages are cascaded with relatively large decoupling capacitors between them, and the energy conversion is done in the sequence of "$\cdots VIVVIV \cdots$". The core concept of BERC is to simplify the middle sequence of "$IVVI$" and reduce it to "I" with soft-charging operation maintained and less components needed. In practical implementations, as compared to the independent resonance within each individual stage in the conventional approach, a shared inductor of BERC now resonates with

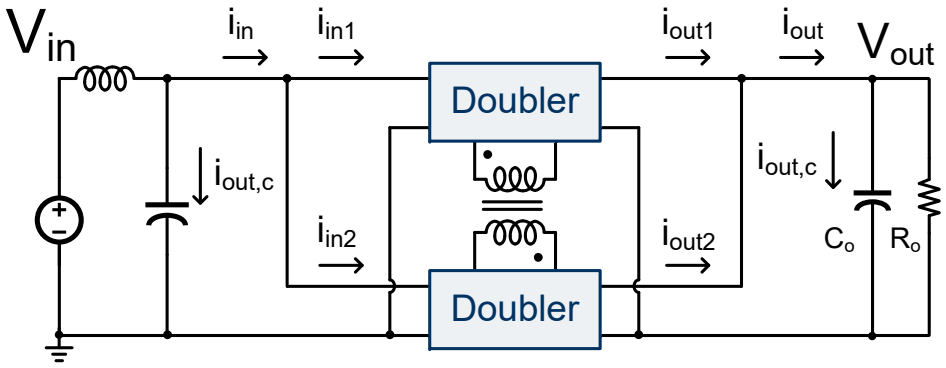
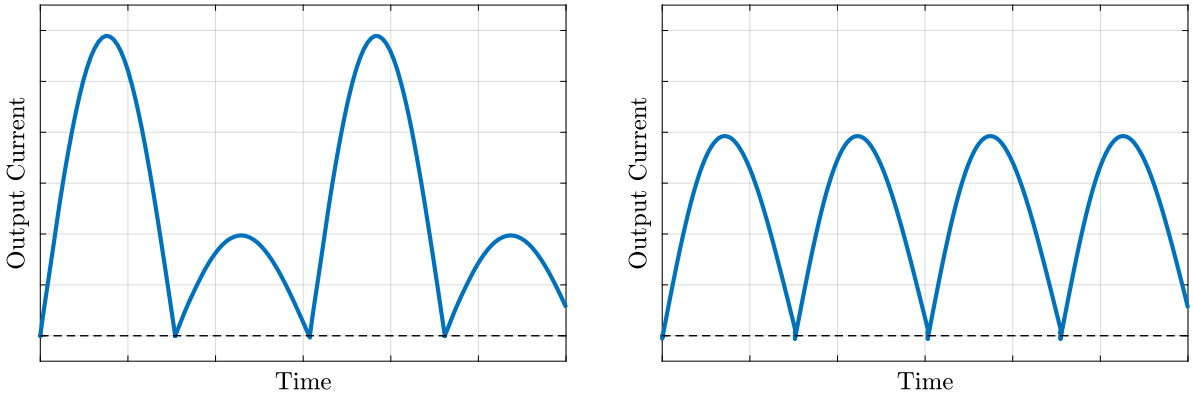


Figure 8.1: Simplified schematic of a 2-phase interleaved Doubler.



(a) 4-to-1 Series-Parallel topology

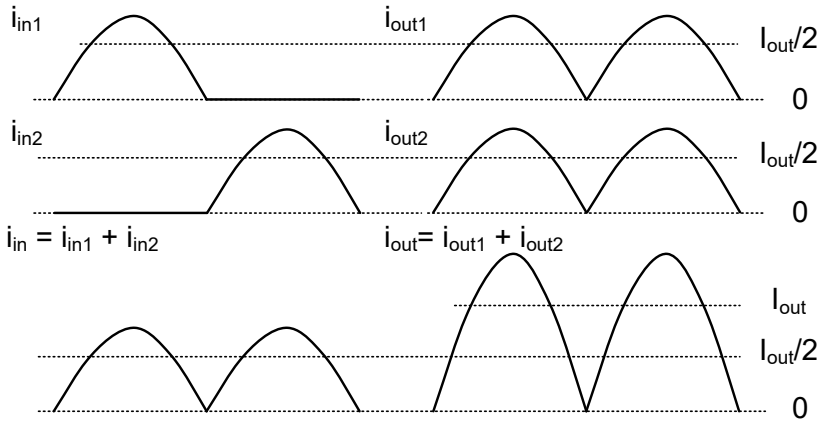
(b) 4-to-1 Dickson topology

Figure 8.2: (a) Unequal and (b) equal phase current in hybrid SC type-II.

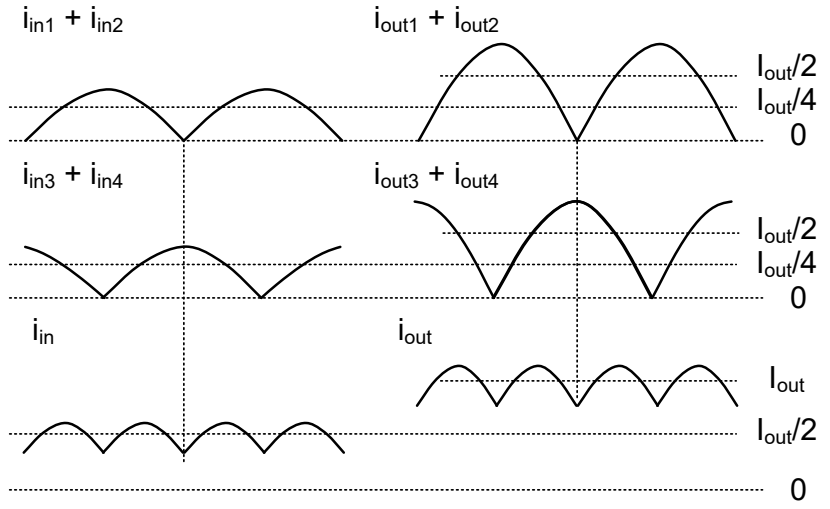
the flying capacitors in both stages. The BERC concept is first applied to doubler topology, obtaining higher power density and maintaining high efficiency, as compared to the cascaded resonant converter [27].

8.1 Filter Capacitor Ripple Reduction

The simplified schematic of a 2-phase interleaved doubler topology is shown in Fig. 8.1, with two converters operating with 180° (or π radians) out of phase between each other. The input RMS current can be reduced by $\sqrt{2}$ times from single phase to 2-phase operation, meaning the input capacitor requirement can be relaxed. However, with 2-phase interleaving, the effect of output current ripple reduction depends on the topologies: (i). reduced ripple when there is unequal phase current as shown in Fig. 8.2 (a), such as series-parallel and ladder topologies; (ii). no reduction effect when there is equal phase current as shown in Fig. 8.2 (b), such as doubler and Dickson topologies. Fig. 8.3 (a) shows the superposition of multi-



(a) 2-phase operation



(b) 4-phase operation

Figure 8.3: Input and output current waveforms of a (a) 2-phase and a (b) 4-phase interleaved Doubler converters.

phase doubler's input and output current, which also shows that output RMS current is not improved for 2-phase operation since i_{out1} and i_{out2} are in phase with the same amplitude. To further reduce the volume of input and output filter capacitor especially when dealing with high output current, another set of 2-phase interleave doubler can be added and the 4-phase interleaved converter can greatly reduce both input and output current ripples as shown in Fig. 8.3(b).

Table 8.1 quantitatively compares the input and output RMS current of the converter as well as the output voltage ripple for different numbers of phases. All of the values listed are normalized to I_{out} for the ease of comparison, where I_{out} is the average output current

Table 8.1: RMS current and output voltage ripple over different number of phases.

# of phases	**1**	**2**	**4**
Phase Shift	0	$(0, \pi)$	$(0, \pi)$, $(\frac{\pi}{2}, \frac{3\pi}{2})$
$I_{in,RMS}$	$\frac{\pi}{4} = 0.785$	$\frac{\pi}{4\sqrt{2}} = 0.555$	$\frac{\sqrt{\pi^2+\pi}}{8} = 0.502$
$I_{out,RMS}$	$\frac{\pi}{2\sqrt{2}} = 1.111$	$\frac{\pi}{2\sqrt{2}} = 1.111$	$\frac{\sqrt{\pi^2+\pi}}{4} = 1.005$
$I_{outc,RMS}$	$\frac{\sqrt{\pi^2-8}}{2\sqrt{2}} = 0.483$	$\frac{\sqrt{\pi^2-8}}{2\sqrt{2}} = 0.483$	$\frac{\sqrt{\pi^2+2\pi-16}}{4} = 0.098$
$V_{out,ripple}$	$\frac{2-\sqrt{2}}{8C_{out}f_{sw}}$	$\frac{2-\sqrt{2}}{8C_{out}f_{sw}}$	$\frac{2\sqrt{2}(1-\cos\frac{3\pi}{8})}{8C_{out}f_{sw}}$

† For number of phases greater than or equal to 2, $I_{in,RMS} = 2 \cdot I_{out,RMS}$ since i_{in} and i_{out} have the same waveform shapes but different amplitudes.

to the load. The input and output RMS current are derived using

$$I_{in/out,RMS} = \sqrt{\frac{1}{T}\int_0^T {i_{in/out}}^2 dt}, \tag{8.1}$$

where T is the switching or resonant period of each phase. It reflects the conduction loss in PCB traces and higher current path requires wider and shorter connections. Assuming the ac component of the output current is fully absorbed by the output capacitor, C_o, the maximum capacitor RMS current can be then derived by

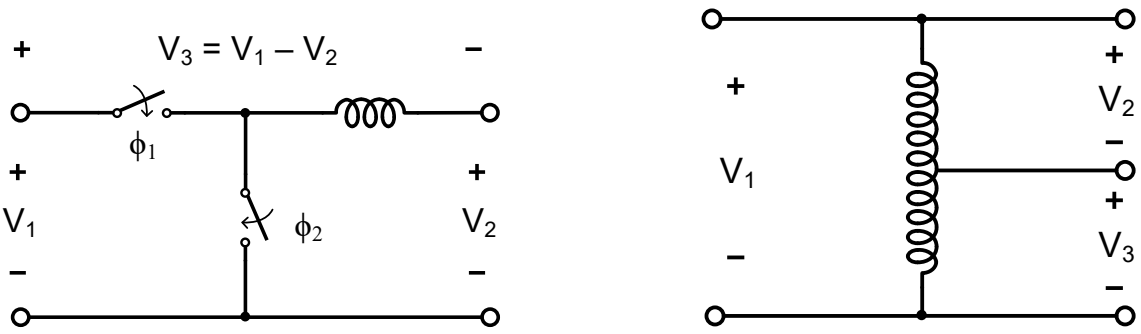
$$I_{outc,RMS} = \sqrt{\frac{1}{T}\int_0^T (i_{out} - I_{out})^2 dt}, \tag{8.2}$$

which determines the capacitors' operating temperature and the output voltage quality. In both (8.1) and (8.2), the superposition output current for a $2N$-phase interleaved doubler converter can be expressed as

$$i_{out,\phi=2N} = \frac{I_{out}}{2N} \cdot \frac{\pi}{2} \cdot \sum_{i=1}^{2N} \sin\left(\theta + \frac{\pi}{N}(i-1)\right),\ \theta \in \left[0, \frac{\pi}{N}\right], \tag{8.3}$$

which is periodic with $\frac{T}{2N}$ or $\frac{\pi}{N}$ (where $N \subset \mathbb{Z}^+$). The constant of $\frac{\pi}{2}$ in (8.3) comes from the conversion between average and peak values of a rectified sine wave. Given the instantaneous and average output current, the voltage ripple across the output capacitor can be derived by

$$\begin{cases} C_{out}\dfrac{dV_{out}}{dt} = i_{out} - I_{out} \\ \Delta V_{out} = V_{out,\max} - V_{out,\min} \end{cases}, \tag{8.4}$$



(a) VIV-type canonical switching cell (b) Symbolic representation

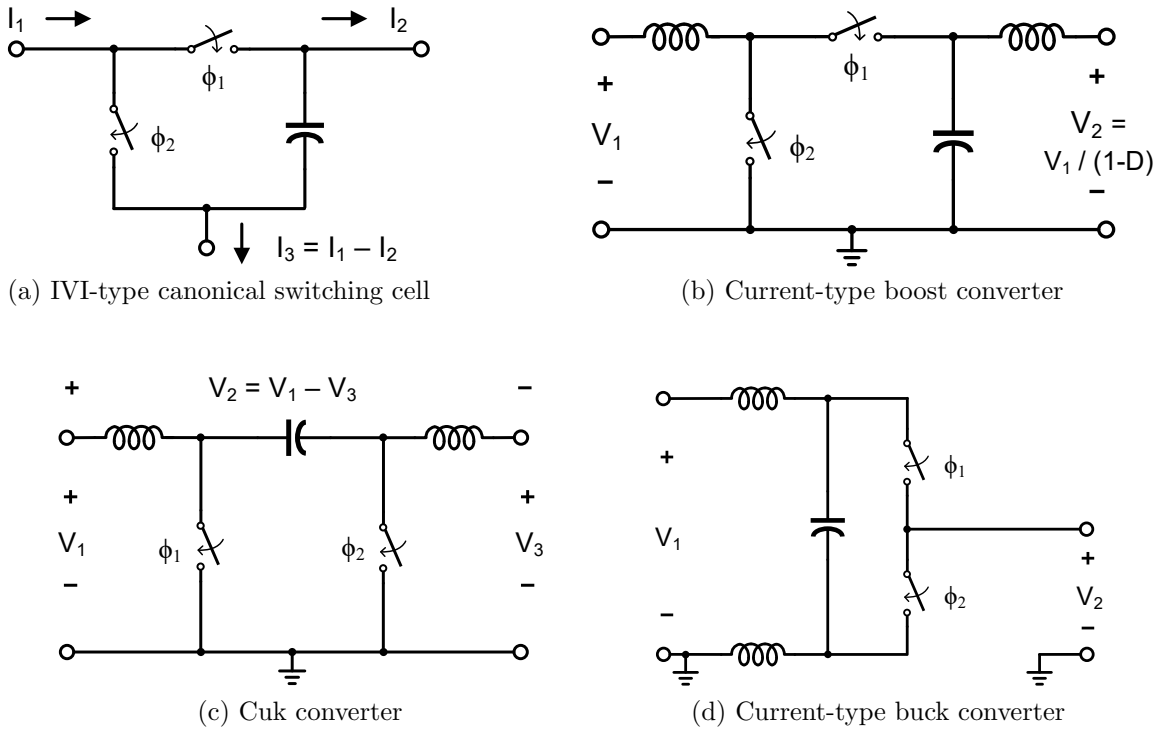
Figure 8.4: VIV-type canonical switching cell for magnetic-based converters and its symbolic representation.

where the maximum, $V_{out,\max}$, and minimum ,$V_{out,\min}$, happen when: $\theta_{\min} = \frac{\pi}{4}$ and $\theta_{\max} = \frac{3\pi}{4}$ in the case of 1 and 2 phases; $\theta_{\min} = \frac{\pi}{8}$ and $\theta_{\max} = \frac{3\pi}{8}$ in the case of 4 phases. Note that $I_{outc,RMS}$ can be reduced by 5 times from 2-phase to 4-phase operation; meanwhile, the output voltage ripple is reduced by 3 times given the same output current, switching frequency and output capacitance. Similarly, the input capacitance can be greatly reduced. By having more interleaving phases, the input and output RMS current can be smoothed out to approximately their average value, hence reducing the filter capacitor requirement and improving the power density. Considering the ripple reduction and the system complexity, a 4-phase interleaved operation is sufficient enough.

8.2 Canonical Switching Cells for Hybrid Switched-Capacitor Converter

In this section, the canonical switching cells for magnetic-based converters are revisited and a new type of fundamental hybrid SC cell will be derived from there. The most common VIV-type canonical cell, composed of two switches and an inductor is shown in Fig. 8.4 (a), is a typical three-terminal network. By tapping any two ports (i.e. two terminals per port) as the input and output, basic power converters including buck, boost and buck-boost converters can be synthesized. For example, a buck converter is formed by having V_1 and V_2 as input and output, respectively. Note that the common terminal of V_1 and V_2 is grounded in practical implementation, and therefore the input and output voltage have the same reference in a buck converter. During steady state, the inductor reaches a *volt-sec* balance and each port voltage can be expressed in terms of V_1:

$$\begin{cases} V_2 = D \cdot V_1 \\ V_3 = (1-D) \cdot V_1 \end{cases}. \tag{8.5}$$



(a) IVI-type canonical switching cell

(b) Current-type boost converter

(c) Cuk converter

(d) Current-type buck converter

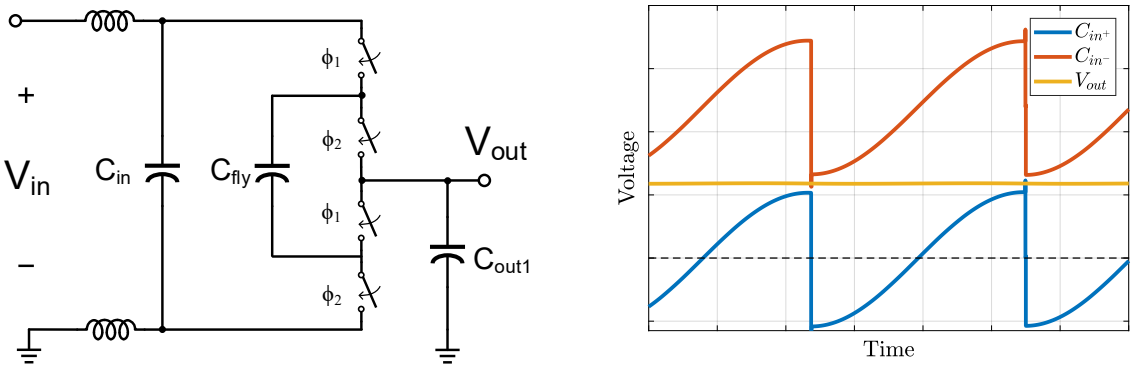
Figure 8.5: IVI-type canonical switching cell for magnetic-based converters.

This canonical cell can also be represented by an autotransformer shown in Fig. 8.4 (b). As opposed to the VIV-type cell transferring energy through an inductor, an IVI-type cell using a capacitor as the main element can be formed as shown in Fig. 8.5 (a) based on the current-voltage duality. Note the connection between actives and passives is transformed from T-network to π-network, and the key parameters that characterize the switching cell are replaced by terminal current. Similar to the port voltage in the VIV-type cell, all terminal current of the IVI-type cell can be derived using the charge balance on the capacitor:

$$\begin{cases} I_2 = D \cdot I_1 \\ V_3 = (1-D) \cdot I_1 \end{cases}. \tag{8.6}$$

The current-type switching cell amplifies current instead of voltage, and it can be used to form current-type power converters. In practical implementations, voltage sources are usually available and so inductors are used to transform voltage to current. For example, a current-type boost converter is shown in Fig. 8.5 (b), which has inductors between the input and output voltage sources. Particularly, a current-type buck-boost converters as shown in Fig. 8.5 (c) is also called Cuk converter, which is known for transferring energy through a capacitor.

The current-type power converters are advantageous in continuous input and output current, which helps reduce the size of filter capacitors. For example, as compared to the



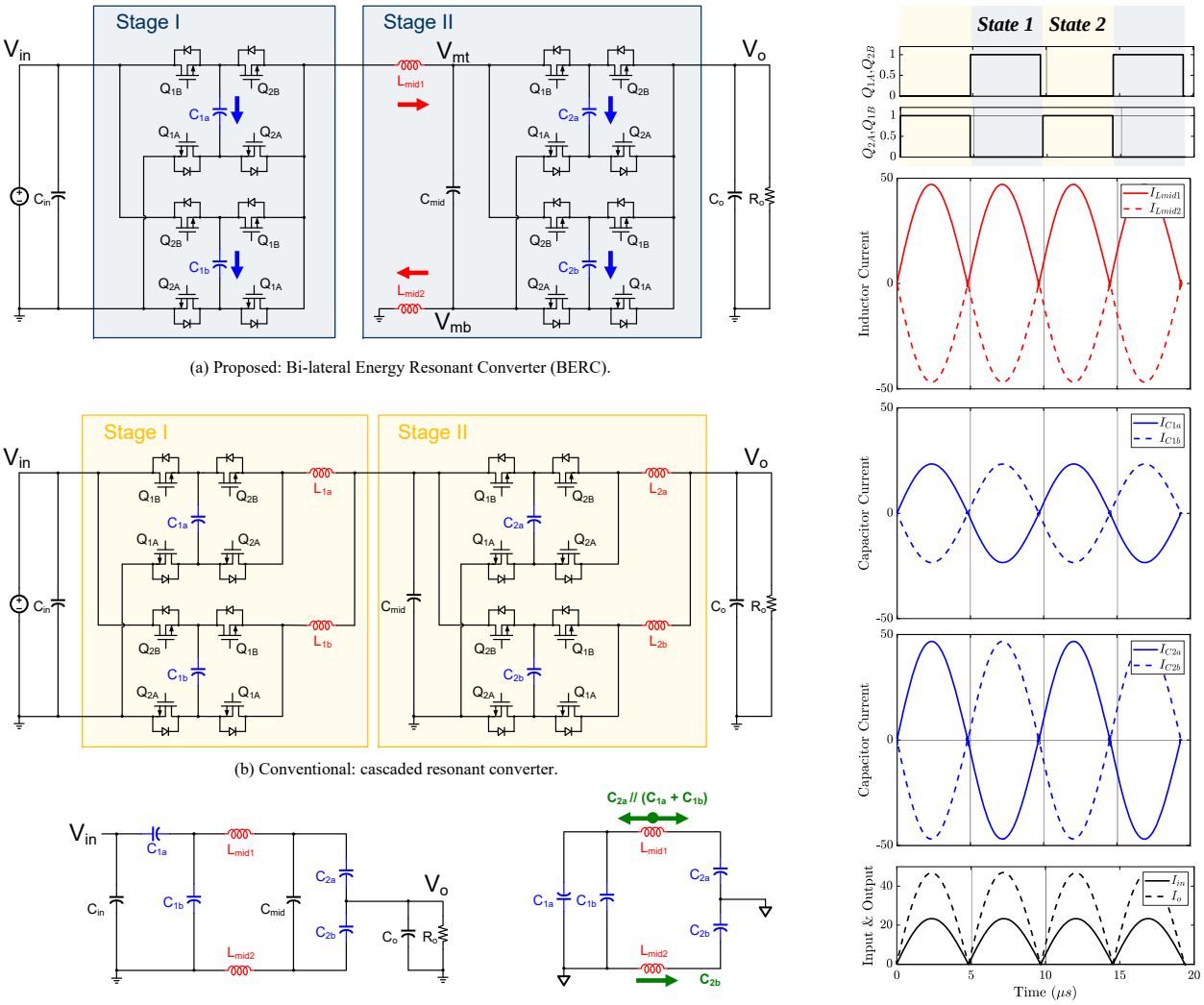
(a) (b)

Figure 8.6: Current-type hybrid switched-capacitor converters.

voltage-type buck converter, a current-type buck converter as shown in Fig. 8.5 (d) features two-phase interleaving with only two switches required. Through the voltage-type canonical switching cell, a voltage-type SC cell for hybrid SC converter was generated and defined in Chapter 4. Similarly, a current-type SC cell can be developed using the current-type switching cell, which is shown as Fig. 8.6 (a). Note the bypass capacitor has to be large enough so that the 2-to-1 SC structure can generate a nice flat voltage at the switching node or the output voltage, as shown in Fig. 8.6 (b). Although the current-type hybrid SC does not have lower switch current and voltage ratings as compared to a two-phased interleaved hybrid SC, the number of switches is reduced and it is particularly beneficial for discrete implementations. More importantly, it provides another type of energy transfer for hybrid SC, enabling a passive reduction technique – BERC.

8.3 Bi-lateral Energy Resonance Converter (BERC)

As shown in Fig. 8.6, the output inductor can be split and relocated to the input [56], which maintains all original features in conventional buck converter, with an extra benefit of decoupling capacitance reduction from continuous input and output current. The concept can be applied to ReSC-based converters for enabling the relocation of the inductor, which then provides an opportunity to merge inductors between two adjacent stages. The schematic of a dual-phase interleaved BERC is shown in Fig. 8.7 (a), which implements a 4-to-1 step-down conversion. For comparison, a conventional 4-to-1 cascaded resonant converter [27] is shown in Fig. 8.7 (b). The stage II of both converters has exactly the same circuit operation and switch stress, except that they have different inductor locations. As can be seen, the two output inductors, L_{2a} and L_{2b}, in the stage II of the conventional converter are now displaced and implemented by two middle inductors, L_{mid1} and L_{mid2}, in the BERC. The new location of L_{mid1} is shared between the output of the first stage and the input of the second stage, allowing the absorption of the other two inductors, L_{1a} and L_{1b}, in the



(a) Proposed: Bi-lateral Energy Resonant Converter (BERC).

(b) Conventional: cascaded resonant converter.

(c) Equivalent circuit during state 1 (Q_{1A} and Q_{2B} are high).

(d) ac equivalent circuit for (c).

(e) Key waveforms for BERC.

Figure 8.7: Schematic and circuit operation of a dual-phase Bi-lateral Energy Resonant Converter (BERC).

conventional first stage. As a result, the proposed BERC requires less inductors as compared to the conventional design, enabling higher power density.

There are mainly two circuit states for operating BERC with zero current switching (ZCS), while the converter switches at resonant frequency, f_{crit}. Two driving signal pairs $Q_{1A}-Q_{2B}$ and $Q_{2A}-Q_{1B}$ are complementary with each other, i.e. $Q_{1A} = Q_{2B} = \overline{Q_{2A}} = \overline{Q_{1B}}$. Note that a deadtime is available between each complementary pair to prevent shoot-through event. During state 1 or when $Q_{1A} - Q_{2B}$ is toggled high, the equivalent circuit of BERC is shown in Fig. 8.7 (c). When the converter is in state 2, the equivalent circuit can be formed by interchanging the locations of C_{1a} (C_{2a}) and C_{1b} (C_{2b}). The nominal blocking voltage is

$V_{in}/2 = 2V_o$ for switches and capacitors in the first stage; and $V_{in}/4 = V_o$ for those in the second stage, except $2V_o$ for C_{mid}.

In order to understand the resonant frequency, f_{crit}, of BERC, an ac equivalent circuit of Fig. 8.7 (c) is obtained as shown in Fig. 8.7 (d). The transformation of the two equivalent circuits implies that the input and output capacitance, C_{in} and C_o are assumed much larger than the flying capacitance, C_{1a-2b}, which is practical in most cases. Finally, owing to the current cancellation (highlighted and discussed in more details at the end of this section), the capacitor C_{mid} can be made sufficiently small such that the ac impedance is dominated by C_{2a} and C_{2b}, justifying C_{mid} removal from the ac model. For simplicity in control, f_{crit} for both states and both stages is maintained the same, and the resonant tank of the BERK needs to fulfill

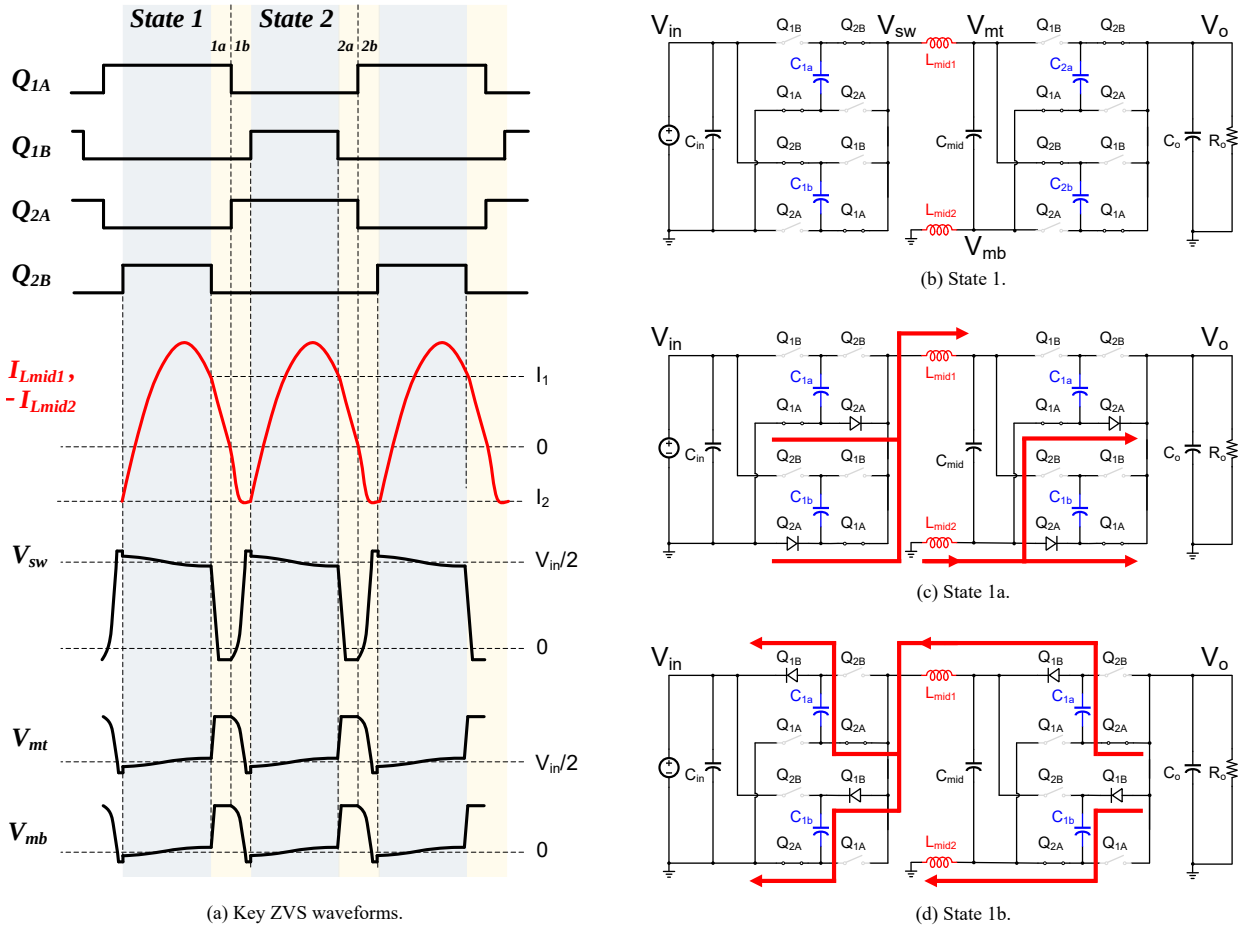
$$f_{crit} = \frac{1}{2\pi \cdot L_{mid1} \cdot \left(\frac{1}{2C_1} + \frac{1}{C_2}\right)^{-1}} = \frac{1}{2\pi \cdot L_{mid2} \cdot C_2}, \tag{8.7}$$

assuming $C_{1a} = C_{1b} = C_1$ and $C_{2a} = C_{2b} = C_2$ for a symmetric printed circuit board (PCB) layout consideration. According to (8.7), there exist an optimal values for C_1, C_2, L_{mid1} and L_{mid2} given their operating conditions and energy densities, e.g. C_1 sustains higher voltage than that of C_2 and therefore less capacitance density is available for C_1. In this work, it is designed that $C_1 = 0.5 \cdot C_2$ and $L_{mid1} = 2L_{mid2}$, for simplicity and compactness of PCB layout.

The key waveform for BERC is obtained as shown in Fig. 8.7 (e), following the passives design suggested by (8.7). By observing the symmetries between I_{Lmid1} and I_{Lmid2}, the resonant frequency is not only the same for both stages, but also for both operational states. The shared inductor, L_{mid1}, bridges between the flying capacitors of both stages, leading to a bi-lateral energy resonance: the flying capacitors, C_{1a} and C_{1b}, in stage I resonate with L_{mid1} through I_{Lmid1}; while C_{2a} and C_{2b} in stage II interchangeably resonate with L_{mid1} and L_{mid2}. Equalizing the resonant frequency also helps share the output current equally between two inductors, evenly spreading the current stress and the generated heat. Meanwhile, due to the mutual current elimination at the top and the bottom plates of C_{mid}, the energy processed by C_{mid} is greatly reduced and small capacitance is required to maintain small voltage ripple, justifying the assumption made in Fig. 8.7 (d).

Zero Voltage Switching Technique

While ZCS in the previous section is able to reduce significant VI overlap loss, the switching loss led from the transistor output capacitance, i.e. $P_{oss} = E_{oss} f_{sw} = C_{oss} V_{ds}^2 f_{sw}$, remains a large part of power losses especially for high-voltage and high-switching-frequency situations. Therefore, the development of a ZVS technique for BERC is critical, and four more states, i.e. states 1a, 1b, 2a and 2b as shown in Fig. 8.8 (a), are added to the two-state ZCS switching scheme. In order to turn on a switch with ZVS, a decent indicator is by observing if the inductor current turns on its body diode, implying E_{oss} is recycled through the inductor. For BERC, the inductor current needs to be bi-directional to achieve ZVS turn-on for all



(a) Key ZVS waveforms.

(b) State 1.

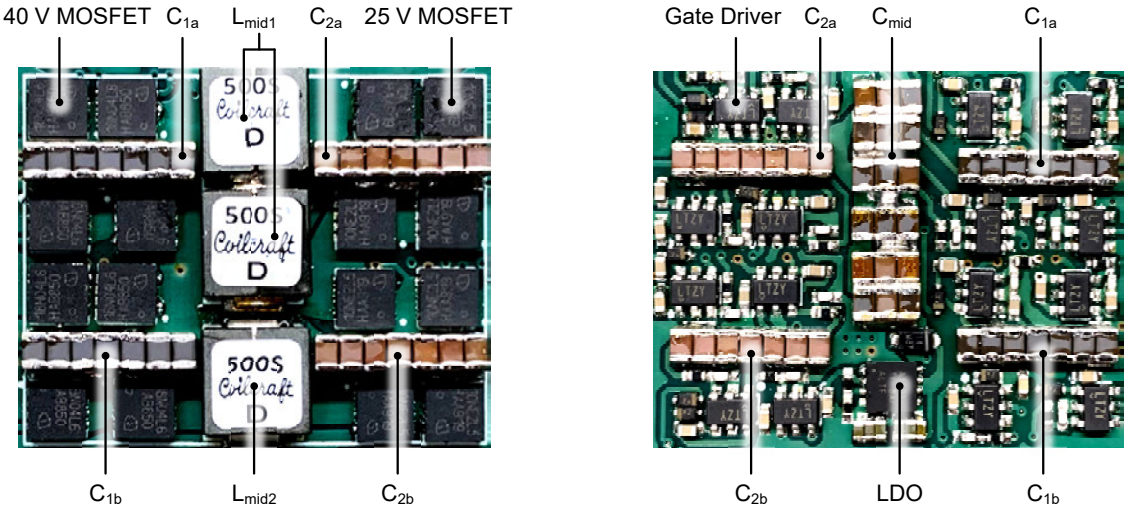
(c) State 1a.

(d) State 1b.

Figure 8.8: Zero voltage switching techniques for BERC.

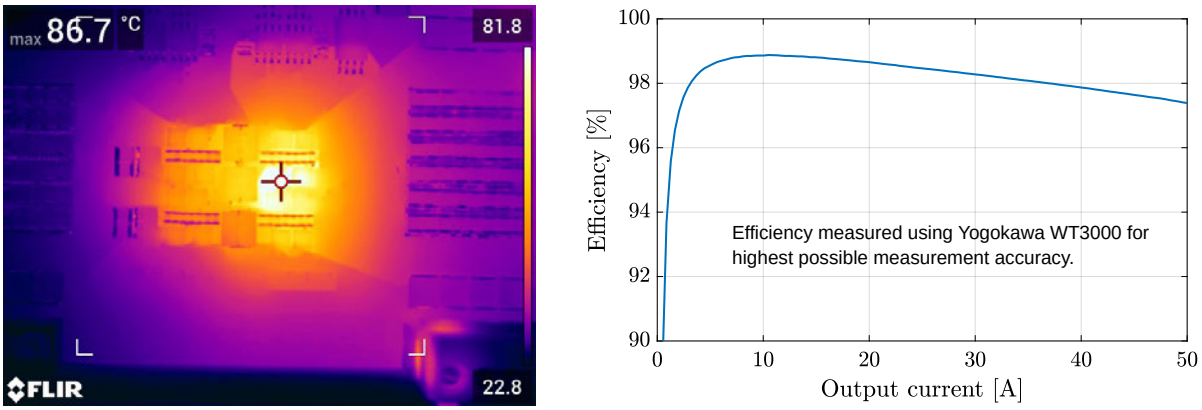
switches, since the negative terminals of the body diodes point toward and away from the inductor, e.g. the opposite directions of D_{2A} and D_{1B}.

Only the ZVS turn-on process for the transition from state 1 to state 2 is illustrated here, and the other transition can be derived accordingly. When state 1 is over or when Q_{2B} is off, switches driven by Q_{2A} and Q_{1B} should be turned on with ZVS. First, the body diode D_{2a} of Q_{2a} should turn on. To do so, the converter enters state 1a when Q_{2B} is turned off and the inductor current, I_{Lmid1}, is still positive, which aligns with the conducting directions of D_{2A} in the first stage. Meanwhile for the second stage, negative I_{Lmid2} is used to conduct D_{2A}. At this moment, Q_{2A} switches are ready for ZVS turn on. However, to prevent the body diodes of Q_{2B} from turning on and undermining the ZVS process, both Q_{1A} and Q_{2A} should be toggled before I_{Lmid1} becomes too negative or I_{Lmid2} becomes too positive. As the converter enters state 1b, negative I_{Lmid1} and positive I_{Lmid2} prepare Q_{1B} for ZVS turn on at the end of state 1b. As a result, BERC can smoothly transition from state 1 to state 2 through the two auxiliary states 1a and 1b.



(a) Top view (b) Bottom view

Figure 8.9: Prototype photograph of BERC, dimensions: 0.83 in x 1.04 in x 0.21 in (or 2.10 cm x 2.63 cm x 0.545 cm).



(a) (b)

Figure 8.10: BERC measurement results: (a) thermal monitor at 50 A output current with fan cooling, (b) efficiency plot for 48 V-to-12 V voltage conversion.

Measurement Results

An annotated photograph of the hardware prototype is shown in Fig. 8.9, with main components highlighted and detailed in Table I. All the switches are gate driven by LTC 4440, which supports high-voltage and high-current driving capabilities. The converter is tested up to 50 A output current, and the temperature monitored at full-load condition is shown in Fig. 8.10, where the peak temperature is 86.7^{o}C with only fan cooling. As a result, the peak power density is 3200 W/in^3. Meanwhile, the efficiency peaks at 98.9% with ZVS enabled. The fabricated PCB prototype has four layers, with 1-oz copper for each layer. The power

Table 8.2: Main components for the BERC PCB and their specifications.

Component	Part Number	Specification
Stage-1 MOSFET Switch	Infineon BSZ018N04LS6	40 V, 40 A, 1.8 $m\Omega_{max}$ @ 10 V_{GS}
Stage-1 Flying Capacitor, C_1	C2012X5R1V226M125AC	Rated 35 V, 22 μF x 21 for each C_1
Stage-2 MOSFET Switch	Infineon BSZ010NE2LS5	25 V, 40 A, 1 $m\Omega_{max}$ @ 10 V_{GS}
Stage-2 Bypass Capacitor, C_{mid}	C2012X5R1V226M125AC	Rated 35 V, 22 μF x 18
Stage-2 Flying Capacitor, C_2	C2012X6S1C226M125AC	Rated 16 V, 22 μF x 21 for each C_2
Stage-2 Inductor, L_{mid1}, L_{mid2}	Coilcraft SLC7530S-500	50 nH, 50A_{sat}, 0.123 $m\Omega_{nom}$

loss due to PCB traces is estimated to be more than 40 % of the overall conduction loss. It can be expected that 4-oz copper can further push the converter to higher efficiency and power density, without hitting the device thermal limits.

8.4 Chapter Summary

This chapter provides a quantitative analysis for multi-phase interleaved ReSC in terms of input, output and filter capacitor RMS current, which suggests a 4-phase ReSC can significantly reduce the passives requirement while maintaining low component counts. On top of that, the BERC techniques are developed to increase the energy utilization of the passive components, which improves power density while maintaining high efficiency. **BERC** features not only an improved passive utilization by merging inductors, but also an alternative interleaving technique for scaling up the output current. The BERC technique is especially beneficial for the multi-stage approach. An example of the fundamental 2-to-1 ReSC converter is employed for each stage in two-stage ReSC converters. The converter prototype enables a high power density of 3200 W/in^3 for 48-to-12 V applications, which is 28 % improvement compared to the conventional cascaded resonant converter, and the highest published performance to date for this class of converters. A ZVS technique specifically tailored for BERC improves the light load efficiency, enabling a peak efficiency of 98.9%. The BERC concept can be applied for the extension to other topologies as well as higher conversion ratios for two-stage ReSC converters [26].

Chapter 9

Conclusions

Hybrid or resonant SC (ReSC) converters showcase excellent switch and passive utilizations, owing to the efficient use of high-performance low-voltage switches and high-energy-density capacitors through the SC structure and the soft-charging operations. As compared to power converters using a single type of energy transfer element, i.e. capacitor- and magnetic-based converters, hybrid SC converters feature (i). smaller passive volume and (ii). lower conduction loss due to the elimination of charge sharing loss in SC converters; therefore, higher efficiency, higher power density and higher conversion ratio can be achieved.

Two types of soft-charging techniques are introduced to form hybrid SC converters, which are by (i). adding inductor at the SC converter output and (ii). adding distributed inductors in series with each flying capacitor of the SC converter. To extend the native conversion ratios, a fundamental voltage-type SC cell is defined and used to synthesize several SC topologies. Various topologies are evaluated through a comprehensive comparison framework based on an FoM – output conductance density, which provides a simpler guideline and a more holistic view for the design direction. In particular, it is found that the FoM is associated with the scaling trend of commercially available switches in terms of voltage ratings and implementation methods (either CMOS integration or discrete components). Together with the practical layout consideration, the switch utilization analysis has shown that (i) the Dickson topology has the best switch utilization when the full switch customization is available; yet, (ii) the series-parallel topology shows promising result when only the switch conductance or only the minimal number of switches is considered. In light of the comparison result for different applications, several topologies, including Dickson, FCML, series-parallel and doubler topologies, are designed, fabricated and measured with high performance.

An on-chip Dickson converter is the first CMOS implementation that showcases high efficiencies for a continuous conversion range between 4:1 and 15:1, suitable for aggressive energy-aware dynamic voltage scaling in portable devices. With the high switch utilization, the Dickson topology favors to low-voltage devices available in the commercial chip fabrication processes, advantageous in reducing the chip area and cost. For example, in the case of direct Li-ion battery (4 V) power conversion, the Dickson topology allows more voltage margin (more than 1.5 V) to 2.5V switches, hence improving the converter reliability. On the

other hand, a proposed on-chip ACC-PFM controller further solidifies hybrid SC converters' reliability by establishing a balancing voltage together with a full-range output voltage regulation through a hybrid approach, i.e. peak current-mode control with constant-off time and valley current-mode with constant-on time for a three-level converter. Also, the duty ratio deviation caused by level shifting, which is identified as one of the root causes for unbalanced flying capacitor voltage, is reduced to sub-nanoseconds through a dedicated delay equalizing level shifter.

The multi-stage approach further extends the hybrid SC converter to higher conversion ratios with high FoM maintained, by individually and optimally designing the high-voltage and high-current stages. It is found that the series-parallel topology is suitable for the low-voltage high-current stage since it has an excellent switch utilization for voltage below 25 V along with the best passive utilization. Also, the series-parallel topology has an easily predictable resonant frequency and simple controller/layout design, since the flying capacitors sustain the same voltage stress and the same voltage derating factors. Other than the selection of topologies for each stage, the multi-stage approach can be further improved by several passive reduction techniques, including the concepts of multi-phase interleaving and BERC. In particular, the novel BERC concept, employing both voltage- and current-type hybrid SC converters, is beneficial in merging inductors of adjacent cascaded stages and significantly improving the power density. The excellent passive utilization of BERC has been validated through an example of two-phase interleaved two-stage doubler topology, which showcases more than 3000 W/in^3.

To leverage the output conductance density in hybrid SC converters, innovative floating supplies and segmented gate driver are implemented and validated in different converters. In order to avoid a high area ratio of driving circuits, it is found that the selection of floating supplies highly depends on the available capacitance density ratio: the voltage borrowing technique is typically applied on-chip, whereas the bootstrap technique is for discrete solutions or given high capacitance density is available. Meanwhile, a general-purpose bootstrap circuit is provided, which allows driving floating switches at any level as long as its within the voltage range. The segmented gate driver eliminates the ringing while maintaining low conduction loss, with small area overhead, which is useful for applications where reliability and efficiency are critical.

In summary, hybrid SC converters have been demonstrated in theory and with hardware implementations that they are promising for high-performance power conversions. Strong future research momentum is expected on developing more efficient topologies, exploring broader device availability, improving light load performance (optimal gate driving and ZVS possibility), advancing more compact passives packaging, and even more interesting combinations of discrete and integrated solutions. Given the excellent results from discrete implementation, increasing interest can be foreseen in integrated solutions as pure SC ICs have been mature enough and reached their limited performance. As the demands of higher conversion ratio increase, for the pushes of efficiency improvement from both the perspectives of power delivery as well as the digital circuit or the energy harvesting devices, high-performance hybrid SC converters can find their wide applications.

Bibliography

[1] S. Jain, S. Khare, S. Yada, V. Ambili, P. Salihundam, S. Ramani, S. Muthukumar, M. Srinivasan, A. Kumar, S. K. Gb, R. Ramanarayanan, V. Erraguntla, J. Howard, S. Vangal, S. Dighe, G. Ruhl, P. Aseron, H. Wilson, N. Borkar, V. De, and S. Borkar, "A 280mV-to-1.2V wide-operating-range IA-32 processor in 32nm CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2012, pp. 66–68.

[2] K. Craig, Y. Shakhsheer, S. Arrabi, S. Khanna, J. Lach, and B. H. Calhoun, "A 32 b 90 nm Processor Implementing Panoptic DVS Achieving Energy Efficient Operation From Sub-Threshold to High Performance," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 545–552, 2014.

[3] B. C. Johnson, K. Shen, D. Piech, M. M. Ghanbari, K. Y. Li, R. Neely, J. M. Carmena, M. M. Maharbiz, and R. Muller, "StimDust: A $6.5mm^3$, wireless ultrasonic peripheral nerve stimulator with 82% peak chip efficiency," in *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2018, pp. 1–4.

[4] T. Ishii, S. Ning, M. Tanaka, K. Tsurumi, and K. Takeuchi, "Adaptive comparator bias-current control of $0.6V$ input boost converter for ReRAM program voltages in low power embedded applications," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2389–2397, Oct. 2016.

[5] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[6] H. Le, S. R. Sanders, and E. Alon, "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, 2011.

[7] L. G. Salem and P. P. Mercier, "A Recursive Switched-Capacitor DC-DC Converter Achieving $2^N - 1$ Ratios With High Efficiency Over a Wide Output Voltage Range," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2773–2787, 2014.

[8] A. Sarafianos and M. Steyaert, "Fully Integrated Wide Input Voltage Range Capacitive DC-DC Converters: The Folding Dickson Converter," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, pp. 1560–1570, 2015.

[9] H. Meyvaert, G. Villar Piqué, R. Karadi, H. J. Bergveld, and M. S. J. Steyaert, "A Light-Load-Efficient 111 Switched-Capacitor DC-DC Converter With 94.7% Efficiency While Delivering 100 mW at 3.3 V," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2849–2860, Dec. 2015.

[10] N. Butzen and M. S. J. Steyaert, "Scalable parasitic charge redistribution: Design of high-efficiency fully integrated switched-capacitor dc–dc converters," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2843–2853, 2016.

[11] A. Biswas, Y. Sinangil, and A. Chandrakasan, "A 28 nm FDSOI integrated reconfigurable switched-capacitor based step-up DC-DC converter with 88% peak efficiency," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, pp. 1540–1549, Jul. 2015.

[12] X. Liu, L. Huang, K. Ravichandran, and E. Sánchez-Sinencio, "A highly efficient reconfigurable charge pump energy harvester with wide harvesting range and two-dimensional MPPT for internet of things," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1302–1312, May 2016.

[13] S. Qin, Y. Lei, C. Barth, W. Liu, and R. C. N. Pilawa-Podgurski, "A high-efficiency high energy density buffer architecture for power pulsation decoupling in grid-interfaced converters," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2015, pp. 149–157.

[14] Z. Ye, S. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and comparison of passive component volume of hybrid resonant switched-capacitor converters," in *IEEE Control and Modeling for Power Electronics (COMPEL)*, Jun. 2019, pp. 1–8.

[15] J. Wibben and R. Harjani, "A High-Efficiency DC–DC Converter Using 2 nH Integrated Inductors," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 844–854, 2008.

[16] Xu Zhang and D. Maksimovic, "Digital PWM/PFM controller with input voltage feed-forward for synchronous buck converters," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2008, pp. 523–528.

[17] N. Sturcken, E. J. O'Sullivan, N. Wang, P. Herget, B. C. Webb, L. T. Romankiw, M. Petracca, R. Davies, R. E. Fontana, G. M. Decad, I. Kymissis, A. V. Peterchev, L. P. Carloni, W. J. Gallagher, and K. L. Shepard, "A 2.5d integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 244–254, Jan. 2013.

[18] C. Huang and P. K. T. Mok, "A 100 MHz 82.4% Efficiency Package-Bondwire Based Four-Phase Fully-Integrated Buck Converter With Flying Capacitor for Area Reduction," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 2977–2988, 2013.

[19] E. A. Burton, G. Schrom, F. Paillet, J. Douglas, W. J. Lambert, K. Radhakrishnan, and M. J. Hill, "FIVR — Fully integrated voltage regulators on 4th generation Intel® Core™ SoCs," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 432–439.

[20] S. J. Kim, Q. Khan, M. Talegaonkar, A. Elshazly, A. Rao, N. Griesert, G. Winter, W. McIntyre, and P. K. Hanumolu, "High Frequency Buck Converter Design Using Time-Based Control Techniques," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 990–1001, 2015.

[21] C. Schaef, N. Desai, H. Krishnamurthy, S. Weng, H. Do, W. Lambert, K. Radhakrishnan, K. Ravichandran, J. Tschanz, and V. De, "A Fully Integrated Voltage Regulator in 14nm CMOS with Package-Embedded Air-Core Inductor Featuring Self-Trimmed, Digitally Controlled Variable On-Time Discontinuous Conduction Mode Operation," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2019, pp. 154–156.

[22] J. T. Doyle, J. C. Stiff, S. Kulkarni, and A. Yildiz, "A Low Cost 100 MHz 2-Stage PSiP and Evolution to a Co-Packaged, Fully-Integrated Voltage Regulator for SoC Power Delivery," in *IEEE Custom Integrated Circuits Conference (CICC)*, 2019, pp. 1–8.

[23] C. Y. Leung, P. K. T. Mok, and K. N. Leung, "A 1-V integrated current-mode boost converter in standard 3.3/5-V CMOS technologies," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 11, pp. 2265–2274, Nov. 2005.

[24] S. Uprety and H. Lee, "A 93%-Power-Efficiency Photovoltaic Energy Harvester with Irradiance-Aware Auto-Reconfigurable MPPT Scheme Achieving 95% MPPT Efficiency Across $650uW$ to 1W and 2.9ms FOCV MPPT Transient Time," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2017, pp. 378–379.

[25] R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer," in *IEEE Power Electronics Specialists Conference (PESC)*, Jun. 2008, pp. 4008–4015.

[26] W. C. Liu, Z. Ye, and R. C. N. Pilawa-Podgurski, "A 97% peak efficiency and 308 A/in^3 current density 48-to-4 V two-stage resonant switched-capacitor converter for data center applications," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2020.

[27] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "The Cascaded Resonant Converter: A Hybrid Switched-Capacitor Topology with High Power Density and Efficiency," *IEEE Transactions on Power Electronics*, pp. 1–1, 2019.

[28] S. Jiang, S. Saggini, C. Nan, X. Li, C. Chung, and M. Yazdani, "Switched tank converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5048–5062, Jun. 2019.

[29] D. Reusch, S. Biswas, and Y. Zhang, "System optimization of a high power density non-isolated intermediate bus converter for 48 V server applications," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2018, pp. 2191–2197.

[30] M. H. Ahmed, A. Nabih, F. C. Lee, and Q. Li, "High-efficiency, high-density isolated/regulated 48V bus converter with a novel planar magnetic structure," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 468–475.

[31] *Demo manual DC2513A: LTC7821EUH high density hybrid step-down synchronous converter*, Analog Devices, Inc. [Online]. Available: `http://www.linear.com/demo/DC2513A`.

[32] Z. Ye, R. A. Abramson, and R. C. N. Pilawa-Podgurski, "A 48-to-6 v multi-resonant-doubler switched-capacitor converter for data center applications," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2020.

[33] Y. Li, X. Lyu, D. Cao, S. Jiang, and C. Nan, "A 98.55% efficiency switched-tank converter for data center application," *IEEE Transactions on Industry Applications*, vol. 54, no. 6, pp. 6205–6222, Nov. 2018.

[34] J. Baek, P. Wang, S. Jiang, and M. Chen, "LEGO-PoL: A 93.1% 54V-1.5V 300A Merged-Two-Stage Hybrid Converter with a Linear Extendable Group Operated Point-of-Load (LEGO-PoL) Architecture," in *IEEE Control and Modeling for Power Electronics (COMPEL)*, 2019.

[35] R. Das and H. Le, "A Regulated 48V-to-1V/100A 90.9%-Efficient Hybrid Converter for POL Applications in Data Centers and Telecommunication Systems," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 1997–2001.

[36] J. S. Rentmeister and J. T. Stauth, "A 48V:2V flying capacitor multilevel converter using current-limit control for flying capacitor balance," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2017, pp. 367–372.

[37] A. Kumar, S. Pervaiz, and K. K. Afridi, "Single-stage isolated 48V-to-1.8V point-of-load converter utilizing an impedance control network and integrated magnetic structures," in *IEEE Control and Modeling for Power Electronics (COMPEL)*, Jul. 2017, pp. 1–7.

[38] W. Liu, P. Assem, Y. Lei, P. K. Hanumolu, and R. Pilawa-Podgurski, "A 94.2%-peak-efficiency 1.53A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65nm CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2017, pp. 182–183.

[39] R. Pilawa-Podgurski and D. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1557–1567, Jul. 2012.

[40] W. Kim, D. Brooks, and G. Wei, "A fully-integrated 3-level DC-DC converter for nanosecond-scale DVFS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jan. 2012.

[41] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "A resonant switched-capacitor ic and embedded system for sub-module photovoltaic power management," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3043–3054, Dec. 2012.

[42] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking applications," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 549–552, Mar. 2006.

[43] G. Villar and E. Alarcon, "Monolithic integration of a 3-level DCM-operated low-floating-capacitor buck converter for DC-DC step-down donversion in standard CMOS," in *IEEE Power Electronics Specialists Conference (PESC)*, Jun. 2008, pp. 4229–4235.

[44] P. Kumar, V. A. Vaidya, H. Krishnamurthy, S. Kim, G. E. Matthew, S. Weng, B. Thiruvengadam, W. Proefrock, K. Ravichandran, and V. De, "A 0.4V-1V 0.2A/mm^2 70% efficient 500MHz fully integrated digitally controlled 3-level buck voltage regulator with on-die high density MIM capacitor in 22nm tri-gate CMOS," in *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2015, pp. 1–4.

[45] X. Liu, C. Huang, and P. K. T. Mok, "A high-frequency three-level buck converter with real-time calibration and wide output range for fast-DVS," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 582–595, Feb. 2018.

[46] J. Xue and H. Lee, "A 2 MHz 12-100 V 90% Efficiency Self-Balancing ZVS Reconfigurable Three-Level DC-DC Regulator With Constant-Frequency Adaptive-On-Time V^2 Control and Nanosecond-Scale ZVS Turn-On Delay," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2854–2866, Dec. 2016.

[47] C. Schaef, S. Weng, B. Choi, W. Lambert, K. Radhakrishnan, K. Ravichandran, J. Tschanz, and V. De, "A 93.8% Peak Efficiency, 5V-Input, 10A Max I_{LOAD} Flying Capacitor Multilevel Converter in 22nm CMOS Featuring Wide Output Voltage Range and Flying Capacitor Precharging," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2019, pp. 146–148.

[48] C. Schaef and J. T. Stauth, "A 3-Phase Resonant Switched Capacitor Converter Delivering 7.7 W at 85% Efficiency Using 1.1 nH PCB Trace Inductors," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2861–2869, Dec. 2015.

[49] S. S. Amin and P. P. Mercier, "A Fully Integrated Li-Ion-Compatible Hybrid Four-Level DC–DC Converter in 28-nm FDSOI," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 720–732, Mar. 2019.

[50] A. Abdulslam and P. P. Mercier, "A Symmetric Modified Multilevel Ladder PMIC for Battery-Connected Applications," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 3, pp. 767–780, 2020.

[51] P. Renz, M. Kaufmann, M. Lueders, and B. Wicht, "A Fully Integrated 85%-Peak-Efficiency Hybrid Multi Ratio Resonant DC-DC Converter with 3.0-to-4.5V Input and 500 μA -to-120mA Load Range," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2019, pp. 156–158.

[52] W. C. Liu, P. H. Ng, and R. C. N. Pilawa-Podgurski, "An 83 mA 96.8% peak efficiency 3-level boost converter with full-range auto-capacitor-calibrating pulse frequency modulation.," in *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2019, pp. 1–4.

[53] W. C. Liu, P. H. Ng, and R. Pilawa-Podgurski, "A Three-Level Boost Converter With Full-Range Auto-Capacitor-Compensation Pulse Frequency Modulation," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 3, pp. 744–755, 2020.

[54] Y. Lei and R. C. N. Pilawa-Podgurski, "A general method for analyzing resonant and soft-charging operation of switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5650–5664, Oct. 2015.

[55] P. T. Krein, *Elements of Power Electronics*, Second Edition. Oxford University Press, 2015.

[56] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, *Principles Of Power Electronics*. Addison-Wesley, 1991.

[57] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Springer US, 2001.

[58] S. R. Pasternak, M. H. Kiani, J. S. Rentmeister, and J. T. Stauth, "Modeling and performance limits of switched-capacitor dc–dc converters capable of resonant operation with a single inductor," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1746–1760, Dec. 2017.

[59] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "A 48-to-12 V Cascaded Resonant Switched-Capacitor Converter for Data Centers with 99% Peak Efficiency and 2500 W/in^3 Power Density," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 13–18.

[60] S. Coday, C. B. Barth, and R. C. N. Pilawa-Podgurski, "Characterization and modeling of ceramic capacitor losses under large signal operating conditions," in *IEEE Control and Modeling for Power Electronics (COMPEL)*, Jun. 2018, pp. 1–8.

[61] Y. Lei, W. Liu, and R. C. N. Pilawa-Podgurski, "An analytical method to evaluate and design hybrid switched-capacitor and multilevel converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2227–2240, Mar. 2018.

[62] Y. Lei, R. May, and R. C. N. Pilawa-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a dickson switched-capacitor converter," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 770–782, Jan. 2016.

[63] Y. Lei, C. Barth, S. Qin, W. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2-kW single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8570–8581, 2017.

[64] *Power and sensing selection guide*, Infineon Technologies AG. [Online]. Available: `www.infineon.com/powerandsensing-selectionguide`.

[65] *Chip multilayer ceramic capacitors for general*, Murata Manufacturing Company, Ltd.

[66] K. M. Cao, W. Lee, W. Liu, X. Jin, P. Su, S. K. H. Fung, J. X. An, B. Yu, and C. Hu, "BSIM4 gate leakage model including source-drain partition," in *IEEE International Electron Devices Meeting (IEDM)*, 2000, pp. 815–818.

[67] C. O. Mathuna, N. Wang, S. Kulkarni, and S. Roy, "Review of Integrated Magnetics for Power Supply on Chip (PwrSoC)," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4799–4816, 2012.

[68] X. Yu, W. Huang, M. Li, T. M. Comberiate, S. Gong, J. E. Schutt-Aine, and X. Li, "Ultra-small, high-frequency, and substrate-immune microtube inductors transformed from 2D to 3D," *Scientific Reports*, vol. 5, p. 9661, 2015.

[69] U. Chaudhry, C. DeVries, S. Kummerl, and C. H. Lim, *Powerful solutions come in small packages*, http://www.ti.com/lit/wp/sszy021/sszy021.pdf.

[70] Z. Liu, L. Cong, and H. Lee, "Design of on-chip gate drivers with power-efficient high-speed level shifting and dynamic timing control for high-voltage synchronous switching power converters," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 6, pp. 1463–1477, Jun. 2015.

[71] A. Seidel, M. S. Costa, J. Joos, and B. Wicht, "Area efficient integrated gate drivers based on high-voltage charge storing," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, pp. 1550–1559, 2015.

[72] T. M. Andersen, F. Krismer, J. W. Kolar, T. Toifl, C. Menolfi, L. Kull, T. Morf, M. Kossel, M. Brändli, and P. A. Francese, "A 10 W on-chip switched capacitor voltage regulator with feedforward regulation capability for granular microprocessor power delivery," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 378–393, Jan. 2017.

[73] S. Nagai, N. Negoro, T. Fukuda, N. Otsuka, H. Sakai, T. Ueda, T. Tanaka, and D. Ueda, "A DC-isolated gate drive IC with drive-by-microwave technology for power switching devices," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2012, pp. 404–406.

[74] P.-Y. Chiu and M.-D. Ker, "Metal-layer capacitors in the 65 nm CMOS process and the application for low-leakage power-rail ESD clamp circuit," *Microelectronics Reliability*, vol. 54, no. 1, pp. 64–70, 2014.

[75] D. El-Damak, S. Bandyopadhyay, and A. P. Chandrakasan, "A 93% efficiency reconfigurable switched-capacitor DC-DC converter using on-chip ferroelectric capacitors," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2013, pp. 374–375.

[76] R. L. Lin and F. C. Lee, "Single-power-supply-based transformerless IGBT/MOSFET gate driver with 100% high-side turn-on duty cycle operation performance using auxiliary bootstrapped charge pumper," in *PESC97, 28th Annual IEEE Power Electronics Specialists Conference*, vol. 2, Jun. 1997, 1205–1209 vol.2.

[77] Z. Ye, Y. Lei, W. C. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Improved bootstrap methods for powering floating gate drivers of flying capacitor multilevel converters and hybrid switched-capacitor converters," *IEEE Transactions on Power Electronics*, pp. 1–1, 2019.

[78] J. Jiang, Y. Lu, C. Huang, W. Ki, and P. K. T. Mok, "A 2-/3-phase fully integrated switched-capacitor DC-DC converter in bulk CMOS for energy-efficient digital circuits with 14% efficiency improvement," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2015, pp. 1–3.

[79] A. Stillwell, E. Candan, and R. C. N. Pilawa-Podgurski, "Active voltage balancing in flying capacitor multi-level converters with valley current detection and constant effective duty cycle control," *IEEE Transactions on Power Electronics*, pp. 1–1, 2019.

[80] D. Reusch, F. C. Lee, and M. Xu, "Three level buck converter with control and soft startup," in *2009 IEEE Energy Conversion Congress and Exposition*, Sep. 2009, pp. 31–35.

[81] J. S. Rentmeister, C. Schaef, B. X. Foo, and J. T. Stauth, "A flying capacitor multilevel converter with sampled valley-current detection for multi-mode operation and capacitor voltage balancing," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016, pp. 1–8.

[82] R. B. Ridley, "A new, continuous-time model for current-mode control (power convertors)," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 271–280, Apr. 1991.

[83] Z. Ye, Y. Lei, Z. Liao, and R. C. N. Pilawa-Podgurski, "Investigation of capacitor voltage balancing in practical implementations of flying capacitor multilevel converters," in *IEEE Control and Modeling for Power Electronics (COMPEL)*, Jul. 2017, pp. 1–7.

[84] W. C. Liu, Z. Ye, and R. C. N. Pilawa-Podgurski, "Comparative analysis on minimum output impedance of fixed-ratio hybrid switched capacitor converters," in *IEEE Control and Modeling for Power Electronics (COMPEL)*, Jun. 2019, pp. 1–7.

[85] Jingquan Chen, A. Prodic, R. W. Erickson, and D. Maksimovic, "Predictive digital current programmed control," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 411–419, Jan. 2003.

[86] H. Wei, C. Chan, U. Chio, S. Sin, S. U, R. P. Martins, and F. Maloberti, "An 8-b 400-MS/s 2-b-Per-Cycle SAR ADC With Resistive DAC," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 11, pp. 2763–2772, Nov. 2012.

[87] S. Wong, U. Chio, Y. Zhu, S. Sin, S. U, and R. P. Martins, "A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1783–1794, Aug. 2013.

[88] Y. Ahn, I. Jeon, and J. Roh, "A multiphase buck converter with a rotating phase-shedding scheme for efficient light-load control," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2673–2683, Nov. 2014.

[89] X. Jing and P. K. T. Mok, "A fast fixed-frequency adaptive-on-time boost converter with light load efficiency enhancement and predictable noise spectrum," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2442–2456, Oct. 2013.

[90] H. Park, M. Kim, and J. Jung, "Spread spectrum technique to reduce emi emission for an llc resonant converter using a hybrid modulation method," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3717–3721, May 2018.

[91] Y. Chu, J. A. Morroni, Y. K. Ramadass, J. Michael A. Davis, C. A. Brill, and F. D. Cimino, "Compensated active electro-magnetic interference filters," English, 20 180 295 758, 2019.

[92] C. Schaef and J. T. Stauth, "A highly integrated series–parallel switched-capacitor converter with 12 V input and quasi-resonant voltage-mode regulation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 456–464, Jun. 2018.

[93] P. H. McLaughlin, P. A. Kyaw, M. H. Kiani, C. R. Sullivan, and J. T. Stauth, "Two-phase interleaved resonant switched-capacitor dc-dc converter with coupled inductors and custom lc resonator," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 2497–2503.

[94] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.

[95] Pit-Leong Wong, Peng Xu, P. Yang, and F. C. Lee, "Performance improvements of interleaving vrms with coupling inductors," *IEEE Transactions on Power Electronics*, vol. 16, no. 4, pp. 499–507, Jul. 2001.

[96] Jieli Li, C. R. Sullivan, and A. Schultz, "Coupled-inductor design optimization for fast-response low-voltage dc-dc converters," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 2, Mar. 2002, 817–823 vol.2.

[97] S. Lu, M. Mu, Y. Jiao, F. C. Lee, and Z. Zhao, "Coupled inductors in interleaved multiphase three-level dc–dc converter for high-power applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 120–134, Jan. 2016.