Hybrid Switched-Capacitor Power Converters: Fundamental Limits and Design Techniques

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Hybrid Switched-Capacitor Power Converters: Fundamental Limits and Design Techniques

by

Zichao Ye

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The dissertation of Zichao Ye, titled **Hybrid Switched-Capacitor Power Converters: Fundamental Limits and Design Techniques**, is approved:

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University of California, Berkeley

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Abstract

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Doctor of Philosophy in Engineering — Electrical Engineering and Computer Sciences

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Associate Professor Robert C.N. Pilawa-Podgurski, Chair

In this dissertation, we develop and explore very-high-performance power conversion systems for emerging applications that require high efficiency and high power density simultaneously, such as large-scale data center power delivery and mobile computing on portable and wearable electronics.

This work focuses on a topological effort to drastically improve the performance of existing power electronics. In particular, a hybrid approach is adopted, in which both inductors and capacitors are used in the voltage conversion and power transfer process. Compared to conventional switched-capacitor (SC) converters, the augmenting inductors can greatly reduce or eliminate the capacitor charge sharing loss, and thus improve the energy utilization of the capacitors without sacrificing efficiency. This process is called soft-charging operation. In combination with other potential advantages such as soft switching and voltage regulation, hybrid SC converters show promise in the development of future high-performance power electronics systems.

This dissertation explores hybrid SC converters from three main aspects: fundamental limits and topology comparisons, practical circuit implementation challenges, and high-performance hardware demonstrations. We start by analyzing the reactive power processed by the passive components of hybrid SC converters operating in resonant mode. This analysis is applied to express and optimize the total passive component volume of resonant switched-capacitor (ReSC) converters. To compare different ReSC topologies, a normalized passive volume parameter is proposed for simple and fair comparison. This normalized passive volume parameter, along with a normalized switch stress parameter (based on switch VA ratings), can be used to visualize and compare the passive and active component utilizations among different topologies, offering a framework to compare the relative performance of different topologies.

The large number of floating switches and flying capacitors pose great challenges in practical circuit implementations. Several bootstrap and charge-pump based techniques are developed to provide gate drive power to the floating switches in a compact and efficient manner. Compared to conventional isolated dc/dc power supply chips, the proposed circuits have a simple structure and operating principle, and can be implemented with a small number of diodes, capacitors, and LDOs, leading to less occupied board area and lower implementation cost. Another crucial practical challenge is flying capacitor voltage balancing. In unbalaced operation, capacitor voltages deviate from their nominal values, potentially resulting in system failure. We experimentally investigate the origins of the voltage imbalance in practical implementations of flying capacitor multilevel (FCML) converters and present corresponding solutions. It is found that an FCML converter with an even number of levels has significantly better capacitor balancing than one with an odd number of levels, due to better inherent immunity to circuit non-idealities.

With the theoretical analysis tools and the practical circuit techniques developed above, a number of high-performance discrete hardware prototypes are designed in the context of 48 V power delivery architecture for modern data centers. Based on a novel cascaded resonant topology, a 48-to-12 V, 4-to-1 fixed-ratio, intermediate bus converter is built with 99% peak efficiency and 2500 W/in^3 power density. To further increase the conversion ratio without increasing circuit complexity, the concept of multi-phase operation is introduced, along with a 6-to-1 cascaded series-parallel topology and an 8-to-1 multi-resonant-doubler topology. In addition to fixed-ratio ReSC converters, a regulated multi-level binary hybrid converter for direct 48 V to 1–2 V point-of-load applications is also developed. All of the hardware prototypes achieve the best in-class efficiency and power density simultaneously, reflecting the great potential of hybrid and resonant switched-capacitor converters for future power conversion systems.

To my family

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The completion of this dissertation is an important milestone in my life as it marks the closure of my graduate school journey. The young adulthood years are of singular importance and I have no regrets having spent them with a world class engineering research group. I am sincerely thankful for the many great people I have met on my journey; their mentorship, support, love, and care are the driving force that keeps me going and makes me want to better myself.

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to Yutian and Shibin, my big brothers and role models. I am greatly indebted for the strong push they gave me at start of my graduate studies. I appreciate their wisdom, humor, and the hotwok lunch boxes we had together. Yutian's leading work on hybrid switched capacitors set a high bar for me to leap and has been the driving force behind my pursuit of excellence to this day. I also wish to thank Joseph and Pourya for being supportive peers throughout our journey. We started together in the same year and now we are finishing together. The classes we took, the circuits we drew, the snacks we shared, and the seasons we had in the sun are sure to be wonderful memories I will cherish forever. A special thanks to Zitao, the best artist among all the engineers I know, and probably the best engineer amongst all artists! Many of the figures and photos in my papers and slides would not look as good as they do without his advice and help. Moreover, Zitao and his wife Yun Hao had been with me throughout the many highs and lows of graduate school. Their presence and support were indispensable for me in navigating through the difficulties of 2020 due to COVID-19 and I cannot overstate my gratitude. Many thanks to Rose for working on multiple projects with me. Her coding and soldering were instrumental in achieving many of the records we broke together. She also provided English editing help for many of our publications. Heartfelt thanks to Nathan Pallo for building and operating a well-equipped group laboratory, and to Maggie and Sam for making birthday cakes and desserts for everyone in the group. Each of you went out of your way to make my graduate life more memorable and I am incredibly thankful for it.

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Chapter 1

Introduction

1.1 Introduction

Power converters are electrical energy processing circuits to convert and control energy flow between different voltage domains and magnitudes. Similar to the blood circulatory system in the human body, power converters manage and deliver the requisite electrical energy in computer systems, personal electronics, automobiles, and just about every possible application of electricity. The most desirable features of power converters are high reliability, high energy efficiency, high power density, and low cost.

Thanks to continued research and development in the past decades, switch-mode power supplies with two alternating voltage levels (such as buck and boost converters) have become prevalent, offering high reliability and low cost. However, a variety of applications have recently emerged with very challenging design requirements that conventional technologies cannot meet. For instance, in space- and thermally-constrained smartphone systems, the conventional buck-based battery chargers cannot support the demand of faster charging speed, owing to their limited efficiency performance. In datacenter and telecommunication systems, the explosive growth of information processing and the associated energy consumption require innovative power delivery architecture and technology with better efficiency and power density.

Due to the fundamental structure of conventional two-level designs, trends toward higher efficiency and power density have reached the point that further improvement becomes increasingly difficult. It is therefore important to rethink the whole problem and come up with new solutions which could achieve a drastic performance improvement. This dissertation focuses on a topological effort to more efficiently utilize the active and passive devices, through a hybrid switched-capacitor/inductor approach. By introducing more switches, the system can have more than two voltage levels (as in the conventional structures). This allows for the use of high-energy-density capacitors in the voltage conversion process and thus reduces the size and loss of the inductive elements. These inductive elements in turn softly charge/discharge the capacitors, reducing the capacitor charge sharing loss.

We believe that increasing the system complexity can offer many advantages and is oftentimes necessary to improve performance. However, it should be done in appropriate ways, which requires a good understanding of both the fundamental limits and the practical design techniques. In this work, we analyze the theoretical benefits of hybrid and resonant switched-capacitor converters, address the important circuit implementation challenges, and design hardware prototypes with cutting-edge performance.

1.2 Organization of Thesis

Chapter 2 starts with the fundamental limitations of conventional switched-inductor and switched-capacitor converters and details the attractive benefits of hybrid resonant switched-capacitor converters. The concept of soft-charging operation is reviewed, together with different possible operating modes including fixed-ratio resonant mode and PWM regulated mode. The characteristics of different inductor augmenting strategies are also discussed.

Chapter 3 presents a new technique to calculate the passive component volume of hybrid resonant switched-capacitor converters, based on the fundamental processed reactive energy. Combining with the switch stress parameter (switch VA ratings), a framework to showcase the relative performance of different topologies is created, which can be used to visualize and compare the utilization of passive and active components.

Several important challenges in the practical implementation of high-performance hybrid switched-capacitor converters are addressed in Chapters 4 and 5. In Chapter 4, a number of bootstrap and charge pump based circuit techniques are developed to power the large number of floating gate drivers in these topologies, in a compact and efficient manner. In Chapter 5, the origins of flying capacitor voltage imbalance in practical flying capacitor multilevel converter designs are investigated experimentally. The presence of non-ideal source impedance and gate signal delay mismatch are found to have non-negligible impacts on capacitor balancing, and even-level designs are proved to have stronger inherent immunity to such nonidealities than odd-level designs.

With the above theoretical and practical knowledge, a number of very high-performance discrete prototypes are designed for emerging datacenter power delivery applications in Chapters 6 through 8. Following a brief overview of different datacenter power delivery architectures, Chapter 6 presents a 48 V to 12 V intermediate bus converter design based on a novel cascaded resonant topology, with 99.0% peak efficiency and 2500 W/in^3 power density. The main performance-enhancing features in this design - the two-phase interleaving concept and the zero-voltage-switching control technique - can also be applied to other resonant switched-capacitor topologies.

Chapter 7 further explores the use of resonant SC converters as intermediate bus converters with high conversion ratios, as recent research suggests that a 4 - 6 V intermediate bus voltage could provide the best overall system efficiency. A major challenge in implementing these converters at high conversion ratios is the large number of circuit components. To address this challenge, we introduce a multi-operating-phase concept to greatly reduce the

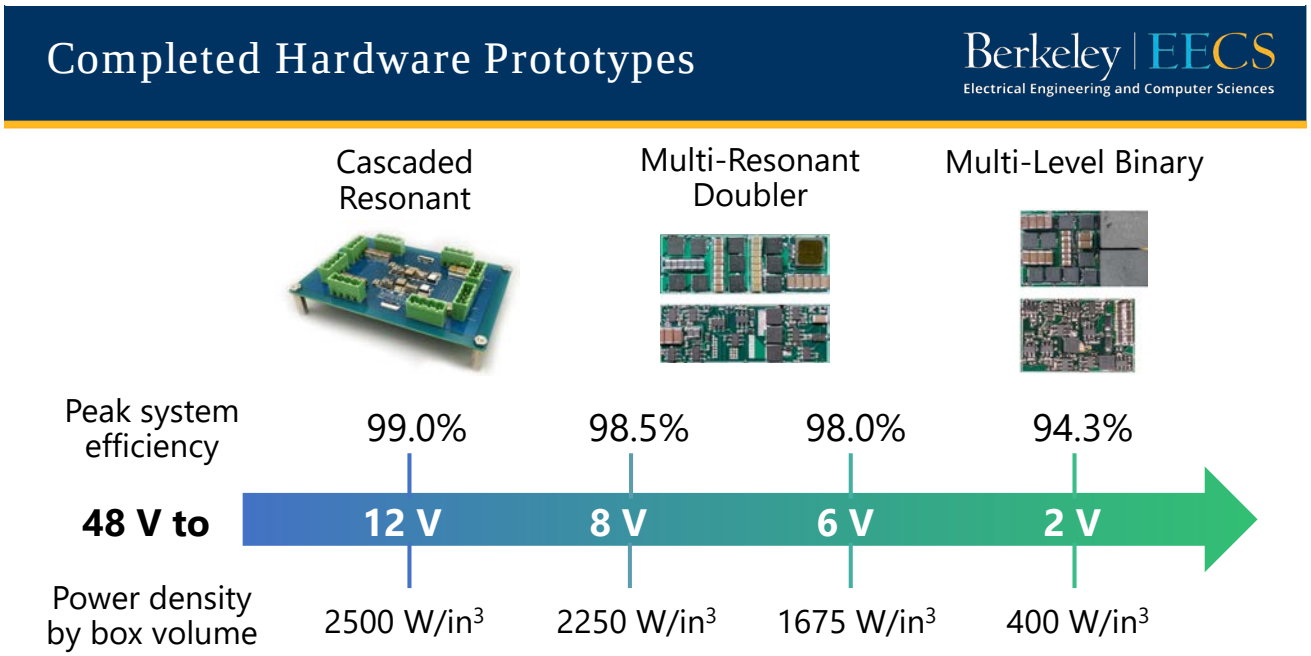


Figure 1.1: Performance summary of the hybrid and resonant SC converter prototypes presented in this dissertation.

circuit complexity and present a family of multi-phase resonant SC topologies. A 48 V to 6 V multi-resonant-doubler converter is presented with 98.0% peak efficiency and 1675 W/in^3 power density.

Chapter 8 extends the multi-operating-phase concept from fixed-ratio resonant SC converters to regulated hybrid SC converters. A multi-level doubler topology with merged 8-to-1 SC stage and two-phase interleaved buck stage is proposed for direct 48 V to point-of-load applications. Its prototype achieves 95.1% peak efficiency from 48 V to 2V, with near 400 W/in^3 power density, demonstrating one of the best in-class performance. Fig. 1.1 summarizes the performance of the three hardware prototypes presented in Chapters 6 through 8.

Chapter 9 discusses some present challenges and suggests areas for future work. Finally, conclusions are given in Chapter 10.

Chapter 2

Fundamentals of Hybrid and Resonant Switched-Capacitor Converters

This chapter first highlights the fundamental limitations of conventional switched-inductor and switched-capacitor (SC) power converters, and then motivates the unique characteristics of hybrid and resonant SC converters. The concept of soft-charging operation is reviewed, followed by different modes of operation to achieve soft-charging. A three-level buck converter and a 2-to-1 resonant SC converter are introduced as examples. The pros and cons of different inductor augmenting strategies are also discussed.

2.1 Limitations of Conventional Topologies

Switched-Inductor Converters

A commonly used switched-mode dc/dc power converter is a buck converter, and its circuit schematic is shown in Fig. 2.1. It can achieve voltage step-down with two switches and one inductor, by switching between two circuit states. In State 1, S_{1A} is on and S_{1B} is off, so that the switch node voltage V_{sw} sees the input voltage V_{in} and the inductor current ramps up. In State 2, S_{1A} turns off and S_{1B} turns on. Then, V_{sw} is pulled to ground and the inductor current ramps down. Through inductor volt-second analysis, it can be derived that $V_{\text{out}} = DV_{\text{in}}$, where D is the duty ratio defined as the time of State 1 over the total time of the two states. The reactive energy that needs to be processed in the inductor per switching cycle is $E_L = \frac{(1-D)P_{\text{out}}}{f_{sw}}$, where P_{out} is the output power and f_{sw} is the switching frequency. More details about the processed reactive energy of passive components are presented in Chapter 3.

There is an inherent trade-off between achievable efficiency and power density in power converter designs. Since the passive components (e.g. inductors) oftentimes contribute a

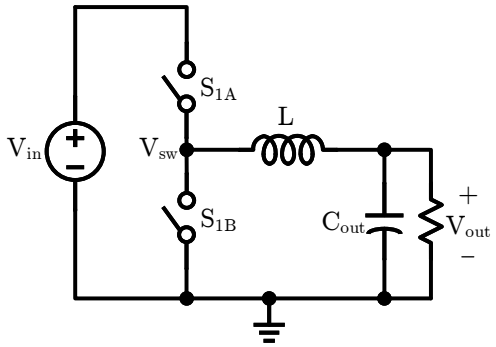


Figure 2.1: Schematic drawing of a buck converter.

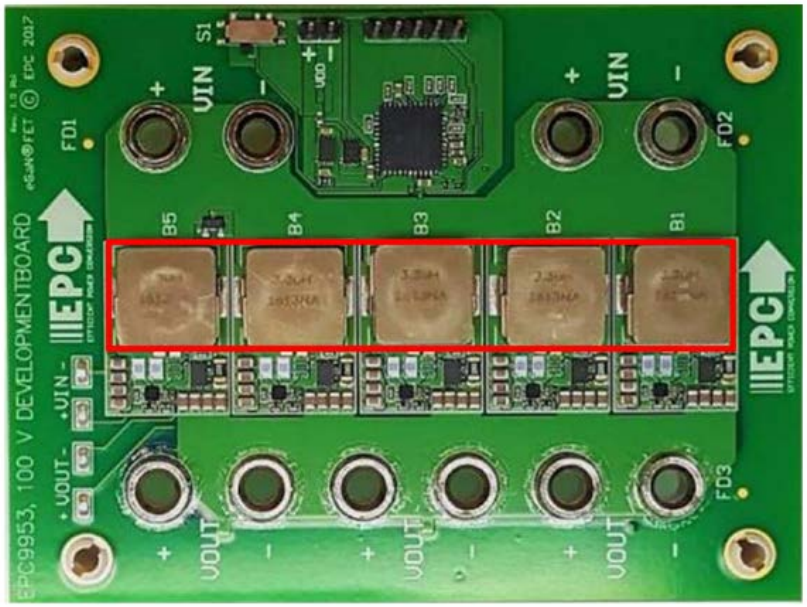


Figure 2.2: A high-performance GaN-based 48-to-12 V buck converter [1].

great portion to the overall volume, it is desirable to reduce their stored energy and therefore physical size by operating at a high switching frequency. However, this will inevitably result in an increase of semiconductor switching loss, magnetic core loss and ac winding loss, as well as other frequency-dependent losses.

The work in [1] reports a highly optimized GaN-based buck converter design for 48-to-12 V data center applications. Owing to the relatively poor energy density of inductors, the converter is designed to operate at 500 kHz. It achieves 96% efficiency and 1000 W/in^3 power density. However, as can be seen in Fig. 2.2, the inductors dominate the size of the overall

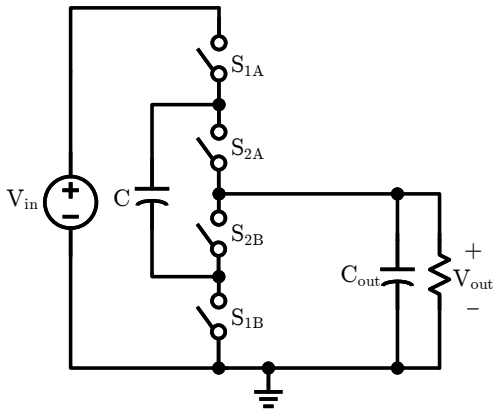


Figure 2.3: Schematic drawing of a 2-to-1 SC converter.

solution. It is difficult to further improve the power density without sacrificing the efficiency, regardless of the advancement of semiconductor technology. On the other hand, the room for efficiency improvement by operating at a lower switching frequency is also limited. Owing to the various loss mechanisms of inductors, it is very challenging to design a buck converter with greater than 98% efficiency for 48-to-12 V conversion, even at a relatively low frequency of 100 to 200 kHz.

Switched-Capacitor Converters

In comparison to inductors, capacitors are known to have much higher energy densities (e.g., up to 100x-1000x higher) [2], [3]. Specifically, multilayer ceramic capacitors (MLCCs), with their high energy density (comparable to electrolytic capacitors) and low dissipation factor (typically less than 5%), are suitable candidates for energy transfer in power converters. Converters that use only capacitors in the energy conversion process are called switched-capacitor (SC) converters [4]–[6].

The schematic drawing of a basic 2-to-1 SC converter is shown in Fig. 2.3. In the first half switching cycle, switch S_{1A} and S_{2B} are on, and the series combination of flying capacitor C and the output is charged by the input voltage source. In the second half switching cycle, S_{2A} and S_{1B} are on. The input is disconnected and the output is powered by the flying capacitor. Through capacitor "charge multiplier vector" analysis [7], it can be found that the flying capacitor voltage and the output voltage are fixed at $V_C = V_{out} = \frac{1}{2}V_{in}$ for the no-load condition. Thanks to the additional voltage level ($\frac{1}{2}V_{in}$) provided by the flying capacitor, the voltage that needs to be blocked by each switch is only $\frac{1}{2}V_{in}$. This allows for the use of low-voltage switches as compared to the conventional two-level switched-inductor converters (e.g., buck converters), in which the switches need to block the full high-level voltage in the system.

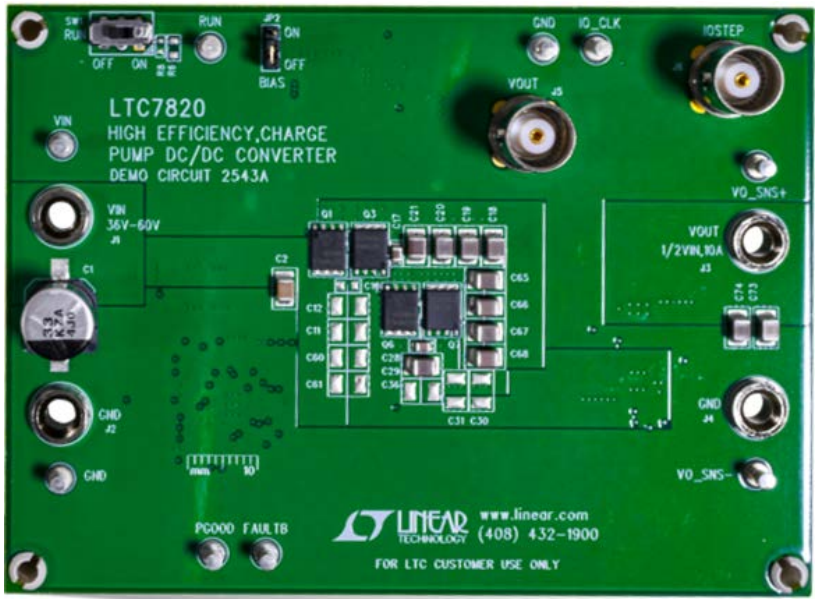


Figure 2.4: A high-performance 48-to-24 V switched-capacitor converter [8].

Historically, SC converters are most commonly used as low-power fully integrated converters, due to the fact that SC topologies can achieve lower switch stress at high conversion ratios and capacitors are easier to be integrated on-chip than inductors [9], [10]. In the past, they were less favored for discrete applications (> 10 W) because of the lack of lossless regulation capability, and the efficiency and electromagnetic interference (EMI) challenges associated with charge sharing loss. Recently, there has been a trend to use SC converters for high-power performance-driven applications, where the stringent efficiency and power density requirements cannot be achieved by inductor-based converters. In these applications, the voltage regulation requirement is not as important. Fig. 2.4 shows the photograph of a commercially available 48-to-24 V, 20 A SC converter [8]. It demonstrates up to 99% efficiency and 4000 W/in^3 power density, along with rugged start-up and protection features.

However, regardless of the dedicated design, this SC converter still suffers from the fundamental loss mechanism in pure capacitor-based converters: capacitor charge sharing loss (also known as charge redistribution loss). Here, we briefly review the origin and effects of this loss.

Fig. 2.5 shows the generic SC converter model as well as the output impedance curve with respect to the switching frequency. The generic SC model [11] consists of an ideal transformer and an output impedance R_{out}. The ideal transformer represents the nominal conversion ratio of the converter. The output impedance R_{out} incorporates both the conduction loss of the converter as well as the capacitor charge sharing loss, and is a good indication of the efficiency performance of the converter. This impedance is usually plotted against the

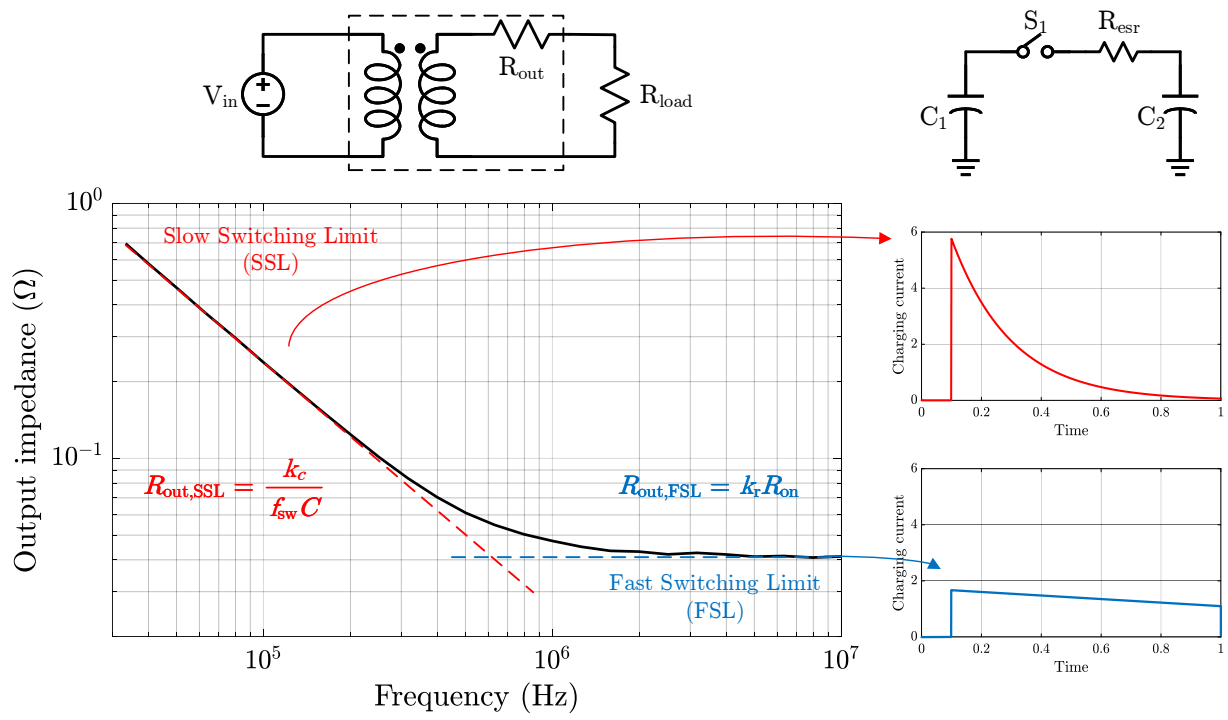


Figure 2.5: Pure SC converter: ideal circuit model, output impedance vs. switching frequency, origin of capacitor charge sharing loss (capacitor charging current at SSL and FSL).

switching frequency to reveal the characteristics of the SC converters. It can be seen that there are two asymptotic operating regions: the fast switching limit (FSL) and the slow switching limit (SSL) [4], [5], [7], [12], [13]. The FSL represents the lowest achievable output impedance of a SC converter. It occurs at high switching frequencies where the capacitor charge transfer is incomplete and the charging current is nearly constant per switching cycle. In this case, the dominating loss is the conduction loss due to the series resistance in the converter (e.g., switch resistance, flying capacitor ESR, PCB trace resistance) and is independent of switching frequency.

On the other hand, the SSL occurs at low switching frequencies, when the output impedance is dominated by the capacitor charge sharing loss, owing to the large instantaneous capacitor current at phase transitions. As can be seen in Fig. 2.5, when two capacitors C_1 and C_2 with different initial voltages are connected in parallel by closing switch S_1, the initial voltage mismatch between the two capacitors ΔV_0 can only be present across the small series resistance R_{esr} in the circuit, assuming the parasitic inductance is negligible. This will result in an exponentially decaying charging current with a high initial value of $I_0 = \frac{\Delta V_0}{R_{\text{esr}}}$,

and R_{esr} will dissipate a power of

$$\begin{aligned} P_{\text{loss}} &= \frac{1}{T}\int_0^T R_{\text{esr}}(I_0 e^{\frac{-t}{\tau}})^2 dt \\ &= \frac{1}{T}\int_0^T R_{\text{esr}}(\frac{\Delta V_0}{R_{\text{esr}}} e^{\frac{-t}{\tau}})^2 dt \\ &= \frac{\Delta V_0^2}{T R_{\text{esr}}}\int_0^T e^{\frac{-2t}{\tau}} dt \end{aligned} \tag{2.1}$$

where τ is the RC time constant of the equivalent circuit. Assuming $C_1 = C_2 = C$, then $\tau = \frac{R_{\text{esr}}C}{2}$. Provided that the switching period T is sufficiently long compared to τ (i.e. in SSL region of operation), (2.1) can be simplified to

$$P_{\text{loss}} = \frac{1}{4} C \Delta V_0^2 f_{\text{sw}} \tag{2.2}$$

where $f_{\text{sw}} = \frac{1}{T}$ is the switching frequency of switch S_1. It can be seen that this power loss is independent of the magnitude of R_{esr}, indicating that reducing the switch on-resistance cannot improve the efficiency when the SC converter is operating in the SSL region.

Since the initial difference in capacitor voltages in one switching cycle is due to the charge transfer ΔQ_0 in the previous cycle, which is further proportional to the output current I_{out}, we can get

$$\Delta V_0 = \frac{\Delta Q_0}{C} = \frac{k_c I_{\text{out}}}{f_{\text{sw}} C} \tag{2.3}$$

where k_c is a topology-dependent constant. Now we find that the power loss in (2.2) is proportional to

$$P_{\text{loss}} \propto \frac{1}{f_{\text{sw}}}, \frac{1}{C}, I_{\text{out}}^2. \tag{2.4}$$

One straightforward way to reduce ΔV_0 and thereby the P_{loss} in SSL is to increase the switching frequency. However, it is often not favorable to do so, since the transistor switching losses, as well as the bottom plate capacitance losses in integrated SC converters, increase proportionally with respect to the switching frequency. Alternatively, ΔV_0 can be reduced by increasing the flying capacitance C, so that the SC converter can enter FSL at a lower switching frequency. But this method will reduce the energy utilization factor of the capacitor and lead to a larger converter size/volume. In summary, capacitor charge sharing loss undermines the energy density advantage of capacitors, resulting in an unavoidable trade-off between achievable efficiency and capacitor size. More discussion about the capacitor energy utilization factor is presented in Chapter 3.

In-between the FSL and the SSL, the output impedance can be approximated by the geometric mean of SSL impedance and FSL impedance [7], or obtained analytically [14], [15].

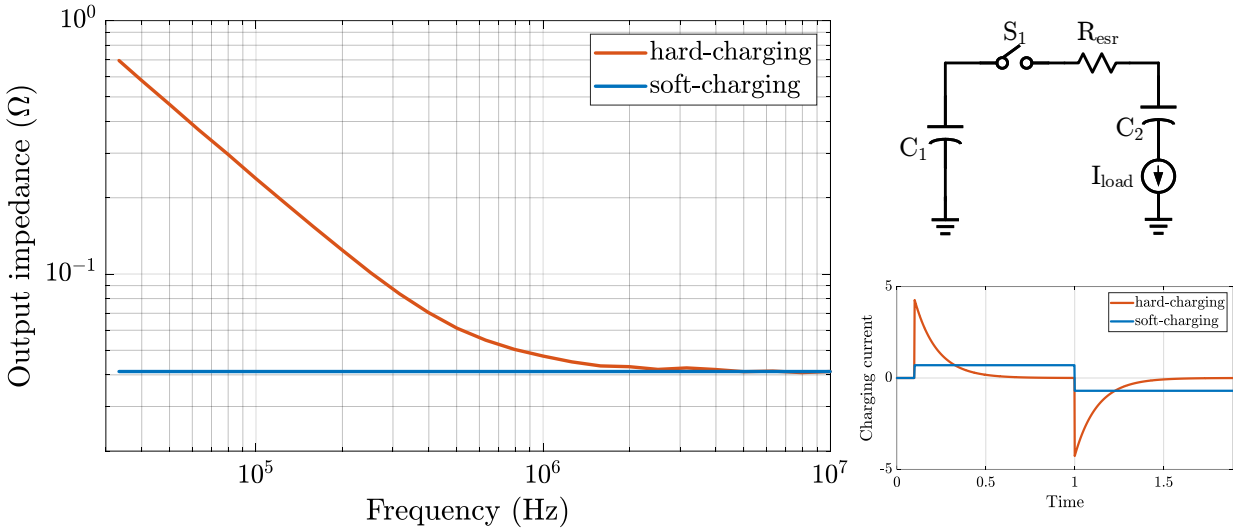


Figure 2.6: Soft-charging operation with ideal current load.

2.2 Soft-Charging Operation

The pioneering concept of soft-charging operation was first proposed in [16]. It is a technique that can greatly improve the efficiency and power density of SC converters, by eliminating the capacitor charge sharing loss. An idealized version of soft-charging operation is illustrated in Fig. 2.6. By inserting a controlled current load into the capacitor charging/discharging path, the majority of voltage mismatch between the flying capacitors and input/output voltage sources will be across the current load, instead of across the series resistance in the circuit as in the pure SC case. As shown in Fig. 2.6, given same amount of transferred charge per switching cycle, the constant soft-charging current has a much lower peak and rms values than the impulse current in the hard-charging case. As a result, the power loss is greatly reduced to $P_{\text{loss}} = I_{\text{load}}^2 R_{\text{esr}}$, and is no longer dependent on the switching frequency and the flying capacitance.

It means that with a controlled current load, the SC converter can approach its FSL performance limit at a much lower frequency. Consequently, the switching loss is reduced compared to a pure SC converter operating in FSL region. Moreover, the capacitors can have larger voltage ripples without sacrificing efficiency. This allows for the use of smaller capacitance with a significantly improved energy utilization factor.

In practice, the majority of loads are voltage-source loads or current-source loads with large decoupling capacitors. An inductive element whose terminal voltage can change instantaneously is needed to interface the SC stage and the voltage-source load. Typically, this can be satisfied by a buck converter [16]–[18] or an inductor [13], [19], [20]. Since a

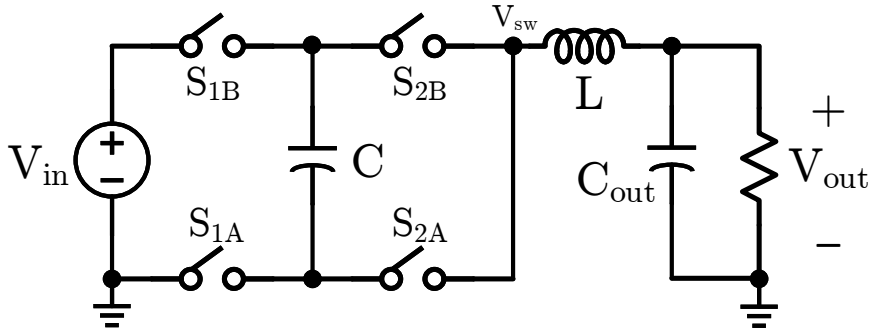
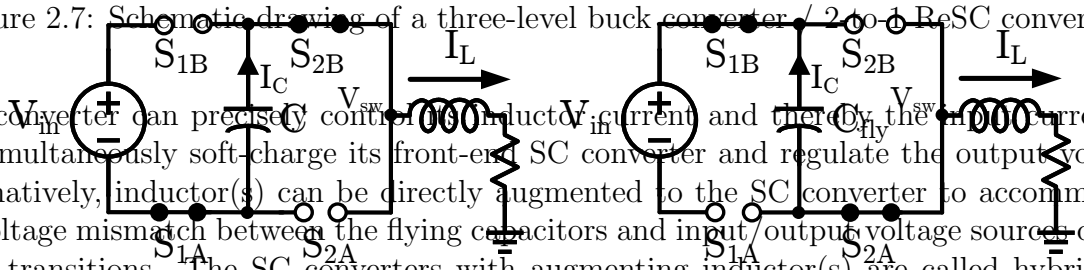


Figure 2.7: Schematic drawing of a three-level buck converter / 2-to-1 ReSC converter.



buck converter can precisely control the inductor current and thereby the input current, it can simultaneously soft-charge its front-end SC converter and regulate the output voltage. Alternatively, inductor(s) can be directly augmented to the SC converter to accommodate the voltage mismatch between the flying capacitors and input/output voltage sources during phase transitions. The SC converters with augmenting inductor(s) are called hybrid and resonant SC converters. As the name implies, the augmenting inductor(s) can facilitate soft-charging in different operation modes. In the next section, the two major operation modes for soft-charging are discussed. In Section 2.4, different inductor augmenting strategies along with their pros and cons are presented.

2.3 PWM Regulated Mode vs. Fixed-Ratio Mode

The schematic drawing of a basic 2-to-1 SC converter with an augmenting inductor at the output node is shown in Fig. 2.7. Depending on the design and operating parameters, it can be viewed as two different converters:

1. Three-level buck converter: a hybrid SC converter with regulation capability.

2. 2-to-1 ReSC converter: a resonant SC converter with fixed conversion ratio.

A three-level buck converter is a hybrid version of buck converter with enhanced performance. It can achieve output voltage regulation through PWM duty cycle control. Even though it uses four switches rather than two switches as in a buck converter, the total switch VA rating remains the same, as the switches are rated at $\frac{V_{\text{in}}}{2}$ only. The high-side switches $\text{S}_{1\text{B}}$ and $\text{S}_{2\text{B}}$ have the same duty ratio and there is a 180° phase-shift between them. The low-side switches $\text{S}_{1\text{A}}$ and $\text{S}_{2\text{A}}$ operate complementarily to $\text{S}_{1\text{B}}$ and $\text{S}_{2\text{B}}$, respectively. In addition to the two voltage levels (V_{in} and ground) in a buck converter, the flying capacitor creates a third voltage level at $\frac{V_{\text{in}}}{2}$, giving rise to the name of the "three-level buck converter". Fig. 2.8

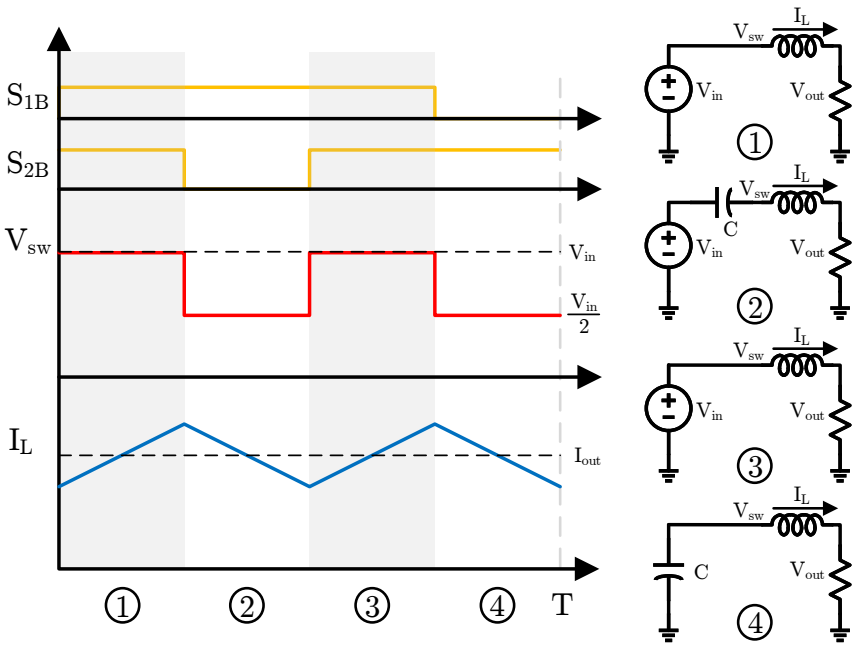


Figure 2.8: Key operating waveforms and circuit states of a three-level buck converter at duty ratio > 0.5.

illustrates the switch node voltage, inductor current, and the associated equivalent circuits for duty ratios greater than 0.5. It can be seen that the inductor sees reduced voltage (between V_{in} and $\frac{V_{\text{in}}}{2}$), at doubled switching frequency. This can reduce the inductor volume by up to 4x as compared to a buck converter with the same switching frequency and power rating. In addition, the inductor is always present in the charging/discharging path of the flying capacitor, and thereby eliminates the capacitor charge sharing loss. Note that in this PWM regulated mode, the inductor sees a staircase voltage and its current is piece-wise linear. The operating principle and the characteristics of a generalized N-level flying capacitor multilevel converter is given in Chapter 5.

A 2-to-1 resonant switched-capacitor (ReSC) converter can be viewed as a special case of the three-level buck covnerter, with the duty ratio fixed at 0.5. Its operating waveforms and equivalent circuits are shown in Fig. 2.9. Since the switch node voltage V_{sw} is always equal to the output voltage at $\frac{1}{2}V_{\text{in}}$, there is no voltage across the inductor except the flying capacitor ripple voltage. Therefore, a very tiny inductor (on the order of nH) can be selected. By tuning the switching frequency to the resonant frequency of the flying capacitor C and the output inductor L ($f_{\text{sw}} = \frac{1}{2\pi\sqrt{LC}}$), the flying capacitor will be charged/discharged in a resonant fashion. For fixed flying capacitance and inductance, this condition corresponds to the minimum operating frequency that allows for full soft-charging [13]. Moreover, thanks to

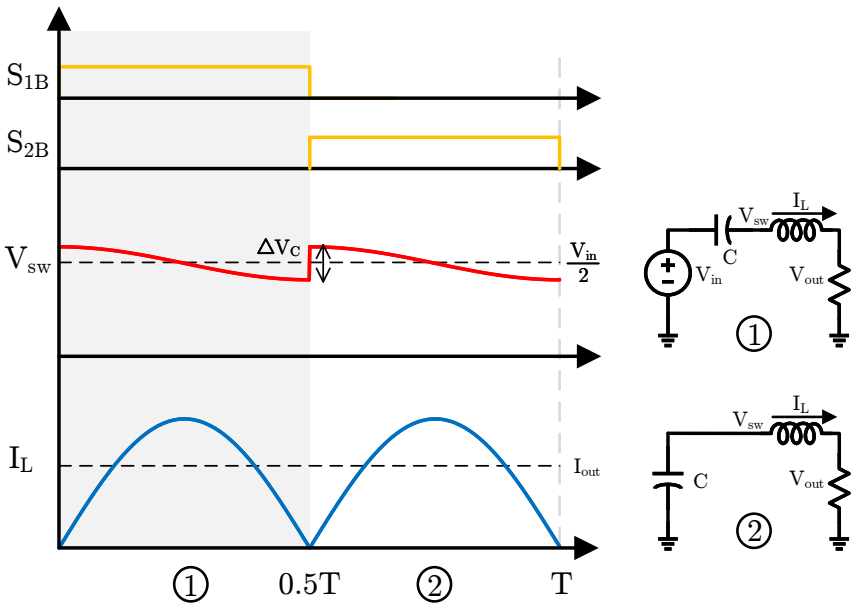
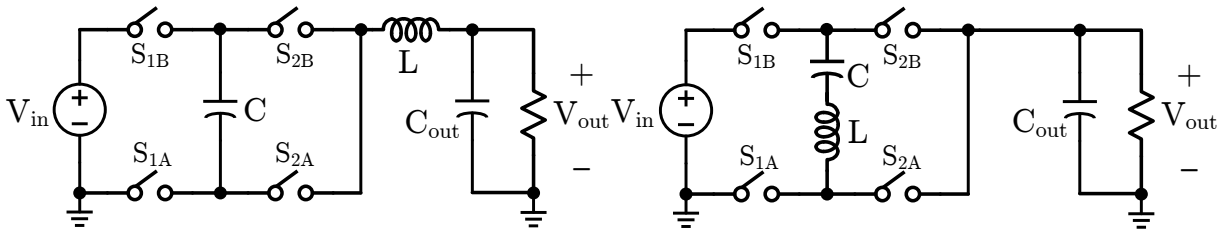


Figure 2.9: Key operating waveforms and circuit states of a 2-to-1 resonant SC converter.

the resonant operation, zero-current switching (ZCS) is naturally achieved and the overlap switching loss caused by the simultaneous existence of switch voltage and current during switching transitions is minimized. As will be discussed in Chapter 6, by tuning the LC tank to be slightly inductive, zero-voltage switching (ZVS) is achievable, eliminating the switch output capacitance loss. Owing to the soft-switching feature, as well as the very small size of the resonant inductor and the resultant low magnetic loss, a 2-to-1 ReSC converter can achieve even higher efficiency and power density than a three-level buck converter. However, this comes at the cost of losing regulation capability, since the small resonant inductor is incapable of handling the required voltage-seconds when the duty ratio deviates from 0.5. Therefore, fixed-ratio resonant SC converters are mainly used as high-efficiency, high-power-density DC transformers. Table 2.1 summarizes and compares the key characteristics of three-level buck converters and 2-to-1 ReSC converters.

The above example is based on a basic 2-to-1 SC converter. In order to determine if an arbitrary SC topology is able to take full advantage of the soft-charging operation with a single inductor at output, a generalized analysis framework is presented in [19]. For topologies that cannot achieve full soft-charging due to the violation of KVL during phase transitions at the internal voltage nodes, a split-phase control technique can be applied [21].

	Three-level Buck	2-to-1 Resonant SC
Soft-charging	Triangular current	Sinusoidal current
Duty ratio	Adjustable	50%
Regulation	Duty cycle control	2:1 fixed ratio
Required inductance	Low	Very low
Soft-switching	Quasi-Square-Wave	ZCS, ZVS
Efficiency	High	Very high
Power density	High	Very high
Substitute	Buck	DC Transformer



(a) Inductor at output (b) Inductor in series with the flying capacitor

Figure 2.10: 2-to-1 SC converter with different augmenting inductor locations.

2.4 Inductor Placement Strategy

In general, there are two ways to augment SC converters with inductor(s). One is placing the inductor at the output node as in the examples shown in Section 2.3. The other is placing the inductor(s) in series with the flying capacitor(s). These two methods are illustrated in Fig. 2.10 with a 2-to-1 SC converter as the base topology.

Under the assumption of fixed-ratio operation with 50% duty ratio, the converters' output impedances are simulated and plotted in Fig. 2.11. The inductor currents at different operating frequencies are shown in Fig. 2.12. It can be seen that, while the two strategies have similar behaviors for switching frequencies lower than the resonant frequency $f_{\text{crit}} = \frac{1}{2\pi\sqrt{LC}}$, the output impedance of the "inductor in series with capacitor" configuration increases

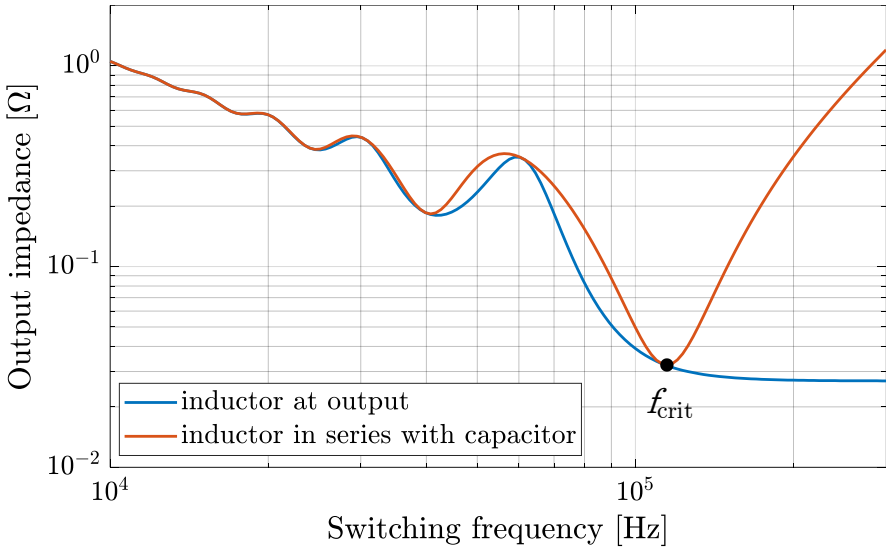
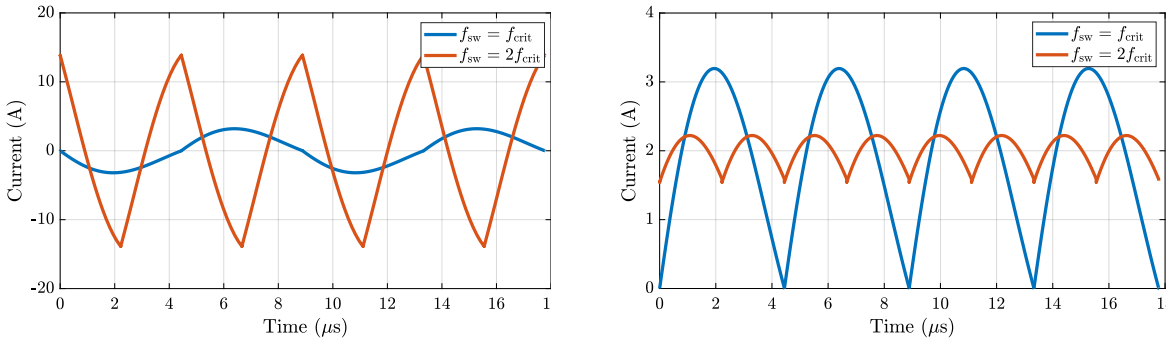


Figure 2.11: Output impedance with respect to inductor location.



(a) Inductor in series with the flying capacitor

(b) Inductor at output

Figure 2.12: Inductor current at different locations and frequencies.

sharply when the frequency is higher than f_{crit}. This is due to the fact that the LC tank becomes inductive with both positive and negative current within one switching state, resulting in large circulating current and associated power loss. Therefore, the most viable way to operate such a converter is at the resonant frequency f_{crit}. This requires precise tuning of the inductance and capacitance with very tight tolerance. Class-I multilayer ceramic capacitors (MLCCs) are usually needed for their stable performance over temperature, dc-bias, and aging. However, they are usually less energy dense and more expensive than Class-II MLCCs. The resonant inductors should also go through careful factory measurement and calibration to ensure low variations from nominal values. Recently, a lock-in controller IC has been designed to optimize the performance of such resonant SC converters, by automatically

detecting the resonance point and adjusting the switching frequency intelligently [22].

In comparison, the "inductor at output" configuration enters the fast switching limit (FSL) region for $f_{\text{sw}} > f_{\text{crit}}$, with a fixed output impedance that is slightly smaller than that at the resonant frequency. This is because the inductor filtering effect leads to a smoother current waveform, which has a smaller RMS value than that of the sinusoidal current in resonant operation. As a result, it is viable to operate the "inductor at output" resonant SC converters at $f_{\text{sw}} \geqslant f_{\text{crit}}$. This allows for more relaxed component tolerance compared to the "inductor in series of capacitor" configuration, as no precise LC tank tuning is needed and high energy density Class-II MLCCs can be used, despite their dc-bias and temperature-varying characteristics.

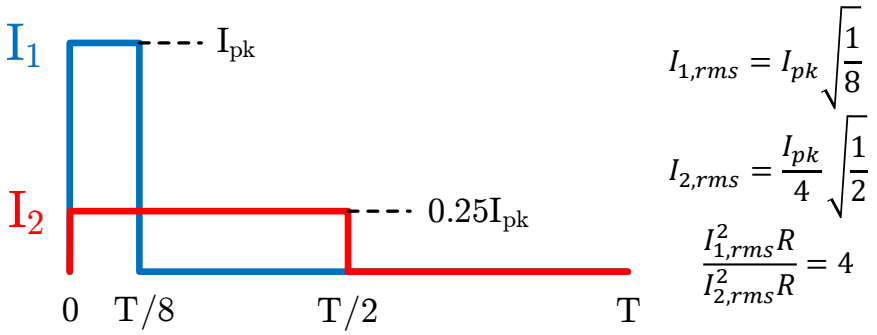
However, the "inductor at output" configuration also has limitations. Firstly, it is only applicable to selective topologies [13], whereas the "inductor in series with capacitor" can be applied to all SC topologies. It should be noted that the switched-tank converter [23] can also be viewed as a type of "inductor in series with capacitor" converter. Even though it is composed of a Dickson converter with augmenting inductors added to every other flying capacitor, LC tanks are present in all current branches. The topology therefore shares the characteristics of the "inductor in series with capacitor" configuration.

Secondly, in the "inductor at output" configuration, the switches will see the flying capacitor ripple voltage on top of their nominal blocking voltage. This could result in limited allowable voltage ripple on flying capacitors in practical implementations, even though soft-charging theoretically permits unconstrained capacitor ripple without an efficiency penalty. In contrast, in the "inductor in series with capacitor" converters, the inductors always shield switches from the capacitor voltage ripples, and thus the theoretical switch voltage rating is always the nominal voltage. Consequently, the capacitors are allowed to have a large ripple without increasing the switch stress, thus compensating for the need of relatively low energy density Class-I MLCCs.

Thirdly, the duty ratio of certain "inductor at output" converters may deviate from 50% and lead to increased switch RMS current and power loss. As discussed in [24], [25], in order to maintain capacitor charge balance, when augmenting a single inductor to the output node of a N-to-1 series-parallel converter, the duty ratio of the series-phase and the parallel-phase need to be adjusted to $\frac{1}{N}$ and $\frac{N-1}{N}$, respectively. In contrast, if distributed inductors are inserted in series with every flying capacitor, the duty ratio of all switches remain at 50%. This also applies to other topologies, such as the Fibonacci converter and the multi-resonant SC converters presented in Chapter 7. To illustrate the effect of duty ratio on RMS current and power loss, Fig. 2.13 compares the current of two switches that have the same switching period, the same amount of transferred charge, but different duty ratio. Assuming a constant capacitor current I_{pk}, the rms value can be calculated as:

$$I_{rms} = I_{pk}\sqrt{D}. \tag{2.5}$$

It can be seen that the switch with $D = \frac{1}{8}$ has twice the rms current and therefore four times the loss in comparison to the one with $D = \frac{1}{2}$, even though they have the same average



$$I_{1,rms} = I_{pk}\sqrt{\frac{1}{8}}$$

$$I_{2,rms} = \frac{I_{pk}}{4}\sqrt{\frac{1}{2}}$$

$$\frac{I_{1,rms}^2 R}{I_{2,rms}^2 R} = 4$$

Figure 2.13: Effect of duty ratio on rms current and output impedance.

	Inductor at output	**Inductor in series with capacitor**
Operating frequency	$f_{sw} \geq f_{crit}$	$f_{sw} = f_{crit}$
Tolerance to component mismatch	Relatively good tolerance	Precise matching required
Duty ratio	Dependent on capacitor charge balance	50%
Output impedance	Increase when duty ratio deviates from 50%	Lowest possible
Applicability	Selective topologies	All topologies
Switch ratings	Switch sees capacitor voltage ripple	Capacitor voltage ripple shielded by inductor
Soft switching	Achievable	Achievable
Regulation capability	Regulation possible	Regulation possible

current. This may put the "inductor at output" resonant SC converters in a less favored position in comparison to the "inductor in series with flying capacitor" converters at high conversion ratios, when the switch area cannot be optimized accordingly. This is particularly a challenge for discrete implementations.

Lastly, regulation is achievable with both inductor augmenting strategies. For the "inductor at output" configuration, duty cycle control can be used as in the three-level buck converter. Phase-shift control or frequency control can also be used for the "inductor in series with capacitor" resonant SC converters [26]–[28], similar to dual-active-bridge converters and series-resonant converters. However, the regulation capability comes at a cost in terms of efficiency and power density, as the inductor size needs to be scaled up compared to the value required in the fixed-ratio resonant operation.

Chapter 3

Modeling and Comparison of Passive Component Volume

The added inductor(s) in hybrid and resonant switched-capacitor (SC) converters offer an additional degree of freedom in the design space, and it is of great interest to understand the trade-offs between capacitor and inductor size and volume allocation. In this chapter, we analyze the reactive power processed by the passive components and use it to calculate the total passive component volume. It is shown that the total passive component volume of resonant SC (ReSC) converters can be expressed as a function of flying capacitor voltage ripple, and the optimized capacitor voltage ripple that minimizes the total volume is dependent on topology specific parameters and the relative energy density ratio between the capacitor(s) and inductor(s). Moreover, we also demonstrate through theoretical analysis and experimentation that ReSC converters use significantly less passive component volume than conventional SC and buck converters for the same amount of power converted. Next, to compare different ReSC topologies, a normalized passive volume parameter is proposed for simple and fair comparison. This can be used along with a normalized switch stress parameter (based on switch VA ratings) to create a framework to showcase the relative performance of different topologies. This framework can be used to visualize and compare the passive and active component utilizations among different topologies. Additionally, the proposed reactive power analysis is extended to hybrid converters with regulation capability.

3.1 Background and Motivation

As discussed in Chapter 2, the augmenting inductor(s) can eliminate the capacitor charge sharing loss present in pure SC converters through soft-charging operation [16], [17], [19], thereby allowing larger capacitor voltage ripple and better capacitor energy utilization. However, depending on the relative energy density of the inductors and capacitors, it is unclear whether the capacitor volume reduction could offset the volume of the augmenting inductor and lead to a smaller overall volume than that of a pure SC converter. Moreover, as the

augmenting inductors offer an additional degree of freedom in the design space, it is crucial to evaluate and find the optimum inductor and capacitor allocation that minimizes the total passive component volume.

Besides optimizing a specific ReSC converter, it is also of great interest to compare the performance of different ReSC topologies. When developing analytical models for topology comparison, a dilemma often faced is the trade-off between complexity and accuracy. To get tractable expressions with moderately good accuracy, a common and reasonable assumption for ReSC converters made by [29], [30] is that the losses are mainly contributed by the semiconductor switches while the volume is solely determined by the passive components. Here, the losses of the passive components are assumed to be comparable among different topologies and could be cautiously omitted during comparison. This is because most existing high performance ReSC converters operate at a relatively low switching frequency (e.g., less than 500 kHz) and the resonant inductors typically have low inductance value (e.g., less than 200 nH) and see the capacitor ripple voltage only, so the ac-related losses of the inductors are relatively small. On the other hand, the DCR loss of the inductors is more dependent on the rating of the output current and should be comparable among topologies. Thus, under these assumptions, if a single overall performance figure-of-merit, – including both volume and efficiency, is not the desired metric, the passive component volume and the semiconductor loss comparisons can be decoupled.

In this Chapter, we strive to gain a better understanding of these questions from the perspective of the fundamental reactive energy/power processed by the passive components. In Section 3.2, we showcase that the total passive component volume of ReSC converters can be ultimately expressed and optimized as a function of flying capacitor voltage ripple. The minimized total volume is only dependent on topology specific parameters and the relative energy density between capacitor and inductor. Following this, a number of observations and design guidelines are derived in Section 3.3 to facilitate practical ReSC converter designs. Additionally, a hardware prototype is built to experimentally demonstrate that ReSC converters use significantly less passive volume than conventional SC and buck converters for the same amount of power converted, while maintaining the best efficiency performance. In Section 3.4, we generalize the proposed reactive power analysis to provide direct passive volume comparison among different ReSC topologies. Combining this with the classical switch total VA rating metric, which reflects potential efficiency, we provide a simple yet powerful framework to evaluate the relative performance (in terms of active and passive component utilization) of different ReSC topologies. Moreover, the theoretical lower-bound limits of passive and active components are derived to identify the framework boundaries such that any new emerging topologies can be analyzed and incorporated into the comparison space. In Section 3.5, with the examples of three-level buck converters and series-capacitor buck converters, the proposed reactive power analysis is extended to hybrid converters with regulation capability.

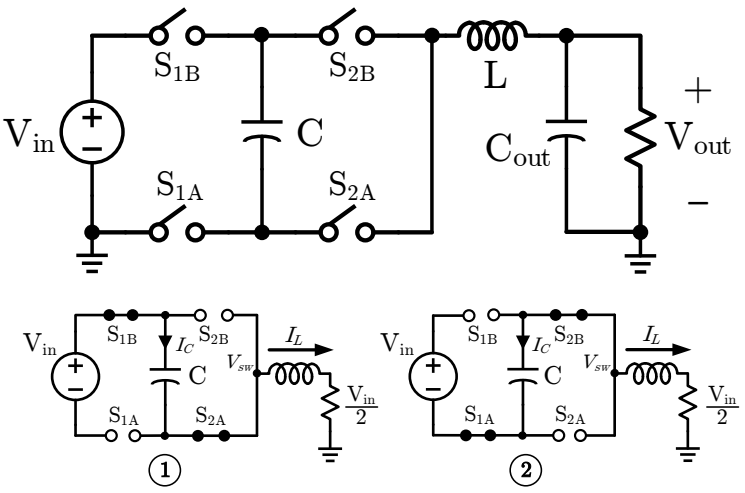


Figure 3.1: Schematic drawing of a 2-to-1 resonant switched-capacitor converter and its two operating states.

3.2 Analysis of Basic 2-to-1 Resonant Switched-Capacitor Converter

The volume of a passive component is directly related to the peak energy it can store, as well as its type and technology. In ReSC converters, the resonant inductors are able to transfer all stored energy as the sinusoidal inductor current reaches zero each switching cycle. In contrast, each flying capacitor can typically only deliver a portion of its stored energy which is determined by the magnitude of its voltage ripple on top of the dc average voltage. To calculate the total passive component volume of ReSC converters, we propose an energy-based method by fundamentally analyzing the reactive power processed by the passive components. Note that the term "reactive power" is also referred to as "indirect power" in [31]. Here, we use the basic 2-to-1 ReSC converter as an example to demonstrate the proposed method. The reactive power processed by the flying capacitor and the resonant inductor is first calculated. Then, this processed power is related to the required stored energy through an energy utilization factor. Finally, the passive component volume is derived by dividing the required stored energy by the energy density of the corresponding passive components. It will be shown that the total passive volume can be expressed and subsequently optimized as a function of the flying capacitor voltage ripple ratio.

The schematic drawing of a 2-to-1 ReSC converter and its two operating states are shown in Fig. 3.1. All switches have a fixed duty ratio of 50%, and there is a 180° phase shift between the "A" switches and the "B" switches. The switching frequency is the resonant frequency of the flying capacitor and the inductor ($f_{\text{sw}} = \frac{\omega_r}{2\pi} = \frac{1}{2\pi\sqrt{LC}}$), as it is the minimum

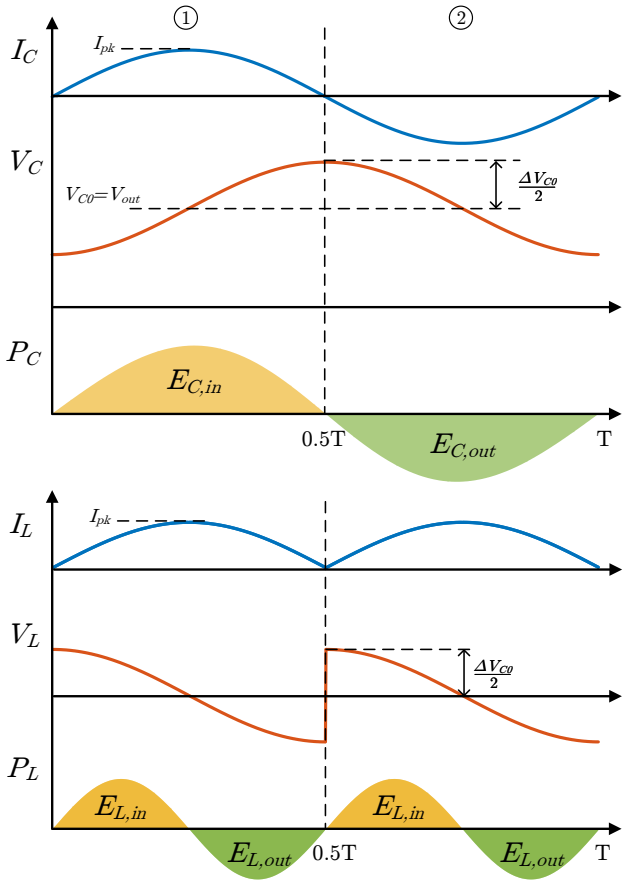


Figure 3.2: Current, voltage, and power waveforms of the flying capacitor and the resonant inductor in a 2-to-1 ReSC converter.

frequency with full soft-charging for hybrid SC converters [19]. As shown in Fig. 3.2, the flying capacitor has a sinusoidal current $I_C = I_{pk}sin(\omega_r t)$, and the corresponding capacitor voltage has a dc component of $V_{C0} = V_{\text{out}}$ and an ac component of $-\frac{I_{pk}}{C\omega_r}cos(\omega_r t)$, with a peak-to-peak ripple voltage of $\Delta V_{C0} = \frac{2I_{pk}}{C\omega_r}$. In contrast, the inductor current is a rectified sine wave with the same amplitude as that of the capacitor current, and the voltage across the inductor has the same peak magnitude as the capacitor voltage ripple, but at twice the frequency. By multiplying the current and the voltage waveforms, the instantaneous power processed by the capacitor $V_C(t)I_C(t)$ and the inductor $V_L(t)I_L(t)$ can be derived as shown in Fig. 3.2, and the shaded areas represent the energy going into and out of the passive component in each cycle.

In periodic steady-state, the average power P_k processed by a reactive element k can be expressed in terms of the cyclically stored energy E_{in}, delivered energy E_{out} and the switching period T: $P_k = \frac{1}{T} \cdot \frac{E_{\text{in}}+E_{\text{out}}}{2} = \frac{1}{T}E_{\text{in}}$, for the assumption of lossless components. By factoring

out the operation dependent term T, this average reactive power term P_k can readily reflect the intrinsic property of the topology. The average power processed by the flying capacitor, P_{C0}, can be calculated as

$$\begin{aligned} P_{C0} &= \frac{E_{C,in}}{T} \\ &= \frac{1}{T}\int_0^{\frac{T}{2}} I_c(t)V_c(t)dt \\ &= \frac{1}{T}\int_0^{\frac{T}{2}} I_{pk}sin(\omega_r t)(V_{\text{out}} - \frac{I_{pk}}{C\omega_r}cos(\omega_r t))dt \\ &= \frac{1}{2}V_{\text{out}}I_{\text{out}} \end{aligned} \tag{3.1}$$

where $I_{\text{out}} = \frac{2}{\pi}I_{pk}$ is the average output current. Similarly, the average power of the resonant inductor is given by

$$\begin{aligned} P_{L0} &= \frac{E_{L,in}}{T} \\ &= \frac{1}{T}\int_0^{\frac{T}{4}} I_L(t)V_L(t)dt \\ &= \frac{1}{T}\int_0^{\frac{T}{4}} I_{pk}sin(\omega_r t)\frac{I_{pk}}{C\omega_r}cos(\omega_r t)dt \\ &= \frac{I_{\text{out}}^2}{32Cf_{\text{sw}}}. \end{aligned} \tag{3.2}$$

Note that the integral is from 0 to $\frac{T}{4}$ only. This is because the inductor sees doubled frequency and stores and delivers energy twice per switching cycle. Therefore, from an energy *storage* perspective, the calculation of the inductor processed power should consider one energy transfer cycle only (half of the switching cycle in this case), resulting in an integral from 0 to $\frac{T}{4}$. This deviates from the Wolaver definition on Page 63 of [32]. Wolaver focused on how much reactive energy needs to be *transferred* to the load per switching cycle, and therefore defined the reactive power processed by a reactive element k to be $P_k = \frac{1}{2}\cdot\frac{1}{T}\int_0^T \mid V_k I_k \mid dt$. This definition would lead to a result that is twice that of (3.2).

Eqn. (3.2) can be further expressed as a function of flying capacitor voltage ripple ratio. By substituting in the average-to-peak capacitor voltage ripple $\frac{1}{2}\Delta V_{C0} = \frac{I_{pk}}{C\omega_r} = \frac{I_{\text{out}}}{4Cf_{\text{sw}}}$, we get

$$P_{L0} = \frac{I_{\text{out}}\Delta V_{C0}}{16} = \frac{P_{\text{out}}}{16}\cdot\frac{\Delta V_{C0}}{V_{\text{out}}} = \frac{P_{\text{out}}}{16}\cdot\frac{\Delta V_{C0}}{V_{C0}} \tag{3.3}$$

where $V_{C0} = V_{\text{out}}$ is the dc average voltage of the flying capacitor. Now that the reactive power processed by the flying capacitor and the resonant inductor have been derived, we can next calculate the energy that needs to be stored by these passive components. For the

flying capacitor, the processed energy E_{C0} (also equals to $E_{C,\text{in}}$ and $E_{C,\text{out}}$ in Fig. 3.2) can be expressed as the average power P_{C0} divided by the switching frequency. Alternatively, it equals the difference between the peak and minimum stored energy per switching cycle:

$$\begin{aligned} E_{C0} &= \frac{P_{C0}}{f_{\text{sw}}} \\ &= \frac{1}{2}C[(V_{C0}+\frac{1}{2}\Delta V_{C0})^2-(V_{C0}-\frac{1}{2}\Delta V_{C0})^2] \\ &= CV_{C0}\Delta V_{C0}. \end{aligned} \tag{3.4}$$

Next, we define the energy utilization factor of the capacitor as the energy transferred by the capacitor per cycle divided by the peak energy stored by the capacitor:

$$\mu_C = \frac{E_{C0}}{E_{C,\text{store}}} = \frac{E_{C0}}{\frac{1}{2}C(V_{C0}+\frac{1}{2}\Delta V_{C0})^2} = \frac{2\frac{\Delta V_{C0}}{V_{C0}}}{(1+\frac{1}{2}\frac{\Delta V_{C0}}{V_{C0}})^2}. \tag{3.5}$$

For a fixed amount of processed energy, a higher μ_C indicates a lower stored energy and smaller capacitor size, and vice versa. The capacitor volume Vol_C can then be expressed with respect to the capacitor processed power as:

$$\text{Vol}_\text{C} = \frac{E_{C,\text{store}}}{\rho_{E,C}} = \frac{\frac{E_{C0}}{\mu_C}}{\rho_{E,C}} = \frac{\frac{P_{C0}}{f_{\text{sw}}\mu_C}}{\rho_{E,C}} \tag{3.6}$$

where $\rho_{E,C}$ is the energy density of the capacitor; it is physically limited by the maximum electrical field of the dielectric material.

For the resonant inductor, the sinusoidal current reaches zero every half cycle. Thus, the inductor processed energy equals the stored energy (i.e. its energy utilization factor $\mu_L = 1$) and

$$\text{Vol}_\text{L} = \frac{E_{L,\text{store}}}{\rho_{E,L}} = \frac{E_{L0}}{\rho_{E,L}} = \frac{\frac{P_{L0}}{f_{\text{sw}}}}{\rho_{E,L}}, \tag{3.7}$$

where $\rho_{E,L}$ is the energy density of the inductor; it is physically limited by the maximum flux density of the magnetic material.

Revisiting (3.1) and (3.3), it can be observed that the power processed by the capacitor is a fixed value. Moreover, it can be shown that this value is equal to the power processed by the flying capacitor in a pure 2-to-1 SC converter. Even though the augmenting inductor does not change the power/energy that is processed by the flying capacitor, it allows unconstrained capacitor voltage ripple $\frac{\Delta V_{C0}}{V_{C0}}$ without efficiency penalty through resonant soft-charging operation, and therefore improves the energy utilization factor of the flying capacitor and results in a smaller capacitor volume. However, the capacitor volume reduction comes as a cost. As shown in (3.3), the power processed by the inductor is an increasing function of $\frac{\Delta V_{C0}}{V_{C0}}$, which leads to an increase in inductor volume (3.7) when the capacitor volume is reduced. The effects of $\frac{\Delta V_{C0}}{V_{C0}}$ on capacitor volume and inductor volume are plotted in Fig. 3.3, assuming $\rho_{E,C}/\rho_{E,L} = 100$.

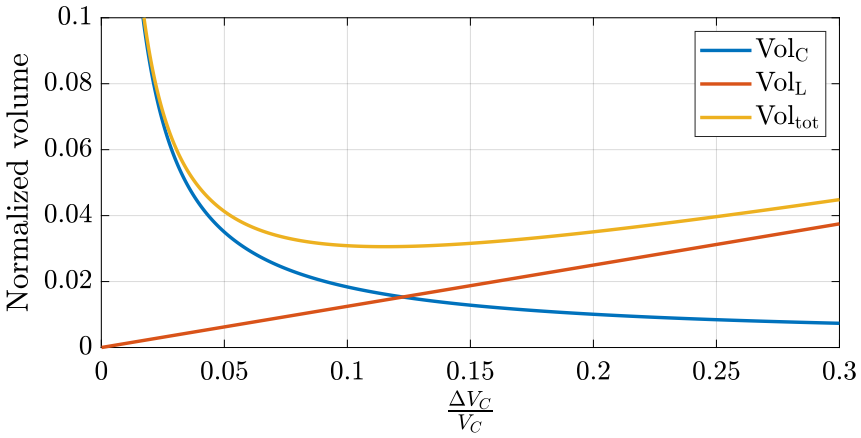


Figure 3.3: The effects of flying capacitor voltage ripple on capacitor volume, inductor volume and overall volume for a 2-to-1 ReSC converter (assuming $\rho_{E,C}/\rho_{E,L} = 100$).

The trade-off between the capacitor volume and the inductor volume can be observed more clearly from:

$$\begin{aligned} \mathrm{Vol_{tot}} &= \mathrm{Vol_C} + \mathrm{Vol_L} \\ &= \frac{P_{\mathrm{out}}}{f_{\mathrm{sw}}}\left(\frac{\frac{1}{4}\left(1 + \frac{V_{C0}}{\Delta V_{C0}} + \frac{\Delta V_{C0}}{4V_{C0}}\right)}{\rho_{E,C}} + \frac{\frac{1}{16}\frac{\Delta V_{C0}}{V_{C0}}}{\rho_{E,L}}\right) \end{aligned} \tag{3.8}$$

where $\mathrm{Vol_C}$ is primarily a function of $\frac{V_{C0}}{\Delta V_{C0}}$ whereas $\mathrm{Vol_L}$ is a function of $\frac{\Delta V_{C0}}{V_{C0}}$. For a given set of P_{out}, f_{sw}, $\rho_{E,C}$ and $\rho_{E,L}$, (3.8) can be differentiated with respect to the capacitor ripple ratio $\frac{\Delta V_{C0}}{V_{C0}}$ to find the value that minimizes the total volume:

$$\frac{d\mathrm{Vol_{tot}}}{\frac{\Delta V_{C0}}{V_{C0}}} = 0 \Longrightarrow \left(\frac{\Delta V_{C0}}{V_{C0}}\right)^* = \sqrt{\frac{4\rho_{E,L}}{\rho_{E,L} + \rho_{E,C}}} \approx 2\sqrt{\frac{\rho_{E,L}}{\rho_{E,C}}}. \tag{3.9}$$

It can be seen that $(\frac{\Delta V_{C0}}{V_{C0}})^*$ is inversely proportional to $\sqrt{\frac{\rho_{E,C}}{\rho_{E,L}}}$. When $\frac{\rho_{E,C}}{\rho_{E,L}}$ increases, $(\frac{\Delta V_{C0}}{V_{C0}})^*$ decreases, corresponding to a passive component allocation with more capacitance and less inductance.

Substituting (3.9) into (3.8), the minimized volume of a 2-to-1 ReSC converter is then given by

$$\mathrm{Vol_{tot,min}} \approx \frac{P_{\mathrm{out}}}{f_{\mathrm{sw}}\rho_{E,L}}\left(\frac{\frac{\rho_{E,L}}{\rho_{E,C}} + \sqrt{\frac{\rho_{E,L}}{\rho_{E,C}}}}{4}\right). \tag{3.10}$$

Note that the above analysis assumes that the passive components are ideal and lossless. The capacitor ESR loss and inductor dc and ac losses are not considered for the volume

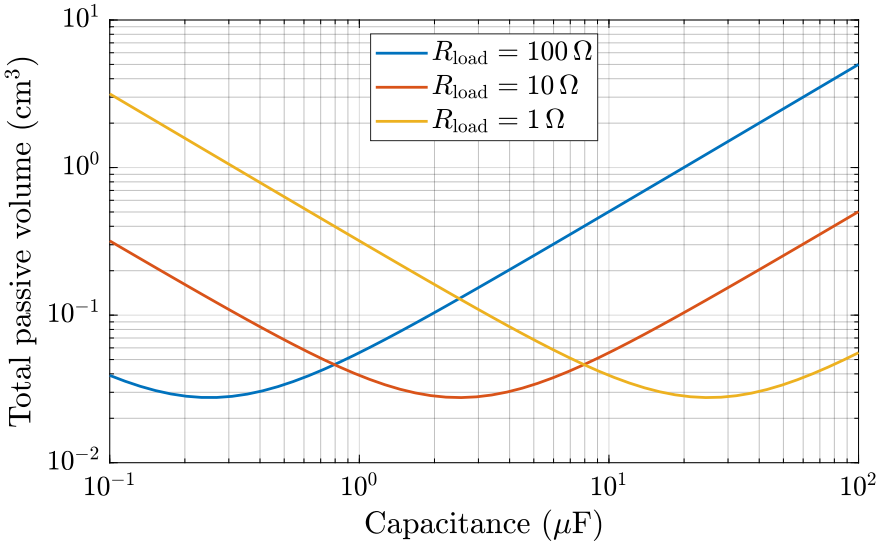


Figure 3.4: Given fixed output power and switching frequency, the 2-to-1 ReSC converter can always achieve the same minimum total passive component volume. But the optimum capacitance (and inductance) allocation depends on the magnitude of the load resistance. Parameters for the plot: $P_{\text{out}} = 100$ W, $f_{\text{sw}} = 100$ kHz, $\rho_{E,C} = 0.1$ J/cm^3, $\rho_{E,C}/\rho_{E,L} = 100$.

optimization. This is based on the fact that the capacitor ESR at the frequency range of interest can be much lower than the switch on-resistance in practical implementations, as usually multiple capacitors are placed in parallel. Similarly, the inductor DCR loss and core loss also only contribute a small portion to the overall loss, as the resonant operation leads to very small inductor volt-second and core size [33]. Therefore, the lossless assumption is applicable and enables simplification of the problem without greatly affecting the practicality of the results. In the next section, the above theoretical analysis will be used to derive guidelines for practical designs, followed by experimental verification.

3.3 Design Guidelines and Comparisons with Other Solutions

Design Guidelines

Given fixed output power and switching frequency, the total passive component volume of the 2-to-1 ReSC converter is plotted in Fig. 3.4 with respect to flying capacitance. It can be seen that, regardless of the magnitude of the load resistance R_{load}, the ReSC converter can always achieve the same minimized total passive component volume, which agrees with (3.10). The optimum flying capacitance that provides the lowest total passive volume is

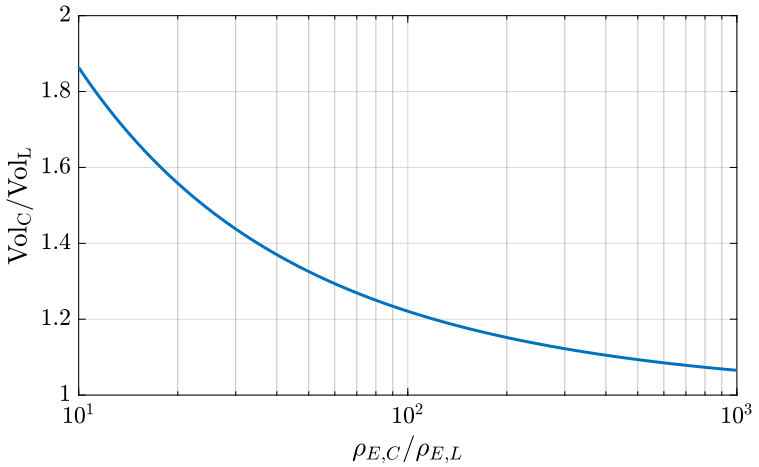


Figure 3.5: The optimum volume ratio between capacitor and inductor with respect to their energy density ratio.

inversely dependent on the load resistance. It indicates that, with fixed output power and switching frequency, higher capacitance (and lower inductance) should be used for applications with lower output voltage and higher output current. This is based on the fact that, given fixed nominal capacitance and inductance values, the capacitor volume depends on the voltage, while the inductor volume depends on the current. The capacitor and the inductor volume that give the minimized total volume can be calculated by substituting the optimized capacitor ripple ratio $(\frac{\Delta V_{C0}}{V_{C0}})^*$ of (3.9) into (3.6) and (3.7), respectively. Fig. 3.5 plots the optimized volume ratio with respect to the energy density ratio between capacitor and inductor. Within a practical range of $100 \leq \rho_{E,C}/\rho_{E,L} \leq 1000$, the optimum volume ratio is slightly greater than 1, indicating that the flying capacitor and the resonant inductor should have similar volume. Note that even though this analysis is based on the assumption of lossless passive components, the result matches with the finding in [34], where the optimized passive component allocation is derived for minimized total power loss.

Comparison with Buck Converter

Now that we have derived the minimized total passive component volume of a 2-to-1 ReSC converter, it is of great interest to compare the result with other types of converters, such as the magnetic-based converters. Since both the inductor in the buck converter and the transformer in the transformer-bridge converter have similar volt-second product requirements, the size of their respective magnetic components will be similar [35]. Here, we calculate the minimum required inductor size of a buck converter at 2-to-1 conversion ratio, with the same output power and switching frequency as that of the ReSC converter.

As derived in [32], the average power processed by the inductor is $P_{L0} = \frac{1}{2}P_{\text{out}}$, when the duty ratio D is 0.5. To maximize the inductor energy utilization factor μ_L, the buck converter should operate in boundary conduction mode so that the inductor current goes to zero every switching cycle and its energy utilization factor is maximized ($\mu_L = 1$). Then, the minimized volume of the inductor of a buck converter can be found to be

$$\text{Vol}_{\text{L,buck}} = \frac{\frac{1}{2}P_{\text{out}}}{f_{\text{sw}}\rho_{E,L}} \tag{3.11}$$

Compared to (3.8), it can be seen that the minimized total volume of the 2-to-1 ReSC converter is 1.2 times that of a 2-to-1 buck converter when $\rho_{E,C} = \rho_{E,L}$. In order for the ReSC converter to achieve a smaller volume than that of a buck converter, we need $\rho_{E,C} \gg \rho_{E,L}$. For instance, if $\rho_{E,C} = 100\rho_{E,L}$, the volume of the ReSC converter is 0.055 times that of the buck converter.

Note that this comparison is based on the assumption that all passive components in the ReSC converter and the buck converter are lossless. In practice, the buck inductor is more lossy than the LC tank of the ReSC converter as will be shown in the experimental verification section. Therefore, this ideal lossless comparison disadvantages the ReSC converter compared to the buck converter.

Comparison with Pure SC Converter

Compared to a pure SC converter, the augmenting inductor of the ReSC converter can help eliminate the capacitor charge sharing loss and therefore allow higher capacitor voltage ripple without degrading the efficiency. However, depending on the relative energy density of inductor and capacitor, it is unclear whether the capacitor volume reduction can offset the volume of the augmenting inductor and lead to a smaller overall volume than that of a pure SC converter.

Moreover, as shown in Fig. 3.4, the capacitance and inductance allocation is dependent on the load resistance. An optimum allocation tends to use more capacitance and less inductance when the load resistance decreases and output current increases. For very low-voltage high-current applications such as the latest GPU power delivery at 1 V and 1000 A [36], the optimum inductance (of each single converter in a multi-phase configuration) might still be very small, giving rise to the question of whether pure SC converters is a better choice than ReSC converters.

Here, we compare the relative passive component volume of the 2-to-1 ReSC converter and the 2-to-1 pure SC converter. It can be easily shown that the power processed by the flying capacitor of a 2-to-1 pure SC converter is the same as that in the ReSC case: $P_C = \frac{1}{2}P_{\text{out}}$. However, its minimized total passive volume cannot be derived with the same method. This is because there is no inductor to constrain its flying capacitor voltage ripple ratio $\frac{\Delta V_C}{V_C}$, and thus its energy utilization factor μ_C is unconstrained and can be as large as 1. Nevertheless, unlike the ReSC converter in which the capacitor voltage ripple and the power loss are decoupled because of soft-charging operation, the pure SC converter suffers

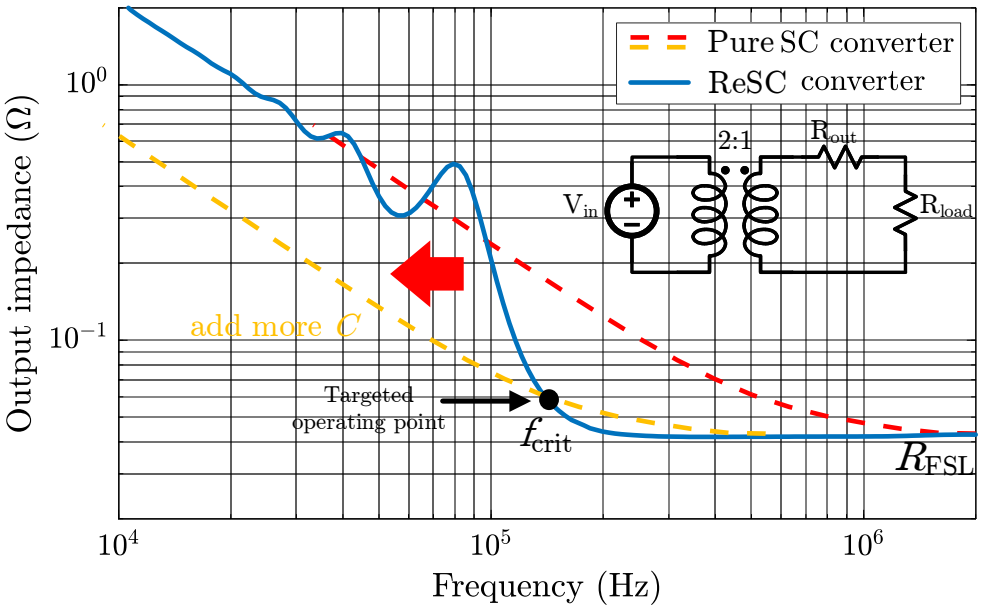


Figure 3.6: Output impedance of 2-to-1 Pure SC and ReSC converters vs. frequency.

from capacitor charge sharing loss, which is dependent on the capacitor voltage ripple ratio. Therefore, in order to have a fair volume comparison, the efficiency of the pure SC converter and the ReSC converter should be kept the same.

Switched-capacitor converters can be modeled by an ideal transformer [7]. The output impedance at the secondary side of the transformer is a good indication of the efficiency performance. In Fig. 3.6, the simulated output impedance of 2-to-1 pure SC converter and 2-to-1 ReSC converter are plotted in red and blue, respectively. They have the same switch on-resistance and flying capacitance. It can be seen that both converters approach the same lowest possible output impedance R_{FSL} at the fast switching limit (FSL) region, which is solely determined by the series resistance in the circuit (e.g., switch on-resistance, capacitor ESR) [7]. With an augmenting inductor, the ReSC converter can approach R_{FSL} at a much lower switching frequency. As derived in [14], when operating at the resonant frequency $f_{\text{crit}} = \frac{1}{2\pi\sqrt{LC}}$, the output impedance of the ReSC converter is

$$R_{\text{out,ReSC}} = \frac{\pi^2}{8} R_{\text{FSL}}. \tag{3.12}$$

In contrast, [14] also shows that the output impedance of 2-to-1 pure SC converter with respect to its switching frequency f_{sw} and flying capacitance C_p is

$$R_{\text{out,pureSC}} = \frac{coth(\frac{1}{4R_{\text{FSL}}C_p f_{\text{sw}}})}{4C_p f_{\text{sw}}}. \tag{3.13}$$

In order for the pure SC converter to have the same efficiency performance, the two converters should have the same output impedance at the same switching frequency. As illustrated in Fig. 3.6, this can be achieved by adding more capacitance to shift the impedance curve of the pure SC converter to the left. By equating (3.12) and (3.13), we get

$$C_p \approx \frac{1}{3.43 R_{\text{FSL}} f_{\text{sw}}}. \tag{3.14}$$

For the simplicity of the following derivation, the numerical constant in (3.14) is substituted with $\zeta = 3.43$:

$$C_p \approx \frac{1}{\zeta R_{\text{FSL}} f_{\text{sw}}}. \tag{3.15}$$

In order to keep the switching loss approximately the same for both converters, f_{sw} should be equal to the resonant frequency of the ReSC converter f_{crit}:

$$f_{\text{sw}} = f_{\text{crit}} = \frac{1}{2\pi\sqrt{LC}} \tag{3.16}$$

where L and C are the resonant inductance and flying capacitance of the 2-to-1 ReSC converter.

Now we calculate the volume of the 2-to-1 pure SC converter, $\text{Vol}_{\text{pureSC}}$, based on its peak stored energy and the energy density of the capacitor, $\rho_{E,C}$:

$$\text{Vol}_{\text{pureSC}} = \frac{\frac{1}{2} C_p (V_o + \frac{1}{2}\Delta V_o)^2}{\rho_{E,C}}. \tag{3.17}$$

Its peak-to-peak capacitor voltage ripple ΔV_o can be expressed as

$$\Delta V_o = \frac{\Delta q_{\text{in}}}{C_p} = \frac{I_{\text{in}} T}{C_p} = \frac{\frac{P_{\text{out}}}{2V_o} T}{C_p} = \frac{P_{\text{out}}}{2 f_{\text{sw}} V_o C_p}. \tag{3.18}$$

By substituting (3.15) and (3.18) into (3.17), we get

$$\text{Vol}_{\text{pureSC}} = \frac{(V_o + \frac{\zeta P_{\text{out}} R_{\text{FSL}}}{4V_o})^2}{2\zeta \rho_{E,C} f_{\text{sw}} R_{\text{FSL}}}. \tag{3.19}$$

Next, dividing (3.19) by (3.10) yields the relative volume ratio:

$$\frac{\text{Vol}_{\text{pureSC}}}{\text{Vol}_{\text{ReSC}}} = \frac{(4 + \frac{\zeta R_{\text{FSL}}}{R_{\text{load}}})^2}{8\zeta \frac{R_{\text{FSL}}}{R_{\text{load}}} (1 + \sqrt{\frac{\rho_{E,C}}{\rho_{E,L}}})} \tag{3.20}$$

where $R_{\text{load}} = \frac{V_o^2}{P_{\text{out}}}$ is the output load resistance. It can be seen that the relative volume ratio is dependent on not only the energy density ratio of capacitor and inductor $\sqrt{\frac{\rho_{E,C}}{\rho_{E,L}}}$, but also

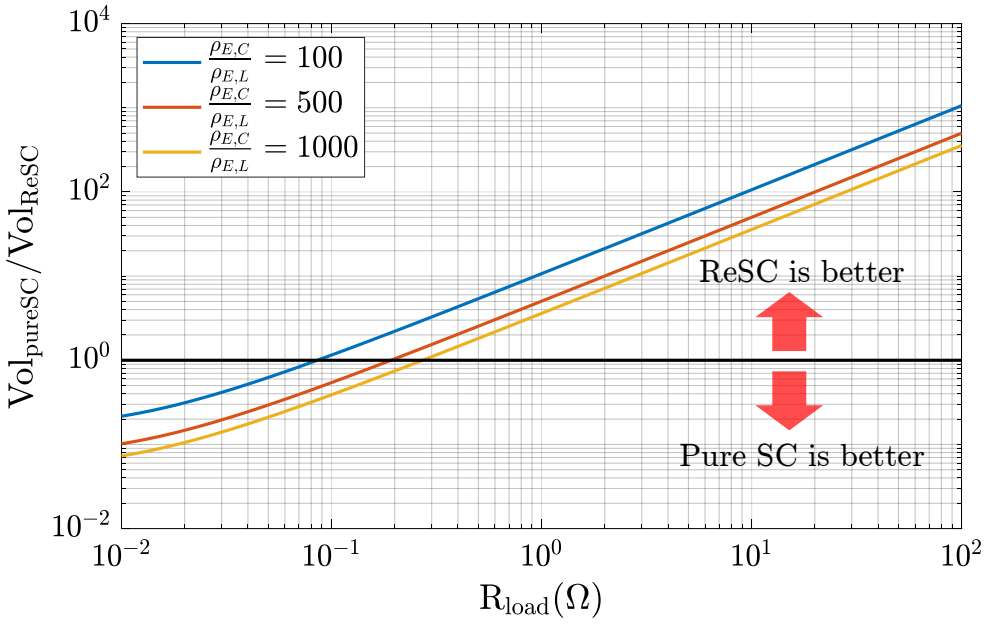


Figure 3.7: Relative passive component volume comparison between 2-to-1 pure SC converter and 2-to-1 ReSC converter (assuming converter series resistance $R_{\mathrm{FSL}} = 5$ mΩ).

the ratio of the converter's series resistance and the load resistance $\frac{R_{\mathrm{FSL}}}{R_{\mathrm{load}}}$. Assuming both converters have a total series resistance R_{FSL} of 5 mΩ, we plot the relative volume ratio as a function of R_{load} as shown in Fig. 3.7. Taking the $\frac{\rho_{E,C}}{\rho_{E,L}} = 100$ case as an example, with the same efficiency performance, the 2-to-1 ReSC converter can achieve smaller total passive component volume when R_{load} is greater than 85 mΩ, otherwise the 2-to-1 pure SC converter is more favorable. If $\frac{\rho_{E,C}}{\rho_{E,L}} = 1000$, the boundary R_{load} increases to 270 mΩ, making the pure SC approach attractive for a broader load range.

Alternatively, we can express the relative volume ratio with respect to converter efficiency. Based on the ideal transformer model [7], the efficiency of SC converters is given by

$$\eta = \frac{R_{\mathrm{load}}}{R_{\mathrm{out}} + R_{\mathrm{load}}}. \tag{3.21}$$

As shown in (3.12), $R_{\mathrm{out}} = \frac{\pi^2}{8} R_{\mathrm{FSL}}$ at the desired resonant operating point and therefore

$$\eta = \frac{R_{\mathrm{load}}}{\frac{\pi^2}{8} R_{\mathrm{FSL}} + R_{\mathrm{load}}}. \tag{3.22}$$

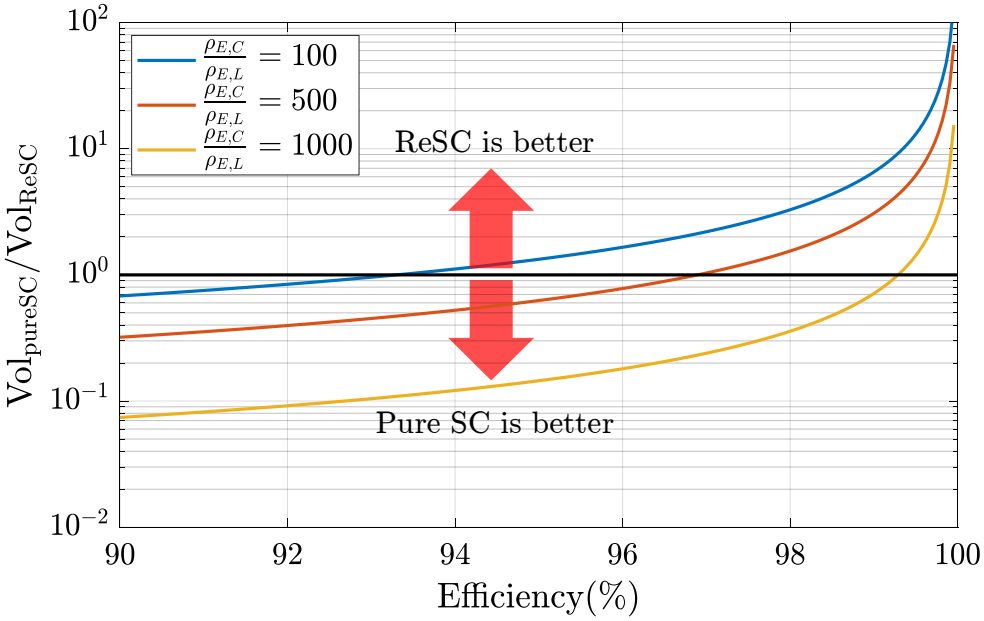


Figure 3.8: Relative passive component volume comparison between 2-to-1 pure SC converter and 2-to-1 ReSC converter with respect to converter efficiency.

Thus, $\frac{R_{\mathrm{FSL}}}{R_{\mathrm{load}}}$ can be written as $\frac{R_{\mathrm{FSL}}}{R_{\mathrm{load}}} = \frac{8}{\pi^2}(\frac{1}{\eta} - 1)$ and (3.20) is equivalent to

$$\frac{\mathrm{Vol}_{\mathrm{pureSC}}}{\mathrm{Vol}_{\mathrm{ReSC}}} = \frac{(4 + \frac{8\zeta}{\pi^2}(\frac{1}{\eta} - 1))^2}{\frac{64\zeta}{\pi^2}(\frac{1}{\eta} - 1)(1 + \sqrt{\frac{\rho_{E,C}}{\rho_{E,L}}})}. \tag{3.23}$$

This way, we are able to directly observe the trade-off between efficiency and passive component volume of different approaches as plotted in Fig. 3.8. For a practical value of $\frac{\rho_{E,C}}{\rho_{E,L}} = 100$, the 2-to-1 ReSC converter can have smaller volume than the pure SC case when the designed efficiency is greater than 93.3%. However, for very low-voltage high-current applications, such efficiency number might be unreachable due to the limits of $\frac{R_{\mathrm{FSL}}}{R_{\mathrm{load}}}$ and pure SC converters could be a better choice.

Note that this analysis assumes the ReSC converter and the pure SC converter have the same series resistance, including switch on-resistance and capacitor ESR. In practice, the capacitor ESR will be slightly higher for the ReSC converter as it uses less capacitors in parallel. In addition, the loss of the resonant inductor, which is mainly dominated by the DCR loss, is also not considered here. If a more precise comparison is desired, the inductor DCR should be incorporated into the total series resistance R_{FSL} for the ReSC converter. Then, instead of directly equating (3.12) and (3.13) to get (3.14), (3.12) should first be scaled

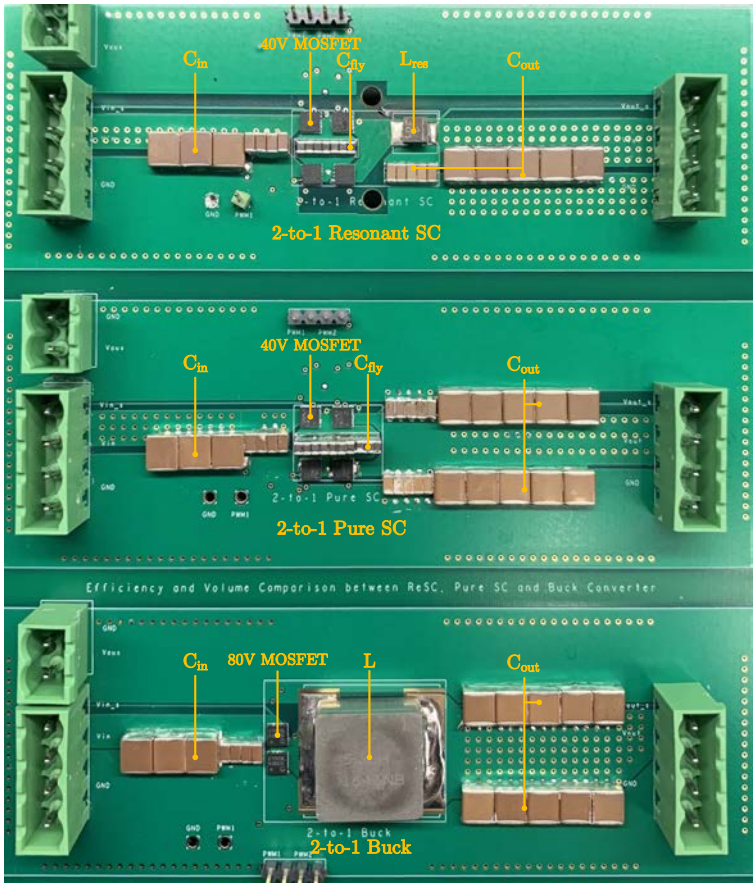


Figure 3.9: Photograph of the hardware prototype for passive component volume and efficiency comparisons.

to take inductor DCR into consideration. This will slightly shift the curves in Fig. 3.7 and 3.8 to the right side, but will not alter the major trend qualitatively.

Experimental Verification

Three hardware prototypes are designed to verify the above passive volume analysis and comparisons. As can be seen from Fig. 3.9, there are three 2-to-1 converters on the board, including an ReSC converter, a pure SC converter and a buck converter. They share the same operating parameters as shown in Table 3.1. Since the efficiency analysis of SC converters in the last subsection mainly considers conduction loss, a relatively low switching frequency of 100 kHz and a high output current of 15 A are selected here to make sure the converters operate at heavy-load region and are conduction-loss dominated.

The major active and passive components of the converters are highlighted in Fig. 3.9, and

Table 3.1: Key converter operating parameters

Input voltage	48 V
Output voltage	24 V
Output current	15 A
Power rating	360 W
Switching frequency	100 kHz

their parameters are tabulated in Table 3.2. Sufficient filtering capacitance is used to ensure negligible input and output voltage ripples, so that their effects on efficiency performance is minimized. For the ReSC converter, given a desired resonant frequency of 100 kHz, the resonant inductor and capacitor are selected as follows. First, the inductor should be able to use all of its stored energy (i.e., its energy utilization factor is $\mu_L = 1$). This requires that the peak inductor current should be close to its saturation point: $I_{\text{sat}} \approx I_{\text{pk}} = \frac{\pi}{2} I_{\text{out}}$. Under this constraint, an inductor with lower profile is desired. However, in order to not degrade the efficiency significantly, the inductor DCR should be comparable to or lower than the equivalent total switch on-resistance. Second, as illustrated in Fig. 3.5, a volume ratio $\frac{\text{Vol}_\text{C}}{\text{Vol}_\text{L}}$ close to one is more likely to minimize the total passive component volume. This principle can be used to guide the L and C allocation. After evaluating the available commercial components, 200 nH Coilcraft XEL4030 inductor is selected for its good balance of volume and loss, and 35V 0805 X5R TDK ceramic capacitors are selected as the flying capacitors. Besides very high energy density, the selected capacitors also have small package size which allows for fine tuning the total flying capacitance. The selected LC tank has an energy density ratio of $\frac{\rho_{E,C}}{\rho_{E,L}} = 233$, a total volume of 76 mm^3 and a volume ratio of $\frac{\text{Vol}_\text{C}}{\text{Vol}_\text{L}} = 0.6$. Note that this $\frac{\text{Vol}_\text{C}}{\text{Vol}_\text{L}}$ slightly deviates from the theoretical optimum due to the limited selection of inductor sizes.

The pure SC converter uses the same switches and flying capacitors as those of the ReSC converter. Given same power rating and switching frequency, its efficiency can be controlled by the amount of flying capacitance. In order to compare the required passive volume with the ReSC converter, an efficiency sweep is performed repeatedly with an increasing amount of flying capacitance, until the pure SC converter can achieve the same efficiency performance as that of the ReSC converter at 15 A output current. The measured efficiency performance is shown in Fig. 3.10. It is found that the pure SC converter needs 272 mm^3 of flying capacitors to match the efficiency of the ReSC converter. This results in a volume ratio $\frac{\text{Vol}_\text{pureSC}}{\text{Vol}_\text{ReSC}}$ of 3.6, as compared to a calculated value of 4.4. The deviation is possibly from the additional loss of the resonant inductor, which is not considered in the model.

For the buck converter, it is very challenging to achieve 99% efficiency at this operating point. Therefore, the comparison of its passive volume is mainly focused on the minimal energy storage requirement, rather than comparable efficiency performance. By performing inductor volt-second analysis, it can be found that when converting 48 V to 24 V at 100 kHz,

Table 3.2: Main component listing of the hardware prototype

	Component	Part number	Parameters
ReSC	Switch	Infineon BSZ018N04LS6	40 V, 1.6 mΩ
	Flying capacitor	TDK C2012X5R1V226M125AC	X5R, 35 V, 22 μF*×9
	Resonant inductor	XEL4030-201ME	200 nH, 22 A I_{sat}
Pure SC	Switch	Infineon BSZ018N04LS6	40 V, 1.6 mΩ
	Flying capacitor	TDK C2012X5R1V226M125AC	X5R, 35 V, 22 μF*×87
Buck	Switch	Infineon BSZ070N08LS5	80 V, 5.9 mΩ
	Inductor	Vishay IHLP6767GZER5R6M01	5.6 μH, 40 A I_{sat}

* The capacitance listed here is the nominal value before dc derating.

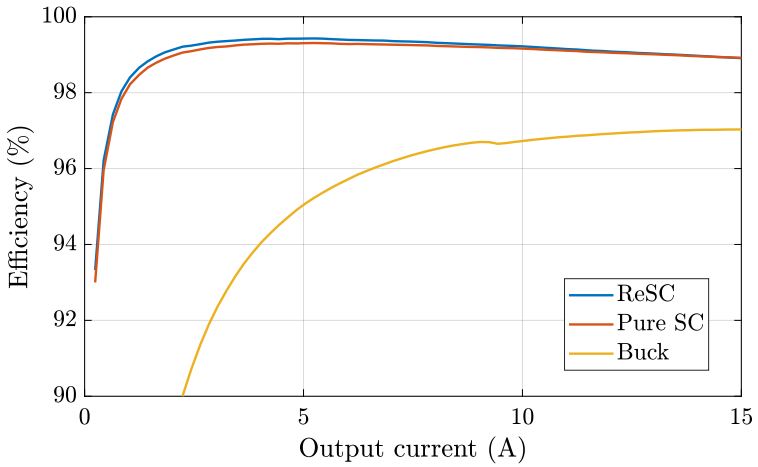


Figure 3.10: Measured 48-to-24 V efficiency (f_{sw} = 100 kHz).

a minimum 4 μH inductance is needed to maintain boundary conduction mode at 15 A output current. Among off-the-shelf inductors, the Vishay IHLP6767 family is found to be a good candidate which can meet both the inductance and saturation current requirements. The selected inductor has 5.6 μH and 40 A saturation current, and thus a total energy storage greater than the minimum requirement. It has a volume of 2059 mm^3 and an energy density ratio $\frac{\rho_{E,C}}{\rho_{E,L}}$ of 94, compared to the resonant capacitor in the 2-to-1 ReSC converter. Note that the energy density of this buck inductor is different and higher than that of the resonant inductor in the ReSC converter. Based on (3.10) and (3.11), the theoretical volume ratio is found to be $\frac{\text{Vol}_{\text{buck}}}{\text{Vol}_{\text{ReSC}}} = 11.5$. On the other hand, the hardware-based actual volume ratio

Figure 3.11: Required passive component volume to achieve the efficiency performance shown in Fig. 3.10.

Table 3.3: Comparison between calculation and experiment

	Calculation	Experiment
$\frac{\text{Vol}_{\text{pureSC}}}{\text{Vol}_{\text{ReSC}}}$	4.4	3.6
$\frac{\text{Vol}_{\text{buck}}}{\text{Vol}_{\text{ReSC}}}$	11.5	11*

* After factoring out the excess energy.

is $\frac{\text{Vol}_{\text{buck}}}{\text{Vol}_{\text{ReSC}}} = 27$. This is because the selected inductor is over-sized with an energy storage capability greater than the required amount. After factoring out the excess stored energy of the inductor ($\frac{4\mu H \cdot 30A^2}{5.6\mu H \cdot 40A^2}$), the true volume ratio $\frac{\text{Vol}_{\text{buck}}}{\text{Vol}_{\text{ReSC}}}$ becomes 11, which closely matches with the calculated result.

Fig. 3.11 showcases the required passive component volume of different solutions, and Table 3.3 compares the experimental volume ratios with the calculated results. The ReSC converter can deliver its promised benefits and achieve the highest efficiency with significantly less passive component volume than conventional solutions.

3.4 Generalized Analysis

So far, we have shown that through reactive power/energy analysis, the total passive component volume of a 2-to-1 ReSC converter can be calculated and optimized based on only P_{out},

f_{sw} (resonant frequency), $\rho_{E,C}$, and $\rho_{E,L}$, by adjusting the capacitor ripple ratio $\frac{\Delta V_{C0}}{V_{C0}}$. There is no need to assume or constrain the L and C values. Next, we generalize this method to any ReSC topologies with any number of flying capacitors and inductors.

Equation Formulation

Since all topologies degenerate to the same basic structure at a conversion ratio of 2, we can use the result of the 2-to-1 ReSC converter as a baseline. Assuming the 2-to-1 ReSC converter has inductance L, flying capacitance C, switching frequency $f_{\text{sw}} = \frac{1}{2\pi\sqrt{LC}}$, output voltage V_{out} and output current I_{out}, its peak-to-peak capacitor voltage ripple can be derived as $\Delta V_{C0} = \frac{I_{\text{out}}}{2Cf_{\text{sw}}}$, and the power processed by the inductor is $P_{L0} = \frac{I_{\text{out}}\Delta V_{C0}}{16}$. When expanding to higher conversion ratios, the capacitance ratio among the flying capacitors should be first determined by the soft-charging requirement [19] and other practical considerations (e.g. same resonant frequency for different LC tanks). For most common topologies (e.g. series-parallel, Dickson, FCML), all added flying capacitors should have the same capacitance C as compared to the 2-to-1 case. For the Doubler topology [37], the capacitance ratio is $C_1 = C$, $C_2 = \frac{1}{4}C$, ... , $C_n = \frac{1}{2^{2n-2}}C$. If an ReSC converter has multiple resonant inductors, it is usually required to have the same resonant frequency for all resonant tanks. Therefore, for the topologies with equal capacitance C, all inductors should have the same value of L. For the Doubler topology, the inductance ratio is $L_1 = L$, $L_2 = 4L$, ... , $L_n = 2^{2n-2}L$. Additionally, both V_{out} and I_{out} remain the same as in the 2-to-1 case. Now, we can express the processed reactive power $P_{C,i}$, average dc voltage $V_{C,i}$ and ac ripple voltage $\Delta V_{C,i}$ of any given flying capacitor C_i in terms of P_{out}, V_{out} and ΔV_{C0} (the capacitor ripple voltage in the 2-to-1 case):

$$C_i \Rightarrow \begin{cases} P_{C,i} = k_i P_{\text{out}} \\ V_{C,i} = \alpha_i V_{\text{out}} \\ \Delta V_{C,i} = \beta_i \Delta V_{C0} \end{cases} \tag{3.24}$$

where k_i, α_i and β_i are topology dependent parameters. An example of how these parameters can be derived will be given in the next subsection. Once these parameters have been calculated, the ripple voltage ratio of C_i can be expressed as

$$\frac{\Delta V_{C,i}}{V_{C,i}} = \frac{\beta_i \Delta V_{C0}}{\alpha_i V_{\text{out}}} \tag{3.25}$$

and the energy utilization factor $\mu_{C,i}$ can be generalized from (3.5) as

$$\mu_{C,i} = \frac{2\frac{\Delta V_{C,i}}{V_{C,i}}}{(1+\frac{1}{2}\frac{\Delta V_{C,i}}{V_{C,i}})^2} = \frac{\frac{2\beta_i \Delta V_{C0}}{\alpha_i V_{\text{out}}}}{(1+\frac{\beta_i \Delta V_{C0}}{2\alpha_i V_{\text{out}}})^2}. \tag{3.26}$$

The required energy storage $E_{C_i,\text{store}}$ of capacitor C_i at a switching frequency of f_{sw} can be derived as

$$\begin{aligned} E_{C_i,\text{store}} &= \frac{P_{C,i}}{f_{\text{sw}}\mu_{C,i}} = \frac{k_i P_{out}}{f_{\text{sw}}\mu_{C,i}} \\ &= \frac{P_{\text{out}}}{f_{\text{sw}}}\left(\frac{k_i}{2} + \frac{k_i\alpha_i}{2\beta_i}\frac{V_{\text{out}}}{\Delta V_{C0}} + \frac{k_i\beta_i}{8\alpha_i}\frac{\Delta V_{C0}}{V_{\text{out}}}\right). \end{aligned} \tag{3.27}$$

Next, the total required energy storage of the sum of the n flying capacitors is given by

$$\begin{aligned} E_{C,\text{tot}} =& \sum_{i=1}^{n} E_{C_i,\text{store}} \\ =& \frac{P_{\text{out}}}{f_{\text{sw}}}\left(K_{\text{tot}} + A_{\text{tot}}\frac{V_{\text{out}}}{\Delta V_{C0}} + B_{\text{tot}}\frac{\Delta V_{C0}}{V_{\text{out}}}\right) \end{aligned} \tag{3.28}$$

where $K_{\text{tot}} = \frac{1}{2}\sum_{i=1}^{n} k_i$, $A_{\text{tot}} = \frac{1}{2}\sum_{i=1}^{n}\frac{k_i\alpha_i}{\beta_i}$, and $B_{\text{tot}} = \frac{1}{8}\sum_{i=1}^{n}\frac{k_i\beta_i}{\alpha_i}$. Similarly, the power processed by an inductor L_i can be expressed as a ratio with the P_{L0} in the basic 2-to-1 case:

$$P_{L_i} = \gamma_i P_{L0} \tag{3.29}$$

and the total required energy of the sum of the m inductors is

$$E_{L,\text{tot}} = \sum_{i=1}^{m} E_{L_i} = \frac{P_{L0}}{f_{\text{sw}}}\sum_{i=1}^{m}\gamma_i = \frac{P_{L0}}{f_{\text{sw}}}Y_{\text{tot}} \tag{3.30}$$

with $Y_{\text{tot}} = \sum_{i=1}^{m}\gamma_i$. Note that this analysis is general in nature, and can be applied to any ReSC converters with different inductor locations, including "inductor at output" and "inductor in series with flying capacitor" configurations [38].

Following the same procedure as that in (3.8), we can express the total passive volume as a function of $\frac{\Delta V_{C0}}{V_{\text{out}}}$:

$$\begin{aligned} \text{Vol}_{\text{tot}} &= \text{Vol}_{\text{C}} + \text{Vol}_{\text{L}} \\ &= \frac{P_{\text{out}}}{f_{\text{sw}}}\left(\frac{K_{\text{tot}} + A_{\text{tot}}\frac{V_{\text{out}}}{\Delta V_{C0}} + B_{\text{tot}}\frac{\Delta V_{C0}}{V_{\text{out}}}}{\rho_{E,C}} + \frac{\frac{1}{16}Y_{\text{tot}}\frac{\Delta V_{C0}}{V_{\text{out}}}}{\rho_{E,L}}\right). \end{aligned} \tag{3.31}$$

By differentiating Vol_{tot} with respect to $\frac{\Delta V_{C0}}{V_{\text{out}}}$, the optimized capacitor ripple ratio r^* and the minimized total passive volume $\text{Vol}_{\text{tot,min}}$ can be derived:

$$r^* = \left(\frac{\Delta V_{C0}}{V_{\text{out}}}\right)^* = \sqrt{\frac{16A_{\text{tot}}\rho_{E,L}}{16B_{\text{tot}}\rho_{E,L} + Y_{\text{tot}}\rho_{E,C}}} \tag{3.32}$$

$$\text{Vol}_{\text{tot,min}} = \frac{P_{\text{out}}}{f_{\text{sw}}\rho_{E,L}}\left(\frac{\rho_{E,L}}{\rho_{E,C}}\left(K_{\text{tot}} + A_{\text{tot}}\frac{1}{r^*} + B_{\text{tot}}r^*\right) + \frac{Y_{\text{tot}}r^*}{16}\right). \tag{3.33}$$

When $\rho_{E,C} \gg \rho_{E,L}$ and $Y_{\text{tot}}\rho_{E,C} \gg 16B_{\text{tot}}\rho_{E,L}$, r^* can be further simplified to:

$$r^* = \sqrt{\frac{16A_{\text{tot}}\rho_{E,L}}{16B_{\text{tot}}\rho_{E,L} + Y_{\text{tot}}\rho_{E,C}}} \approx \sqrt{\frac{16A_{\text{tot}}\rho_{E,L}}{Y_{\text{tot}}\rho_{E,C}}} \tag{3.34}$$

yielding an approximated minimized total volume of

$$\text{Vol}_{\text{tot,min}} \approx \frac{P_{\text{out}}}{f_{\text{sw}}\rho_{E,L}}\Big(K_{\text{tot}}\frac{\rho_{E,L}}{\rho_{E,C}} + \frac{1}{2}\sqrt{\frac{A_{\text{tot}}Y_{\text{tot}}\rho_{E,L}}{\rho_{E,C}}}\Big). \tag{3.35}$$

In this expression, no detailed L and C values need to be assumed or constrained. The P_{out}, f_{sw}, $\rho_{E,L}$ and $\rho_{E,C}$ terms depend on the operating condition and the remaining terms are purely topology specific parameters. This equation can be used to quantitatively calculate the minimum achievable passive volume of any hybrid resonant SC converter at a given power level and switching frequency. Note that this analysis assumes that all flying capacitors have an energy density of $\rho_{E,C}$ and all resonant inductors have an energy density of $\rho_{E,L}$. For the topologies that use multiple types of capacitors and inductors with different power densities [23], (3.31) can be modified to incorporate multiple ρ_{E,C_i} and ρ_{E,L_i}.

Example of N-to-1 Resonant Series-Parallel Converter

Here, we use an N-to-1 resonant series-parallel converter as an example to demonstrate how the topology dependent parameters k_i, α_i, β_i and γ_i in (3.24) and (3.29) can be derived.

Resonant series-parallel converters can be implemented with two types of augmenting inductors: distributed inductors and a single inductor at output. The circuit schematics and the associated current waveforms of these two types of implementations are shown in Fig. 3.12. In an N-to-1 series-parallel converter, there are $N-1$ flying capacitors with equal capacitance. All are connected in series in the series-phase ϕ_s and paralleled in the parallel-phase ϕ_p. Through KVL analysis, it can be found that all capacitors have an average dc voltage of V_{out}. According to (3.24), $V_{C,i} = \alpha_i V_{\text{out}}$, thus

$$\alpha_1 = \alpha_2 = \cdots = \alpha_{N-1} = 1. \tag{3.36}$$

As derived in [32], the power processed by a capacitor C_i can be calculated as

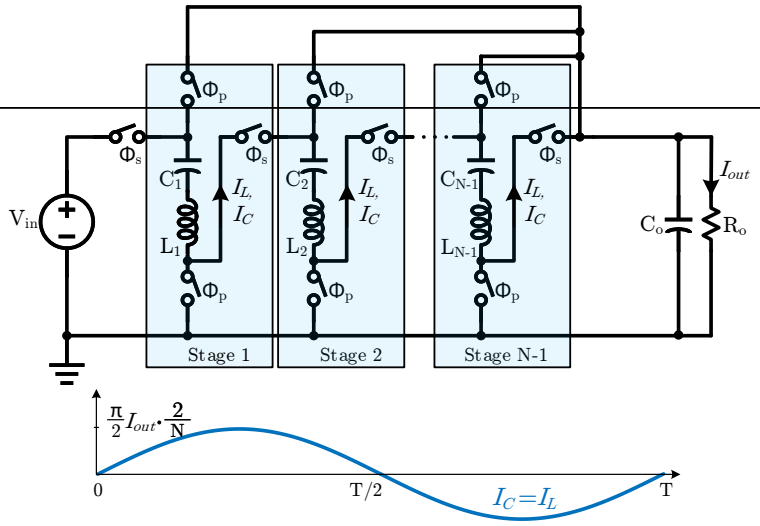
$$P_{C,i} = \frac{1}{2}\overline{|\, V_{C,i}I_{C,i}\,|} \tag{3.37}$$

where

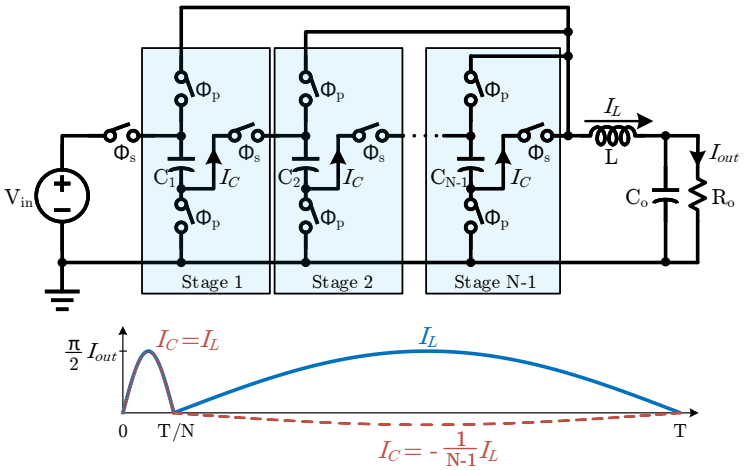
$$\overline{|\, V_{C,i}I_{C,i}\,|} \triangleq \frac{1}{T}\int_0^T |\, V_{C,i}I_{C,i}\,|\, dt. \tag{3.38}$$

For ReSC converters, (3.37) can be simplified to

$$P_{C,i} = \frac{1}{2}V_{C,i}I_{C,i} \tag{3.39}$$



(a) Distributed inductors



(b) Single inductor at output

Figure 3.12: N-to-1 resonant series-parallel converters with different inductor locations.

where $V_{C,i}$ is the average dc voltage and $I_{C,i}$ is the average charging (or discharging) current through C_i.

Through charge flow analysis [7], it can be found that $I_{C,i} = \frac{2}{N} I_{\text{out}}$ in a N-to-1 series-parallel converter. Thus, $P_{C,i} = k_i V_{\text{out}} I_{\text{out}} = \frac{V_{\text{out}} I_{\text{out}}}{N}$ and

$$k_1 = k_2 = \cdots = k_{N-1} = \frac{1}{N}. \tag{3.40}$$

The voltage on capacitor C_i is $V_{C,i} - \frac{I_{pk_{c,i}}}{C_i \omega_{r_{c,i}}} cos(\omega_{r_{c,i}} t)$. Thus, its peak-to-peak voltage ripple is

$$\Delta V_{C,i} = \frac{2 I_{pk_{c,i}}}{C_i \omega_{r_{c,i}}} \tag{3.41}$$

where $I_{pk_{c,i}}$ is the peak current flowing through C_i and $\omega_{r_{c,i}}$ is the resonant frequency of the LC tank associated with C_i. For the distributed inductor configuration in Fig. 3.12a, C_i and $\omega_{r_{c,i}}$ are the same as those in the basic 2-to-1 case, whereas its peak current $I_{pk_{c,i}}$ is $\frac{2}{N}$ times of the baseline value I_{pk}, yielding $\Delta V_{C,i} = \frac{2}{N} \Delta V_{C0}$ and

$$\beta_{1,dis} = \beta_{2,dis} = \cdots = \beta_{N-1,dis} = \frac{2}{N}. \tag{3.42}$$

For the single inductor at output configuration in Fig. 3.12b, the duty ratio of ϕ_s changes to $\frac{T}{N}$ to maintain capacitor charge balance. In ϕ_s, all capacitors are connected in series ($C_{\text{eq}} = \frac{1}{N-1} C$) and conduct the entire output current ($I_{pk} = \frac{\pi}{2} I_{\text{out}}$). The voltage ripple of each capacitor is

$$\Delta V_{C,i} = \frac{1}{N-1} \cdot \frac{2 I_{pk}}{C_{eq} \frac{1}{\sqrt{L C_{eq}}}} = \frac{1}{\sqrt{N-1}} \Delta V_{C0} \tag{3.43}$$

leading to a set of different β values compared to the distributed inductor case:

$$\beta_{1,single} = \beta_{2,single} = \cdots = \beta_{N-1,single} = \frac{1}{\sqrt{N-1}}. \tag{3.44}$$

The power processed by inductor L_i can be calculated with the integral method in (3.2). Alternatively, if all inductors are assumed to have the same value L, $P_{L,i}$ can be related to P_{L0} by comparing the amplitude of its peak current $I_{pk_{L,i}}$ and the effective switching period T_{eff}. For the distributed inductor case, the inductor current is related to the baseline current by $I_{pk_{L,i}} = \frac{2}{N} I_{pk}$, resulting in $E_{L,i} = \frac{4}{N^2} E_{L0}$. Since $T_{\text{eff}} = T = 2\pi\sqrt{LC}$ is the same as the 2-to-1 case, $P_{L,i} = \frac{E_{L,i}}{T_{\text{eff}}} = \frac{4}{N^2} P_{L0}$ and

$$\gamma_{1,dis} = \gamma_{2,dis} = \cdots = \gamma_{N-1,dis} = \frac{4}{N^2}. \tag{3.45}$$

For the single inductor at output case, the inductor conducts the entire output current $I_{pk_{L,i}} = I_{pk}$ and therefore $E_{L,i} = E_{L0}$. The effective switching period can be calculated as the average of the series resonant period and the parallel resonant period:

$$T_{\text{eff}} = \frac{T_{series} + T_{parallel}}{2} = \frac{2\pi\left(\sqrt{L\frac{C}{N-1}} + \sqrt{L(N-1)C}\right)}{2} \tag{3.46}$$

resulting in $P_{L,i} = \frac{2\sqrt{N-1}}{N} P_{L0}$ and

$$\gamma_{single} = \frac{2\sqrt{N-1}}{N}. \tag{3.47}$$

Table 3.4: Key parameters of N-to-1 series-parallel converter

	k_i	α_i	β_i	γ_i
Distributed inductors	$\frac{1}{N}$	1	$\frac{2}{N}$	$\frac{4}{N^2}$
Single inductor	$\frac{1}{N}$	1	$\frac{1}{\sqrt{N-1}}$	$\frac{2\sqrt{N-1}}{N}$

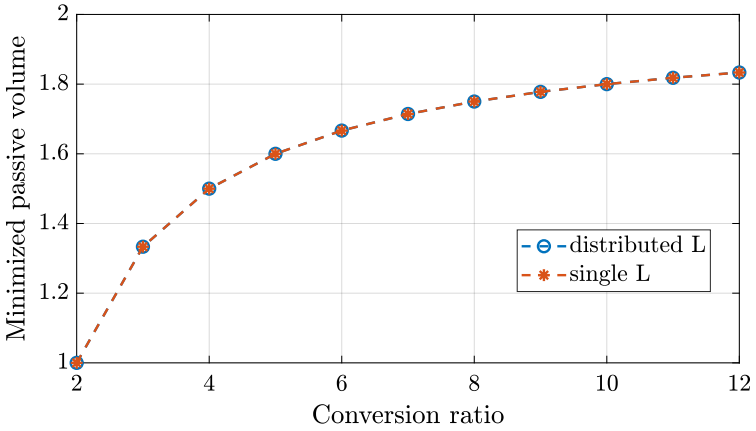


Figure 3.13: Minimized total passive volume of N-to-1 resonant series-parallel converters with different inductor locations (normalized to the 2-to-1 case).

The calculated topology dependent parameters are summarized in Table 3.4. It can be seen that the capacitor ripple term β_i and the inductor power term γ_i are different for the two types of inductor locations. Nevertheless, as shown in Fig. 3.13, they can achieve the same total minimized passive volume, as calculated from (3.33). This example demonstrates that the proposed method is applicable to generalized ReSC topologies with different inductor placement strategies.

3.5 Resonant SC Topology Comparison

Besides optimizing the total passive component volume, the proposed method can also be used to compare the relative volume of different ReSC topologies. It can be observed from (3.35) that the expression of the minimized total passive volume consists of two parts. The first part $\frac{P_{\text{out}}}{f_{\text{sw}}\rho_{E,L}}$ depends on the operating conditions, and can be viewed as the volume of an inductor that stores all of the energy delivered to the load in each switching cycle. The remaining part contains topology dependent parameters and the energy density ratio of

capacitor and inductor. It represents the relative volume ratio to an inductor whose volume is $\frac{P_{\text{out}}}{f_{\text{sw}}\rho_{E,L}}$ and can be considered as a "passive component utilization factor" of the topology. By normalizing with respect to the $\frac{P_{\text{out}}}{f_{\text{sw}}\rho_{E,L}}$ portion of (3.35), a normalized passive component volume M_p is defined as

$$\begin{aligned} M_p =& \frac{\text{Vol}_{\text{tot,min}}}{\frac{P_{\text{out}}}{f_{\text{sw}}\rho_{E,L}}} \\ =& \frac{\rho_{E,L}}{\rho_{E,C}}(K_{\text{tot}} + A_{\text{tot}}\frac{1}{r^*} + B_{\text{tot}}r^*) + Y_{\text{tot}}r^*. \end{aligned} \tag{3.48}$$

Note that this M_p is independent of f_{sw} and P_{out}, indicating that it can provide a direct volume comparison among different topologies at the same output power and switching frequency.

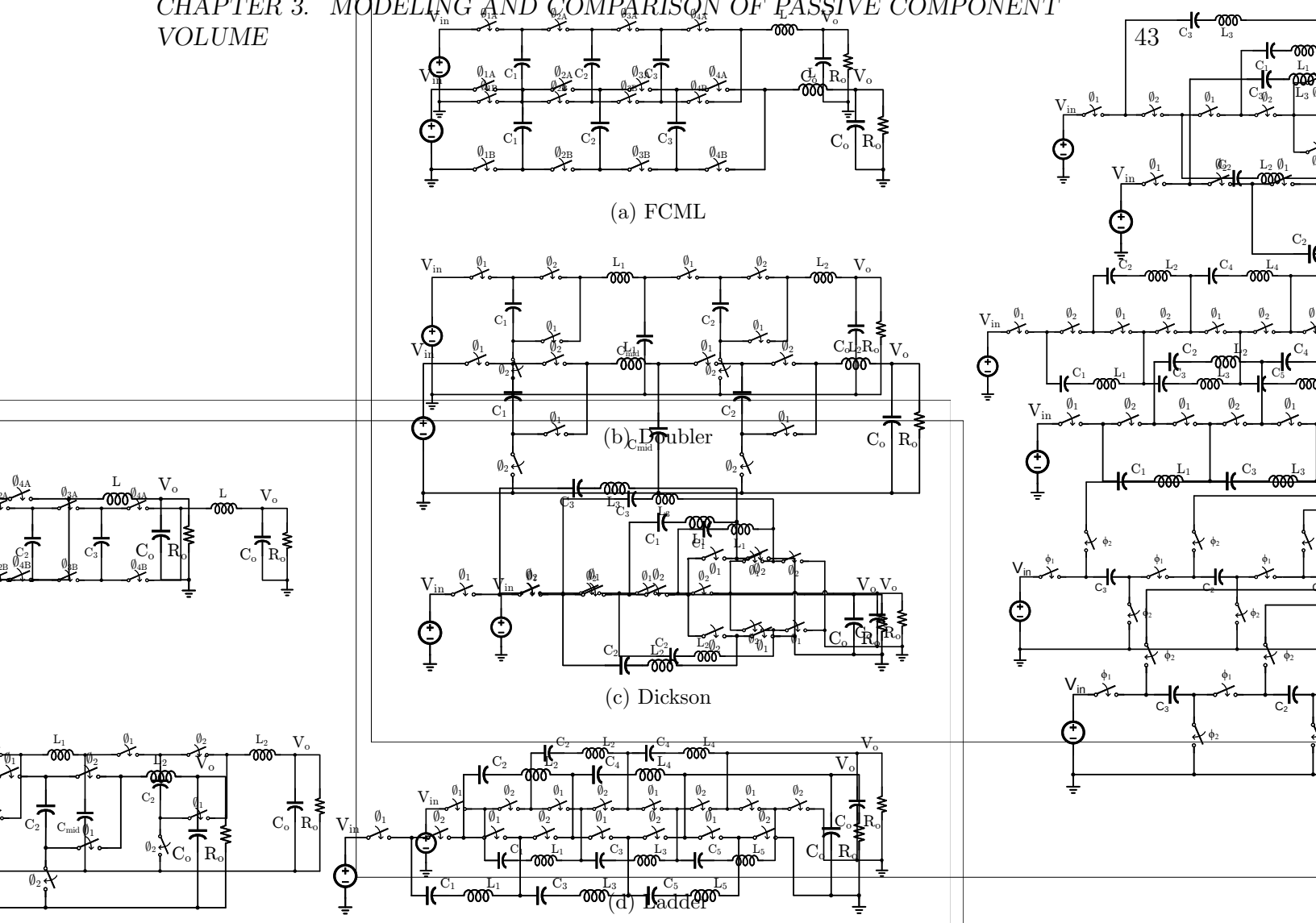
Here, we compare the normalized passive component volume M_p of various ReSC topologies that are adapted from common SC converters [23], [38]–[41]. The circuit schematic of the series-parallel topology is shown in Fig. 3.12 and the schematics of the other topologies under investigation are shown in Fig. 3.14. Their M_p values are calculated and plotted in Fig. 3.15, and a buck converter is included for reference. Even though empirical data shows that the ratio of $\frac{\rho_{E,C}}{\rho_{E,L}}$ can be as high as 1000 [42], a relatively conservative ratio of $\frac{\rho_{E,C}}{\rho_{E,L}} = 100$ is used here. The buck converter is assumed to operate at the boundary conduction mode such that its inductor energy utilization is maximized.

It can be seen from Fig. 3.15 that, thanks to the high energy density of capacitors, all ReSC converters outperform the buck converter by a wide margin, especially at relatively low conversion ratios. In particular, the series-parallel topology achieves the lowest passive component volume among all topologies. This result agrees with the finding in [35], [42], where the series-parallel converter is at the theoretical Wolaver limit [32] of passive components. Additionally, although requiring high voltage capacitors, the FCML topology achieves relatively good passive component utilization, owing to the frequency multiplication effect that reduces the energy storage requirement of the components.

For the same switching frequency, a lower total switch stress indicates a potentially lower conduction loss, lower switching loss, and smaller switch size. Therefore, it can be used as a good indication of potential efficiency [30]. The switch stress is defined as

$$\text{Total switch stress } = \sum_{\text{switches}} V_{ds}I_{ds} \tag{3.49}$$

where V_{ds} is the peak blocking voltage seen by the switch and I_{ds} is the average current through the switch. As discussed in [24], the rms current value should be used for the best accuracy when the duty ratio is deviated from 50%. However, as most ReSC topologies of interest operate at 50% duty ratio and the rms/average ratio is fixed, the average current value is used here as a close approximation. Since one can express V_{ds} using the output voltage ($\beta_v V_{\text{out}}$), and I_{ds} using the output current ($\beta_i I_{\text{out}}$), the normalized switch stress M_s



(a) FCML

(b) Doubler

(c) Dickson

(d) Ladder

Figure 3.14: 4-to-1 resonant switched-capacitor converter topologies.

can be defined as

$$M_s = \frac{\text{total switch stress}}{V_{\text{out}} I_{\text{out}}} = \sum_{\text{switches}} \beta_v \beta_i. \tag{3.50}$$

This can be viewed as the total switch power rating necessary to deliver a certain power to the output. More details regarding this metric can be found in [13]. Fig. 3.16 shows the calculated M_s of the topologies of interest, with the Dickson [21], [43] and Ladder topologies at the Wolaver limit [35]. It should be emphasized that the derived M_p and M_s reflect the intrinsic performance of passive and active component utilization and are independent of detailed operating conditions (e.g., P_{out}, f_{sw}).

Fig. 3.17 compares the relative performance of various topologies at a ratio of 4-to-1. In general, the topologies that have high normalized switch stress tend to have lower

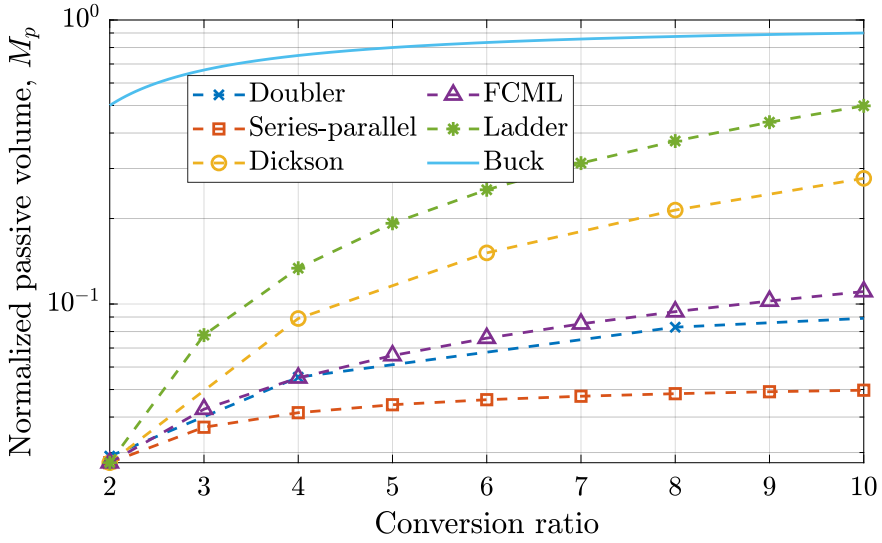


Figure 3.15: Normalized passive volume (assuming $\rho_{E,C}/\rho_{E,L} = 100$). Lower is better.

normalized passive volume, and vice versa. With the series-parallel and Dickson topologies at the theoretical boundaries of passive and active component Wolaver limits, respectively, all other classical and emerging topologies will fit inside those bounds. Note that the switched-tank (STC) converter [23] has the same theoretical performance as the Dickson as they share the same fundamental structure. This plot allows designers to quickly visualize and compare the trade-offs of different solutions.

It should be noted that practical converter designs have more considerations and the actual performance of different topologies can be different than what is plotted here. For instance, the lowest voltage rating of widely available discrete power MOSFETs is at present about 25 V. Thus, for discrete applications with input voltage lower than 25 V, the topologies with low switch voltage rating and switch VA stress (e.g., Dickson) cannot fully utilize their potential. In this case, the topology efficiency comparison should be based on switch conductance G rather than GV^2 (VA rating) [24]. Then, it is found that the series-parallel topology can achieve one of the lowest output impedances among all ReSC topologies, even though its normalized switch stress is the highest in Fig. 3.17. In addition, the implementation complexity should also be considered, such as the number of components, the design of gate drive circuit and the ease of PCB layout. This may put the doubler topology in an attractive position because of its simple and highly modular design. Note that the inter-stage decoupling capacitors in the doubler topology are not included in the passive volume calculation, as they can be eliminated by two-phase interleaving operation, which is detailed in Chapter 6.

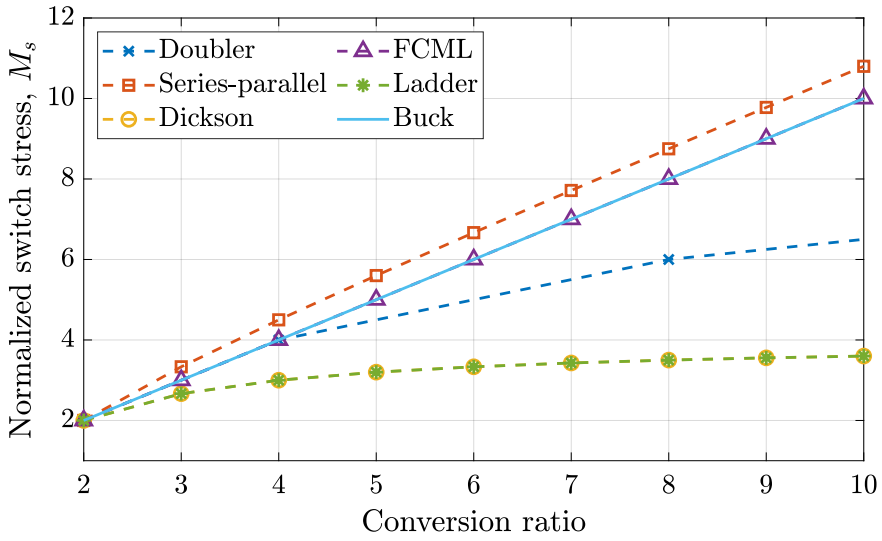


Figure 3.16: Normalized switch stress. Lower is better.

3.6 Comparison of Regulated Hybrid Converters

So far, all analysis has focused on fixed-ratio ReSC converters, in which the inductors see only the flying capacitor voltage ripples. Next, we briefly discuss how the reactive power calculation can be applied to analyze and compare hybrid SC converters with regulation capability. In such converters, the switched-capacitor stage is typically combined with a buck stage. The buck stage can achieve voltage regulation through pulse-width modulation (PWM), while serving as a current source for capacitor soft-charging operation. In this section, we analyze two basic hybrid converter topologies, the three-level buck converter and the series-capacitor buck converter. Their circuit schematics are shown in Fig. 3.18. In spite of having the same number of switches and flying capacitor, they have very different operating characteristics and advantages owing to different inductor placement strategy.

Calculating the Reactive Power of Three-Level Buck Converter

Here, we detail the reactive power calculation of a three-level buck converter. The same method can be applied to any other regulated hybrid SC topologies. Since the three-level buck converters have different circuit operating states for duty ratio $D < 0.5$ and $D > 0.5$, the calculations are carried out for these two intervals separately.

(1) $D < 0.5$

The four circuit operating states and the corresponding durations are shown in Fig. 3.19. Assuming the flying capacitor C_1 is at its nominal voltage $\frac{1}{2}V_{\text{in}}$ with no voltage ripple, then the switch node voltage V_{sw} will be at $\frac{1}{2}V_{\text{in}}$ during state 1 and 3, and at ground during state

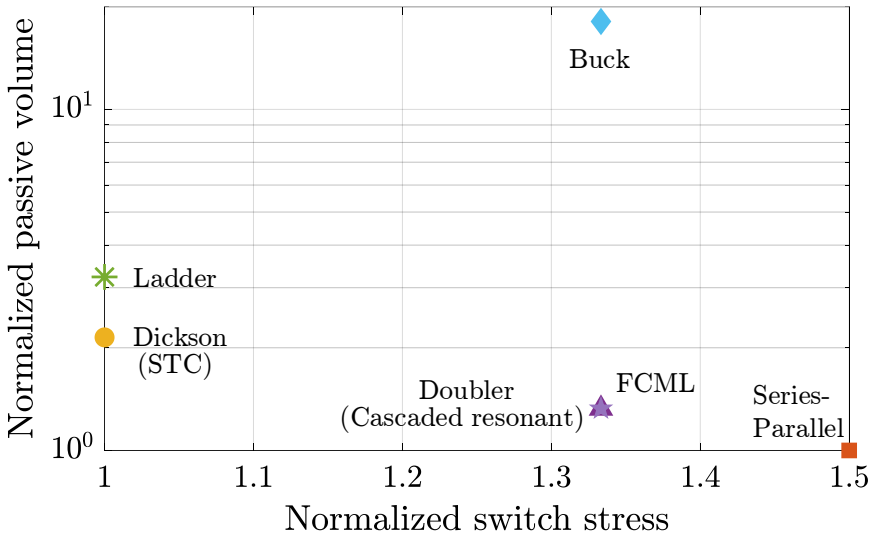
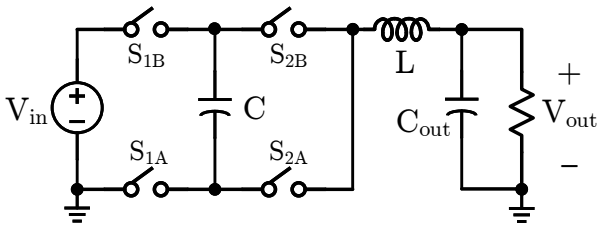


Figure 3.17: 4-to-1 ReSC topology comparison.

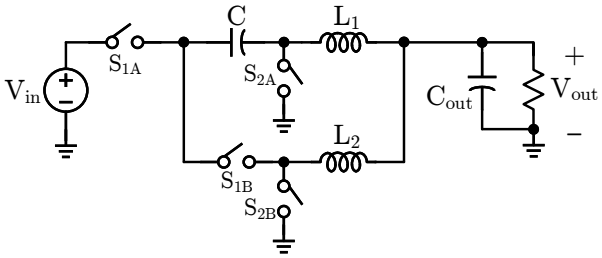
2 and 4. Since C_1 is only charged in one state (state 1) and discharged in another (state 3), its processed power simply equals the charging power at state 1 (or the discharging power at state 3). Assuming the inductor current is constant, we find:

$$\begin{aligned} P_{\mathrm{C}} &= P_{\mathrm{C,state1}} \\ &= \frac{\frac{1}{2} V_{\mathrm{in}} I_{\mathrm{out}} DT}{T} \\ &= \frac{1}{2} \frac{V_{\mathrm{out}}}{D} I_{\mathrm{out}} D \\ &= \frac{1}{2} P_{\mathrm{out}}. \end{aligned} \tag{3.51}$$

It can be seen that the power processed by the flying capacitor is a constant value for $D < 0.5$. The power processed by the inductor can be calculated in a similar way. However, since it transfers energy twice per switching cycle, only one charging state should be considered for



(a) three-level buck converter



(b) Series-capacitor buck converter

Figure 3.18: Schematic drawings of two example regulated hybrid converters.

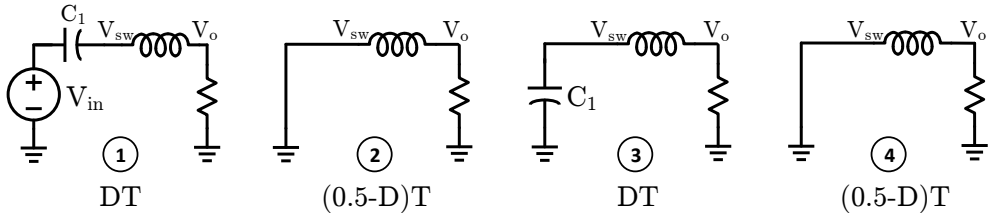


Figure 3.19: Circuit operating states of a three-level buck converter at $D < 0.5$.

power calculation:

$$\begin{aligned} P_{\mathrm{L}} &= P_{\mathrm{L,state1}} \\ &= (\frac{1}{2}V_{\mathrm{in}} - V_{\mathrm{out}})I_{\mathrm{out}}D \\ &= (\frac{1}{2} - D)\frac{V_{\mathrm{out}}}{D}I_{\mathrm{out}}D \\ &= (\frac{1}{2} - D)P_{\mathrm{out}} \end{aligned} \tag{3.52}$$

(2) $D > 0.5$

The circuit operating states for $D > 0.5$ is shown in Fig. 3.20, and the capacitor and inductor power can be calculated as follows:

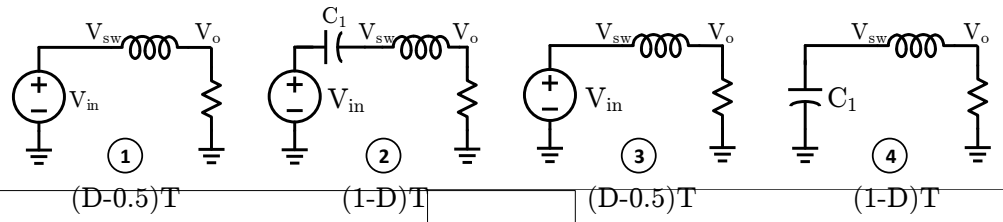
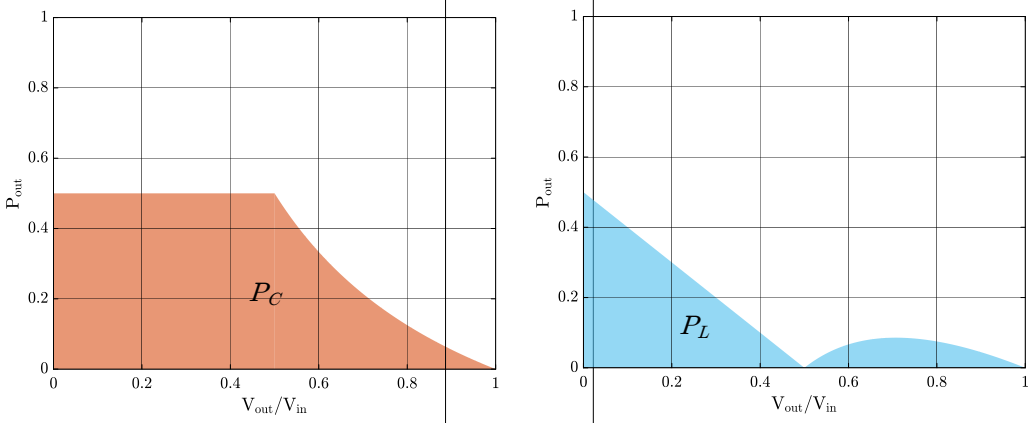


Figure 3.20: Circuit operating states of a three-level buck converter at $D > 0.5$.

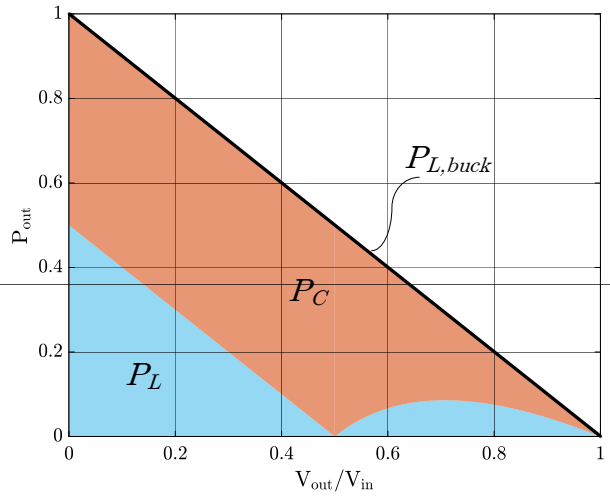


(a) Capacitor power (b) Inductor power

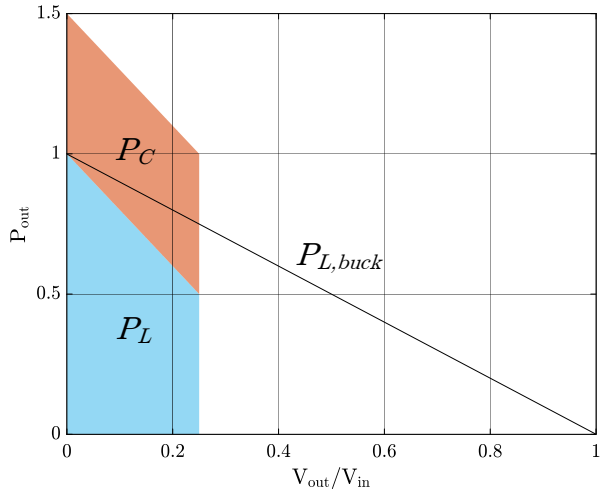
Figure 3.21: Reactive power processed by the passive components of a three-level buck converter.

$$\begin{aligned} P_{\mathrm{C}} &= P_{\mathrm{C,state2}} \\ &= \frac{1}{2} V_{\mathrm{in}} I_{\mathrm{out}} (1-D) \\ &= \frac{1-D}{2D} P_{\mathrm{out}} \end{aligned} \tag{3.53}$$

$$\begin{aligned} P_{\mathrm{L}} &= P_{\mathrm{L,state1}} \\ &= (V_{\mathrm{in}} - V_{\mathrm{out}}) I_{\mathrm{out}} (D-0.5) \\ &= (1-D) \frac{V_{\mathrm{out}}}{D} I_{\mathrm{out}} (D-0.5) \\ &= (-D + \frac{3}{2} - \frac{1}{2D}) P_{\mathrm{out}} \end{aligned} \tag{3.54}$$



(a) Three-level buck converter



(b) Series-capacitor buck converter

Figure 3.22: Average power processed by the passive components in hybrid converters.

The above calculated P_C and P_L are plotted in Fig. 3.21, and the combined total reactive power is plotted in Fig. 3.22a.

Comparison of Three-Level Buck and Series-Capacitor Buck

Fig. 3.22 plots the reactive power processed by the passive components of the three-level buck converter and the series-capacitor buck converter, as a function of conversion ratio $\frac{V_{\text{out}}}{V_{\text{in}}}$. This reactive power analysis can directly reflect the passive component utilization

of a hybrid converter. In [32], Wolaver derived that the reactive power P_{ind} that needs to be processed by a converter with a gain of G ($G = \frac{V_{\text{in}}}{V_{\text{out}}}$ for a step-down converter) is governed by $P_{\text{ind}} \geq \frac{G-1}{G} P_{\text{out}}$. It can be seen from Fig. 3.22a that the total reactive power of the three-level buck converter is equal to that of a conventional buck converter, which is known to be at the Wolaver limit. Thanks to the reduced voltage stress and the frequency doubling effect, the inductor experiences less volt-second and processes significantly less power than a conventional buck converter. Even though the total processed power remains the same, a great portion is now processed by the high energy-density flying capacitor, resulting in reduced total passive component volume and less power loss on the inductor. When $\frac{V_{\text{out}}}{V_{\text{in}}} = 0.5$, there is no voltage across the inductor except for the flying capacitor voltage ripple. Thus, the 2-to-1 ReSC converter can be considered as a special operating mode of three-level buck converter with minimum required inductance, at the cost of no regulation capability.

The series-capacitor buck converter can be viewed as a 2-to-1 SC converter cascaded by a two-phase interleaved buck converter, whose maximum duty ratio is 0.5. This leads to a maximum conversion ratio of $\frac{V_{\text{out}}}{V_{\text{in}}} = 0.25$. Its detailed operating principle can be found in [44]. The reactive power processed by the series-capacitor buck converter is shown in Fig. 3.22b. Because of the nature of cascaded converters, its total processed reactive power is unavoidably higher than the Wolaver limit. However, the series-capacitor buck still has the potential to achieve less total passive component volume and higher power density than the conventional buck converter. It can be shown that the power processed by the flying capacitor is a fixed value of $P_C = \frac{1}{2} P_{\text{out}}$, whereas the inductor power is equal to that of a buck converter with half of the input voltage $P_L = \frac{G-2}{G} P_{\text{out}}$. When $\frac{V_{\text{out}}}{V_{\text{in}}} = 0.25$, the power processed by the inductor is 33% lower than that of a buck converter rated for the full input voltage. Even for a high conversion ratio of $\frac{V_{\text{out}}}{V_{\text{in}}} = 0.1$, an 11% inductor power reduction is achieved. Given the same switching frequency and inductance value, this can be translated to an 11% inductor current ripple reduction. This property is noteworthy since even meager reductions in inductor current ripple may result in significant savings in core loss. Additionally, the series-capacitor buck converter has attractive features such as reduced switching loss owing to lower voltage stress on switches, and automatic current balancing for interleaving operation.

To calculate and compare the total passive component volume of different topologies at a given conversion ratio, a current ripple ratio of the inductor and a voltage ripple ratio of the flying capacitor need to be assumed first. Then, the corresponding energy utilization factors are known and the passive component volume can be derived with the method presented in Section 3.2. Considered the very high energy density ratio between capacitor and inductor (e.g., $\frac{\rho_{E,C}}{\rho_{E,L}} > 100$), it is desirable to use the SC network to achieve a higher voltage conversion ratio, so that the voltage and power stress of the following buck stage can be reduced. This strategy has the potential to further reduce both the total passive component volume and the power loss on the inductor, given that the implementation complexity of the SC stage can be properly managed. A new hybrid SC topology with an 8-to-1 SC stage is proposed

in Chapter 8.

3.7 Chapter Summary

This chapter models the passive component volume of hybrid resonant switched-capacitor converters from the perspective of the reactive power processed by the passive components. It is shown that the total passive component volume can be expressed as a function of flying capacitor voltage ripple, and the optimum inductor and capacitor allocation that minimizes the total volume is dependent on their relative energy density and topology specific parameters. Detailed analysis and experimental results are also provided to showcase that a 2-to-1 ReSC converter can use significantly less passive volume than conventional SC and buck converters for the same power conversion, while maintaining the best efficiency performance. To compare the passive component utilization of different ReSC topologies, a normalized passive volume parameter is proposed for direct and fair comparison. Along with the normalized switch stress parameter (based on switch VA ratings), a framework to compare the relative performances of different ReSC topologies is created. Using the proposed method, the series-parallel topology exists at the theoretical lower limit of passive volume, whereas the Dickson and the Ladder topologies exist at the lower limit of switch stress. These boundaries can ultimately help evaluate the performance of other newly proposed topologies. Lastly, the proposed passive component modeling method is extended to hybrid converters with regulation capabilities.

Chapter 4

Capacitor Voltage Balancing of Flying Capacitor Multilevel Converters

Capacitor voltage natural balancing is an attractive feature of flying capacitor multilevel (FCML) converters. However, with the commonly used phase-shifted pulse-width modulation (PSPWM), the capacitor voltages still can deviate from nominal, and active balancing is often required. Although the natural balancing mechanism and its dynamics have been extensively studied in existing literature, the sources that are responsible for capacitor imbalance in engineering practice are still unclear. This chapter experimentally investigates the origins of the voltage imbalance in practical implementations of FCML converters and presents the corresponding circuit analysis as well as solutions that improve balancing. It is shown that the source impedance and the input capacitor can greatly deteriorate capacitor balancing. Moreover, we also demonstrate in theory and with experiments that an FCML converter with an even number of levels inherently has stronger immunity to such disturbance than one with an odd number of levels. It is also found that the gate signal propagation delay mismatch in half-bridge gate drivers can lead to capacitor imbalance, and this problem is addressed by an alternative gate drive power supply design. Last, the variations of on-resistance among different switches are found to have a relatively small impact on capacitor voltage balancing.

4.1 Background and Motivation

Recently, the FCML converter [45] has received increased attention owing to its potential for high-density high-efficiency power conversion. While originally developed for high-voltage high-power applications, recent advances in semiconductor devices (e.g., GaN and SiC) and multilayer ceramic capacitors (MLCCs) have also made the FCML topology attractive for applications with lower voltage and power ratings. Its promising performance has been demonstrated by recent works for a variety of applications, including dc/dc converters with high-conversion-ratio [33], [46], [47], single-phase ac/dc power-factor-correction (PFC) front-

end and energy buffer [48], [49], and dc/ac inverters for renewable integration and transportation electrification [50], [51].

A major implementation challenge of FCML converter is flying capacitor voltage balancing, which describes the scenario where the capacitor voltages deviate from their nominal values due to various disturbances, resulting in an increase of the drain-to-source voltage stress across the switches. To prevent switch failures from capacitor imbalance, typically over-rated switches have to be used for an extra safety margin with accompanying performance penalties.

To regulate the capacitor voltages within a desired set of bounds, active balancing techniques [47], [52]–[57] can be applied to selectively charge or discharge one or more flying capacitors by adjusting the duty ratio of the corresponding switches. Such techniques require the monitoring of capacitor states, which can be achieved by direct flying capacitor voltage sensing [53], switch node voltage sensing [54], and peak and valley inductor current detection [47], [55]. However, these methods can be difficult/costly to apply to FCML converters with a high number of levels, high switching frequency and small capacitor values, due to the high bandwidth sensing and control required and the added area overhead.

Alternatively, FCML converters can rely on the natural balancing property of the PSPWM scheme [50], [58]–[60]. The existence of the natural balancing mechanism and its dynamics has been widely studied in both frequency domain [60]–[62] and time domain [63]–[65]. The general consensus is that the current harmonics at multiples of switching frequency are responsible for self-balance. These harmonics are the result of capacitor voltage imbalance, and will act to counteract the imbalance by dissipating power through the series resistance of the circuit. As a result, the capacitor voltages converge to their nominal values. This self-balancing property can offset the adverse effect of the non-idealites and the disturbances in the circuits. Yet, its strength depends on a number of factors, including duty ratio, inductor and load resistor values, switching frequency and more. To improve the natural balancing strength, passive RLC balance booster [61] or alternative modulation schemes [65] can be used at the cost of additional power loss and implementation complexity.

Compared to the study of balancing theories and techniques, the sources of the disturbances that cause capacitor imbalance have not been extensively investigated in past works. It is of great interest to understand the physical origins of the non-idealities responsible for capacitor voltage imbalance so that they can be eliminated or reduced by design. This way, high-density and naturally-balanced FCML converters can be made, facilitating a wider adoption of such topology. In this chapter, a number of practical factors that introduce capacitor voltage imbalance are investigated experimentally, and the corresponding mitigation strategies are presented.

In Section 4.2, the operating principle of FCML converters is briefly reviewed. In Section 4.3, the effect of source impedance and input capacitance are studied and found to have a strong influence on capacitor balancing. Moreover, we demonstrate in theory and with experimental results that an FCML converter with an even number of levels has significantly stronger immunity to voltage-type disturbances (such as input voltage ripple) than one with an odd number of levels. In Section 4.4, we show that the slight difference in gate drive

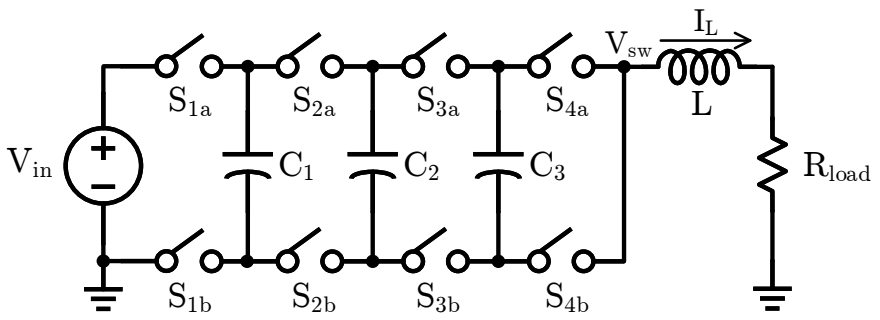


Figure 4.1: Schematic drawing of a five-level FCML buck converter.

supply voltage can cause mismatch of the gate signal propagation delays, and thus lead to capacitor imbalance. To minimize the delay mismatch, a modified cascaded bootstrap circuit is designed, which can supply equal voltages to all gate drivers and improve capacitor voltage balancing. In addition, we also experimentally show that the variation in switch on-resistance has a relatively small impact on the capacitor voltage balancing.

4.2 Operating Principle of FCML Converters

In an N-level FCML converter with an input voltage V_{in}, there are $(N-1)$ pairs of switches and $(N-2)$ flying capacitors with voltage ratings of $\frac{V_{\text{in}}}{N-1}$, $\frac{2V_{\text{in}}}{N-1}$, ..., $\frac{(N-2)V_{\text{in}}}{N-1}$, respectively. With phase-shifted pulse-width modulation (PSPWM) [58], the $(N-1)$ pairs of switches turn on and off with a phase shift of $\frac{360}{(N-1)}$ degrees, creating $(N-2)$ intermediate voltage levels. Therefore, the filter inductor has less voltage ripple ($\frac{V_{\text{in}}}{N-1}$) at increased pulse frequency ($(N-1)f_{\text{sw}}$), resulting in significantly reduced size. Moreover, since the switch voltage stress is the difference between the voltages of adjacent capacitors, each switch has an ideal voltage rating of $\frac{V_{\text{in}}}{N-1}$.

The schematic drawing of an example five-level FCML buck converter is shown in Fig. 4.1. The top side "a" switches have a duty ratio of D, the complementary "b" switches at the bottom side have a duty ratio of $(1-D)$, and the output voltage is given by $V_{\text{out}} = DV_{\text{in}}$. Figure 4.2 shows the gate signals of the "a" switches, the switch node voltage and the inductor current of the five-level converter operating at $D = \frac{5}{8}$. It can be seen that each switch has a phase lag of 90° from the previous one. This modulation technique creates 8 sub-circuits within one switching period as shown in Fig. 4.2. Assuming the flying capacitors have balanced voltages at their nominal values, $V_{C1} = \frac{3V_{\text{in}}}{4}$, $V_{C2} = \frac{V_{\text{in}}}{2}$ and $V_{C3} = \frac{V_{\text{in}}}{4}$, then the switch node alternates between $\frac{V_{\text{in}}}{2}$ and $\frac{3V_{\text{in}}}{4}$, at four times of the switching frequency. This reflects a significant reduction in the applied volt-seconds across the inductor, compared to a two-level converter switching between ground and V_{in}.

In practical implementations, the flying capacitor voltages can often deviate from their nominal values due to various reasons. This can result in unbalanced switch node voltage,

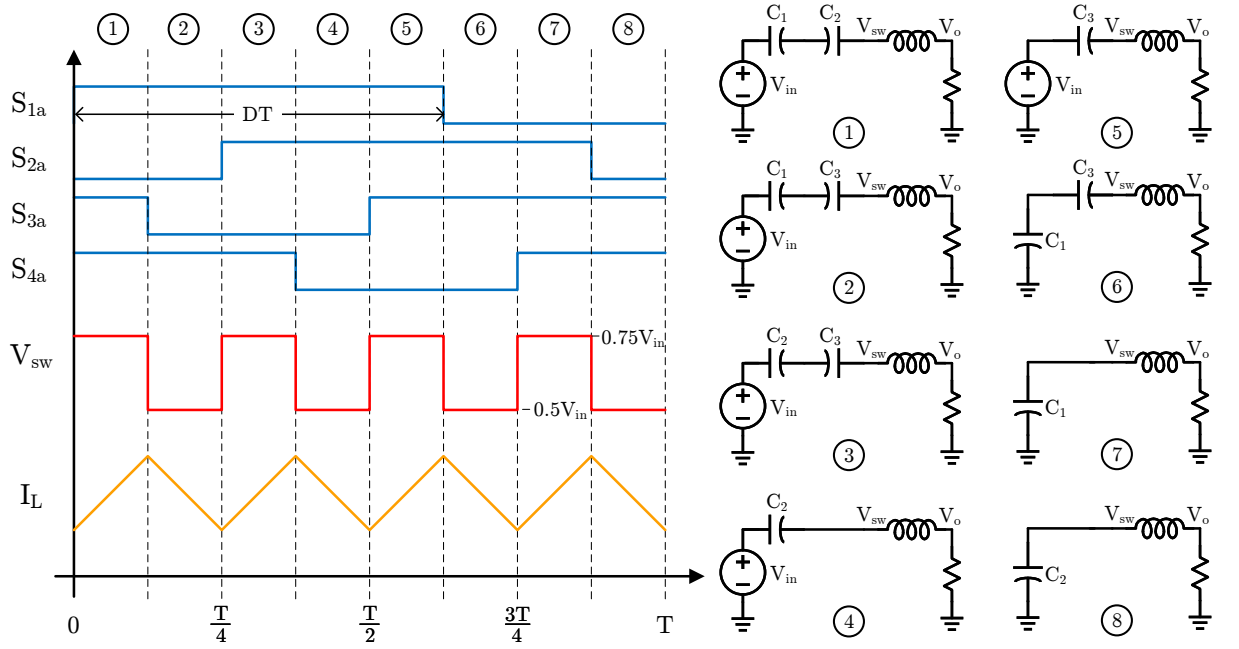


Figure 4.2: PWM, switch node voltage, and inductor current waveforms of a five-level FCML buck converter at $\frac{1}{2} < D < \frac{3}{4}$.

increased current ripple and assoicated loss on the inductor. More importantly, this can lead to an increased drain-to-source voltage stress across the switches. To isolate and study the various disturbances individually, an FCML converter testbed with flexible configuration capability (3/4/5-level, gate drive voltage, switch selection) is designed and built. Its schematic drawing is shown in Fig. 4.3 and an annotated hardware photograph is shown in Fig. 4.4. Since the focus is on steady-state capacitor voltage variations rather than balancing dynamics, dc/dc tests are performed. However, the results can also be informative to ac/dc and dc/ac cases as they can be viewed as dc/dc operations with slowly varying duty ratios

4.3 Imbalance Caused by Source Impedance

In prior capacitor balancing works, the input is treated as an ideal voltage source [60]–[62], [64], [65]. However, as shown in Fig. 4.3, there is usually a large and mainly inductive source impedance Z_{in} between the input voltage source V_{DC} and the actual converter input V_{in} in practical implementations. This results in a triangular-shape input voltage ripple whose magnitude ($\Delta V_{\text{in}} = \frac{D(1-D)I_{\text{out}}}{C_{\text{in}} f_{\text{sw}}}$) is partly determined by the amount of low-ESR low-ESL input capacitors that are placed close to the converter input. It is found that this ripple can cause capacitor voltage imbalance, and its effect is significantly more drastic if the FCML

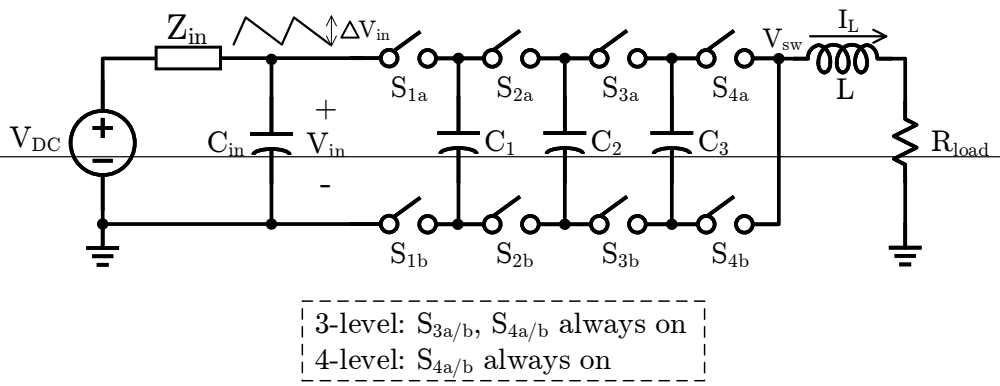


Figure 4.3: Schematic drawing of the configurable 3/4/5-level FCML buck converter prototype. There is a source impedance Z_{in} between the input voltage source V_{DC} and the actual converter input V_{in}. The magnitude of the input voltage ripple ΔV_{in} is determined by the low-ESR low-ESL input capacitor.

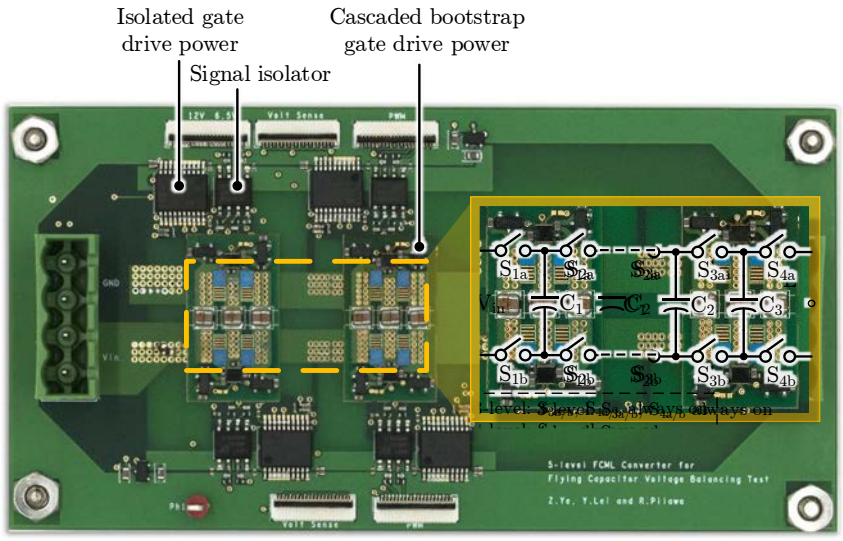


Figure 4.4: Photograph of the configurable 3/4/5-level FCML buck converter prototype.

converter has an odd number of levels.

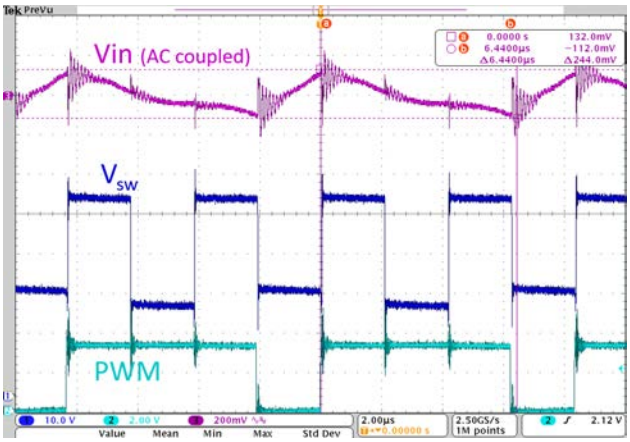


Figure 4.5: Measured input voltage ripple of a three-level FCML converter.

The Three-Level Case

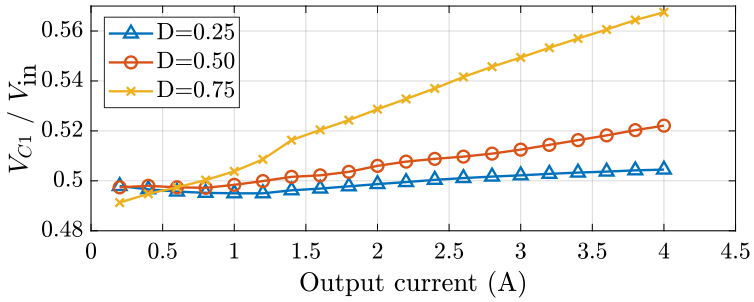
Experiment

An FCML buck converter prototype with flexible configuration capability (3/4/5-level) is implemented as shown in Fig. 4.4. The flying capacitor voltage of the FCML prototype operating as a three-level converter (schematic shown in Fig. 4.3) is measured with different input capacitance. The prototype uses 100 V EPC2016C GaN switches, and is operated with 50 V input voltage, 120 kHz switching frequency, 10 μF flying capacitor, 1 μH filter inductor, and up to 4 A output current. There is a source impedance owing to the twisted wire pairs between the power supply and the input of the prototype.

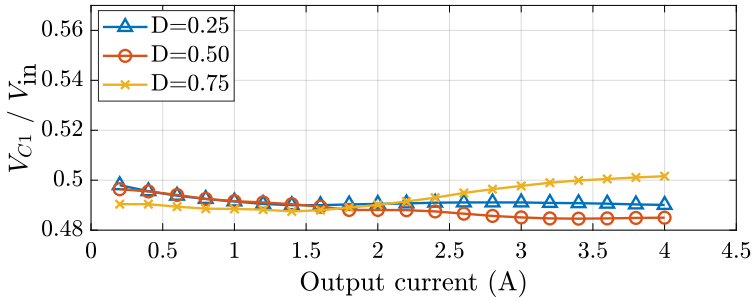
The triangular-shape input voltage ripple can be observed in Fig. 4.5. Figure 4.6a shows the normalized flying capacitor voltage (V_{C1}/V_{in})with 13 μF of input capacitance (X7R ceramic, after dc bias derating). It can be seen that the capacitor voltage quickly deviates from its nominal value ($V_{C1}/V_{\text{in}} = 0.5$) when the duty ratio and output current increase. In comparison, as shown in Fig. 4.6b, the balancing improves dramatically when the input capacitance increases to 65 μF. Note that the balancing performance can be further improved by eliminating the gate signal delay mismatch, which will be discussed in Section 4.4.

Theoretical Analysis

Here, we perform a time-domain analysis to explain this phenomenon. The FCML converter of Fig. 4.3 is configured with S_{3a}, S_{3b}, S_{4a} and S_{4b} are all shorted, thereby generating a three-level converter. The circuit states of the three-level converter operating in CCM mode (inductor current does not go negative) at $D > 0.5$ (where D is the duty ratio) and the corresponding waveforms are shown in Fig. 4.7. For ease of illustration, large flying capacitors are assumed here such that the capacitor voltage ripple is negligible. In the case where the input is an ideal voltage source ($Z_{\text{in}} = 0$), the switch node waveform (V_{sw} in Fig. 4.7) will be



(a) $C_{\text{in}} = 13\ \mu\text{F}$



(b) $C_{\text{in}} = 65\ \mu\text{F}$

Figure 4.6: Measured flying capacitor voltage of a three-level FCML converter.

a rectangular pulse wave between V_{DC} and $\frac{1}{2}V_{\text{DC}}$. In practice, if we consider the triangular-shape input voltage ripple that would result from a non-negligible source impedance, the actual switch node voltage (V_{sw} labeled with large Z_{in} in Fig. 4.7) will be higher than V_{DC} in state 1, but lower than V_{DC} in state 3. As a result, the inductor sees different voltages in these two states, and the corresponding current slopes will be different. This leads to a higher capacitor charging current in state 2, assuming the converter has ideal initial conditions (e.g. balanced capacitor voltage). Consequently, the net charge into the capacitor over one complete switching cycle will be positive. This results in a flying capacitor voltage increase, which matches the experimental results. Note that this analysis does not apply to the $D < 0.5$ case. In general, when an FCML converter operates at its bottom operating region (V_{sw} is between ground and $\frac{V_{\text{in}}}{N-1}$ for a N-level converter), the input voltage source only connects to the rest of the circuit for one sub-period, and thus on average it has negligible effect to the switch node voltage and capacitor balancing. It can be seen from Fig. 4.6a that, even with insufficient C_{in} (therefore relatively large input voltage ripple), the three-level converter can still have a relatively good balancing for $D = 0.25$.

The above graphical interpretation can also be formulated for more general analysis. To capture the capacitor charge/discharge behaviors, all of the operating states within a switching cycle are analyzed in sequence. As can be inspected from Fig. 4.7, state 1 and 3

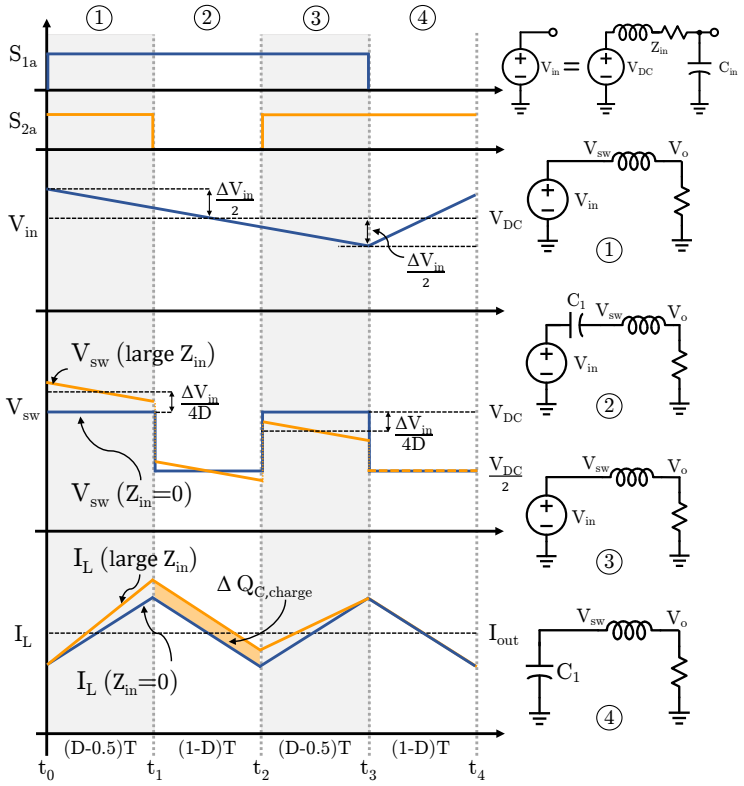


Figure 4.7: The flying capacitor voltage of a three-level FCML converter will increase in the presence of input voltage ripple.

have the same duration of $d_1 = (D - 0.5)$, whereas state 2 and 4 have $d_2 = (1 - D)$. Here we take ΔV_{C_1} as the state variable, which is defined as the deviation of the flying capacitor voltage from its nominal value:

$$\begin{aligned} \Delta V_{C_1} &= V_{C_1} - V_{C_1,\text{nominal}} \\ &= V_{C_1} - \frac{V_{\text{in}}}{2}. \end{aligned} \tag{4.1}$$

Since ΔV_{C_1} is determined by the net charge flowing through the capacitor, the standard inductor volt-second analysis can be performed to determine the current flow and thereby ΔV_{C_1}. As can be seen in Fig. 4.7, the voltage across the inductor is the difference between V_{sw} and $V_o = DV_{\text{in}}$. When the triangular-shape input voltage ripple is considered (whose peak-to-peak amplitude is ΔV_{in}), the switch node voltage V_{sw} will also experience the same amount of ripple. Through geometric calculation, it can be shown that V_{sw} will be higher than the ideal case by $\frac{\Delta V_{\text{in}}}{4D}$ (on average) in state 1, and lower by $\frac{\Delta V_{\text{in}}}{4D}$ in state 3. Therefore

we can write the inductor voltage in each state as

$$\begin{cases} V_{L1} = (1-D)V_{\text{in}} + \dfrac{\Delta V_{\text{in}}}{4D} \\ V_{L2} = (1-D)V_{\text{in}} - V_{C_1} \\ V_{L3} = (1-D)V_{\text{in}} - \dfrac{\Delta V_{\text{in}}}{4D} \\ V_{L4} = V_{C_1} - DV_{\text{in}} \end{cases} \tag{4.2}$$

Then the peak and valley inductor current in each switching interval can be calculated using volt-second balance on the inductor. This results in

$$\begin{cases} i(t_1) = i(t_0) + V_{L1}d_1T/L \\ i(t_2) = i(t_1) + V_{L2}d_2T/L \\ i(t_3) = i(t_2) + V_{L3}d_1T/L \\ i(t_4) = i(t_3) + V_{L4}d_2T/L \end{cases} \tag{4.3}$$

Since capacitor C_1 is charged in state 2 and discharged in state 4, the average charging and discharging current can be found as

$$I_{C_1,\text{charge}} = \frac{i(t_1) + i(t_2)}{2} \tag{4.4}$$

$$I_{C_1,\text{discharge}} = \frac{i(t_3) + i(t_4)}{2} \tag{4.5}$$

And finally, by using

$$\Delta I_{C_1} = I_{C_1,\text{charge}} - I_{C_1,\text{discharge}} \tag{4.6}$$

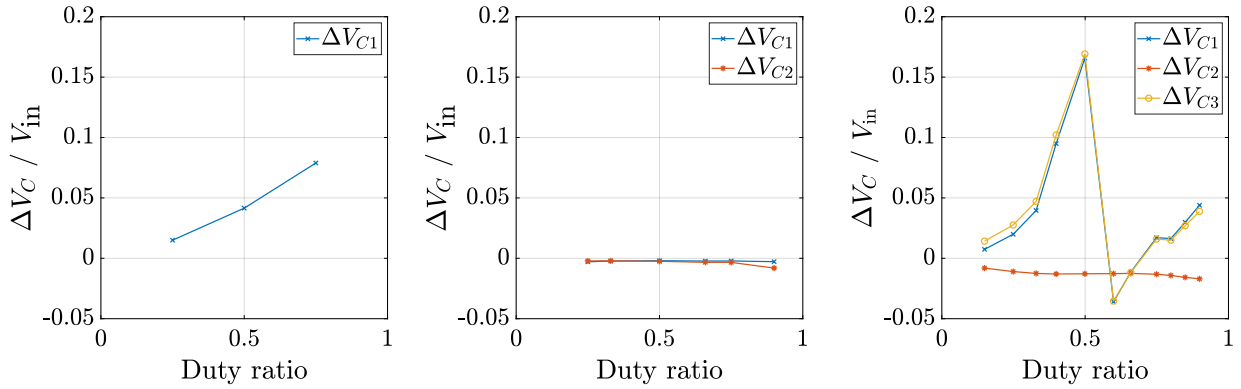
$$= C_1 \frac{d\Delta V_{C1}}{dt} = C_1 \Delta \dot{V}_{C1} \tag{4.7}$$

to combine all of the above equations together, we then get:

$$\Delta \dot{V}_{C1} = 0 \cdot \Delta V_{C1} + \frac{(2D-1)T}{8DLC_1} \cdot \Delta V_{\text{in}}. \tag{4.8}$$

It indicates that for the case considered here ($D > 0.5$), the voltage on C_1 will keep increasing in the presence of input voltage ripple, if the three-level FCML converter is ideal and lossless. In practice, a natural-balancing mechanism will try to counteract this effect and limit the capacitor voltage deviation. The general consensus is that the current harmonics at multiples of switching frequency are responsible for self-balance. These harmonics are the result of capacitor voltage imbalance, and will act to counteract the imbalance by dissipating power through the parasitic resistance of the circuit [60]–[65]. To quantitatively predict the boundary of capacitor deviation, a methodology with combined continuous and discrete state-space analysis is presented in [66], which analyzes the equivalent LCR circuit of each sub-circuit within a switching period.

The Four-Level and Five-Level Cases



(a) three-level (b) four-level (c) five-level

Figure 4.8: Measured flying capacitor voltage variations ($C_{\text{in}} = 13\ \mu$F, $I_{\text{out}} = 4$ A).

To further investigate the effect of source impedance on capacitor balancing, the FCML converter testbed is then configured to four-level mode and five-level mode, respectively. Fig. 4.8 compares the balancing performance ($\Delta V_C = V_{C,\text{actual}} - V_{C,\text{nominal}}$) of the three possible configurations under the same operating conditions. It can be seen that at this small-input-capacitance high-load-current condition, the capacitor voltage deviation ΔV_C of the three-level mode and the five-level mode can be as high as 8% and 18% of V_{in}, respectively. In comparison, the four-level mode shows near perfect capacitor balancing, with a maximum ΔV_C of 0.8% V_{in}. To understand this unique behavior, we extend the preceeding state-space method to four-level and five-level cases.

State-Space Analysis

The system equations of the FCML converter under the influence of input voltage ripple are listed in (4.9) - (4.11) for three-level, four-level and five-level cases, respectively. The system parameters of (4.10) and (4.11) are tabulated in Table 4.1 and Table 4.2, where T is the switching period and C_i stands for the flying capacitor in its corresponding row. As discussed in the previous subsection, the very low duty ratio region (where V_{sw} switches between ground and $\frac{V_{\text{in}}}{N-1}$) is not considered in this analysis, since the input voltage ripple has less effect on capacitor balancing at this region.

$$\underbrace{\Delta\dot{V}_{C1}}_{\dot{\mathrm{x}}} = \underbrace{0}_{A} \cdot \underbrace{\Delta V_{C1}}_{\mathrm{x}} + \underbrace{\frac{(2D-1)T}{8DLC_1}}_{B} \cdot \underbrace{\Delta V_{\text{in}}}_{u} \tag{4.9}$$

$$\underbrace{\begin{bmatrix}\Delta\dot{V}_{C1}\\ \Delta\dot{V}_{C2}\end{bmatrix}}_{\dot{\mathrm{x}}} = \underbrace{\begin{bmatrix}0 & \mathrm{a}_1\\ -\mathrm{a}_2 & 0\end{bmatrix}}_{A} \cdot \underbrace{\begin{bmatrix}\Delta V_{C1}\\ \Delta V_{C2}\end{bmatrix}}_{\mathrm{x}} + \underbrace{\begin{bmatrix}\mathrm{b}\\ 0\end{bmatrix}}_{B} \cdot \underbrace{\Delta V_{\mathrm{in}}}_{u} \tag{4.10}$$

$$\underbrace{\begin{bmatrix}\Delta\dot{V}_{C1}\\ \Delta\dot{V}_{C2}\\ \Delta\dot{V}_{C3}\end{bmatrix}}_{\dot{\mathrm{x}}} = \underbrace{\begin{bmatrix}0 & \mathrm{a}_1 & 0\\ -\mathrm{a}_2 & 0 & \mathrm{a}_2\\ 0 & -\mathrm{a}_3 & 0\end{bmatrix}}_{A} \underbrace{\begin{bmatrix}\Delta V_{C1}\\ \Delta V_{C2}\\ \Delta V_{C3}\end{bmatrix}}_{\mathrm{x}} + \underbrace{\begin{bmatrix}\mathrm{b}_1\\ \mathrm{b}_2\\ \mathrm{b}_3\end{bmatrix}}_{B} \cdot \underbrace{\Delta V_{\mathrm{in}}}_{u} \tag{4.11}$$

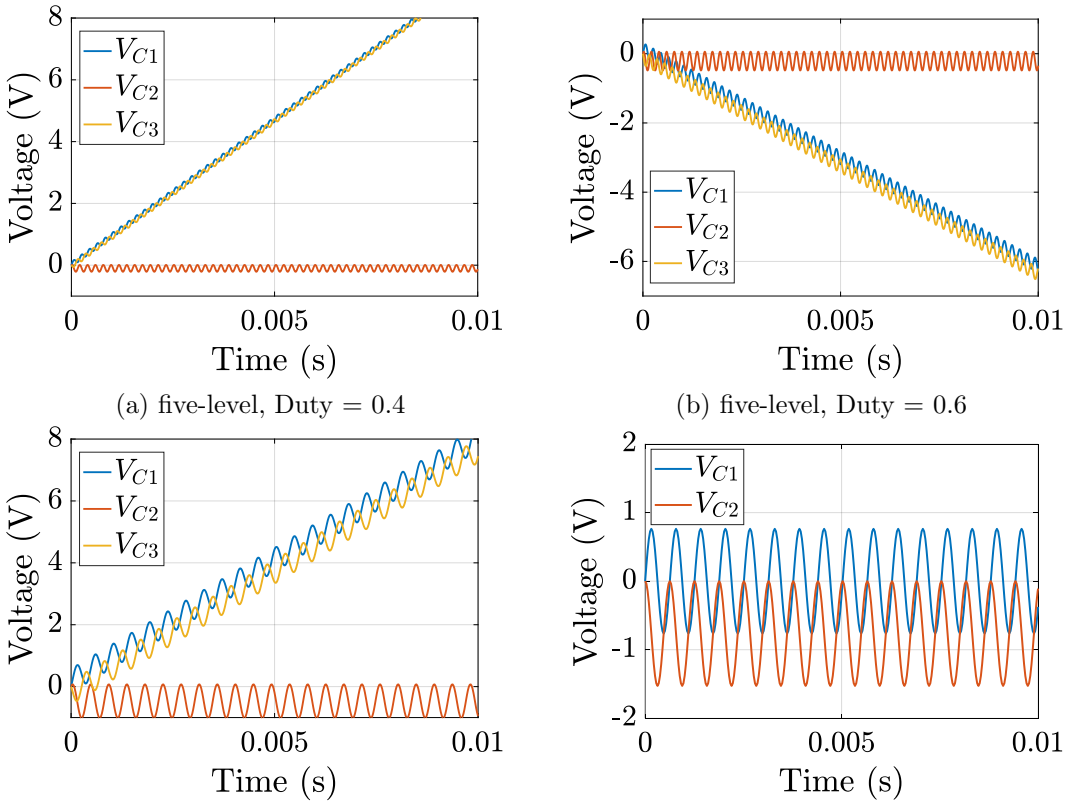
Table 4.1: Four-level converter system parameters

Duty	(0.33, 0.66)	(0.66, 1)
$\mathrm{a_i}$	$\frac{(-6D^2+6D-1)T}{2LC_i}$	$\frac{(1-D)T}{2LC_i}$
b	$\frac{(-3D^2+4D-1)T}{12DLC_1}$	$\frac{(9D-5)T}{36DLC_1}$

Table 4.2: Five-level converter system parameters

Duty	(0.25, 0.5)	(0.5, 0.75)	(0.75, 1)
$\mathrm{a_i}$	$\frac{(-8D^2+8D-1)T}{4LC_i}$	$\frac{(-8D^2+8D-1)T}{4LC_i}$	$\frac{(1-D)T}{2LC_i}$
b_1	$\frac{(-16D^2+16D-3)T}{64DLC_1}$	$\frac{(-16D^2+24D-7)T}{64DLC_1}$	$\frac{(8D-5)T}{32DLC_1}$
b_2	$\frac{(16D^2-8D+1)T}{64LC_2}$	$\frac{(-48D^2+64D-19)T}{64DLC_2}$	$\frac{T}{32DLC_2}$
b_3	$\frac{(-16D^2+8D-1)T}{64LC_3}$	$\frac{(48D^2-64D+19)T}{64DLC_3}$	$\frac{-T}{32DLC_3}$

It can be observed from (4.9) - (4.11) that the FCML converter has a uniform system equation structure, which will be generalized to N-level in the next subsection. However, due to the unique characteristics of the A matrix, it is singular for three-level and five-level as their determinants are zero. It indicates that (4.9) and (4.11) have no steady-state solution unless the input u is zero. In other words, due to the input voltage ripple, the capacitor voltage will continue to diverge in this lossless system. The simulated step responses of the five-level case are shown in Fig. 4.9a to 4.9c. It predicts that, while the voltage on capacitor C_2 stay close to its nominal value, the voltages on C_1 and C_3 will increase continuously when $D \in (0.25, 0.5)$ and $(0.75, 1)$, and will decrease continuously when $D \in (0.5, 0.75)$. In practice, the system is not lossless, and the series resistance in the circuit will act to bring the capacitor voltages back



(a) five-level, Duty = 0.4

(b) five-level, Duty = 0.6

(c) five-level, Duty = 0.8

(d) four-level, Duty = 0.8

Figure 4.9: Simulated step response of the flying capacitor voltages using the proposed models (ΔV_{in} is the input).

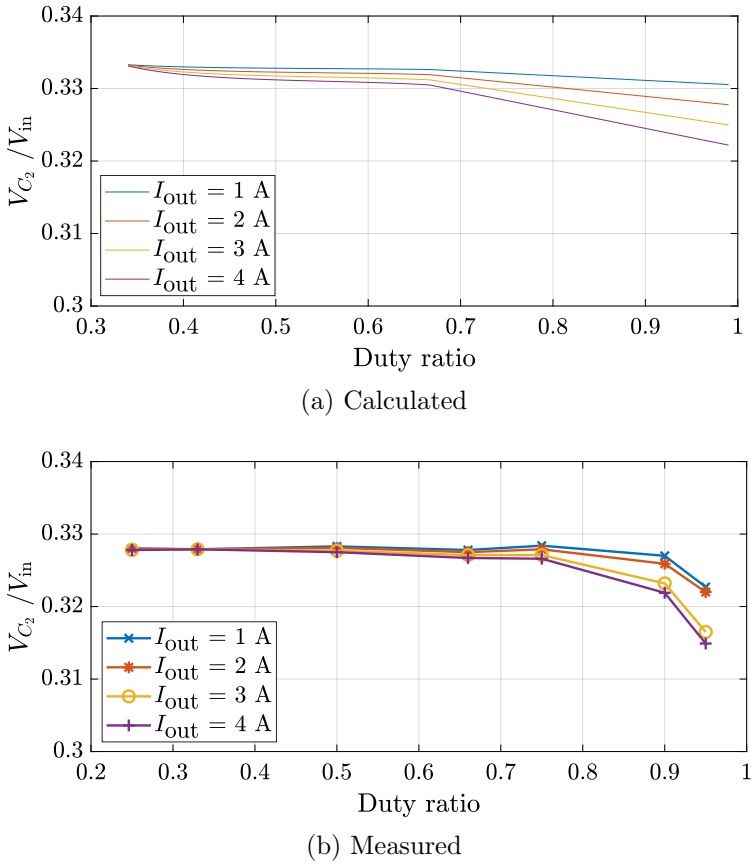
towards their nominal values, through the natural balancing property discussed in existing literature [60]–[65]. Nevertheless, the natural balancing strength depends on a number of factors, and it can often times be limited.

In contrast, a four-level FCML converter can have significantly stronger immunity to the input ripple disturbance. Although the form of (4.10) looks similar to that of (4.9) and (4.11), the determinant of its A matrix is nonzero. In this case, steady-state solutions exist for the four-level converter, and they are found as:

$$\Delta V_{C1} = 0 \tag{4.12}$$

$$\Delta V_{C2} = \begin{cases} \frac{-3D^2+4D-1}{6D(6D^2-6D+1)} \cdot \Delta V_{\text{in}} & D \in (0.33, 0.66) \\ \frac{5-9D}{18D(1-D)} \cdot \Delta V_{\text{in}} & D \in (0.66, 1) \end{cases} \tag{4.13}$$

This indicates that, under the influence of the input voltage ripple, the voltage on capacitor C_1 will stay at its nominal value (0.66 V_{in}) and the voltage on C_2 (nominal value: 0.33 V_{in})



(a) Calculated

(b) Measured

Figure 4.10: Capacitor voltage variation of a four-level FCML converter under the influence of input voltage ripple.

will be disturbed by a fraction of ΔV_{in}. This can also be observed from the step response of the system, which is plotted in Fig. 4.9d.

Given fixed input capacitance and switching frequency ($C_{\text{in}} = 13\ \mu$F, $f_{\text{sw}} = 120$ kHz in this example), the input voltage ripple can be calculated with respect to the duty ratio and the output current, using $\Delta V_{\text{in}} = \frac{D(1-D)I_{\text{out}}}{C_{\text{in}} f_{\text{sw}}}$. Then the variation of V_{C2}, due to ΔV_{in}, can be derived using (4.13), as plotted in Fig. 4.10a. It can be seen that C_2 remains near-perfect balancing when $D \in (0.33, 0.66)$, regardless of the magnitude of I_{out} and the corresponding ΔV_{in}. For $D \in (0.66, 1)$, the capacitor voltage decreases linearly with a slope determined by I_{out} (also affected by C_{in} and f_{sw}). Nevertheless, even with the small input capacitance in this example, V_{C2} only drops by 1.4% V_{in} at heavy load and extreme duty ratio, reflecting satisfactory capacitor balancing.

In order to understand the reason for this different behavior, a graphical illustration is presented in Fig. 4.11. As in the three-level case, in the presence of input voltage ripple, the switch node voltage is disturbed and will therefore change the slope of the inductor current. However, the difference is that after the voltage of C_2 deviates by an amount calculated

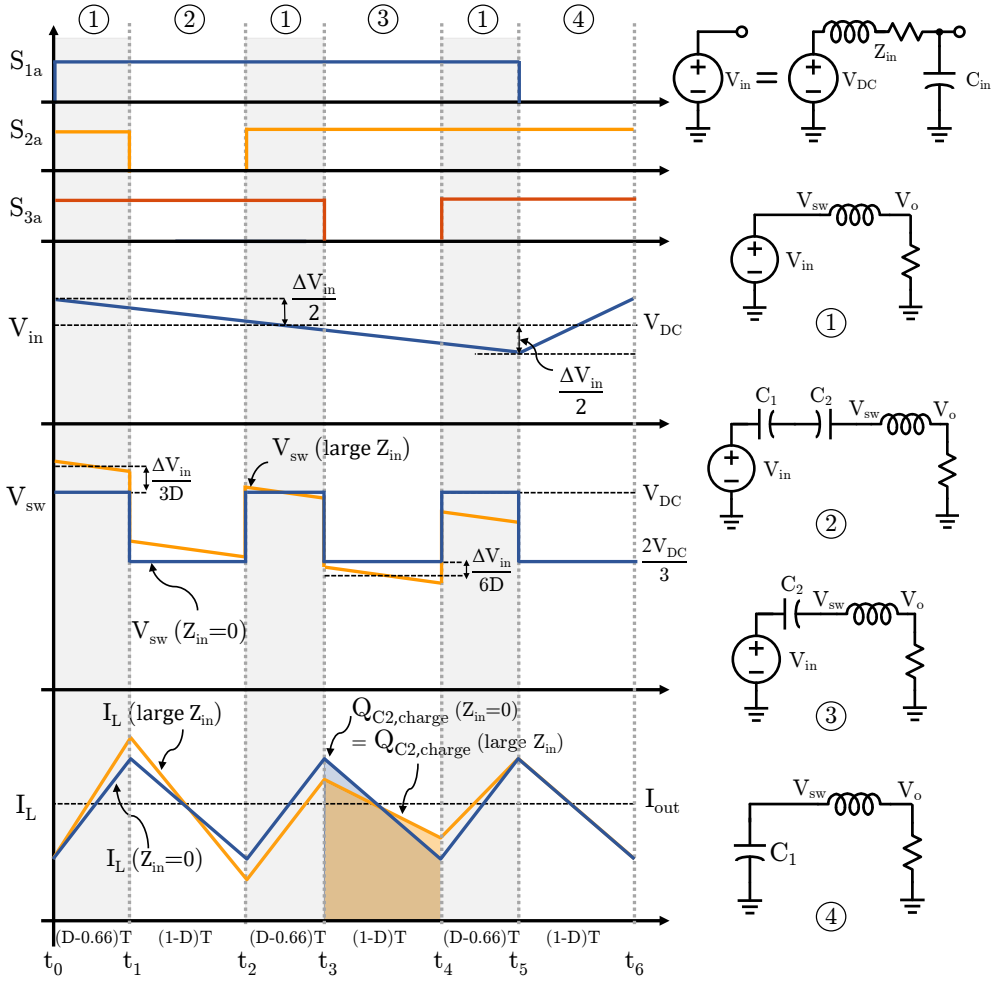
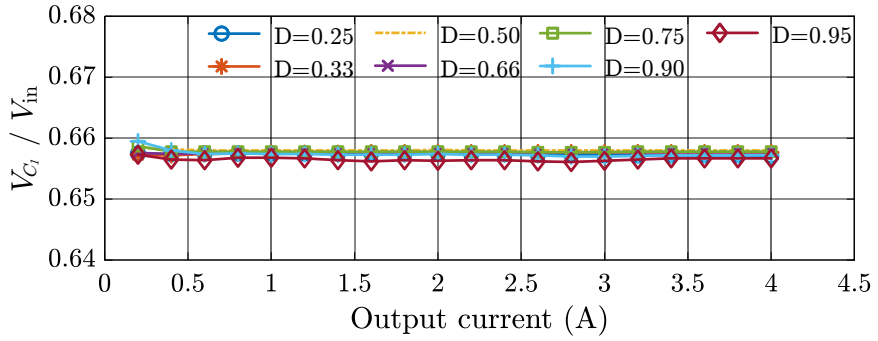


Figure 4.11: The flying capacitor voltages of a four-level FCML converter can stabilize themselves in the presence of input voltage ripple.

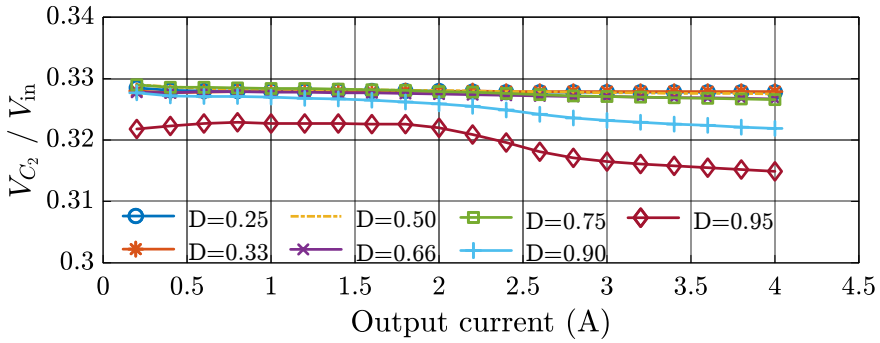
in (4.13), the inductor current will have the same average value as that of the ideal case ($Z_{\text{in}} = 0$) in state 2 and 3, resulting in zero net charge on C_1 and C_2 per switching cycle. It indicates that the capacitor voltages are balanced to this point without further deviation. Even though this analysis assumes the FCML system is ideal and lossless, the capacitors here are able to stabilize themselves regardless, without the help of the natural balancing mechanism through parasitic resistance.

Experimental Results

To verify the theory above, the prototype is first configured to a four-level FCML converter with 13 μF input capacitance. Figure 4.10b shows the voltage of capacitor C_2 with respect to duty ratio. As predicted, V_{C2} maintains its nominal value for the majority of the duty



(a) Flying capacitor C_1



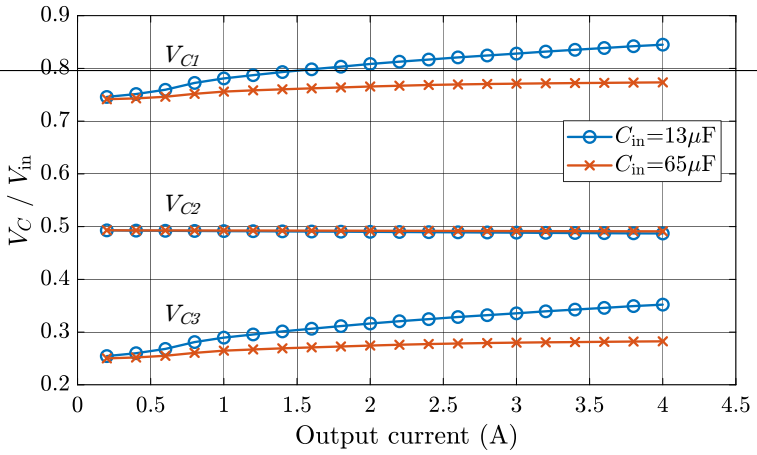
(b) Flying capacitor C_2

Figure 4.12: Measured flying capacitor voltages of a four-level FCML covnerter ($C_{\text{in}} = 13$ μF).

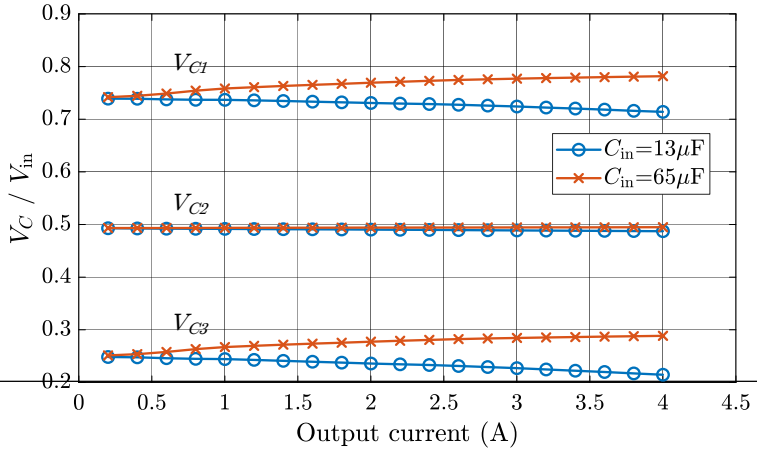
ratios, but starts to decrease at heavy load when $D > 0.9$, which is in good agreement with Fig. 4.10a. It can also be seen from Fig. 4.12 that while C_2 experiences a small amount of voltage deviation at extreme cases, C_1 can stay close to its nominal value over the full load range for all duty ratios. Considering the small input capacitance used in this test, we conclude that a four-level converter has outstanding self-balancing performance regardless of the input voltage disturbance.

Similar experimental validation was performed with the prototype configured as a five-level converter. At $D = 0.4$, the input voltage ripple causes V_{C1} and V_{C3} to drift up. Although the natural balancing property strives to bring the capacitor voltages back, its effectiveness is limited and large voltage deviation can be observed from the blue line in Fig. 4.13a. With larger input capacitance, ΔV_{in} is reduced, leading to the reduced imbalance (red line) in Fig. 4.13a. The experimental result shown in Fig. 4.13b for $D = 0.6$ also agrees with the prediction of the step response (V_{C1} and V_{C3} decrease due to ΔV_{in}, V_{C2} remains at its nominal value).

The measured V_{C1} across the entire duty ratio range is shown in Fig. 4.14. Even though greater input capacitance can help improve capacitor balancing, the system can still be very unbalanced when the duty ratio is close to 0.5. This is because PSPWM cannot guarantee



(a) Duty = 0.4



(b) Duty = 0.6

Figure 4.13: Measured flying capacitor voltages of a five-level FCML converter.

natural balancing for a five-level converter at this region, due to the inefficient use of redundant states [64], [65]. As shown in Fig. 4.15, there are six possible circuit configurations that can generate the $\frac{1}{2}V_{\text{in}}$ voltage level, whereas the PSPWM only utilizes the first four states, in which C_1 and C_3 are always connected with opposite polarities. As a result, they only need to maintain a fixed voltage difference of $\frac{1}{2}V_{\text{in}}$ but their absolute values are unconstrained. In [67], an alternative modulation technique which uses more redundant states (state 5 and 6 in Fig. 4.15) has been proposed to improve the balancing performance.

The N-Level Case

Next, we generalize the state-space analysis in the last subsection to an FCML converter with any number of levels N (and with $n = N - 2$ flying capacitors), and show that an

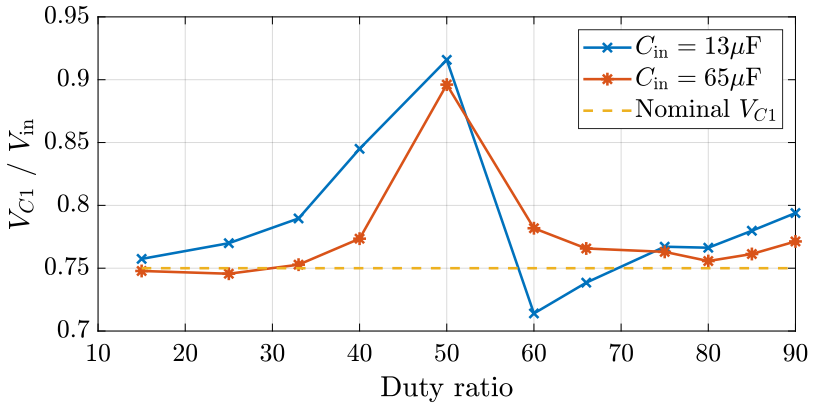


Figure 4.14: Measured C_1 voltage of five-level FCML converter.

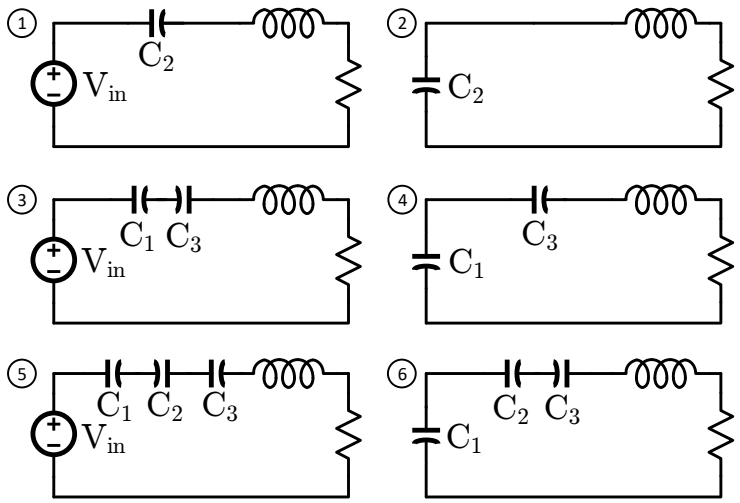


Figure 4.15: Six possible circuit configurations that can generate the $\frac{1}{2}V_{in}$ voltage level in a five-level FCML converter. PSPWM utilizes the first four states.

even-level converter can have fundamentally better immunity to voltage-type disturbances (e.g., input voltage ripple) than one with an odd number of levels. As demonstrated through (1) to (8), by analyzing the equivalent circuit of each sub-interval within one switching cycle, the piece-wise linear system can be modeled in state-space form as

$$\dot{\mathbf{v}} = A\mathbf{v} + B\mathrm{u} \tag{4.14}$$

where $\mathbf{v}$ is a column vector of the voltage variations of the flying capacitors from their nominal values

$$\mathbf{v} = \begin{bmatrix} \Delta V_{\mathrm{C1}} & \Delta V_{\mathrm{C2}} & \cdots & \Delta V_{\mathrm{Cn}} \end{bmatrix}^T. \tag{4.15}$$

The input u is a voltage-type disturbance, which can be either the input voltage ripple as analyzed in this work or any other type of voltage variation that is applied to the system. Regardless of the specific source of u, the A matrix reflects the intrinsic system characteristics and will remain the same as long as the timing of each sub-interval is accurate. To demonstrate the unique structure of the A matrix, we use

$$\Delta I_C = C\Delta\dot{V}_{\mathrm{C}} \tag{4.16}$$

to rearrange (4.14). By moving the flying capacitance terms in the denominators of A (as can be observed from Table 4.1 and Table 4.2) to the left side of the equation, $\dot{\mathbf{v}}$ becomes

$$\mathbf{i} = \begin{bmatrix} C_1\Delta\dot{V}_{\mathrm{C1}} & C_2\Delta\dot{V}_{\mathrm{C2}} & \cdots & C_{\mathrm{n}}\Delta\dot{V}_{\mathrm{Cn}} \end{bmatrix}^T \tag{4.17}$$

and the state-space equation now becomes

$$\mathbf{i} = A'\mathbf{v} + B'\mathrm{u} \tag{4.18}$$

with a system matrix A' of

$$A' = \begin{bmatrix} 0 & \mathrm{a}_{1,2} & \mathrm{a}_{1,3} & \cdots & \mathrm{a}_{1,\mathrm{n}-1} & \mathrm{a}_{1,\mathrm{n}} \\ \mathrm{a}_{2,1} & 0 & \mathrm{a}_{2,3} & \cdots & \mathrm{a}_{2,\mathrm{n}-1} & \mathrm{a}_{2,\mathrm{n}} \\ \mathrm{a}_{3,1} & \mathrm{a}_{3,2} & 0 & \cdots & \mathrm{a}_{3,\mathrm{n}-1} & \mathrm{a}_{3,\mathrm{n}} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ \mathrm{a}_{\mathrm{n}-1,1} & \mathrm{a}_{\mathrm{n}-1,2} & \mathrm{a}_{\mathrm{n}-1,3} & \cdots & 0 & \mathrm{a}_{\mathrm{n}-1,\mathrm{n}} \\ \mathrm{a}_{\mathrm{n},1} & \mathrm{a}_{\mathrm{n},2} & \mathrm{a}_{\mathrm{n},3} & \cdots & \mathrm{a}_{\mathrm{n},\mathrm{n}-1} & 0 \end{bmatrix}. \tag{4.19}$$

This A' can be further simplified to the form of

$$A' = \begin{array}{c} \\ j \\ \\ i \\ \\ \end{array} \begin{array}{c} \begin{array}{ccccc} & j & & i & \end{array} \\ \begin{bmatrix} \ddots & \vdots & & \vdots & \\ \cdots & 0 & \cdots & \mathrm{a}_{\mathrm{j,i}} & \cdots \\ & \vdots & \ddots & \vdots & \\ \cdots & \mathrm{a}_{\mathrm{i,j}} & \cdots & 0 & \cdots \\ & \vdots & & \vdots & \ddots \end{bmatrix} \end{array}. \tag{4.20}$$

The interpretation of the above system matrix A' is as follows: owing to the nature of PSPWM, there can be only one or two flying capacitors connected in series in the power loop at any time. During the time when two capacitors are connected in series, they share the same current with one being charged and the other being discharged. Therefore, for any two arbitrary flying capacitors C_{i} and C_{j} that are connected, we have

$$\mathrm{a}_{\mathrm{i,j}} = -\mathrm{a}_{\mathrm{j,i}}. \tag{4.21}$$

Since the focus is on the structure of the A' matrix, the detailed expression of $a_{i,j}$ is omitted here, but can be derived with the periodic steady-state volt-second analysis presented in Section 4.3 for each duty ratio range.

Furthermore, considering all of the states that C_{i} is connected in the circuit, it can be found that the voltage variation of C_{i} will not induce any net current on itself. Therefore, all of the diagonal terms in the square matrix are zero:

$$\mathrm{a_{i,i}} = 0. \tag{4.22}$$

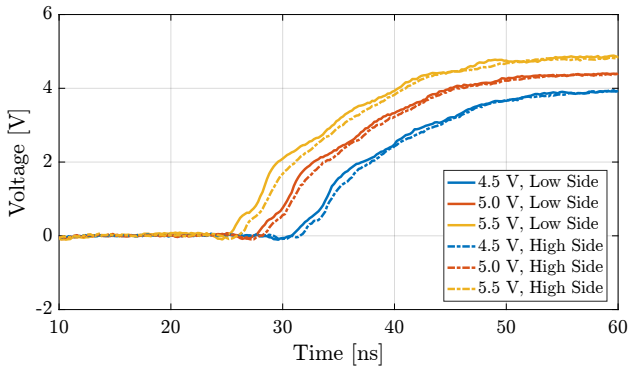
The above unique properties of FCML converter with PSPWM lead to the special structure of the A' in (4.20), which is a square matrix whose transpose equals its negative ($A'^T = -A'$). This is known as a skew-symmetric matrix, and a key property is that the determinant vanishes to zero if its rank n is odd. Thus, without considering the series resistance and the corresponding natural balancing mechanism, portions of the flying capacitors in an odd-level converter will continue to diverge if a disturbance is present, whereas an even-level converter can reach a steady-state value. This finding agrees with the 3/4/5-level analysis, and proves that an FCML converter with an even number of levels has fundamentally better immunity to disturbances than one with an odd number of levels. Note that at nominal duty ratios where $D = \frac{m}{n}$ ($m = 1, ..., n-1$), an even-level converter can also exhibit imbalance when m and n are not co-prime [68]. The good balancing performance of even-level converters have been demonstrated by recent six-level ac/dc work [69] and ten-level dc/ac work [70]. In addition, [70] also presents a control technique that can maintain good capacitor balancing during startup.

4.4 Imbalance Caused by Gate Driver Delay and Uneven Switch Resistance

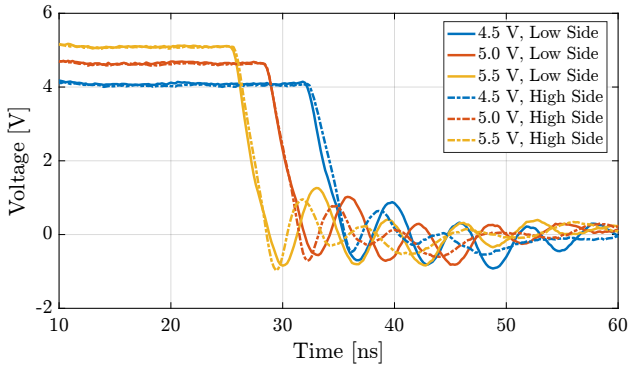
Gate Driver Delay Mismatch

In practical implementations of FCML converters, to reduce the complexity and footprint of the gate drive circuit, every two adjacent switches can be grouped into a pair and be driven by a half-bridge gate driver. The low-side switch of each half-bridge can be powered by an isolated power supply [71], and the high-side switch can be powered by the bootstrap method. Because of the forward drop of the bootstrap diode, the supply voltage of the high-side switch can be lower than that of the low-side by approximately $0.5 - 0.6$ V. It is found that this slight supply voltage difference between the low-side and high-side drivers can result in a mismatch of the gate signal propagation delay (from the input to the output of the gate driver). As a result, both the phase shift and the duty ratio of the control signals will be distorted, even with precise PWM generation.

The rising and falling edge propagation delays of TI LM5113 GaN half-bridge driver [72] are measured with different supply voltages, and the results are shown in Fig. 4.16. It is



(a) Rising edge delay after gate resistor



(b) Falling edge delay

Figure 4.16: Measured LM5113 gate driver propagation delay (from gate driver input to output).

found that in real scenarios where the low-side segment has a 5 V supply and the high-side segment has a 4.5 V supply, there is approximately an additional 7 ns turn-on delay and an additional 4 ns turn-off delay for the high-side driver.

To illustrate the effect of these additional delays, a time-domain analysis is performed. The circuit schematic is shown in Fig. 4.17 and the analytic waveforms are shown in Fig. 4.18. Compared to switch S_{2a} (driven by the low-side driver), both the turn-on and turn-off time of S_{1a} (driven by the high-side driver) will be delayed (by $t_{r,\text{delay}}$ and $t_{f,\text{delay}}$ in Fig. 4.18), resulting in a phase shift distortion. Since $t_{r,\text{delay}} > t_{f,\text{delay}}$, the duty ratio is also distorted, and both the capacitor charging time and the charging current will be less than their counterparts in the discharging state, leading to a capacitor voltage decrease. This effect can pose challenges to high-density designs that aim for high switching frequency and simple gate drive solutions. Note that the additional delay of the low-side switch S_{2b} over S_{1b} is not considered. This is due to the fact that the inductor current will naturally flow through the corresponding body diodes during deadtime and that the delay will not change the current path.

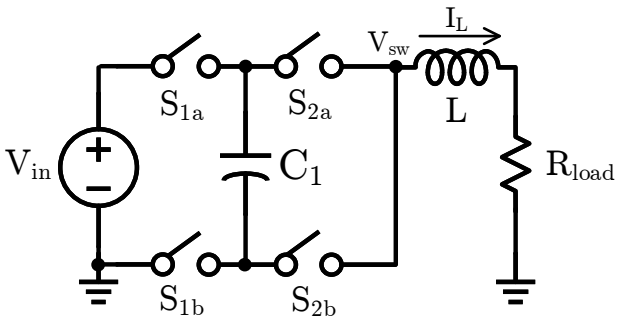


Figure 4.17: Schematic drawing of a three-level FCML buck converter.

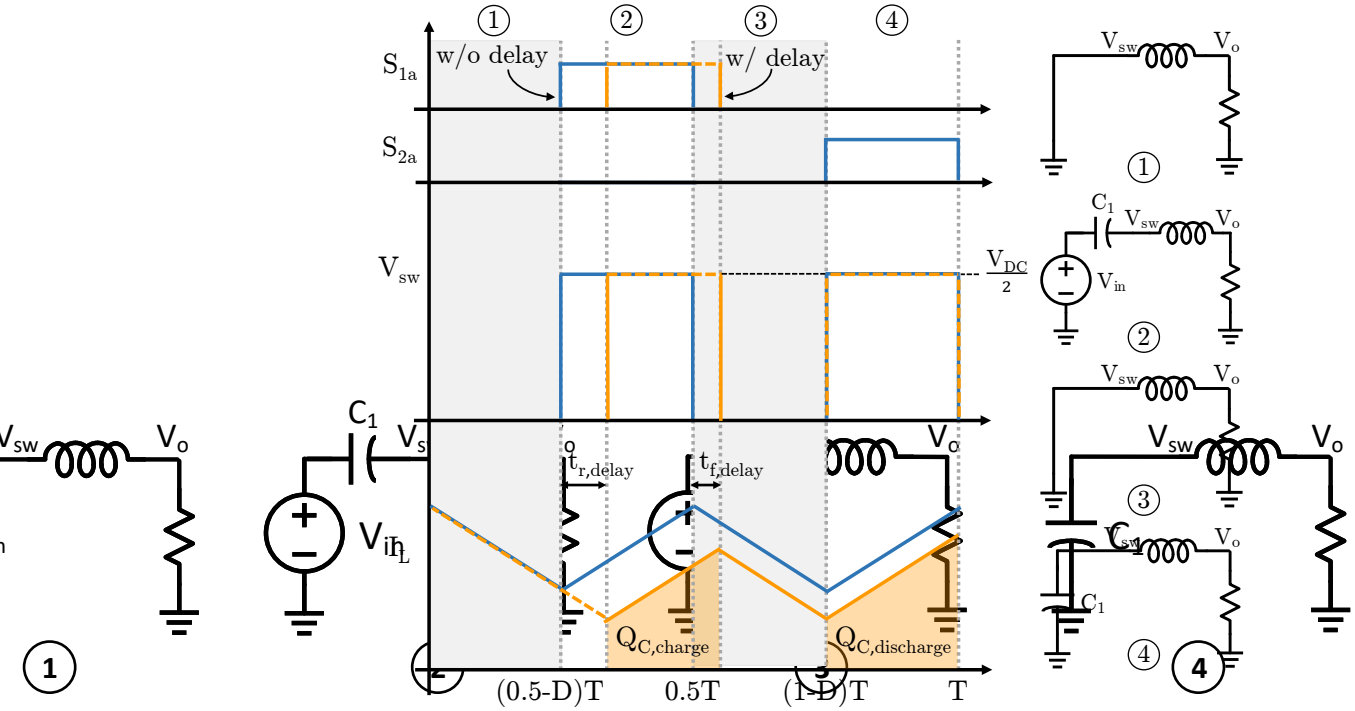


Figure 4.18: The effects of gate signal delay mismatch on capacitor balancing for a three-level FCML converter.

The previous experimental results shown in Fig. 4.6 are obtained with this kind of gate drive configuration. In order to eliminate the delay mismatch, a modified cascaded bootstrap circuit (as shown in Fig. 4.19) is designed to supply equal gate drive voltages to all of the gate drivers. The proposed circuit is discussed in more detail in Chapter 5, and is more efficient, compact and cost-effective than the isolated dc/dc solution. Another solution that can provide near equal gate drive voltages is the synchronous bootstrap method [73]. It

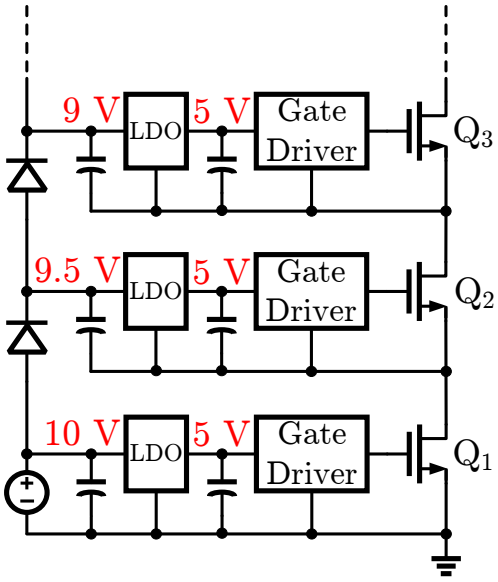


Figure 4.19: Schematic drawing of a cascaded bootstrap circuit.

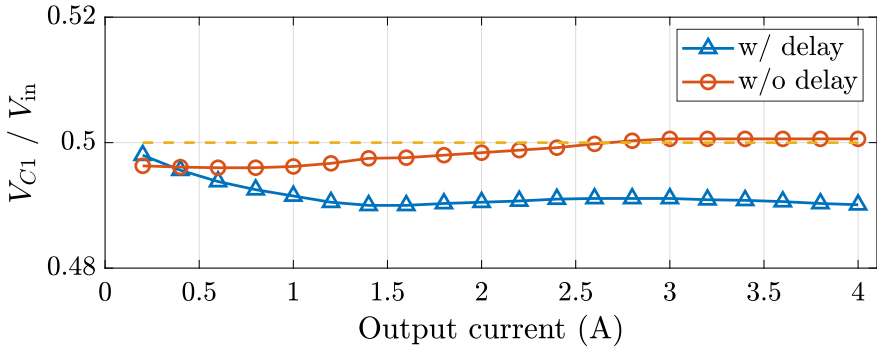
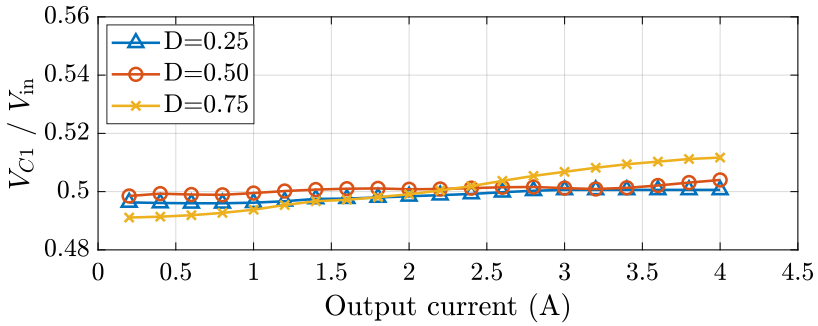


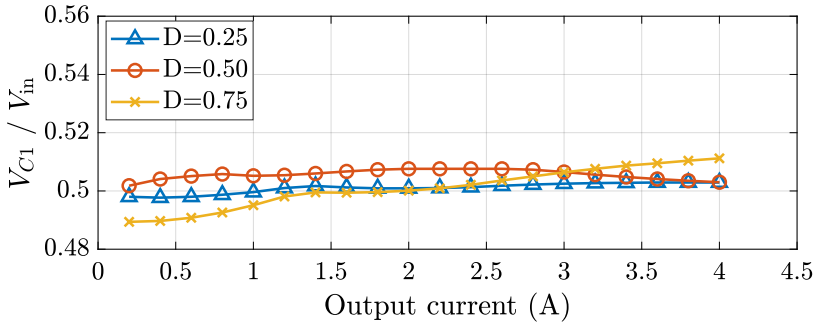
Figure 4.20: Measured effect of gate delay mismatch on capacitor voltage (three-level, $C_{in} = 65\ \mu F$, $D = 0.25$).

replaces the bootstrapping diode with an actively controlled switch, so that the voltage drop can be greatly reduced.

To validate the benefits of such a design, the three-level prototype is reconfigured to be powered by this method. It can be seen from Fig. 4.20 that, compared to the original gate drive method which causes the flying capacitor voltage to be lower than the nominal value, the proposed gate drive method can eliminate the delay mismatch and help achieve near perfect capacitor balancing. The complete results with various duty ratios are shown in Fig. 4.21a. In contrast to Fig. 4.6b, the capacitor voltage increases to its nominal value



(a) no delay mismatch



(b) no delay mismatch and different on-resistance

Figure 4.21: Measured flying capacitor voltage of a three-level FCML covnerter ($C_{\text{in}} = 65$ μF).

for $D = 0.25$ and $D = 0.5$. In addition, the prototype also demonstrates improved capacitor balancing for $D = 0.75$, a situation where the input voltage ripple strongly disturbs the capacitor balancing. However, in this case the flying capacitor voltage is lower than its nominal value when the load current is low, which is inconsistent with the analysis shown in Fig. 4.7. The reason behind this discrepancy is that the input voltage ripple has a different waveform at light-load, due to the negative inductor current in forced CCM mode.

The analytic waveforms showing V_{sw} and I_L at light-load condition are depicted in Fig. 4.22. Assuming that the output current is zero and the three-level FCML converter operates in forced CCM mode, the inductor only carries the ripple current. In this case, the input voltage ripple is no longer a triangular shape. Instead, it is quadratic with a smaller amplitude (compared to the triangular input voltage ripple during normal operation), which is similar to the output voltage ripple of a buck converter. Because of this quadratic voltage ripple, the switch node voltage is slightly higher than normal in state 1 and 3, but lower in state 2. Thus, the slope of the inductor current is steeper at the first three states, leading to a current flowing through C_1 in state 4 that is higher than normal. As shown in Fig. 4.22, the inductor current reverses polarity later than expected in state 4, which results in net

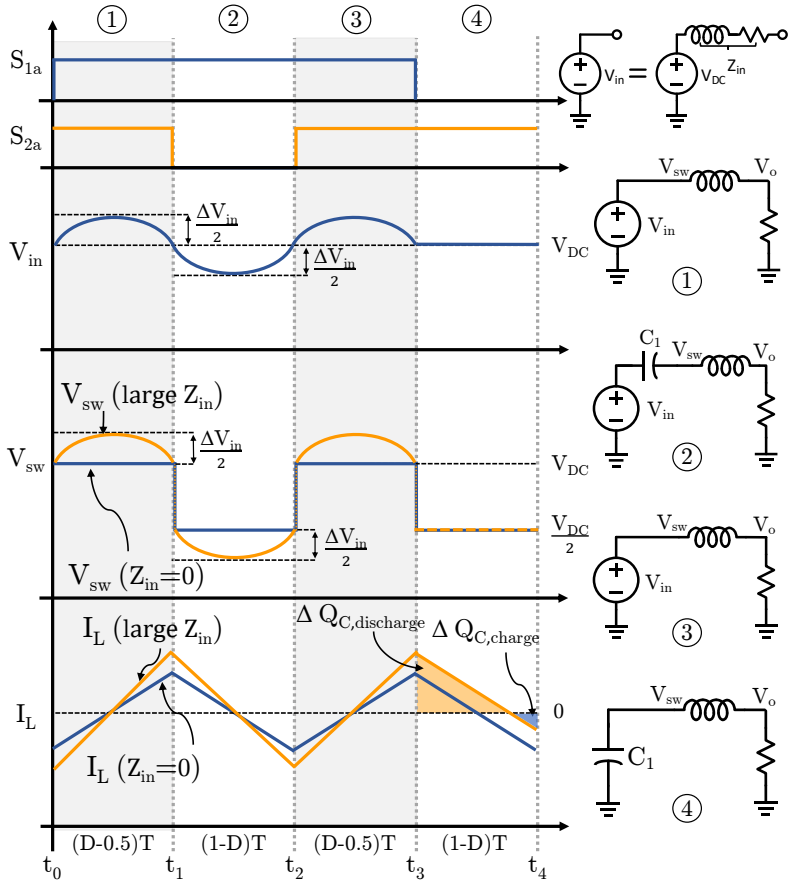


Figure 4.22: The effect of input ripple on capacitor balancing at light-load condition of a three-level converter with $D > 0.5$.

charge flowing out of the capacitor. In comparison to the analysis in Fig. 4.7, this demonstrates that depending on the amplitude of the load current, the input voltage ripple can cause the flying capacitor voltage to deviate towards opposite directions, which agrees with the measured three-level case at $D = 0.75$ in Fig. 4.21a.

Uneven Switch Resistance

The supply voltage difference produced by the original gate drive circuit can not only introduce gate signal delay mismatch, but also result in slightly higher on-resistance at the high-side switch (compared to the low-side). To investigate the effect of on-resistance variations on capacitor balancing, we modify the prototype by keeping the high-side switches the same as before (16 mΩ $R_{\text{ds,on}}$), but changing the low-side ones to EPC2001C GaN switches with 7 mΩ $R_{\text{ds,on}}$ (as shown in Fig. 4.23). The gate signal delay mismatch is eliminated by the proposed cascaded bootstrap circuit, and the turn-on time are tuned to be the same for

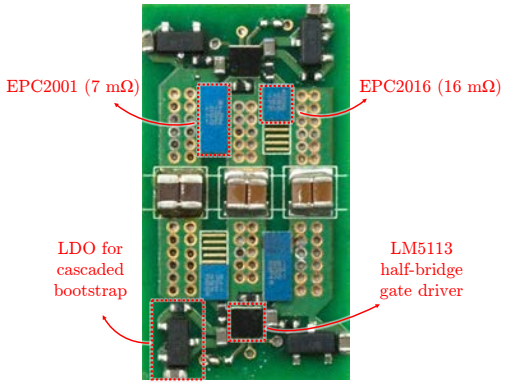


Figure 4.23: Switching cell design.

all switches with different gate resistance (the turn-off time can still be slightly different). As shown in Fig. 4.21b, the influence of uneven resistance on balancing is small compared to the other two factors discussed. The capacitor voltage remains almost the same as before for $D = 0.25$ and $D = 0.75$, and drifts slightly for $D = 0.5$, which is a special duty ratio where the inductor does not see any voltage ripple.

4.5 Chapter Summary

This chapter investigates the origins of the non-idealities that can cause flying capacitor voltage imbalance in practical implementations of FCML converters. A number of effects are characterized in detail experimentally, along with theoretical circuit analysis that explains their existence. It is first found that the source impedance and the associated input capacitance can have a drastic impact on capacitor balancing, especially for odd-level converters. A state-space analysis is then performed to show that the determinant of the system matrix is zero when the FCML converter has an odd number of levels, and results in no steady-state solutions for the system when a disturbance is present. In comparison, an even-level converter has a non-zero determinant and thus an inherently better immunity to voltage-type disturbances including the input voltage ripple. It is also discovered that the slight supply voltage difference in half-bridge gate drivers can cause a mismatch of gate signal propagation delays, which leads to a distortion of phase-shift and duty ratio, and ultimately gives rise to capacitor imbalance. An alternative gate drive power supply circuit is designed to address this problem. Even with large (e.g., $>$ 2x) variations of on-state resistance among various switches, the impact on capacitor voltage balancing is small.

Chapter 5

Circuit Techniques for Powering Floating Gate Drivers

A major challenge in the implementation of flying capacitor multilevel (FCML) converters and hybrid switched-capacitor (SC) converters is providing gate drive power to the large number of floating switches. A common solution uses isolated dc/dc converters, which are bulky, expensive, and energy inefficient. To design more compact and efficient gate drive power supply circuits, five methods are presented and compared in this chapter: bootstrap at deadtime, cascaded bootstrap with low-dropout (LDO) regulator, double charge pump, gate-driven charge pump, and synchronous bootstrap. By leveraging the inherent properties of multilevel converters, these methods can overcome the limitation of conventional bootstrap method (diode forward voltage drop) and make it possible to transfer ground-referenced power to all of the floating switches for any FCML or hybrid SC converters. Compared with the typical isolated dc/dc solution, these methods have simple structure and operating principle and can be implemented with a small number of diodes, capacitors, and LDOs. Experimental results show that an example power supply circuit can cut the size of the power stage of a state of the art seven-level FCML converter by half at 1/6 of the cost.

5.1 Background and Motivation

As discussed in Chapter 4, FCML converters have demonstrated excellent performance for a variety of applications [45], [50], [51], [74]–[78]. From a broader perspective, the FCML topology can be viewed as a type of hybrid switched-capacitor (SC) converter topology, which mainly uses high energy density capacitors in the power conversion process and thereby reduces the filter inductor size. It has been shown that hybrid SC converters have the potential

Part of this chapter was presented in the author's master thesis [94]. This chapter includes new circuit techniques (cascaded bootstrap with LDOs and synchronous bootstrap potential), more analysis and comparison of different methods, potential IC implementations, as well as the applicability to more hybrid SC converter topologies.

to outperform conventional two-level converters by a wide margin [29]. Besides ac conversions, these hybrid SC converters have also shown promise in low voltage dc/dc applications, including data center power delivery, CMOS point-of-load converters, automotives, etc. [23], [37], [79], [80].

In order to use the flying capacitors to generate the required multilevel voltages in FCML and hybrid SC converters, a large number of switches are needed, and most of them are not ground-referenced (i.e., are "floating switches"). To drive these floating switches, both the gate signals and the gate drive power need to be level-shifted from the control potential (typically ground), imposing challenges in practical implementations. In addition to digital isolators, the level-shifting of gate control signals can be alternatively achieved with isolated gate drivers (GDs) or high-side GDs with built-in level-shifters, resulting in no additional circuit components than the GD. In comparison, providing power to the floating GD is more challenging. The state of the art uses on-chip isolated dc/dc converters with integrated transformers [71]. Although this is an easy-to-use integrated solution, the large space occupied by the chip and the associated components (compared to the power switches and the GDs) and the poor energy efficiency (as low as 20%) can significantly reduce the theoretical efficiency and power density advantages of FCML and hybrid SC topologies, when the power level of the application is relatively low. Furthermore, the high bill-of-materials cost also prevents the widespread adoption of such converters.

Since the FCML and the hybrid SC are non-isolated topologies, it is not strictly required to employ galvanically isolated power supplies for the GDs. Alternative methods to provide power to high-side drivers have thus been explored in past works. Through charge pumping circuitry, it is possible to generate higher voltages from a single, ground-reference voltage source. One such example is the self-boost charge pump circuit in [81], which can transfer power to any floating reference. However, it becomes difficult to scale to a large number of floating switches owing to high circuit complexity. Another technique utilizes the switching characteristics of the main converter to transfer energy from the power stage to the floating GDs. The pulsed linear regulator proposed in [82] can also provide floating power by taking advantage of the high dv/dt transient during switching transition. A concern of this method is the reliability and applicability under all operating conditions, as the variation of parasitics can have a direct effect on its operation. Instead of exploring methods to power a generic floating switch, the scope of this chapter is limited to FCML converters and hybrid SC converters. Even though these topologies have a large number of floating switches, they are topologically connected to either other switches or flying capacitors (which can be viewed as voltage sources). Thus, as shown in this chapter, it is possible to utilize these unique characteristics to simplify the design of floating power supplies for these types of converters. The resulting solution should not only achieve the same functionality as that of an isolated dc/dc converter, but also needs to be simple, compact, efficient, and inexpensive. IC compatible circuit elements are preferred as the final goal is to monolithically integrate the GD and its power supply.

The bootstrap technique [83], [84] is the simplest and the most widely used method to drive the high-side switch of a half-bridge. It can be viewed as a 1-to-1 charge pump (or SC

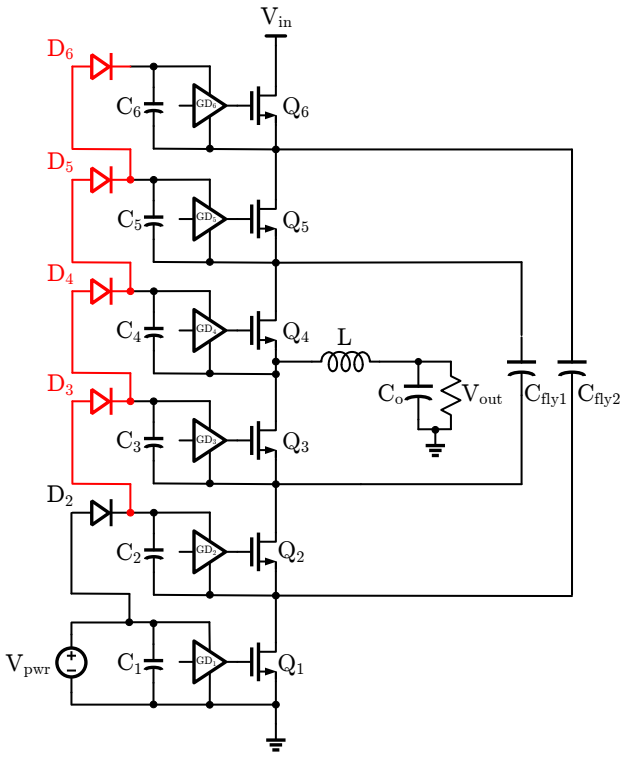


Figure 5.1: Schematic drawing of a cascaded bootstrap circuit on a four-level FCML buck converter.

converter) that consists of one diode and one switch. The bootstrap capacitor gets charged when the low-side switch is turned on, and then, it is automatically level-shifted to power the high-side switch with the diode blocking the drain-to-source voltage of the low-side switch. This method only requires one bootstrap diode that is integratable with the gate driver, and no control is needed. Since the multilevel topology has a string of series-connected switches, the concept of bootstrap can be extended to charge any floating switch from its neighboring low-side switch [8], [85]–[87]. A schematic drawing of an example four-level FCML converter powered by the cascaded bootstrap method is shown in Fig. 5.1. However, one practical limitation of this circuit is the effect of bootstrap diode forward voltage drop, which limits the achievable gate drive voltage at nodes in later stages of the cascade. This is a particularly important consideration when employing GaN transistors, as the allowed gate drive voltage is relatively narrow, leaving little room for deviations both above and below the limit (e.g., 4.5–6 V [88]).

In this chapter, we propose and investigate five methods to improve the original bootstrap technique. All proposed circuits have a simple structure and operating principle, and can be combined wisely to power any FCML converters and hybrid SC converters in a compact and efficient manner. In Section 5.2, we first start by analyzing the overcharge effect of bootstrap during deadtime, which is a special case for GaN transistors that can be used to

compensate the forward drop of the bootstrap diode. The implementation constraints and design considerations are discussed in detail in the context of FCML converters. In Section 5.3, an improved cascaded bootstrap circuit with LDOs is designed, which can provide equal gate drive voltage for all switches. To study the effect of varying duty cycle (in dc/ac and ac/dc operations) on the charging behavior of the bootstrap circuit, an in-depth numerical analysis is performed to help size the bootstrap capacitance, and various FCML prototypes are built to verify its performance. While being a simple and robust solution, the cascaded bootstrap with LDOs requires a relatively high voltage ground-referenced power supply (e.g., 16 V for a seven-level FCML) which may not be easily accessible for certain applications. Thus, in Section 5.4, we present another technique named double charge pump, which is a 1-to-2 voltage doubler constructed with two diodes and the two internal switches of the GD. It can generate a sufficiently high voltage at each stage such that a low-voltage ground-referenced power supply (e.g., 6 V) can be used for the cascaded operation without issues. Another limitation of the cascaded bootstrap method is the inherent cascaded efficiency penalty. Owing to the forward voltage drop of the bootstrap diodes, the efficiency of the overall bootstrap circuit goes down as the number of stages increases. In Section 5.5, we propose another charge pump circuit named gate-driven charge pump, which uses a low-side driver to transfer power to a corresponding high-side driver. This method decouples the chain relationship of the cascaded bootstrap, and can be applied to power a large number of high-side switches in FCML converters efficiently. In Section 5.6, we also explore the synchronous bootstrap technique proposed in [89], which replaces the bootstrap diode with self-controlled eGaN FET. Owing to the low on-resistance of eGaN FETs, the forward voltage drops in the cascaded bootstrap circuit is significantly reduced and the overall efficiency can be improved.

Combining the original cascaded bootstrap with the double charge pump and the gate-driven charge pump, a complete gate drive power supply circuit is built for a seven-level FCML converter in Section 5.7. Compared with the state of the art seven-level design [50] for the Google Little Box Challenge, the proposed circuit can cut the size of the power stage by half, with 15% gate drive loss reduction and more than 80% cost reduction. Moreover, these methods are also applicable to other hybrid SC converters, such as the Dickson converter and the series-parallel converter. Furthermore, the cascaded bootstrap circuit with LDOs has been tested on a number of prototypes, including the seven-level boost PFC front-end in [77], the six-level buck PFC front-end in [90], as well as the six-level dc/ac in [91]. With great robustness and usability, this method has proved itself to be an excellent replacement for the isolated dc/dc ic chips. A GD chip with built-in cascaded bootstrap LDO and gate-driven charge is also proposed and defined, with the potential to achieve more power dense FCML designs.

Providing reliable power to the GDs directly relates to the safe operation of power converters. Compared with isolated dc/dc gate drive power supplies, the proposed bootstrap and charge pump circuits rely on the operation of the main power circuit. Therefore, designers should understand the safe operating area as well as the limitations of the methods, and then select the most suitable one(s) based on the characteristics of the converter topol-

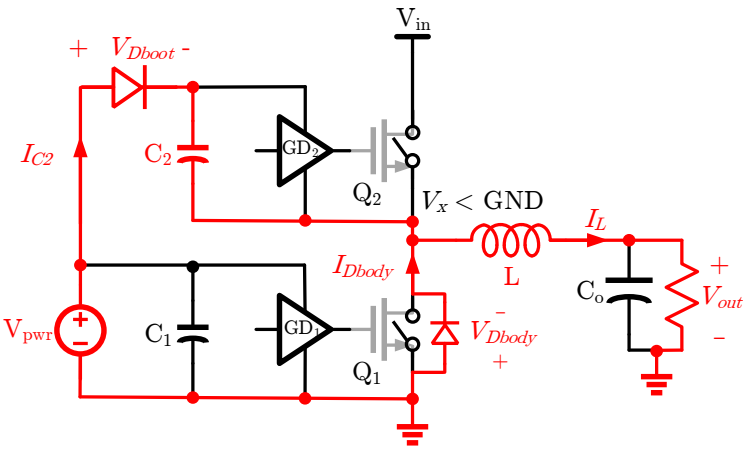


Figure 5.2: Inductor current flow in a two-level buck converter during deadtime.

ogy. It is crucial to make sure that all gate drive voltages are within the desired range (no over-voltage or under-voltage), at the designed switching frequency and duty cycle, and are stable under all conditions including start-up, light-load, and heavy-load. In Section 5.8, the five methods are compared with more discussions on design tradeoffs so that they can be appropriately applied to other topologies.

5.2 Bootstrap at Deadtime

Operating Principle

The overcharge effect of bootstrapping during deadtime is illustrated in Fig. 5.2 with a two-level buck converter as an example. Assuming that the inductor current remains positive at the deadtime when both switches are off, the body diode of the low-side switch will conduct to keep the inductor current flowing. As a result, the switch node voltage V_x will be lower than the ground potential by one body diode's forward voltage drop, and the bootstrap capacitor C_2 can be charged with the charging current I_{C2} flowing into the inductor, yielding the Kirchhoff's current law (KCL) constraint of (5.1) and the Kirchhoff's voltage law (KVL) constraint of (5.2)

$$I_L = I_{C2} + I_{Dbody} \tag{5.1}$$

$$V_{C2} = V_{\text{pwr}} - V_{D\text{boot}} + V_{D\text{body}} \tag{5.2}$$

where $V_{D\text{boot}}$ represents the forward voltage drop of the bootstrap diode and $V_{D\text{body}}$ represents the effective voltage drop across the transistor when the body diode is on. Although a GaN transistor does not have a conventional body diode, its reverse bias operation has a similar function, which leads to an equivalent $V_{D\text{body}}$ as high as 2 V (with a strong dependence on switch current [92]). Therefore, the voltage drop across the bootstrap diode $V_{D\text{boot}}$ can be

canceled by this factor, and the voltage on the bootstrap capacitor can be overcharged to exceed the ground-referenced gate drive power supply. Note that this is usually considered as an undesirable behavior in the literature [93], as the extra voltage on C_2 (thereby extra high V_{gs}) may result in damage of the GaN transistor. However, with proper implementation, this mechanism may help get equal or higher voltage on bootstrap capacitors through repeated bootstrap operation, and make the gate drive circuit shown in Fig.5.1 achievable.

Design Considerations

In practice, the aforementioned overcharge mechanism does not apply to all floating switches in a FCML converter, and the magnitude of the overcharge also depends on the converter's operating condition. Here, we analyze the factors that affect its performance and discuss the conditions that need to be satisfied before applying this special mechanism for the cascaded bootstrap operation.

Magnitude and Direction of Inductor Current

The key idea of this method is to exploit the inductor current that flows through the body diode (or equivalent body diode caused by reverse conduction of GaN switches) during deadtime and use the associated forward voltage drop to cancel the voltage drop of the bootstrap diode. However, at start-up and light-load when the average inductor current is low, only the small inductor ripple current will flow through the body diode. This will not only result in smaller voltage drop across the body diode, but also limit the bootstrap charging current, which is constrained by (5.1). That said, the overcharge effect at deadtime is minimal when the inductor current is low, and the voltage on the bootstrap capacitor will approach that of the typical bootstrap operation ($V_{C2} = V_{\text{pwr}} - V_{D\text{boot}}$). Owing to this unavoidable forward voltage drop at each stage during start-up, it is crucial to make sure that the bootstrap capacitor voltage at later stages of the cascade will not trigger the undervoltage protection of the GD, and is sufficient to turn on the switch. After the load current increases, the bootstrap capacitors will have higher voltage due to the overcharge effect.

The direction of the inductor current also matters. For the buck converter shown in Fig. 5.2, the current always flows from the inductor into the load (assuming the inductor current ripple is small compared to the average current), indicating that only the low-side switch will experience reverse current flowing through its body diode. The same rule also applies to FCML buck converters, in which the body diodes of the high-side switches will never turn on. This indicates that these switches cannot benefit from the overcharge effect (e.g., Q_5 and Q_6 in Fig. 5.1. Note that Q_4 is an exception as it is charged by the low-side Q_3). The situation of a FCML boost converter is the opposite. Since the current always flows out of the inductor and then flows into the load through the high-side switches, only the body diodes of these switches will conduct during deadtime. Therefore, the bootstrap overcharging during deadtime only applies to power the high-side switches in a step-up implementation.

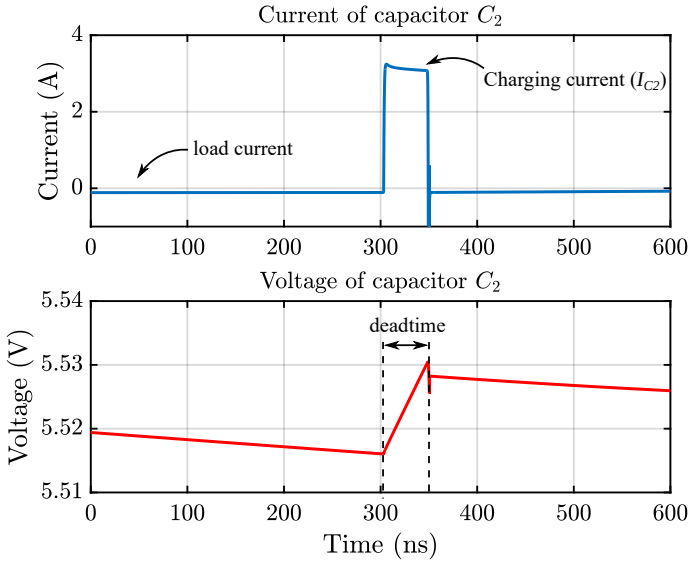


Figure 5.3: Simulated cascaded bootstrap circuit during deadtime ($V_{\text{pwr}} = 5$ V, $V_{D\text{body}} = 2$ V, $V_{D\text{boot}} = 0.6$ V).

Gate Drive Power

While (5.2) gives the theoretical maximum voltage of bootstrap capacitor C_2, its actual operating voltage will be lower due to the insufficient charging time (the deadtime) and the large current flowing through the bootstrap diode (corresponding to the load current that needs to be delivered to the gate drive circuit). The FCML converter with cascaded bootstrap shown in Fig. 5.1 is simulated in LTspice with a detailed model of the EPC2016C GaN transistor [88]. The voltage and current of C_2 are shown in Fig. 5.3. It can be seen that, during the deadtime, the capacitor is charged by a near constant current, which implies that the capacitor charge transfer is incomplete. Assuming a small capacitor voltage ripple, the average voltage of a bootstrap capacitor $V_{C,i}$ is given by

$$V_{C,i} = V_{C,i-1} + V_{D\text{body}} - V_{D\text{boot}} - I_{C,i}R_{D\text{boot}} \tag{5.3}$$

where $R_{D\text{boot}}$ is the equivalent resistance of the bootstrap diode and $I_{C,i}$ is the charging current for capacitor C_i during the deadtime. Thus, the actual voltage drop across the bootstrap diode is $(V_{D\text{boot}} + I_{C,i}R_{D\text{boot}})$, which is greater than the minimum diode turn-on voltage $V_{D\text{boot}}$. As shown in the bottom plot of Fig. 5.3, the average voltage of C_2 is approximately 5.5 V, instead of 6.4 V as given by (5.2).

In a cascaded bootstrap configuration, a gate drive stage is powered by the bootstrap capacitor of the previous stage. For example, C_6 provides power for GD_6, while C_5 provides power for both GD_5 and C_6 (and thus indirectly GD_6). Therefore, the charging current of

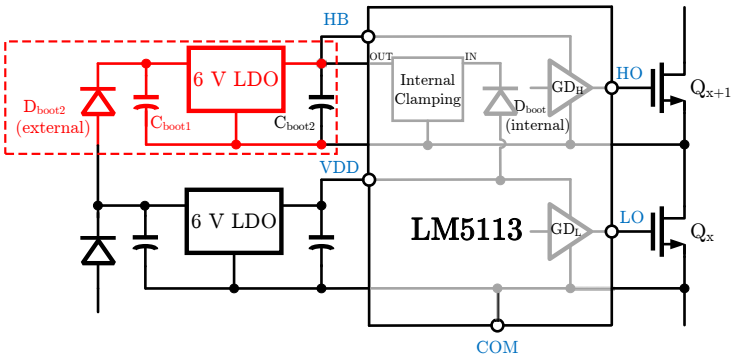


Figure 5.4: Additional circuitry to observe the overcharge effect of bootstrap operation at deadtime.

the ith bootstrap capacitor is given by

$$I_{C,i} = \frac{\sum_{x=i}^{n} Q_{\text{gate},x}}{t_{\text{dead}}} \tag{5.4}$$

where n is the total number of switches, $Q_{\text{gate},x}$ is the charge delivered to the GD_x in one switching period, and t_{dead} is the length of deadtime. Combining (5.3) and (5.4), we can see that due to a larger load charge and the resultant larger charging current, the bootstrap capacitor closer to ground (corresponding to a smaller i) will experience less overcharge effect.

Length of Deadtime

As shown in Fig. 5.3, bootstrapping happens during the deadtime. Since the required gate drive charge is fixed per switching cycle, a longer deadtime can help reduce the charging current ($\Delta Q = I\Delta t$), which further leads to higher average capacitor voltage according to (5.3). Nevertheless, as the current flowing through the body diode contributes to power loss, a smaller deadtime is preferred from the conversion efficiency perspective. If the cascaded bootstrap method is chosen, careful calculations and measurements should be performed to make sure the converter has sufficient gate drive voltages while maintaining a high overall conversion efficiency.

Hardware Verification

A hardware prototype of the four-level FCML converter in Fig. 5.1 is implemented to validate the theory described above. The bottom four switches ($Q_1 - Q_4$) are powered by the cascaded bootstrap method. Due to the direction of the current flow, the overcharge effect at deadtime does not apply to the top two switches (Q_5 and Q_6). Thus, they are powered by the gate-driven charge pump method (described in detail in Section 5.5) to ensure sufficient gate drive

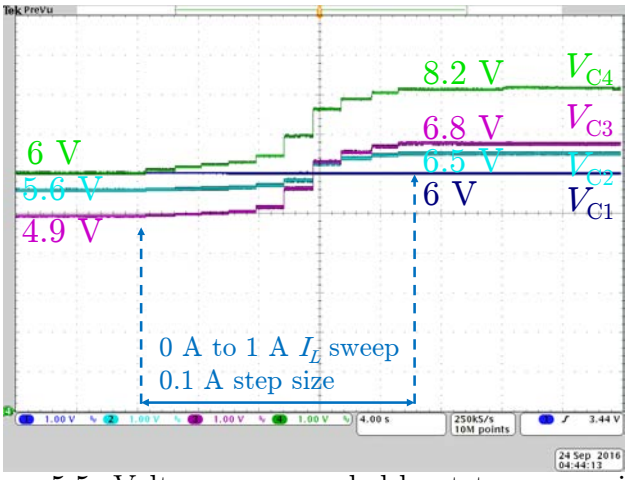


Figure 5.5: Voltage on cascaded bootstrap capacitors.

voltage magnitude. In order to reduce the number of components, TI LM5113 half-bridge GDs [72] are used so that only three drivers are needed to drive the six switches. Owing to the internal clamping of the built-in bootstrap diode in the LM5113, it is not possible to fully observe the body diode voltage gains through the cascaded bootstrap operation. For observational purpose, a redundant external diode is introduced to bypass the internal clamping function and an LDO is added to limit the V_{gs} of the GaN transistor, as illustrated in Fig. 5.4.

The voltage waveforms (corresponding to capacitors C_1 to C_4 in Fig. 5.1) with load current sweep is shown in Fig. 5.5. The switching frequency is 120 kHz. Capacitor C_1 is connected to the ground power supply, and its voltage is fixed at 6 V. At zero load current, the voltages on C_2 and C_3 are each reduced by approximately one diode drop from the previous voltage, indicating that the overcharge effect at deadtime is not sufficient to compensate for the voltage drop of the bootstrap diodes. In this situation, it is important to make sure that the lowest voltage in the cascade ($V_{C3} = 4.9$ V) can still fully enhance the GaN transistor [88], so that the effect of switch on-resistance mismatch on converter operation is minimal. Compared with C_3, C_4 is overcharged to 6 V at zero load current condition (only inductor ripple current exists). As explained in (5.4), the capacitor at the end of the cascaded bootstrap chain processes the least amount of gate drive power. Therefore, it has the lowest capacitor charging current and the most noticeable overcharge effect. After the load current increases, V_{C2} to V_{C4} all start to increase. When I_L is approximately 0.7 A, all bootstrap capacitor voltages exceed 6 V (V_{pwr}). After I_L is increased to 1 A, the voltage on each bootstrap capacitor becomes higher than its low-side neighbor because of the overcharge effect. It can be observed from Table 5.1 that the length of deadtime has a strong influence on the gate voltage. A shorter deadtime design will require a higher load current to overcharge the bootstrap capacitors to exceed the voltage of the ground power supply.

Table 5.1: Measured voltage on cascaded bootstrap capacitors with 1 A load current and different deadtimes

Capacitor	33 ns	66 ns	100 ns
C_1	6 V	6 V	6 V
C_2	5.62 V	5.82 V	6.52 V
C_3	5.28 V	5.86 V	7.26 V
C_4	5.95 V	6.96 V	8.44 V

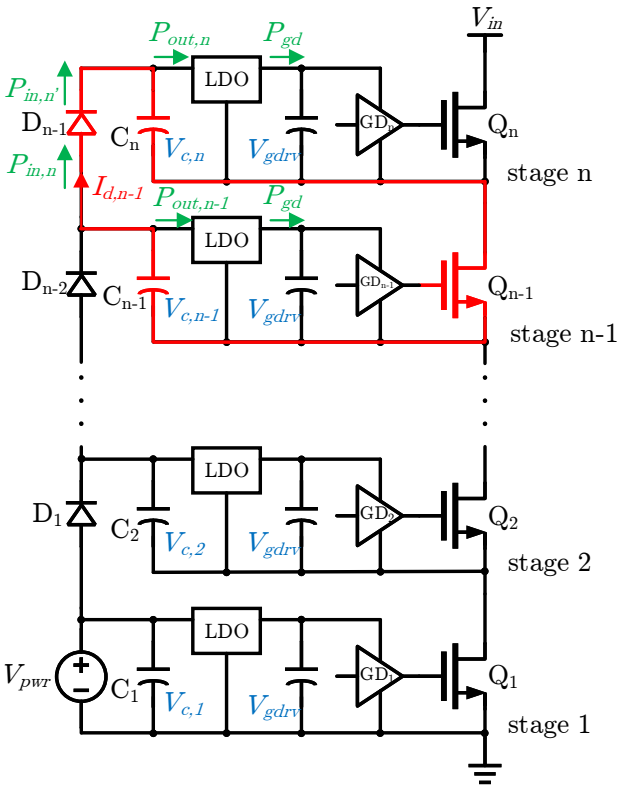


Figure 5.6: Schematic drawing of a cascaded bootstrap circuit with LDOs on a string of series-connected switches.

5.3 Cascaded Bootstrap with LDOs

Operating Principle

To overcome the limitations of the overcharge effect at deadtime, an improved cascaded bootstrap method with high-voltage ground-referenced power supply and LDOs is proposed.

As shown in Fig. 5.6, the ground-referenced power supply has a voltage V_{pwr} that is higher than the required gate drive voltage V_{gdrv}, such that there remains sufficient voltage at each stage of the cascade after the diode forward voltage drops. To protect the switch and the GD, an LDO is used at each stage to step down the bootstrapped voltage to the desired value. With sufficient voltage on the ground power supply, this simple and modular method can provide equal gate drive voltage for all floating switches.

Design Guidelines

This method relies on the excess voltage on the power supply to make the bootstrap operation cascadable. However, this high voltage has to be stepped down to the required gate drive voltage in a resistive manner (by bootstrap diodes or LDO), resulting in an overall cascaded bootstrap efficiency of

$$\eta_{\text{total}} = \frac{V_{\text{gdrv}}}{V_{\text{pwr}}}. \tag{5.5}$$

This implies that the efficiency is reduced as the number of floating switches increases, because V_{pwr} needs to be increased to compensate for additional diode forward voltage drops. To optimize the efficiency, V_{pwr} should be tuned to ensure that the LDO of the top switch (the switch at the end of the cascade) sees a voltage that is only slightly higher than the required gate drive voltage ($V_{c,n} \simeq V_{\text{gdrv}} + V_{\text{ldo,dropout}}$), as any excess voltage on the LDO is unnecessary loss. In order to understand the factors that affect the operation of the cascaded bootstrap circuit and determine a suitable V_{pwr}, we analyze the power flowing through the cascaded bootstrap circuit and discuss the important design considerations of such circuit.

As illustrated in Fig. 5.6, the gate drive power of stage n is provided by the bootstrap capacitor C_n. When switch Q_1 is on, C_n is charged by its low-side neighbor C_{n-1} through bootstrap diode D_{n-1}. Assuming the average current flowing throughD_{n-1} is $I_{d,n-1}$, then the average gate drive power transferred from stage $n-1$ to stage n (from C_{n-1} to C_n) is

$$P_{\text{in},n} = V_{c,n-1} I_{d,n-1}. \tag{5.6}$$

Since the average diode current $I_{d,n-1}$ can be expressed in terms of the charge transferred per switching cycle $I_{d,n-1} = Q_{d,n-1} f_{\text{sw}}$, (5.6) can be alternatively written as

$$P_{\text{in},n} = V_{c,n-1} Q_{d,n-1} f_{\text{sw}}. \tag{5.7}$$

For bootstrap circuit operating at a relatively high switching frequency (> 100 kHz), the on-state bootstrap charging current $I_{\text{on},n-1}$ becomes a near constant value [94]. Thus, $Q_{d,n-1}$ can be approximated to be

$$Q_{d,n-1} \simeq I_{\text{on},n-1} \frac{d}{f_{\text{sw}}} \tag{5.8}$$

where d is the duty ratio when the main switch is on and the bootstrap operation is active. Therefore, we can further express $P_{\text{in},n}$ as

$$P_{\text{in},n} \simeq V_{c,n-1} I_{\text{on},n-1} \frac{d}{f_{\text{sw}}} f_{\text{sw}} = V_{c,n-1} I_{\text{on},n-1} d. \tag{5.9}$$

Next, by modeling the bootstrap diode as a voltage source V_f in series with an on-resistance R_{on}, the charging current can be derived to be

$$I_{\text{on},n-1} = \frac{V_{c,n-1} - V_{c,n} - V_f}{R_{\text{on}}}. \tag{5.10}$$

If we define $(V_{c,n-1} - V_{c,n} - V_f)$ as $\Delta V_{c,n-1}$, then $P_{\text{in},n}$ can be expressed as

$$P_{\text{in},n} \simeq \frac{V_{c,n-1}\Delta V_{c,n-1} d}{R_{\text{on}}}. \tag{5.11}$$

Excluding the loss on the bootstrap diode D_{n-1}, the actual power delivered to C_n at stage n is

$$P_{\text{in},n'} \simeq \frac{V_{c,n}\Delta V_{c,n-1} d}{R_{\text{on}}}. \tag{5.12}$$

This power is then consumed by the following LDO and gate drive circuit. The gate drive power includes the quiescent power and the switching power that goes into the switch:

$$P_{\text{gd}} = V_{\text{gdrv}} I_q + f_{\text{sw}} C_{\text{iss}} V_{\text{gdrv}}^2 \tag{5.13}$$

where V_{gdrv} is the gate drive voltage, I_q is the GD quiescent current and C_{iss} is the input capacitance of the switch. After including the power loss on the LDO, the total power consumed by stage n becomes

$$P_{\text{out},n} \simeq \underbrace{\frac{V_{c,n}}{V_{\text{gdrv}}}}_{1/\eta_{\text{LDO}}} \times \underbrace{V_{\text{gdrv}}(I_q + f_{\text{sw}} C_{\text{iss}} V_{\text{gdrv}})}_{\text{GD power}} \tag{5.14}$$

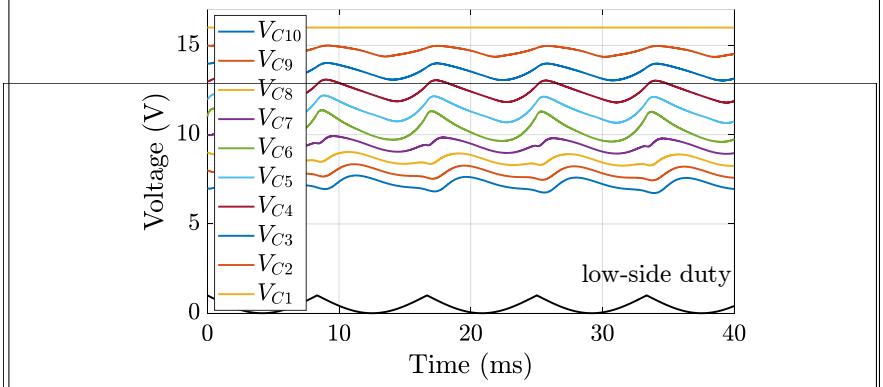
$$= V_{c,n}(I_q + f_{\text{sw}} C_{\text{iss}} V_{\text{gdrv}}). \tag{5.15}$$

Since the net power into C_n is zero in steady state, we get

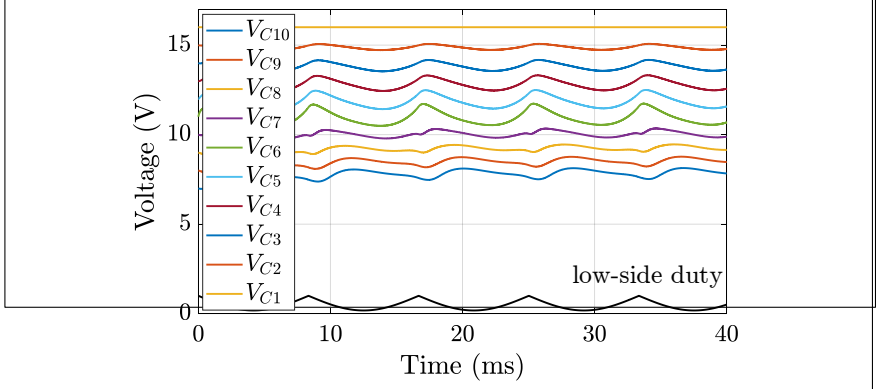
$$P_{\text{in},n'} = P_{\text{out},n}. \tag{5.16}$$

With this equality, we are able to derive the ground power supply voltage of an N-level FCML dc/dc converter. For instance, with desired V_{gdrv}, $V_{c,n}$, d and f_{sw}, $V_{c,n-1}$ can be calculated through (5.16). Then, $V_{c,n-2}$ can be derived with the updated P_{out} value, which is the sum of $P_{\text{in},n}$ and $P_{\text{out},n-1}$. With $N-1$ iterations, the minimum $V_{c,1}$ (corresponding to the highest possible overall gate drive efficiency) to supply equal gate drive voltage for all floating switches can be determined.

By comparing (5.12) and (5.15), it can be observed that the power consumed by the GD $P_{\text{out},n}$ is a function of f_{sw}, but the input power supplied by the cascaded bootstrap circuit $P_{\text{in},n'}$ is not. This is because all bootstrapped power comes from the ground power supply, and it is a function of duty ratio (or effective switch on-time) rather than switching frequency. This fundamental limitation may pose challenge to operation with very low duty ratio, which



(a) DC/AC operation, modulation index = 1



(b) AC/DC operation, $V_{\text{rms}} = 220$ V, $V_{\text{rec}} = 380$ V

Figure 5.7: Simulated cascaded bootstrap voltages of a six-level FCML converter under different operating conditions ($f_{\text{ac}} = 60$ Hz, $f_{\text{sw}} = 120$ kHz, $V_{\text{pwr}} = 16$ V, $C_{\text{boot}} = 20$ μF, switch: GS61004B[95], GD: Si827x[96], diode: $V_f = 0.6$ V, $R_{\text{on}} = 5$ Ω).

may occur in dc/ac and ac/dc cases. For such cases, a higher ground power supply voltage than that of a dc/dc case with the same averaged duty ratio is required for extra headroom, so that the top switch at the end of the cascade can maintain normal operation in the worst case.

The simulated gate drive voltages of a six-level FCML converter operating in dc/ac and ac/dc modes are shown in Fig. 5.7. It can be seen that the bootstrap capacitors experience a voltage swing over the line cycle, owing to the change of available bootstrap charging time. More bootstrap capacitance can be used for better filtering and less voltage swing, but it can be limited by cost and space in practical implementations. Compared with the ac/dc case, the duty ratio of the low-side switches in the dc/ac case has lower average value and lower absolute value (d reaches 0). According to (5.11), given fixed ground power supply voltage, it will result in larger capacitor voltage drops and lead to lower voltage on the capacitor at each stage. Care must be taken to make sure that the minimum voltage at the last stage is sufficient to fully enhance the switch (6 V for the GaN switch in this example).

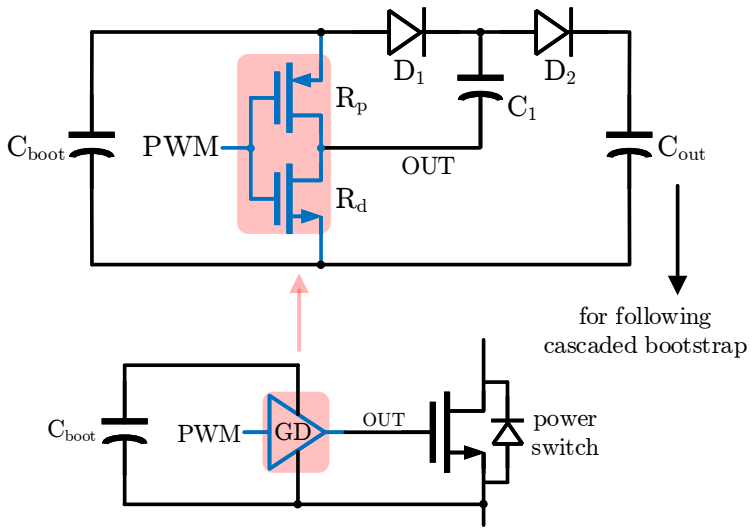


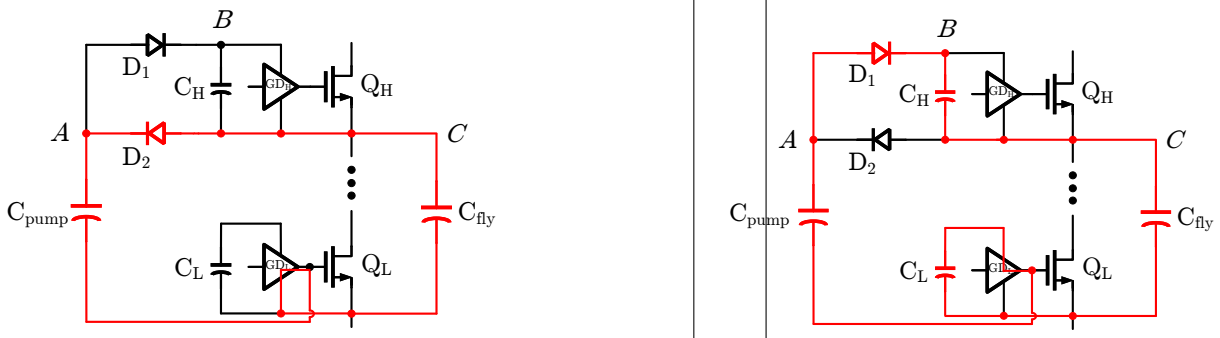
Figure 5.8: Schematic drawing of a double charge pump circuit.

The functionality and robustness of this method have been successfully verified on various ac/dc and dc/ac FCML converter prototypes [77], [90], [91]. In such implementations, the ground reference of the LDOs is not fixed. Instead, they experience the same magnitude of voltage swing (with high $\mathrm{d}v/\mathrm{d}t$) as the main switches during switching transitions. Therefore, it is critical to minimize the parasitics in the layout, such that the LDOs can remain stable under all conditions. Additionally, owing to the low gate charge and the associated fast switching speed of GaN switches, suitable gate resistances should be employed to ensure the proper operation of the bootstrap circuit.

5.4 Double Charge Pump

As discussed above, the cascaded bootstrap circuit with LDOs is a simple and robust solution. However, it requires a high voltage power supply, which may not be easily accessible for certain applications. Here, we present another charge pump circuit to boost up the bootstrapped voltage, so that a low-voltage power supply can be used for the cascaded operation without the concerns of the diode forward voltage drops.

As shown in Fig. 5.8, a 1-to-2 voltage doubler (also called double charge pump) is constructed by utilizing the two existing internal switches of the GD. Only two diodes and two capacitors are needed, and no additional control signals are required. Since the diodes only need to block the input voltage ($V_{C_{\mathrm{boot}}} < 10$ V), low-voltage, low-profile Schottky diodes can be used. The double charge pump has two operating states. In the first state, the PWM signal is low and the pull-down switch R_d is active, so that C_1 is charged by C_{boot} through diode D_1. In the second state, the PWM signal is high and the pull-up switch R_p is active. Therefore, D_1 is reverse biased, and C_{out} is charged by the series combination of C_1 and



(a) State 1 (b) State 2

Figure 5.9: Schematic drawing of a gate-driven charge pump circuit.

C_{boot} through D_2. The output voltage of this double charge pump will be approximately twice the gate drive voltage $V_{C_{\text{boot}}}$ minus the forward drops of D_1 and D_2. For instance, assuming the desired gate drive voltage is 6 V, and the drop of each diode is as high as 1 V (due to incomplete charge transfer and high charging current), the double charge pump can still provide 10 V output, which is sufficient to power the next 4–5 switches in an FCML converter through the cascaded bootstrap operation.

One concern of this method is the efficiency, since eventually the doubled voltage must be regulated to the desired gate drive voltage in a resistive manner, either through the voltage drops of the diodes or through the LDO in front of the GD. If n double charge pumps are used to power a given stage in the cascaded bootstrap, its efficiency will be $\eta \simeq (\frac{1}{2})^n$. Thus, double charge pumps should be utilized cautiously, as unnecessary use may degrade the efficiency of the power supply circuit. An implementation example is given in Section 5.7.

5.5 Gate-Driven Charge Pump

The three methods discussed above strive to overcome the effect of diode forward voltage drops in a cascaded bootstrap circuit. However, there remains another main limitation, which is the cascaded efficiency penalty. Because of the forward voltage drop of the bootstrap diodes, the efficiency of the overall bootstrap circuit goes down as the number of stages increases. Here, we propose another charge pump circuit named gate-driven charge pump. Instead of transferring power between neighboring switches through a bootstrap diode, the proposed circuit can transfer power from a low-side driver to a corresponding high-side driver, as long as the two drivers have a flying capacitor connected in between. This method can not only be applied to power a large number of high-side switches in an FCML converter efficiently, but also be used in various hybrid switched-capacitor topologies, as many of them share the same fundamental structure (two switches and a flying capacitor in between).

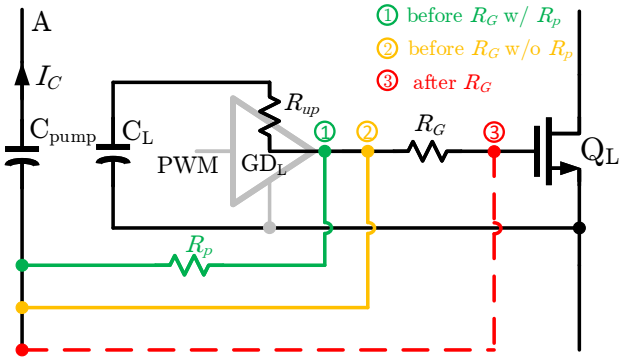


Figure 5.10: Different ways to connect gate-driven charge pump.

Operating Principle

The schematic drawing of a gate-driven charge pump is illustrated in Fig. 5.9. In order to transfer charge from C_L to C_H, one capacitor C_{pump} and two low-voltage rating diodes D_1 and D_2 are needed. The positive terminal of C_{pump} is connected with C_{fly} through diode D_2. The negative terminal of C_{pump} is connected to the gate of switch Q_L. When Q_L is off, its gate is pulled low to its source. As a result, the voltage of C_{pump} will be charged to the voltage of C_{fly} minus the forward drop of D_2. In the other state, when Q_L is turned on by pulling its gate high, C_{pump} is connected to C_L through the pull-up transistor inside gate driver GD_L. Assuming C_L has a voltage of 6 V, the voltage at the positive side of C_{pump} (Node A) will also be 6 V higher than its value in State 1. Thus, D_2 will be reverse biased, and D_1 will conduct. Capacitor C_H can, therefore, be charged through the loop highlighted in red in State 2 of Fig. 5.9. The final voltage of C_H will be

$$V_{C_H} = V_{C_L} - V_{D1} - V_{D2}. \tag{5.17}$$

Since D_1 and D_2 only need to block the voltage of capacitor C_H, small Schottky diodes with low forward drop can be used. Experimental result shows that the forward drop of a 10 V Schottky diode can be as low as 0.2 V, and therefore only 0.4 V of voltage drop will occur during the gate-driven charge pump operation, reflecting good efficiency performance. In addition, the capacitor being charged, like C_H in this example, does not need to charge another capacitor. It means that the voltage drop will not continue to increase with respect to the number of levels, as in the cascaded bootstrap case. Furthermore, this proposed circuit does not require any pre-charge circuit for start-up. With small-signal analysis, it can be shown that GD_L operates as an ac voltage source, such that a few milliampere current can flow through C_{pump} to charge C_H even if the voltage on C_{fly} is zero.

Effect on the Main Switch

Because both the gate-driven charge pump and the double charge pump utilize the gate terminal of a power switch to transfer energy, care must be taken to ensure that the normal

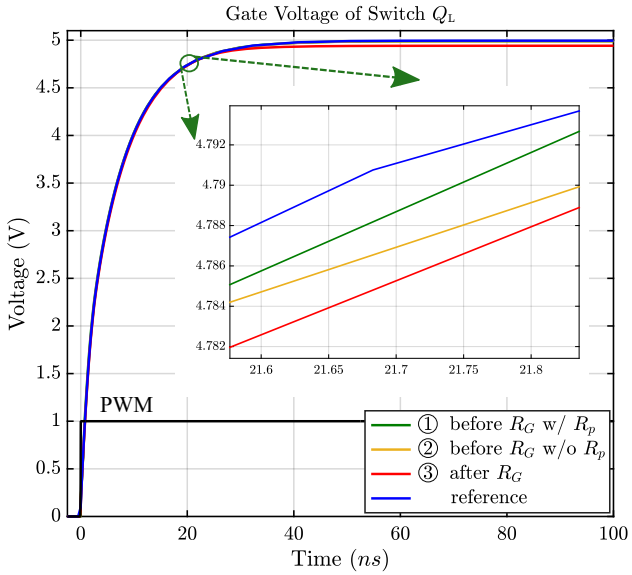


Figure 5.11: Turn-on behavior of EPC 2016C GaN switch with gate-driven charge pump connected (simulation parameters: $R_{\text{up}} = 1\ \Omega$, $R_G = R_p = 10\ \Omega$, $C_L = C_H = C_{\text{pump}} = 1\ \mu F$, $V_{C_L} = 5\ V$).

operation of the corresponding power switch will not be affected. Here, we analyze the turn-on behavior of a power switch which has a gate-driven charge pump connected. The analysis of a double charge pump can be performed in a similar manner.

Typically, a small-valued gate resistor is connected between the GD and the gate terminal of the power switch. As shown in Fig. 5.10, there are three possible ways to connect the gate-driven charge pump. The negative terminal of C_{pump} can be connected to either the GD side of the gate resistor R_G or the power switch side of the gate resistor. When connected to the GD side, an additional current limiting resistor R_p can be added to limit the peak current flowing through C_{pump}.

To study the turn-on behavior of the GaN switch with the three kinds of gate connections depicted in Fig. 5.10, an LTspice simulation with a detailed model of the EPC2016C GaN switch [88] is performed. The simulated gate-to-source voltages of Q_L is shown in Fig. 5.11. The blue line is a reference curve representing the normal switching behavior of Q_L without any gate-driven charge pump connected. It can be seen that the gate-driven charge pump has negligible effect on the switching operation of the power switch, regardless of the type of gate connection. This is mainly because the gate-driven charge pump only needs to transfer a small amount of charge (the gate charge of Q_H) in each switching period and the corresponding charging process can be completed quickly. If the gate-driven charge pump needs to transfer more charge (e.g., for a digital isolator or another power switch), the resultant charging current will increase. It is recommended to connect the gate-driven charge pump to the GD side of the gate resistor (before R_G). This way, the gate capacitance of Q_L and C_H has different charging paths (only share the pull-up resistor R_{up} inside the

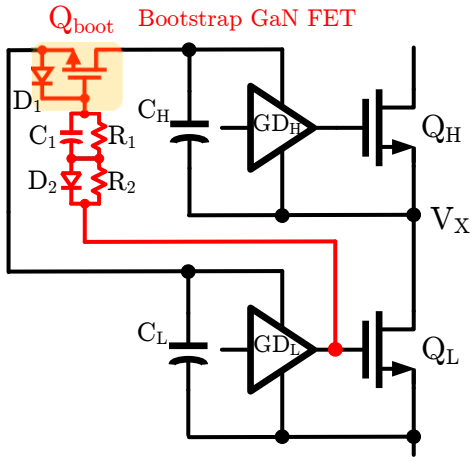


Figure 5.12: Schematic drawing of a synchronous bootstrap circuit.

GD), so that the charging operation of the gate-driven charge pump has minimal effect on the turn-on behavior of the power switch.

Alternatively, instead of using the GD of switch Q_L to transfer charge, an additional GD / CMOS inverter circuit which has the same ground reference can be added for charge pumping purpose. Although at the expense of one extra component, the gate-driven charge pump can operate without any limitations (e.g., no constraint on duty cycles, no effect on the operation of the main switch). It may also operate at a frequency higher than the switching frequency of the main switches, which could potentially reduce the size of the charge pump capacitor.

5.6 Cascaded Synchronous Bootstrap

Another method that can simultaneously overcome the diode drop issue and improve the efficiency is to replace the bootstrap diode with an actively-controlled transistor with lower on-resistance. The synchronous bootstrap technique proposed in [89] provides a simple way to control the GaN-based bootstrap switch. This is achieved by utilizing the gate terminal of the main switch to make the bootstrap eGaN FET switch synchronously, essentially operating as a bootstrap diode with very low voltage drop (limited only by the on-resistance of the bootstrap switch).

The schematic drawing of the synchronous bootstrap circuit is shown in Fig. 5.12. The bootstrap eGaN FET Q_{boot} [97] is an N-channel device, and has a built-in diode from source to gate. Notice that it has extremely small input capacitance (7 pF) so that no additional GD is needed. In order to make Q_{boot} switch synchronously with the low-side switch Q_L, a level-shifting circuit is built on top of the gate of Q_L. When the gate is pulled low, capacitor C_1 can be charged to approximately the voltage of C_L. When the gate is pulled high, C_1 will

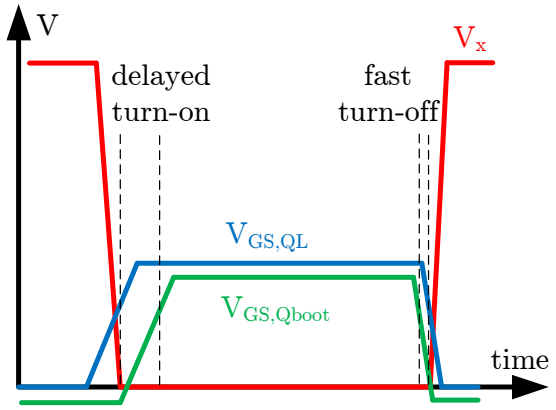


Figure 5.13: Key switching waveform of the synchronous bootstrap circuit.

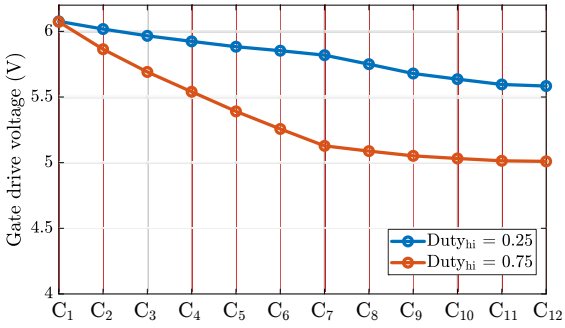


Figure 5.14: Measured cascaded synchronous bootstrap voltages on a seven-level FCML buck converter at no-load condition (switch: EPC2001C, $f_{\text{sw}} = 140$ kHz).

pump the gate voltage of the bootstrap eGaN FET to be higher than its source terminal, so that Q_{boot} is turned on and C_H can be charged as in a traditional bootstrap.

Unlike a diode, the bootstrap eGaN FET can conduct bidirectionally. Care must be taken to make sure that Q_{boot} switches at the right time and current will never flow from C_H to C_L. Otherwise, Q_L may be damaged due to the overcharge of C_L. As shown in Fig. 5.13, Q_{boot} should not be switched on until Q_L is enhanced and its drain-to-source voltage V_x is discharged to zero. A current limiting resistor R_2 is therefore used to slow down the turn-on speed of the bootstrap eGaN FET. During the turn-off transition, the bootstrap eGaN FET needs to be pulled down quickly by the diode D_2, before the switch node voltage V_x starts to ramp up. The resistance of R_1 is selected to be much larger than that of R_2. This is so that the voltage divider they create can help charge C_1 to $(V_{\text{CL}} - V_{D1})$, whose voltage is not decreased by the forward drop of D_2.

Assuming the voltage drop across Q_{boot} is small, the voltage of C_H can be charged up to approximately the voltage of C_L, with little voltage loss. This indicates that the synchronous bootstrap technique can be used to improve the cascaded bootstrap circuit in Fig. 5.1 with

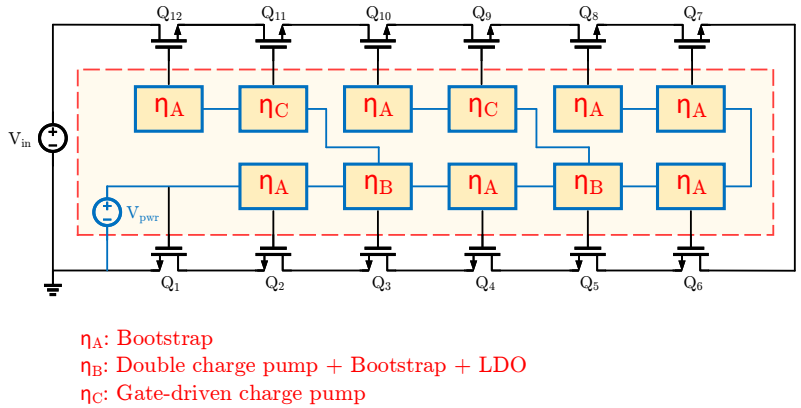


Figure 5.15: Proposed gate drive power supply methods for a seven-level FCML converter.

less cascaded voltage drops and higher gate drive efficiency. This proposed technique is tested on a seven-level FCML dc/dc converter prototype, and the measured bootstrap voltages are plotted in Fig. 5.14 (C_1 corresponds to the bottom switch that connects to the ground, C_{12} corresponds to the top switch that connects to the input). With 6 V on the ground-referenced power supply, all of the 12 switches have a gate drive voltage greater than 5 V, which is within the accepted operating range. However, as predicted in (5.12), the bootstrapped voltages heavily depend on the duty ratio, and a higher duty ratio on the high-side switches will result in lower voltages due to less bootstrap charging time through the low-side switches. This may impose challenges for ac/dc or dc/ac operations, in which the duty ratio varies in a large interval. In addition, a higher switching frequency will also result in lower bootstrapped voltages, and it is difficult to improve besides further reducing the on-resistance of the bootstrap eGaN FETs. In comparison, at the expense of lower efficiency, these challenges can be easily addressed by the cascaded bootstrap method with LDOs discussed previously, as the input voltage can be increased to supply more power and the LDOs can filter out the voltage variations due to the ac operation. The 1000 unit price of the bootstrap eGaN FET [97] is around \$0.5, as compared to \$0.1 for a Schottky diode with the same voltage rating. For a seven-level FCML design, the cascaded synchronous bootstrap circuit may contribute \$5 extra cost. However, depending on the applications, this extra cost might be acceptable.

5.7 Implementation Examples

FCML Converters

Fig. 5.15 is a simplified schematic showing the power supply method for each switch of a seven-level FCML converter. A complete schematic with detailed power circuit implementations can be found in [98]. To save the number of components, half-bridge GDs are used and every two adjacent switches (e.g. Q_1 and Q_2) are driven by one driver. The high-side

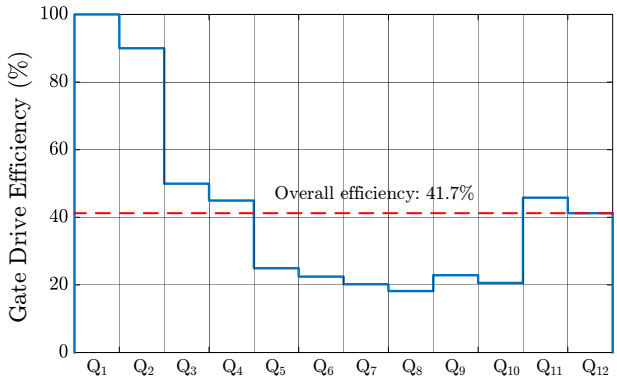


Figure 5.16: Calculated efficiency of the proposed gate drive power supply circuit.

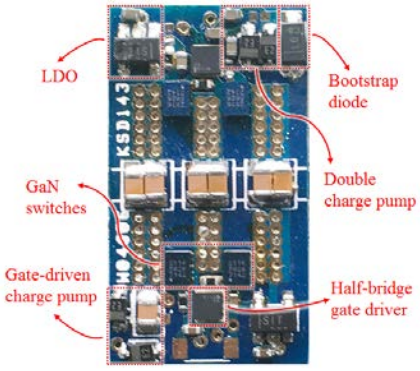


Figure 5.17: Power module (switching cell) design with proposed gate drive power supply circuit.

switch of each half-bridge ($Q_{i,\ i\ is\ \text{even}}$) is powered by the intrinsic bootstrap diode and no additional circuit is needed. To overcome the accumulated diode drops, the double charge pump method is used twice (at Q_3 and Q_5) to boost up the gate drive voltage back to the desired value. Since Q_7 is at the end of the cascade, the overcharge effect at deadtime can help increase the voltage and so double charge pump is not used. The high-side switches (Q_9 and Q_{11}) are powered by gate-driven charge pumps. Compared with bootstrap-based methods, this method does not suffer from the cascaded voltage drops and has higher efficiency. The efficiency analysis of the proposed gate drive power supply circuit is covered in [98] and the calculated result for every single switch in the seven-level implementation is shown in Fig. 5.16. As expected, the gate drive power supply efficiency decreases for the switches that are further away from the ground, as double charge pump and cascaded bootstrap methods are needed repeatedly to transfer the power. However, the efficiency increases for the top four switches. This is due to the use of the gate-driven charge pump, which is more efficient

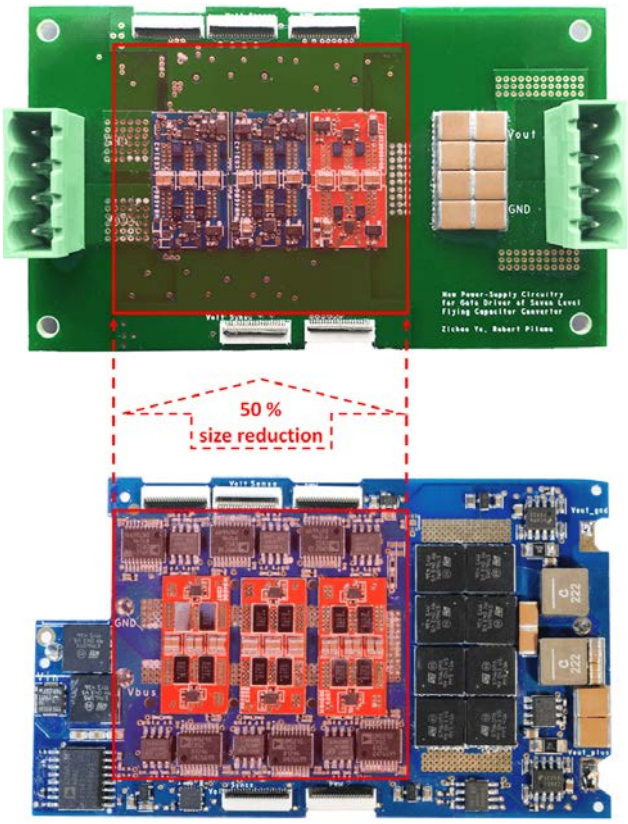


Figure 5.18: Comparison of the hardware prototype with [99].

than the other two methods.

To demonstrate the functionality of the proposed gate drive power circuit, a seven-level FCML converter prototype is built and its implementation details can be found in [98]. The size of prototype's power module (switching cell) is the same as that in [99], which is a state of the art Google Little Box Challenge finalist's design with a power density of 216 W/in^3. However, the difference is that the six isolated dc/dc power supplies used in [99] are replaced by the proposed power supply circuit, which is successfully integrated around the GaN switches and GDs as shown in Fig. 5.17. Note that for GaN-based implementations, it is particularly important to minimize the parasitic inductance in the gate drive loop and the main power commutation loop [50], [100], [101]. This modular switching cell design can not only reduce the parasitic loop inductance of FCML converters, but also reduce the fabrication and debugging complexity significantly. The digital isolators are put to the back side of the board (right beneath the switching cells) with no extra space. As a result, approximately 50% converter area reduction is achieved, with the capability to output the same amount of power with equal or better efficiency. Fig. 5.18 compares the photographs of the two prototypes and showcases the size reduction achieved.

Table 5.2: Measured gate drive power supply voltages of the seven-level FCML converter (at 250 V_{DC} to 100 V_{DC})

C	No V_{in}	$I_L = 1$A	$I_L = 2$A	$I_L = 3.5$A	$I_L = 5$A
C_1	5.98 V	5.98 V	5.98 V	5.98 V	5.98 V
C_2	5.12 V	5.22 V	5.21 V	5.23 V	5.27 V
C_3	6.01 V	6.03 V	6.03 V	6.05 V	6.06 V
C_4	5.26 V	5.30 V	5.29 V	5.32 V	5.32 V
C_5	6.01 V	6.04 V	6.06 V	6.10 V	6.12 V
C_6	5.27 V	5.31 V	5.33 V	5.37 V	5.40 V
C_7	4.89 V	5.43 V	5.75 V	5.90 V	6.07 V
C_8	4.63 V	5.14 V	5.45 V	5.60 V	5.73 V
C_9	5.51 V	5.40 V	5.47 V	5.70 V	5.97 V
C_{10}	5.24 V	5.12 V	5.15 V	5.40 V	5.65 V
C_{11}	5.45 V	5.29 V	5.40 V	5.67 V	5.79 V
C_{12}	5.19 V	5.02 V	5.13 V	5.39 V	5.48 V

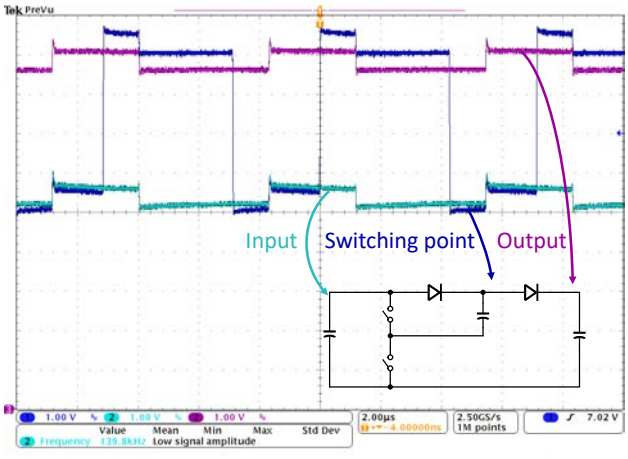


Figure 5.19: Measured double charge pump operation.

The measured gate drive voltage of each switch of the prototype is listed in Table 5.2 under various operating conditions. It can be seen that, the minimum gate drive voltage is greater than 4.5 V at start-up, which is sufficient to fully enhance the switch. When load current increases, the voltage difference between switches quickly reduces, leading to negligible on-resistance difference. The operations of the double charge pump and the gate-driven charge pump are captured and shown in Fig. 5.19 and Fig. 5.20. Table 5.3 compares the performance of the proposed gate drive power circuit with the isolated dc/dc converters used in [99]. The proposed solution takes much less space and has higher efficiency. Additionally, based on the

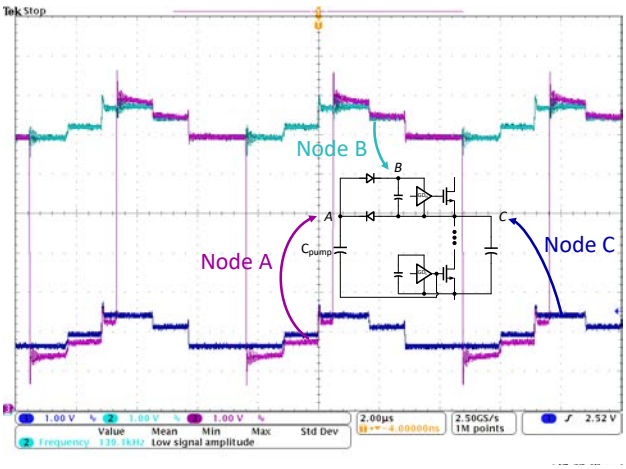


Figure 5.20: Measured gate-driven charge pump operation.

Table 5.3: Comparison with the state of the art solution

	Isolated DC/DC Converter	Proposed Circuit
Parts count	6 ICs, 36 caps and 12 res	11 diodes, 11 caps 5 LDOs and 2 res
Size	$> 6\times$ 112 mm^2	$\sim$ 130 mm^2
Efficiency	$< 27\%$	$\sim 41.7\%$
Cost	$\sim$ \$19.00	$\sim$ \$3.35

1000-unit price, it is found that the cost of the proposed solution is only 1/6 of the isolated dc/dc solution.

Hybrid SC Converters

The proposed methods are also applicable to the emerging hybrid and resonant switched-capacitor converters, as many of them share the same fundamental structures as FCML converters. An example gate drive power supply circuit for a 4-to-1 Dickson converter is shown in Fig. 5.21. Switch Q_5 can be powered by Q_3 with the cascaded bootstrap, and the diode forward drop is not a concern becuase of the overcharge effect at deadtime. Since Q_7 and Q_4 have a flying capacitor C_{fly} connected in between, a gate-driven charge pump can be used to power Q_7. If more switches and flying capacitors are added to the string for a higher conversion ratio, this method can be used repeatedly without issues.

A 4-to-1 series-parallel converter with its gate drive circuit is shown in Fig. 5.22. The three pairs of series and parallel switches ($Q_{\text{s1}}/Q_{\text{p1}}$, $Q_{\text{s2}}/Q_{\text{p2}}$, $Q_{\text{s3}}/Q_{\text{p3}}$) can be easily driven by

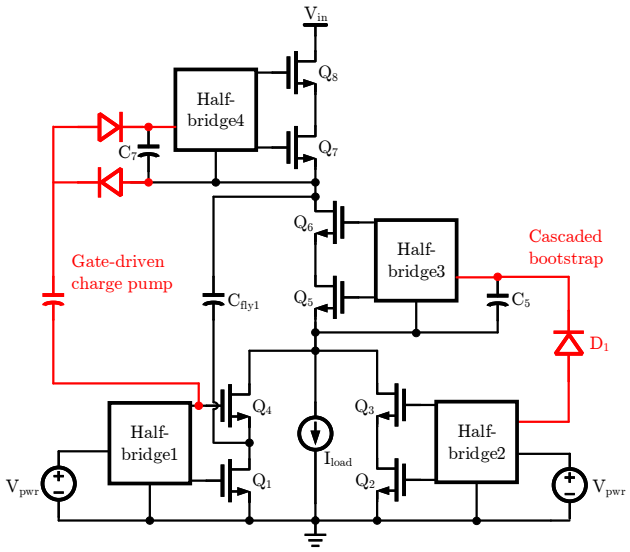


Figure 5.21: An example gate drive circuit for a 4-to-1 Dickson converter.

ground-referenced half-bridge drivers. Following Q_{s1}, there are four switches (Q_{p4}–Q_{p6}, Q_{s4}) that need to be powered by the cascaded bootstrap. Considering the large diode drop due to the high transferred power through the bootstrap diode, a double charge pump is used to guarantee sufficient voltage for all following switches. Note that the discussion above focuses on providing floating gate drive power only. For signal level-shifting, a high-side driver can be used instead of a half-bridge driver, at the expense of more ICs. In either case, these power supply methods remain valid.

Gate Driver IC Definition

The proposed cascaded bootstrap with LDO and the gate-driven charge pump could potentially be integrated with the GD itself. Fig. 5.23 shows the block diagram of a single isolated GD chip with a built-in LDO and two low-voltage diodes. A separate inverter buffer that has the same ground reference as the main GD is also added for dedicated gate-driven charge pump operation. As shown in Fig. 5.24, a four-level FCML converter can be driven by this standalone GD chip and a couple of decoupling capacitors and bootstrap diodes, without the need of any additional ICs. The bottom four GDs are powered through a cascaded bootstrap. Thanks to the built-in LDO, all GDs can have the same gate drive voltage. While the cascaded bootstrap can provide power to the top two GDs as well, gate-driven charge pumps can provide better gate drive power efficiency. With the built-in diodes and inverter buffer, GD_Q_6 can be powered by GD_Q_2, with one charge pump capacitor C_{pump1} only. Similarly, GD_Q_5 can be powered GD_Q_3.

Furthermore, this proposed GD chip can also be used for other hybrid SC converters.

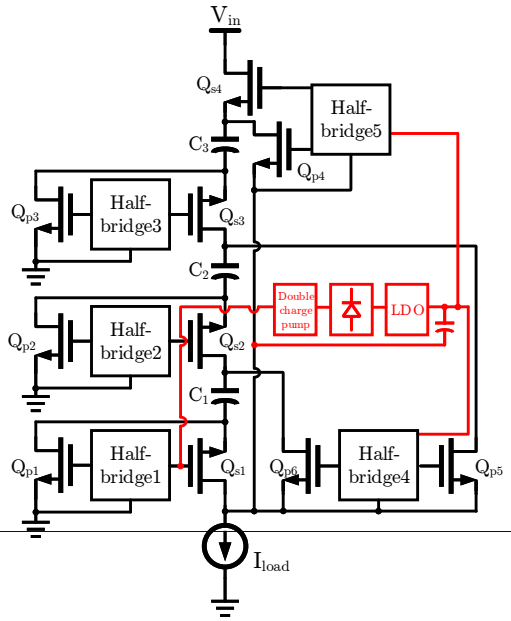


Figure 5.22: An example gate drive circuit for a 4-to-1 series-parallel converter.

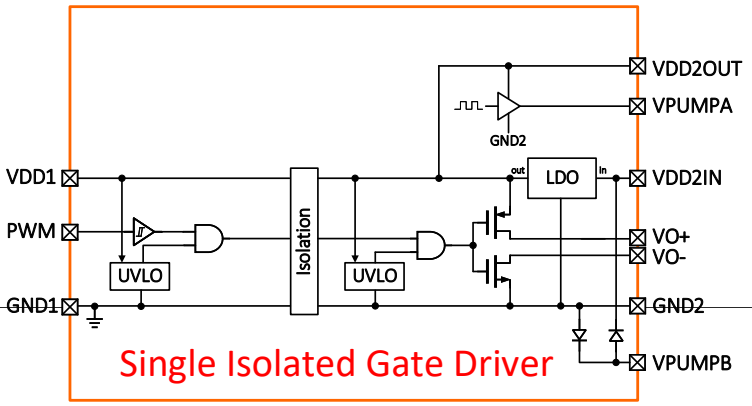


Figure 5.23: Block diagram of a proposed gate driver IC with built-in LDO and self-oscillatory inverter for cascaded bootstrap and gate-driven charge pump operations.

Through increased integration, the gate drive complexity and cost are reduced, and the power density and the reliability are improved, taking these emerging topologies a step closer to broader industry adoption.

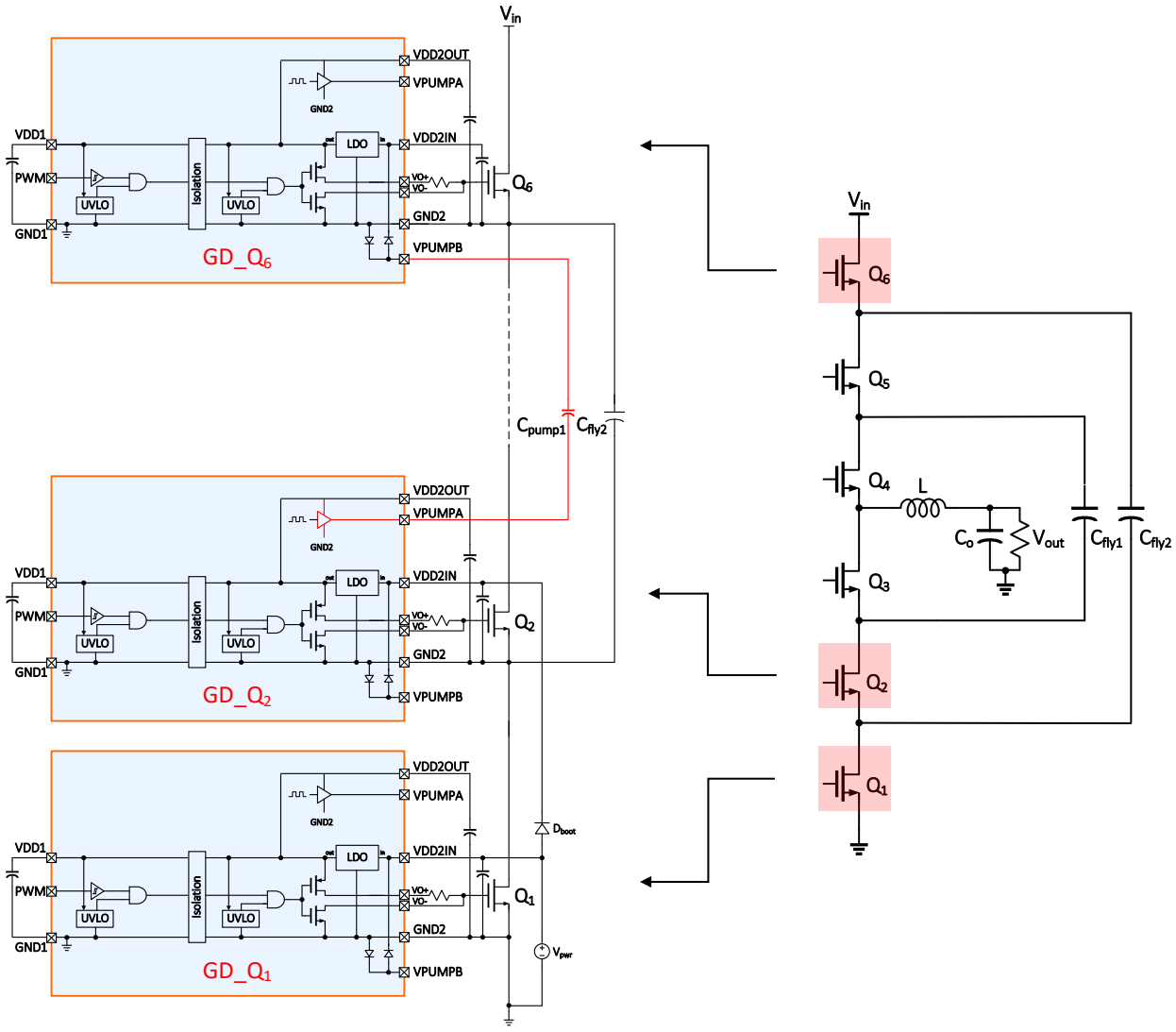


Figure 5.24: Powering a four-level FCML converter with the proposed gate driver IC.

5.8 Design Considerations

The proposed methods can potentially be applied to topologies beyond FCML and hybrid SC converters. To highlight their characteristics, the five methods are compared and summarized in Table 5.4. The first four focus on overcoming the forward voltage drops in the cascaded bootstrap operation, and the last method replaces bootstrap with a charge-pump based operation. The overcharge effect at deadtime can help compensate the forward drop of the bootstrap diode without the need for any additional circuits. However, it only applies to GaN switches and its effect depends on a number of factors. Usually, it can be safely used

Table 5.4: Key characteristics of the five proposed methods

Method	Basic structure	Constraints	Component counts	Efficiency	Notes
Bootstrap at deadtime	series connected switches	high	low	high	For GaN only. Operation depends on various factors, use with caution.
Cascaded bootstrap with LDOs	series connected switches	very low	low	depends on number of cascade	Low complexity, high applicability. Can power a large string of switches. Need high-voltage power supply.
Double charge pump	series connected switches	low	medium	low	Can boost the bootstrap voltage in the cascade at the cost of a relatively low efficiency.
Synchronous bootstrap	series connected switches	medium	medium	very high	Greatly reduced voltage drop compared to diode, but can still be a concern at extreme duty ratio and other cases.
Gate-driven charge pump	two switches with a flying capacitor in between	low	low	high	A preferred method to power the high-side switches of FCML converters and many hybrid SC converters.

to the last 1–2 switches in the cascade if their worst case voltages at no-load condition are already sufficient to enhance the switches. The overcharge effect at higher load can be used to further reduce the on-resistance. In comparison, the cascaded bootstrap method with LDOs has minimal constraints. If a high-voltage power supply is available, it can be used as a standalone method to drive any FCML converters and ladder-type SC converters, which have a large number of series-connected switches. Another method to get a sufficiently high bootstrap voltage is the double charge pump, which can be deployed anywhere in the converter. However, its efficiency ($\sim 50\%$) is relatively low compared to that of other methods and so should be used with caution. Thanks to the low on-resistance bootstrap eGaN FET, the synchronous bootstrap method can achieve very high efficiency. Nevertheless, the forward voltage drops can still be a problem when the duty ratio is extreme and there are many switches in the string. Instead of powering a large string, if two switches have a flying capacitor in between, a gate-driven charge pump can be a good option. This simple and low-cost charge pump can power the high-side switches of FCML converters and Dickson converters with an efficiency higher than the bootstrap-based methods.

5.9 Chapter Summary

This chapter presents five bootstrap and charge pump based methods for powering the floating GDs of FCML converters and hybrid SC converters with detailed analytical discussions and experimental verifications. Depending on the converter topology, one or more of the proposed methods can be selected to build a customized power supply circuit and transfer ground-referenced power to the large number of floating GDs in an effective and efficient manner. All these methods have simple structures and can be implemented with a few basic circuit components, such as diodes, capacitors, and LDOs. Various FCML converter prototypes are successfully built and tested to verify the functionality of the proposed methods.

Experimental results indicate that the customized power supply circuit is more efficient and compact than the widely used isolated dc/dc power supply chips, with significantly reduced cost. The pros and cons of the methods are also discussed and tabulated so that they can be properly applied to more topologies with floating switches.

Chapter 6

Cascaded Resonant Switched-Capacitor Converter

Resonant switched-capacitor (ReSC) converters have efficient utilization of both active and passive components, and hold the potential to achieve higher efficiency and higher power density than conventional SC and magnetic-based converters. This chapter presents a new ReSC converter topology, comprising two cascaded 2-to-1 ReSC converters, to address high-conversion-ratio applications. The proposed cascaded resonant converter has a simple structure and operating principle, and can achieve one of the best overall performance among popular ReSC topologies. A 36-60 V input, 4:1 fixed-ratio bus converter prototype for data center application is designed and constructed. We present detailed design guidelines and discussions addressing practical challenges, such as component variations and interstage decoupling requirements. With 48 V input and operating at the typical zero-current switching (ZCS) mode of ReSC converters, the prototype achieves a peak efficiency of 98.85% (including gate drive loss) and a power density of 2500 W/in^3, both of which are significantly higher than the-state-of-the-art. Furthermore, we propose a zero-voltage switching (ZVS) method to improve light-load efficiency. Through this control method, which greatly reduces the output capacitance loss, the prototype can maintain an efficiency above 97% starting from 3% of the rated load, with a peak of 99.0%.

6.1 Background and Motivation

In previous chapters, the fundamental limits and design techniques of hybrid and resonant SC converters are discussed. In this and the next two chapters, we focus on developing high-performance topologies and presenting cutting-edge hardware implementations. While the developed topologies are generic in nature, data center power delivery is selected as the core application we strive to work on, as it has become one of the most impactful fields which urgently needs innovative power electronics solutions. In modern data centers, there are various architectures to convert the 48 V bus voltage down to 1–2 V for digital

circuits. For the classic two-stage approach, ReSC converters can be used as intermediate bus converters to provide high-efficiency fixed-ratio conversion. This chapter discusses a high-performance 48-to-12 V solution based on a new ReSC topology, and Chapter 7 extends the ReSC discussion to higher conversion ratios. For the emerging single-stage approach, regulated hybrid SC converters with a merged buck stage can be used, and this approach is detailed in Chapter 8.

In this chapter, we focus on 4-to-1 fixed-ratio ReSC converters. As the name implies, ReSC converters operate at the resonant frequency of the flying capacitor and the augmenting inductor. This frequency is known as the minimum frequency (for inductor at output configuration) that allows full soft-charging operation. Since inductor volume is primarily dependent on the current rating, ReSC converters with minimum added inductance can be specifically suitable for low-voltage high-current applications like the commonly used 48-to-12 V conversion in data centers [23], [39], [102], where extreme efficiency and power density are critical, and voltage regulation is not required. As discussed in Section 3.3, with a given efficiency target, the capacitor and inductor values can be selected to achieve a minimal passive component volume, which can be significantly smaller than that of a conventional SC or a magnetic-based converter. Moreover, thanks to the resonant operation, zero-current switching (ZCS) is naturally achieved, and the switching loss caused by the simultaneous existence of switch voltage and current during switching transitions is minimized.

To further explore the potential of ReSC converters, we propose an interleaving-based method to cascade 2-to-1 ReSC converters for higher conversion ratios, in an efficient and compact manner. The proposed converter, named the cascaded resonant converter, inherits the simple structure and operating principle of its fundamental 2-to-1 element, and has the potential to outperform Dickson-based and FCML-based ReSC converters. In addition to the soft-charging and ZCS capabilities, we also demonstrate that zero-voltage switching (ZVS) operation is achievable, which can help eliminate the transistor output capacitance loss and further increase the efficiency.

A 36-60 V input, 4:1 fixed-ratio (unregulated), non-isolated bus converter prototype is designed and implemented based on the proposed topology. Depending on the deadtime and phase shift, the converter can operate in either ZCS or ZVS mode. Experimental results indicate that the ZVS operation can yield a higher light-load performance (efficiency remains above 97% starting from 3% of the rated load) and a higher peak efficiency (ZVS: 99.0%, ZCS: 98.85%, gate drive loss included). The prototype has a total box volume of 0.28 in^3 (4.586 cm^3), and has been tested with up to 60 A output current (900 W at 15 V output), leading to an ultra-high power density of 3100 W/in^3 (190 kW/L).

The remainder of this chapter is organized as follows. Section 6.2 gives a brief overview of the data center power delivery architecture. Section 6.3 discusses the basic (ZCS) operation of the proposed cascaded resonant converter, presents an interleaving technique to reduce the interstage decoupling requirement, and compares this topology with other ReSC converters. Section 6.4 provides hardware design guidelines and experimental results. Section 6.5 presents a ZVS control technique to further improve the performance of the converter, followed by a loss analysis and a comparison with the-state of-the-arts. Furthermore, Section

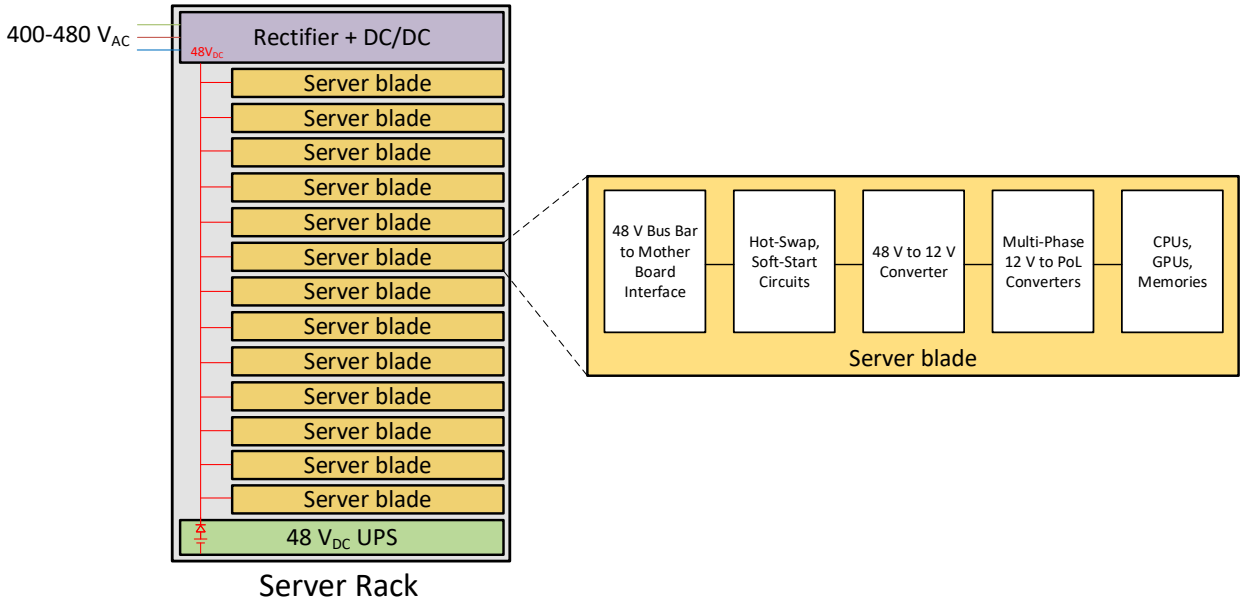


Figure 6.1: An example data center power delivery system from line to point-of-loads.

6.6 discusses the benefits of cascading and interleaving ReSC converters and generalizes the concept to other topologies.

6.2 Overview of Data Center Power Delivery Architecture

48 V Architecture

In [103], it is reported that in 2014, data centers used more than 1.8% of all electricity in the U.S. With emerging applications like data analytics, machine learning, artificial intelligence, and other high-performance computing use cases, the power consumption of data centers maintains a very fast growth rate. Therefore, improving the energy efficiency of data centers can have significant positive impacts, both economically and environmentally. In addition to efficiency, the increasing load current and power requirements on motherboards also pose great challenges for power integrity, thermal performance and reliability, and power density and scalability.

Because of the high bus bar and cabling loss and other limitations in the conventional 12 V distribution system, the industry has begun the transition to a 48 V distribution system. Compared to the 12 V architecture, the new 48 V architecture can reduce the distribution loss in the bus bars and interface components by up to 16x. Less copper planes and VIAs are needed due to the lower current flow at 48 V. Moreover, the 48 V bus also enables the

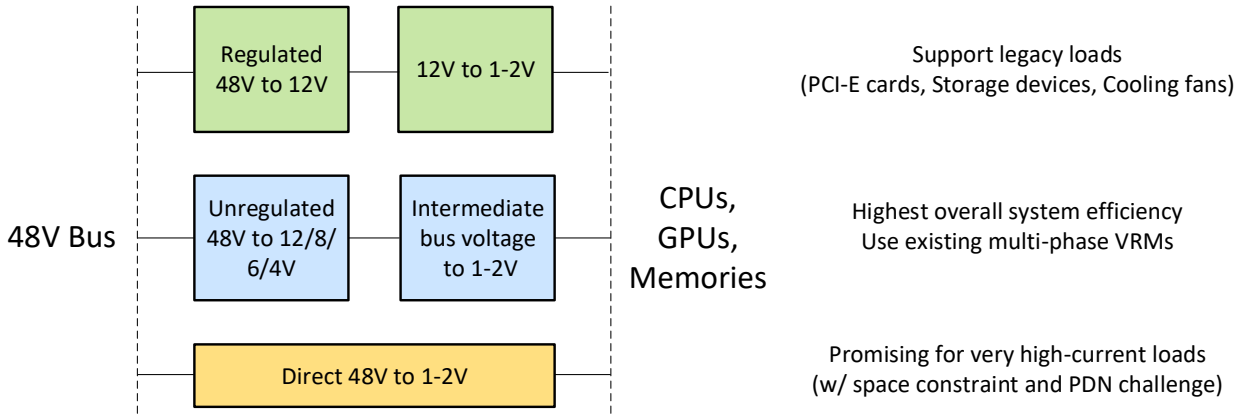


Figure 6.2: Comparison of different approaches to convert 48 V down to 1–2 V.

usage of in-rack back-up batteries during power outage, with better dynamic response and reliability. Since 48 V (48 V nominal, with a range of 36–60 V) is a safe voltage level for human contact during maintenance or accidental contact, galvanic isolation is not required (though the isolation function is typically still provided by the front-end converters) [104], and innovative non-isolated topologies with very high-performance can be adopted for step-down conversions from 48 V.

An example data center power delivery system with a 48 V dc bus is illustrated in Fig. 6.1. The three-phase line voltage is first stepped down to 48 V_{dc} through an in-rack rectifier. To convert the 48 V down to 1–2 V for digital loads, a two-stage intermediate bus architecture (IBA) can be used [105]. In contrast to other architectures, the majority of the power conversion in IBA is performed on the motherboard, from 48 V backplane to 12 V bus using a bus converter, and then down to 1 V using multi-phase buck converters [105], [106].

48 V to Point-of-Load Conversion

A major challenge in such systems is the conversion from the 48 V bus to the extreme low voltage and high current operating levels of CPUs and GPUs. Various approaches have been proposed to address such a high step-down conversion ratio, and the three major ones are illustrated in Fig. 6.2.

The first and the most straightforward approach is using regulated 48-to-12 V bus converters, followed by multi-phase 12 V to point-of-load (PoL) voltage regulation modules (VRMs). The regulated 48-to-12 V converters enable the quick adaptation of 12 V based work loads to the 48 V system, including legacy 12 V motherboards and other commodities such as PCI-E cards, hard drives and cooling fans. Compared to the 12 V loads, the majority of the power is stepped down again to 1–2 V for CPUs, GPUs, and other power-hungry digital circuits. Since the voltage regulation is typically provided by downstream converters,

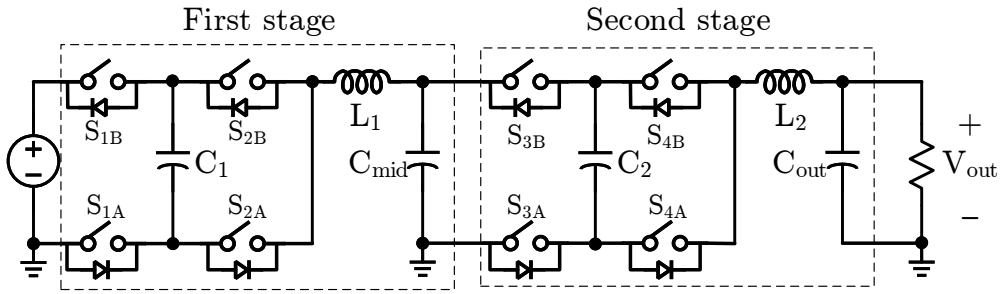


Figure 6.3: Schematic drawing of a cascaded resonant converter.

either in the 12V VRMs, or even on-chip using a fully integrated voltage regulation (FIVR) converter [107], the 12 V intermediate bus voltage does not need to be tightly regulated.

With the relaxed regulation requirement, innovative fixed-ratio topologies can be used to dramatically improve the performance of 48-to-12 V conversion. In this chapter, we propose a 4-to-1 cascaded resonant SC converter, which can have significantly higher efficiency and power density than other commonly used solutions.

Compared to a 12 V bus voltage, recent research [104], [108] suggests that a lower intermediate bus voltage (e.g., 6 V) may provide higher overall efficiency, once both the intermediate bus converters and the second-stage VRMs are considered. Moreover, with the reduced voltage stress at the second stage, the VRMs can have smaller inductors and therefore be placed closer to the input power pins of the load. This can reduce the power loss and improve the dynamic response associated with the power distribution network (PDN), which is particularly important for the application-specific integrated circuits (ASICs) with very high current demand. In Chapter 7, we propose new multi-resonant SC topologies with high conversion ratios for this improved two-stage approach.

In addition to two-stage approaches, a single-stage, direct 48 V to PoL approach has also been explored [109]–[113]. With well-defined specification of the targeted loads, a dedicated singe-stage design may provide better overall efficiency, power density, and reduced system cost. The power stamp alliance (PSA) has worked on defining a standard product footprint and functions that provide a standard modular board-mounted 48V-to-PoL solution [111]. In Chapter 8, we present a hybrid SC based solution which has achieved promising performance according to the PSA specifications.

6.3 Cascaded Resonant Converter

Operating Principle

The schematic drawing of the cascaded resonant converter is shown in Fig. 6.3, which can be seen as a cascade of two 2-to-1 SC structures with an inductor at each output. Although the operating principle is completely different, this topology can be viewed as two cascaded three-

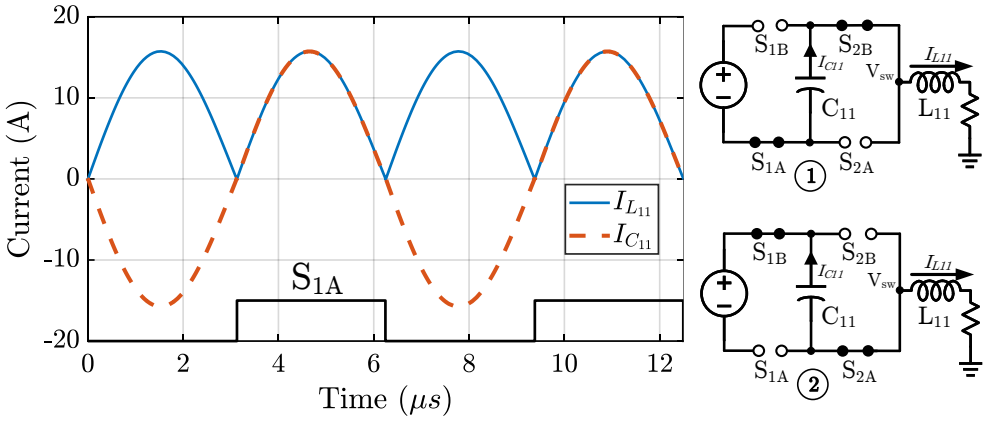


Figure 6.4: Simulated inductor/capacitor current at first stage.

level buck converters. Alternatively, the topology can also be viewed as an augmented 4-to-1 doubler SC converter [7], with two inductors inserted to achieve soft-charging operation. To achieve ultra efficient and compact fixed ratio (no regulation capabiliy) resonant operation, all switches have a fixed duty ratio of 50%, and every two adjacent switches have a phase shift of 180°. The nominal switching frequency is the resonant frequency of the flying capacitor and the inductor ($f_{\text{sw}} = \frac{1}{2\pi\sqrt{L_1 C_1}} = \frac{1}{2\pi\sqrt{L_2 C_2}}$), as it is the minimum frequency with low conduction loss for soft-charging hybrid SC converters [19]. As shown in Fig. 6.4, the flying capacitors are resonantly charged in one state and discharged in the other state, resulting in no charge-redistribution loss. Additionally, since the inductor current takes the shape of a rectified sine wave, the current reaches zero at moments of phase transitions and ZCS is achieved when switching at this frequency.

However, converters operated in this way require the point of coupling between the cascaded converters to present a stiff voltage, thus enforcing $C_{\text{mid}} \gg C_1$ & C_2, so that C_{mid} does not take part in the resonant operation. Consequently, the volume of C_{mid} could dominate the size of the capacitors. As shown in Fig. 6.5, to avoid such penalty, we propose to introduce a second cascaded resonant converter, connected in parallel with the first converter at the input, middle and output point, and operated 180° out of phase. It can be seen from Fig. 6.6 that, with this interleaving operation, the combined input current of the second stage also becomes a rectified sine wave, which closely matches the inductor current of the first stage. Thus, an equal amount of charge is delivered and removed from C_{mid} at all times, ensuring a stiff midpoint voltage without requiring a large capacitor. The proposed control technique and interleaved topology thus enable a significant reduction of C_{mid} while still ensuring correct resonant operation. If multi-phase interleaving is used for higher load current, one should make sure that the number of phases is an even number such that every pair of phases can be 180° out of phase to cancel out C_{mid}. Moreover, since the first stage and the second stage have the same operating principle, the total input source current also becomes a continuous rectified sinusoidal current owing to the two-phase interleaving opera-

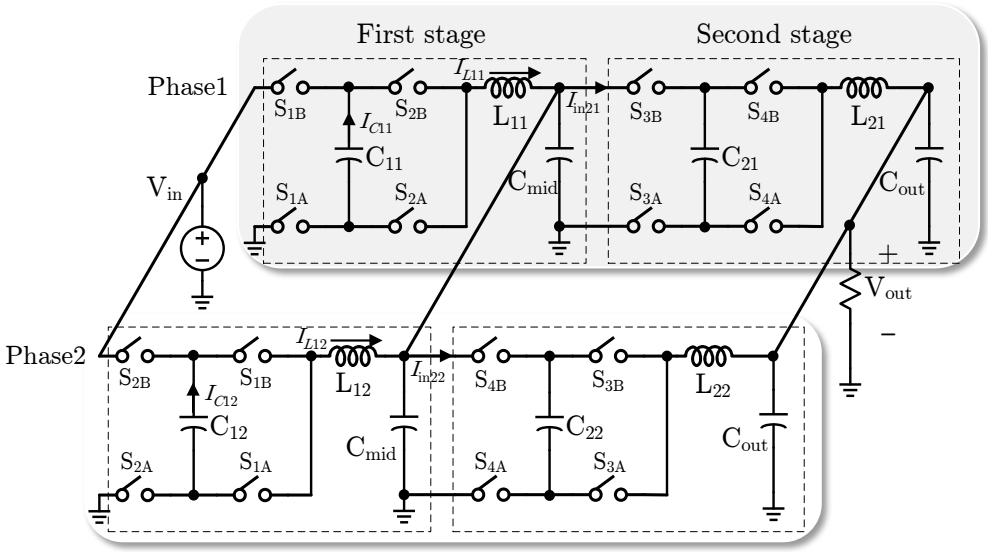


Figure 6.5: Schematic drawing of a two-phase interleaved cascaded resonant converter.

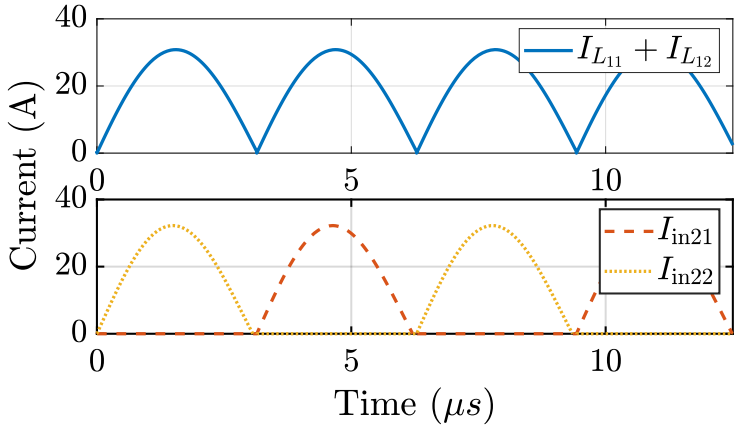


Figure 6.6: Minimize C_{mid} with interleaved design.

tion. This non-pulsating input current can greatly reduce the input decoupling requirement and simplify the EMI filter design.

Topology Comparison

To illustrate the theoretical performance of the cascaded resonant converter, we replot Fig. 3.17 in Fig. 6.7. Generally speaking, switch stress reflects power loss and passive component volume reflects power density. For the same switching frequency, a lower total switch stress indicates a potentially lower conduction loss, lower switching loss, and smaller size. Thus, a converter with lower switch stress can operate at a higher switching frequency for

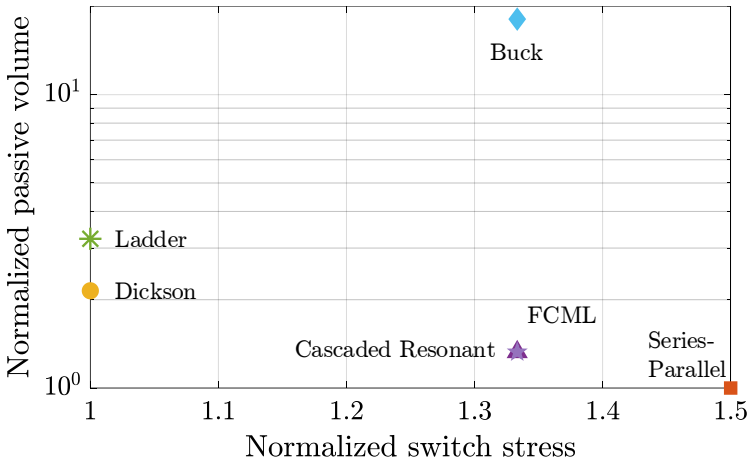


Figure 6.7: Comparison of various ReSC converters at a conversion ratio of 4-to-1.

the same amount of loss, which results in reduction of passive component volume. Therefore, comparing both metrics can be indicative of the overall performance potential of the converter.

Fig. 6.7 shows the calculated metrics of various topologies for delivering the same amount of power, at a conversion ratio of 4-to-1. The metrics are normalized with respect to the topology that has the lowest rating (i.e., the best performance). It is shown that all ReSC converters out-perform the buck converter by a wide margin, assuming the energy density of capacitors is 100 times higher than that of inductors. Among the ReSC converters, the split-phase Dickson converter with a single inductor at the output [21] has the best switch utilization, but has relatively large passive volume. On the other hand, the series-parallel converter with a single inductor at the output [41] has the best passive component utilization, but has high switch stress. In comparison, the proposed cascaded resonant converter has a good balance of active and passive component utilization, indicating the potential to achieve high efficiency and high power density simultaneously.

It should be noted that practical converter designs have more considerations regarding the circuit complexity and the actual performance of different topologies can be different than what is plotted here. For instance, as ReSC converters have a large number of floating switches, the switch quantity and the complexity of gate drive circuit is also an important design knob that affects the overall performance. In addition, the soft-switching ability and the characteristic of the input source current can affect EMI, and the number of passive components and the associated parasitic resistance can contribute additional conduction loss. After a comprehensive analysis of the theoretical performance, the available components on the market and the ease of gate drive circuit design/layout, the cascaded resonant topology is found to be the optimum ReSC solution for data center intermediate bus converters.

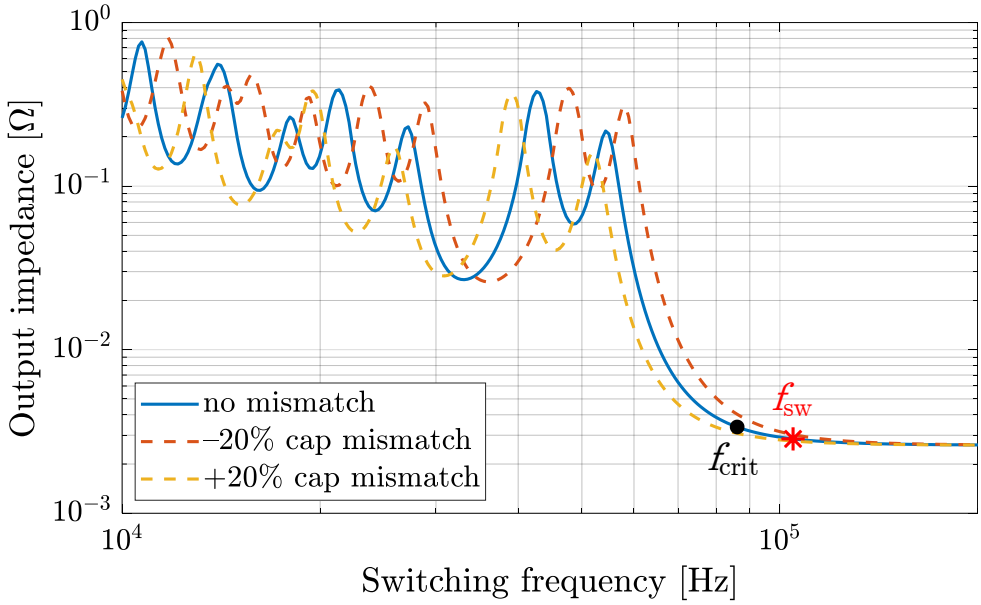


Figure 6.8: Output impedance plot for cascaded resonant converter.

6.4 Design Guidelines and Experimental Results

Component Tolerance

In practical implementations, both the flying capacitor and the resonant inductor can deviate from their nominal values due to various reasons [114], and make it difficult to guarantee perfect resonant operation. To study the effects of component variations on the cascaded resonant converter, its output impedance with respect to the tolerance of the flying capacitor (nominal capacitance and 20% mismatch) is simulated in LTspice with a frequency sweep from 10 kHz to 200 kHz, and the result is plotted in Fig. 6.8. As expected, at the resonant frequency f_{crit}, the output impedance increases if the actual flying capacitors are smaller than their nominal values. On the other hand, when operating in the FSL region, the output impedance is insensitive to the capacitor variance. Therefore, for better component tolerance, it is worthwhile to trade off the ZCS operation at f_{crit}, and to operate the cascaded resonant converter at a slightly higher switching frequency. Moreover, for the high-current IBA application, the slight reduction of output impedance (and therefore conduction loss) in the FSL region may cancel out the increase in switching loss, and lead to a higher overall efficiency.

Thanks to this mitigation method, the cascaded resonant converter can have relatively good component tolerance. Thus, high-energy-density (which is comparable to electrolytic) low-dissipation-factor (typically less than 5%) Class-II ceramic capacitor can be used, despite of its dc-bias and temperature varying characteristics. By contrast, for those ReSC converters with the "inductor in series with capacitor" configuration, it is often necessary to use high

precision Class-I ceramic capacitors for perfect resonant operation, at the expense of higher cost and lower energy density.

Loss Calculation

To better understand the loss distribution of the cascaded resonant converter, here we provide the calculation of the main sources of the losses. As will be shown in the experimental results, the conduction loss dominates in this kind of low-voltage high-current application. The total conduction loss can be calculated with $P_{\text{cond}} = P_{\text{cond,1}} + P_{\text{cond,2}}$, where $P_{\text{cond,1}}$ is the conduction loss of the first stage and $P_{\text{cond,2}}$ is the conduction loss of the second stage. At stage i (i $\in \{1, 2\}$), $P_{\text{cond,i}} = \sum_{j=1}^{2} I_{\text{rms,i}}^2 R_i$, where j is the number of phases and R_i is the sum of the series resistance in the current path, including switch on-resistance, capacitor ESR, inductor DCR and PCB trace resistance. The rms current can be alternatively expressed in terms of the average output current and the rms-to-average ratio: $I_{\text{rms,i}} = K_i I_{\text{out,i}}$. For perfect resonant operation where the inductor current is a rectified sine wave, $K_i = 1.11$. For higher switching frequency, K_i starts to decrease and approach 1. Its exact value can be determined from circuit simulation. Similarly, the converter switching loss needs to be calculated for every stage and every phase individually: $P_{\text{sw}} = \sum_{i=1}^{2} P_{\text{sw,i}}$, and $P_{\text{sw,i}} = \sum_{j=1}^{2} (P_{\text{coss,i}} + P_{\text{overlap,i}})$. The switch output capacitance loss $P_{\text{coss,i}}$ is given by $P_{\text{coss,i}} = n \cdot \frac{1}{2} f_{\text{sw}} C_{\text{oss,i}} V_{\text{ds,i}}^2$, where n is the number of switches (4 in this case), $C_{\text{oss,i}}$ is the switch output capacitance and $V_{\text{ds,i}}$ is the voltage across the switch before it turns on. Note that this portion of the loss can be eliminated by the ZVS control technique that is introduced in the next section. The switch overlap loss can be approximately given by $P_{\text{overlap,i}} = n \cdot \frac{1}{2} V_{\text{off}} I_{\text{on}} (t_{\text{turn-on}} + t_{\text{turn-off}})$, where V_{off} is the off-state voltage, I_{on} is the on-state current, and $t_{\text{turn-on}}$ and $t_{\text{turn-off}}$ are the duration for which the voltage and current overlap when the switch turns on and turns off, respectively. When operating at the resonant frequency, the converter is in ZCS mode and this overlap loss is nonexistent. However, as discussed above, the converter is recommended to operate slightly faster for lower conduction loss and better tolerance to component variations. This way, the converter has non-zero turn-off current and associated turn-off overlap loss, whereas the turn-on current is still close to zero with negligible turn-on loss.

Hardware Design

The added inductor offers an additional degree of freedom in the design space. The values of capacitors and inductors should be designed to reach a desired resonant frequency, while minimizing the total passive component volume. The lower bound of the capacitance needed is set by the allowed capacitor voltage ripple and temperature rise. Although the hybrid resonant operation allows larger RMS current through capacitors than regular SC converters without efficiency penalty, the associated capacitor voltage ripple ($\Delta V_{C_{fly}} = \frac{I_{\text{out}}}{2 f_{\text{sw}} C_{\text{fly}}}$) will be present across the switches and must be considered when selecting switches. In addition, the temperature rise of a capacitor is also a function of RMS current, and should ideally be kept low (e.g., 10 °C) for reliability purposes. In terms of inductor selection, the saturation

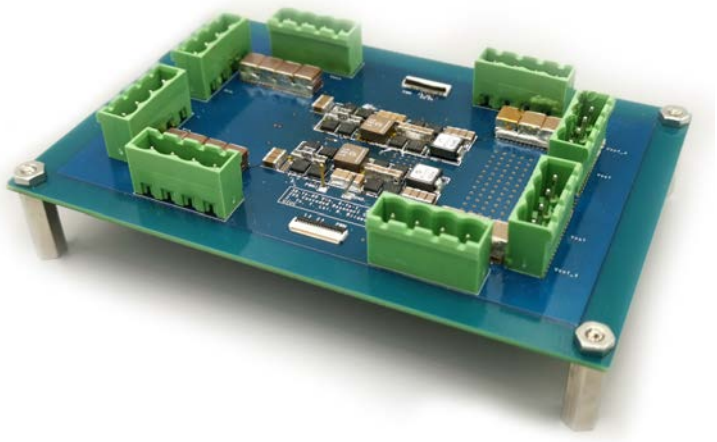


Figure 6.9: Photograph of the hardware prototype (two-phase interleaved).

Table 6.1: Main component listing of the cascaded resonant converter

Component	Part number	Parameters
1st stage MOSFET	Infineon BSZ025N04LS	40 V, 2.5 mΩ
1st stage flying capacitor (C_1)	TDK C2012X5R1V226M125AC	35 V, 22 μF*×12
1st stage inductor (L_1)	Coilcraft XAL6030-181MEL	180 nH, 39 A I_{sat}
1st stage output capacitor (C_{mid})	TDK C3216X5R1H106K160AB	50 V, 10 μF*×19
2nd stage MOSFET	Infineon BSZ013NE2LS5I	25 V, 1.3 mΩ
2nd stage flying capacitor (C_2)	TDK CGA4J1X5R1C106K125AC	16 V, 10 μF*×16
2nd stage inductor (L_2)	Coilcraft SLC7530S-500ML	50 nH, 50 A I_{sat}
2nd stage output capacitor (C_{out})	TDK C3216X5R1E476M160AC	25 V, 47 μF*×8
Gate driver	Texas Instruments LM5113	100 V half-bridge
Bootstrap diode	Infineon BAT6402VH6327XTSA1	40 V Schottky

* The capacitance listed here is the nominal value before dc derating.

current (I_{sat}) will likely become the most constraining factor, because of the high peak current ($\frac{\pi}{2}I_{out}$) in resonant operation. Given constrained inductor height and volume, it is recommended to use the highest inductance that can satisfy the I_{sat} requirement. Besides optimizing the passive component volume, the ESR of the capacitors and the DCR of the inductors are also important design metrics that can significantly affect the efficiency.

Owing to the unique structure of the cascaded resonant topology, each switch only needs to block half of the input voltage (30 V for the 1st stage and 15 V for the 2nd stage) plus the

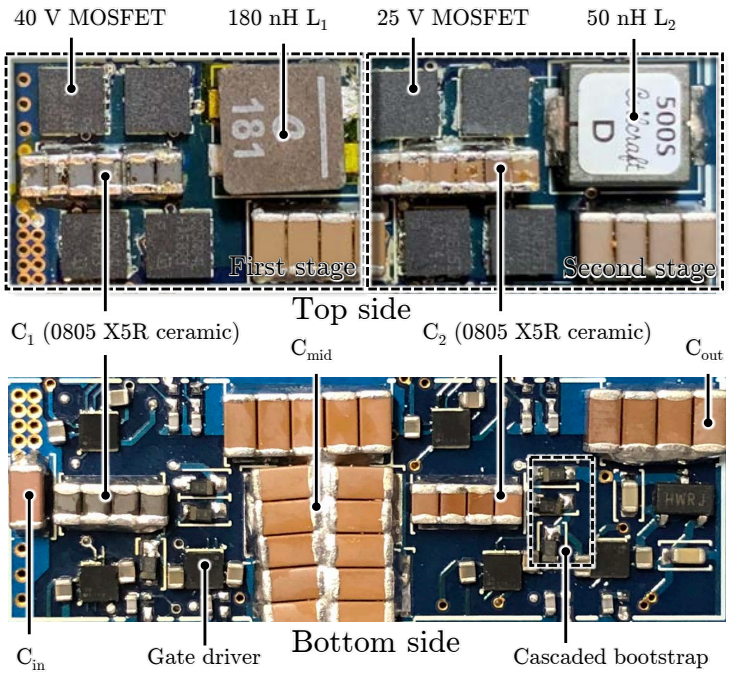


Figure 6.10: Annotated photograph of the converter (one phase).
Dimensions: 1.38×0.46×0.22 inch (3.5×1.17×0.56 cm).

capacitor voltage ripple, allowing the use of low voltage MOSFETs (40 V and 25 V). Note that at this voltage rating, eGaN FETs generally do not outperform silicon MOSFET significantly (with slightly lower input/output capacitance and similar on-resistance/footprint), but have a much higher cost [115], [116]. Since the designed resonant frequency is relatively low ($\sim$ 100 kHz), the switching loss is not a dominating factor and MOSFETs are a better choice from a cost perspective.

In order to decrease the size and the power consumption of the gate drive circuit, high side gate drivers (with internal level-shifters) are used to drive the floating switches, and the cascaded bootstrap method presented in Chapter 5 is applied to provide the required floating gate drive power. Since this topology relies on its natural balancing property [117] to maintain the flying capacitor voltage at its desired value, the timing of the control signals (duty ratio, phase shift and gate drive propagation delay) should be carefully matched for all switches [118]. The photograph of the two-phase interleaved hardware prototype (with connectors and additional filter capacitors) is shown in Fig. 6.9. The PCB is a standard, low-cost 4-layer board with 2 oz copper. Fig. 6.10 provides a closer look of the converter (one phase) with key components highlighted. The metrics of the LC tanks as well as the other main components can be found from Table 6.1. Based on the largest quantity sell price on Digikey, the total cost of the main components is $\sim$ \$70, excluding the cost of the PCB and the micro-controller. In particular, the gate drivers and the capacitors each contributes about 40% to the total cost.

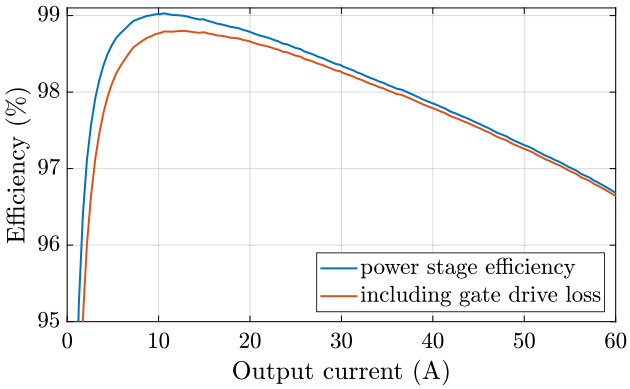


Figure 6.11: Measured 36 V to 9 V efficiency (f_{sw} = 91 kHz).

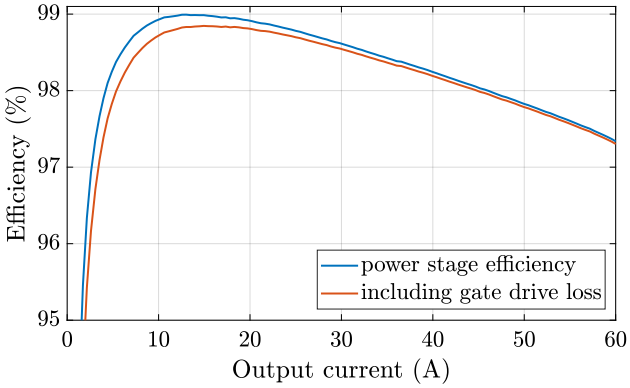


Figure 6.12: Measured 48 V to 12 V efficiency (f_{sw} = 100 kHz).

ZCS Experimental Results

The two-phase interleaved prototype has been tested with up to 60 A output current with a Yokogawa WT3000E precision power meter. The converter can output 900 W power in 60-to-15 V conversion, with a very high power density of 3100 W/in^3 or 190 kW/L. The total volume is the sum of the two phases and the volume of each phase is measured by the smallest rectangular box that can contain the converter (the x and y dimensions are shown in Fig. 6.10 and the z dimension is the sum of the thickness of the PCB and the tallest components on the top and bottom sides of the board). For 48-to-12 V conversion, the power density is 2500 W/in^3 or 152 kW/L. Higher power density can be expected with further component optimization, as the current commercial off-the-shelf inductors (maximum height of 0.118 inch) are much taller than the other components (maximum height of 0.071 inch).

The efficiency performance at various input voltages are measured and plotted in Fig 6.11

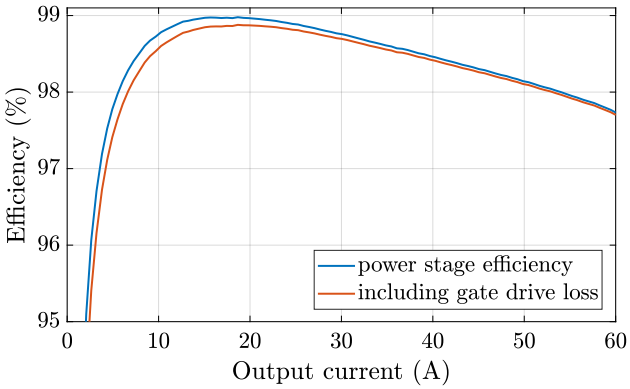


Figure 6.13: Measured 60 V to 15 V efficiency ($f_{\text{sw}} = 111$ kHz).

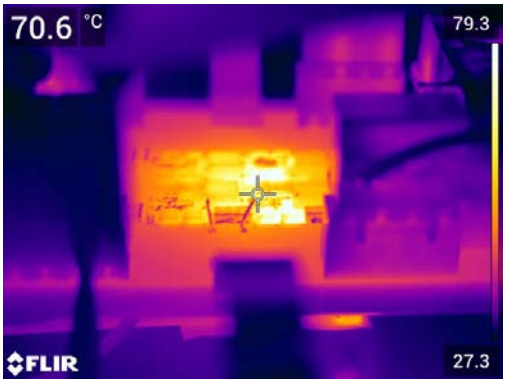


Figure 6.14: Thermal performance with fan cooling only ($V_{\text{in}} = 48$ V, $I_{\text{out}} = 60$ A).

to Fig 6.13. By slightly tuning the switching frequency, the prototype can achieve 99.0% peak power stage efficiency across the entire input range. For the commonly used 48-to-12 V conversion, the overall efficiency (including gate drive loss) has a peak of 98.85%, and maintains 97.23% at full power. This excellent efficiency performance can significantly reduce the complexity of thermal management design. As shown in Fig. 6.14, the converter can operate at a reasonable temperature at full power with fan cooling only. In addition, the high efficiency also reduces the impact of load regulation. Although the converter is in fixed-ratio mode (open loop), its output voltage only droops 350 mV (3% of V_{out}) at full load. Thanks to the sufficient C_{mid} onboard, the two phases can also operate independently (no interleaving) with comparable efficiency performance, providing extra redundancy and robustness. Furthermore, phase-shedding can be implemented to improve light-load efficiency.

As shown in Fig. 6.15, the two-phase interleaved inductor currents have good current sharing, and the converter is operating at a frequency slightly higher than the resonant frequency with imperfect ZCS. Moreover, the currents at the second stage take a shape similar to that in the first stage (shown in Fig. 6.16), which can significantly reduce the

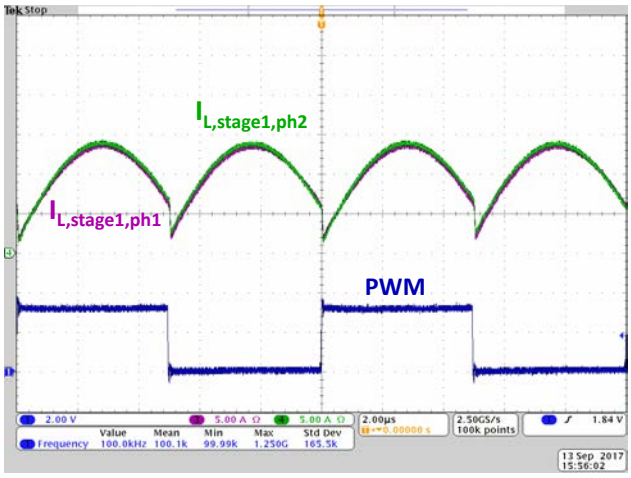


Figure 6.15: The interleaved inductor currents at the first stage.

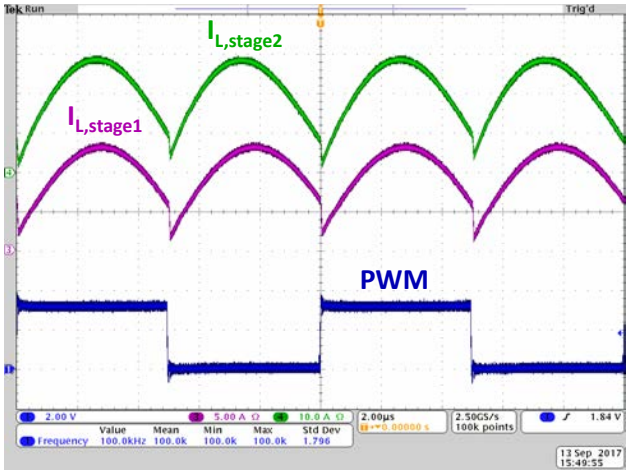


Figure 6.16: The inductor currents of the two stages (one phase).

decoupling requirement of C_{mid}. The prototype is also able to handle large load transients. In Fig. 6.17, a load step from 10 A to 30 A is introduced. The observed output voltage does not show significant undershoot, and stabilizes within a few switching cycles.

6.5 Zero Voltage Switching Technique

Theoretical Analysis

Compared to ZCS, ZVS can further reduce the switching loss contributed by the transistor output capacitance ($P_{\text{Coss}} \simeq \frac{1}{2} f_{\text{sw}} C_{\text{oss}} V_{\text{ds}}^2$), and greatly improve the light-load efficiency. Interestingly, the ZVS realization of ReSC converters demands that the switching frequency is higher than the resonant frequency [119], [120], which coincides with the strategy to improve component tolerance discussed in the last section. Here, we propose a technique to operate

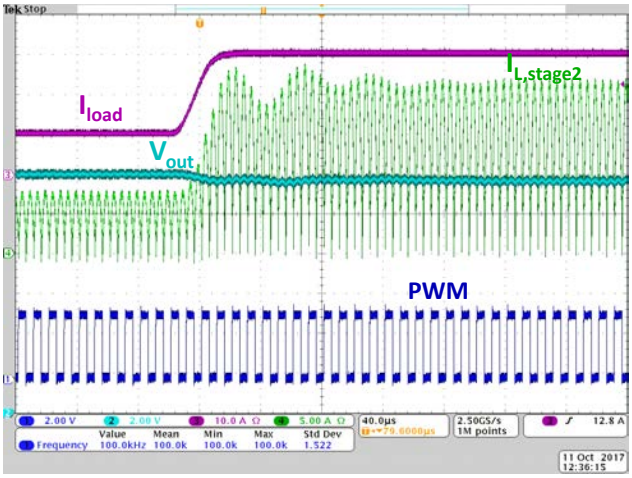


Figure 6.17: Transient response of 10 A to 30 A load step.

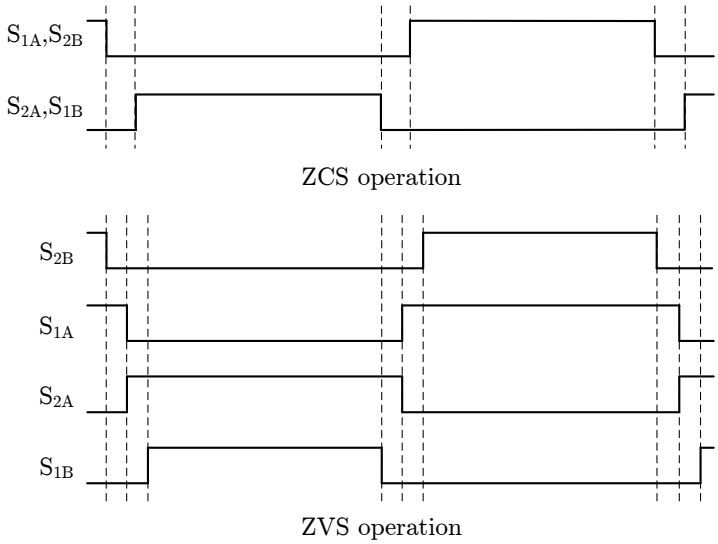


Figure 6.18: Control signals for different modes of operation.

the cascaded resonant converter in ZVS mode, and the required modifications of the control signals are shown in Fig. 6.18.

To turn on a switch with ZVS, one sufficient condition is that the body diode is conducting before the switch turns on. This condition demands that the current flowing through the switch is negative (from source to drain) during the switch turn-on period. In order for the cascaded resonant converter to fulfill the ZVS requirement, the bottom switches (S_{1A} - S_{4A} in Fig. 6.3) need to turn on when the inductor current is positive, and the top switches (S_{1B} - S_{4B}) need to turn on when the inductor current is negative.

The waveforms of the inductor current and switch node voltage in ZVS mode are depicted in Fig. 6.19, and a zoomed-in view of the switching transition is shown in Fig. 6.20. Since

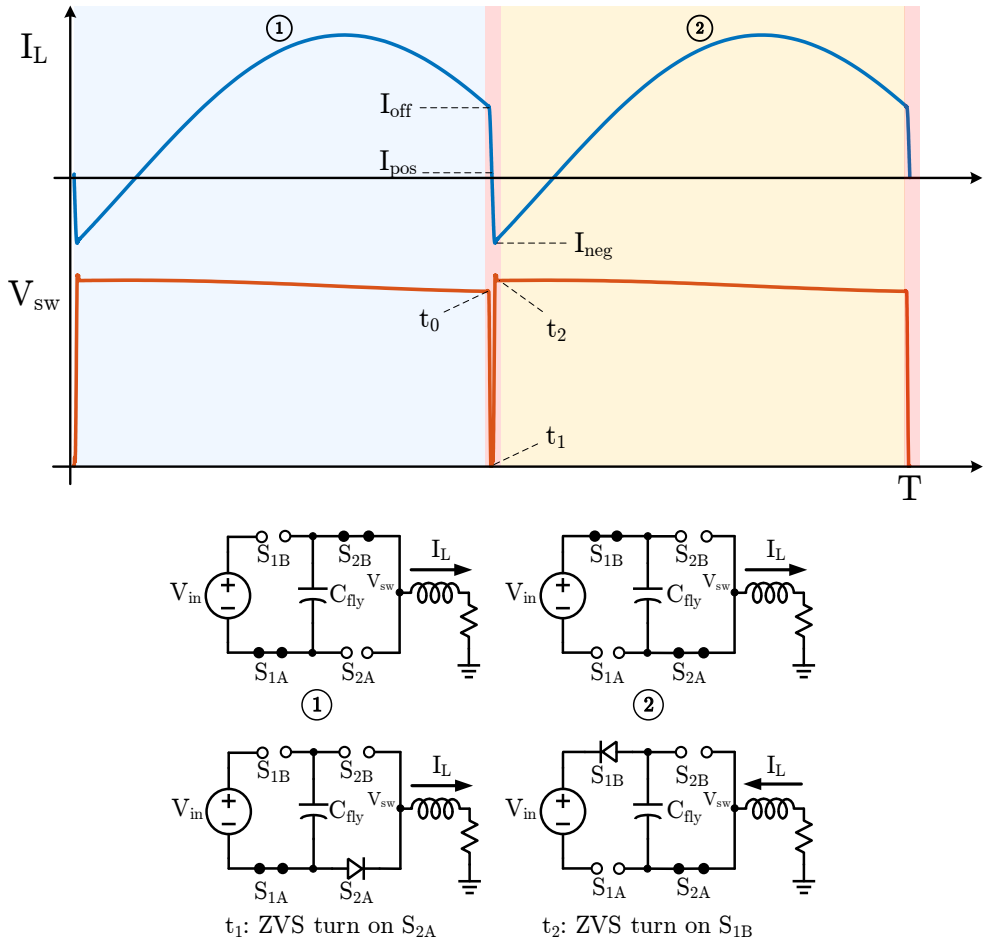


Figure 6.19: Zero voltage switching operation on cascaded resonant converter.

the switching frequency is higher than the resonant frequency, the inductor current remains positive ($I_{\mathrm{L}} = I_{\mathrm{off}}$) at the end of state 1. After switch $\mathrm{S_{2B}}$ is turned off at $t = t_0$ (which will introduce V-I overlap turn-off loss), the positive inductor current begins to discharge the C_{oss} of $\mathrm{S_{2A}}$ and to charge the C_{oss} of $\mathrm{S_{2B}}$ simultaneously. Assuming the drain-to-source voltage V_{DS} of $\mathrm{S_{2A}}$ decreases to 0 (V_{sw} also decreases to 0) while the inductor current is still greater than zero, the body diode of $\mathrm{S_{2A}}$ will begin to conduct. Thus, at $t = t_1$, $\mathrm{S_{2A}}$ can be softly turned on with a slightly positive inductor current ($I_{\mathrm{L}} = I_{\mathrm{pos}} \simeq 0$), and $\mathrm{S_{1A}}$ can be turned off at the same time with near-zero turn-off loss. Notice that if $\mathrm{S_{2A}}$ is not turned on in time and the inductor current reverses polarity, the C_{oss} of $\mathrm{S_{2A}}$ will be charged back up again and the ZVS condition is missed.

Since the switch node voltage V_{sw} is zero after $\mathrm{S_{2A}}$ is turned on at $t = t_1$, the inductor current will become negative, and resonantly charge the C_{oss} of $\mathrm{S_{1A}}$ (and discharge the C_{oss} of $\mathrm{S_{1B}}$). Given sufficient time, the V_{DS} of $\mathrm{S_{1B}}$ decreases to 0 (and V_{sw} goes back to $\frac{V_{\mathrm{in}}}{2}$) while the negative inductor current remains a near constant value flowing through $\mathrm{S_{1B}}$'s body diode.

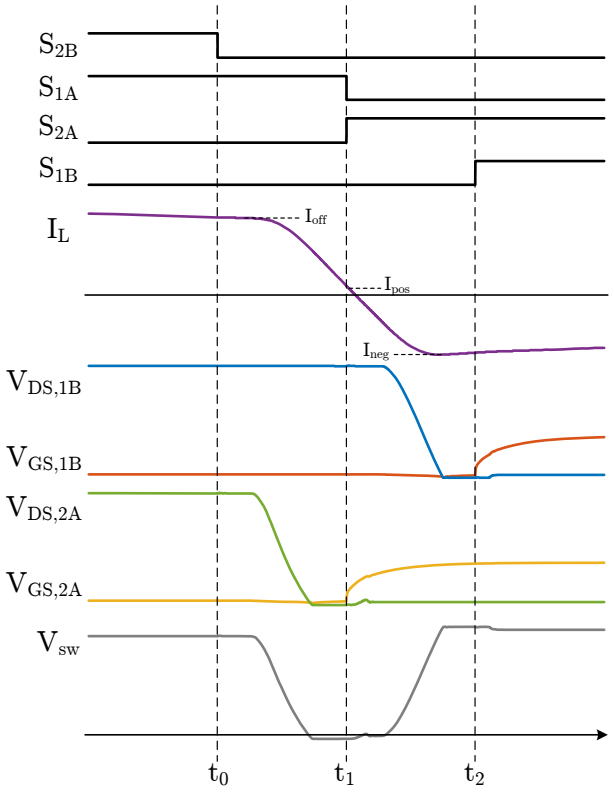


Figure 6.20: Detailed view at the ZVS switching moment.

Finally, S_{1B} is turned on with ZVS at $t = t_2$ and the converter enters the next main operating state (state 2), after which S_{1A} and S_{2B} achieve ZVS turn-on.

To achieve the aforementioned ZVS operation, there are a few requirements on the design and control of the converter. First, the inductor needs to have sufficient energy to charge and discharge the transistor output capacitances (or equivalently the switch node capacitance):

$$LI_{\text{off}}^2 > C_{\text{oss,tot}} V_{\text{out}}^2 \tag{6.1}$$

$$LI_{\text{neg}}^2 > C_{\text{oss,tot}} V_{\text{out}}^2 \tag{6.2}$$

where $C_{\text{oss,tot}} = 2C_{\text{oss}}$ is the sum of the output capacitances of a pair of low-side and high-side switches. Since C_{oss} is a nonlinear function of V_{DS}, the charge equivalent value should be used as discussed in [121]:

$$C_{oss,Q\text{eq}}(V_{\text{DS}}) = \frac{Q_{\text{oss}}(V_{\text{DS}})}{V_{\text{DS}}} = \frac{\int_0^{V_{\text{DS}}} C_{\text{oss}}(v)dv}{V_{\text{DS}}}. \tag{6.3}$$

It can be observed from (6.1) that, given fixed output capacitance energy, a higher inductance is desired as it can reduce the required turn-off current I_{off} and thereby turn-off switching

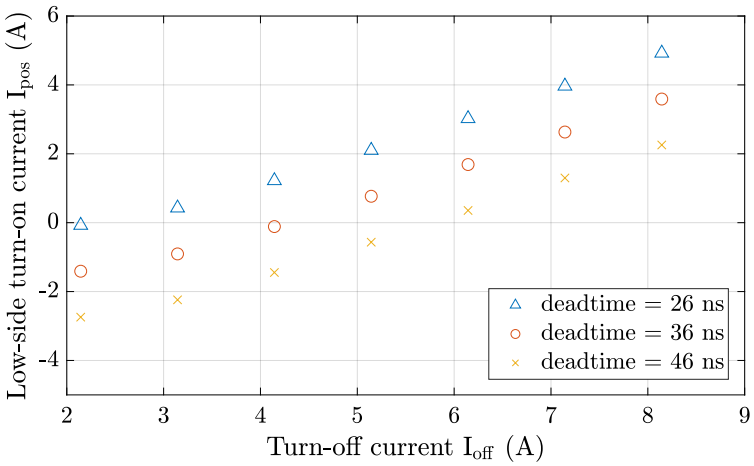


Figure 6.21: Effect of deadtime on the turn-on of low-side switch (L = 180 nH, $C_{\text{oss,tot}}$ = 1.5 nF).

loss. The minimum I_{off} and I_{neg} can be derived from (6.1) and (6.2):

$$I_{\text{off,min}} = I_{\text{neg}} = \sqrt{\frac{C_{\text{oss,tot}} V_{\text{out}}^2}{L}}. \tag{6.4}$$

Assuming the low-side switch (e.g., S_{2A} in Fig. 6.20) turns on at exactly $I_{\text{pos}} = 0$, then the minimum deadtime $t_{\text{dead,min}} = t_2 - t_1$ to reach I_{neg} can be easily found to be one quarter of the resonant period:

$$t_{\text{dead,min}} = \frac{\pi}{2}\sqrt{LC_{\text{oss,tot}}}, \tag{6.5}$$

which sets the lower bound of the deadtime to turn on a high-side switch with ZVS. Fig. 6.21 illustrates the effects of a longer deadtime on the switching operation, using the circuit parameters of the first stage of the designed prototype. It can be seen that, with longer deadtime (e.g., $t_0 - t_1$ in Fig. 6.20), the turn-on current of the low-side switch, I_{pos}, may become negative when the turn-off current I_{off} is relatively low, indicating the absence of ZVS at light load. Thus, to achieve optimum light-load efficiency with ZVS, the deadtime should be set close to (6.5), as deviations below and above this value will both lead to imperfect ZVS and higher switching loss. Similarly, the switching frequency should be selected properly such that the turn-off current I_{off} is close to the value defined in (6.4) at light load.

The switching behavior of the switches with a deadtime of (6.5) is shown in Fig. 6.22. At light to medium load where I_{off} is relatively low ($\sim$ 2 A to $\sim$ 4 A), both the low-side and high-side switches can achieve ZVS turn on. At heavy load, the deadtime is insufficient for I_{neg} to go sufficiently negative so that the high-side switches will have C_{oss} loss. However, the converter is conduction loss dominated at heavy load. Therefore, it is unnecessary to pursue full range ZVS operation with dynamic deadtime, as the increase of conduction loss due to the increased RMS current resulting from the negative current requirement for ZVS, will be larger than the reduction of switching loss, and hurt the overall efficiency.

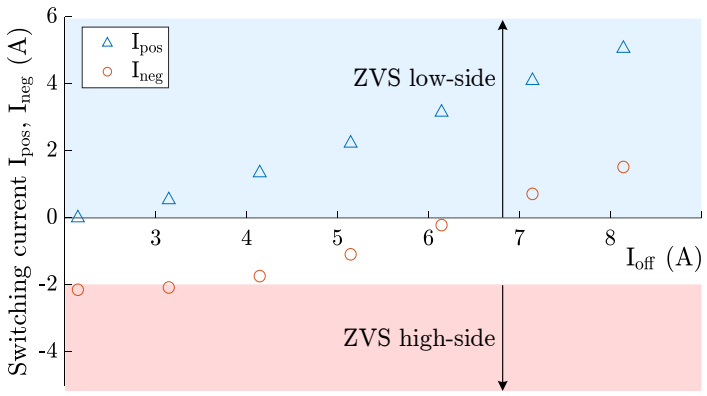


Figure 6.22: Achieving complete ZVS at light load with the optimum deadtime.

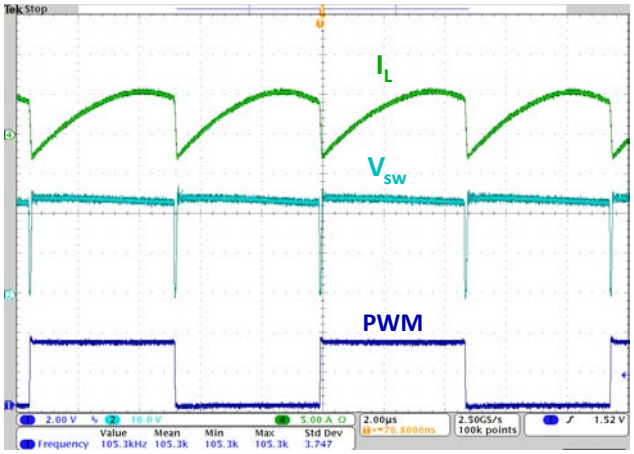


Figure 6.23: I_{L} and V_{sw} under ZVS.

ZVS Experimental Results

The prototype is tested with the proposed ZVS technique, and the captured waveform of the inductor current and the switching node voltage is shown in Fig. 6.23, which closely matches the analytic plot in Fig. 6.19. As can be seen in Fig. 6.24, switch S_{1A} achieves ZVS turn-on when the inductor current is positive, followed by S_{2B} (shown in Fig. 6.25), when the inductor current reverses direction and completely discharges its output capacitance. By observing the switching operation of each switch ($S_{1A,B}$ to $S_{4A,B}$), it is possible to fine-tune the deadtimes of the two stages separately to optimize the overall efficiency.

The comparison of efficiency performance under different operation modes are plotted in Fig 6.26. It can be seen that the power stage efficiency under ZVS operation (3% load: 98.0%, peak: 99.2%, full load: 97.25%) is higher than that of the ZCS operation (3% load: 95.6%, peak: 99.0%, full load: 97.35%) at light to medium load, thanks to the elimination/reduction of the transistor output capacitance loss. At heavy load, when the conduction loss begins to

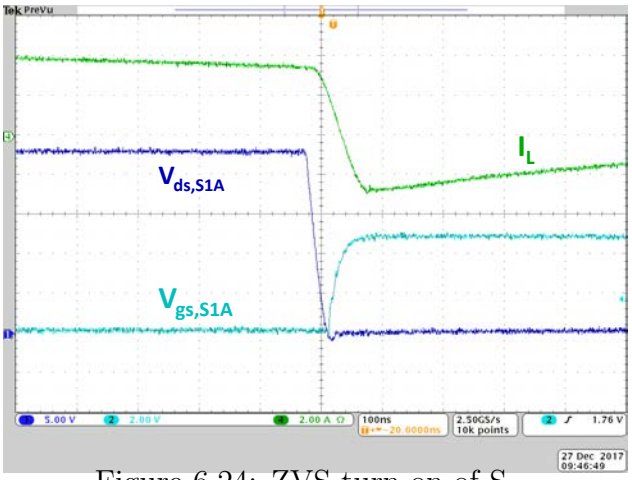


Figure 6.24: ZVS turn-on of S_{1A}.

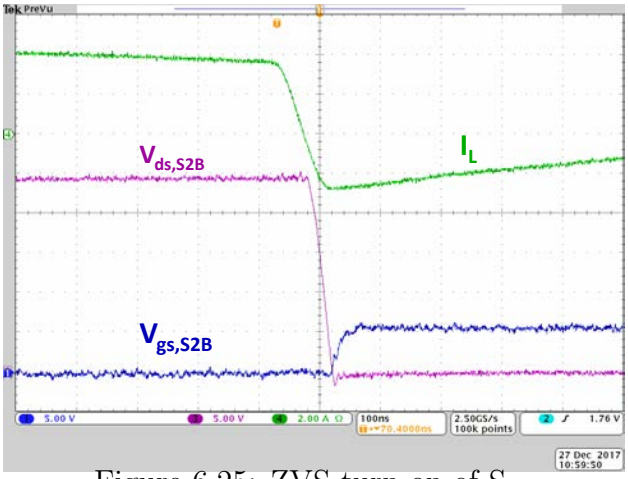


Figure 6.25: ZVS turn-on of S_{2B}.

dominate, the efficiency of the ZVS operation falls behind slightly, due to a higher total RMS current. The overall ZVS efficiency (including gate drive loss) at various input voltages is shown in Fig. 6.27. For the 48-to-12 V conversion, the overall efficiency has a peak of 99.0%, and maintains 97.2% at full power. It should be pointed out that the selected low-voltage Infineon OptiMOS switches have ultra low input and output capacitances that are comparable to the eGaN FETs in the same class. A more obvious efficiency improvement through the adoption of the ZVS technique can be expected when higher voltage MOSFETs (with higher parasitic capacitances) are used for other applications.

To better understand the operation and the potential improvements of the cascaded resonant converter, a loss analysis is performed and shown in Fig. 6.28. Not surprisingly, the conduction loss due to switch on-resistance, flying capacitor ESR and inductor resistance represents a large portion of the overall loss. In addition, the PCB copper loss (2 oz copper used in this design) is also significant, reflecting the importance of proper layout design,

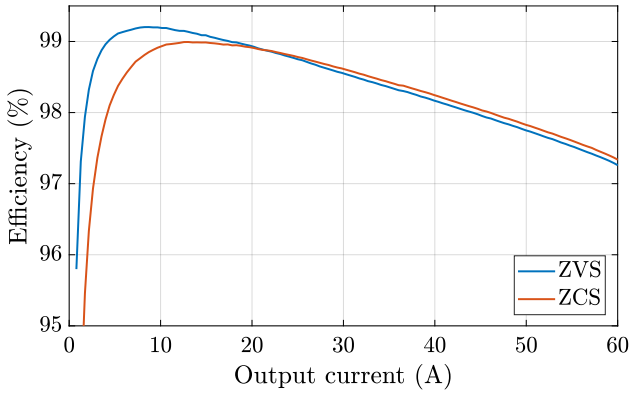


Figure 6.26: Comparison of measured 48-to-12 V power stage efficiency.

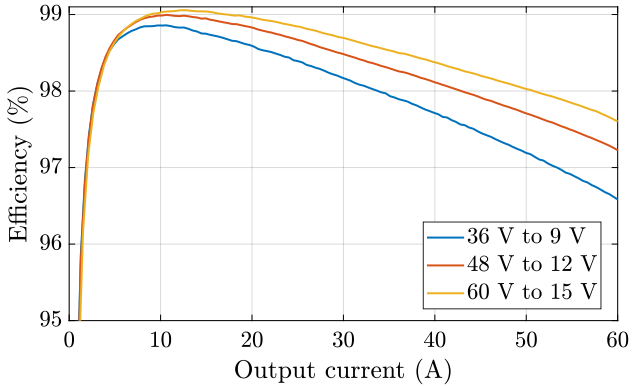


Figure 6.27: ZVS efficiency including gate drive loss.

especially when the current is high and the components are densely populated for high power density design. If cost permits, thicker copper (e.g. 5 oz) and more inner layers with better current carrying capability can be used to further improve the efficiency. At the peak efficiency point where conduction losses do not yet dominate, implementing ZVS to eliminate switch C_{oss} loss can help improve the overall efficiency. The remaining switching loss at this point is the V-I overlap loss of the high-side switches (S_{1B} to S_{4B}) at turn-off time. When the load current increases, the inductor current will not go negative (unless the deadtime is increased), resulting in additional C_{oss} loss for the high-side switches. However, as can be seen from the pie chart at the full power point, even with the slight increase, the switching loss has minimal effect on the overall performance. Another noticeable source of loss at light load range is the gate drive loss, even though the applied cascaded bootstrap method has been shown to be one of the most efficient and compact ways to supply floating gate drive power [98]. Since this high gating loss is mainly due to the large number of switches associated with the converter, reducing the operation of the switches at light load with phase-shedding or burst mode control can help improve the efficiency. Manufacturer loss models were used to calculate inductor core loss and ac winding loss. Owing to the

Gate drive	245	250				
Total	1279	19683				

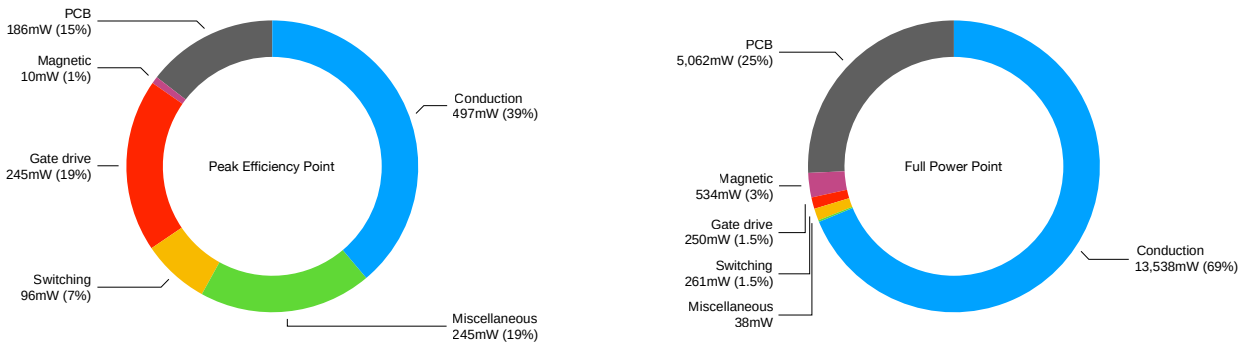


Figure 6.28: Loss breakdown of the prototype in ZVS mode.

relatively low switching frequency, the magnetic loss in the cascaded resonant converter is not a significant source of loss. The remainder of the losses, which are not accounted for in other loss models, are categorized as miscellaneous loss. More detailed magnetics loss models may increase the estimated magnetics losses. Additionally, recent work [3] has highlighted the increased capacitor losses when used in large dc bias and ac current amplitude as done here.

Finally, we perform a detailed survey and comparison to the-state-of-the-art converters in this space, including both industry and academic work [1], [23], [122]–[125]. Fig. 6.29 highlights both the isolation and regulation capabilities of the-state-of-the-art solutions, showcasing their effects on achievable performance and allowing designers to make trade-offs regarding the suitability of each design for various applications. Under the space of non-isolated and unregulated converters, this work is compared with other representative solutions that have similar voltage and power ratings. The results are tabulated in Table 6.2. Thanks to the high energy density of capacitors and the efficient utilization of the switches and passive components, the cascaded resonant converter can have performance superior to that of conventional SC and magnetic-based converters. Compared with the Google switched tank converter, this work uses a different ReSC topology with Class-II ceramic capacitors and inductor-at-output configuration. Despite the lack of auxiliary circuits (e.g., start-up, protection) and rigorous reliability tests that commercial products require, we demonstrate that the cascaded resonant converter is a promising ReSC topology with the potential to achieve high efficiency and high power density simultaneously.

1

6.6 Cascading and Interleaving Strategies

An alternative 12-switch design of the cascaded resonant converter is shown in Fig. 6.30. Since the output current of a 2-to-1 ReSC converter is a continuous rectified sine wave, two-phase interleaving is not required for the first stage. If the high-voltage switches in the first stage ($S_{1A,1B}$, $S_{2A,2B}$) have sufficiently low on-resistance to process the full rated power

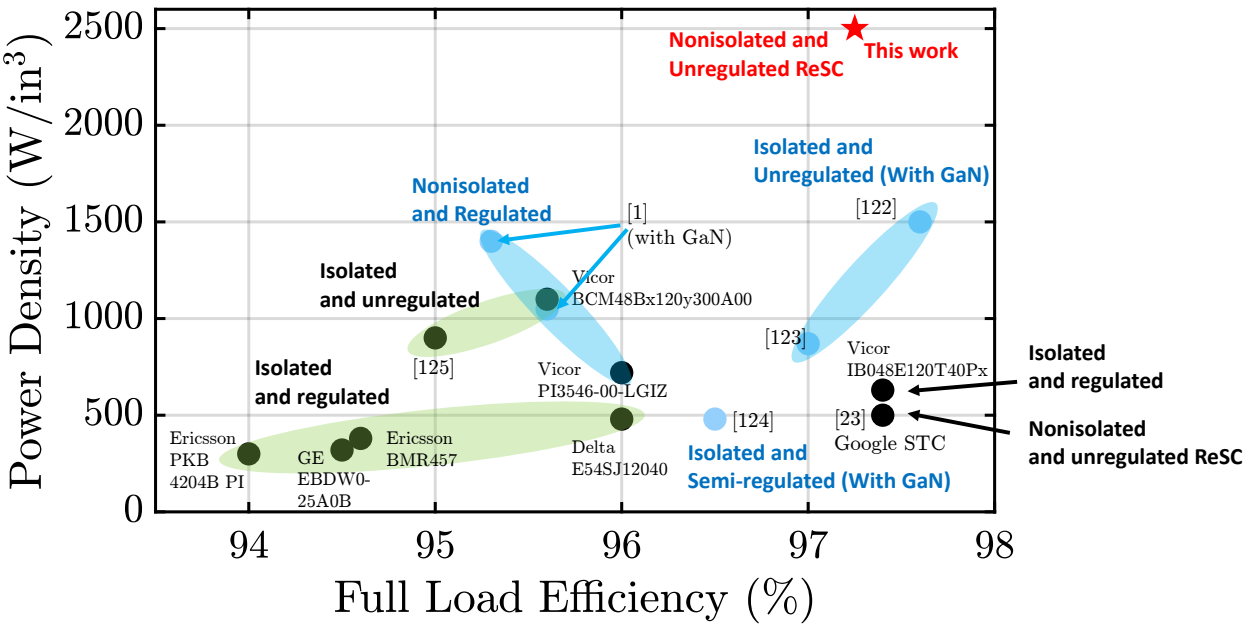


Figure 6.29: Comparison of full-load efficiency and power density of state-of-the-art commercial products and previously published research.

Table 6.2: Comparison of this work and existing non-isolated intermediate bus converters

Reference	Topology	Output current (A)	Power Density (W/inch^3)	Efficiency	Notes
This work	cascaded resonant	60	2500	full load: 97.23% peak: 99.0%	based on 48:12V conversion, gating loss included
LTC7820 [8]	cascaded pure 2-to-1 SC	40	up to 1500	full load: ≤97.0% peak: ≤98.6%	highly integrated 48:12 V design, detailed data unavailable (use conservative estimate)
EPC9130 [1]	5-phase interleaved buck	60	> 1000	full load: 95.8% peak: 96.2%	48:12V, GaN switches, **regulated**
Google switched tank converter [23]	modified Dickson	50	500 (power stage only: switches and passives)	full load: 97.41% peak: 98.61%	54 V input, 4:1 fixed ratio, components are not densely populated

with good efficiency performance, a cascaded design with non-interleaving first-stage can be considered to save component count and board area. A second revision of the cascaded resonant converter using this 12-switch design and the latest OptiMOS transistors is reported in [126]. With the same specifications (36–60 V input, 4-to-1 fixed-ratio, 60 A output current), the improved design achieves over 4000 W/in^3 power density and 98.0% full-load efficiency, while maintaining the same 99.0% peak efficiency. These results set a new record for the 48-to-12 V data center application, showcasing the superior performance of the cascaded resonant topology.

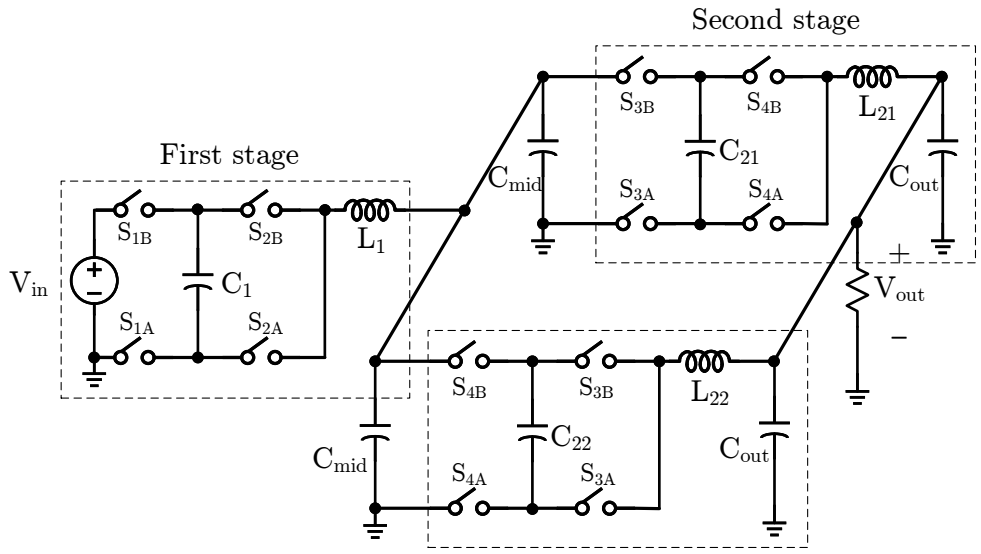


Figure 6.30: An alternative 12-switch design of the cascaded resonant converter with single first-stage.

Besides the basic 2-to-1 ReSC converters, the cascaded resonant concept can be extended to other more complex ReSC topologies for higher conversion ratios. Compared to building a high-ratio single-stage ReSC converter, cascading converters with simpler structures may greatly reduce the component count, control complexity, and system failure rate owing to less series-connected switches in the system. This is because the voltage conversion of SC converters is based on capacitor voltage "addition" or "subtraction". In contrast, through cascading operation, capacitor voltage "multiplication" or "division" can be achieved.

Another challenge associated with the high conversion ratio is the simultaneous existence of high input voltage and high output current. For a single-stage ReSC converter, the achievable output power is usually limited by the output current, whereas the high-voltage devices at the input side are often times underutilized. By dividing the system into multiple cascaded stages, the high-voltage input stage and the high-current output stage can be designed and optimized separately. Specifically, by first stepping down the high input voltage with a simple but efficient 2-to-1 ReSC converter, the voltage stress of the rest of the system is greatly reduced. Then, multiple downstream ReSC converters can be paralleled to provide the requisite high output current. Since these converters see low input voltage, the topologies which favor low-voltage-rating devices can be used for optimal performance.

For instance, as shown in Fig. 6.31, two-phase interleaved switched-tank converters (STC) can be cascaded with a front-end 2-to-1 ReSC converter. The STC (or the Dickson converter) is known for its low switch voltage rating and good switch utilization (i.e., low VA rating). However, it requires high voltage capacitors and therefore suffers from relatively low achievable power density compared to other ReSC topologies. With halved input voltage, the

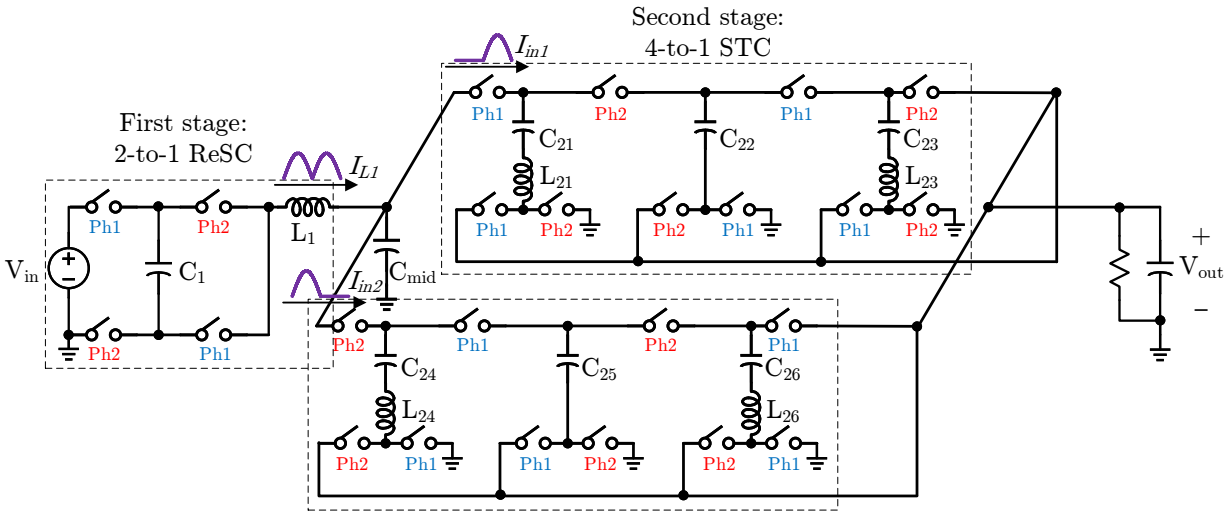


Figure 6.31: Cascading 2-to-1 ReSC with two-phase interleaved switched-tank converters (STC).

high-efficiency advantage of the STC topology can be fully utilized, and the disadvantage in passive component utilization is mediated. Moreover, as in the original cascaded resonant converter, the combined input current of the two-phase interleaved STC converter becomes a continuous rectified sine wave, which matches the output current of the 2-to-1 ReSC converter. As a result, the interstage decoupling requirement of C_{mid} can be greatly reduced.

The interleaving strategy can also be applied to other ReSC topologies with duty ratios other than 50%. Owing to the augmenting inductor at the output, the duty ratio of the series-phase and the parallel-phase of the 4-to-1 series-parallel converters become $\frac{1}{4}$ and $\frac{3}{4}$, respectively. As shown in Fig. 6.32, four series-parallel converters can be paralleled and interleaved with 90° phase shift to make their combined input current a continuous rectified sine wave. By operating the 2-to-1 ReSC stage at twice the frequency of the series-parallel stage, the currents of the two stages are matched and C_{mid} can be reduced.

In addition to cascaded operation, a multi-operating-phase concept can be used to achieve high conversion ratio with ReSC converters, while maintaining a relatively low component count. In the next chapter, we present a family of multi-resonant SC converters with conversion ratios greater than 4-to-1.

6.7 Chapter Summary

This chapter presents a new ReSC converter topology and its control method. By cascading 2-to-1 ReSC converters and implementing an interleaved control method, high-performance

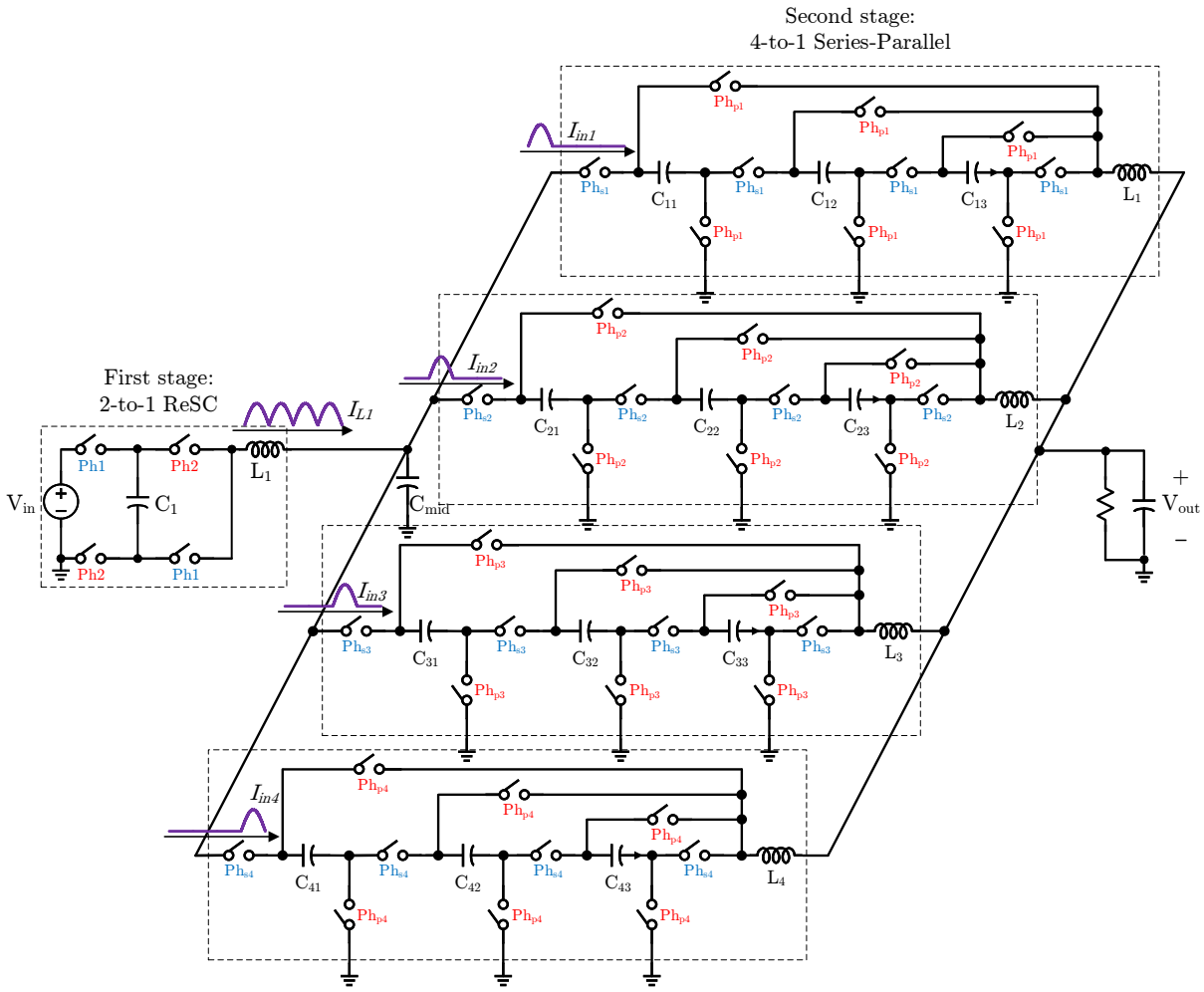


Figure 6.32: Cascading 2-to-1 ReSC with four-phase interleaved series-parallel converters.

high-conversion-ratio power conversion can be achieved with the original simple structure and operating principle. We demonstrate in theory and with a hardware prototype that, the proposed cascaded resonant converter has high utilization of both active and passive components, and is an excellent candidate for 48-to-12 V data center application. It is shown that the large interstage decoupling requirement in practical implementations can be alleviated with a two-phase interleaving method, and the effects of component variations can be mitigated by operating at a frequency slightly higher than the resonance. A ZVS control method is also developed to improve light-load efficiency, and the method can also be applied to other ReSC topologies. The prototype achieves 99.0% peak efficiency and up to 3100 W/in^3 power density. Finally, the concept of cascading and interleaving converters is extended to other more complex ReSC topologies for higher conversion ratios.

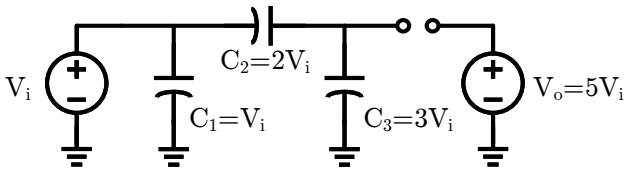
Chapter 7

Multi-Resonant Switched-Capacitor Converter

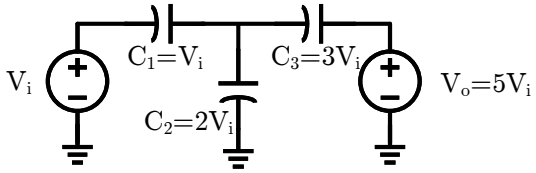
Compared with conventional SC converters with two operating phases, SC converters with multiple operating phases can achieve the same conversion ratio with fewer capacitors and switches. This feature makes multi-phase SC converters an attractive candidate for applications with high conversion ratios. This chapter presents a family of multi-phase ReSC converters with high conversion ratios. They are called multi-resonant SC converters, which can be synthesized from the basic doubler and the series-parallel topologies. Both theoretical analysis and experimental results from a practical implementation are provided to demonstrate the benefits of the multi-resonant approach. The hardware prototype can operate in both 6-to-1 mode and 8-to-1 mode, with one of the best in-class performances.

7.1 Background and Motivation

This chapter is a continuation of Chapter 6. We strive to build high-performance ReSC converters with high conversion ratios. One potential application is the two-stage power delivery architecture from 48 V to the point-of-load voltages for data centers. In contrast to 48-to-12 V bus converters for the legacy 12 V bus, recent research [104] suggests that a lower intermediate bus voltage (e.g., 4–6 V) may provide higher overall efficiency, once both the intermediate bus converter and the second-stage buck converters are considered. Therefore, there is increased interest in highly efficient fixed-ratio conversion with an 8-to-1 to 12-to-1 ratio. For such a high conversion ratio, a transformer is usually needed. Reference [127] demonstrates a GaN-based 48-to-6 V fixed-ratio LLC converter with 98% peak efficiency and 1100 W/in^3 power density, which uses a highly optimized 8-to-1 matrix transformer. In contrast, the majority of existing ReSC works focus on 4-to-1 or 6-to-1 ratios, and high performance ReSC works with higher conversion ratios have not been widely demonstrated. This is because the number of components (switches and capacitors) increases proportionally with respect to the conversion ratio, and the increased circuit implementation complexity



Phase 1

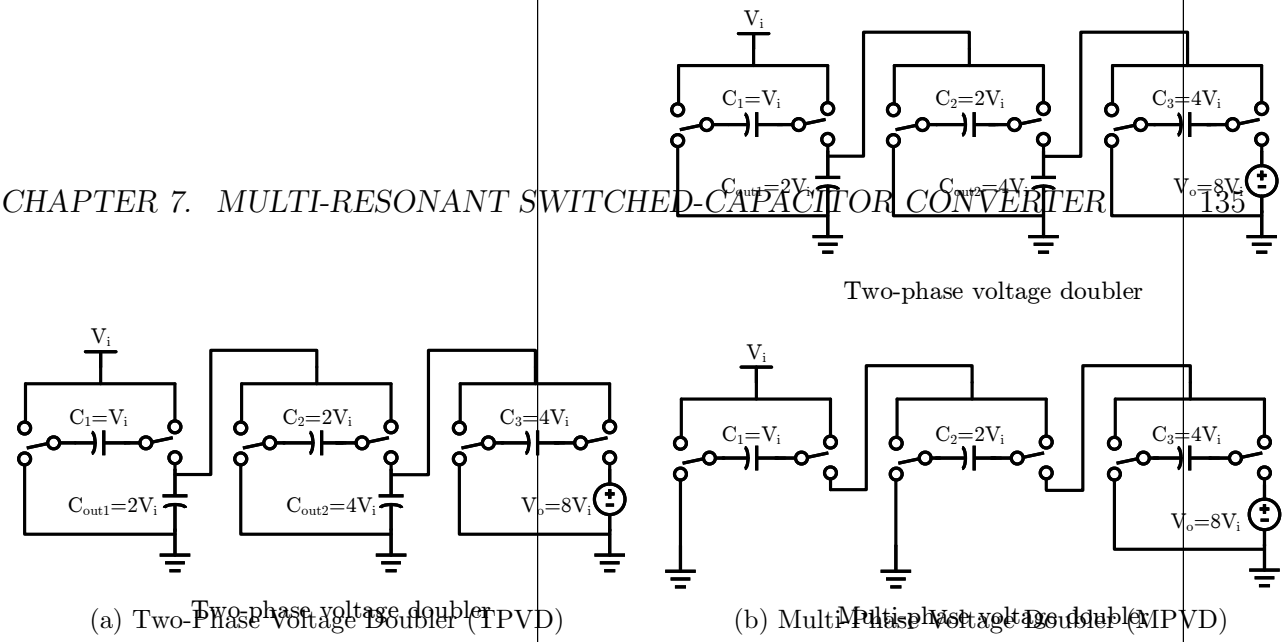


Phase 2

Figure 7.1: The maximum voltage gain in two-phase SC converters follows the Fibonacci sequence.

can potentially reduce the theoretical performance benefits. To address this challenge, the multi-operating-phase concept is proposed and explored in this chapter.

In Section 7.2, the theoretical performance limit of SC converters is briefly reviewed. Compared with typical SC converters which have two operating phases, multi-phase SC converters can achieve the same conversion ratio with significantly fewer switches and flying capacitors [128]. This is extremely beneficial in practical implementations when high conversion ratios are needed. In Section 7.3, we demonstrate how to generate and synthesize multi-phase SC topologies from conventional two-phase SC topologies, and compare their similarities and differences. In Section 7.4, an 8-to-1 multi-resonant-doubler converter is presented, with detailed theoretical analysis, experimental results, and performance comparison. This converter features the least-possible number of switches and capacitors among all SC converters at this conversion ratio. Even though the multi-resonant-doubler does not have a significant advantage in switch utilization compared to other two-phase SC converters, it has superior passive component utilization, as well as additional benefits in practical circuit design. A 48-to-6 V, 40 A, fixed-ratio converter prototype is designed and implemented. The prototype achieves 98.6% peak efficiency (98.0% including gate drive loss) and 1675 W/in^3 power density. In Section 7.5, the multi-resonant-doubler is modified to a 6-to-1 cascaded series-parallel converter, which also achieves the best overall performance in its class. Finally, in Section 7.7, the multi-operating-phase concept is generalized to a family of multi-resonant SC converters, with conversion ratios spanning from 8-to-1 to 12-to-1.



(a) Two-Phase Voltage Doubler (TPVD) (b) Multi-Phase Voltage Doubler (MPVD)

Figure 7.2: Exponential growth of voltage gain with voltage doublers.

7.2 Theoretical Performance Limit of SC converters

Two-Phase SC Converters

According to [128], [129], for two-phase SC converters, the realizable conversion ratio with k capacitors ($k-1$ flying capacitors and one output capacitor) is bounded by the kth Fibonacci number F_k:

$$M[k] = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1 \le P[k] \le F_k}{1 \le Q[k] \le F_k} \tag{7.1}$$

where $F_1 = 1, F_2 = 2, F_3 = 3, ..., F_n = F_{n-1} + F_{n-2}$. Similarly, the bound on the number of switches required in any SC circuit is found to be $3k - 2$. Intuitively, the voltage gain is achieved by capacitor voltage addition (or subtraction) in two-phase SC converters. By adding (or subtracting) the voltage of every two neighboring flying capacitors by turns, the capacitor voltages and the output voltage increases (or decreases) in a Fibonacci fashion, achieving the maximum achievable voltage gain. The two operating phases of a Fibonacci step-up converter with three flying capacitors C_1, C_2, and C_3 are shown in Fig. 7.1. In Phase 1, C_1 is charged to the input voltage V_{i} and C_3 is charged by the series combination of C_1 and C_2 to $3V_{\text{i}}$. In Phase 2, C_2 is charged by the series combination of C_1 and input voltage to $2V_{\text{i}}$, whereas the output voltage is charged by C_2 and C_3 to $5V_{\text{i}}$. A property of the Fibonacci sequence is that the ratio of every two successive Fibonacci numbers approaches the golden ratio (1.618). It indicates that the fastest possible voltage growth rate (with respect to the number of flying capacitors) of a two-phase SC converter is 1.618.

Multi-Phase SC Converters

As discussed in [130], given the same number of capacitors and switches, if multiple operating phases can be introduced, the maximum realizable gain with k capacitors ($k - 1$ flying capacitors and one output capacitor) becomes

$$M[k]_{max} = 2^{k-1} \tag{7.2}$$

p phases	Number of capacitors k				
	1	2	3	4	5
2 (Fibonacci)	1	2	3	5	8
3 (Tribonacci)	1	2	4	7	13
4 (Tetranacci)	1	2	4	8	15
5 (Pentanacci)	1	2	4	8	16

which is greater than the Fibonacci bound. From a circuit perspective, this can be implemented by a chain of 2-to-1 voltage doublers, which effectively achieves capacitor voltage multiplication (or division).

As shown in Fig. 7.2a, a voltage doubler with three flying capacitors C_1, C_2, and C_3 can achieve a gain of 8. However, with two-phase operation, the voltage doubler requires two intermediate decoupling capacitors C_{out1} and C_{out2}, resulting in a total required capacitor number that is higher than that predicted in (7.2). One method to eliminate the intermediate decoupling capacitors is to operate two two-phase doublers in parallel with interleaving control, which is discussed in Chapter 6. Alternatively, more operating phases can be added such that some flying capacitors are disconnected from the circuit for some phases, thereby relaxing the intermediate decoupling requirement. The multi-phase voltage doubler (MPVD) in Fig. 7.2b can achieve the theoretical maximum gain of (7.2) with 4 capacitors (3 flying capacitors and one output capacitor). Note that even though the gain becomes 2^{k-1} for multi-phase operation, the minimum number of switches required remains $3k-2$. It indicates that it is possible to further reduce the switch number of the MPVD in Fig. 7.2, from 12 switches to the theoretical minimum of 10 switches while keeping the voltage gain at 8. The formal expression and proof of the gain of multi-phase SC converters is provided in [131], [132]. With p operating phases, the maximum realizable gain is

$$M_{max}^{(p)}[k] = F_k^p \tag{7.3}$$

where F_k^p is the p-th order generalized Fibonacci number. The p-th hyper-Fibonacci numbers are defined by the recursion:

$$F_k^p = \begin{cases} 2^{k-1} & k = 1, ..., p \\ F_{k-1} + ... + F_{k-p} & k > p \end{cases} \tag{7.4}$$

It means that when the number of phases p is greater than or equal to the number of capacitors k, the highest possible conversion ratio 2^{k-1} can be achieved. When $p < k$, the attainable gain is the p-th order Fibonacci summation. If $p = 2$, the equation degenerates

to the regular Fibonacci sequence. An example is provided in Table 7.1. With 4 capacitors (3 flying capacitors and one output capacitor), two-phase operation can provide a maximum gain of 5. If 3 phases are used, the gain equals the sum of the previous three Fibonacci numbers (Gain $= 1 + 2 + 4 = 7$). With 4 or more phases, the gain saturates at 8 ($= 2^{(4-1)}$).

7.3 Generation and Synthesis of Multi-Phase Topologies

In this section, we present an example of how to derive multi-phase SC converters from their two-phase counterparts while maintaining the same fundamental structure, through gating signal modification and/or minor circuit changes. The first circuit schematic shown in Fig. 7.3 is a classic 4-to-1 series-parallel topology, featuring 10 switches and 3 flying capacitors. Because an inductor is augmented at the output node for soft-charging operation, the duty ratios of the series-phase and the parallel-phase need to be adjusted accordingly, and they are $\frac{T}{4}$ and $\frac{3T}{4}$, respectively.

Next, as shown in the second part of Fig. 7.3, by moving the source terminal of the top-most horizontal switch to the positive side of the second flying capacitor, a 6-to-1 cascaded series-parallel converter is derived. Note that this is a completely new topology that has not been explored in existing works, and its detailed operating principle is presented in Section 7.5. Compared to the 4-to-1 series-parallel converter, it has the same number of components, and only the rating of one switch and one flying capacitor are increased from V_o to $3V_o$. In order to achieve a higher conversion ratio, an extra operating phase is introduced, such that the converter can merge the operation of two cascaded converters together: the first four switches and the first flying capacitor forms a 2-to-1 SC stage, followed by a 3-to-1 series-parallel stage formed by the rest of the components. Note that the 2-to-1 step-down operation only takes place at the first $\frac{1}{3}$ of the switching period.

Similarly, if the source terminal of the second top-most horizontal switch is relocated to that shown in the third part of Fig. 7.3, another classic topology, the Fibonacci converter, is derived. Given fixed capacitor and switch number, the conversion ratio of the Fibonacci topology is at the theoretical limit of two-phase SC converters.

Moreover, by introducing two extra operating phases, an 8-to-1 conversion ratio can be achieved with exactly the same structure. It can be viewed as another type of multi-phase voltage doubler, which features the minimum number of switches for this conversion ratio (less than the MPVD shown in Fig. 7.2b). The multi-phase operation of this structure was first proposed in [133]. Since the flying capacitors carry binary voltages (($\frac{1}{8}$, $\frac{2}{8}$, $\frac{4}{8}V_{in}$), it is known as a binary converter. Furthermore, [134], [135] have demonstrated that all fractions of the input voltage ($\frac{1}{8}$, $\frac{2}{8}$, $\frac{3}{8}$,..., $\frac{7}{8}V_{in}$) can be derived by adjusting the gating signals, and thus named it the extended binary converter (EXB). In Section 7.4, we expend upon this by exploring the performance of a new implementation of this structure, with an augmenting inductor for ultra-efficient 8-to-1 fixed-ratio conversion. This converter is called the

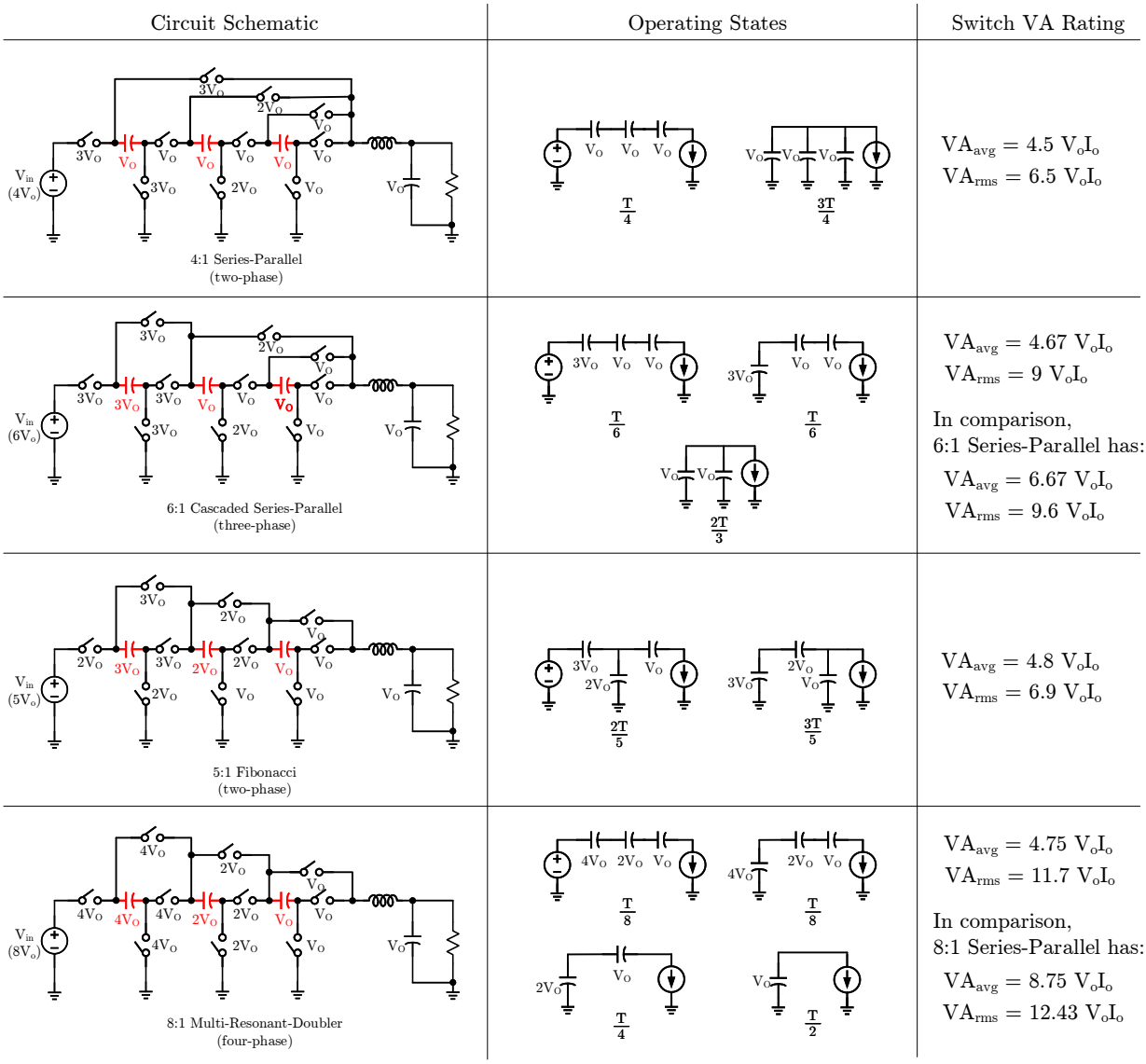
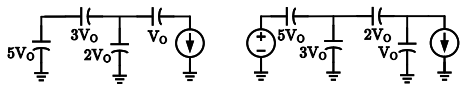


Figure 7.3: Achieving different conversion ratios with the same fundamental structure.

multi-resonant-doubler (MRD), as the augmenting inductor resonates with different flying capacitor combinations in different phases and therefore forms multiple resonances within a switching period.



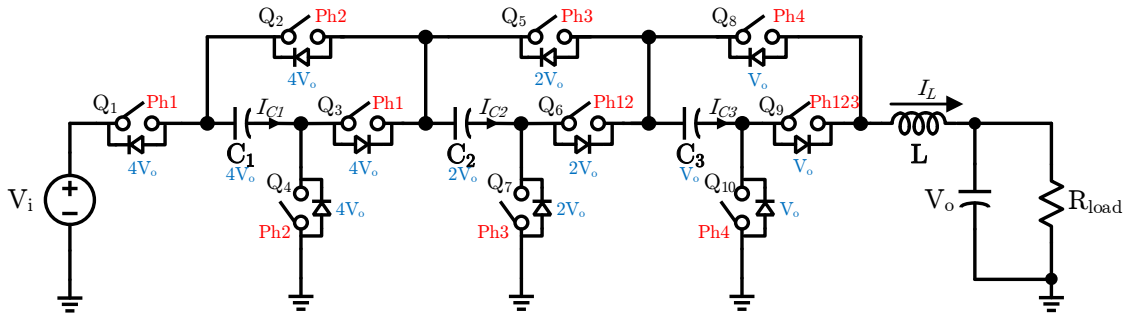


Figure 7.4: Schematic drawing of the 8-to-1 multi-resonant-doubler converter with device ratings and control signals labeled.

7.4 8-to-1 Multi-Resonant-Doubler Converter

Operating Principle

The schematic drawing of the 8-to-1 multi-resonant-doubler (MRD) converter with four operating phases is shown in Fig. 7.4. Its basic SC structure can be viewed as one practical implementation of a multi-phase voltage doubler that achieves the theoretical maximum gain with the least number of components (3 flying capacitors and 10 switches for a gain of 8). Because of the voltage doubler structure, the flying capacitors carry binary voltages ($C_1 = 4V_o$, $C_2 = 2V_o$, $C_3 = V_o$) and the switches see the same voltage as that of the corresponding capacitors ($Q_{1-4} = 4V_o$, $Q_{5-7} = 2V_o$, $Q_{8-10} = V_o$). The key control signals, inductor and capacitor current waveforms, and the equivalent circuit of the four operating phases are shown in Fig. 7.5. It can be seen that all flying capacitors are charged and discharged in a resonant fashion, resulting in soft-charging and ZCS. The detailed operation of the four phases are as follows:

- Phase 1: The "Ph1", "Ph12" and "Ph123" switches in Fig. 7.4 are ON. C_1, C_2, C_3 and L are connected in series. All flying capacitors are resonantly charged by the input. The duration of phase 1 is $\frac{1}{8}$ of the switching cycle. The equivalent resonant frequency of this phase is $f_{r,\text{ph1}} = \frac{1}{2\pi\sqrt{LC_{eq1}}}$, where $\frac{1}{C_{eq1}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$.

- Phase 2: The "Ph2", "Ph12" and "Ph123" switches are ON. In this phase, all flying capacitors are still connected in series, but C_1 is being discharged. The length of the phase and the equivalent resonant frequency remain the same as those of Phase 1.

- Phase 3: The "Ph3" and "Ph123" switches are ON. In this phase, C_1 is disconnected and C_3 is only charged by C_2. In order to maintain capacitor charge balance, the duration of this phase is doubled to $\frac{1}{4}$ of the switching cycle. The equivalent resonant frequency of this phase is now $f_{r,\text{ph3}} = \frac{1}{2\pi\sqrt{LC_{eq3}}}$, where $\frac{1}{C_{eq3}} = \frac{1}{C_2} + \frac{1}{C_3}$.

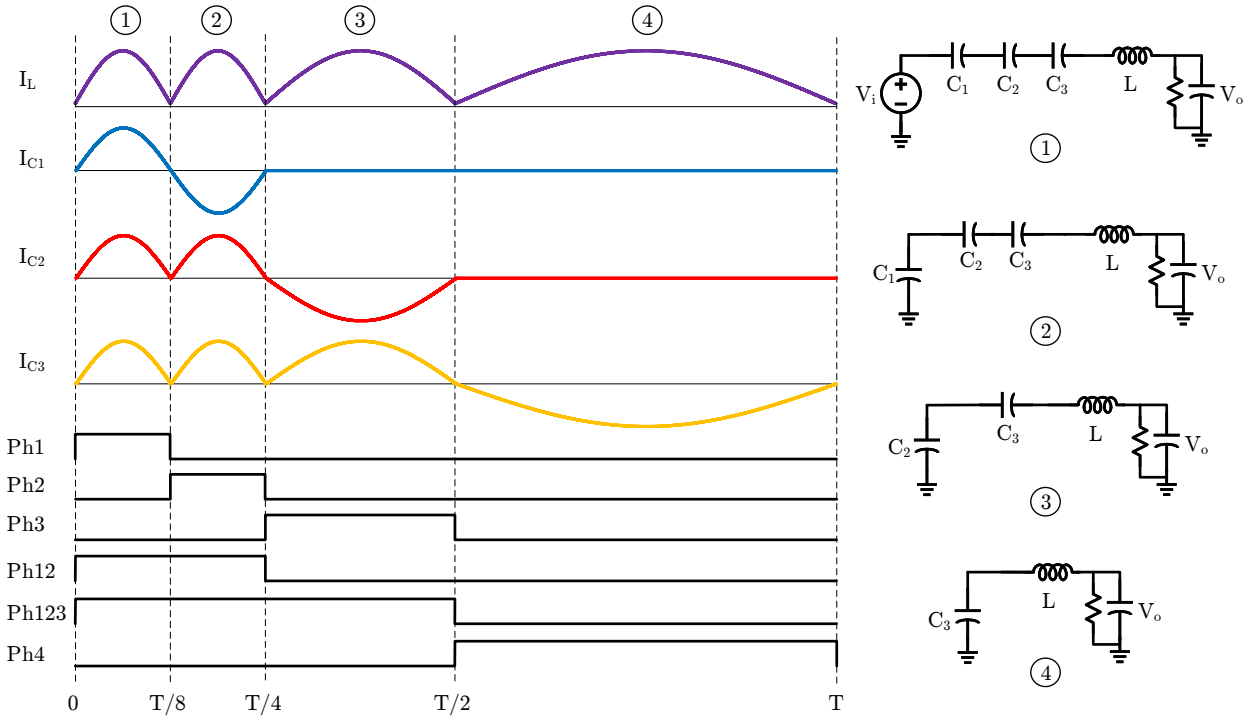


Figure 7.5: Inductor and capacitor current waveforms, control signals, and equivalent circuits of the 8-to-1 multi-resonant-doubler converter.

- Phase 4: Only the "Ph4" switches are ON. In this phase, both C_1 and C_2 are disconnected and C_3 is resonantly discharged to the load. The equivalent resonant frequency of this phase is $f_{r,\text{ph4}} = \frac{1}{2\pi\sqrt{LC_3}}$. Since the duration of this phase is $\frac{1}{2}$ of the switching cycle, the overall switching frequency with four phases combined would be the same as $f_{r,\text{ph4}}$ ($f_{\text{sw}} = f_{r,\text{ph4}} = \frac{1}{2\pi\sqrt{LC_3}}$), which is only determined by L and C_3.

By equating the relative length of different phases and the corresponding resonant frequency, the required ratio of the flying capacitors can be found to be $C_1 = \frac{1}{12}C_3$ and $C_2 = \frac{1}{3}C_3$. These reduced capacitance requirements are due to the fact that the resonant charging currents of C_1 and C_2 are at higher frequencies than C_3. It indicates that even though C_1 and C_2 must be rated for higher voltages than C_3, their physical volume could still be very similar due to their reduced capacitance. Moreover, these capacitor ratios relate to two operation constraints. First, these exact ratios are needed to achieve ZCS for all switches. Second, these ratios determine the minimal capacitor values that are needed to achieve soft-charging operation. In practical implementations, it is very challenging to maintain an exact capacitor ratio. Nevertheless, the soft-charging operation is guaranteed as long as the actual capacitors exceed their minimum required values. In practice, the imperfect ZCS operation

Table 7.2: Comparison of component number of 8-to-1 SC converters

Topology	Switch Number	Capacitor Number	Notes
Multi-Resonant-Doubler	10 ($4V_o$×4, $2V_o$×3, V_o×3)	3 ($4V_o$, $2V_o$, V_o)	one inductor, four-phase operation
Cascaded Resonant	12 ($4V_o$×4, $2V_o$×4, V_o×4)	3 ($4V_o$, $2V_o$, V_o)	three inductors, two C_{mid}
Fibonacci	13 ($5V_o$×2, $3V_o$×4, $2V_o$×3, $2V_o$×4)	4 ($5V_o$, $3V_o$, $2V_o$, V_o)	at the limit of two-phase SC
Series-Parallel	22 ($7V_o$×3, 6-$2V_o$×2, V_o×9)	7 (V_o×7)	one inductor at output is possible
Dickson (Switched-Tank)	22 ($2V_o$×6, V_o×16)	7 ($7V_o$, $6V_o$, ... , V_o)	four inductors for STC [23]

Table 7.3: Comparison of passive and active component utilization of 8-to-1 SC converters

Topology	Passive Volume	VA_{rms} Rating	R_{out} (assuming same R for all switches)
Multi-Resonant-Doubler	1.7	11.7	2.75 (10 switches), 2 (13 switches), 1.25 (22 switches)
Cascaded Resonant	1.7	8.5	2.625 (12 switches), 1.625 (16 switches), 1.125 (24 switches)
Fibonacci	2.2	8.9	2.165 (13 switches), 1.4775 (16 switches)
Series-Parallel	1	12.4	1.25 (22 switches)
Dickson (Switched-Tank)	4.4	5	0.8 (22 switches)

due to capacitor ratio mismatch is found to have a relatively minor effect on the performance of the converter.

Performance Comparison

Next, we use the MRD as an example to compare the performance of multi-phase SC converters with typical two-phase SC converters. For discrete implementations (especially for low-voltage applications), both the switch number (and the associated gate drive circuitry) and the passive component number can greatly affect the solution size. Table 7.2 compares the required number of components of the MRD and other 8-to-1 SC converters. It can be seen that the MRD uses fewer components than all other topologies, including the cascaded resonant converter (a type of two-phase voltage doubler) and the Fibonacci converter, which is at the theoretical lower limit of two-phase SC converters. Moreover, as shown in Table 7.3, when considering the total passive component volume from the fundamental energy transfer perspective as discussed in Chapter 3, the doubler-based topologies are found to have excellent passive component utilization among all topologies. Because of these reasons, the MRD has the potential to achieve higher power density than its two-phase counterparts.

Nevertheless, the switch number reduction is not free and can result in higher switch VA rating and output impedance (which negatively impacts efficiency). Assuming all switches have the same on-resistance R, which is often the case for applications lower than 25 V due to limited discrete power MOSFET selection [24], the output impedance of the MRD is $2.75R$ with the minimum number of switches (10 switches), which is higher than the other topologies. If conduction loss is a major concern, more switches can be paralleled in the key current path. The output impedance can be reduced to $2R$ for 13 switches, or $1.25R$ for 22 switches, resulting in comparable output impedance to other topologies with a similar

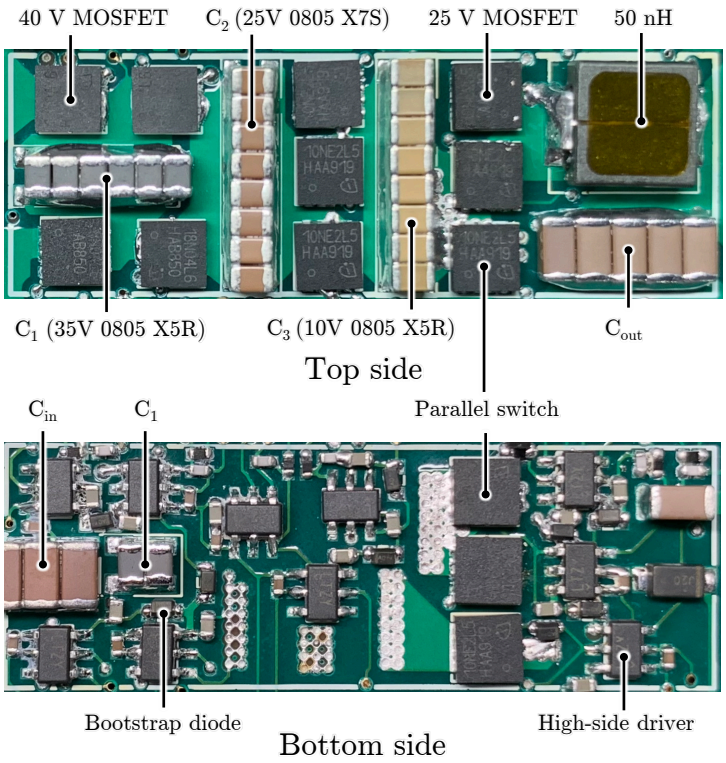


Figure 7.6: Photograph of the converter prototype. Dimensions: 1.38 × 0.46 × 0.22 inch (3.5 × 1.17 × 0.55 cm).

number of total switches. Fundamentally, there is no win-win situation that can achieve low component count and low output impedance simultaneously. The Dickson and series-parallel converters can have low output impedance because they use a large number of switches to split the current into multiple parallel paths. In comparison, the MRD uses less switches but has only one current path and thereby higher output impedance.

However, in practical implementations, MRD's low required switch count can make it more adaptable to different applications compared to two-phase topologies with an inherently large number of switches and gate drivers. Depending on the design specifications, more switches can be paralleled to reduce the output impedance, without requiring additional gate drive circuits. In addition, the low component count can greatly simplify the PCB layout and increase power density. Since PCB loss contributes a large portion to the overall loss for low-voltage high-current applications, a clean and simple PCB layout is important for a high-performance design.

Hardware Implementation and Experimental Results

An annotated photograph of the hardware prototype is shown in Fig. 7.6, with key components highlighted. Table 7.4 provides the main operating parameters of the converter and

Table 7.4: Key prototype parameters of the MRD converter

	Nominal	Range
Input voltage	48 V	40 – 60 V
Output voltage	6 V	5 – 7.5 V
Output current	40 A	40 A
Power rating	240 W	200 – 300 W
Switching frequency	70 kHz	70 – 78 kHz

Table 7.5: Main component listing of the MRD converter

Component	Part number	Parameters
Switch Q_1-Q_4	Infineon BSZ018N04LS6	40 V, 1.8 mΩ
Switch Q_5-Q_{10}	Infineon BSZ010NE2LS5	25 V, 1 mΩ
Flying capacitor C_1	TDK C2012X5R1V226M125AC	X5R, 35 V, 22 μF*×14
Flying capacitor C_2	TDK C2012X7S1E106K125AC	X7S, 25 V, 10 μF*×16
Flying capacitor C_3	Murata GRM21BR61A476ME15L	X5R, 10 V, 47 μF*×16
Resonant inductor L	Coilcraft SLC7530S-500ML	50 nH, 50 A I_{sat}
Gate driver	Analog Devices LTC4440	80 V, high-side
Bootstrap diode	Infineon BAT6402VH6327XTSA1	40 V, Schottky

* The capacitance listed here is the nominal value before dc derating.

Table 7.5 lists the specifications of the main components. Thanks to the reduced-voltage stress of the doubler topology, low voltage silicon MOSFETs can be used (40 V for Q_{1-4} and 25 V for Q_{5-10}). In order to reduce the output impedance, Q_{8-10} are each implemented with two paralleled switches, one on each side of the board. The cascaded bootstrap method discussed in Chapter 5 is used to power the floating gate drivers. The PCB has 4 layers and is fabricated with 4 oz copper on the outer layers (where the critical conduction path is) and 3 oz copper on the inner layers.

The minimum switching frequency is determined by the inductor and the capacitor C_3, where $f_{\text{sw,min}} = \frac{1}{2\pi\sqrt{LC_3}}$. However, as discussed in Chapter 6, to counteract the effects of component non-idealities and further reduce the conduction loss, the converter can operate at a frequency that is slightly higher than resonance, at the expense of imperfect ZCS operation and slightly increased switching loss. For this prototype, $f_{\text{sw,min}} = 52$ kHz and the actual switching frequency is 70 kHz when operating at 48-to-6 V. Measured waveforms of inductor current and switch node voltage are shown in Fig. 7.7. The converter is also able

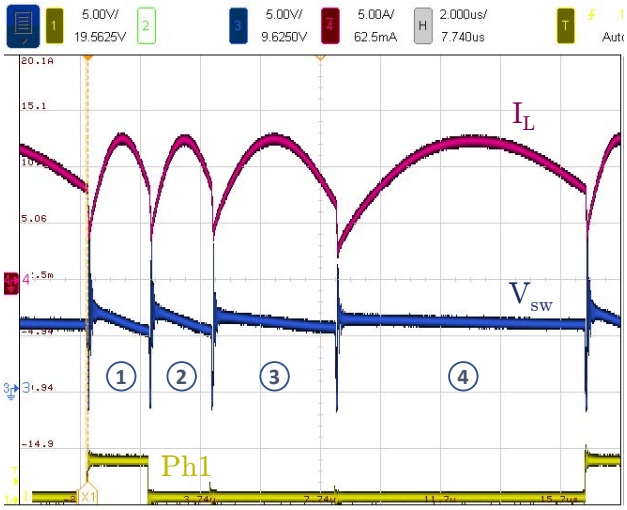


Figure 7.7: Waveform of inductor current and switch node voltage.

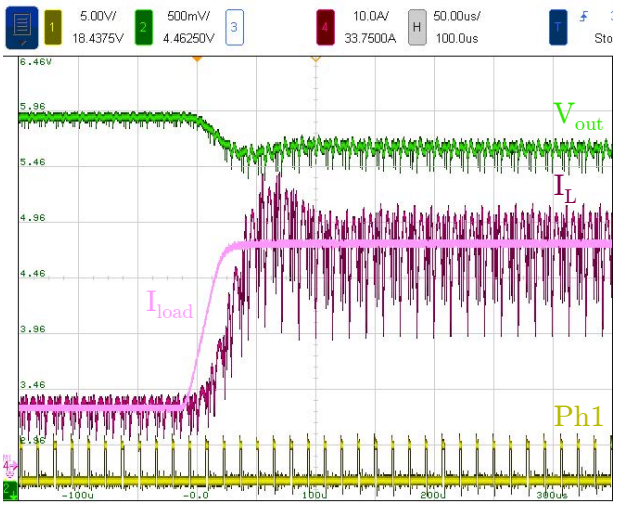


Figure 7.8: Load-step from 10 A to 40 A at 48 to 6 V.

to handle large load transients. In Fig. 7.8, the output voltage does not show significant undershoot after a 10 A to 40 A load step and stabilizes within a few switching cycles.

The converter has been tested up to 40 A output current. Based on the volume of the smallest rectangular box that can contain the converter, the power density is 1675 W/in^3 (102 kW/L) for 48-to-6 V conversion and 2100 W/in^3 (128 kW/L) for 60-to-7.5 V conversion. The efficiency is measured with a Yokogawa WT3000E precision power meter, and the results are plotted in Fig. 7.9 to Fig. 7.11 for various input voltages. For the nominal 48-to-6 V conversion, the peak efficiency is 98.6% (98.0% including gate drive loss). The full load

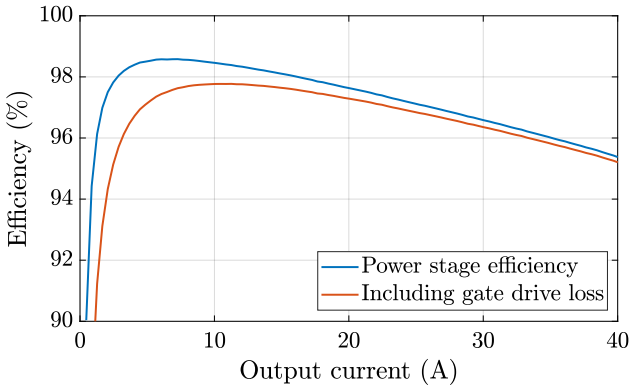


Figure 7.9: Measured 40 V to 5 V efficiency ($f_{\text{sw}} = 70$ kHz).

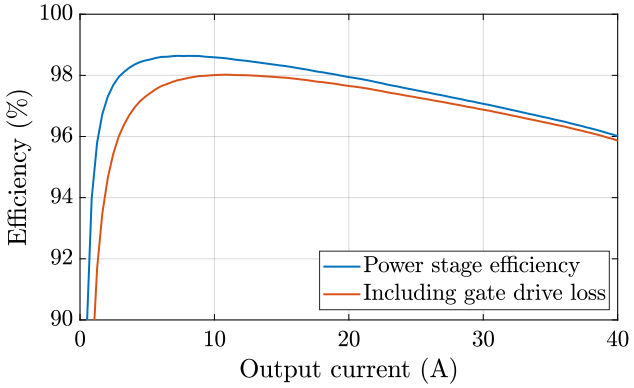


Figure 7.10: Measured 48 V to 6 V efficiency ($f_{\text{sw}} = 70$ kHz).

efficiency at 40 A is 96.0% (95.9% including gate drive loss). The high efficiency performance can greatly reduce the thermal management requirement. As shown in Fig. 7.12, the converter maintains a maximum temperature of around 60°C at full power with fan cooling only. Additionally, the high efficiency also reduces the impact of load regulation. Even though the converter operates in fixed-ratio mode (open loop), the output voltage only droops 250 mV (4.2% of V_{out}) at full load as depicted in Fig. 7.13.

Table 7.6 compares this work with some of the best existing works. Compared with the best in-class LLC converter [127], this work has very similar efficiency performance, but can achieve 50% more power density at a much lower power rating. This makes it easy to be placed very close to the actual load to minimize the power distribution loss, while maintaining the flexibility to scale up for higher power needs. Since there are no other 8-to-1 SC works for this application yet, we also compare the results with the 4-to-1 switched-tank converter [23]. Although the efficiency is slightly lower, the MRD can achieve doubled conversion ratio with much higher power density.

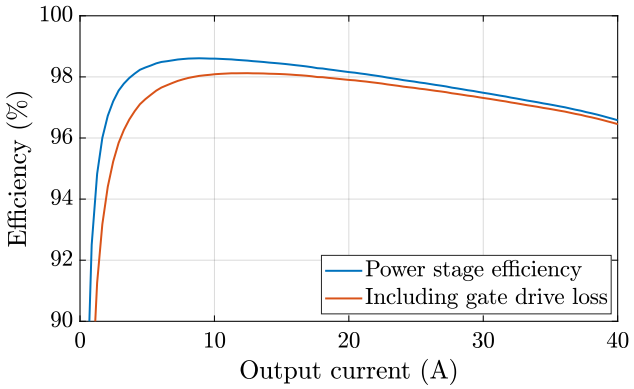


Figure 7.11: Measured 60 V to 7.5 V efficiency ($f_{\text{sw}} = 78$ kHz).

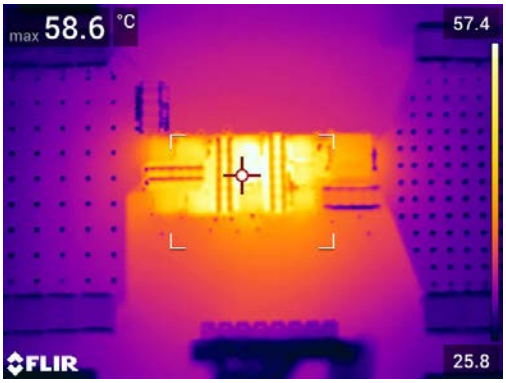


Figure 7.12: Thermal performance with fan cooling only ($V_{\text{in}} = 48$ V, $I_{\text{out}} = 40$ A).

Parallel Operation for Higher Output Power

Owing to the nature of multi-phase operation, part of the converter only operates for a portion of the switching period. As shown in Fig. 7.14, capacitor C_1 (rated at 4 V_{o}) only operates in the first quarter period and C_2 (rated at 2 V_{o}) operates in the first half period. This unique characteristic can potentially be utilized to save component counts and space in interleaved parallel operation for higher output power. Since the first doubler stage ($8V_{\text{o}}$ to $4V_{\text{o}}$) only operates for one quarter of the period, it can be used to drive four paralleled phases (with 90° phase shift each), only at the cost of increased switching frequency (thereby switching loss) of the first stage, and four additional switches for the four parallel phases in the second stage. Similarly, each doubler at the second stage ($4V_{\text{o}}$ to $2V_{\text{o}}$) can drive two following stages ($2V_{\text{o}}$ to V_{o}). This arrangement can help fully utilize the availability of all circuit components, and save space and cost compared to traditional interleaving designs with straightforward converter paralleling. A simple version of this concept is demonstrated in [137].

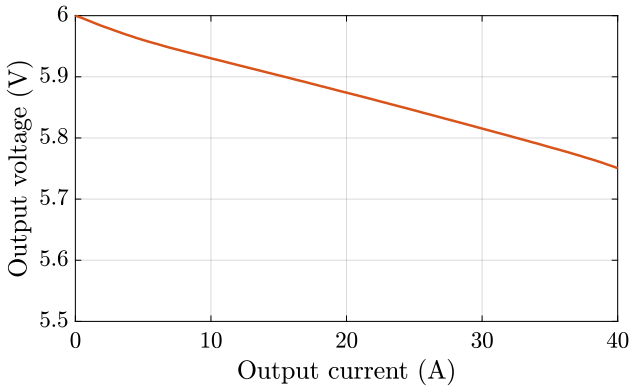


Figure 7.13: Load regulation ($V_{\text{in}} = 48$ V, $V_{\text{out}} = 6$ V).

Table 7.6: Comparison of this work and existing high-step-down bus converters

Reference	Topology	Voltage ratio	Output current	Power Density (W/inch^3)	System Efficiency	Notes
This work	Resonant Multi-phase Doubler	48-to-6 V	40 A	1675	full load: 95.9% peak: 98.0%	fixed-ratio, silicon MOSFET
EPC AppNote014 [127]	LLC	48-to-6 V	150 A	1100	full load: 96.9% peak: 98.0%	fixed-ratio, Gen-5 GaN FET
EPC9205 [136]	Buck	48-to-6 V	14 A	$\leq$ 900	full load: 91.8% peak: 93.9%	Gen-5 GaN FET
Google Switched-Tank [23]	Resonant Dickson	54-to-13.5 V	50 A	500	full load: 97.41% peak: 98.61%	54 V input, 4:1 fixed-ratio, components are not densely populated

7.5 6-to-1 Cascaded Series-Parallel Converter

Operating Principle

With the same fundamental structure and the same number of components, the MRD converter can be converted to a 6-to-1 multi-resonant SC converter, by moving the source terminal of Q_5 from the positive side of C_3 to the switch node. Its circuit schematic is shown in Fig. 7.15. Through three-phase operation, the converter can behave as a 2-to-1 converter cascaded with a 3-to-1 series-parallel converter, herein named cascaded series-parallel converter. Thanks to the multi-phase operation, this topology uses fewer switches and capacitors than other two-phase 6-to-1 SC converters. Even though its conversion ratio is not as high as that of the MRD converter, its series-parallel stage can split the output current into two paths, thus reducing the conduction loss and improving the conversion efficiency.

The key control signals, inductor and capacitor current waveforms, and the equivalent circuit of the three operating phases are shown in Fig. 7.16. It can be seen that, the converter achieves a 2-to-1 step-down during the first $\frac{1}{3}$ of the switching period through a series-mode

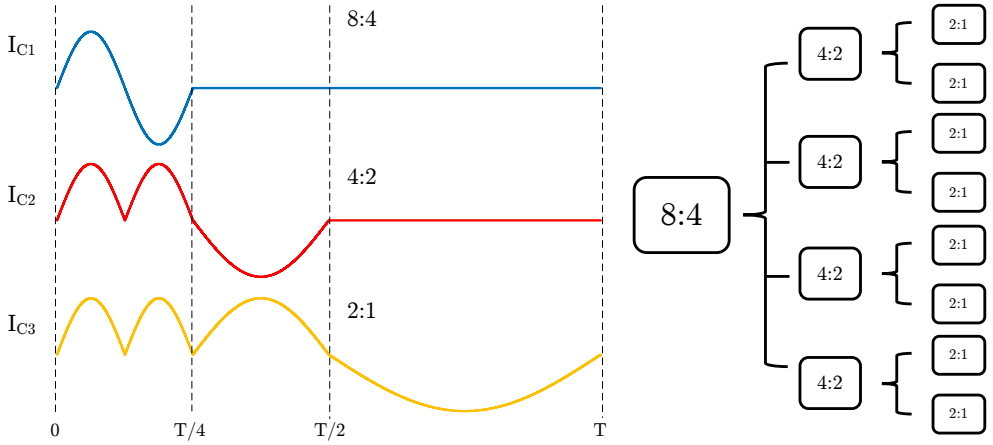


Figure 7.14: Parallel operation of MRD converters to optimize the utilization of the flying capacitors and the associated switches.

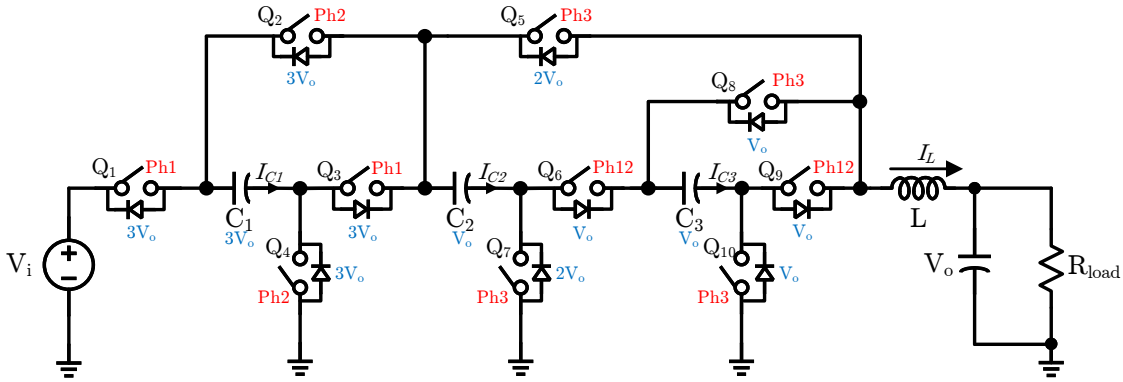


Figure 7.15: Schematic drawing of the 6-to-1 cascaded series-parallel converter with device ratings and control signals labeled.

operation, followed by a 3-to-1 parallel-mode operation during the last $\frac{2}{3}$ of the switching period. The detailed operation of the three phases are as follows:

- Phase 1: The "Ph1" and "Ph12" switches in Fig. 7.15 are ON. C_1, C_2, C_3 and L are connected in series. All flying capacitors are resonantly charged by the input. The duration of Phase 1 is $\frac{1}{6}$ of the switching cycle. The equivalent resonant frequency of this phase is $f_{r,\text{ph1}} = \frac{1}{2\pi\sqrt{LC_{eq1}}}$, where $\frac{1}{C_{eq1}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$.

- Phase 2: The "Ph2" and "Ph12" switches are ON. In this phase, all flying capacitors are still connected in series, but C_1 is being discharged. The length of the phase and

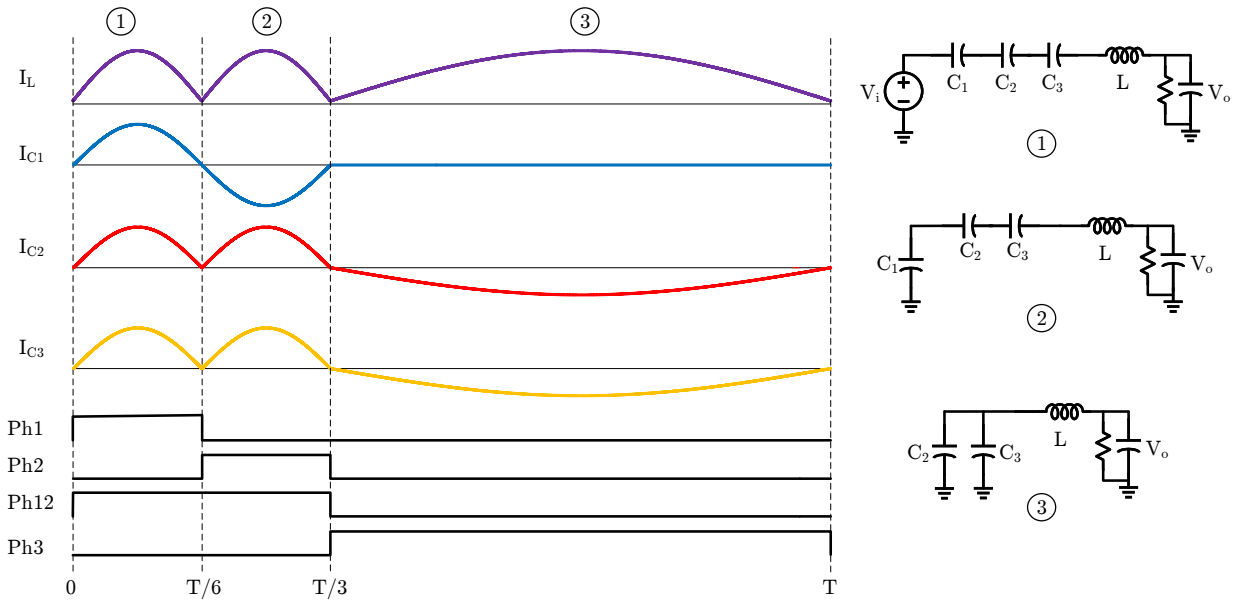


Figure 7.16: Inductor and capacitor current waveforms, control signals, and equivalent circuits of the 6-to-1 cascaded series-parallel converter.

the equivalent resonant frequency remain the same as in Phase 1.

- Phase 3: Only the "Ph3" switches are ON. In this phase, C_1 is disconnected, C_2 and C_3 are in parallel, and are resonantly discharged to the load. The equivalent resonant frequency of this phase is $f_{r,\text{ph3}} = \frac{1}{2\pi\sqrt{L(C_2+C_3)}}$.

The parallel operation in Phase 3 demands that $C_2 = C_3 = C$, while capacitor charge balance analysis of C_1 indicates that the minimum C_1 that is required to achieve soft-charging operation is $C_{1,\text{min}} = \frac{1}{6}C$.

Using the methodology outlined in Section 3.5, Fig. 7.17 compares the theoretical passive and active component utilization of various ReSC converters at a conversion ratio of 6-to-1. A buck converter is also included for reference. It can be seen that, the proposed cascaded series-parallel converter can achieve similar theoretical performance to the series-parallel converter even with a greatly reduced number of components. This is of note as the passive volume of the series-parallel topology is known to be at the theoretical lower limit [25]. Compared to the switched-tank converter (STC), the cascaded series-parallel converter can potentially achieve higher power density, even though the switch stress is higher. Moreover, as discussed in [138], the efficiency performance of the series-parallel based converters is underestimated by the switch VA analysis, when the switches cannot be sized optimally due to limited selections in discrete designs. This is often the case for ReSC-based 48 V

Table IV: Measured Converter Performance

Metric	V_{in} = 40 V f_{sw} = 65 kHz	V_{in} = 48 V f_{sw} = 68 kHz
Peak Efficiency	99.0% (98.4% with gate loss)	99.0% (98.5% with gate loss)
Full-Load Efficiency	96.7% (96.6% with gate loss)	97.1% (97.0% with gate loss)
Power Density	1840 W/in^3	2230 W/in^3

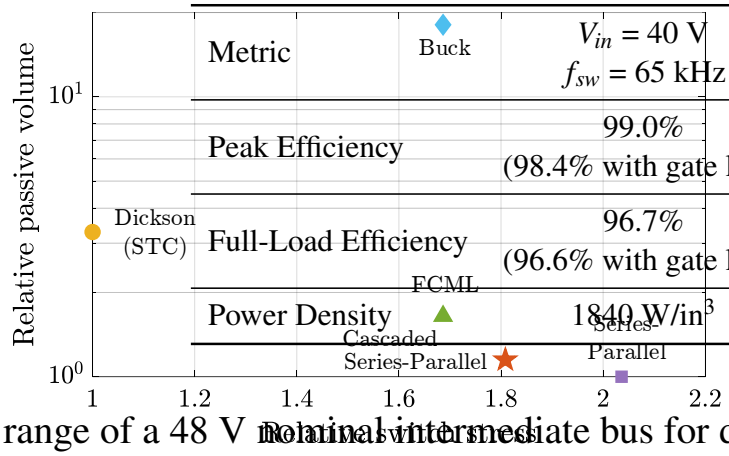


Figure 7.17: Theoretical performance comparison between several 6-to-1 converters.

range of a 48 V nominal intermediate bus for datacenter applications. Efficie
and 54-to-9 V operation are shown in Fig. 5 and Fig. 7. Table IV lists the e
of the converter for all tested input voltage and frequency conditions.

Fig. 5: Relative passive volume vs. normalized switch stress for several 6-to-1 converters.

well as the low output impedance exhibited by the converter due to its many parallel curre
The proposed topology operat opology, and has
to exhibit very high performa Dickson-based to
to its low passive volume and antage of switch
relatively mild considering the

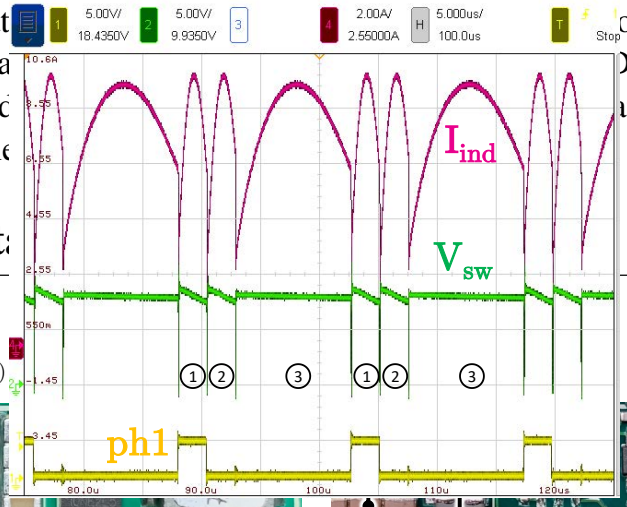


Fig. 9: Inductor current, switch node voltage, and ph1 gate signal waveforms for 48-to-8 V.

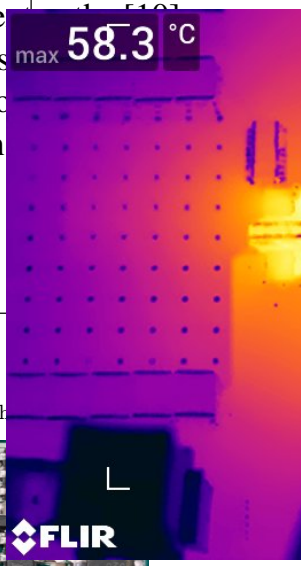


Fig. 10: Thermal i
48-to-8 V operatio

Hardware Implement

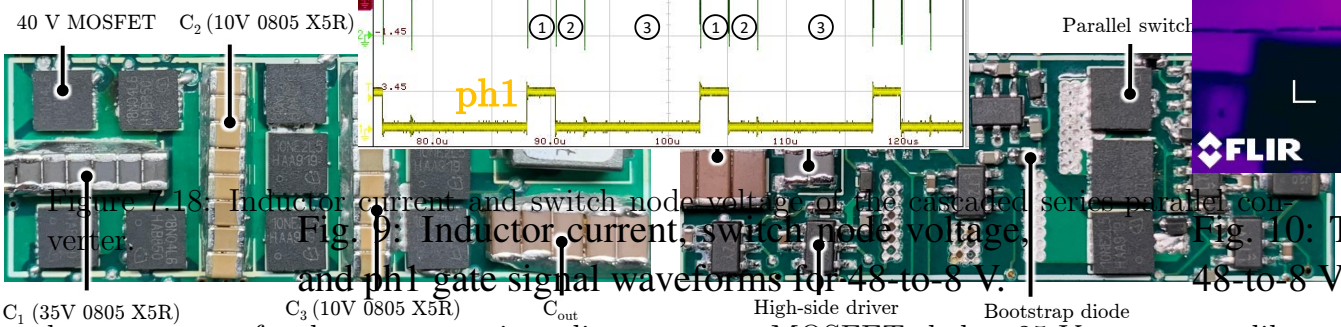


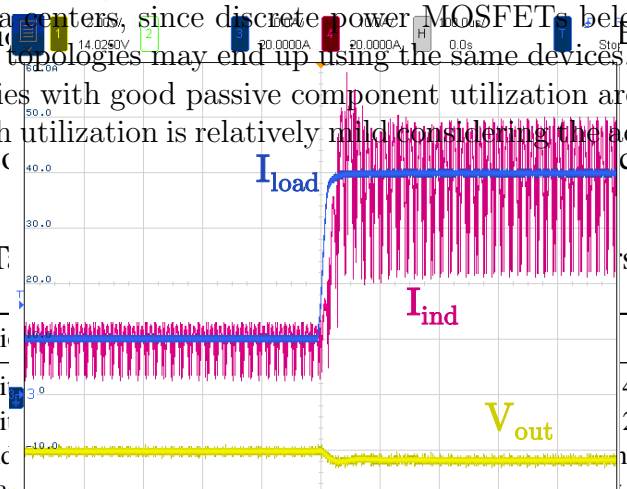
Figure 7.18: Inductor current and switch node voltage of the cascaded series-parallel converter.

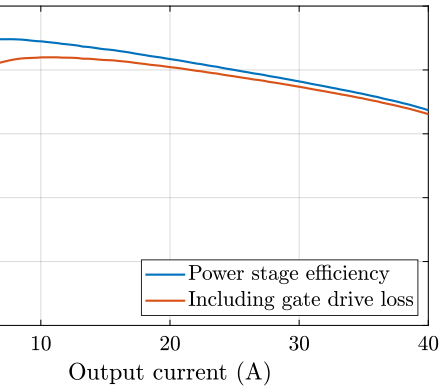
bus converters for datacenters, since discrete power MOSFETs below 25 V are not readily
available and different topologies may end up using the same devices. As a result, the series-
parallel based topologies with good passive component utilization are more favored, as their
disadvantageous switch utilization is relatively mild considering the actual switches available.

Fig. 4: Photograph of the c ch (3.5 × 1.17 × 0.5

T s

Component	Descripti	Value
Q1-Q4	40 V Si swi	40 V, 40 A, 1.8 mΩ
Q5-Q10	25 V Si swi	25 V, 40 A, 1.0 mΩ
L	Resonant inc	nH, 50 A I_{sat}, 0.123 mΩ
C1	Flying Capa	22 µF* 35 V X5R 0805





ig. 5: Measured efficiency 0 to 6.7 V, f_{sw} = 65 kHz).

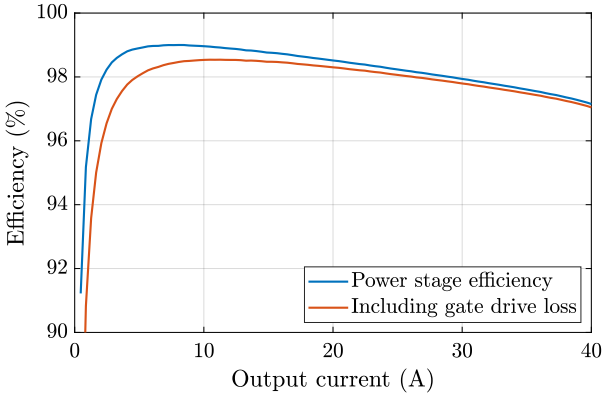
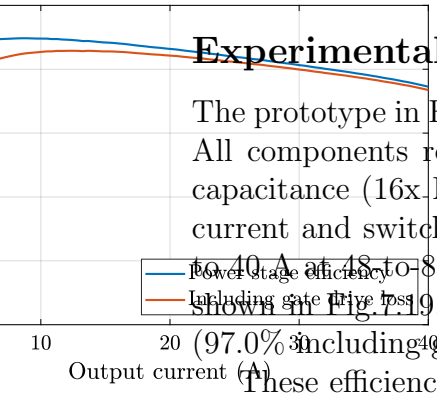


Figure 7.19: Measured 48 V to 8 V efficiency of the cascaded series-parallel converter (f_{sw} = 68 kHz).

Fig. 6: Measured efficiency 48 to 8 V, f_{sw} = 68 kHz.



ig. 7: Measured efficiency 54 to 9 V, f_{sw} = 75 kHz.

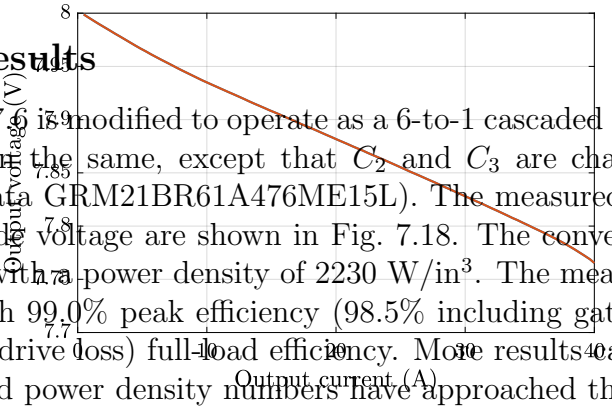


Fig. 8: Load regulation V_{in} = 48 V, V_{out} = 8 V.

Experimental Results

The prototype in Fig. 7.6 is modified to operate as a 6-to-1 cascaded series-parallel converter. All components remain the same, except that C_2 and C_3 are changed to have the same capacitance (16x Murata GRM21BR61A476ME15L). The measured waveforms of inductor current and switch node voltage are shown in Fig. 7.18. The converter has been tested up to 40 A at 48-to-8 V, with a power density of 2230 W/in^3. The measured efficiency result is shown in Fig. 7.19, with 99.0% peak efficiency (98.5% including gate drive loss) and 97.1% (97.0% including gate drive loss) full-load efficiency. More results can be found in [139].

These efficiency and power density numbers have approached those of the cascaded resonant converter with a 4-to-1 ratio in Chapter 6, demonstrating the great potential of this cascaded series-parallel topology. Note that the tested hardware is designed for the MRD converter with the source terminal of Q_5 connected to the drain terminal of Q_8. Consequently, Q_8 in fact carries all of the output current rather than half as shown in Fig. 7.15. With hardware specifically optimized for this topology, higher efficiency performance can be expected.

7.6 Alternative Topology Variations

The presented MRD and cascaded series-parallel multi-resonant converters are modular, and can be extended to higher conversion ratios. The basic building block is shown in Fig. 7.20. It consists of three switches and one capacitor. Depending on the desired conversion ratio and the number of operating phases, the right side of Q_1 can be connected either to the neighboring block to form a doubler stage, or to the output inductor to form a series-parallel stage.

e, as at these low voltages the performance of Si can match that of GaN. The high-current ($Q_8 - Q_{10}$) are paralleled to reduce conduction losses. Each floating switch is driven by a side gate driver powered using the cascaded bootstrap method [21], from a 9 V source. The ve current was measured with a Yokogawa WT310 digital power meter, while the power current, and efficiency was measured with a Yokogawa WT3000 precision power meter accurate results at the high efficiencies obtained. Table II lists the components used in the

the operating conditions. The gate drive signals were programmed with a constant deadtime. e converter was tested up to 40 A output current and achieved a peak efficiency of 99.0% d efficiency of 97.1% (98.5% and 97.0% with gate drive loss included, respectively) for tep-down conversion operating at 68 kHz. The power density at full-load was 2230 Win^3 olume of 0.139 in^3 (2.29 cm^3). Efficiency curves for 48-to-8 V operation from 0 A to 40 A ig. 6. Efficiency curves were also taken for additional voltage levels within the expected

Table III: Converter Operating Conditions

Parameter	Value

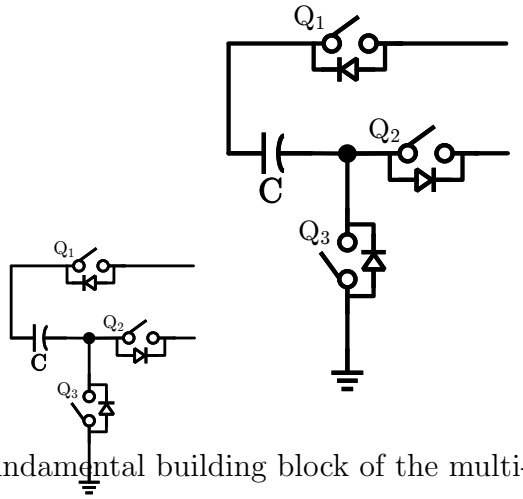


Figure 7.20: Fundamental building block of the multi-phase resonant SC converter.

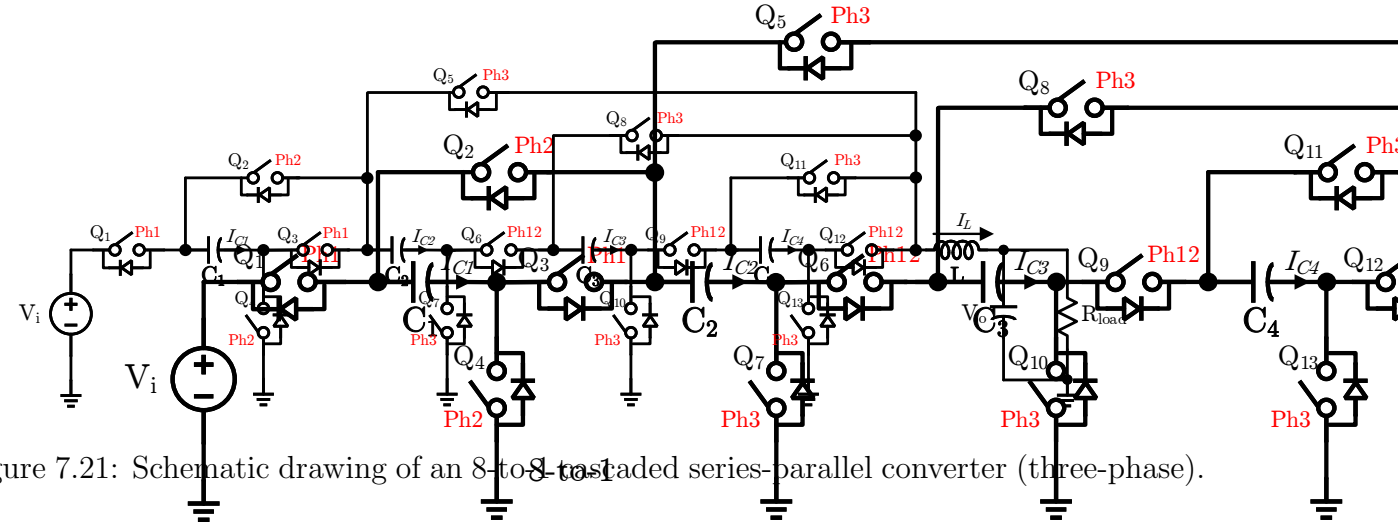
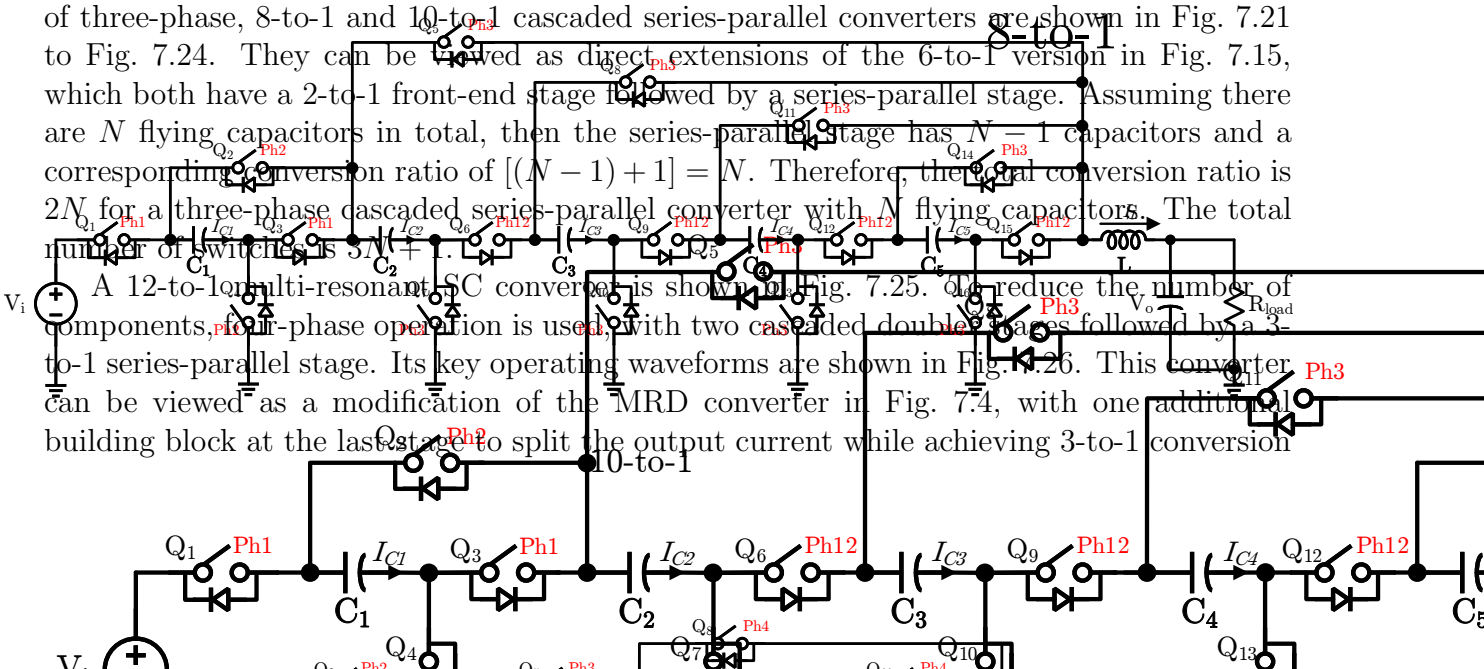


Figure 7.21: Schematic drawing of an 8-to-1 cascaded series-parallel converter (three-phase).

A few examples are demonstrated here. The circuit schematics and operating waveforms of three-phase, 8-to-1 and 10-to-1 cascaded series-parallel converters are shown in Fig. 7.21 to Fig. 7.24. They can be viewed as direct extensions of the 6-to-1 version in Fig. 7.15, which both have a 2-to-1 front-end stage followed by a series-parallel stage. Assuming there are N flying capacitors in total, then the series-parallel stage has $N-1$ capacitors and a corresponding conversion ratio of $[(N-1)+1]=N$. Therefore, the total conversion ratio is $2N$ for a three-phase cascaded series-parallel converter with N flying capacitors. The total number of switches is $3N+1$.

A 12-to-1 multi-resonant SC converter is shown in Fig. 7.25. To reduce the number of components, four-phase operation is used, with two cascaded double stages followed by a 3-to-1 series-parallel stage. Its key operating waveforms are shown in Fig. 7.26. This converter can be viewed as a modification of the MRD converter in Fig. 7.4, with one additional building block at the last stage to split the output current while achieving 3-to-1 conversion



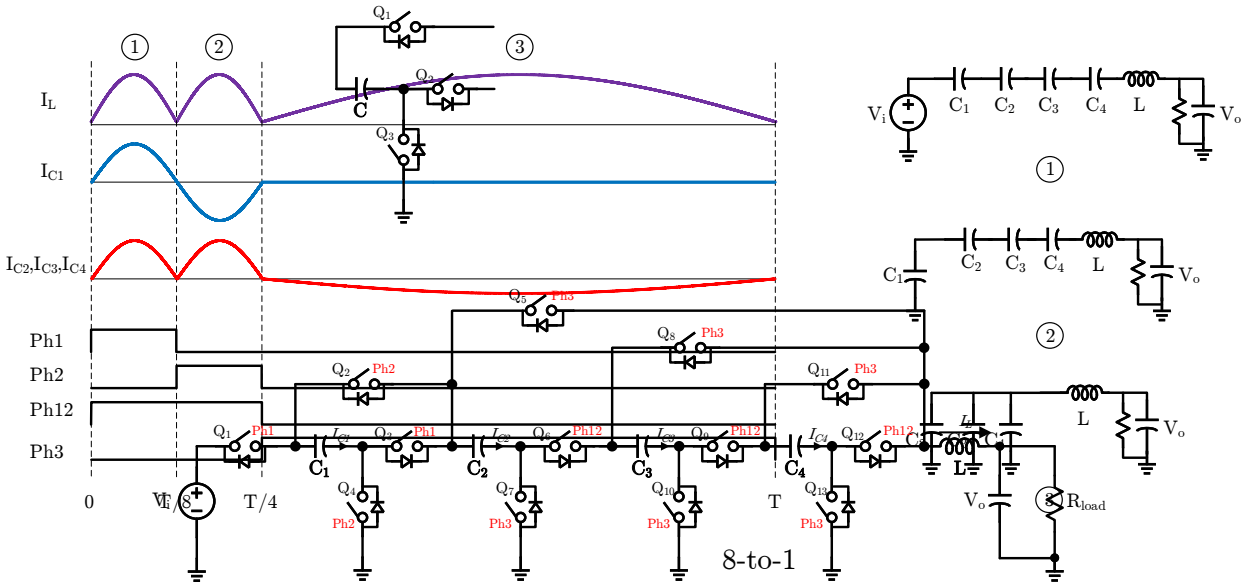


Figure 7.22: Inductor and capacitor current waveforms, control signals, and equivalent circuits of the 8-to-1 cascaded series-parallel converter.

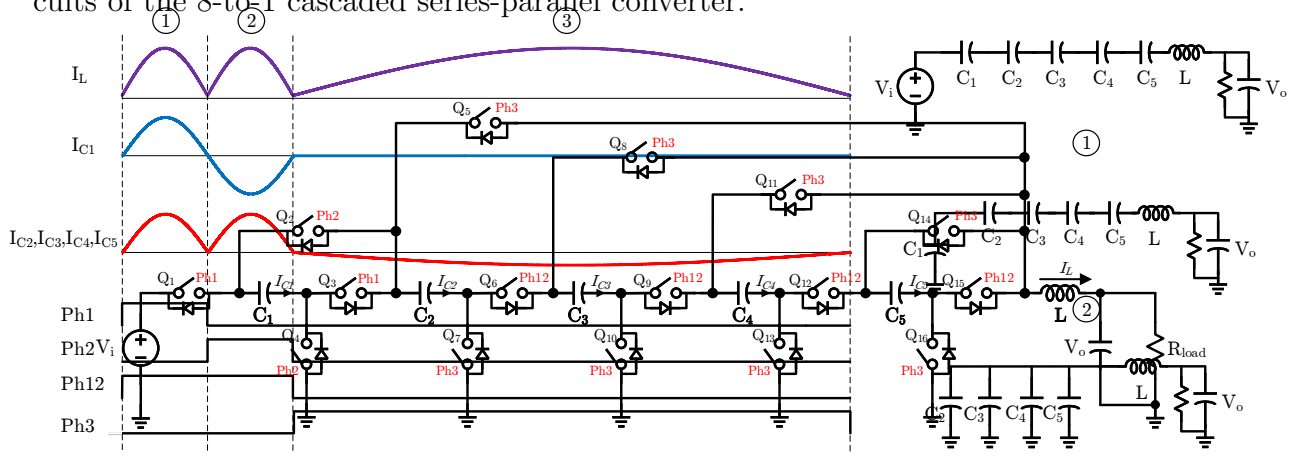
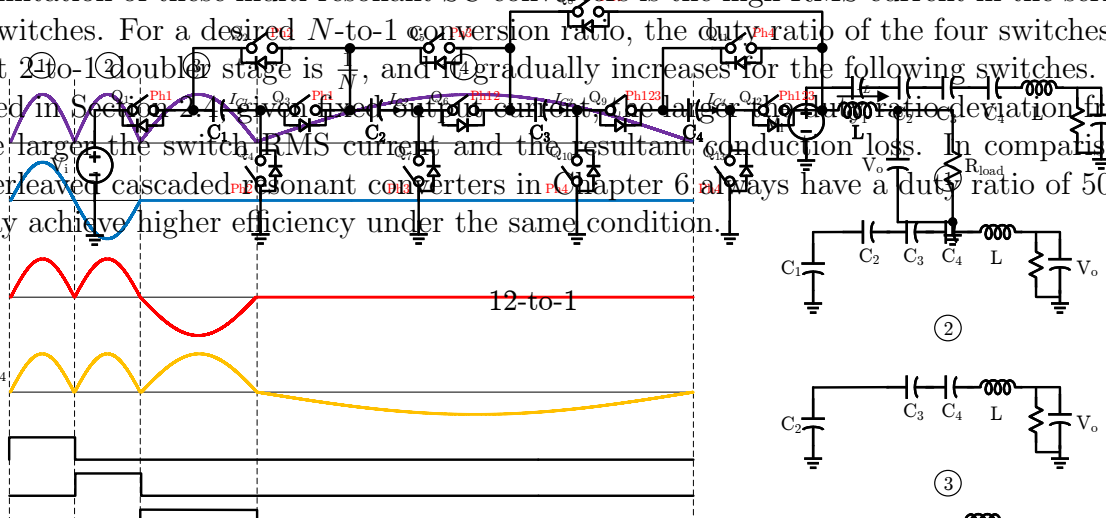


Figure 7.23: Schematic drawing of a 10-to-1 cascaded series-parallel converter (three-phase).

ratio.

A limitation of these multi-resonant SC converters is the high RMS current in the series-mode switches. For a desired N-to-1 conversion ratio, the duty ratio of the four switches in the first 2-to-1 doubler stage is $\frac{1}{N}$, and it gradually increases for the following switches. As discussed in Section 3.4.3, given fixed output current, the large duty ratio deviation from 0.5, the larger the switch RMS current and the resultant conduction loss. In comparison, the interleaved cascaded resonant converters in Chapter 6 always have a duty ratio of 50%, and may achieve higher efficiency under the same condition.



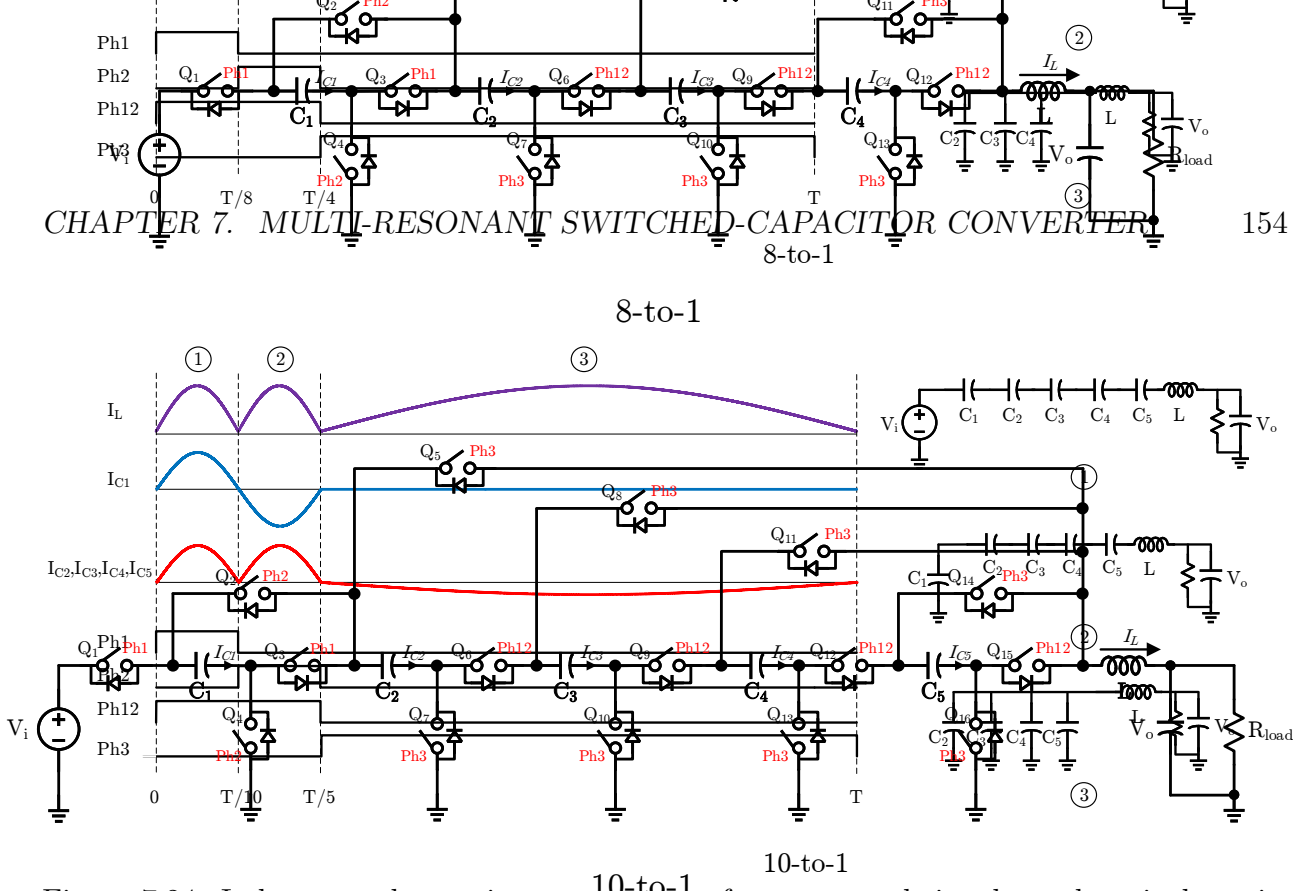


Figure 7.24: Inductor and capacitor current waveforms, control signals, and equivalent circuits of the 10-to-1 cascaded series-parallel converter.

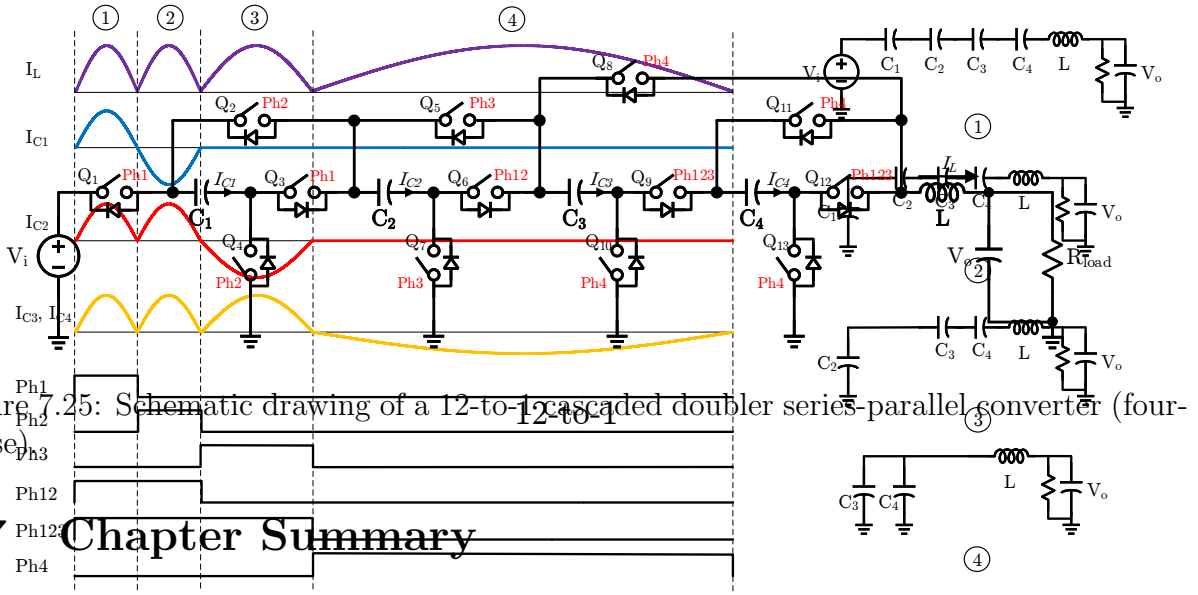
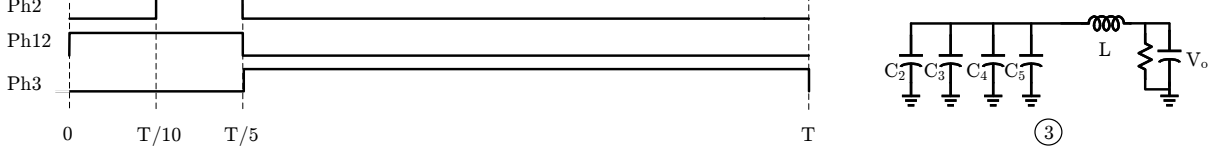


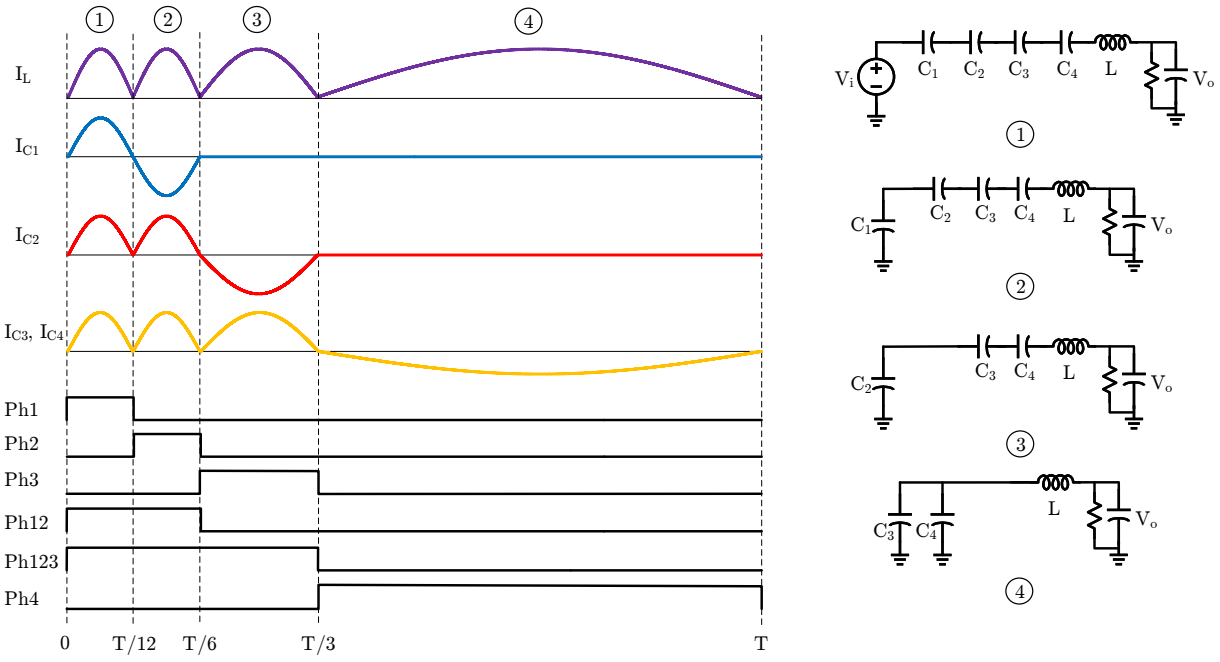
Figure 7.25: Schematic drawing of a 12-to-1 cascaded doubler series-parallel converter (four-phase).

7.7 Chapter Summary

In this chapter, the concept of multi-operating-phase is explored and applied to ReSC converters. Compared with two-phase operation, the multi-phase operation can achieve the same conversion ratio with significantly fewer capacitors and switches, leading to potentially better power density and efficiency performance. Two multi-resonant topologies, the 8-to-1 multi-resonant-doubler and the 6-to-1 cascaded series-parallel converter, are proposed and analyzed. Their superior performance is demonstrated by theoretical comparisons and hardware prototypes. At 48 V to 8 V, the cascaded series-parallel prototype achieves 99.0% peak efficiency (98.5% including gate drive loss), 97.1% full-load efficiency (97.0% including



10-to-1



12-to-1

Figure 7.26: Inductor and capacitor current waveforms, control signals, and equivalent circuits of the 12-to-1 cascaded doubler series-parallel converter.

gate drive loss), and 2230 W/in^3 power density. At 48 V to 6 V, the multi-resonant-doubler prototype achieves 98.6% peak efficiency (98.0% including gate drive loss), 96.0% full-load efficiency (95.9% including gate drive loss), and 1675 W/in^3 power density. These results show great promise of using multi-resonant SC converters in high step-down (and step-up) applications such as two-stage power delivery from a 48 V_{dc} bus in data centers.

Chapter 8

Multi-Level Binary Hybrid Switched-Capacitor Converter

This chapter presents a new hybrid SC topology to address the need of direct power conversion from 48 V_{dc} to point-of-load (PoL) voltages in datacenters. The proposed hybrid converter carries *Multi-Level Binary* (MLB) voltages on the flying capacitors, which make it well-suited for PoL applications with very high conversion ratios. It can be viewed as an 8-to-1 multi-phase doubler SC converter merged with a two-phase interleaved buck converter [140]. Compared to two-phase hybrid SC topologies, multi-phase operation can achieve higher conversion ratio at the SC stage with an equal or fewer number of components, and thus reduce the switch and inductor stress of the following buck stage. In addition, the output inductors in the proposed topology benefit from a frequency multiplication effect similar to that of FCML converters. This can help further reduce the inductor size without increasing the switching frequency.

8.1 Background and Motivation

As discussed in Chapter 6 and 7, to address the challenge of very high conversion ratio from 48 V_{dc} to the extreme low voltage and high current point-of-loads (PoL) in modern datacenters, a two-stage approach is commonly used. The 48 V is first converted to an intermediate bus voltage (e.g., 12, 8, 6 V) through a bus converter, then stepped down to 1–2 V by PoL converters [33], [105], [138], [139], [141]–[143]. However, depending on application specifics, a number of recent works have demonstrated direct 48 V to PoL conversion [109]–[113], and have shown promise for better overall efficiency, power density and reduced system cost. For such a high conversion ratio, a transformer-based converter is commonly used [110], [111]. Unavoidably, there is a trade-off between conversion efficiency and voltage regulation range. To address this challenge, the high step-down and the regulation requirements can be split between a highly efficient fixed-ratio LLC converter and an upstream buck-boost converter [112] or a series-stacked buck converter with partial power processing [113].

In addition to transformer-based solutions, recently proposed hybrid topologies comprising multi-phase buck converters merged with a fixed-ratio SC converter have also shown attractive features for direct 48 V to PoL conversion [18], [144], [145]. Similar to transformers, SC converters also have excellent performance at fixed-ratio conversions, thanks to their efficient utilization of active and passive components [7], [19], [25]. By combining the buck and the SC stages, the total number of components (e.g., switches and decoupling capacitors) can be reduced compared to cascaded two-stage solutions. More importantly, the inductors in the buck stage can greatly reduce or eliminate the capacitor charge sharing loss of the SC converter through soft-charging operation [16], [19], leading to very efficient fixed-ratio conversion in the SC stage. However, due to the fact that the circuit complexity of SC converters increases in proportion to the conversion ratio, the SC stage in the majority of existing hybrid works can only achieve a conversion ratio of 4-to-1 or 6-to-1, with the remaining conversion burden placed on the buck stage. Given a fixed output voltage, the efficiency of a buck converter generally decreases with increasing input voltage. If the first stage SC converter can achieve a higher conversion ratio without much extra loss, the input voltage of the buck converter can be decreased, and the overall 48V-to-PoL efficiency can be improved. References [104], [108] suggest that using a highly efficient 48 V to 6 V fixed-ratio converter in conjunction with a 6 V to PoL buck converter can provide improved overall efficiency.

This chapter proposes and explores a new hybrid topology with *Multi-Level Binary* (MLB) voltages on the flying capcitors that can simultaneously achieve high efficiency and power density for direct 48 V to PoL applications. The proposed MLB-PoL converter consists of an 8-to-1 SC stage and a two-phase interleaved buck stage with natural current balancing. By having multiple operating phases, the SC stage can achieve a conversion ratio of 8-to-1 with the theoretical minimum number of components (10 switches and 3 capacitors). The operation of the output buck stage is merged with the SC stage without the need for additional switches, thereby reducing the conduction loss. Furthermore, the inductors of the buck stage also benefit from a frequency multiplication effect similar to that of the FCML converter [45], [50]. This can further reduce the inductor size without increasing the switching frequency of the SC stage. A 48 V to 2.5–1.0 V converter prototype with 65 A output current is built and tested. At 48 V to 2 V, the prototype achieves 95.1% peak efficiency (94.3% including gate drive loss), 91.3% full load efficiency (91.1% including gate drive loss), and 395 W/in^3 power density.

8.2 Proposed Topology

The schematic drawing of the proposed MLB-PoL converter is shown in Fig. 8.1, with switch and capacitor voltage ratings labeled in red and operating phases labeled in blue. The voltage, current, and PWM waveforms of the converter and the equivalent circuit model of different operating phases are shown in Fig. 8.2. The proposed converter can be viewed as an 8-to-1 SC converter merged with a two-phase interleaved buck converter.

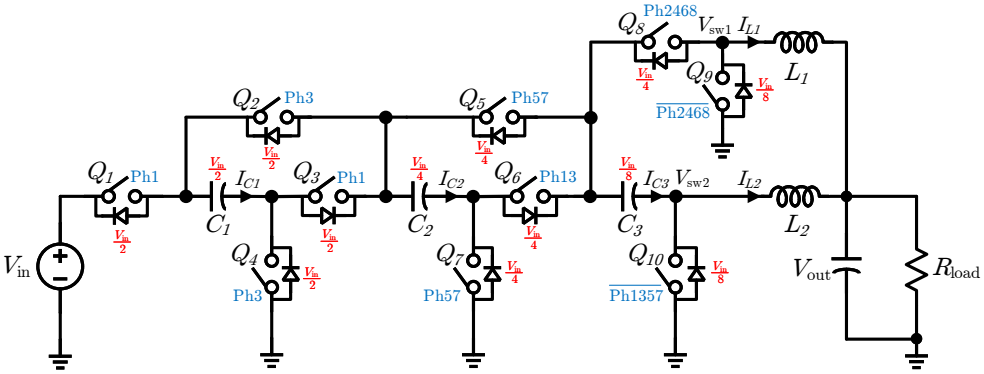
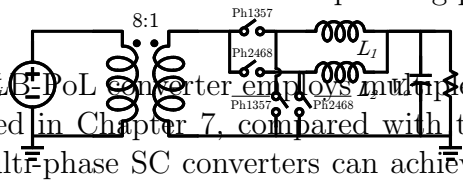


Figure 8.1: Schematic drawing of the proposed MLB-PoL converter. The device voltage ratings are labeled in red and the operating phases of the switches are labeled in blue.



The MLB-PoL converter employs multiple operating phases within each switching cycle. As discussed in Chapter 7, compared with typical SC converters that have two operating phases, multi-phase SC converters can achieve the same conversion ratio with significantly fewer switches and flying capacitors. The SC stage in the proposed topology is an 8-to-1 multi-phase voltage doubler (same as the multi-resonant-doubler ReSC converter in Chapter 7) [133], [142], which is one practical circuit implementation that achieves the theoretical maximum gain for an 8-to-1 SC converter (i.e., 10 switches and 3 capacitors). The flying capacitors carry binary voltages: $C_1 = \frac{1}{2}V_{\text{in}}$, $C_2 = \frac{1}{4}V_{\text{in}}$ and $C_3 = \frac{1}{8}V_{\text{in}}$, as do the switches: $Q_{1,2,3,4} = \frac{1}{2}V_{\text{in}}$, $Q_{5,6,7,8} = \frac{1}{4}V_{\text{in}}$ and $Q_{9,10} = \frac{1}{8}V_{\text{in}}$.

To maintain flying capacitor charge balance in multi-phase SC converters, the lower voltage capacitors must be charged/discharged for more time than the higher voltage ones [146]. Here, in order to merge the operation of the SC stage with the buck stage, the charge/discharge cycles of C_2 and C_3 are divided into multiple phases. As shown in Fig. 8.2, C_1 is charged in Phase 1 and discharged in Phase 3, C_2 is charged in Phase 1 and 3, and discharged in Phase 5 and 7, whereas C_3 is charged in Phases 1, 3, 5, 7 and discharged in Phases 2, 4, 6, 8. The operation of the two-phase interleaved buck stage is merged with the SC stage without additional switches. This can help reduce the conduction loss compared to a two-stage approach, where the buck converter is directly cascaded with a SC converter. The two inductors are energized (i.e., current ramped up) alternately: L_1 is energized by C_3 during Phases 2, 4, 6, 8, and L_2 is energized by the series combination of the flying capacitors during Phases 1, 3, 5, 7. Phase 9 is the freewheeling state for output voltage regulation where the current in both inductors ramps down.

There is an inherent current balancing mechanism between the two inductors. If I_{L1} is higher and over-discharges C_3, the switch node voltage of L_2 will then become higher, inducing a higher I_{L2} that can charge C_3 back to its nominal value. This operation is similar to the automatic current sharing behavior of the series-capacitor buck converter, which can

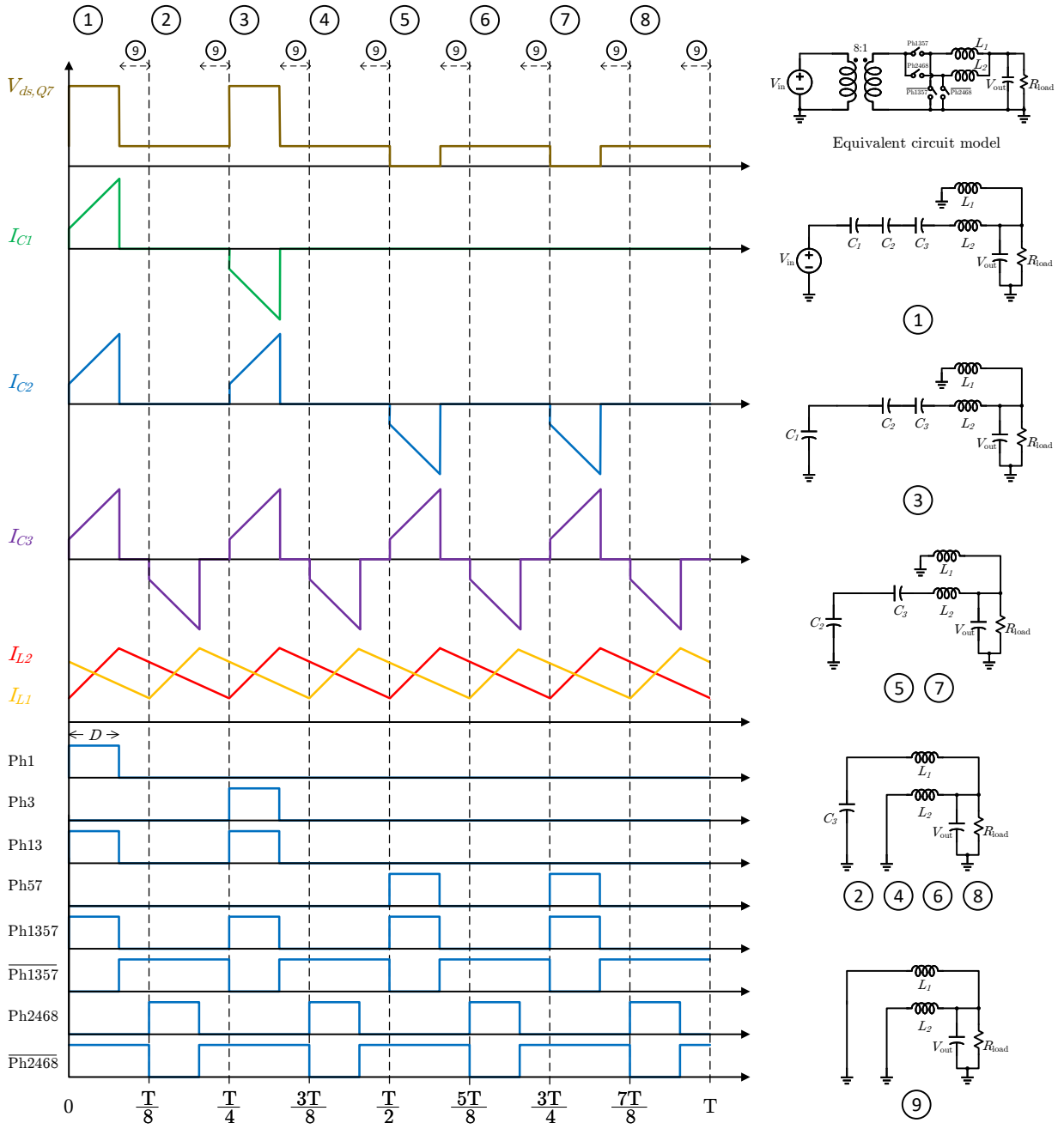


Figure 8.2: Voltage, current and PWM waveforms of the proposed MLB-PoL converter and equivalent circuit models.

be found in [147]. Here, C_3 acts as the series capacitor that creates a negative feedback loop between the capacitor voltage and the average inductor currents. There is a caveat

Table 8.1: Voltage rating and operating frequency of the main active and passive components

	V_{blocking}	f_{sw}
Q_1 - Q_4	$\frac{V_{\text{in}}}{2}$	f_0
Q_5 - Q_7	$\frac{V_{\text{in}}}{4}$	$2f_0$
Q_8	$\frac{V_{\text{in}}}{4}$	$4f_0$
Q_9 - Q_{10}	$\frac{V_{\text{in}}}{8}$	$4f_0$ (ZVS)
C_1	$\frac{V_{\text{in}}}{2}$	f_0
C_2	$\frac{V_{\text{in}}}{4}$	$2f_0$
C_3	$\frac{V_{\text{in}}}{8}$	$4f_0$
L_1,L_2	$\frac{V_{\text{in}}}{8}$ - V_{out}	$4f_0$

about negative inductor current. When operating in forced continuous-conduction mode, the inductor current may go negative at light load. When all switches are OFF during deadtime, the body diodes of Q_1, Q_2, Q_5, and Q_8 will conduct to keep the current flowing, and therefore connect the switch node V_{sw} to the input. This will result in excess voltage stress on certain switches. In order to clamp the switch node voltage and protect the switches, zener diodes or transient-voltage-suppression diodes can be added to the switch nodes. Owing to similar fundamental SC structures, this phenomenon also appears in the cascaded series-parallel converter and the multi-resonant-doubler converter presented in Chapter 7, and the same mitigation method can be applied.

The MLB-PoL topology also benefits from an inductor frequency multiplication effect similar to that of the FCML converter. Defining f_0 as the switching frequency of C_1 and the associated switches $Q_{1,2,3,4}$, then C_2 and $Q_{5,6,7}$ operate at $2f_0$ and C_3, $Q_{8,9,10}$, and $L_{1,2}$ operate at $4f_0$. Note that out of the three switches operating at $4f_0$, only Q_8 is hard switched at $\frac{V_{\text{in}}}{4}$, while Q_9 and Q_{10} operate with ZVS. In addition, the higher voltage rated switches operate at a lower frequency, reducing switching loss. This feature can provide inductor size reduction without increasing the frequency of all switches, particularly those with a higher voltage rating. The device voltage ratings and the corresponding switching frequencies are summarized in Table 8.1.

In order to derive the output voltage expression, we define D as the duty cycle of signal Ph1 as shown in Fig. 8.2. Since the inductors see four times the switching frequency, the effective duty cycle of the buck stage is $D_{\text{eff}} = \frac{DT}{\frac{T}{4}} = 4D$. The output voltage can then be derived by combining the conversion ratio of the fixed-ratio SC stage (DCX ratio) and the

Table 8.2: Comparison of the voltage conversion strategies of selected hybrid converters at 48 V to 2 V conversion

	DCX ratio	Buck ratio
This work	8:1	3:1
LEGO [18]	6:1	4:1
DIH [148]	6:1	4:1
MIH [144]	4:1	6:1
SC Buck [145], [149]	4:1	6:1

conversion ratio of the buck stage:

$$\begin{aligned} V_{\text{out}} &= V_{\text{in}} \cdot \text{DCX\_ratio} \cdot \text{buck\_ratio} \\ &= V_{\text{in}} \cdot \frac{1}{8} \cdot 4D \\ &= \frac{DV_{\text{in}}}{2}. \end{aligned} \tag{8.1}$$

As it is regulated with a duty cycle, the converter can share the same control techniques as that of conventional buck converters. Note that the maximum D is limited by the length of each operating phase to $\frac{1}{8}$. Thus, the highest output voltage of the proposed converter is $\frac{V_{\text{in}}}{16}$. With 48 V input, the maximum output voltage at the no-load condition is 3 V, making it incapable of supplying loads at 3.3 V. This reduced output range is a trade-off compared to other hybrid topologies with 4-to-1 or 6-to-1 SC stages. Nevertheless, if a lower output voltage is desired, the proposed converter with its 8-to-1 SC stage has the potential to achieve better performance compared to the 4-to-1 and 6-to-1 topologies. As shown in Table 8.2, for the desired conversion from 48 V to 2 V, the proposed converter can achieve the highest DCX ratio at the SC stage among all hybrid topologies, resulting in reduced stress at the following buck stage. This reduced stress can improve the buck stage efficiency, which can have a substantial impact on the overall system efficiency. Moreover, it is found that the total switch VA rating ($\sum V_{ds} I_{rms}$) of the proposed converter can be as low as half that of a stand-alone buck converter, indicating better switch utilization in addition to reduced inductor stress.

8.3 Hardware Design and Experimental Results

A 48 V to 2.5–1.0 V hardware prototype with 65 A output current is designed and tested to verify the functionality of the proposed converter. The annotated photograph of the prototype is shown in Fig. 8.3, and the specifications of the key components are tabulated in Table 8.3. The main operating parameters are summarized in Table 8.4.

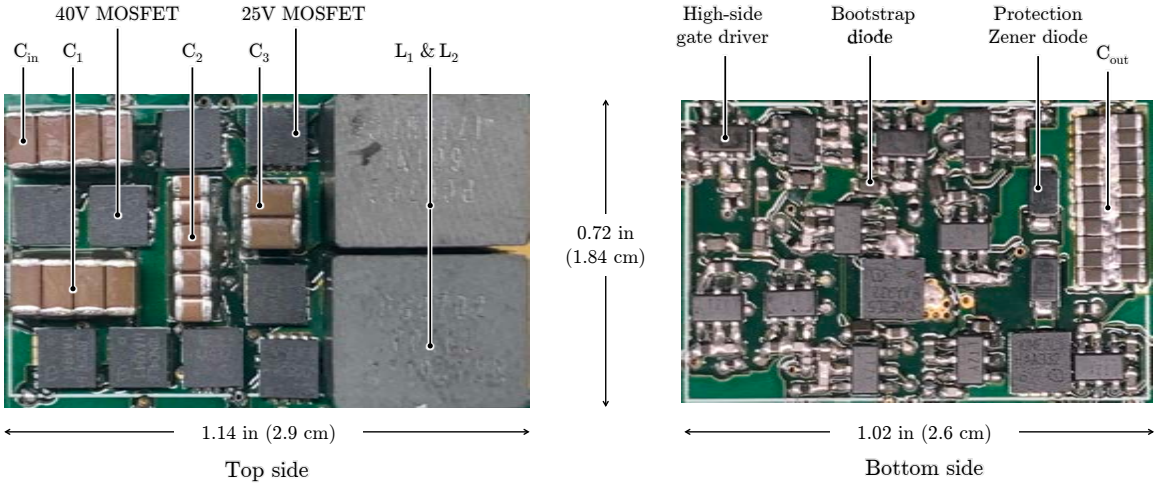


Figure 8.3: Photograph of the prototype. Dimensions: 1.14 × 0.72 × 0.39 inch (2.9 × 1.84 × 1.01 cm).

In order to report a power/current density number by box volume and to compare directly with other commercial power modules, all main components are tightly placed within a 1.14 inch by 0.72 inch (2.9 cm by 1.84 cm) rectangular PCB area. The switches, flying capacitors, and the inductors are on the top side, while the gate drive circuits and other protection components are placed directly underneath on the back side of the board. Input and output capacitors are also included in the box area. Due to the reduced voltage stress of the doubler SC topology, low-voltage MOSFETs can be used (40 V for Q_{1-4} and 25 V for Q_{5-10}). Since Q_{10} carries all of the output current, an additional switch is paralleled to reduce the conduction loss. High-side gate drivers with internal level-shifters are used to drive the switches, and a cascaded bootstrap circuit [73] is implemented to power the floating gate drivers. The PCB has 6 layers and is fabricated with 4 oz copper on the outer layers (where the critical conduction path is) and 2 oz copper on the inner layers.

The inductor selection is a critical design knob that affects the peak efficiency, the full-load efficiency, and the power/current density of the prototype. The Eaton HC1-1R0-R inductor used in [18] has high inductance (1 μH) and low DCR (1.23 mΩ), which may result in excellent peak and full-load efficiency. However, its bulky package size greatly limits the achievable box power/current density. The Coilcraft XAL7070-102 inductor has similar inductance and current rating, but comes in a smaller package size at the cost of higher DCR. It has the potential to achieve high peak efficiency and power density, though possibly at the expense of lower full-load efficiency compared to the Eaton inductor. Note that the peak efficiency of these hybrid converters usually appears at a very light-load condition, whereas the efficiency performance at middle to heavy load range might be more important in practical applications. Ultimately, the Pulse PG0702.601NL is selected, as it offers an

Table 8.3: Main component listing of the prototype

Component	Part number	Parameters
Switch Q_1-Q_4	Infineon BSZ018N04LS6	40 V, 1.8 mΩ
Switch Q_5-Q_8	Infineon BSZ010NE2LS5	25 V, 1.0 mΩ
Switch Q_9-Q_{10}	Infineon IQE006NE2LM5CG	25 V, 0.65 mΩ
Parallel Q_{10}	Infineon BSZ010NE2LS5	25 V, 1.0 mΩ
Flying capacitor C_1	TDK C3216X5R1V226M160AC	X5R, 35 V, 22 μF*×8
Flying capacitor C_2	TDK C2012X7S1E106K125AC	X7S, 25 V, 10 μF*×12
Flying capacitor C_3	TDK C3216X5R1A107M160AC	X5R, 10 V, 100 μF*×4
Inductor L_1,L_2	Pulse PG0702.601NL	600 nH, 0.91 mΩ
Input capacitor C_{in}	TDK C3216X7S2A335M160AB	X7S, 100 V, 3.3 μF*×8
Output capacitor C_{out}	TDK C1608X5R1A226M080AC	X5R, 10 V, 22 μF*×20
Gate driver	Analog Devices LTC4440-5	80 V, high-side
Bootstrap diode	Infineon BAT6402VH6327XTSA1	40 V, Schottky

* The capacitance listed here is the nominal value before dc derating.

Table 8.4: Key parameters of the prototype

Input voltage	48 V
Output voltage	1.0 - 2.5 V
Output current	65 A
Switching frequency (inductor)	250 kHz
Current density	198 A/in^3

attractive compromise between size and low DCR with a nominal inductance of 600 nH and a DCR of 0.95 mΩ, all in an acceptable package size. Although the peak efficiency of the prototype with this inductor is nearly 1% lower than a prototype using either of the 1 μH inductors, it achieves a good combination of high power/current density and full-load efficiency.

Compared to ReSC converters, the flying capacitor selection in these types of regulated hybrid SC converters is more relaxed, as the C and L values do not need to be tuned precisely so that the converter operates at the LC resonance point. The capacitance values have relatively minor effects on efficiency performance and flying capacitor voltage balancing. Nevertheless, it is important to make sure that the switches do not exceed their maximum voltage ratings and that the switch node voltage does not drop too low (i.e., to ground) due

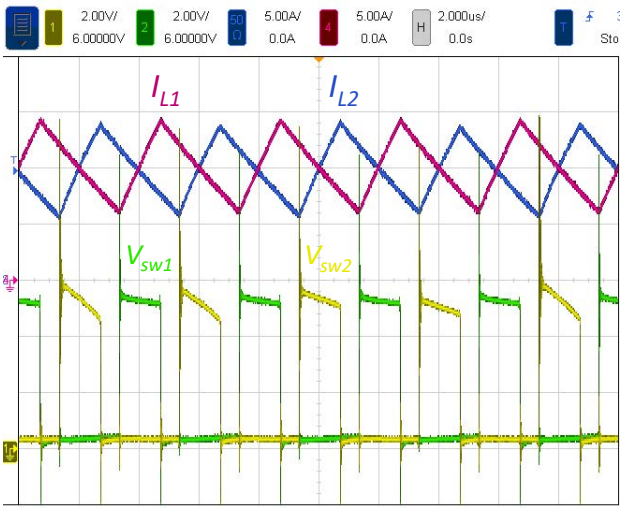


Figure 8.4: Balanced interleaved inductor currents ($V_{\text{out}} = 2$ V, $I_{\text{out}} = 20$ A).

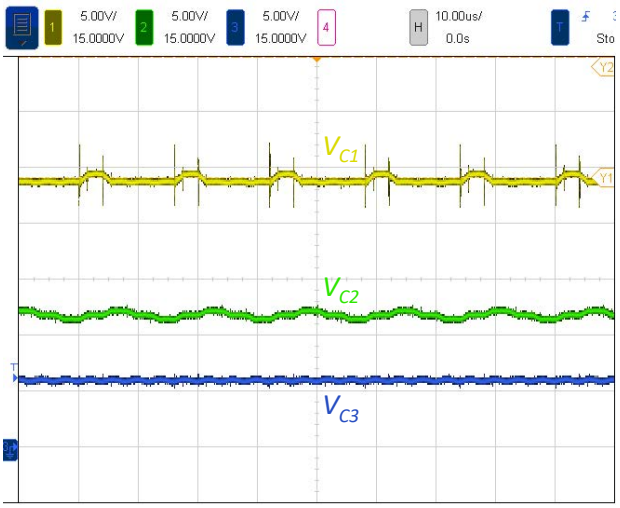


Figure 8.5: Flying capacitor voltages at $V_{\text{out}} = 2$ V and $I_{\text{out}} = 20$ A.

to the capacitor voltage ripple. Note that it may be possible to further reduce the amount of flying capacitance in the prototype, as the current design has not been fully optimized.

The two inductor currents and the corresponding switch node voltages are shown in Fig. 8.4, and exhibit good balancing. Fig. 8.5 shows the voltages across the C_1, C_2, and C_3 capacitors, which also exhibit good balancing, matching well with the theoretical values of 24 V, 12 V, and 6 V.

The performance of the prototype is measured with a Yokogawa WT3000E precision power meter. The converter is tested up to 65 A output current, resulting in a current density

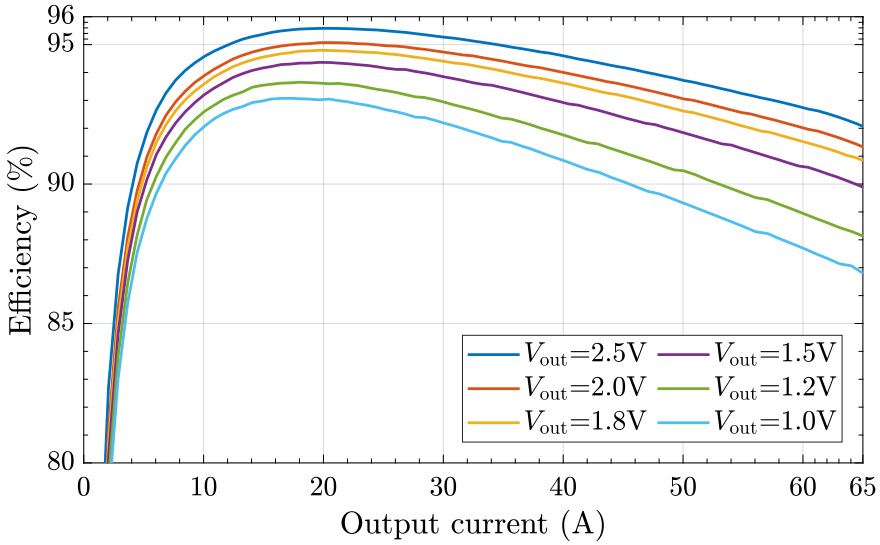
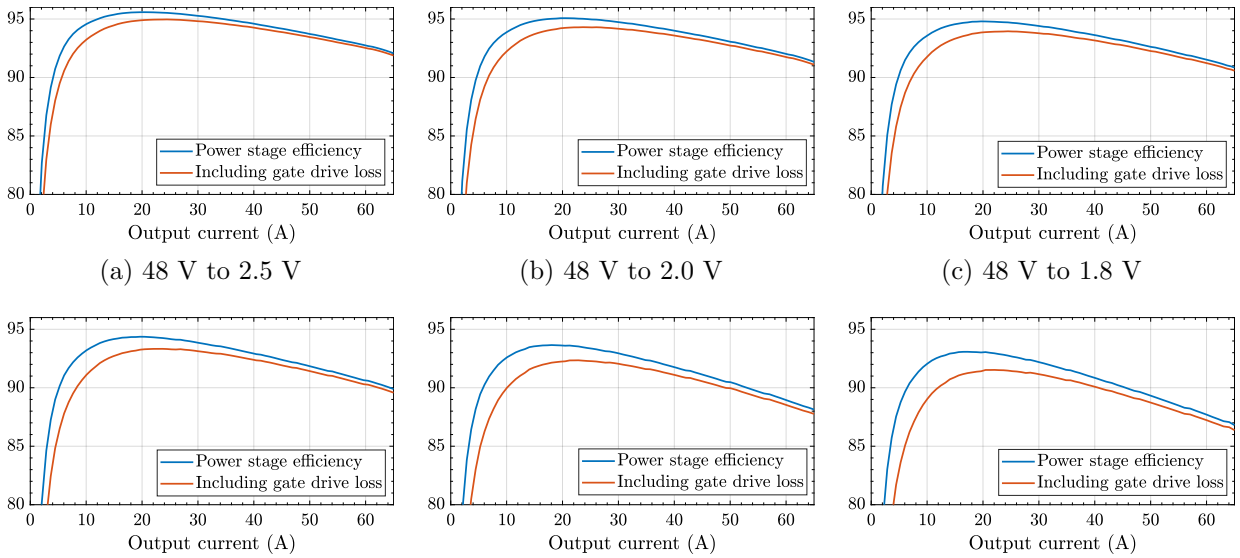


Figure 8.6: Measured power stage efficiency from 48 V to 2.5–1.0 V.

of 198 A/in^3 (as measured by the smallest rectangular box that can contain the converter). The measured power-stage efficiencies at various commonly-used output voltages are plotted in Fig. 8.6, and the corresponding system efficiencies with gate drive loss included are shown in Fig. 8.7. Table 8.5 summarizes the peak and full-load efficiencies of each output voltage, as well as the power density by box volume and surface area. The converter operates at an effective switching frequency of 250 kHz (as seen by the inductors). At 48 V to 2 V, the prototype achieves 95.1% peak efficiency (94.3% including gate drive loss), 91.3% full load efficiency (91.1% including gate drive loss), and 395 W/in^3 power density. As shown in Fig. 8.8, the maximum temperature of the board at thermal equilibrium is about 85°C, when operating at full-load with 110 CFM fan cooling only.

Table 8.6 compares this work with some of the best existing hybrid SC works with similar power ratings. As discussed previously, the proposed converter is designed to slightly trade peak efficiency at light-load for better heavy-load efficiency and power/current density. It can be seen that the proposed converter is able to carry the highest per-phase inductor current, while maintaining very good heavy-load efficiency. The comparison of current density is not straightforward, as different works use different calculation methods. Regardless, both the current density by box volume and by component volume reported in this work show the MLB-PoL's great potential. Furthermore, not only is this converter well suited to deliver tens of amperes in a very compact form factor, but it can also be easily paralleled and scaled up for use in applications requiring hundreds of amperes.

Since all major components of the converter are packed into a small rectangular box, we are also able to directly compare with some of the best existing commercial power modules in this field. The results are summarized in Table 8.7. Although being the first proof-of-concept



(a) 48 V to 2.5 V (b) 48 V to 2.0 V (c) 48 V to 1.8 V

(d) 48 V to 1.5 V (e) 48 V to 1.2 V (f) 48 V to 1.0 V

Figure 8.7: Measured efficiency at various output voltages.

prototype without advanced packaging technologies, this work shows very comparable efficiency and current density performance. Note that the efficiency sweep of this work is obtained by slowly ramping up the load currents, and thus the switch resistance increases at heavy load due to higher switch temperature. In contrast, industry products are commonly tested under pulsed load conditions where the switch junction temperature is equal to the ambient temperature. Therefore, a higher efficiency number can be expected if the proposed converter is tested under the same industry procedure. We also note that the current design has not been optimized, as the commercial off-the-shelf inductors (maximum height of 0.315 inch) are much taller than the other components (maximum height of 0.126 inch). Further optimization of the magnetic components (e.g., customized coupled inductors with PCB windings) and advanced 3D packaging technologies (e.g., board cutouts for recessing inductors) could dramatically improve the power/current density.

8.4 Alternative Topology Variation

The multi-operating-phase concept can also be applied to transform other SC converters to hybrid SC converters with merged buck stage at the output. Here, we demonstrate one hybrid variation of the 6-to-1 cascaded series-parallel SC converter presented in Section 7.4. The circuit schematic of the proposed hybrid converter is shown in Fig. 8.9, and its key operating waveforms and equivalent circuits are shown in Fig. 8.10. The core structure of the SC stage remains the same as that of the cascaded series-parallel converter, with a 2-to-

Table 8.5: Summary of measured efficiency and power density results at various output voltages

Output voltage	Power stage efficiency	System efficiency (including driver loss)	Power density
2.5 V	Peak: 95.6% Full load: 92.1%	Peak: 95.0% Full load: 91.9%	494 W/in^3 196 W/in^2
2.0 V	Peak: 95.1% Full load: 91.3%	Peak: 94.3% Full load: 91.1%	395 W/in^3 157 W/in^2
1.8 V	Peak: 94.8% Full load: 90.9%	Peak: 94.0% Full load: 90.6%	356 W/in^3 141 W/in^2
1.5 V	Peak: 94.4% Full load: 89.9%	Peak: 93.3% Full load: 89.6%	296 W/in^3 118 W/in^2
1.2 V	Peak: 93.7% Full load: 88.1%	Peak: 92.4% Full load: 87.8%	237 W/in^3 94 W/in^2
1.0 V	Peak: 93.1% Full load: 86.8%	Peak: 91.5% Full load: 86.4%	198 W/in^3 79 W/in^2

Table 8.6: Comparison of this work and existing hybrid SC works

TABLE VI: Comparison of this work and existing hybrid SC works

Reference	Topology	Voltage ratio	Output current	Current Density	Efficiency	Notes
This Work	Hybrid 8-to-1 Multi-phase Doubler SC + two-phase Buck	48-to-1.5 V	65 A	198 A/in^3 (by box volume) 583 A/in^3 (by component volume)	System efficiency including driver loss: full load: 89.6% (I_{out}=32.5A/phase) heavy load: 91.4% (I_{out}=25A/phase) medium load: 92.4% (I_{out}=20A/phase) peak: 93.3% (I_{out}=13A/phase)	Total volume of the main power devices (switches, capacitors, inductors) is used for the "by component volume" current density calculation
LEGO PoL [13]	Hybrid 6-to-1 Dickson SC + 12-phase Buck	48-to-1.5 V	300 A	114 A/in^{3*} (by box volume)	Power stage efficiency:* full load: 87.7% (I_{out}=25A/phase) peak: 96.0% (I_{out}=4A/phase)	Current density is estimated with optimum vertical inductor stack-up
MIH [14]	Hybrid 4-to-1 Dickson SC + three-phase Buck	48-to-1.6 V	40 A	213 A/in^{3*} (by component volume)	Including *calculated* gate charge loss:* full load: 85.6% (I_{out}=13.3A/phase) peak: 93.9% (I_{out}=3.3A/phase)	Total component volume of main power devices (switches, capacitors, inductors) is used for density calculation
Crossed-coupled QSD Buck [15]	Hybrid 4-to-1 SC + two-phase Buck	48-to-1.5 V	40 A	100 A/in^3 (by component volume)	Power stage efficiency:* full load: 92.7% (I_{out}=20A/phase) peak: 95.1% (I_{out}=8A/phase)	The "by component volume" current density is estimated with the same method above

* According to direct correspondence with the author.

TABLE VII: Comparison of this work and existing commercial products

Reference	Topology	Voltage ratio	Output current	Current Density	Efficiency	Notes
This Work	Hybrid 8-to-1 Multi-phase Doubler SC + two-phase Buck	48-to-1.5 V	65 A	198 A/in^3 (by box volume) 583 A/in^3 (by component volume)	System efficiency including driver loss: full load: 86.4% peak: 91.5%	Total volume of the main power devices (switches, capacitors, inductors) is used for the "by component volume" current density calculation
ADI LTM4664 [8]	4-to-1 SC + two-phase buck	48-to-1 V	50 A	415 A/in^3	full load: 88.0% peak: 90.8%	Highly integrated power module
TI [9]	Transformer-based	48-to-1 V	50 A	N/A	full load: 87.7% peak: 90.7%	GaN FET
CHB1300PDB1EVM [10]	Transformer-based	48-to-1 V	70 A	167 A/in^3	Typical: 91%	Highly integrated power module, quad output voltage
bel power stamp [11]	Transformer-based	48-to-1 V	200 A	588 A/in^3	Typical: 90%	Highly integrated power module
Vicor PRM [31] + 2 VTMs [32]	Buck-Boost + Sine Amplitude Converter	fixed	200 A	588 A/in^3	Typical: 90%	Highly integrated power module

1 front-end stage followed by a 3-to-1 series-parallel stage, and therefore a total conversion ratio of 6-to-1 at the SC stage. Besides the original inductor (L_3 in Fig. 8.9) that is in series combination with all flying capacitors, two additional inductors are augmented to the positive terminal of each flying capacitor in the series-parallel stage. This way, C_2 and C_3 are softly discharged by L_1 and L_2 during the parallel mode, respectively. In order to have balanced and interleaved inductor currents, their discharging time are split to 4 phases 2 and 5 and 3 phases 3 and 6, respectively. Owing to this multi-operating phase control strategy, the high voltage components (Q_1–Q_4 and C_1) only need to operate at half the frequency of the other components. Compared to the MLB converter, even though the conversion ratio of the SC stage is only doubled from 3-to-1 to 6-to-1, the number of inductors increases from two to three. Besides, the MLB converter employs multiple operating phases to achieve 8-to-1 conversion ratio, but the SC phases increase from two to four.

but it can also be easily paralleled and scaled up for use in applications requiring more amperes.

Since all major components of the converter are packed into a small rectangular box, we are also able to directly compare with some of the best existing commercial power modules in this field. Although being the first proof-of-concept prototype without advanced packaging technologies, this work shows very comparable efficiency and current density performance. Note that the efficiency sweep of this work is

number of components. This high SC conversion ratio can reduce the inductor volt-second stress of the following buck stage. Moreover, an inductor frequency multiplication effect is able to further reduce the inductor size without increasing the switching frequency of the SC stage. A 48 V to 2.5-1.0 V converter prototype with 65 A output current was built and tested. At 48 V to 2 V, the prototype achieved

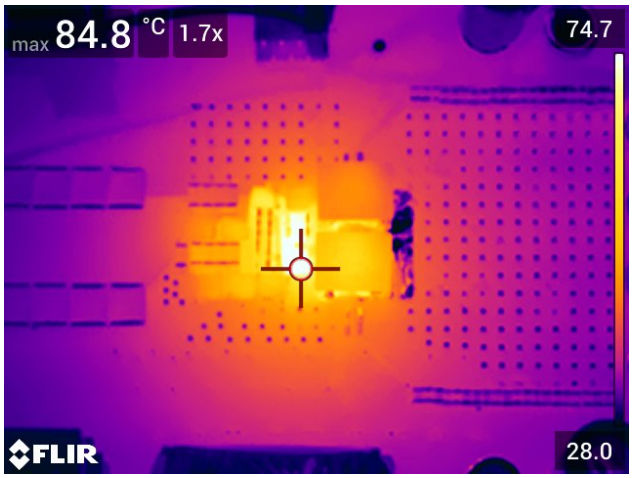


Figure 8.8: Thermal performance at equilibrium with 110 CFM fan cooling only ($V_{\text{out}} = 2.0$ V, $I_{\text{out}} = 65$ A).

Table 8.7: Comparison of this work and existing commercial products

Reference	Topology	Voltage ratio	Output current	Current Density	System Efficiency	Notes
This Work	Hybrid 8-to-1 SC + two-phase Buck	48-to-1 V	65 A	198 A/in^3	full load: 86.4% 50 A: 88.7% peak: 91.5%	
ADI LTM4664 [109]	4-to-1 SC + two-phase buck	48-to-1 V	50 A	415 A/in^3	full load: 88.0% peak: 90.8%	Highly integrated power module
TI [110] LMG5200POLEVM	Transformer-based	48-to-1 V	50 A	N/A	full load: 87.7% peak: 90.7%	GaN FET
bel power stamp [111]	Transformer-based	48-to-1 V	70 A	167 A/in^3	Typical: 91%	Highly integrated power module, fixed output voltage
Vicor PRM [150] +2*VTM [151]	Buck-Boost + Sine Amplitude Converter	48-to-1 V	200 A	588 A/in^3	Typical: 90%	Highly integrated power module

to three, leading to higher output current capability. Given that this topology has a very similar component number (one more switch, one more inductor) to the MLB converter, an even higher power density could be achieved.

8.5 Chapter Summary

This chapter presents a new hybrid topology with Multi-Level Binary (MLB) voltages on the flying capacitors that can simultaneously achieve high efficiency and power density for direct 48 V to PoL applications. The proposed MLB-PoL converter employs multiple operating

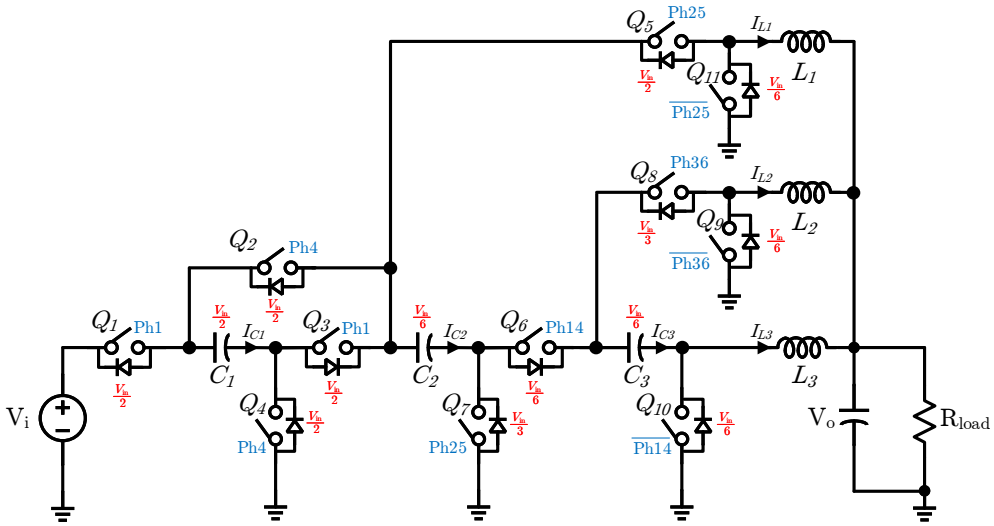
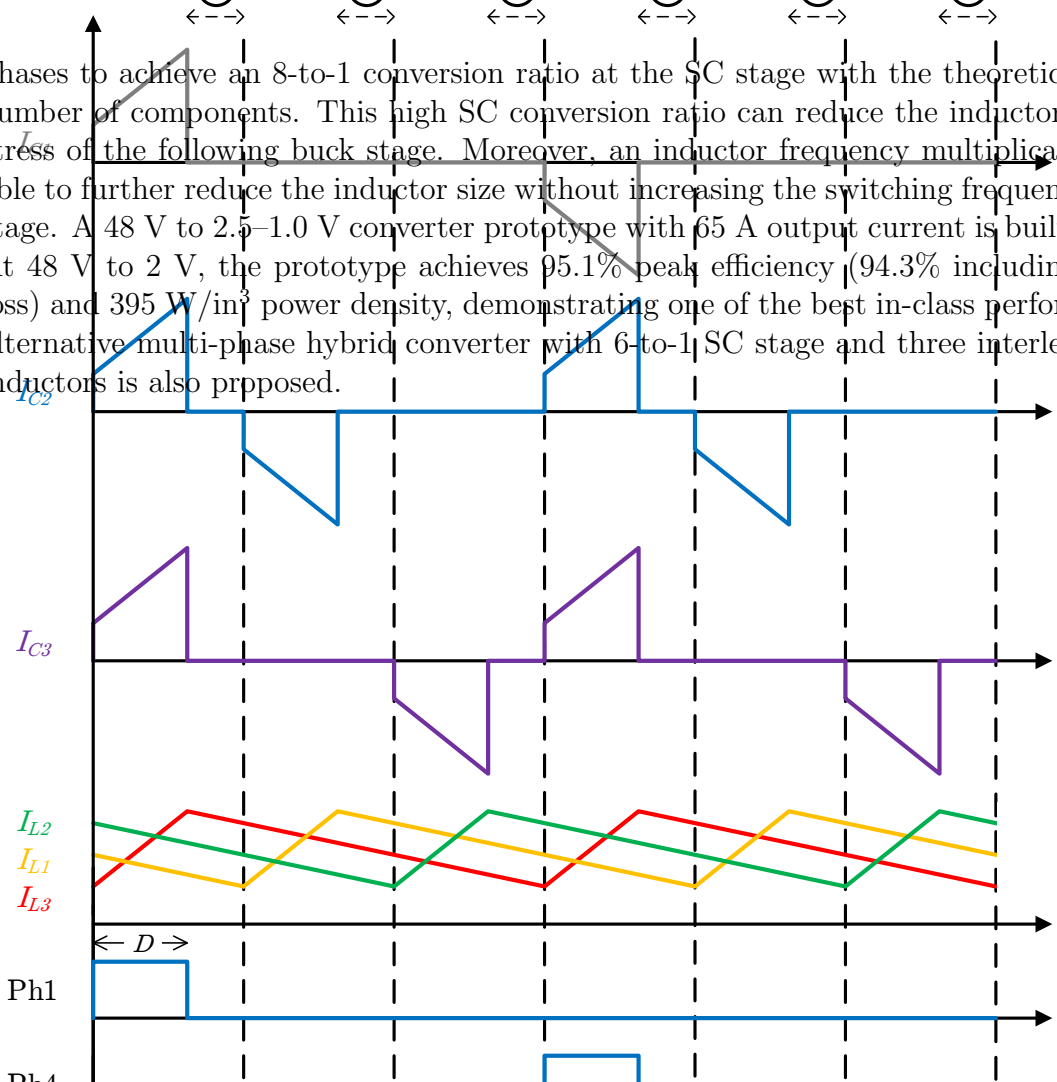
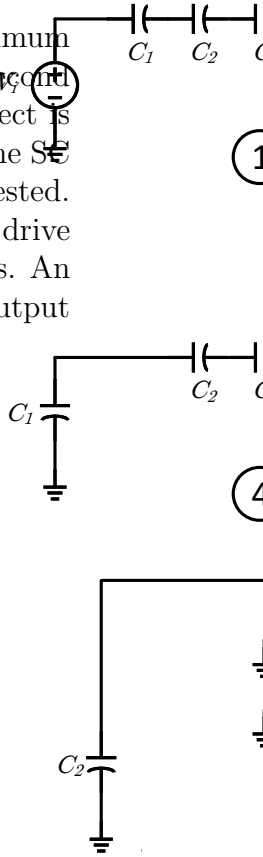


Figure 8.9: Schematic drawing of a proposed multi-phase hybrid converter with a 6-to-1 SC stage and three interleaved output inductors. The device voltage ratings are labeled in red and the operating phases of the switches are labeled in blue.

phases to achieve an 8-to-1 conversion ratio at the SC stage with the theoretical minimum number of components. This high SC conversion ratio can reduce the inductor volt-second stress of the following buck stage. Moreover, an inductor frequency multiplication effect is able to further reduce the inductor size without increasing the switching frequency of the SC stage. A 48 V to 2.5–1.0 V converter prototype with 65 A output current is built and tested. At 48 V to 2 V, the prototype achieves 95.1% peak efficiency (94.3% including gate drive loss) and 395 W/in^3 power density, demonstrating one of the best in-class performances. An alternative multi-phase hybrid converter with 6-to-1 SC stage and three interleaved output inductors is also prpposed.





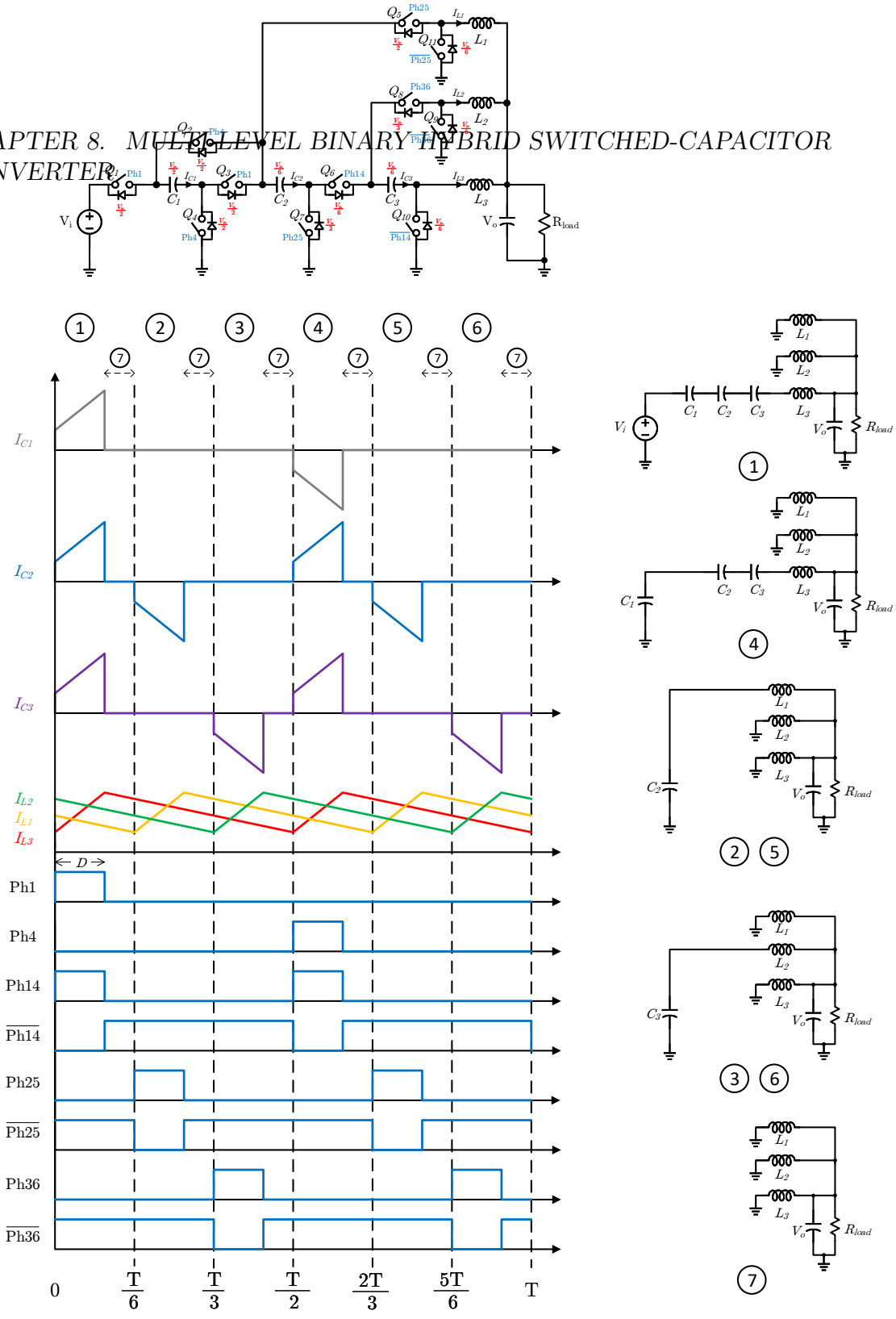


Figure 8.10: Voltage, current, PWM waveforms, and equivalent circuit models of the proposed hybrid SC converter with a 6-to-1 SC stage.

Chapter 9

Future Work

It should be recognized that hybrid and resonant switched-capacitor converter design remains an emerging topic in power electronics, with limited industry penetration to date. There is more theoretical work to complete and more practical implementation challenges to address. This chapter provides an outlook for hybrid and resonant SC converters and discusses some possible future work.

Performance Wishlist

In order to outperform LLC converters in high-performance fixed-ratio conversions, ReSC converters need to demonstrate more favorable characteristics in the following areas:

- High conversion ratio. In existing discrete implementations, the performance advantage of ReSC converters diminishes with respect to the conversion ratio. At a 4-to-1 ratio, the cascaded resonant converter in Chapter 6 has efficiency and power density advantages over the latest high-frequency LLC converter with a highly optimized magnetic structure [122]. However, at an 8-to-1 ratio, the performance advantages of ReSC converters (such as the multi-resonant doubler converter in Chapter 7) is greatly reduced. For applications with even higher conversion ratios, such as the direct 48-to-1 V step-down for data center applications [112], ReSC converters cannot yet compete with transformer-based converters.

- Flat efficiency curve and heavy load performance. With similar power and voltage ratings, ReSC converters usually have better light-load efficiency than LLC converters, owing to less magnetic loss. However, their efficiency usually peaks at lighter loads compared to LLC converters, and then starts to drop at a faster rate, especially when the conversion ratio is high. This is because the switch count and the associated output impedance of ReSC converters typically increases proportionally with respect to conversion ratio, whereas the circuit structure and switch count of LLC converters remain unchanged. As a result, ReSC converters cannot achieve a low output output impedance as easily as LLC converters at high conversion ratios.

- High output current. In LLC converters, the current and power rating can be easily scaled up by splitting the output current into multiple paralleled stages at the secondary side of the transformer. In comparison, as discussed in Section 6.6, because of the high circuit complexity, it is challenging for ReSC converters to achieve high conversion ratio and high output current simultaneously. To address this problem, strategic interleaving and cascading operations can be applied on selective topologies with simple basic structures.

- High operating frequency. Owing to the use of high energy density capacitors, ReSC converters can achieve high power density at a relatively low switching frequency. Most existing high-performance discrete implementations operate in the range of 50 to 350 kHz. To date, the ability of operating ReSC converters efficiently at higher frequencies has not been widely demonstrated. In fact, some frequency related loss mechanisms in practical implementations of SC converters have not been fully explored and understood. Through an experiment that was not included in the dissertation, an unclear frequency-dependent loss was discovered. A 2-to-1 SC converter prototype (with 25 V rated discrete MOSFETs) operating at 4-to-2 V exhibited a significant power loss increase with respect to switching frequency ($P_{\text{loss,400kHz}} \approx 3P_{\text{loss,100kHz}}$), which was not expected at the heavy load condition tested, where conduction loss is usually dominant, especially when the voltage level and the associated switching loss of the switches are low.

- Full soft switching. In order to operate at a high frequency (in the MHz range) efficiently, it is essential to achieve full zero voltage switching and zero current switching on all switches, across the full load range. Among existing ReSC converters, the cascaded resonant converter and the Dickson converter can achieve full soft-switching on all switches, but the condition is load-dependent. For the multi-phase ReSC converters and the series-parallel converter, the single augmenting inductor at the output node is incapable of soft charging/discharging all switches, owing to the complex internal charge flow paths.

- New topologies with merged magnetic structures. The increasing use of capacitors in energy transfer is not meant to completely eliminate magnetic components. On the contrary, the hybrid approach itself demonstrates that a good combination of capacitors and inductors can yield a better overall performance. In addition to merging capacitors with inductors or buck converters, it is also worthwhile to explore the opportunity for merging capacitors with transformers, which may have potential benefits for applications with very high conversion ratios or isolation requirements. Some early works in this field include the MultiTrack architecture [79] and the multilevel structure with merged transformer-based current doublers [152].

Practical Implementation Challenges

- Start-up circuit. When the input voltage of the hybrid resonant SC converter is not well controlled, a dedicated start-up circuit is needed. Alternatively, the switch connected to the input may need to be rated for a higher-than-nominal voltage to accommodate the worst-case scenario. This may penalize different topologies differently. For instance, the first switch in a series-parallel converter needs to block a high voltage regardless, therefore the penalty considering the start-up condition is relatively mild. In contrast, the first switch in a Dickson converter only blocks V_{out} during normal operation, but it has to be rated for V_{in} when the start-up condition needs to be considered. In applications where the input voltage can be slowly ramped up to the rated voltage, no additional start-up circuit is needed. For instance, in a cascaded two-stage architecture, the previous stage can serve as a soft-start circuit for the following stage.

- PCB layout. The complex circuit structure of hybrid and resonant SC converters complicates PCB design, which in return directly impacts the performance of the converter. Therefore, the ease of layout should be considered when comparing different topologies. A good PCB layout should have short interconnect traces (low parasitic resistance and inductance) and small switching node area (low parasitic switching loss), while being compact and power dense. The cascaded resonant converter is found to have unique advantages in terms of PCB design.

- Gate drive loss. As discussed in Chapter 5, hybrid and resonant SC converters have a large number of switches and the associated gate drive loss contributes a non-negligible portion to the overall loss. Therefore, the gate drive circuit should be designed to be as efficient as possible, and the gate drive loss should be included in the overall efficiency measurement.

- Capacitor balancing. This remains a crucial challenge for hybrid SC converters, especially for FCML converters. Many benefits of such topologies rely on the reduced voltage stress on the switches, and it is of great importance to ensure the voltages of flying capacitors are balanced and close to their nominal values.

- Input and output capacitance. For ReSC converters, the input and output capacitors participate in the resonant operation. Consequently, their values may have a direct impact on the conversion efficiency. There is a great value in analyzing the effects of input and output capacitance on the output impedance of ReSC converters, both theoretically and experimentally.

Devices, Integration, and Packaging

While this dissertation mainly studies hybrid and resonant SC converters from a topological perspective, the other aspects in power converter designs should not be neglected. In

particular, device customization, power train integration, and advanced packaging have the potential to further improve the performance of hybrid and resonant SC converters.

- Discrete low-voltage power MOSFETs. For low-voltage high-current applications such as 48 V data center power delivery, the switch blocking voltage of many hybrid resonant SC converters can be as low as 6–10 V. However, the minimum rating of existing discrete power MOSFETs with the requisite on-resistance value is 25 V. If lower voltage rated devices are available, the theoretical performance benefits of these topologies can be better realized.

- Customized capacitor packaging. In practical implementations, multiple MLCCs may need to be paralleled to get the desired capacitance value. With standard assembly technology, these MLCCs have to be spaced apart in order to meet manufacturing component clearance tolerances, and they cannot be stacked in multiple layers. With customized capacitor arrays (a long row of capacitors packaged together by manufacturers), the reliability and power density of the converters can be greatly improved.

- FET and driver integration. From an industry perspective, a major challenge of these topologies is the complex structure and the large number of components, which translates to cost and reliability concerns. This problem can be addressed through better integration of the power device and the associated gate drive circuit. The LTC7820 from ADI [8] integrates four series-connected gate drivers on a single chip and greatly simplifies the design of the 2-to-1 SC converter. The EPC2152 [153] presents a monolithic half-bridge module with integrated power devices, gate drivers, level shifter, and bootstrap circuit. Through further efforts to improve integration, the design of hybrid and resonant SC converters can be expected to be as easy as that of buck and boost converters today.

- Magnetic components. For the hardware prototypes presented in this dissertation, commercial off-the-shelf inductors are used for ease of design. However, they have become the bottleneck of the entire system: the output current rating is usually limited by the inductor saturation current and the power density is limited by the height/volume of the inductor. For fixed-ratio ReSC converters, customized one-turn inductor shows great promise [154]. For regulated hybrid SC converters, coupled indcutors may provide dramatic performance improvement [155]. In addition, innovative structures such as the merged LC resonator [156] and the piezoelectric resonator [157] maybe worth further attention.

- Advanced packaging. Packaging not only determines the power density, but also directly impacts the electrical and thermal performance of the converter. Most existing hybrid and resonant SC works are board-level designs. It would be interesting to see more demonstrations with advanced power module designs. Recently, the concept of vertical power delivery has emerged for very high current ASICs applications. Ref [158]

demonstrates a 3-D stacking concept for hybrid SC converters with good power density performance.

Chapter 10

Conclusions

This dissertation demonstrates the great performance potential of hybrid and resonant switched-capacitor power converters, through both theoretical analysis and experimental verification. With augmenting inductor(s), the capacitor charge sharing loss in SC converters can be eliminated, thereby increasing the energy utilization factor of the capacitors without sacrificing the efficiency performance. When operating in resonant mode, ReSC converters can behave as a dc transformer and achieve very efficient and power dense fixed-ratio conversion. When operating in PWM regulated mode, hybrid SC converters can achieve better performance than conventional buck and boost converters, thanks to the reduced inductance requirement and better utilization of the switches.

In order to evaluate the advantages of passive component utilization of hybrid resonant SC converters, a passive component modeling method is proposed, by fundamentally analyzing the reactive power processed by the passive components. It is shown that the total passive component volume can be expressed as a function of flying capacitor voltage ripple, and the optimum inductor and capacitor allocation that minimizes the total volume is dependent on their relative energy density and topology-dependent parameters. The analysis and the associated experimental results also showcase that a 2-to-1 ReSC converter can use significantly less passive volume than conventional SC and buck converters for the same power conversion, while maintaining the best efficiency performance. In addition, by combining the proposed passive utilization metric with the switch utilization metric (switch VA rating), a framework to compare the relative performances of different ReSC topologies is created.

To realize the excellent performance potential of hybrid and resonant SC converters, two important practical implementation challenges are investigated, and corresponding mitigation strategies are presented. The first is flying capacitor voltage balancing, which is particularly challenging for flying capacitor multilevel converters. It is found that the source impedance and the associated input capacitance can have a drastic impact on capacitor balancing, and an FCML converter with an even number of levels inherently has stronger immunity to such disturbance than a converter with an odd number of levels.

The second challenge is in regard to powering the large number of floating gate drivers

in these topologies. To make the gate drive power suppy circut more compact and efficient, five circuit techniques are presented: bootstrap at deadtime, cascaded bootstrap with LDO, double charge pump, gate-driven charge pump, and synchronous bootstrap. By leveraging the inherent properties of multilevel converters, these methods can overcome the limitation of the conventional bootstrap method (i.e., the diode forward voltage drop) and make it possible to transfer ground-referenced power to all of the floating switches for any FCML or hybrid SC converters.

The excellent performance of hybrid and resonant SC converters is also demonstrated by three hardware prototypes for 48 V data center power delivery applications. The first is a 48-to-12 V cascaded resonant converter. By cascading two standard 2-to-1 ReSC converters, a 4-to-1 conversion ratio can be achieved, while keeping the same simple operating principle and full zero voltage switching capability. To reduce the size of the interstage decoupling capacitor, a two-phase interleaving strategy is adopted. The prototype achieves 99.0% peak efficiency (with gate drive loss included) and 2500 W/in^3 power density.

In order to achieve higher conversion ratios with manageable circuit complexity, the concept of multiple-operating-phase is applied. Compared to ReSC converters with two operating phases, the proposed multi-resonant SC converters can achieve the same conversion ratio with significantly fewer switches and capacitors. For 48-to-8 V conversion, a cascaded series-parallel topology is proposed, and its prototype achieves 98.5% peak efficiency (with gate drive loss included) and 2230 W/in^3 power density. For 48-to-6 V conversion, a multi-resonant-doubler converter is developed, with 98.0% peak efficiency (with gate drive loss included) and 1675 W/in^3 power density.

For direct 48 V to point-of-load conversion, a regulated hybrid SC topology — the multi-level binary (MLB) converter, is presented. Owing to the multi-phase operation, the MLB converter can achieve 8-to-1 conversion ratio at its SC stage, which is the highest among all existing hybrid topologies. The two-phase interleaved inductors at the output buck stage have balanced currents due to an inherent balancing mechanism. Moreover, the inductors benefit from a frequency multiplication effect similar to that in FCML covnerters, which results in a higher effective inductor frequency without the need for increasing the operating frequency of all other components. A 48 V to 2.5–1.0 V prototype with 65 A output current is built and tested. At 48 V to 2 V, the prototype achieves 94.3% peak efficiency (with gate drive loss included), and 395 W/in^3 power density. All these hardware prototypes achieve the best in-class efficiency and power density simultaneously, reflecting the great potential of hybrid and resonant SC converters for future power conversion systems.

Last but not least, some possible future works are discussed. With more research into device customization, power train integration, and advanced packaging, the cost and reliability concerns of hybrid resonant SC converters can be alleviated. Combined with increased research into exploiting the topological potential and addressing the practical implementation challenges, a broader adoption of hybrid and resonant SC converters by the power electronics society can be expected.

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