Design and Fabrication of VCSELs for 3D Sensing

Kevin Cook

Electrical Engineering and Computer Sciences
University of California, Berkeley

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Design and Fabrication of VCSELs for 3D Sensing

By

Kevin Taylor Cook

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Abstract

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Vertical-cavity surface-emitting lasers (VCSELs) are critical components in many optical systems. They already drive the transmission of data in massive datacenters and supercomputers, and they are becoming the state of the art in 3D sensing systems that allow computers to perceive the world more like humans. These systems have important applications in medicine, autonomous vehicles, facial recognition, and gesture detection. VCSELs have shown the promise of improving resolution while decreasing module cost due to their extremely scalable fabrication process.

The first 3D sensing mechanisms that VCSELs promise to improve are swept-source optical coherence tomography and frequency-modulated continuous-wave LIDAR. These techniques use a wavelength tunable source to probe the distance to reflectors in the beam path. The resolution of these systems is limited by the fractional tuning range of the source. This work presents a method to increase the fractional tuning range of tunable VCSELs by coupling the energy in the cavity out of the gain medium and into the tuning gap. The design is demonstrated experimentally to increase the tuning range by a factor of two over a comparable tunable VCSEL.

The second family of 3D sensing mechanisms demand high-power, high-efficiency VCSEL arrays to illuminate an entire scene to identify gestures and faces. The final chapter of this dissertation describes a novel fabrication method leveraging the oxidation of AlGaAs to form a high-contrast grating (HCG) reflector in a VCSEL array. The process is scaled from a proof of concept, to the first high-efficiency HCG VCSEL, and finally to an array of HCG VCSELs. The introduction of an HCG to the device reduces the fabrication cost and introduces polarization control to the array, creating a platform for new possibilities in 3D sensing.

To my family.

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Acknowledgements

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1 Introduction

1.1 Vertical-Cavity Surface-Emitting Lasers

Vertical-cavity surface-emitting lasers (VCSELs) were first demonstrated in 1979[1], brought to room temperature in 1988 [2], and integrated with practical electrical pumping in 1989 [3]. They have since become one of the most widely deployed types of lasers due to their high performance and low cost, driving the thousands of short-reach optical interconnects in datacenters [4]. In the past decade, a new market for VCSELs has emerged: 3-dimensional sensing. Since computational resources have caught up to the computer vision algorithms developed decades ago, 3D sensing is becoming ubiquitous, with systems deployed in driverless cars, factories, doctor's offices, and even cell phones.

VCSELs have been demonstrated at a variety of wavelengths for many applications. For telecommunications, VCSELs are produced at wavelengths of 850 nm (GaAs/AlGaAs) [5], 1300 nm (InGaAsP/InP) [6], and 1550 nm (InGaAsP/InP) [7], which correspond to dips in the absorption spectrum of water. To increase the bandwidth of short-reach interconnects, short wavelength division multiplexing (SWDM) is being designed to use VCSELs at a variety of wavelengths between 800 nm at 1000 nm [8]. For 3D sensing, the wavelengths of interest include 940 nm for facial recognition and 1060 nm for ophthalmic optical coherence tomography. Illumination at 940 nm is popular for imaging because it is fully invisible and corresponds to a dip in the solar spectrum [9]. Tunable VCSELs centered at 1060 nm or 1300 nm are used for OCT to avoid water absorption in live tissue.

In contrast to an edge-emitting semiconductor laser, which has a cavity defined by an in-plane waveguide and cleaved facet mirrors, a VCSEL cavity is defined by a stack of layers grown on a semiconductor substrate. The most fundamental difference between the two types of lasers is the direction of light propagation and emission: the light in an edge-emitting laser propagates along the plane of the substrate, while the light in a VCSEL propagates vertically through the cavity. This difference gives several practical benefits to the VCSEL over an edge-emitting laser. The first benefit comes during the manufacturing process: a VCSEL can be tested at the wafer level prior to dicing and packaging each device. This allows VCSEL wafers and even individual devices to be binned for different applications, reducing the overall cost of a VCSEL. In contrast, the edge-emitting laser will not function properly until the wafer is cleaved, which requires extra handling of defective devices. The second practical benefit of the VCSEL is the shape of its emission. Since the lateral waveguide structure is symmetrical (typically circular), the far field angle of the emitted light is also circular. Waveguides used in edge-emitting lasers are typically asymmetrical to promote the transverse-electric mode for lower threshold, which causes an elongated emission from the facet. The emission shape has a great impact on optical fiber coupling. VCSELs can be butt-coupled to multimode optical fibers, while edge-emitting lasers must use a cylindrical lens to focus the light into an acceptable shape. The emission shape is also important for 3D sensing, where the emission from each laser must be discernable from its neighbors. A third advantage for VCSELs is the process for implementing laser arrays. To create an array of edge-emitting lasers, laser diodes must be stacked on top of and beside one another

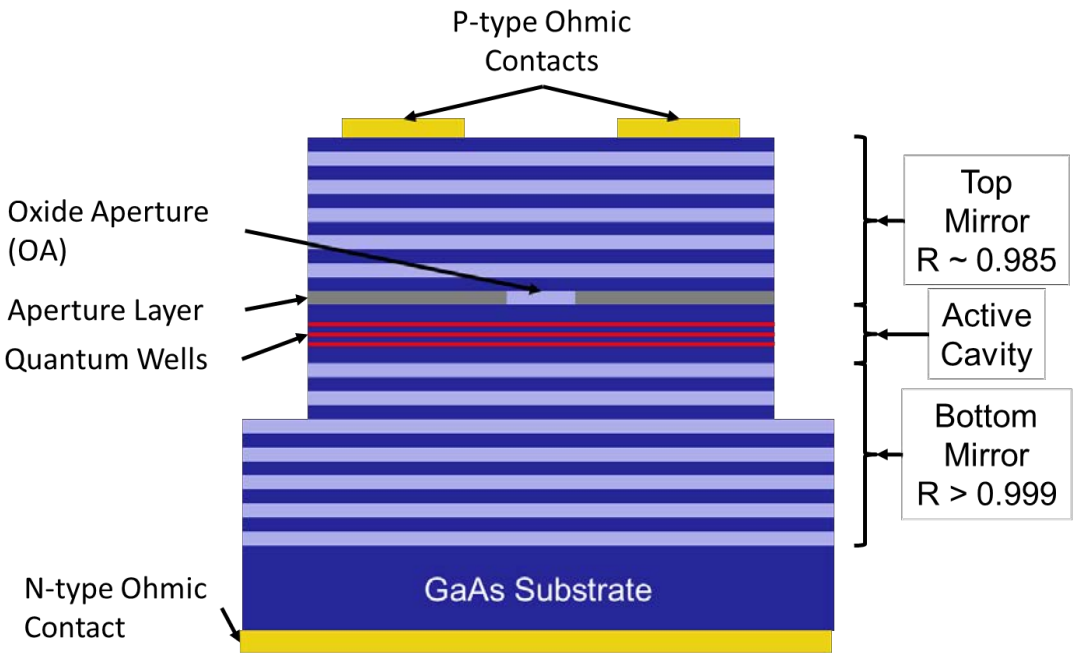


Figure 1.1. Structure of a typical VCSEL. The optical cavity is defined by the 1λ active cavity terminated on either end by a distributed Bragg reflector (DBR). Since the cavity is so short, the mirrors must be extremely reflective. Current injection is provided by p-type contacts on the top of the VCSEL and a large area n-type contact covering the back of the chip. The oxide aperture simultaneously concentrates the injected current and optical field into a small area to produce a high quantum well gain. In the optical path at the center of the VCSEL, a darker shade of blue corresponds to a higher refractive index.

by packaging. This requires appropriate bonding methods and the sequential handling of each individual laser. In contrast, arbitrary arrays of VCSELs can be produced with the same process used for single VCSELs. The array pattern is only determined by the layout of the masks used to produce the VCSEL array.

A typical VCSEL, illustrated in Figure 1.1, is composed of a stack of hundreds of epitaxially grown layers of III-V materials. At the center of the VCSEL is a multiple quantum well gain structure, encased in a cavity that is a single wavelength (1λ) long. This extremely short cavity is placed between two distributed Bragg reflectors (DBRs) with reflectances that exceed 99% to provide optical feedback into the active cavity. In order to facilitate electrical pumping, one of the semiconductor mirrors is doped p-type, and the other n-type, forming a p-n junction across the active cavity.

When the VCSEL diode is forward biased, electrons and holes recombine in the quantum wells, producing light through spontaneous emission. As forward current increases, the number of electrons and holes present in the conduction and valance bands increase, causing an inversion of charge carriers. The inverted carriers enable stimulated emission, producing gain. Once enough gain is provided by the quantum wells, the oscillation of the resonant cavity mode will become self-sustaining, and the device will produce a coherent beam of light out of the plane of the

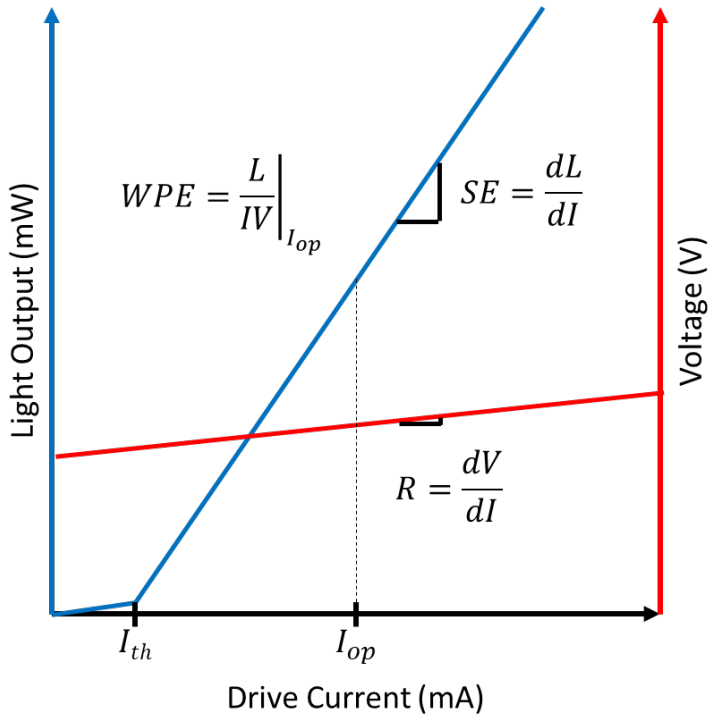


Figure 1.2. LIV plot for a VCSEL. The light output is low until the device is supplied with the threshold current, I_{th}. Beyond this point, the light output increases at a rate known as the slope efficiency (SE) until thermal rollover (not shown). The wall plug efficiency (WPE) is the complete power efficiency of the device. The electrical behavior of a VCSEL is the same as a diode, which can be represented by a turn on voltage and a series resistance.

semiconductor. In the light versus current characteristic of a VCSEL, this corresponds to a sudden change of slope at the threshold current I_{th} of the device. Above threshold, the light output increases with a slope known as the slope efficiency (SE) of the device. The overall power efficiency – the output power divided by the input electrical power at a given operating current – is known as the wall plug efficiency (WPE) or power conversion efficiency (PCE). The wall-plug efficiency is a powerful metric because it incorporates both the electrical and optical performance of the VCSEL.

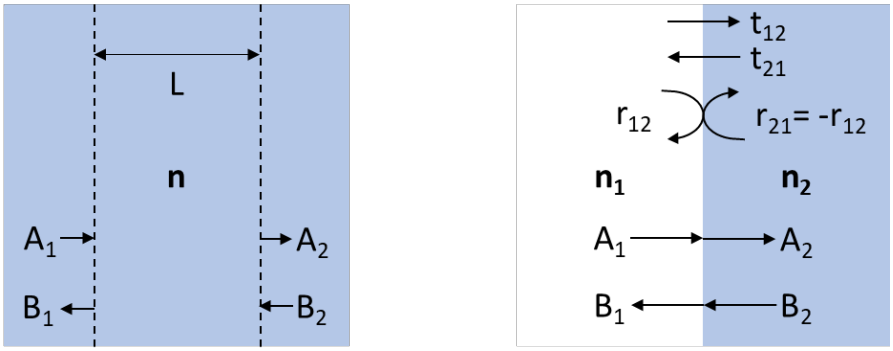


Figure 1.3. The transfer matrix method can model the optical structure of a VCSEL using the multiplication of two basic units. The first is the propagation through a region with refractive index n and length L. The transfer matrix is constructed with phase accumulation according to the real part of the refractive index and attenuation according to the imaginary part. The second elemental matrix represents the interface between two different materials. The reflection and transmission coefficients are defined by Fresnel's equations.

1.2 Optical Analysis of VCSEL Structures

The reflection coefficients for the top and bottom mirrors of a VCSEL must be calculated using the thickness and refractive index of each layer in the VCSEL. The transfer matrix formalism, described in [10] and reviewed in this section, is useful for this task.

The propagation of an electromagnetic field through a material is represented with *1.1*, where *k* is the propagation constant of the light within the material.

$$E(z) = E(0)e^{jkz} \tag{1.1}$$

If there is loss or gain present in the material, due to absorption or spontaneous emission for example, *k* will take a complex value. This results in the introduction of a decay or growth term in the propagation equation.

$$k = \frac{2\pi(n + j\kappa)}{\lambda} = \frac{2\pi n}{\lambda} + j\frac{2\pi\kappa}{\lambda} = \beta + j\alpha \tag{1.2}$$

$$E(z) = E(0)e^{j\beta z}e^{-\alpha z} \tag{1.3}$$

The behavior of light incident on an interface can be described by the Fresnel coefficients *r* and *t*. For surface-normal incidence, as is the case in a VCSEL, these coefficients are given by the following equations.

$$r_{12} = \frac{n_1 - n_2}{n_1 + n_2} \tag{1.4}$$

$$t_{12} = \frac{2n_1}{n_1 + n_2} \tag{1.5}$$

Note that the expression for the reflected wave amplitude will be negative if $n_2 > n_1$. This corresponds to a phase shift of π radians. When the wave is travelling in the opposite direction – from n_2 to n_1 – the sign of the reflection coefficient is flipped.

The transfer matrix relates the input and output ports of an arbitrary optical system by *1.6*, where A and B represent the forward-travelling and backward-travelling waves at the input and output ports of the system.

$$\begin{bmatrix} A_1 \\ B_1 \end{bmatrix} = \boldsymbol{T} \begin{bmatrix} A_2 \\ B_2 \end{bmatrix} \quad 1.6$$

The entries in a transfer matrix can be related to the complex transmission and reflection coefficients of the optical system by solving the matrix equations for the system. These transfer matrices for interfaces between materials and propagation through a length of material are given below.

$$\boldsymbol{T}_{interface} = \frac{1}{t_{12}} \begin{bmatrix} 1 & r_{12} \\ r_{12} & 1 \end{bmatrix} \quad 1.7$$

$$\boldsymbol{T}_{propagation} = \begin{bmatrix} e^{ikL} & 0 \\ 0 & e^{-ikL} \end{bmatrix} \quad 1.8$$

The true power of the transfer matrix method lies in combining simple elements to build a complex system. For example, a single DBR pair can be expressed by the multiplication of four matrices, and a 15 pair DBR can be expressed as the resulting matrix raised to the power of 15.

$$\boldsymbol{T_{DBR\,pair} = T_{int1} T_{prop1} T_{int2} T_{prop2}} \quad 1.9$$

$$\boldsymbol{T_{DBR} = T_{DBR\,pair}^{15}} \quad 1.10$$

Once the full structure is multiplied into one matrix, the amplitude transmittance and reflectance can be found by limiting the optical system to a single input (A_1 or B_2) and solving for the desired ratio.

$$t_{12} = \left.\frac{A_2}{A_1}\right|_{B_2=0} = \frac{1}{T_{11}} \quad 1.11$$

$$r_{12} = \left.\frac{B_1}{A_1}\right|_{B_2=0} = \frac{T_{21}}{T_{11}} \quad 1.12$$

$$t_{21} = \left.\frac{B_1}{B_2}\right|_{A_1=0} = \frac{det(T)}{T_{11}} \quad 1.13$$

$$r_{21} = \left.\frac{A_2}{B_2}\right|_{A_1=0} = -\frac{T_{12}}{T_{11}} \quad 1.14$$

The transfer matrix method is applied to VCSEL analysis by breaking the cavity into two analytical blocks somewhere near the center of the resonant cavity. In this work, the cavity is broken just below the interface at the top of the active cavity. Over a range of wavelengths, the reflection coefficient r_{12} is calculated for the top half and the bottom half of the cavity. The

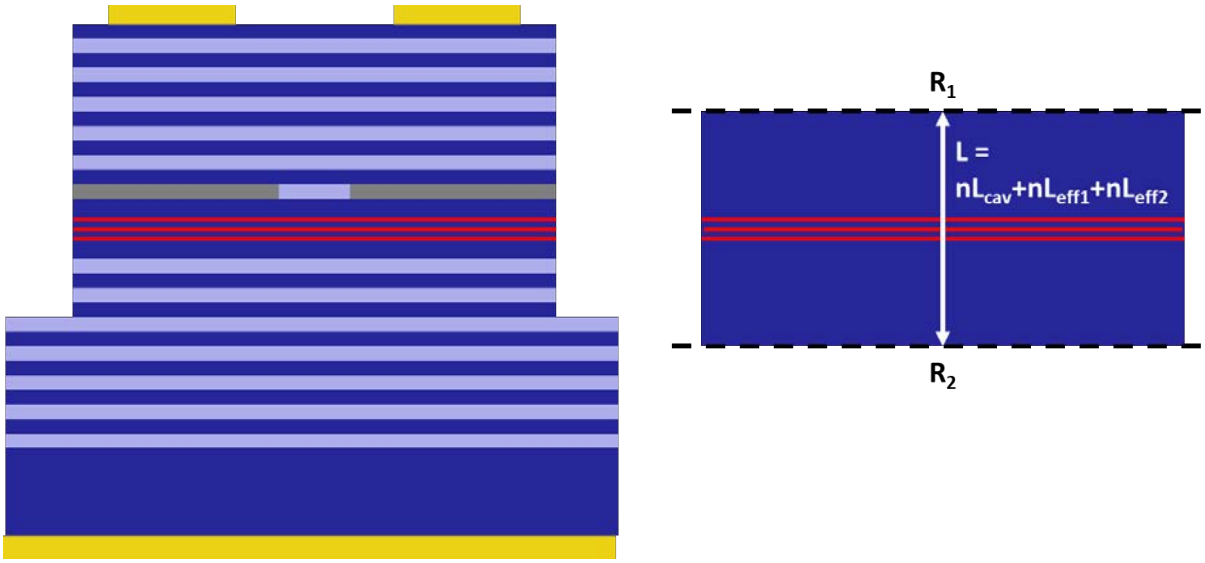


Figure 1.4. VCSEL structure modeled as a Fabry-Perot cavity. The VCSEL structure shown on the left can be analyzed as the FP cavity shown on the right. The DBRs are replaced by planar reflectors with an effective length that corresponds to the penetration depth of the optical mode into each reflector. The refractive index of the active cavity is used to fill the space between the cavity and the planar reflector.

analysis of resonant wavelength and other parameters is performed in analogy to a Fabry-Perot (FP) cavity.

The distributed reflectors in a VCSEL can be abstracted into planar reflectors with reflectance R that are a length L_{eff} away from the first interface of the DBR, as shown in Figure 1.4. When this abstraction is made, the cavity becomes an FP cavity. An FP cavity will resonate when the phase accumulated by a round trip through the cavity is a multiple m of 2π. For the simplified FP cavity with planar mirrors, the resonant wavelength is easily calculated using *1.16*.

$$\phi = 2\pi m = 2\beta L \tag{1.15}$$

$$\lambda_r = \frac{2nL}{m} \tag{1.16}$$

The spacing between adjacent FP modes is known as the free spectral range (FSR). At large modal numbers, the FSR is often approximated to be a constant. With modal numbers under 20, which are common in VCSEL cavities, the spacing between each mode differs too much for a good approximation.

In order to find the resonant wavelength for a VCSEL, the reflection phase accumulated in each mirror can be calculated numerically and summed to find the wavelength that satisfies the round-trip phase condition.

$$\Phi_{RT}(\lambda_r) = \angle r_{top}(\lambda_r) + \angle r_{bottom}(\lambda_r) \tag{1.17}$$

Once the resonant wavelength is determined and the phase is known at each wavelength, the effective length of the cavity can be determined by taking the derivative of *1.17*

$$L_{eff} = \frac{1}{2}\frac{d\phi}{d\beta} = -\frac{\lambda_r^2}{4\pi n_g}\frac{\partial}{\partial\lambda}\left[\angle r_{top}(\lambda) + \angle r_{bottom}(\lambda)\right]\Big|_{\lambda=\lambda_r} \quad 1.18$$

In order to form a laser, gain must be added to the FP cavity. The threshold material gain, g_{th}, is the amount of gain required to sustain laser oscillation in the cavity. For a simple FP cavity, the change of intensity after a round trip through the cavity is given by *1.19*, where g and α_i represent the gain and loss of photons per unit length within the cavity, and the confinement factor Γ represents the fraction of the standing wave which overlaps with the gain material.

$$\frac{I_1}{I_0} = R_1 R_2 e^{2L(\Gamma g - \langle\alpha_i\rangle)} \quad 1.19$$

When the laser is above threshold, this quantity is equal to unity. The threshold material gain can be determined by rearranging this equation.

$$g_{th} = \frac{\langle\alpha_i\rangle}{\Gamma} + \frac{1}{2\Gamma L}\ln\left(\frac{1}{R_1 R_2}\right) = \frac{\langle\alpha_i\rangle + \alpha_m}{\Gamma} \quad 1.20$$

The first term of this equation represents the modal internal loss of the laser. It incorporates loss mechanisms such as band-edge absorption, free-carrier absorption, and scattering loss due to epilayer surface roughness. The second term of this equation represents the loss of photons through the mirrors at the ends of the cavity, expressed as a distributed loss term.

In a VCSEL, the axial confinement factor and cavity length are not obvious. Instead of using these factors as input parameters to solve for g_{th}, it is simpler to use g_{th} to solve for Γ and L. Using the principle introduced in *1.3*, gain and internal loss can be added to the VCSEL cavity by including an imaginary part when defining the refractive index of each layer. In this case, the gain and internal loss are included in the values calculated for mirror reflectance, and the round-trip gain in the cavity can be calculated using the transfer-matrix method by the following equation. When this quantity is equal to zero, the VCSEL has achieved threshold.

$$G_{RT}(g) = -\ln\left(\frac{1}{\left|r_{top}(\lambda_r)\right|^2 |r_{bottom}(\lambda_r, g)|^2}\right) \quad 1.21$$

When G_{RT} is evaluated with no internal loss added to the cavity through complex refractive indices, the calculated g_{th}, L_{eff}, R_1, and R_2 can be used in *1.22* to calculate the confinement factor of the cavity.

$$\Gamma = \frac{1}{2L_{eff}g_{th}}\ln\left(\frac{1}{R_1 R_2}\right) \quad 1.22$$

1.3 High Contrast Gratings

The DBR is not the only reflector that is suitable for use in a VCSEL. A high-contrast grating (HCG) can also be designed to produce extremely high reflectance.

An HCG is a diffraction grating composed of a high refractive index material surrounded on all sides by a low refractive index cladding [11]. By designing the period Λ, duty cycle η, and

grating thickness t_g, various phenomena can be observed. HCGs have been used to implement high reflectance mirrors [12], high quality factor resonators [13], high-efficiency waveguide couplers [14], and even Fresnel lenses [15]. Their myriad phenomena are engineered by tailoring the modes supported by the periodic waveguide structure to produce interference to control the amplitude and phase of the diffraction orders of the grating [16]. While the coupling efficiency into various diffraction orders is only calculated numerically, HCGs still obey the basic laws of diffraction gratings. For example, the diffraction angle of order m is given by the following equation.

$$\sin(\theta) = \frac{m\lambda}{n\Lambda} \tag{1.23}$$

In order to prevent light from coupling into non-zero diffraction orders and being directed away from the laser's axis of propagation, HCG reflectors are designed with $n\Lambda < \lambda$. This ensures that none of the higher orders will propagate in the HCG cladding. If the spacer between the VCSEL cavity and the grating is too thin, however, then the evanescent first order can still couple into the semiconductor, causing diffraction loss.

To incorporate HCGs into the transfer-matrix calculations introduced in the previous section, rigorous coupled-wave analysis (RCWA) is used to calculate the reflection and transmission coefficients of each diffraction order. The zeroth order coefficients are used to construct a transfer matrix. Due to the presence of higher diffraction orders, it is not safe to assume that the interface is lossless.

$$\boldsymbol{T_{HCG}} = \frac{1}{t_0}\begin{bmatrix} 1 & r_0 \\ r_0 & 1 \end{bmatrix} \tag{1.24}$$

$$t_0^2 + r_0^2 \neq 1 \tag{1.25}$$

The first HCG VCSEL was demonstrated in 2007 [12], and the structure has since been used to produce wavelength tunable VCSELs at a variety of wavelengths for a variety of applications[17]–[22]. HCG reflectors have several properties that make them ideal for application in VCSELs. First, HCG reflectors are much thinner than DBRs, since they only require a single layer of 100-400 nm to give over 99% reflectance. This is useful from a production standpoint, as it is less expensive to grow a thinner epitaxy. The requirement of a low index cladding layer integrates well with MEMS tunable VCSELs, which require a tunable length air gap between the upper reflector and active cavity. An HCG can provide extremely broadband reflectance, which is obviously important for broadband wavelength tunability. Finally, an HCG offers polarization control. A 1D HCG generally only provides high reflectance for a single incident polarization, so the output of an HCG VCSEL is linearly polarized without the 3dB power penalty involved in passing an unpolarized source through a linear polarizer. This is an advantage whenever signal to noise ratio is a concern, as a polarization sensitive detector can reject randomly polarized noise.

2 3D Sensing Systems

2.1 Time of Flight

Time of flight (TOF) imaging is the simplest system for 3D sensing. In direct TOF, a light source is switched on and off to quickly illuminate a scene, and the reflected light is measured with a photodetector. The time delay τ between the illumination and detection pulses is measured, and the delay is converted to a distance d by the following equation.

$$d = \frac{\tau c}{2n} \tag{2.1}$$

Direct TOF is very sensitive to the ambient light conditions in the scene. For example, if a light in the room is switched on, the resulting rising edge detected by the PD may clock the wrong time delay. This can be alleviated by averaging over many pulses, but averaging will limit the framerate of the TOF camera.

Indirect TOF can boost signal to noise ratio by giving the illumination a unique fingerprint. A sinusoidal component is superimposed on the pulsed drive current, modulating the amplitude of the illumination.

$$I_{VCSEL}(t) = I_0 + I_1 \sin(\omega t) \tag{2.2}$$

The photodetector will measure the reflected signal added to the background light present in the scene.

$$I_{PD}(t) = B + A \sin(\omega t) \tag{2.3}$$

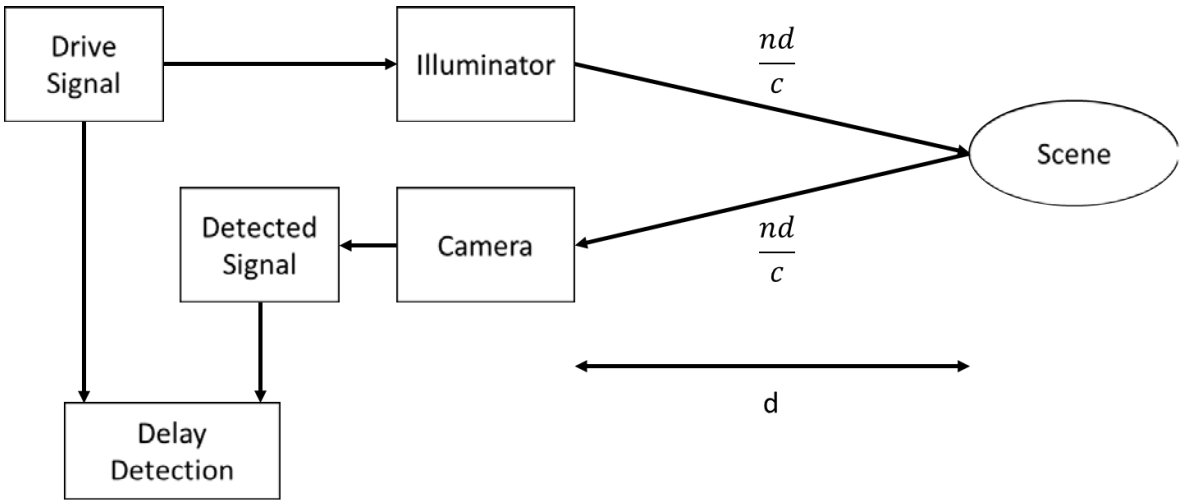


Figure 2.1 System diagram for time of flight detection. The light produced by the illuminator is delayed by a time τ that is proportional to the distance to the scene. The camera detects the signal, and the delay between the drive signal and detected signal is calculated.

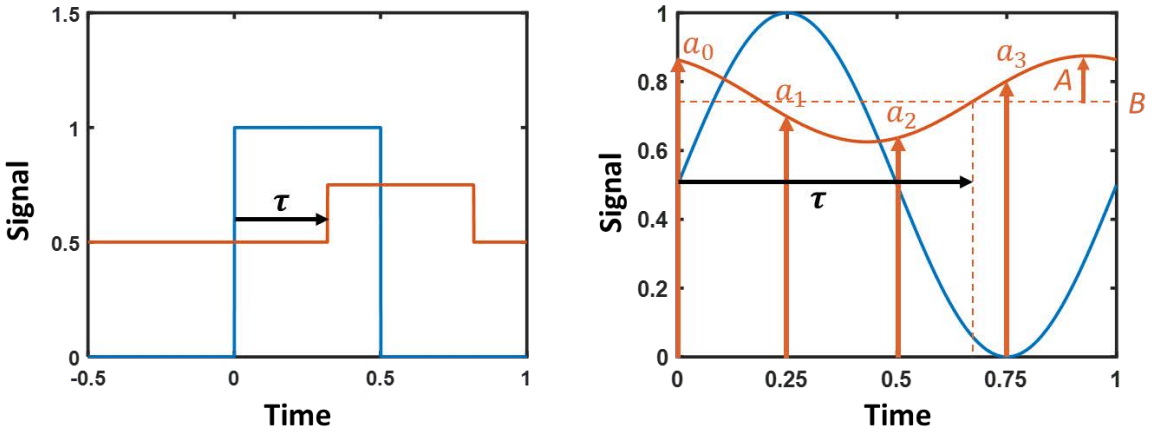


Figure 2.2 Comparison between direct and indirect TOF signals. In direct time of flight, the difference between two pulses is measured by detecting a rising edge or by integrating the total light received within a specified window. In indirect time of flight, the detected sinusoid is measured at four samples per period of the drive signal. These four samples allow the direct computation of detected modulation amplitude A, background signal level B, and phase ϕ, which is proportional to the delay τ.

If the intensity on the photodetector is measured at four times the drive frequency of the illuminator, then the phase, amplitude, and background level of the acquired signal can be computed with the four sampled values [23][24].

$$\phi = tan^{-1}\left(\frac{a_3 - a_1}{a_0 - a_2}\right) \quad 2.4$$

$$A = \frac{\sqrt{(a_3 - a_1)^2 + (a_0 - a_2)^2}}{2} \quad 2.5$$

$$B = \frac{a_0 + a_1 + a_2 + a_3}{4} \quad 2.6$$

Since any periodic signal shifted beyond 2π wraps back around to zero phase, the range of this technique is limited by the periodicity of the sinusoidal modulation. The measured depth is a fraction of the maximum range.

$$R_D = \frac{c}{2f} \quad 2.7$$

$$d = R_D \frac{\phi}{2\pi} \quad 2.8$$

The depth noise is given by equation *2.9*, which shows the paths for increasing the accuracy of indirect TOF measurements.

$$\sigma_L = \frac{c}{8A}\sqrt{\frac{B}{fN}} \quad 2.9$$

The main parameter that is controlled by the VCSEL is A: the amplitude of the sinusoidal modulation. At a minimum, the VCSEL must have a high enough modulation bandwidth to

produce a large signal at the drive frequency. For facial recognition in a smart phone, the maximum range can be safely limited to under a meter, which corresponds to a 150 MHz drive frequency. This is easily reached in a VCSEL, which is typically modulated at 10 GHz in datacom applications. If the modulation bandwidth requirement is met, then a VCSEL with a high wall-plug efficiency will give a large value of A.

2.2 Optical Coherence Tomography

Another emerging application for VCSELs is swept-source optical coherence tomography (SS-OCT). An SS-OCT system is illustrated in Figure 2.3 [25]. The tunable laser is swept across its frequency range at a rate of α.

$$\omega_{laser} = \alpha t \tag{2.10}$$

The output of the swept laser is passed through a 50/50 directional power coupler, and the output is used to illuminate a reference mirror and the sample under test. The reflected light from each sample is collected back into the fibers and mixed in the directional power coupler. The intensity is measured as a function of time using a photodetector.

$$E = E_{sample} + E_{ref} = Ae^{j\omega_s t} + Be^{j\omega_r t} \tag{2.11}$$

$$I(t) = EE^* = A^2 + B^2 + ABe^{i(\omega_s t - \omega_r t)} + ABe^{j(-\omega_s t + \omega_r t)} \tag{2.12}$$

$$I(t) = A^2 + B^2 + AB\cos\big((\omega_s - \omega_r)t\big) \tag{2.13}$$

$$\omega_{OCT} = \omega_s - \omega_r \tag{2.14}$$

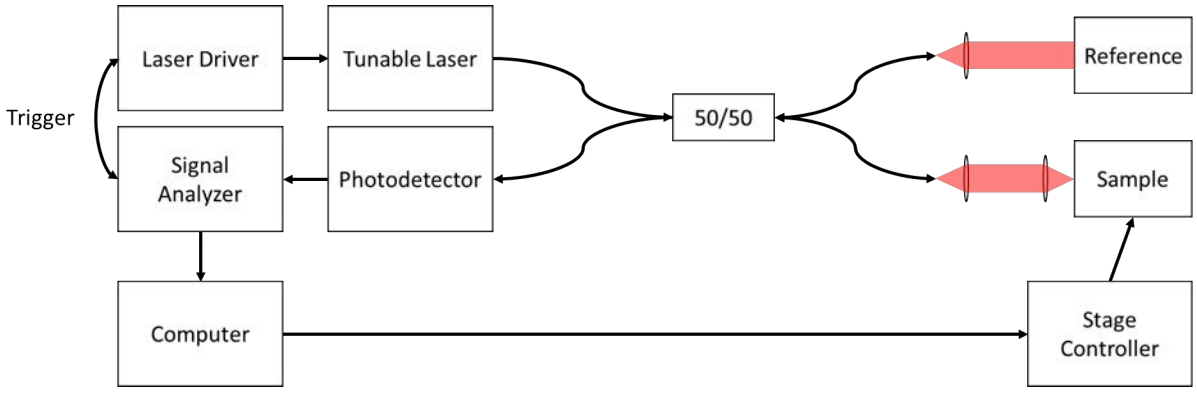


Figure 2.3. Optical coherence tomography system schematic. The tunable laser is used to illuminate the reference and sample arms of an interferometer, and the interferometric signal is detected by a photodetector. The signal analyzer measures the beat frequencies in the detected signal, and a computer converts the frequency spectrum to a depth profile. The computer is also used to move the sample after a scan is taken, allowing the system to build up a 3D image out of 1D scans.

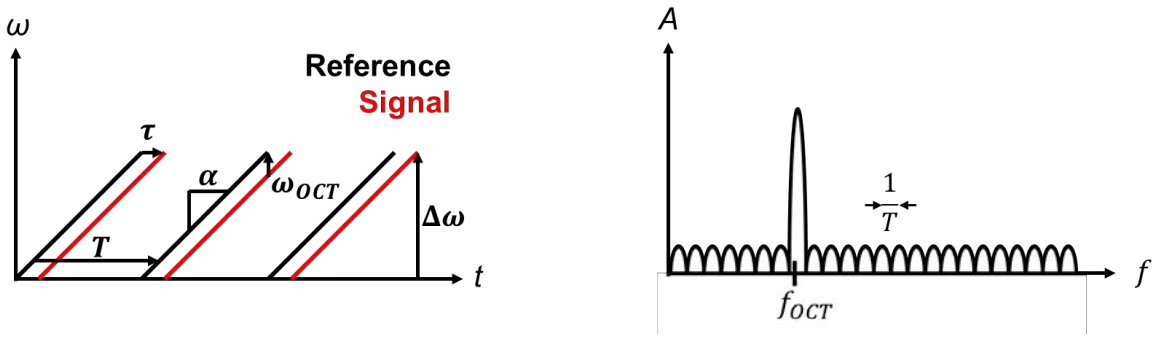


Figure 2.4. An example OCT measurement. The first plot shows the detected frequency as a function of time. Any difference in path length between the reference and signal arm cause a difference in frequency, which will manifest as a beat in signal intensity. The spectrum of the signal can be reconstructed with a fast Fourier transform of a single sweep period.

Any difference in depth L between the reference and sample will cause a delay τ in the swept signal, producing a beat frequency.

$$\omega_s = \alpha t \tag{2.15}$$

$$\omega_r = \alpha(t - \tau) \tag{2.16}$$

$$\omega_{OCT} = \alpha\tau \tag{2.17}$$

The fast Fourier transform (FFT) is used to compute the electrical spectrum of the amplified photocurrent. The spectrum directly correlates to the reflectivity profile of the sample under test when the frequency axis is scaled by $c/2n\alpha$.

One limit placed on the depth resolution is caused by the tuning range of the light source [26]. If the FFT uses a rectangular window function that spans one period of the wavelength sweep T, then the resulting spectrum will have lobes spaced by $\delta\omega_{OCT} = 2\pi/T$, limiting the frequency resolution to δf_{OCT} and the depth resolution to δL.

$$\delta L = \frac{c\delta\omega_{OCT}}{2n\alpha} = \frac{c\pi}{n\alpha T} \tag{2.18}$$

If the frequency range of the tunable laser is given by $\Delta\omega$, then the tuning slope can be replaced by $\alpha = \Delta\omega/T$.

$$\delta L = \frac{c\pi}{n\Delta\omega} \tag{2.19}$$

Since laser outputs are usually measured in wavelength space rather than frequency space, it is useful to transform the frequency tuning range into a wavelength tuning range.

$$\Delta\omega = \frac{2\pi c}{\lambda_{min}} - \frac{2\pi c}{\lambda_{max}} = \frac{2\pi c\Delta\lambda}{\lambda_{min}\lambda_{max}} \approx \frac{2\pi c\Delta\lambda}{\lambda_c^2} \tag{2.20}$$

$$\delta L = \frac{\lambda^2}{2n\Delta\lambda} = \frac{1}{2}\frac{\lambda_c}{n}\frac{\lambda_c}{\Delta\lambda} \tag{2.21}$$

The source-limited minimum resolution of an SS-OCT system is refactored to show the influence of two key parameters of a tunable laser. The resolution is first proportional to the wavelength of the laser inside the measured medium. It is intuitive that a smaller wavelength can be used to resolve a smaller displacement. Second, the resolution is inversely proportional to the fractional tuning range of the laser, $\Delta\lambda/\lambda$. This metric quantifies the absolute tuning range normalized to the center wavelength and is useful for comparing tunable lasers that operate at different wavelengths. Since the center wavelengths is usually dictated by absorption in the medium to be imaged, the fractional tuning range is the critical engineering parameter that needs optimization.

2.3 Structured Light

Structured light sensing relies on triangulation. The points of the triangle are defined by the illuminator, the camera, and the scene. The distance between the illuminator and the camera d is fixed by the construction of the system, and the angle projected by the illuminator θ_i is fixed by the far field pattern of the illuminator. The camera measures the angle of the reflected light θ_r, and the distance from the camera to the object is given by

$$L = \frac{\sin(\theta_i)}{\sin(\theta_i + \theta_r)} d \qquad 2.22$$

The measured reflection angle and calculated distance fully describe the vector between the camera and the object. In order to build a 3D map of an object, a map of these vectors need to be measured. There are several strategies to take the series of measurements required.

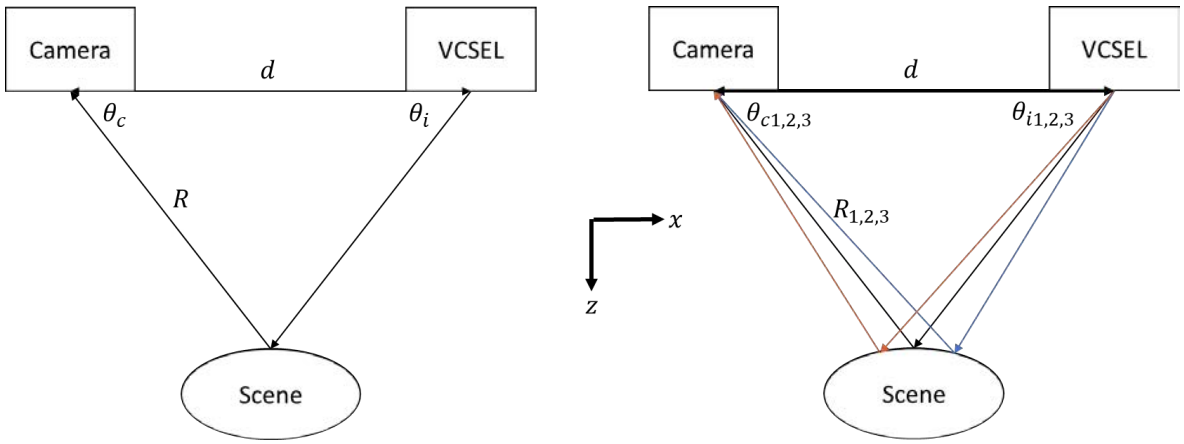


Figure 2.5. Structured light uses triangulation to determine the distance R between the camera and a point on the scene. The emission angle of the light source is structured to provide a known set of illumination angles θ_i, so a measurement of θ_c with a camera provides all the information required to solve for the position of the illuminated point on the scene.

First, a system can scan the scene and calculate the vector at each scan location. This can be performed with a single laser dot scanned in θ_{ix} and θ_{iy}, or with a line of light along the y axis that is scanned over θ_{ix}. A line can be produced with the asymmetric emission of an edge emitting laser, or by scanning a circular beam along the y axis much faster than the frame rate of the system. This method required minimal computation power and is not susceptible to fringe limits, but has a low throughput and is not suited for scanning moving objects.

In order to capture a scene in a single frame, the scene can be illuminated with a structured light pattern. The simplest structured light pattern is a series of vertical stripes of light and dark. If the displacement of each stripe is small compared to a calibration image, then the distance to each point on the lines can be calculated directly, but many algorithms have been developed to infer the position of the pattern [27]. The lateral resolution of the system is determined by the density of the illuminated points and depends on the distance to the scene. Since the distance to the scene is typically much larger than the desired lateral resolution, the paraxial approximation can be used to simplify the expression.

$$x = z \tan \theta_{ix} \approx z\theta_{ix} \tag{2.23}$$

$$\delta x \approx z\, \delta\theta_{ix} \tag{2.24}$$

One of the primary applications of structured light sensing is facial detection in smart phones. In this application, the size, cost, and efficiency of the module are very important. This makes VCSELs a very attractive option for illumination, since they are small, inexpensive, and efficient. Furthermore, VCSELs can be integrated into arbitrary patterns by mask layout.

The illumination module has a few key components. The VCSEL array creates a structured field of point sources that spans approximately 1 mm x 1 mm. The VCSEL array is collimated, transforming the displacement from the optical axis into a fan out angle. A single tile of a face detection system only spans about 5°, so the paraxial approximation is once again valid.

$$\theta_{ix} = \operatorname{atan}\frac{h}{f_c} \approx \frac{h}{f_c} \tag{2.25}$$

The angular resolution, and thus the lateral resolution, is proportional to the space between two emitters.

$$\delta\theta_{ix} = \frac{\delta h}{f_c} \tag{2.26}$$

$$\delta x = \frac{z\, \delta h}{f_c} \tag{2.27}$$

In a smartphone facial detection application, the distance to the target is set by the length of the user's arm, and the focal length of the collimating lens is limited by the size of the illumination module. In order to improve resolution, the spacing between VCSELs must be reduced as much as possible.

The collimated beams are passed through a diffractive optical element that tiles the VCSEL pattern, which spans approximately 5°, to illuminate a field of view of approximately 60°. The

period of the DOE must be designed to match the diffraction angle to the single-tile illumination angle.

$$\Lambda = \frac{\lambda}{sin(2\theta_{ix,max})} \tag{2.28}$$

Since the power of the light is split between many diffracted orders by the DOE, the VCSEL array must have a high output power to produce a detectable signal. To produce a pattern without bright and dim spots, the output power of each emitter must be uniform across the array, and the divergence angle must be small enough that the emission from the edge devices falls inside the lens pupil.

3 Air Cavity Dominant Tunable VCSELs

3.1 Introduction

Wavelength tunable VCSELs were first demonstrated in 1995, with a primary application target of wavelength division multiplexing (WDM) [28]. In a WDM system, a wavelength tunable VCSEL can be used as a reconfigurable source which can be configured on the fly to communicate on any given channel within a multiplexing scheme. This reduces the size of a required spare inventory in a datacenter and even allows for the inclusion of reconfigurable spares on an integrated communications card. Tunable VCSELs were first realized at short-reach interconnect wavelengths between 850 and 980 nm and were later extended to the C-band centered at 1550 nm [29]. Tunable VCSELs in the C-band are compatible with dense wavelength division multiplexing (DWDM), where a single tunable VCSEL can span the entire band of possible communications channels that extends from 1530 nm to 1565 nm.

Tunable VCSELs have also been designed for tunable diode laser absorption spectrometry (TDLAS). By tuning the emission wavelength across a known molecular absorption wavelength and monitoring the transmitted signal, the presence and concentration of common organic molecules, like CO or NH_3, can be detected [30]. This technique requires lasers operating at long wavelengths (1.5-3 um), where molecular absorption resonances typically reside.

More recently, tunable VCSELs have been applied to ranging applications including frequency-modulated continuous wave (FMCW) lidar and optical coherence tomography (OCT) [19]. As shown by Equation *2.21*, the resolution of these techniques are limited by the wavelength range used in the measurement. In a system with a single pixel photodetector and a swept wavelength source, the spectral range is limited by the tuning range of the light source.

3.2 Tunable VCSEL Structures

Tunable VCSELs share a common structure that includes a fixed reflector, a gain region, and a movable reflector.

The gain region is typically a λ or $\lambda/2$ portion of semiconductor material which contains several quantum wells, designed to give high gain across the targeted wavelength range. For wavelengths shorter than 1200 nm, the gain region is lattice-matched to GaAs, and may incorporate InGaAs, GaAsP, AlGaAs, or GaAs [22], [28]. For longer wavelengths, especially at the O-band and C-band, the gain region is lattice-matched to InP [18], [31], [32].

The fixed reflector is generally a distributed Bragg reflector (DBR), which can be formed using several different methods. The simplest way to form a DBR reflector is by growing it epitaxially in an MOCVD or MBE reactor. This is convenient for GaAs-based VCSELs, where a refractive index difference Δn of 0.5 can be easily obtained by alternating between GaAs and AlGaAs [17], [28]. For a higher bandwidth mirror, alternating GaAs and AlAs layers can be grown and then oxidized to form a Δn of almost 2. This structure can be monolithically integrated with a GaAs-compatible gain region [19] or bonded onto an InP gain region [31], depending on the wavelength of operation. A third option is to deposit alternating dielectric layers after the epitaxy is complete, which can give a Δn of 1 [32].

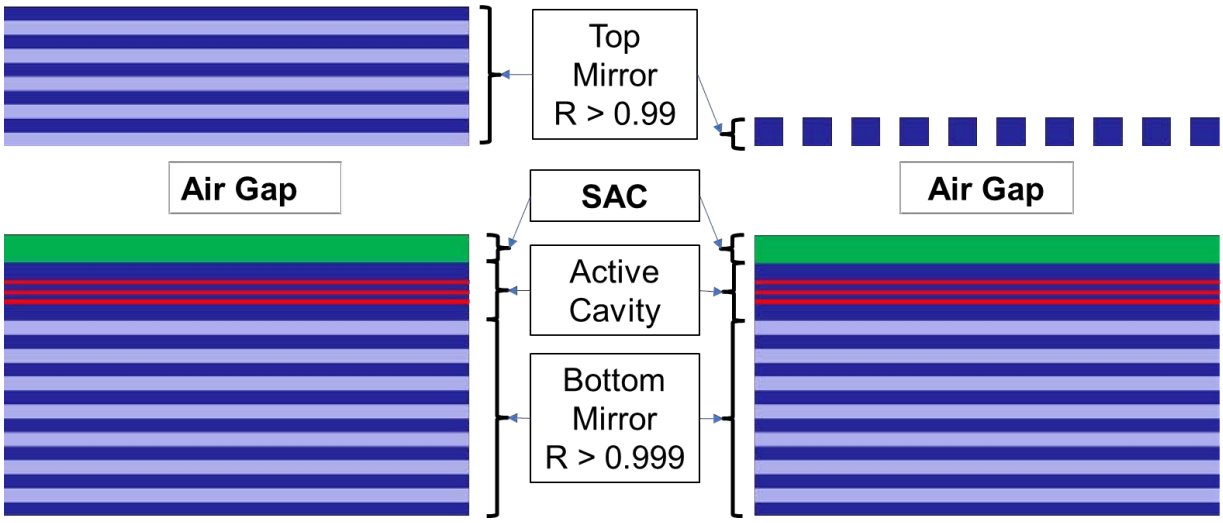


Figure 3.1. Cross-sectional schematic of two wavelength tunable VCSELs. Both VCSELs have a movable top mirror, an air gap, a semiconductor-air coupling interface, and active cavity, and a bottom mirror. The VCSEL on the left utilizes a DBR for the tuning mirror, while the VCSEL on the right uses an HCG reflector.

The first tunable VCSEL was demonstrated with an epitaxially grown DBR as the upper reflector. The DBR was formed into a cantilever by etching the outline of the cantilever into the GaAs-based epitaxy, then releasing the cantilever from the substrate with a selective etch [28]. Tuning mirrors have also been demonstrated by depositing a series of dielectrics with evaporation or plasma-enhanced chemical vapor deposition (PECVD) after the III-V epitaxy is complete [32], [33], then micromachining them to form the tunable mirror. Finally, the movable reflector can be implemented as an HCG, which provides broadband reflectance with a single epitaxial layer [17].

The movable mirror must be suspended over an air gap, which can be made longer or shorter by utilizing a microelectromechanical system (MEMS) actuator. The interface between the semiconductor layers and the air gap can have a significant reflectance and can create profound performance differences between otherwise identical VCSELs. This region is called the semiconductor-air coupling (SAC) region, and it is investigated in depth in this work [21].

3.3 Tuning Range Limitations

The tuning range of a VCSEL is limited by the smallest of three ranges: the maximum displacement of the microelectromechanical system (MEMS) supporting the tuning mirror, the threshold bandwidth, and the free spectral range (FSR).

In order to optimize the MEMS, the device needs to be designed to displace the mirror over a half wavelength in air. The tuning curve of a VCSEL is quasi-periodic beyond this distance, so any additional distance only adds to the cavity length, which detracts from the FSR. The displacement of the MEMS can come from multiple actuator types, including piezoelectric actuators, thermal actuators, and electrostatic actuators. Piezoelectric actuators require the deposition of a piezoelectric material, which can introduce stress in response to an applied

voltage and displace the MEMS spring toward or away from the gain material [34]. This has the advantage of bi-directional actuation but comes with the drawback of requiring an extra material deposition, which increases device complexity and cost. Thermal actuators make use of differences in thermal expansion coefficients between materials and displaces the mirror in response to a temperature shift provided by a resistive heater. Thermal actuators can be designed to displace the mirror inwards or outwards but are limited in actuation speed by a thermal time constant [32]. Electrostatic actuators leverage the attractive force that exists between the plates of a capacitor, with one plate being the tuning reflector and the other being the SAC interface [28]. Applying a voltage will displace the mirror toward the SAC interface. Electrostatic actuators offer simple fabrication and high actuation speeds but can only be used to shorten the cavity and suffer from a gap-closure instability. Once the mirror is displaced by approximately one third of the original gap length, the mirror will collapse into the SAC interface. In order to account for this instability with electrostatic actuation, the length of the airgap must be at least $3\lambda/2$. If the MEMS is actuated with at its mechanical resonance frequency, this distance can be reduced since the mirror will travel both up and down in comparison to its resting position.

The threshold bandwidth limitation comes from Equation *1.20*, which defines the condition for laser threshold. In a fixed-wavelength laser, the threshold condition only needs to be considered at the fixed lasing wavelength. For a tunable laser, the threshold condition needs to be considered across the entire tuning range. Gain, mirror loss, and confinement factor all become functions of wavelength and mirror position. At the center of the tuning range, gain is at its highest, requiring smaller mirror loss and confinement to achieve threshold. Away from the tuning center, the gain decreases, requiring decreased mirror loss and increased confinement. At a wavelength that is sufficiently far from the tuning center, the loss will become greater than the gain can compensate, and the device will no longer achieve threshold. This range has been optimized by decades of research and development in epitaxial material quality and quantum well design for higher gain, and by the introduction of high bandwidth reflectors such as HCGs and dielectric DBRs.

The FSR limitation is a result of competing Fabry-Perot (FP) modes. If two FP modes are within the threshold bandwidth of the tunable laser, then both will be able to lase. If one of the two modes has a lower threshold gain than the other, then the gain will be clamped at the lower threshold, and the other FP mode will not achieve threshold. Since the threshold material gain rises on both the high wavelength and low wavelength sides of the threshold gain curve, the FSR of the tunable VCSEL will determine the exact crossover between adjacent modes. The FSR is inversely related to the effective length of the VCSEL cavity, which does not remain constant across the tuning range. In modern tunable VCSELs, the FSR is the ultimate limit of the tuning range.

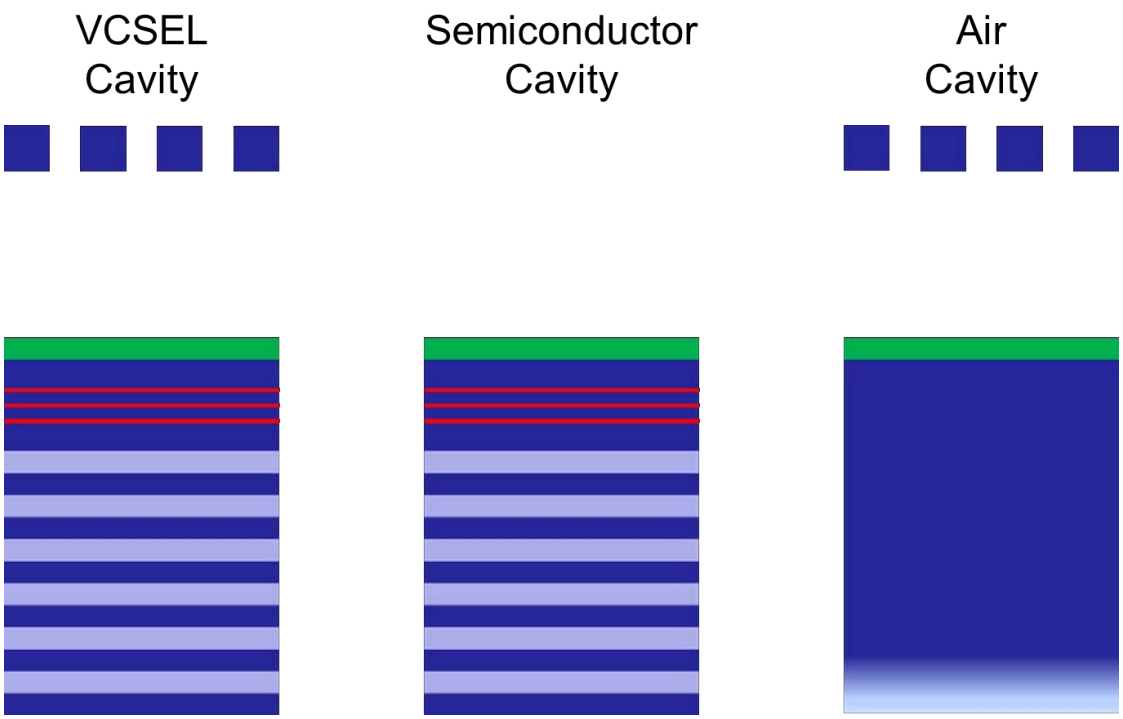


Figure 3.2. A tunable VCSEL cavity is composed of two coupled cavities. The semiconductor cavity exists between the upper surface of the SAC region and the bottom of the lower reflector. The air cavity exists between the upper reflector and the bottom of the SAC region. The resonances of these two cavities control the tuning behavior of the full VCSEL cavity. The design of the SAC region will have profound effects on the resonant behavior of these three cavities.

3.4 Coupled Cavity VCSEL Designs

Since the tunable VCSEL has a high refractive index drop in the middle of the device, the optical path can be interpreted as a system of 2 coupled cavities: one centered in the semiconductor gain region and one residing in the air gap. Both the semiconductor cavity and the air cavity have independent resonances, and the coupling between the two cavities is dictated by the design of the SAC interface.

In the earliest tunable VCSELs, nothing special was done to engineer the SAC interface. Semiconductor cavities were designed according to normal VCSEL design rules, with a high index active region and an integer number of DBR pairs between the active region and the air cavity. This semiconductor cavity dominant (SCD) design maximizes the confinement factor of the laser at the center of the tuning range, which was expected to minimize the threshold gain. This design causes a tuning characteristic that has a steep slope at the edge of the tuning range, but a small slope at the center of the tuning range [20], [28].

In order to increase the tuning range, researchers added an antireflection coating to the SAC interface, merging the semiconductor cavity and air cavity into one extended cavity (EC) [35]. This eliminates produces a constant tuning slope and increases the FSR at the edges of the tuning

range. The EC design was used to set the prior record for fractional tuning range for electrically pumped tunable VCSELs, and has shown impressive results for optically pumped tunable VCSELs as well [6], [19], [32].

A third design is also possible. In this design, the semiconductor cavity is designed according to typical VCSEL design rules but is terminated with an additional $\lambda_C/4$ section of high index semiconductor material. This maintains the high reflectance SAC interface but produces a semiconductor cavity which is antiresonant ($\varphi = \pi$) at the center wavelength. The optical field is coupled into the air cavity at the tuning center, which is the fundamental characteristic of an air cavity dominant (ACD) VCSEL. This design causes a reduction in confinement factor at the center wavelength, but the cavity loss is compensated by an increased effective length [21].

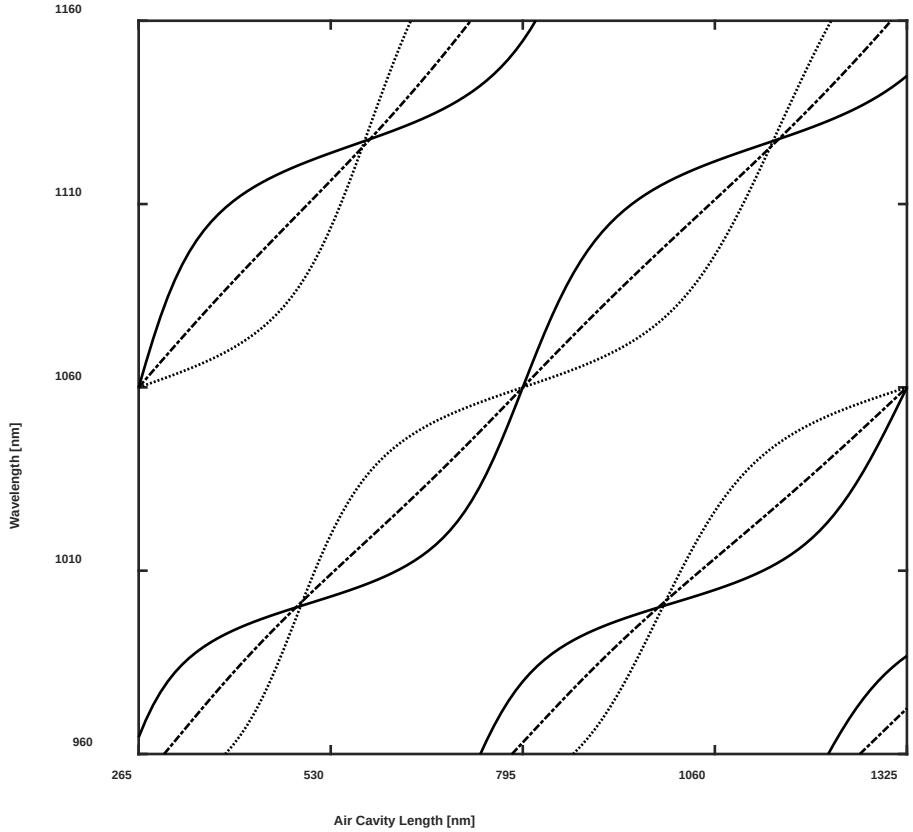


Figure 3.3. Comparison between ACD, EC, and SCD tuning characteristics for the simplified tunable VCSEL model. The wavelength of the EC VCSEL varies almost linearly with air cavity length. The wavelength of the SCD VCSEL has a small slope at the center wavelength of 1060 nm, resulting in poor tuning efficiency. The wavelength of the ACD VCSEL has a maximum tuning slope at the center wavelength, but reduced slope at the tuning edges. Reprinted with permission from [21].

3.5 Coupled Cavity VCSEL Modelling

In order to investigate the tuning behavior of the three tunable VCSEL designs (SCD, EC, and ACD), a simplified structure is investigated as a model. This structure consists of a $4\lambda_C$ section of semiconductor ($n = 3.5$), a $\lambda_c/4$ SAC region ($n = n_{SAC}$), and a variable-length air cavity ($n = 1$). The simulation is bounded by two ideal reflectors, which provide $r = 0.999 + 0j$ across all wavelengths. This simple structure can be used to model each case by selecting an appropriate refractive index for the SAC region. For the SCD design, n_{SAC} is set to 1 to match the refractive index of the air gap. For the EC design, n_{SAC} is set to the geometric mean of 1 and 3.5, which is the ideal index for an antireflection coating. For the ACD design, n_{SAC} is set to 3.5 to match the refractive index of the semiconductor portion.

The resonant wavelengths of the full VCSEL structure, the semiconductor cavity, and the air cavity can each be determined using the transfer matrix method. For the VCSEL cavity, the structure is split immediately below the SAC region, and the reflection phase is computed for the top half and bottom half of the structure. The resonant wavelength is solved by finding the wavelength which has a round trip phase of a multiple of 2π radians. This analysis is repeated with modifications to determine the resonance wavelength of the semiconductor and air cavities. For the semiconductor cavity, the upper ideal reflector is excluded from the simulation and the structure is split immediately below the SAC region. For the air cavity, the lower ideal reflector is excluded, and the structure is split immediately above the SAC region. This analysis is repeated for every air gap length of interest, which has a range chosen to correspond to typical dimensions of an electrostatic MEMS actuator.

The VCSEL resonance as a function of air gap length is shown in Figure 3.3 for the SCD, EC, and ACD device configurations. As shown experimentally, the SCD curve has a small slope at the tuning center [20] and the EC curve is approximately linear [32]. The ACD curve shows the opposite characteristics of the SCD curve, with a high tuning slope at the center wavelength. Since the ideal reflectors have infinite bandwidth, the tuning curves show a periodic behavior as the air gap length and wavelength increase. In a physical device, these tuning curves would be sampled in the y dimension by the threshold bandwidth determined by the gain material and the reflectance of the mirrors.

When $n_{SAC} = 1$, the optical structure represents the simplest possible SCD VCSEL. The resonance lines of this structure are shown in Figure 3.4. Note that the x-axis extends to -265 nm, which corresponds to the point where the upper reflector touches the top of the semiconductor in the SCD structure. The semiconductor resonance lines are plotted in blue. The semiconductor cavity resonance does not depend on the position of the tuning mirror, so the semiconductor resonances are shown by horizontal lines. The air cavity resonance is linear versus the position of the tuning mirror, and is shown in red. The resonance for the full structure is plotted in black. Starting from L = -265 nm, the full structure resonance starts coincident with the semiconductor cavity resonances. The full structure resonance follows the semiconductor cavity resonance to an avoided crossing between the semiconductor and air cavity resonances. The semiconductor resonance then follows the air cavity resonance to another avoided crossing.

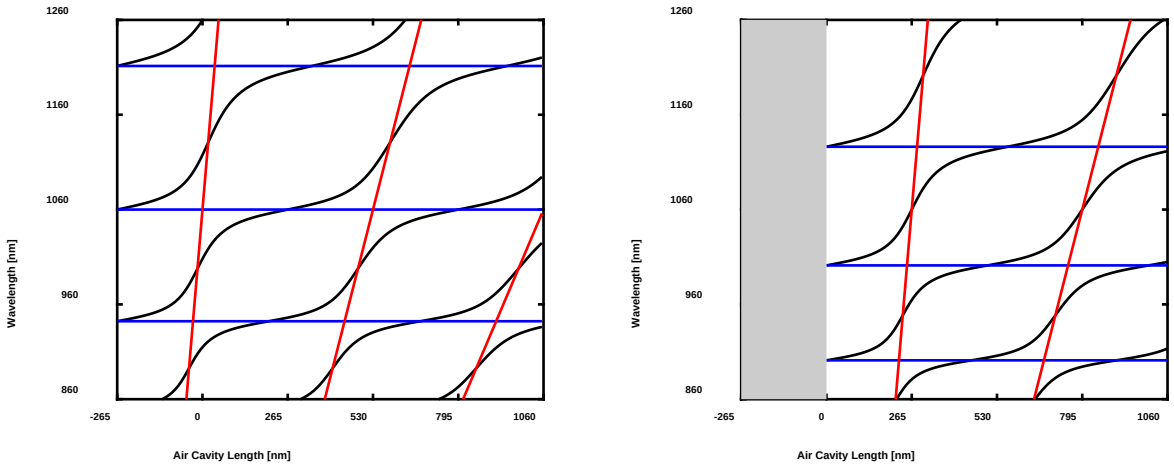


Figure 3.4. Tuning curves for SCD (left) and ACD (right) devices. Blue lines show the semiconductor cavity Fabry-Perot modes, which are independent of air cavity length. Red lines show air cavity modes, which are linear with air cavity length. Black lines show the resonance of the coupled-cavity VCSEL. Crossings between semiconductor and air cavity resonances result in anti-crossing behavior between adjacent VCSEL cavity modes. Reprinted with permission from [21].

When $n_{SAC} = 3.5$, on the other hand, the optical structure represents the ACD VCSEL. An airgap length of -265 nm no longer makes physical sense, so the plots begin at L = 0 nm, when the upper reflector touches the semiconductor portion. Again, the VCSEL cavity resonance begins at the same wavelengths as the semiconductor cavity and avoids crossings to alternate between the semiconductor and air resonances.

The largest difference between the SCD and ACD tuning curves is in the alignment of the semiconductor cavity resonance with the center wavelength. In the SCD case, there is a resonance at the center wavelength, so the VCSEL curves must have reduced slope to follow the horizontal resonances. In the ACD case, only the air cavity has resonances at the center wavelength, so the tuning curve is forced to follow the steep air cavity resonance lines. It is also apparent that the FSR of the VCSEL resonance lines is narrower near avoided crossings, and wider when the VCSEL follows the semiconductor resonance.

When infinite bandwidth mirrors are used, the difference between SCD and ACD devices is subtle. The two series of resonances are almost identical, only shifted with respect to wavelength. Once finite bandwidth mirrors are included in the simulation, the difference becomes dramatic. The finite bandwidth mirrors will sample the section of the tuning curve on the y-axis nearly symmetrically around the center wavelength. Once VCSEL modes that are outside of the mirror bandwidth are excluded, the FSR at the center wavelength is too large to matter, and the FSR at the tuning edges will determine the ultimate range of the device.

3.6 Practical Tunable VCSEL Design

In order to extend the simplified model to a real VCSEL structure, more detail is added to the optical structure. The lower reflector is replaced by a DBR composed of GaAs and AlGaAs. The 4λ semiconductor cavity is replaced with a 1λ AlGaAs cavity containing strain compensated InGaAs quantum wells with GaAsP barriers. The λ/4 SAC layer is replaced with a 4-pair upper DBR with an extra λ/4 layer that will be used to set the semiconductor cavity to be resonant or antiresonant. The upper mirror is replaced with an HCG reflector.

Figure 3.5 shows the tuning curve of the full VCSEL structure designed for a tuning center of 1055 nm when configured as SCD, EC, and ACD. For each case, the mode with the lowest threshold material gain is plotted in bold, while the nonlasing modes are shown with dashed lines. The wavelength range is bounded by the bandwidth of the lower DBR mirror. The FSR-limited tuning range can be determined by measuring the change in wavelength between the minimum and maximum values of a single solid curve. This comparison shows that the FSR-limited tuning range of an ACD VCSEL is greater than that of an otherwise identical EC or SCD VCSEL.

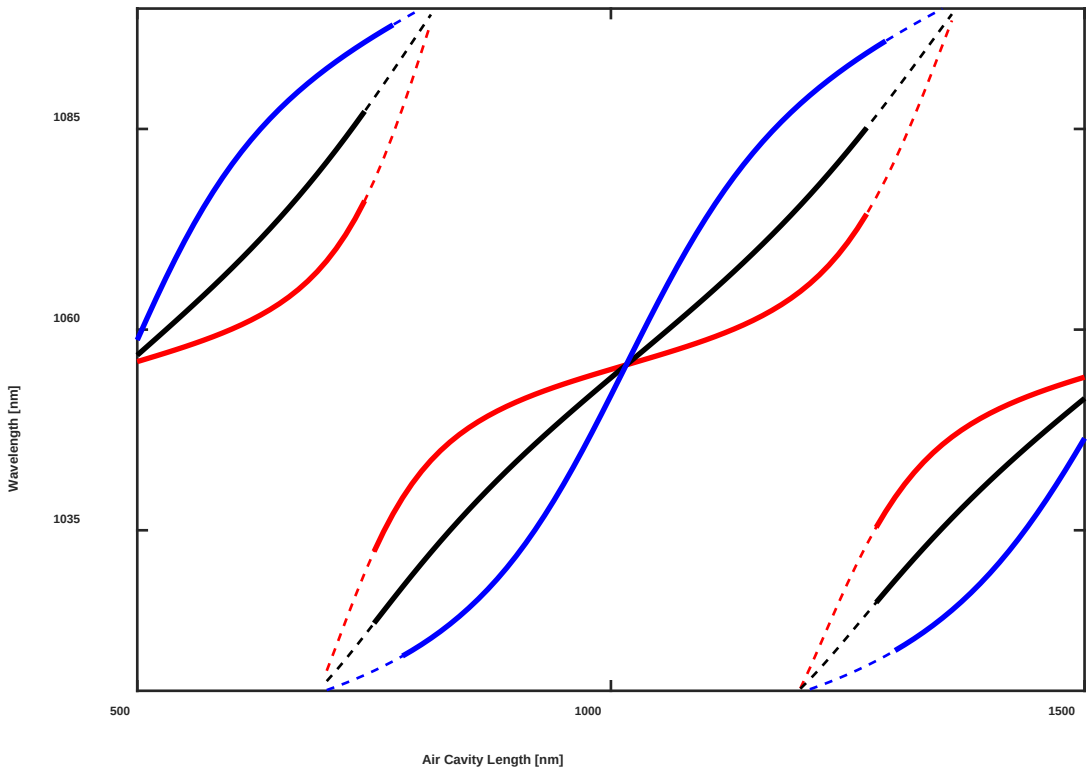


Figure 3.5. ACD VCSELs (blue) have a higher tuning range than nearly identical EC (black) or SCD (red) VCSELs because the ACD design has a wider FSR at the tuning edges. For each trace, the dominant mode with the lowest g_{th} is plotted in bold. Vertical discontinuities in the bold line represent a jump between dominant modes, and the height of the discontinuity is the FSR. The FSR for the ACD VCSEL is 76 nm, while the FSR for the EC and SCD devices is 59 nm and 39 nm, respectively.

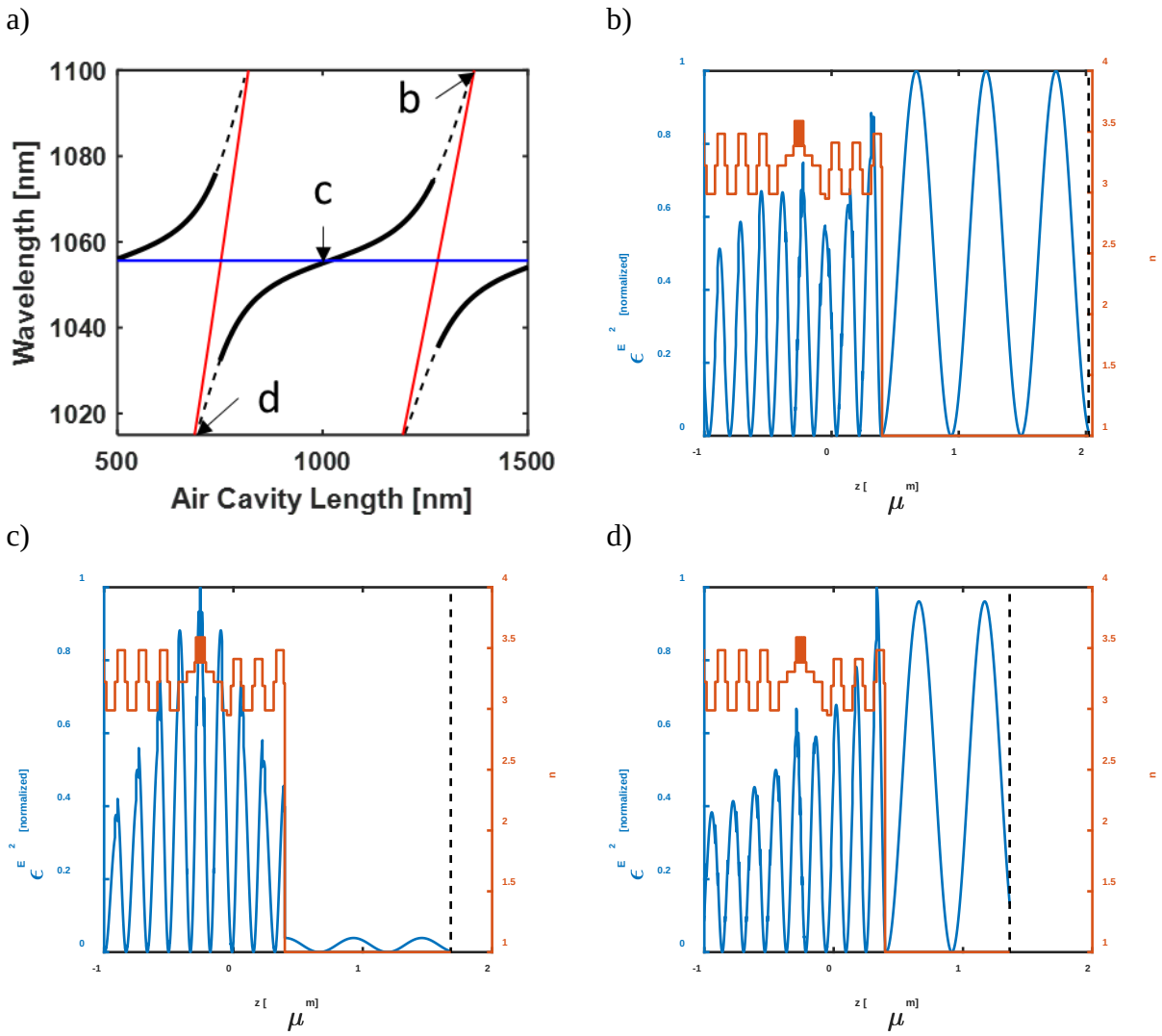


Figure 3.6. SCD VCSEL resonance analysis. (a) The VCSEL resonance is shown in black, the semiconductor cavity resonance is shown in blue, and the air cavity resonances are shown in red. The dominant VCSEL mode is plotted in bold. Three points on the VCSEL resonance curve are sampled: (b) the upper end of the tuning curve, (c) the center of the tuning curve, and (d) the lower end of the tuning curve. The electric energy distribution is shown against the refractive index profile of the VCSEL. At the upper and lower ends of the tuning curve, which overlap with the air cavity resonance, the energy is coupled strongly into the air. At the center of the tuning curve, which resides on the semiconductor cavity resonance, the energy is coupled into the active cavity.

As in the simplified device, the semiconductor cavity and air cavity resonances can be calculated for the SCD and ACD VCSEL designs. The resonances for the SCD VCSEL are shown in Figure 3.6 in blue and red. In addition, plots showing the electric energy distribution are shown for various points along the central resonance. Figure 3.6(b) shows the electric energy distribution at 1100 nm, where the VCSEL curve intersects the air cavity mode. This plot shows a large amount of energy confined in the air cavity in comparison to the energy in the semiconductor cavity.

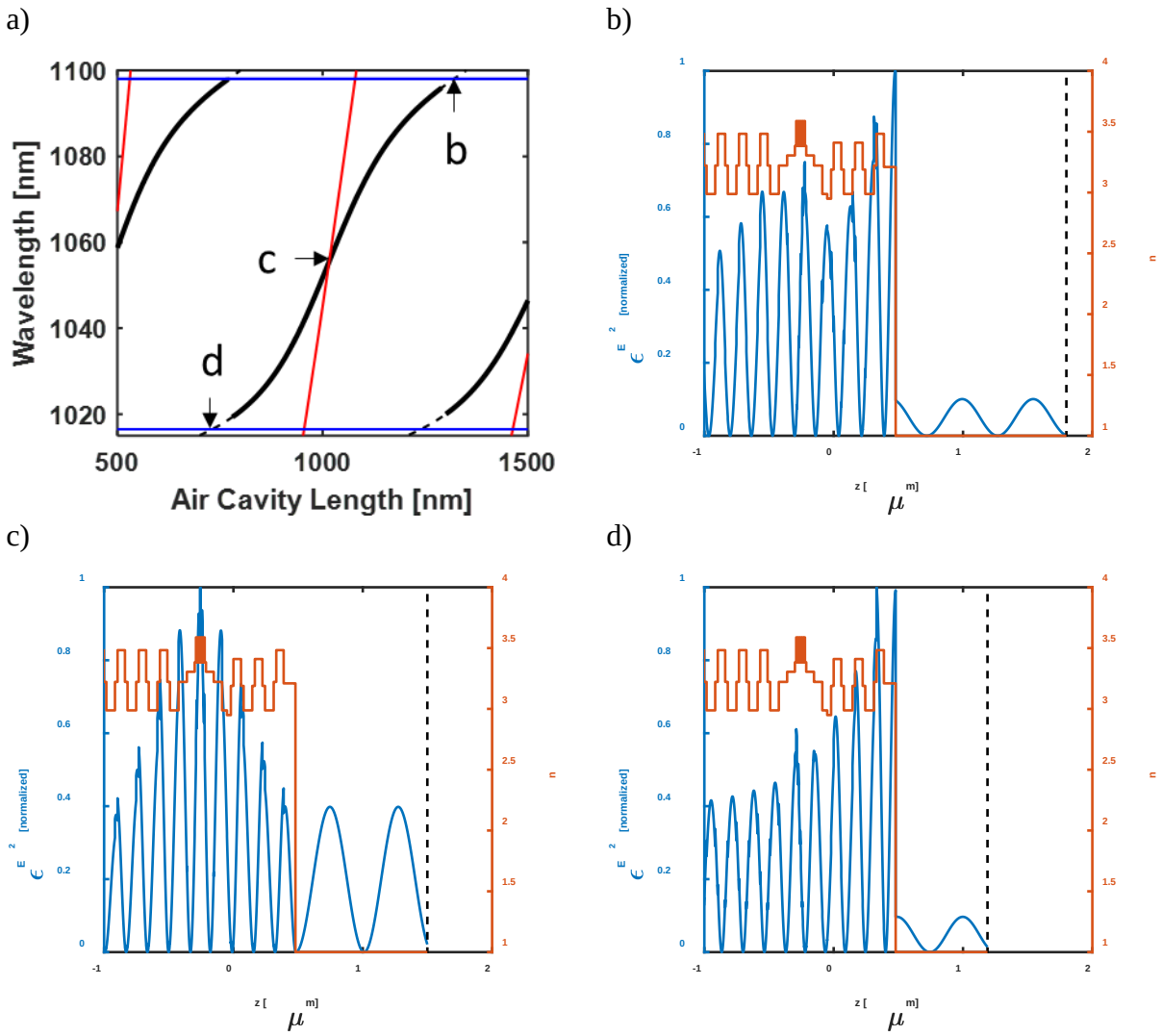


Figure 3.7. ACD VCSEL resonance analysis. (a) The VCSEL resonance is shown in black, the semiconductor cavity resonance is shown in blue, and the air cavity resonances are shown in red. The dominant VCSEL mode is plotted in bold. Three points on the VCSEL resonance curve are sampled: (b) the upper end of the tuning curve, (c) the center of the tuning curve, and (d) the lower end of the tuning curve. The electric energy distribution is shown against the refractive index profile of the VCSEL. At the upper and lower ends of the tuning curve, which overlap with the semiconductor cavity resonance, the energy is coupled strongly into the semiconductor cavity. At the center of the tuning curve, which resides on the air cavity resonance, the energy is coupled into the air cavity.

Figure 3.6(d) shows the energy confinement at the other end of the curve, where the energy is again pushed into the air cavity. Figure 3.6(c) shows the energy distribution at the center of the tuning range, when the VCSEL resonance intersects the semiconductor cavity resonance. In this plot, the energy in the air cavity is minimized.

Figure 3.7 shows the energy distribution in the ACD device, which shows opposite behavior to the SCD device. The energy confinement plots show strong confinement in the semiconductor at

the edges of the tuning spectrum and larger confinement in the air at the tuning center. In both the ACD and SCD energy confinement plots, the field is well aligned with the quantum wells at the tuning center but visibly misaligned with the quantum wells near the tuning edges. This causes a reduction in confinement factor as the resonant wavelength moves away from the center wavelength, which in turn causes an increase in threshold material gain.

3.7 Threshold Material Gain of an ACD VCSEL

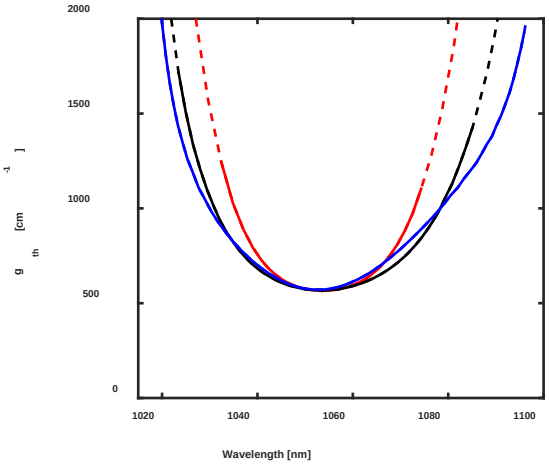
Forcing the electric energy distribution to reside outside of the semiconductor portion of a wavelength tunable VCSEL is counterintuitive to the design principle that confinement factor should be maximized in order to minimize the laser threshold current. If other factors are not considered, the reduced confinement in the ACD VCSEL could correspond to an unreachably high threshold material gain that renders the enhanced tuning range useless. Rigorous transfer matrix simulations show that this is not the case.

After determining the resonant frequencies of the three VCSEL structures, transfer matrix calculations can also be used to determine the threshold material gain of each mode. Loss and gain can be added to the simulation by including an imaginary part in the refractive index of each layer. First, a small amount of loss (20 cm^{-1}) is added to every semiconductor layer in the laser, while the air is left lossless. Next, gain is added to the quantum well layers incrementally, and the round-trip gain is calculated according to *1.21*. The threshold material gain is the amount of gain required to produce a round-trip gain of 0. This is repeated for each resonant mode at each point on the VCSEL tuning curve in order to find the threshold material gain as a function of lasing wavelength.

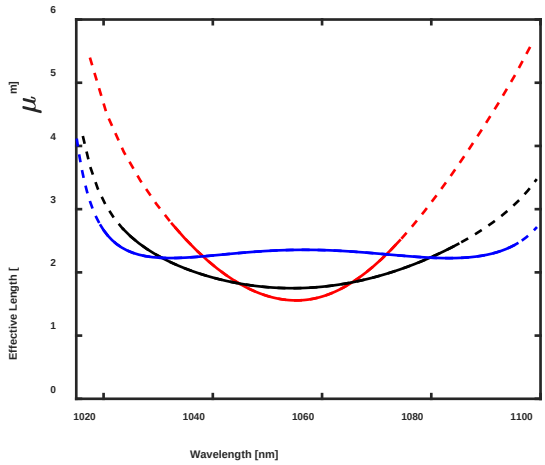
The threshold material gain is shown in Figure 3.8(a) for the SCD, EC, and ACD VCSELs. The threshold gain at the center of the tuning curve has less than a 1% difference between all three designs. The threshold material gain for the three devices diverges at higher and lower wavelengths. It increases the slowest for the ACD device, which results in a significantly lower threshold at the tuning edges in comparison to the EC and SCD devices.

Since a VCSEL uses distributed reflectors instead of a planar mirror, the length of the VCSEL cavity is a nontrivial parameter. The effective length of a VCSEL cavity is the sum of the gain cavity length, the effective length of the lower reflector, and the effective length of the upper reflector. The effective length of a reflector is defined in analogue to a planar mirror shifted a certain distance away from the plane of reference. The distance between a planar mirror and the plane of reference creates a negative phase slope with respect to wavelength. If the phase of an arbitrary reflector is known, then the effective length can be determined by calculating the derivative of the slope with respect to wavelength. This is calculation is performed numerically for the ACD, EC, and SCD VCSEL structures and is plotted in Figure 3.8(b). At the tuning center, the ACD device has the highest effective length. The upper reflector, which includes the air cavity, will store photons and only gradually return them to the active cavity. This increased round-trip delay is analogous to a long cavity with a long transit time.

a)



b)



c)

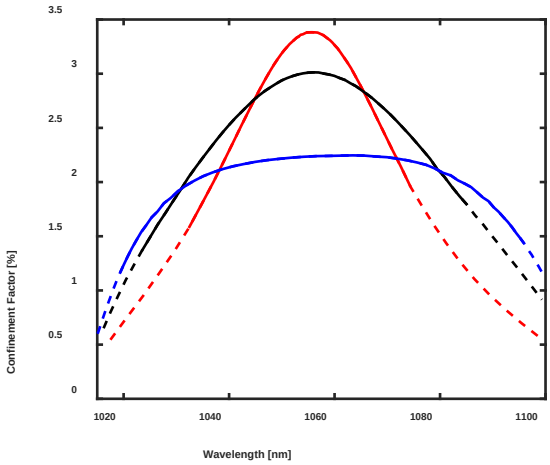


Figure 3.8. Calculated parameters of the simulated ACD, EC, and SCD VCSEL cavities. (a) The threshold material gain of all three VCSEL designs are within 1% of each other at the center of the tuning range. (b) At the tuning center, the ACD VCSEL has the highest effective length measured from the active cavity. As the wavelength moves away from the center wavelength, the effective length stays the most constant for the ACD device. (c) As expected, the confinement factor in the ACD device is much lower than the confinement factor in the SCD device. Near the edges of the tuning range, the ACD device has the highest confinement factor. Reprinted with permission from [21].

Mirror loss in a VCSEL is given by Equation *3.1*, which shows that an increase in effective length is desirable to compensate for a reduced confinement factor.

$$\alpha_m = -\frac{1}{2\Gamma L}\ln(R_1 R_2) \qquad 3.1$$

Mirror loss can also be rigorously calculated using the transfer matrix method by setting all other sources of loss to zero and calculating the threshold material gain of the VCSEL. Once the mirror loss is calculated, this equation can be used to solve for the confinement factor of the

three devices. The resulting confinement factor is plotted in Figure 3.8(c) for the three designs, which illustrates that the difference in confinement factor of the three designs is compatible with the nearly identical threshold material gain.

3.8 Fabrication of an ACD VCSEL

Tunable VCSELs with an ACD design were fabricated in order to prove the increased tuning range and low threshold. Process cross-sections are shown in Figure 3.9.

The process begins with a 4" epiwafer that consists, from bottom to top, of a GaAs buffer layer, a lower DBR with 38.5 pairs of alternated GaAs and AlGaAs, which contains a 1λ n-type contact layer, a 1λ active cavity containing InGaAs quantum wells with GaAsP buffers, a 6 pair upper DBR containing an oxide aperture layer, a λ/4 InGaP etch stop, an GaAs sacrificial layer, and an $Al_{0.60}Ga_{0.40}As$ HCG layer. In order to provide the desired electrical structure, the layers below the active cavity are doped n-type, the cavity is left undoped, the layers between the active cavity and the etch stop are doped p-type, and the remaining layers are doped n-type.

First, HCGs and their supporting MEMS are defined using electron beam lithography in PMMA A4 resist. A proximity effect correction is applied to the pattern to assign an increasing dose to gratings with decreasing duty cycle in order to ensure a high-fidelity pattern. The grating is etched using reactive ion etching in $SiCl_4$ and Ar chemistry. The etch is timed so that it proceeds into the sacrificial layer while minimizing erosion of the resist. The PMMA is removed with acetone, isopropyl alcohol and water.

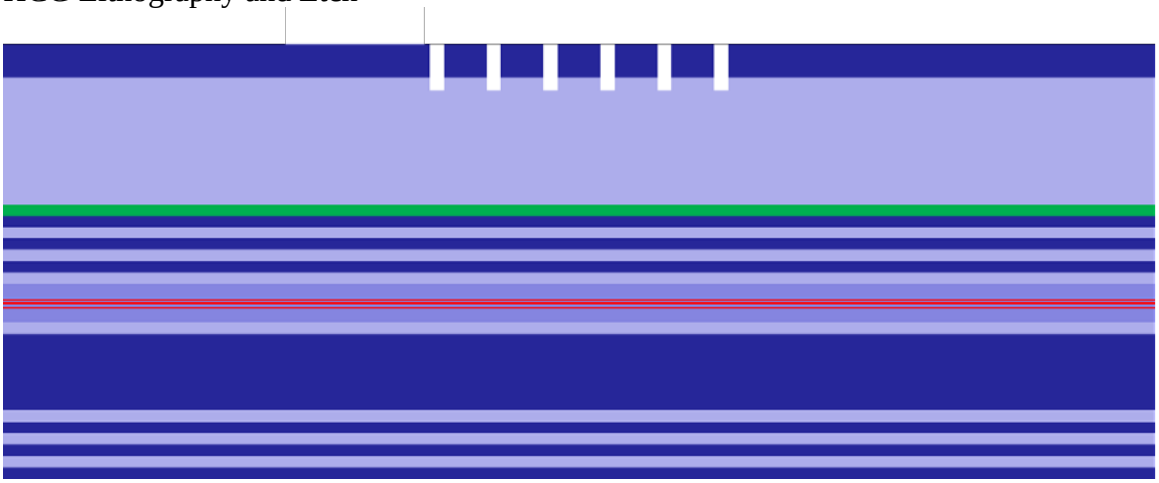
Next, the tuning mesa is formed. The pattern is defined with contact lithography using 1 um i-line photoresist. The mesa is etched using H_2SO_4:H_2O_2:H_2O 1:8:160, which etches GaAs at a rate of 0.26 micrometers per minute and has extremely high selectivity against the InGaP etch stop. The tuning mesa is square and rotated 45 degrees away from the chip edges in order to have identical etching on all edges of the mesa.

The oxidation mesa is formed using a similar process. The pattern is defined using i-line lithography. The etch stop is removed using 37% HCl, which etches InGaP over GaAs with high selectivity. The mesa is etched using the same dilute piranha (1:8:160).

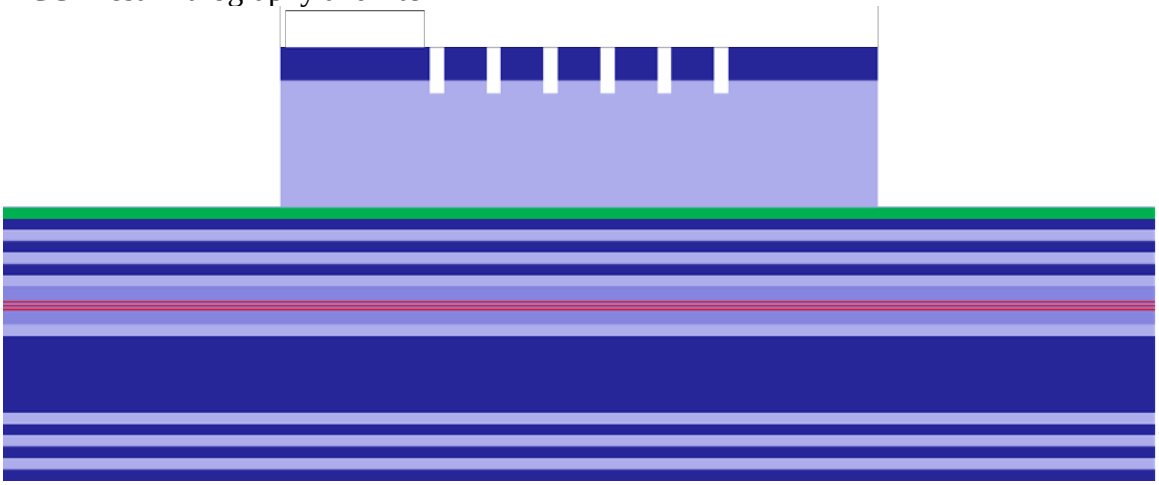
The chip is oxidized at 420 degrees in an N_2 + H_2O ambient. The $Al_{0.98}Ga_{0.02}As$ aperture layer is oxidized to form a porous Al_2O_3 layer that extends from the edge of the oxidation mesa toward the center of the device. The oxidation is timed to control the width of the resulting aperture, which is targeted at 6 μm. The oxidation aperture is inspected with an InGaAs CCD. A range of mesa sizes from 60 to 64 um is drawn on the oxide mesa mask in order to produce intentional variation in the size of the oxide aperture.

Contacts are defined using a liftoff process. First, LOR 5A is applied to the chip and cured at 185C. Next, i-line resist is coated on top of the LOR 5A. The chip is exposed using a contact aligner and is developed in OPD 4260 TMAH-based developer. The pattern is defined in the i-line resist, and the LOR 5A is etched away to produce a reentrant photoresist profile. Two contact regions are defined: the tuning contact is on top of the HCG layer, and the laser contact is

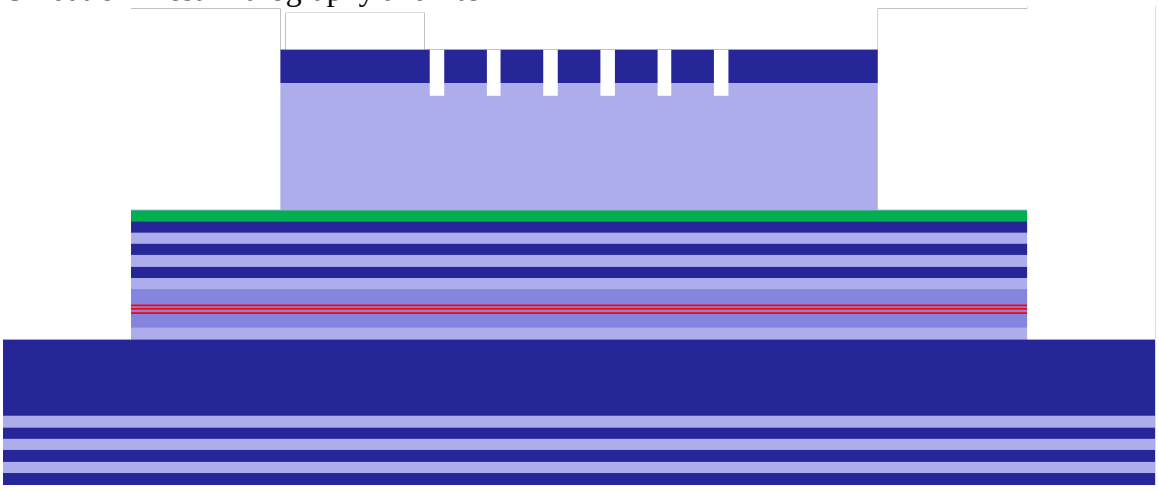
a) HCG Lithography and Etch



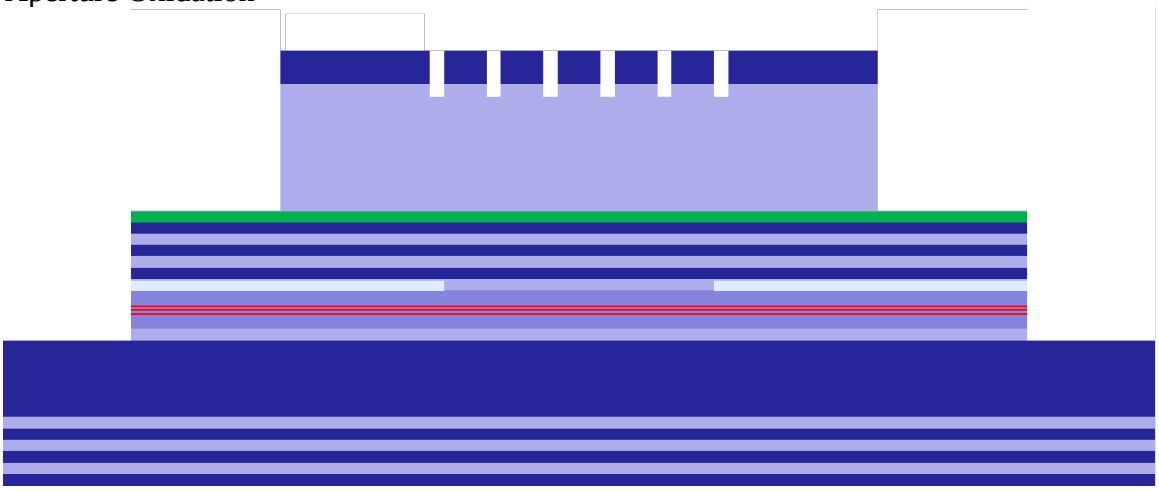
b) HCG Mesa Lithography and Etch



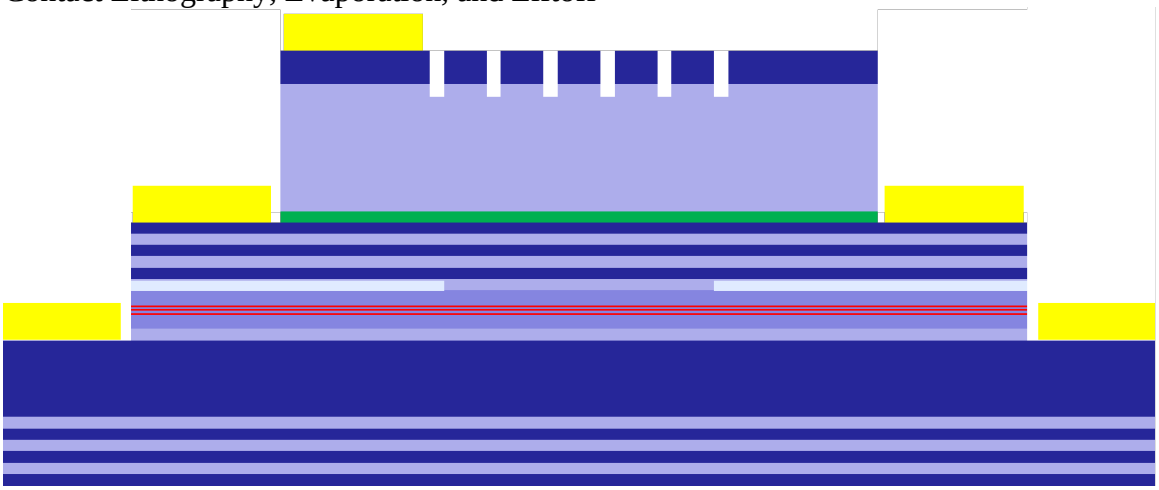
c) Oxidation Mesa Lithography and Etch



d) Aperture Oxidation



e) Contact Lithography, Evaporation, and Liftoff



f) MEMS Release Lithography, Etch, and Critical Point Drying

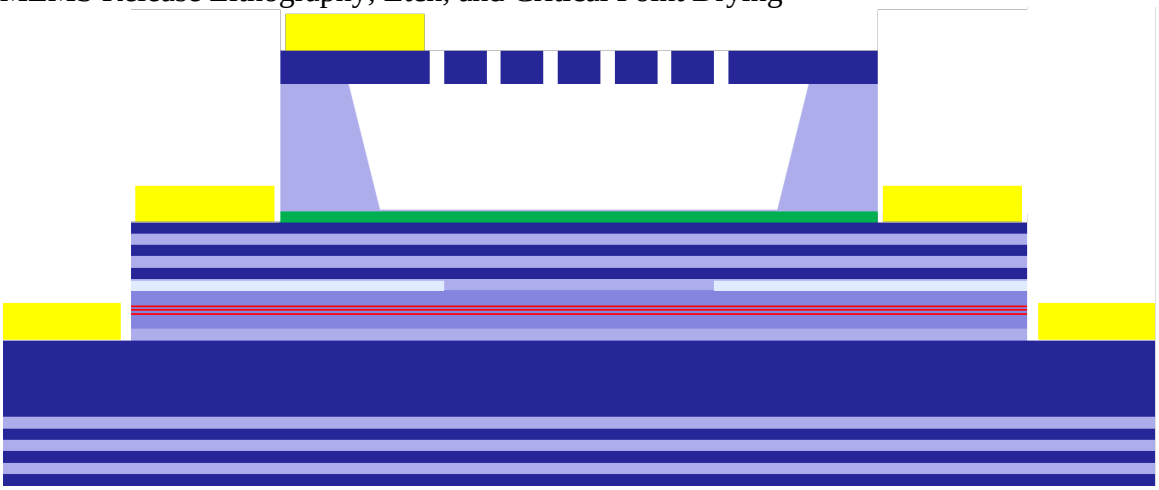


Figure 3.9. Cross-section diagrams for the fabrication process used to produce ACD MEMS-tunable HCG VCSELs.

placed on top of the oxidation mesa. Electron beam evaporation is used to deposit 5 nm Ti and 250 nm Au on the front side of the wafer, and then again on the back side of the wafer. Liftoff is performed by immersing the coated chip in Remover 1165 (NMP-based photoresist stripper), which dissolves the LOR 5A and i-line photoresist. A pipette is used to blow the lifted Ti/Au foil off of the chip.

Finally, the HCG is released from the substrate. The HCG region is exposed using contact lithography in S1818 photoresist. The back side of the chip is also coated in S1818. The chip is then immersed in a highly selective buffered citric acid and peroxide etchant. This etch removes GaAs with a selectivity of 1000:1 against $Al_{0.60}Ga_{0.40}As$. The GaAs sacrificial layer is removed from the area beneath the HCG and MEMS supports. The chip is dried in a critical point drier to avoid MEMS stiction that would render the device useless. A successfully released HCG and a finished tunable VCSEL is shown in Figure 3.10.

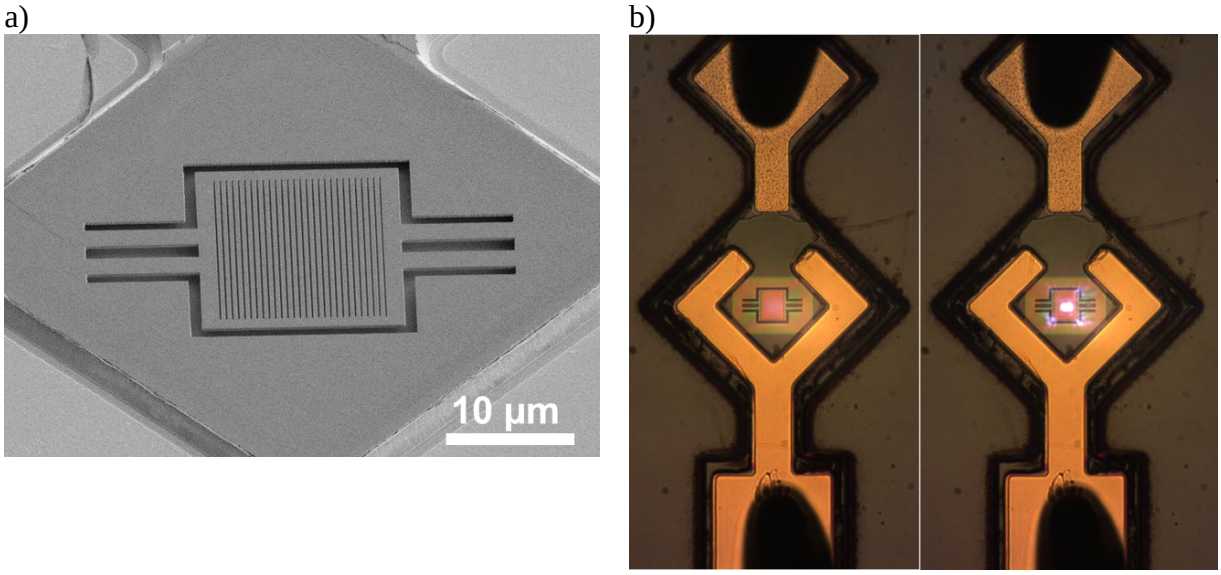


Figure 3.10. (a) A scanning electron microscope micrograph of the finished tunable HCG reflector. The edges of the HCG mesa and laser contact are visible near the edge of the frame. (b) Microscope image of the finished devices. The contact at the top of the image is used to bias the MEMS junction, while the contact at the bottom of the screen is used to drive the VCSEL. The device is pictured below and above threshold. Reprinted with permission from [22].

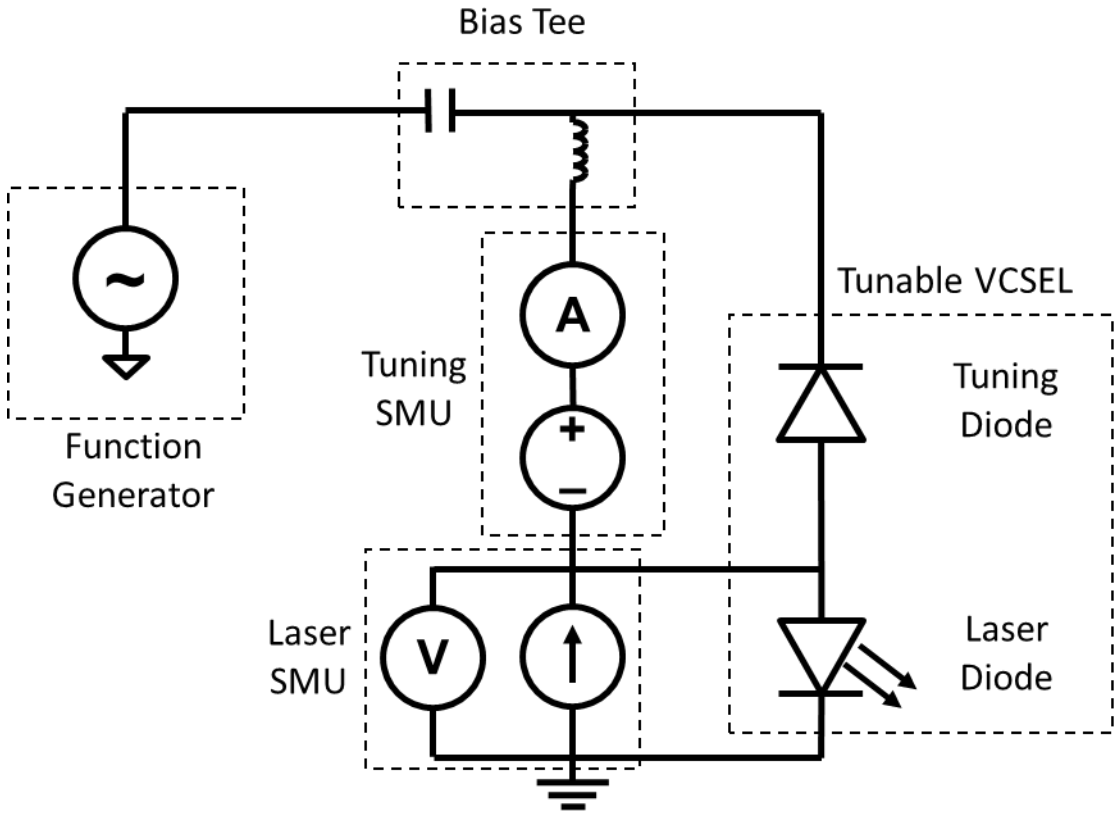


Figure 3.11. Driving circuit for tunable VCSEL measurements. Two source-meter units (SMUs) are used to apply a DC current through the laser diode and a DC voltage across the tuning diode. The tuning diode is reverse biased in order to support a large tuning voltage with a low leakage current. A bias tee is used to couple an AC voltage into the tunable VCSEL contact, facilitating mixed-signal MEMS biasing for resonant excitation.

3.9 ACD Device Performance

The tunable VCSELs produced using this process can be modelled as a pair of diodes with a common anode. The two diodes are the laser diode (LD), which is forward biased in order to produce a carrier inversion in the quantum wells in the depletion region. The tuning diode (TD) is reverse biased in order to produce a large MEMS bias voltage. The reverse breakdown voltage of the TD is approximately 35V. The MEMS is designed so that the mirror can be displaced by $\lambda/2$ with a voltage that is lower than breakdown.

The first test of the performance of any VCSEL is a light-current-voltage (LIV) measurement. In this device, the current through the LD is swept from 0 mA to 10 mA using a source-measure unit. At each current setpoint, the voltage across the diode is measured with the driving SMU and the light output is measured with a large area photodetector. The light being absorbed by the large area photodetector is converted to photocurrent, which is measured by a second SMU. This measurement shows the threshold current, slope efficiency, and thermal characteristics of the device at a glance.

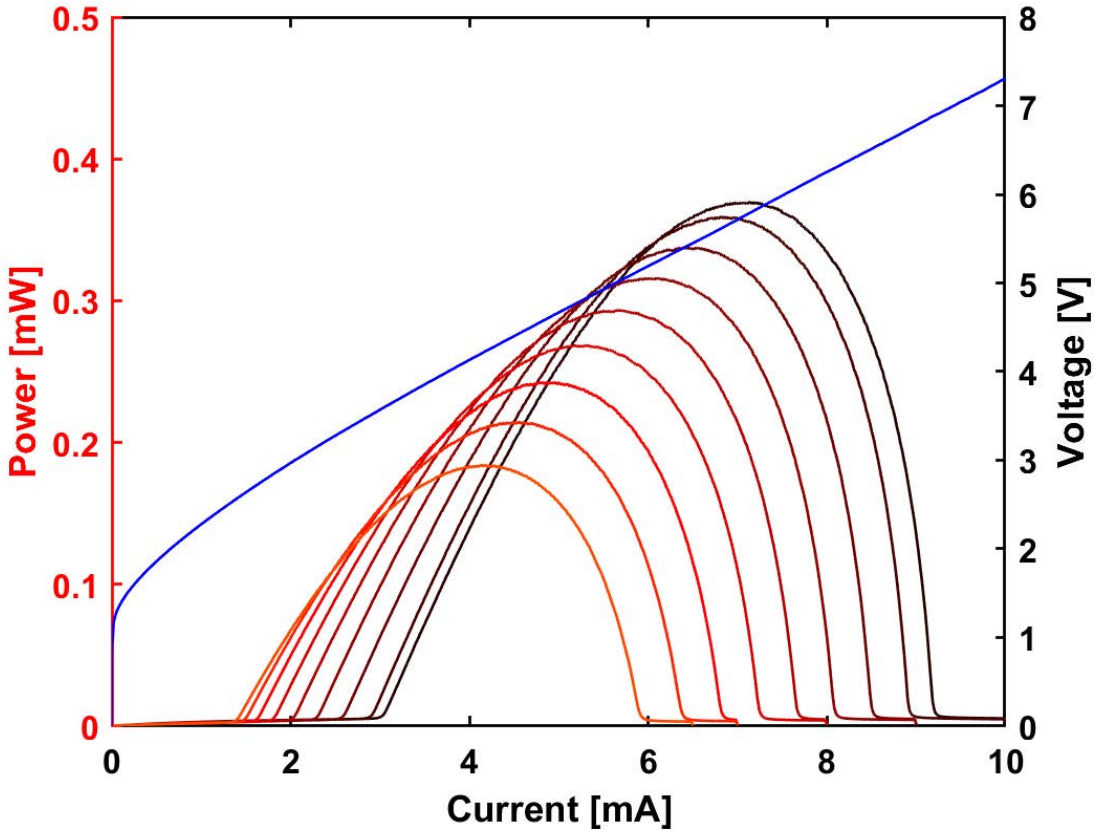


Figure 3.12. LI curves measured on a tunable VCSEL with no tuning bias. The VCSEL can reach threshold across the entire tested range of chuck temperatures from 20°C to 100°C. As temperature increases, the peak power and threshold current both decrease. The voltage is measured at 20°C, and is indicative of a high series resistance in the VCSEL and in the measurement setup.

The LIV curves for the ACD tunable VCSEL are shown for a variety of chuck temperatures in Figure 3.12. The black curve shows the light output at room temperature (20°C) and the red curve shows the light output at 100°C. There are two strong trends versus temperature. First, the threshold current of the laser decreases with increasing temperature. When the tuning mirror is sitting at its rest position, the resonant wavelength of the VCSEL cavity is much longer than the peak wavelength in the quantum well gain spectrum. As temperature is increased, the wavelength of the gain peak and the cavity resonance both redshift, but the gain peak shifts at a greater rate. At the red edge of the tuning range, this results in a higher gain for the same drive current, which in turn causes a reduced threshold current. Second, the thermal rollover happens faster at a higher chuck temperature, resulting in a lower peak power output. This is the other side of the same thermal effect that reduces the drive current. As the quantum well temperature is pushed even higher by Joule heating, the peak of the gain spectrum shifts beyond the cavity resonance, and the device is unable to reach threshold. The voltage is high due to series resistance introduced by unoptimized doping and contact metallurgy.

After confirming the performance of the VCSEL with no tuning bias, the tuning capabilities of the VCSEL are tested. First, the LD is pumped with 5 mA, with no bias applied to the TD. This produces a laser peak at 1070 nm. As the TD bias is increased to 16.7 V, the emission blueshifts down to 1023.2 nm. At this wavelength, the next Fabry-Perot resonance begins to compete with the dominant peak. The next FP resonance can be made dominant by applying a larger TD bias, increasing the threshold material gain for the lower wavelength resonance, or by increasing the LD drive current, which shifts the gain peak toward the longer wavelength FP mode. The maximum wavelength of 1096.3 nm is reached by increasing the LD drive current to 7 mA and decreasing the TD bias to 15.5 V. In order to get back to the starting wavelength, the voltage is increased to 17 V and the chuck temperature is increased to 45°C. The complete tuning range of 73.1 nm corresponds to a fractional tuning range of 6.9%, which was the record for an electrically pumped laser at the time of discovery.

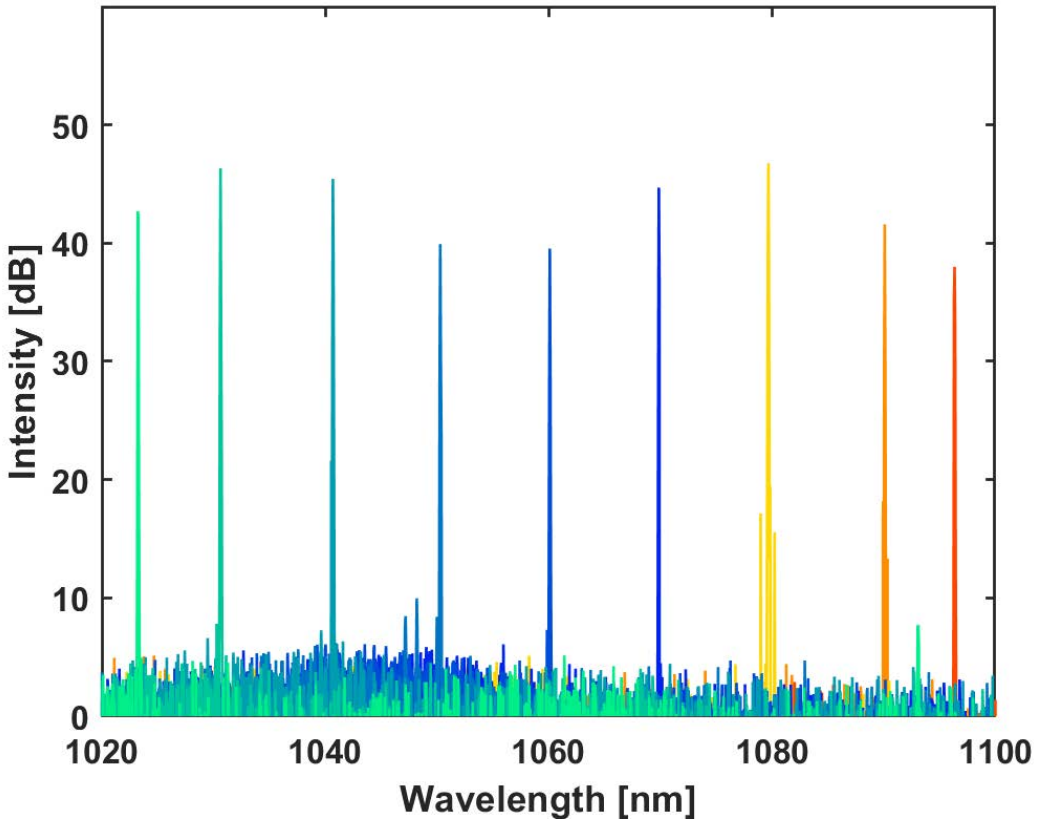


Figure 3.13. Static tuning spectrum of a 1060 nm ACD VCSEL. The range between 1023.2 nm and 1070 nm is accessed with electrostatic tuning. Current tuning and temperature tuning are used to cover the upper end of the spectrum. The full static tuning range is 73.1 nm, which corresponds to a fractional tuning range of 6.9%. A side-mode suppression ratio of more than 20 dB is maintained across the whole range. Reprinted with permission from [22].

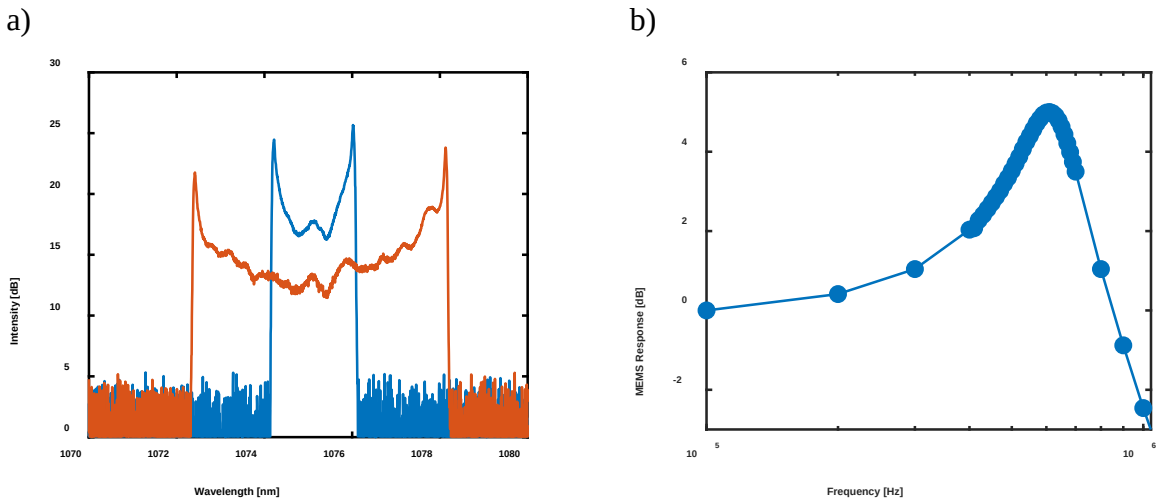


Figure 3.14. The resonant frequency of the MEMS is determined by measuring the frequency response. A large DC bias and a small DC bias is applied to the tuning diode using the bias tee. The excitation frequency is swept from 100 kHz to 1 MHz, and the bandwidth of the VCSEL (a) is measured at each frequency. The blue and red curves show the swept spectrum at 100 kHz and 610 kHz, respectively. The frequency response (b) shows a resonance at 610 kHz that enhances the measured bandwidth by a factor of 3.

The VCSEL was designed with a zero-displacement wavelength of approximately 1090 nm, but the measured zero-displacement wavelength of the statically tuned VCSEL was much shorter, which indicated the mirror was being displaced into the cavity with no applied bias. Using SEM inspection, it was found that the HCG MEMS has a thin residue that will charge and darken under an electron beam. Test samples showed that this residue is deposited during the RIE process that etches the grating. During the etch, the $SiCl_4$ deposits a thin layer of silicon on the sidewalls of the PMMA, which oxidizes upon exposure to air.

A second batch of ACD VCSELs from the same wafer was fabricated with a slightly modified process: prior to dissolving the PMMA, the chip is immersed in buffered HF to remove the Si residue. Under SEM inspection, there is no visible residue left behind with this process. Upon testing, it was found that the laser turns on at 1089.6 nm as expected.

The second batch of ACD VCSELs was patterned with a stiffer MEMS. Using a large TD bias of 31.5 V, the wavelength of the VCSEL can be electrostatically tuned down to 1073.6 nm. In order to reach beyond this wavelength, resonant MEMS tuning is leveraged [36]. If the MEMS is driven at its resonant frequency, it can be driven to much larger displacements since the peak displacement and peak voltage are out of phase with one another. The measurement circuit shown in Figure 3.11 uses a bias tee to apply an arbitrary AC voltage along with a DC bias.

First, the resonant frequency of the MEMS is measured with a frequency sweep. The TD is biased with a DC voltage of 30 V and an AC voltage of 1 V_{PP}, while the LD is biased with a

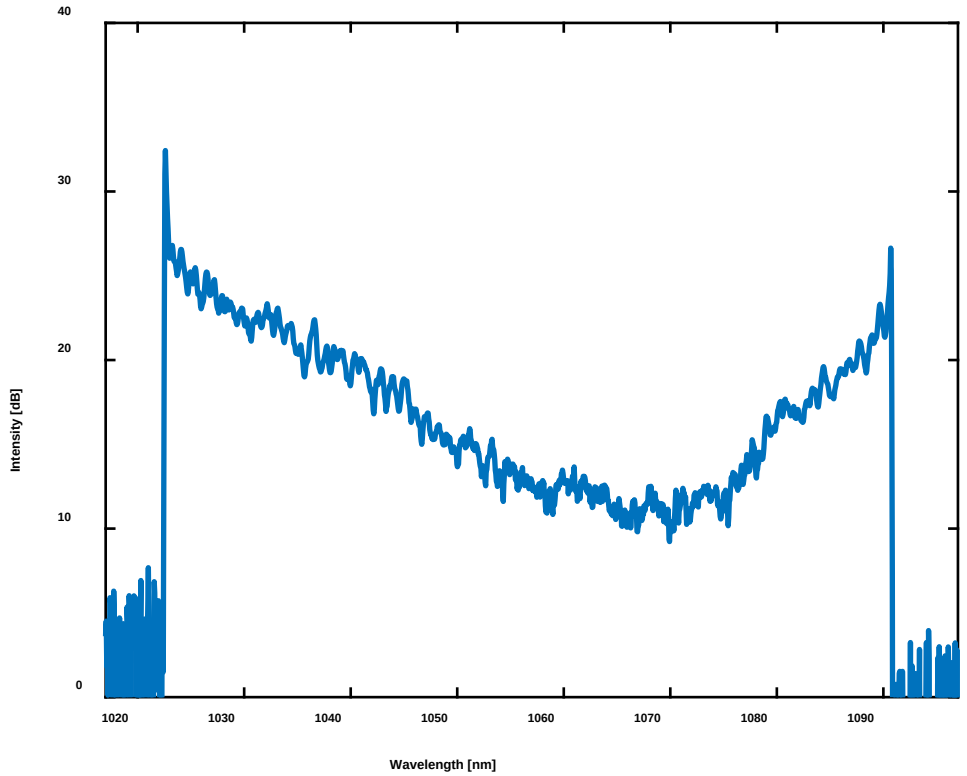


Figure 3.15. The ACD VCSEL with improved fabrication process resonates at a wavelength of 1089.6 nm with no tuning bias. The VCSEL can be tuned to 1073.6 nm with a DC tuning bias of 31.5 V, which is approaching the breakdown voltage of the junction. The MEMS is actuated at its resonant frequency of 550 kHz by adding an AC voltage of 10 V_{pp} to the tuning contact. The swept spectrum of the ACD tunable VCSEL reaches from 1022.6 nm to 1090.7. Reprinted with permission from [21].

current of 5 mA. The frequency is swept from 100 kHz to 1 MHz, which includes the theoretically calculated mechanical resonance. At each frequency, the bandwidth of the optical spectrum is measured with an optical spectrum analyzer. This bandwidth corresponds to the magnitude of the displacement of the MEMS in response to the AC signal. The response shows a resonance at 610 kHz with a bandwidth enhancement of 3.16 times the low-frequency response.

Resonant excitation is used to probe the swept tuning range of the ACD VCSEL with the improved process. The VCSEL is turned on at 1089.6 nm with 4.5 mA through the LD. A DC bias of 31.5 V is applied to the TD, shifting the wavelength to 1073.6 nm. Finally, an AC bias of 10 V_{PP} at 550 kHz is added to sweep the wavelength across the range from 1022.6 nm to 1090.7 nm. This 68.1 nm tuning range corresponds to a fractional tuning range of 6.5%, which is the highest swept tuning range demonstrated for an electrostatically actuated tunable VCSEL.

In order to verify the low threshold of the ACD VCSEL design, the threshold current for each wavelength was measured using the same experimental setup. For this measurement, the TD bias is set to sweep the entire tuning range: 31.5 V DC + 10 V_{PP} AC at 550 kHz. The current through

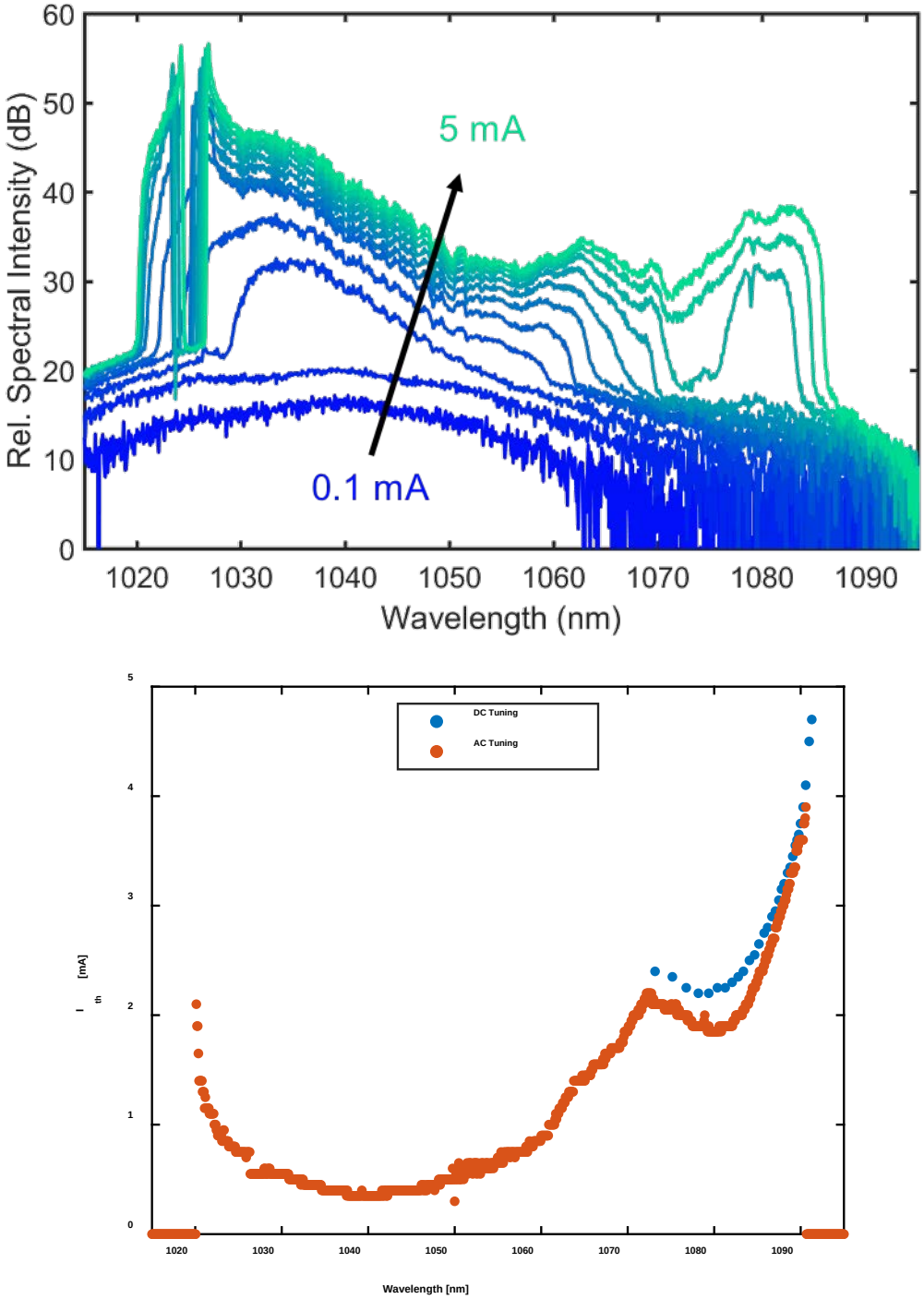


Figure 3.16. In order to measure the threshold current as a function of wavelength, a series of spectra is measured. First, the voltage across the tuning diode is set to sweep the VCSEL across the full wavelength spectrum. Next, the current through the laser diode is increased from 0.1 mA to 5 mA. At every point, the spectrum of the tunable VCSEL is measured. The threshold current of the VCSEL is extracted at each wavelength by finding the sudden increase in slope that corresponds to laser threshold. The measurement is confirmed with DC tuning for the accessible range of wavelengths. Reprinted with permission from [21].

the LD is then stepped from 0.1 mA to 5 mA, and the spectrum is measured at each bias condition. For each wavelength, the threshold is then extracted by finding the change in slope efficiency that corresponds to the threshold current (I_{th}) of the laser. As predicted by the transfer matrix calculations, the threshold is very low close to the tuning center with a minimum of 0.35 mA at 1040 nm. Toward the edges of the tuning spectrum, I_{th} increases to approximately 4 V. At 1075 nm, there is a peak in the threshold current. This corresponds to a change in the dominant transverse mode of the VCSEL. At the peak wavelength, the two modes compete for gain, which causes both to have a higher threshold. For a portion of the spectrum, this measurement is verified by taking DC tuning LIV measurements. This technique can only be extended down to 1073.6 nm, since larger voltages would cause the MEMS to collapse. The shape of the curve follows the swept threshold measurement with a slightly higher measured threshold.

3.10 Conclusion

The calculations and measurements presented in this section show a practical way to increase the tuning range of a tunable VCSEL. The optical energy distribution in a tunable VCSEL is dictated by the behavior of the semiconductor and air cavities. By designing a semiconductor cavity that is antiresonant at the center wavelength, the field is forced into the air cavity at the center of the tuning range and the semiconductor cavity at the edge of the tuning range. This maximizes the FSR of the VCSEL at the tuning edges – where competition between FP modes is possible – and maximizes the tuning slope of the VCSEL at the tuning center by coupling the energy more closely to the tuning reflector.

The ACD cavity design is experimentally demonstrated to double the electrostatic tuning range of a comparable SCD VCSEL from 34 nm [20] to 68.4 nm. An even wider range of 73.1 nm is reachable if the additional control parameters of chuck temperature and current injection are used to redshift the emission wavelength. Counterintuitively, the antiresonant cavity design does not significantly increase the threshold current of the device.

The ACD cavity design can be easily combined with other cavity-shortening methods, including using a $\lambda_c/2$ cavity, removing the upper DBR [37], and using an oxidized GaAs/Al_2O_3 lower DBR [19], to further increase the FSR of a tunable VCSEL. The design principle is also applicable to optically pumped devices, which do not need contact or oxidation layers, for an even shorter cavity and longer FSR.

4 Oxide Spacer High-Contrast Grating VCSELs

4.1 High-Power VCSEL Arrays

While the power output of a single VCSEL is smaller than the output of a single edge-emitting laser, the VCSEL architecture is convenient for forming integrated VCSEL arrays. Since the placement of a laser is defined lithographically, the single VCSEL process is scalable to hundreds of emitters just by using an appropriate mask set. The first high-power VCSEL array was demonstrated in 1998 [38], and its application to 3D sensing (LIDAR) was suggested in 1999 [39]. In the past decade, a confluence of several research fields has led to high competition in producing high power, high efficiency VCSELs for face identification and gesture recognition. First, VCSEL research and development has produced higher efficiency devices with denser integration, making the devices attractive for handheld applications. Second, process technology development has improved uniformity and scaled VCSEL processes from 2 inch wafers to 6 inch wafers, reducing fabrication costs and unlocking more advanced lithography technologies used for silicon at 6 inch nodes. Finally, computational resources have become ubiquitous, enabling the execution of computer vision algorithms in real time on a smartphone. These combined technologies have created market forces that are driving a renaissance in VCSEL development.

VCSEL arrays are primarily used in TOF and SL 3D sensing systems. In TOF, the VCSEL array is simply used as a high efficiency illuminator, which can be modulated at iTOF frequencies. The emission from the VCSEL is passed through an engineered diffuser, which creates a uniform far-field pattern from the discrete elements. Generally, this pattern is a rectangle in angular dimensions. In SL, the VCSELs are used to define discrete angles in an illumination pattern. When the pattern is used to illuminate a 3D object, the pattern is distorted proportionally to depth. With knowledge of the reference pattern, an algorithm can use the distorted pattern to construct a 3D model of the illuminated scene. If the pattern produced by the VCSELs deviates too far from the reference pattern expected by the algorithm, then the algorithm will be unable to reconstruct the depth profile.

The primary figures of merit for VCSEL arrays are the wall plug efficiency, divergence angle, emitter pitch, and uniformity. The wall plug efficiency is a combined measure of many important parameters of a VCSEL, including the threshold current, slope efficiency, and electrical resistance of an array. In order to achieve a high wall plug efficiency, it is important to optimize the mirror loss of the cavity so that the device has a low threshold, but enough light escapes the top mirror for a large slope efficiency. The electrical performance must also be optimized by designing the doping profile [40] of the laser to give low resistance without introducing excessive free carrier absorption [41]. The divergence angle of a VCSEL is determined by the shape of the transverse modes supported by the cavity, which depend on the effective index contrast between the core of the VCSEL and the optical cladding defined by oxidation. Higher order modes result in a higher divergence, which can leave a dark spot in the center of the illuminated field or increase the spot size of an SL pattern. The emitter pitch is also an important factor in the resolution of SL applications. As shown in Equation *2.27*, placing emitters closer together allows a higher lateral resolution. The emitter pitch is generally limited by the critical dimensions on the mask. Area must be reserved for the optical aperture, the ohmic contacts, the

oxidation trenches, and for overlay tolerance. As these parameters are pushed to smaller values, the uniformity of the array will suffer. Smaller contacts cause higher resistance, which hinders current distribution. Narrower oxidation trenches are more sensitive to oxidation conditions, which cause higher aperture nonuniformity. Varying trench dimensions – which can occur at the edges of uniform arrays and at any point in a random array – will cause variation in etch depth and thus in oxidation rate.

4.2 High Contrast Gratings in VCSEL Arrays

Many features of a high contrast grating would be a benefit in the creation of high power VCSEL arrays for 3D sensing. The introduction of a designable surface creates the opportunity to reduce divergence angle [42], collimate the beam [15], steer the output [43], and control polarization [12] – as an ensemble device or at the device level. For example, it is very straightforward to produce a single polarization with a 1D HCG. This creates the opportunity to produce a high power VCSEL array with a linearly polarized output. If a polarizer is also used on the detector in the 3D sensing system, then ambient light can be reduced in comparison to the light from the illumination source, increasing the signal to noise ratio. Alternatively, each VCSEL could be assigned a different polarization to introduce randomness without hurting the uniformity of the emission by changing the loading of the trench etch. Finally, a small subset of VCSELs could be assigned an orthogonal polarization to the rest of the array, allowing for simple centering of the reference pattern.

The other advantage of the HCG VCSEL architecture is epitaxy cost. In high volume manufacturing, the cost of the VCSEL epitaxy is about one third of the total cost of the device. An HCG reflector can be one quarter the thickness of an equivalent DBR, which reduces the total epitaxial thickness by one third. The tradeoff that comes along with this reduction in epitaxial complexity is the need to pattern a subwavelength grating, but the saved epitaxial thickness is more expensive than the operating cost of a deep UV stepper due to the high throughput of the latter.

In order to integrate an HCG into a useful VCSEL array, the layout area of the HCG needs to be minimized. This is difficult for an air spacer, which must have some support outside of the active region of the grating, as seen in Figure 3.10. Furthermore, the air spacer HCG has additional processing challenges associated with it. To prevent MEMS collapse, the HCG release process must be performed at the very end of the process, after wafer thinning. Extreme care must be taken during dicing and packaging, which drives up the cost of the device. For these reasons, a solid spacer is preferable for an HCG VCSEL array.

Solid spacer HCGs have been produced in the past. Some have been implemented in SOI [44], but this requires a bonding process to add the rest of the VCSEL structure to the device, which is plagued with yield and reliability issues. HCG layers can also be created by depositing a low index dielectric and a high index dielectric or semiconductor using PECVD or evaporation. This process requires two extra deposition steps with extremely high accuracy and precision. In this work, we leverage the selective oxidation of AlGaAs to produce a low index spacer from a layer that is monolithically integrated in the MOCVD epitaxy that is used to produce the rest of the VCSEL.

4.3 Selective Oxidation of AlGaAs

Modern VCSELs utilize the selective wet oxidation of AlGaAs to define an electrical and optical aperture at the center of a VCSEL. During the epitaxy, a thin oxide aperture (OA) layer with an Al mole fraction higher than 98% is included near the quantum well region. During fabrication, an etch process such as wet etching, reactive ion etching (RIE), or inductively couple plasma (ICP) etching is used to expose the edges of the oxide layer. After thoroughly cleaning the substrate, the wafer is loaded into an oxidation furnace where the etched structure is exposed to water vapor at a high temperature. A family of reactions take place [45], [46]:

$$2AlAs + 6H_2O = Al_2O_3 + As_2O_3 + 6H_2$$

$$As_2O_3 + 3H_2 = 2As + 3H_2O$$

$$As_2O_3 + 6H = 2As + 3H_2O$$

The first reaction oxidizes AlAs to form both Al_2O_3 and As_2O_3. The second and third reactions volatilize the As_2O_3, leaving behind a porous Al_2O_3. Since the water vapor does not need to diffuse through an amorphous layer, the oxidation depth progresses linearly as a function of time. This is in stark contrast to Si oxidation, where the oxidation rate is strongly dependent on the rate of diffusion through the amorphous SiO_2 for thick films. If the oxidation of AlGaAs is performed in an O_2 ambient, then the As_2O_3 will not be reduced and volatilized, and the oxidation rate will decrease to zero at a depth of tens of nanometers.

The oxidation of the OA layer occurs from the edge of the etched region toward the center of the VCSEL to a depth of approximately 10 microns, depending on the layout. The oxidation process creates two important differences between the oxidized Al_2O_3 and the unoxidized AlGaAs. First, the Al_2O_3 is insulating instead of semiconducting. This forces the current injected through the contacts to flow through the center of the device, which creates a high current density. Second, the Al_2O_3 has a much lower refractive index (1.6 versus 3.0). The higher refractive index in the unoxidized core confines the light in the transverse direction, guiding it into the region with high current density.

The oxidation rate of AlGaAs is exponentially dependent on the mole fraction of Al. As a result, the other layers in the VCSEL structure will oxidize much more slowly than the OA layer, which reduces series resistance by leaving a wider conductive area. If the top and bottom layers of the VCSEL are composed of GaAs, they can be put into the furnace unprotected due to their near-zero oxidation rate.

The oxide spacer HCG VCSEL leverages the existing wet oxidation step to produce a low index HCG spacer simultaneously with the OA. The HCG epitaxy must include a low-Al HCG layer on top of a high-Al oxide spacer (OS) layer. The grating is etched through the HCG layer and into the OS layer. When the VCSEL is oxidized in a furnace, the gas diffuses through the openings of the grating and oxidizes the underlying OS layer. Since the HCG layer is composed of a low-Al material, it does not oxidize significantly. At the end of the process, a high index grating is left on top of a low index cladding, satisfying the requirements for a high contrast grating.

a) b)

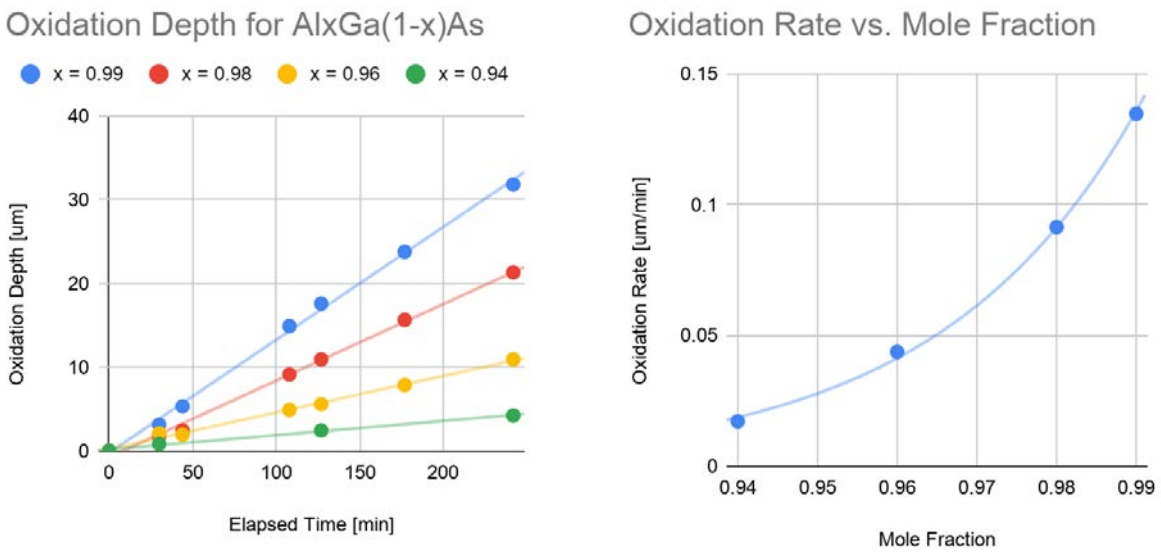


Figure 4.1. The mole fraction of $Al_xGa_{1-x}As$ has an exponential influence on the oxidation rate of the material. Test structures containing mole fractions between 0.94 and 0.99 were grown with MOCVD, etched using dilute Piranha solution, and oxidized at 435°C. The oxidation depth was monitored in real time with an in-situ IR microscope. The oxidation rate is extracted with a linear fit of the measured data.

Since the oxide formed through the AlGaAs oxidation process is porous, mechanical stability is a large concern. It has been shown that the oxide of a pure AlAs layer is prone to delamination during thermal processing, but adding even 2% of Ga to the structure reduces the risk significantly [45]. In order to prevent delamination of the oxide spacer HCG, the Al mole fraction must be reduced to the lowest possible value that will still fully oxidize.

In order to determine the ideal composition of the oxide spacer, several experimental test structures were grown using MOCVD that contained $Al_xGa_{1-x}As$ layers enclosed by GaAs. The epitaxial test wavers were patterned with 50 um stripes, and etched using H_2SO_4:H_2O_2:H_2O 1:8:160. After cleaning the photoresist off the wafers, the samples were oxidized at 435°C and the oxidation depth was monitored with an in-situ IR microscope. The oxidation depth was recorded as a function of time, and the oxidation rate for each mole fraction was fit with a linear regression. As indicated in the literature [45], the oxidation rate shows an exponential dependence on mole fraction. Since the desired oxidation depth of the OS layer is up to a micron and the desired oxidation depth of the OA layer is more than 10 microns, it is safe to pick a composition of 0.94 for the OS layer and 0.99 for the OA layer. This ensures that the OS is fully oxidized when the OA reaches its target depth.

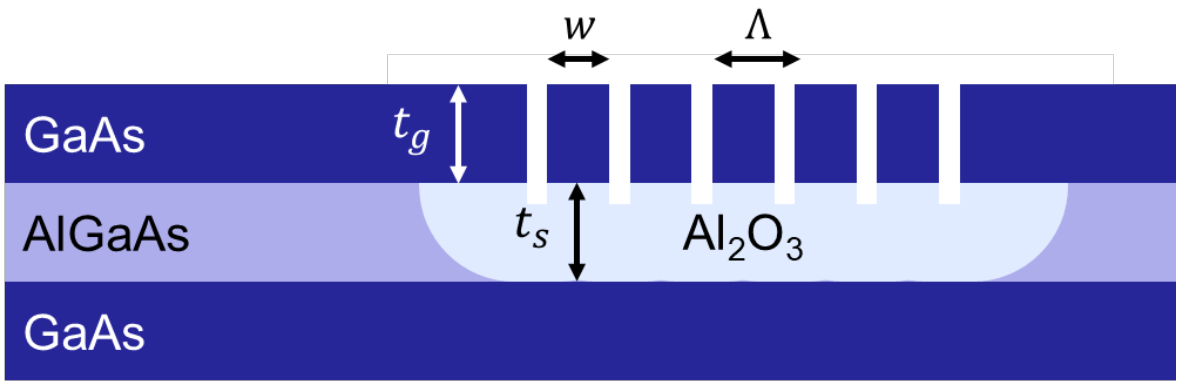


Figure 4.2. Schematic of an oxide spacer high-contrast grating (OS HCG). The GaAs grating is sitting on top of the fully oxidized Al_2O_3 spacer. The grating is parametrized by the refractive indices of the grating and spacer (n_g and n_s), the thickness of the grating and spacer layers (t_g and t_s), and the period and bar width of the grating (Λ and w).

4.4 Simulating the Oxide Spacer HCG

A schematic of an oxide spacer HCG is shown in Figure 4.2. The simulation domain for the OS HCG begins in the top semiconductor layer in the VCSEL epitaxy. There is a spacer with thickness t_s, which is assumed to be fully oxidized Al_2O_3 with $n_s = 1.6$. On top of the spacer, there is a GaAs grating with period Λ, bar width b, thickness t_g, and refractive index n_g.

First, the grating is designed to maximize reflectance at the VCSEL target wavelength of 980 nm when the spacer thickness is infinite when Λ is fixed to a similar value to the design of the tunable VCSEL HCG reflector. The structure is simulated using RCWA to calculate the power reflectance R into the zeroth grating order. It is found that the layer structure is capable of providing broadband R of more than 99.5% across a wide range of bar widths. This indicates a wide process window for the HCG lithography and etch process. The HCG only needs to provide high reflectance at the fixed resonance wavelength of the VCSEL, but a broadband mirror also gives a wide tolerance to the epitaxial variations that may shift the lasing wavelength. For a conservative proof of concept, the dimensions that yield the highest possible R are selected for lithography in a range of $w = 260\ nm - 290\ nm$.

Next, the minimum thickness for the OS layer is studied. For a fixed $\Lambda, w,$ and t_g, the power reflectance spectrum is calculated as a function of t_s. At very small values of t_s, optical power begins to be reflected into the first diffraction order, reducing the zeroth order reflectance. Even so, the structure is expected to give $R > 99.5\%$ at a spacer thickness of only 75 nm. There are two lobes in the reflectance as a function of spacer thickness. The two lobes are spaced by a thickness of $\lambda/2$, exhibiting the periodic behavior expected as the thickness of a layer in an optical stack is increased. The t_s values with the largest bandwidth are selected for fabrication: 130-170 nm and 430-470 nm.

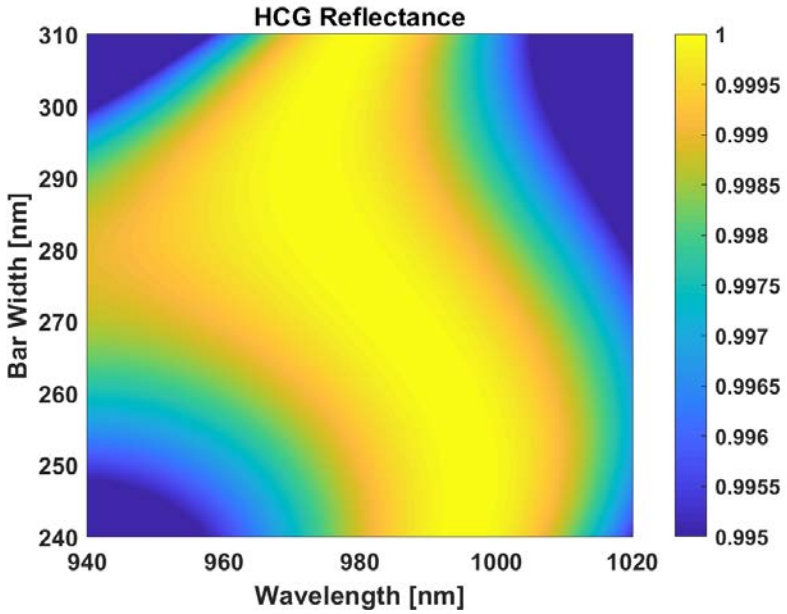


Figure 4.3. Simulated HCG reflectance for an infinite spacer thickness. The HCG reflector has a high tolerance to variation in bar width, remaining higher than 99.9% for the entire region between 250 nm and 310 nm. The grating provides broadband reflectance as well, spanning more than 80 nm for some designs. This makes the grating tolerant to variations in the cavity length due to variations in the epitaxy.

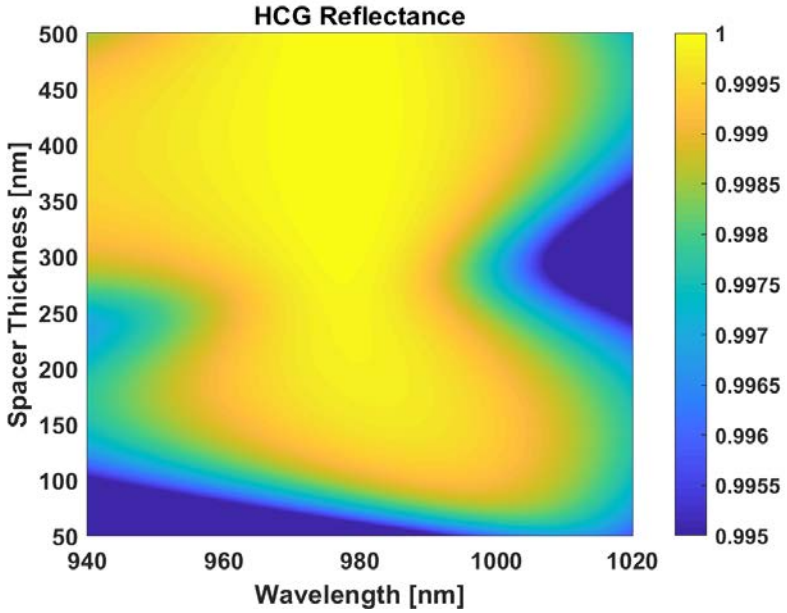


Figure 4.4. Simulated HCG reflectance for a finite spacer thickness. The OS HCG is capable of providing high reflectance down to a spacer thickness of 75 nm. Two high-bandwidth lobes are present centered around t_s of 150 nm and 450 nm. The difference between these two lobes is half of the design wavelength in $n_s = 1.6$, which is expected periodicity in an optical layer thickness.

4.5 Oxide Spacer HCG VCSEL Fabrication

Oxide spacer HCG VCSELs begin with an MOCVD grown epitaxial structure. From bottom to top, the structure consists of an AlGaAs/GaAs DBR, an active cavity containing InGaAs/GaAsP quantum wells, an OA layer, a current spreading and contact layer, the OS layer, and finally the HCG layer. For a short experimental loop, the region below the active cavity was grown by a contractor on a 4" GaAs substrate. The structure was capped with a thin layer of GaAsP. The substrate was diced into 1 cm x 1 cm chips, and a second epitaxial growth produced the top half of the structure. A thermal decomposition step was used to remove the GaAsP, and then the upper portion of the epitaxy was grown [47]. This allowed the researches to make changes to the quantum well, OS, and HCG layers without the time- and resource-intensive growth of the n-type bottom DBR.

After the epitaxy is complete, the HCG VCSEL is fabricated using a top-down fabrication process illustrated in Figure 4.5. First, the HCG is patterned with electron beam lithography. Three grating designs are used. Keeping period the same, the bar width is varied from 270 nm to 290 nm to test a range of designs with different reflectances. In order to improve write times for large arrays, the electron beam lithography process was modified from the tunable VCSEL process. Modifications included the use of a higher acceleration voltage (100 kV versus 50 kV), which facilitated the use of a higher beam current (1 nA versus 150 pA). The gratings were then etched using $SiCl_4$ RIE.

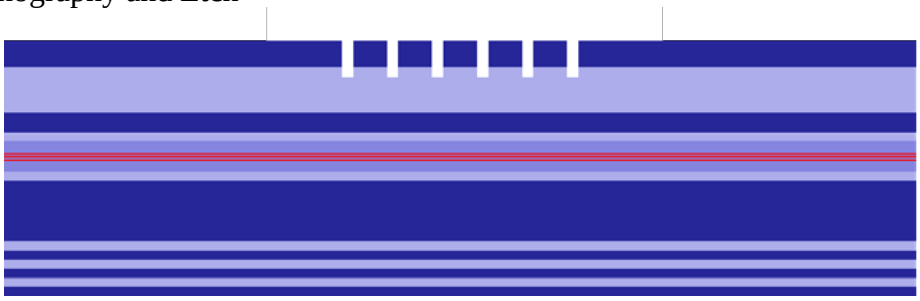
Since the OS layer is etched at a rate of several microns per minute in 5:1 buffered HF, a new method of etch residue removal was developed. Various removal methods, including dissolution in acetone and n-methyl-pyrrolidone and ashing in O_2 plasma were unsuccessful. Physical agitation, such as sonication and high-pressure solvent liftoff, can remove the residue. Sonication is undesirable since it can damage the strained quantum wells and reduce material gain. It was suspected that high-pressure solvent liftoff may delaminate the high contrast gratings, but it did not prove to be a problem. As such the high-pressure solvent liftoff technique was employed for post-etch cleaning. The results of the treatment are shown in Figure 4.6.

After etching and cleaning the grating, an HCG mesa is patterned with i-line photolithography with a contact mask aligner. The HCG mesa is etched with two selective etchants. First, the HCG layer is removed using citric acid and hydrogen peroxide. This etch stops on the OS layer, which is subsequently removed with 1:5 $HCl:H_2O$. The OS layer etch stops on the underlying p-type contact layer. The photoresist is removed using Remover 1165.

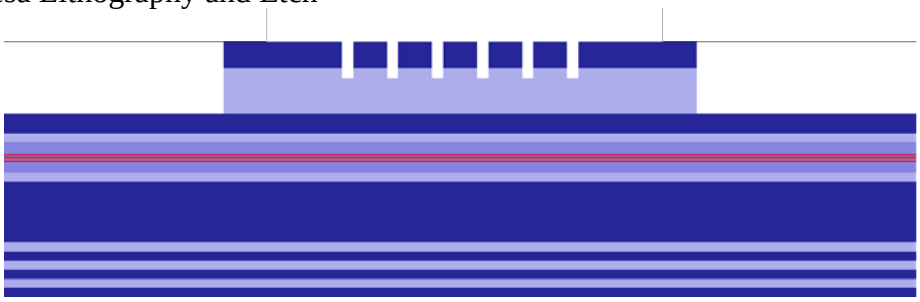
The oxidation mesa is defined next, using another i-line photoresist mask and chemical etching. Dilute piranha (1:8:160 $H_2SO_4:H_2O_2:H_2O$) is used to etch through the active cavity, and down to the n-type contact layer. The photoresist is removed using Remover 1165, and the sample is rinsed in IPA and H_2O.

Next, the wafer is oxidized in a specially designed VCSEL oxidation furnace with an IR microscope for monitoring the oxidation depth in-situ. As seen in Figure 4.7, the OA layer oxidizes from the edges of the oxidation mesa toward the center of the device. The OA decreases

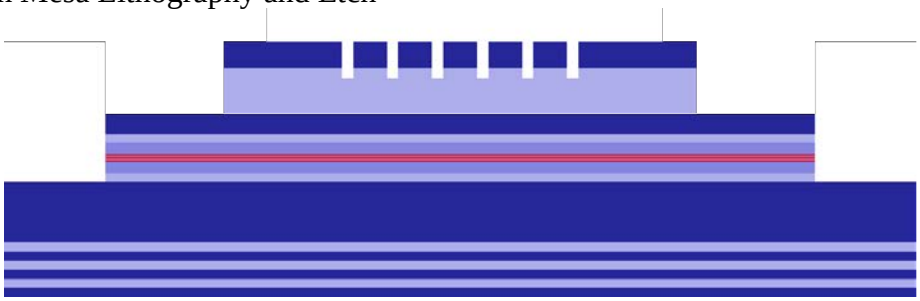
a) HCG Lithography and Etch



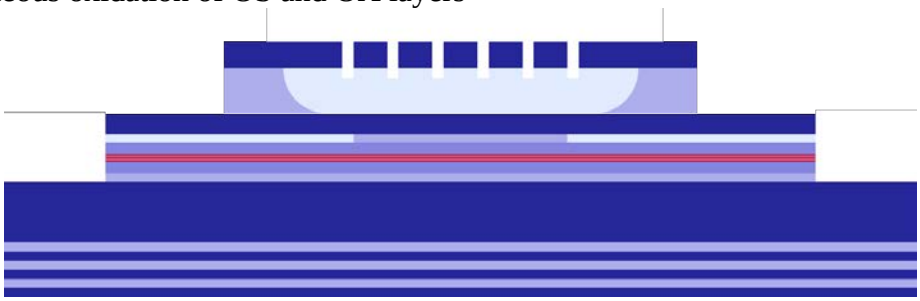
b) HCG Mesa Lithography and Etch



c) Oxidation Mesa Lithography and Etch



d) Simultaneous oxidation of OS and OA layers



e) Lithography, Evaporation, and Liftoff

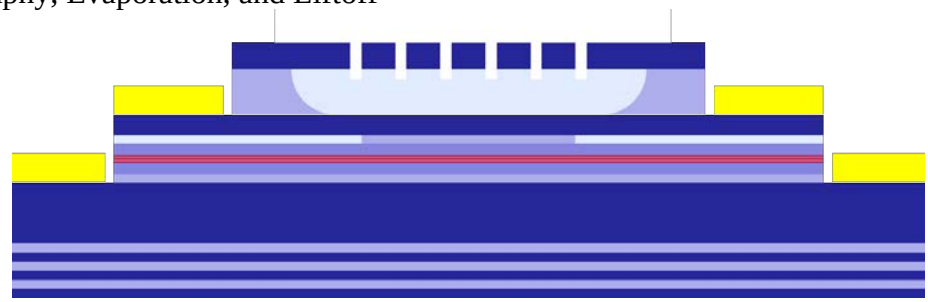


Figure 4.5. Fabrication cross-section drawings for an oxide spacer HCG VCSEL.

a) b)

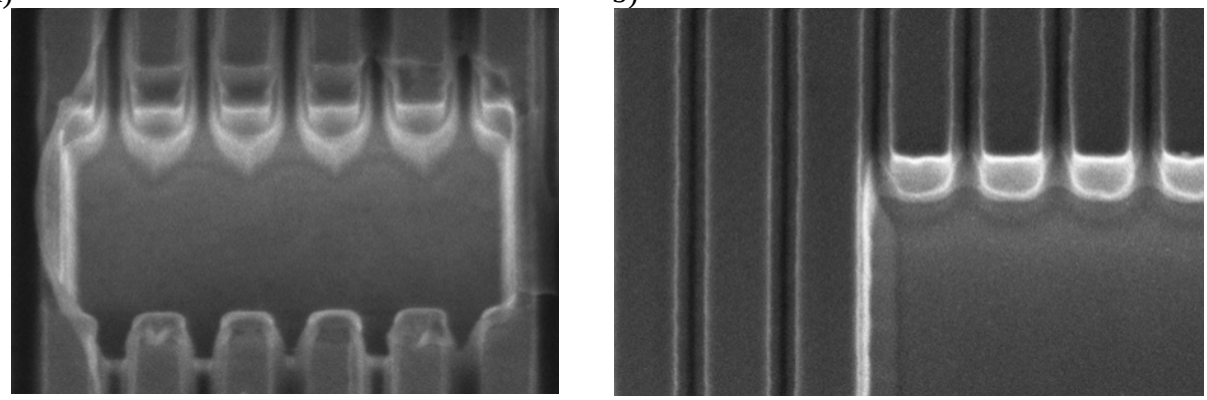


Figure 4.6. Tilt-view SEM micrographs showing the OS HCG cross section. In both images, the boundary between the HCG layer and OS layers are visible at the bottom of the etched trenches. (a) After the HCG etch using $SiCl_4$ RIE, a residual Si compound is left around the PMMA. When the PMMA is removed with an organic solvent soak, the insoluble Si compound remains on the bars, hindering oxidation when it falls across the gaps. (b) If a high-pressure organic solvent rinse is used, the Si compounds can be mechanically released from the edges of the gratings, leaving behind only the etched GaAs grating.

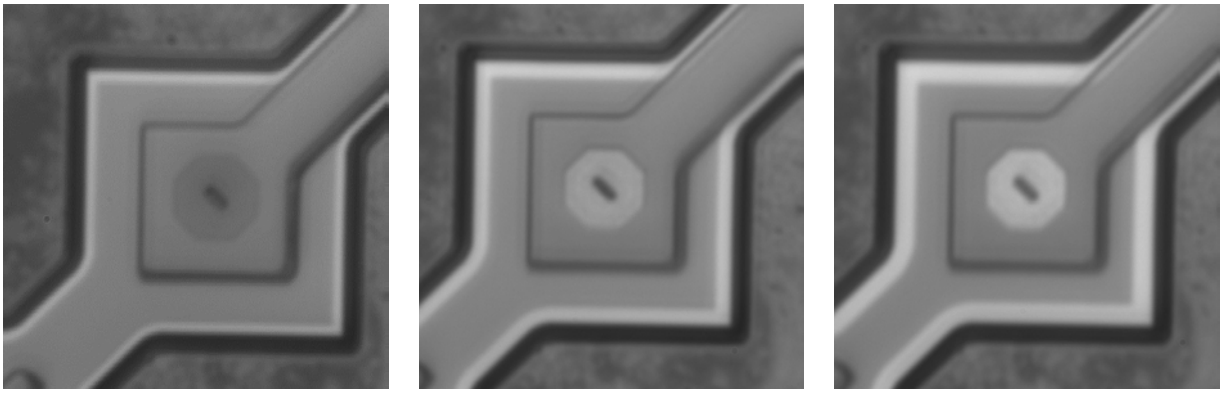


Figure 4.7. Oxidation progression of an OS HCG VCSEL. These IR microscope images were taken at an interval of one picture every 5 minutes. Two layers are oxidizing. At the edge of the square oxidation mesa, a light gray boundary progresses towards the center of the VCSEL as time progresses. This is the boundary of the oxide aperutre. At the center of the VCSEL, the octagonal HCG changes from dark to light uniformly across the HCG area, indicating the oxidation is progressing through the bars rather than from the central test structure. The color change is caused by a change in reflectance of the sample at near-IR wavelengths. Reprinted with permission from [48].

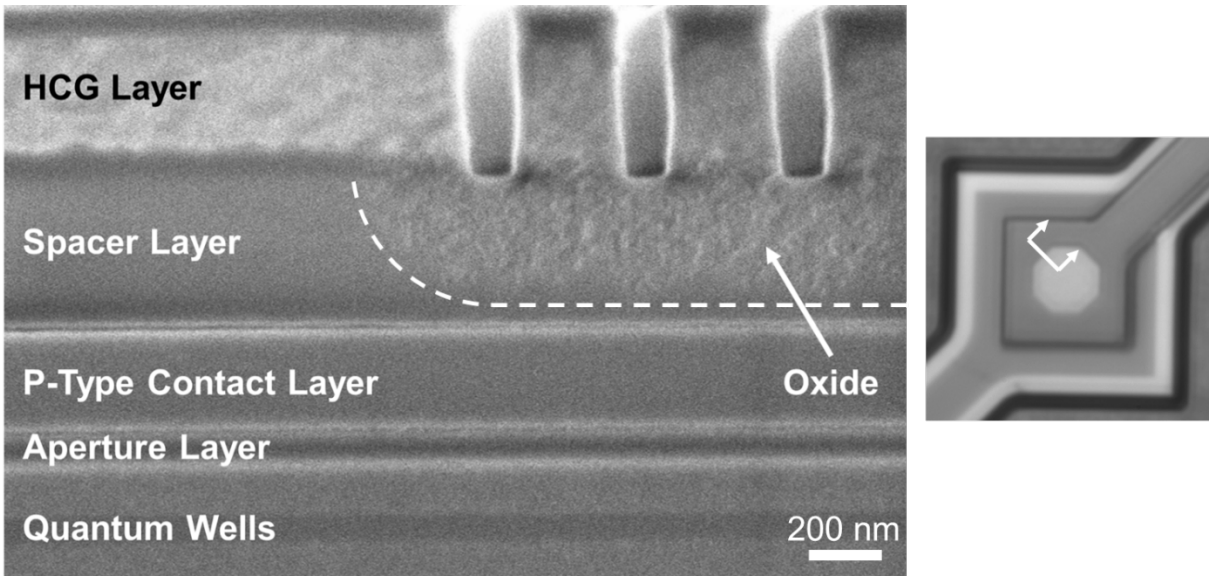


Figure 4.8. SEM cross-section of the fabricated HCG VCSEL. The orientation of the cross-section is indicated on the IR microscope image to the right. The HCG etch reaches the top of the spacer layer, which allows the porous oxide to form in the oxidation furnace. The bars do not delaminate, even when the sample is cleaved in half.

in width as the oxidation progresses. At the same time, the OS layer is oxidized through the bars of the HCG. This is indicated by the color change in the octagonal HCG in Figure 4.7. The color of the octagonal grating changes uniformly – not from center to edge or edge to center – indicating that the grating etch reached the desired depth at all points in the grating. The grating that was monitored includes a central trench that is intended for failure analysis, but this trench does not affect the oxidation of the HCG. VCSELs that do not have this feature also undergo a large color change during oxidation, as shown in Figure 4.8. After oxidation is complete, the grating is encapsulated in 5 nm of Al_2O_3 deposited with atomic layer deposition (ALD). This film prevents further oxidation and increases the mechanical stability of the grating.

Finally, contacts are deposited. This process uses a bilayer LOR 5A and i-line photoresist stack patterned by photolithography with a contact aligner. The VCSEL is coated with Ti/Au on the front side, and eutectic Ge/Au/Ni/Au to form a back-side contact. Liftoff is performed with a high-pressure solvent rinse, and the sample is annealed at 360°C to alloy the n-type ohmic contact.

4.6 Prototype Results

Two different epitaxial designs were fabricated in order to prove the concept of the OS HCG VCSEL. According to the reflectance calculations, the first VCSEL had a 450 nm OS layer and the second VCSEL had a 150 nm OS layer. Aside from the thickness of the OS layer, the two VCSELs were produced according to the same design.

The fabrication, including the top half of the epitaxy, was performed on a 1 cm x 1 cm chip, so there are extreme process deviations from the center to the edge of the chip. Most importantly, the epitaxial Al incorporation is lower at the edge of the chip due to a marginally decreased temperature during growth, which reduces the oxidation rate at the edge of the chip. As a result, the devices have very narrow oxide apertures at the center, and very wide oxide apertures at the edges of both chips. The aperture area of each device on the 150 nm design is interpolated from measurements of test structures placed between the devices on the chip. The aperture area is mapped in Figure 4.9.

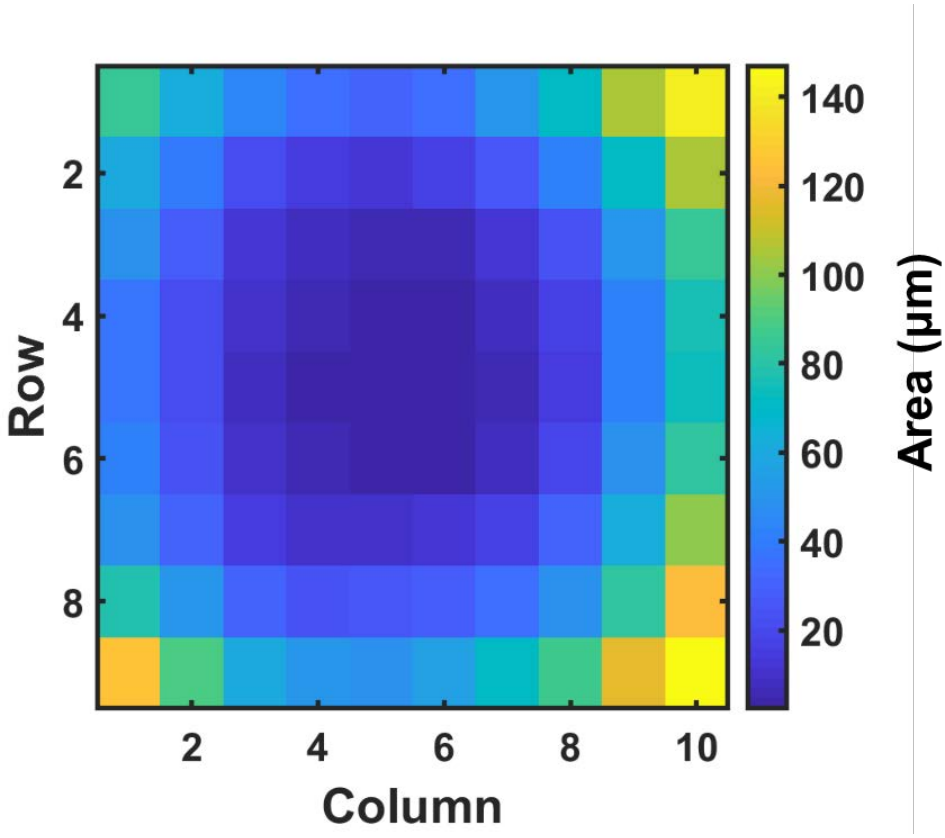


Figure 4.9. Oxide aperture area of the devices produced using the 150 nm epitaxy. The rows and columns of devices are equally distributed across a 1 cm x 1 cm chip. The aperture area increases with distance from the center of the chip due to lower Al incorporation during epitaxy. Since the 450 nm chip was fabricated simultaneously, it has a similar distribution of oxide apertures.

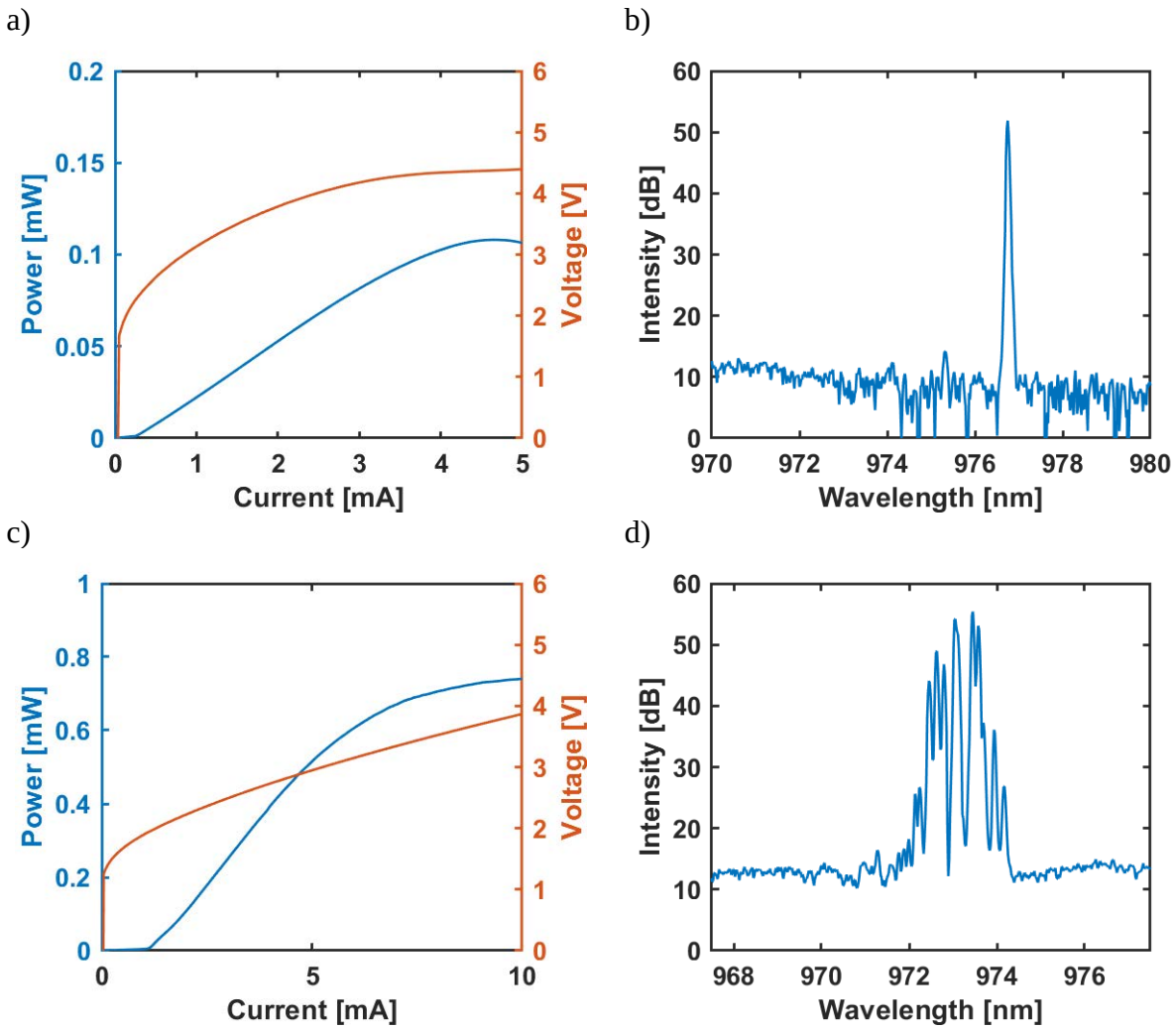


Figure 4.10. Sample LIV and spectrum measurements for OS HCG VCSELs with a 150 nm oxide spacer. Small aperture devices at the center of the wafer (a, b) show very low thresholds and single-mode operation. Large aperture devices (c, d), show larger thresholds, higher power, and multimode lasing.

At the center of each chip, where the oxide apertures are narrow, there are single-mode VCSELs. These VCSELs have a very low threshold current, which suggests a high HCG reflectance, but the effect is confounded by the low area that defines the current density. A single mode is supported with a side-mode suppression ratio (SMSR) of over 30 dB. These are found on both the 150 nm and 450 nm spacer chips. At the edges of each chip, where the oxide apertures are widest, there are multimode VCSELs. Despite the large aperture, these VCSELs have a moderate threshold current, which confirms the high HCG reflectance. Many transverse modes are supported by the large OA, and the output power is significantly higher. On both chips, the output power is low and there is a large series resistance that results in a high operating voltage. As a result, the VCSELs have a low wall plug efficiency.

The LIV and spectrum is measured for 90 devices on each chip. The threshold current and peak wavelength are mapped for these 180 devices in Figure 4.11. HCG designs were assigned to each device by row: row 1 has a bar width of 270 nm, row 2 has a bar width of 280 nm, and row 3 has a bar width of 290 nm. For higher numbered rows, this pattern repeats. For both designs, there is a slight trend in threshold current and wavelength as a function of HCG dimension, but the performance of the VCSEL is dominated by the process variations across the chip. The threshold current is proportional to the aperture area, so the devices at the center of each chip have a much lower threshold than those at the edges. The wavelength maps show a trend from edge to edge on the two chips. This indicates a difference in growth rate at the two edges of the chip and is likely caused by the geometry of the growth chuck. The growth chuck has pockets for four 1 cm chips that are displaced from the center of the chuck. Any variation in temperature or gas flow from the center to the edge of the chuck would cause a variation from edge to edge on the chips. Overall, the 450 nm chip has a shorter cavity than designed, which resulted in a much lower median wavelength.

In total, 179 out of 180 measured devices were able to achieve threshold, which proves that the oxide spacer HCG is a feasible structure to use as a VCSEL reflector. In order to turn the prototype VCSELs into a useful device, the wall plug efficiency must be increased.

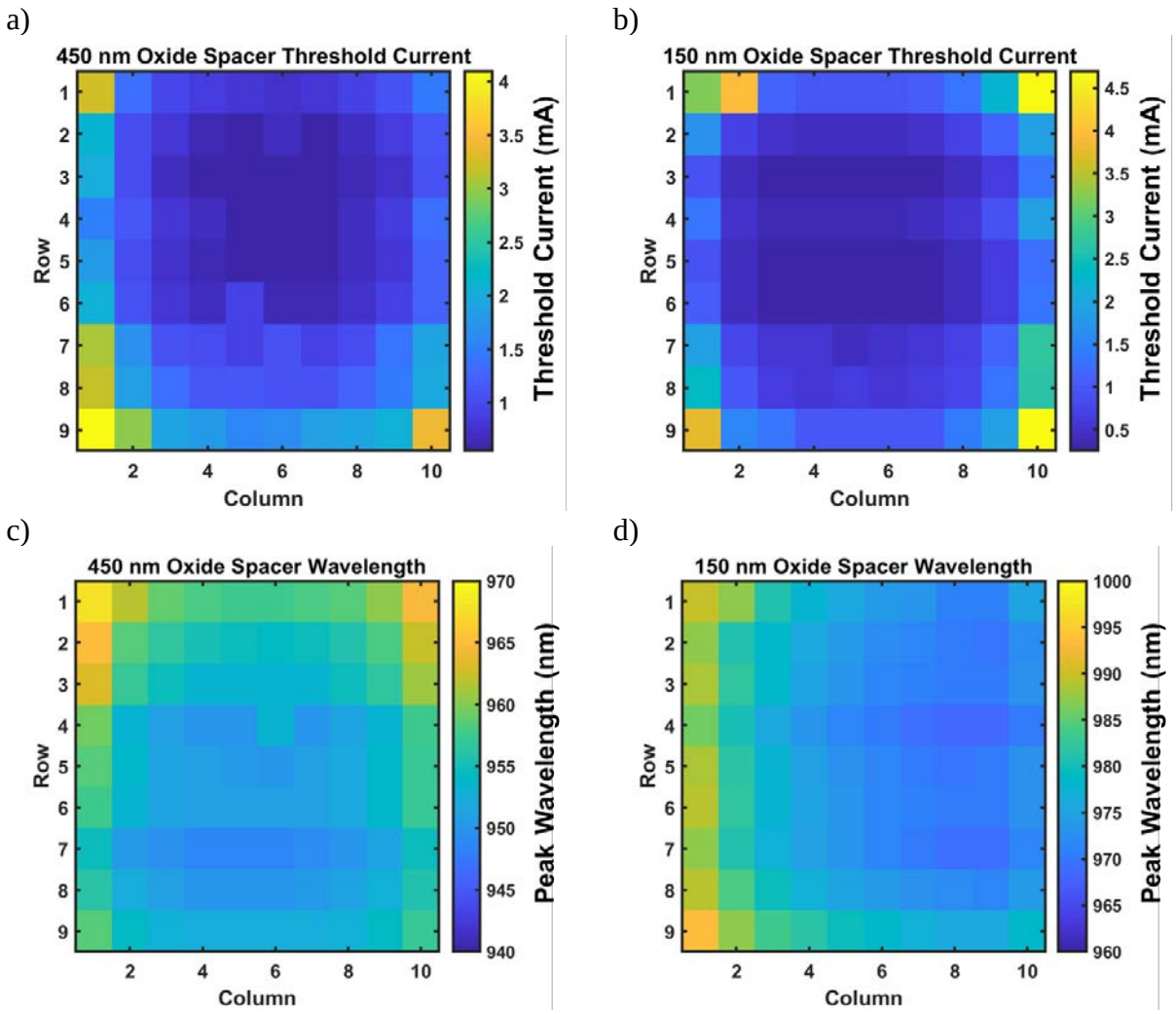


Figure 4.11. 90 devices were measured on each chip, spanning across the 1 cm x 1 cm chip. (a, b) Threshold current map for the 450 nm and 150 nm prototype chips. The threshold current was extracted from the LIV plot by finding the increase in slope of the LI curve. The threshold current map shows a strong correlation with oxide aperture area. (c, d) Wavelength maps for the 450 nm and 150 nm chips. The wavelength varies from edge to edge on the chip, indicating a faster growth rate on one side of the chip.

a) b)

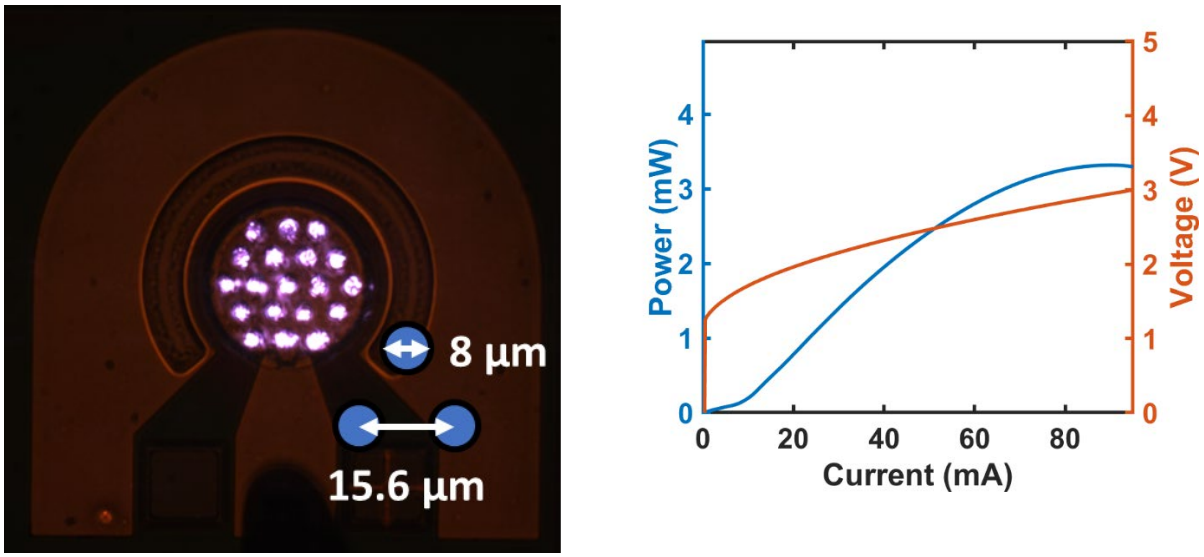


Figure 4.12. A high density VCSEL array fabricated with the prototype HCG VCSEL design. The aperture diameter is 8 µm and the pitch of the array is 15.6 µm, which gives an area fill factor of 24%. The power output is significantly increased over the single VCSEL power output.

4.7 Prototype Arrays

The process for producing the prototype HCG VCSELs was extended to produce an HCG VCSEL Array prototype. The process begins with an identical epitaxial structure. During the HCG lithography, oxidation trenches are added to the electron beam lithography pattern, which are then etched during the HCG etch with RIE. The HCG mesa is etched with RIE instead of wet etching, and during this process the oxidation trenches are etched even deeper. A larger oxidation mesa is etched around the full array using RIE. During oxidation, the aperture oxidation progresses from the border of the oxidation trenches outward, forming hexagonal VCSEL apertures. After the p-type contact is evaporated, the structure is planarized with photosensitive benzocyclobutene (BCB), which is patterned with the contact aligner and cured. Finally, large contact pads are evaporated on top of the BCB, allowing the devices to be probed.

The double etch process in the HCG trenches caused the arrays to have poor yield, but emitter counts up to 19 were functional. As in the single devices, the output power of the VCSEL array leaves room for improvement. The fabricated arrays had an element pitch of 15.6 µm and an aperture diameter of 8 µm, which gives an area fill factor of 24%, proving the capability of integrating OS HCG VCSELs into high density arrays. Using an optimized process, epitaxial design, and HCG design will improve the performance of both the single emitters and the VCSEL arrays.

4.8 Improving Performance

The prototype OS HCG VCSELs have two important problems that contribute to their low efficiency. First, the operating voltage is high. This can be reduced by optimizing the doping profile and the geometry of the current path between the contacts and the quantum wells. Second, the slope efficiency is low. Since the threshold current is low, there is room to trade threshold current for a higher slope efficiency by increasing the transmittance of the HCG reflector.

In order to optimize the current path, design elements are adapted from DBR VCSELs. First, the doping of the OA layer is increased to reduce resistance through the OA. Next, a few pairs of DBR are added between the current spreading layer and the OA layer to increase the thickness of the current spreading region between the contacts and the OA and increase the lithographic tolerance of the HCG. Finally, the thickness of the current spreading layer and the doping level of the contact interface are both increased.

In order to optimize the slope efficiency, a second figure of merit is considered. This is the fractional power of the top reflector. In this equation, the subscript 1 denotes the top HCG reflector on the VCSEL, and 2 denotes the bottom DBR.

$$F_1 = \frac{t_1^2}{(1 - r_1^2) + \frac{r_1}{|r_2|}(1 - |r_2|^2)} \tag{4.1}$$

This parameter defines the fraction of light that exits the cavity through the top surface of the top mirror. In an HCG reflector, light can be transmitted or reflected in the zeroth order, but it can also be reflected into the first order at typical grating dimensions. In other words, the power transmittance and reflectance in the zeroth order do not add up to unity, so there is a portion of power that is lost due to diffraction. If r_1 and t_1 are used to refer to only the zeroth order transmittance and reflectance, then Equation *4.1* takes this diffraction loss into account.

The plots of R_1 and F_1, shown in Figure 4.13, respectively, illustrate this diffraction loss for an HCG with a fixed grating thickness and spacer thickness. As expected, the region with the highest reflectance has a very low fractional power output. More surprisingly, the F_1 heatmap shows poor extraction efficiency even as the reflectance of the grating is reduced to 98%. To design an efficient HCG reflector, this reduction in F_1 due to mirror loss must be considered.

a) b)

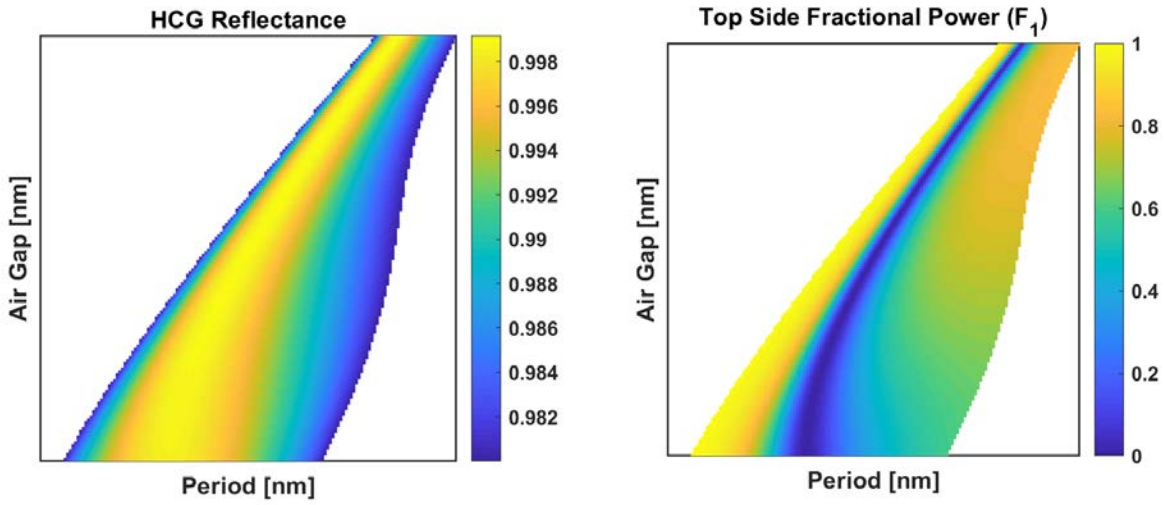


Figure 4.13. Reflectance and fractional power for HCG designs for a 940 nm VCSEL. The reflectance of an HCG needs to be large enough to give the VCSEL a low threshold, but small enough to allow light to leak out of the upper reflector. The fractional power measures the amount of light that escapes from the top reflector of the VCSEL and will determine the maximum slope efficiency of the VCSEL.

4.9 Process Scaling

Electron beam lithography is a useful tool for prototyping, but it is not scalable to large arrays. With an optimized recipe, the write time for a 1 cm x 1 cm chip of VCSEL arrays with proximity effect correction takes hours to days to write. In order to produce VCSEL arrays, the HCG definition process must be migrated to deep ultraviolet (DUV) lithography, which can process tens of 6" wafers per hour.

DUV lithography is a well-established technology in Si manufacturing. The light sources used are excimer lasers, with wavelengths of 248 nm for KrF or 193 nm for ArF. The baseline resolution and depth of focus for a DUV stepper is given by a modified version of the Rayleigh criterion, where k_1 and k_2 indicate the performance of the process.

$$CD = k_1 \frac{\lambda}{NA} \tag{4.2}$$

$$\mathrm{D_F} = \mathrm{k_2} \frac{\lambda}{\mathrm{NA^2}} \tag{4.3}$$

For the stepper used in this work, the maximum *NA* is 0.63. Typical values for k_1 range from 0.4 to 0.9. This gives the stepper a minimum resolution of 157 nm with an ideal process. In practice, the stepper used in this work is rated for a 250 nm critical dimension (CD), but it can be reduced to approximately 200 nm (k_1 = 0.5) by using a backside antireflection coating (BARC) and off-axis illumination.

BARC is a spin-on polymer that is applied to the wafer prior to the application of photoresist. Without it, the interface between the wafer and the photoresist has a significant reflectance, which produces vertical standing waves in the photoresist, which will negatively affect the

control of the HCG linewidth. BARC provides a low index step – reducing reflection – and then absorbs the 248 nm light within the film.

Off-axis illumination is another technology that can be used to improve k_1 and k_2. With a 4x scale reticle, the pitch of an HCG is about 4 times the wavelength of light, so multiple diffracted orders will be generated when the light passes through the reticle. The aerial image that is formed by the objective lens at the wafer surface is defined by the interference between the diffracted orders, which necessitates the use of at least two orders. If the angle of illumination is tilted to half of the diffraction angle between each order, then the image pupil can be used to discard all but the zeroth and first diffraction orders. This effect can increase k_1 and k_2 by effectively cutting the illumination cone in half.

Since OAI relies on diffraction through the reticle, the angle must be designed for a specific pitch. By examining the illumination that falls inside the image pupil, the coefficients $s_{1,2,3}$ for one-beam, two-beam, and three-beam imaging can be calculated for each pitch on the mask. Three-beam imaging is the type of imaging that occurs with conventional illumination: the zeroth, first, and negative first diffraction orders all reach the wafer. Two-beam imaging is the desired imaging condition: only two diffraction orders (zero and one or zero and negative one) reach the mask. One-beam "imaging" does not form an image at all: if an image is an interference pattern between multiple diffraction orders, then a single beam can only apply a flat dose across the whole wafer, reducing the image quality. An OAI exposure is optimized by maximizing the 2-beam imaging coefficient, a function of the partial coherence factor, which is an expression of the angle of incidence in *NA*-space [49]. Equation *4.6*is used to calculate the partial coherence factor for several HCG pitches in order to determine the optimal exposure conditions, shown in Figure 4.14.

$$\sigma = \frac{n \sin\theta}{NA} \tag{4.4}$$

$$\gamma = \frac{1}{\pi}\cos^{-1}\left\{\frac{1}{2}\left[\left(\frac{\lambda}{\Lambda\, NA}\right)\frac{1}{\sigma} + \left(\frac{\Lambda\, NA}{\lambda}\right)\left(\sigma - \frac{1}{\sigma}\right)\right]\right\} \tag{4.5}$$

$$s_2 = \begin{cases} 2(1-\gamma) & 1-\sigma \le \dfrac{\lambda}{pNA} \le \sqrt{1-\sigma^2} \\ 2\gamma & \sqrt{1-\sigma^2} \le \dfrac{\lambda}{pNA} \le 1+\sigma \end{cases} \tag{4.6}$$

In the ASML PAS 5500/300, an OAI exposure is specified by two values of σ, σ_{inner} and σ_{outer}, which correspond to 10% encircled flux and 90% encircled flux of the annular illumination pattern. The values used for the exposure of the designed HCGs are 0.4 and 0.6, respectively.

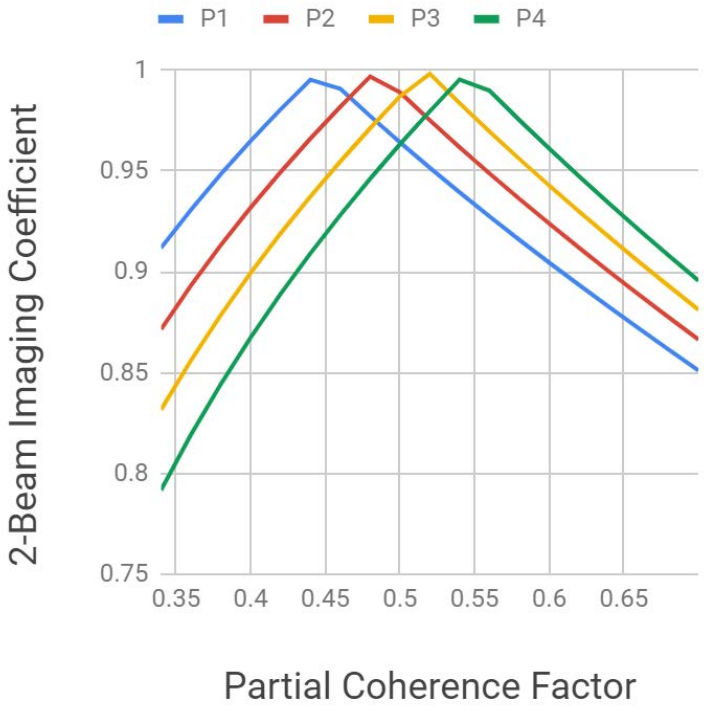


Figure 4.14. The 2-beam imaging coefficient is used to optimize the exposure conditions for the oxide spacer HCG lithography using a DUV stepper. The image formed at the wafer is an average of the one-beam, two-beam, and three-beam intensity patterns, weighted by their respective coefficients. The partial coherence factor represents the angle of incidence on the reticle. The four pitches show high s_2 at a partial coherence factor range from 0.4 to 0.6.

The process window for the DUV exposure was investigated by exposing a focus/energy matrix. In this exposure test, a device-representing test structure was stepped across the wafer while varying the focus offset by row and the exposure energy by column. The exposed area was etched using ICP, and the wafer was cleaned using a high-pressure solvent spray. The resulting test structures, which contain a 220 nm CD, were measured at a variety of exposure energies and focus offsets. The results are shown in the Bossung plot and CD contour plot in Figure XX. Each line in the Bossung plot shows the printed CD as a function of focus offset for a given exposure energy. As the exposure energy approaches the optimum value, the printed CD approaches the designed CD of 220 nm. The CD contour shows a contour plot of the CD as a function of both focus offset and exposure energy. For an exposure latitude of 0.5 mJ/cm^2, the depth of focus is larger than 1 µm for a <5% CD variation. Since the HCG is the first step in the fabrication process, there is no topography on the wafer. This means the image is in very good focus for the extent of the 0.36 µm photoresist film, and there is room to increase the thickness of the resist if required by the etch selectivity.

a) b)

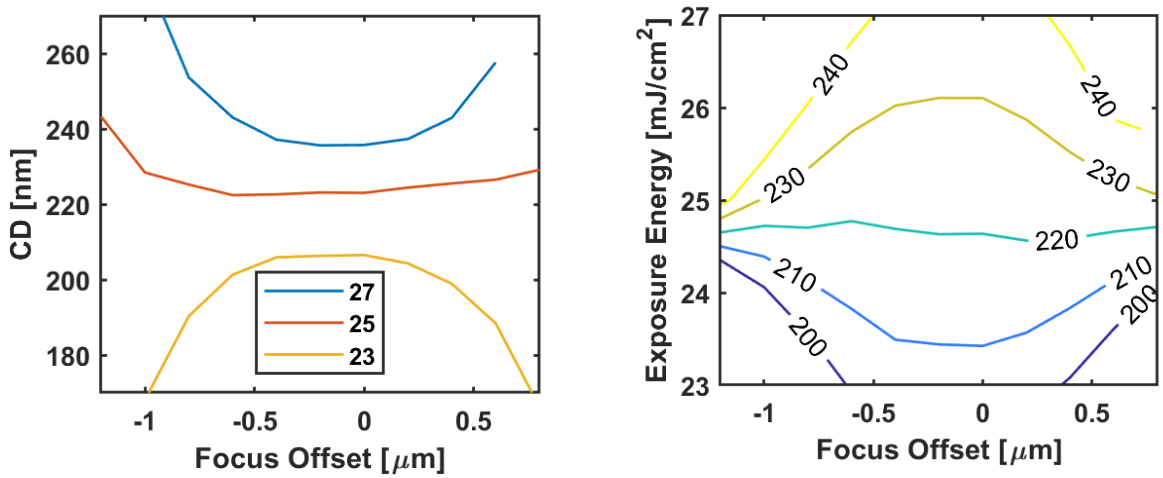


Figure 4.15. The DUV exposure process utilizing BARC and OAI gives a reasonable process window for a 220 nm line. (a) The Bossung plot shows the printed CD as a function of focus offset for three different exposure energies. The lines flatten near the designed CD of 220 nm. (b) The focus contour shows a process window with 0.5 mJ/cm^2 of exposure latitude and over 1 µm of focus latitude for a CD variation of ±5%.

In addition to the challenge of producing a 200 nm CD, there are also practical challenges involved in processing 6" GaAs epiwafers. A GaAs wafer is twice as heavy and fractures at half the stress of an identical Si wafer, so the 6" wafer must be handled with extreme caution. The thermal cycles involved in photolithography can create enough stress to fracture the wafer in the presence of a small scratch. The epitaxial layers are overall compressively strained, which causes a wafer bow of 70-90 um. This bow is too large for reliable wafer handling with robots designed for Si wafers, so it must be compensated in order to use the lithography tools.

The bow of a GaAs epiwafer can be compensated in two ways. First, it is possible to deposit a tensile bow compensation film on the front side of the wafer. This is possible using plasma-enhanced chemical vapor deposition (PECVD) to deposit Si_3N_4 at a high temperature and with a large NH_3/SiH_4 gas ratio [50]. This bow compensation film has several drawbacks. First, the film stress is low, so the film thickness needs to exceed 1 µm. It is challenging to transfer a 200 nm space into such a thick film. Additionally, it requires a deposition time of more than 1 hour, plus heating and cooling time. Only one wafer can be processed in each run, so this does not scale well to multiple wafers. Second, the film stress is unstable with time. High stress PECVD Si_3N_4 films will relax over time as the H_2 content of the film changes. This requires photolithography immediately after depositing the Si_3N_4 film, which is impractical in a shared fabrication facility.

The second option for bow compensation is to deposit a compressive film on the back side of the wafer. It is easy to create a compressive SiO_2 film with PECVD. This compensation film does not relax over time and leaves the front side of the wafer clear for lithography and etching, but can hurt yield since the epitaxial surface may be scratched during loading and unloading. This can be minimized by ensuring the use of a very flat surface beneath the wafer, and by depositing

a protective coating on the front side of the epiwafer. Compressive SiO_2 was chosen as the bow compensation film for the improved oxide spacer HCG VCSEL process. No front side protection layer was deposited, but a virgin silicon wafer was used as an intermediate layer between the GaAs wafer and the metallic platen of the PECVD tool.

The mesa etch processes used in the fabrication of the prototype OS HCG VCSELs is insufficient for the production of VCSEL arrays. The chemical etching produces a large (>1 μm) undercut of the photoresist. The etch rate of GaAs and AlGaAs is not the same for any chemical etchant, so the DBR layers become corrugated and the OA layer has a very deep undercut (>5 μm). Furthermore, the etch rates are crystallographically dependent, which does not work well with a close-packed hexagonal lattice. Several ICP dry etching recipes were developed for OS HCG VCSEL processing. The first recipe provides equirate etching of GaAs and AlGaAs, and is suitable for grating etching and oxidation trench etching. The second recipe provides selectivity between AlGaAs and InGaP, which can be employed as an etch stop for either the grating or the oxidation trenches. The third recipe selectively etches GaAs over AlGaAs, which can be used during the grating etch in order to terminate the etch at the top of the OS layer. All three recipes provide a selectivity to photoresist of more than 2, which is more than enough for the <500 nm grating etch and the <2 um trench etch.

Ultimately, the redesigned OS HCG VCSELs were fabricated using a similar process to the prototype devices. After the 6” epiwafer is cleaned in organic solvents, an SiO_2 bow compensation layer is applied to the back side of the wafer. The wafer is coated with BARC and 0.36 μm DUV photoresist, and exposed in the DUV stepper using the optimized OAI parameters. The photoresist is hardbaked in an oven at 120°C, and the wafer is diced into 2 cm x 2 cm chips to fit the 2” ICP coil.

The gratings are etched using the nonselective or Al-selective ICP process. A separate BARC breakthrough process is not included – the nonselective ICP process etches through the 60 nm BARC film in 23 seconds. The chips are cleaned using a high pressure solvent spray, a solvent rinse, and oxygen plasma treatment.

The HCG mesa is defined using an i-line stepper and etched using ICP. The selective etch is used to stop on an InGaP layer that protects the p-contact layer. The oxidation trench etch is performed in a similar fashion with a thicker photoresist. The chip is oxidized in a furnace, and a 20 nm Al_2O_3 layer is deposited to encapsulate the oxide.

The front side of the chip is protected with a thick photoresist layer, and the backside of the chip is etched in buffered HF to remove the bow compensation layer. Etch completeness is measured by monitoring the adhesion of water to the surface of the wafer. Aqueous solutions (such as BHF) will not wet the GaAs surface as well as it wets the SiO_2 surface.

The p-type contact pattern is defined in a bilayer LOR 5A and i-line photoresist stack. Buffered HF is used to remove the Al_2O_3 in the contact region. The InGaP etch stop is removed with $HCl:H_3PO_4$ 1:3, and Ti/Au is evaporated on the front side of the chip. The chip is turned over, and a backside Ge/Au/Ni/Au contact is evaporated. Finally, the chip is finished with liftoff in the high pressure solvent spray and annealed to form an ohmic contact.

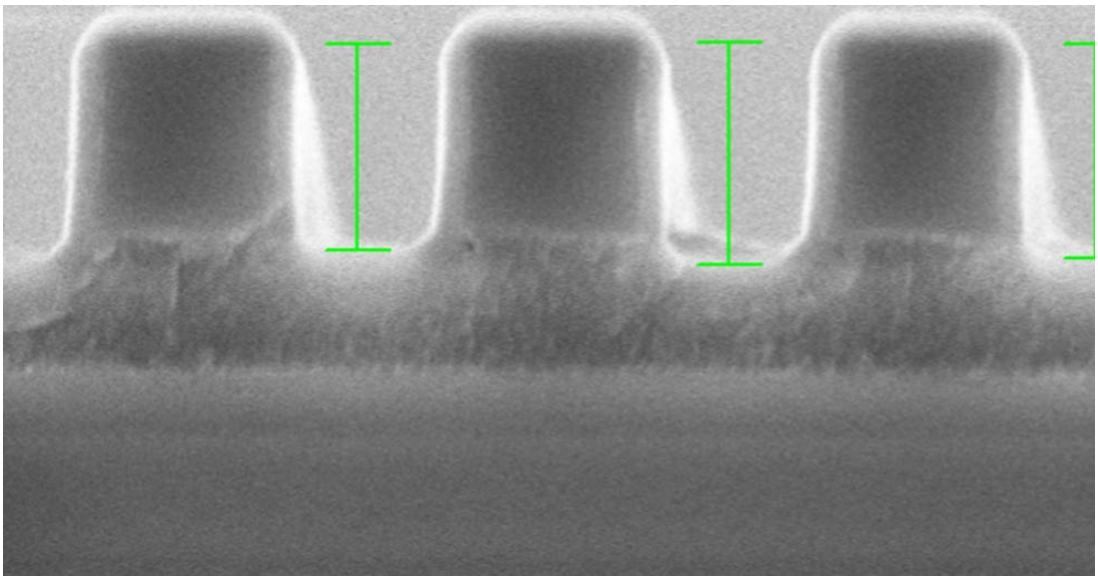


Figure 4.16. SEM cross section of improved HCG device. The DUV process creates gratings with a higher performance at a larger CD than the electron beam lithography process. The grating etch terminates in the oxide spacer, which is fully oxidized. The gratings are encapsulated with 20 nm ALD.

4.10 Improved Device Results

The redesigned OS HCG VCSELs were fabricated with a range of grating dimensions sampling the design space simulated in Figure 4.13. The reticle was designed this way to test a large portion of the design space, including many different combinations of reflectance and fractional power output. For the HCG etch process, two different etches were used. The first etch is timed to stop within the OS layer, and the second etch uses SF_6 to stop the etch at the interface between the OS and HCG layers.

After fabricating devices with the improved DUV process, the LIV characteristics of 9600 devices per chip are measured using an automated probe station. The laser yield, defined as the fraction of devices with a measurable threshold, is mapped as a function of grating design in Figure 4.17. The laser yield is strongly related to the width of the HCG bar and the duty cycle of the grating. As the width of the HCG bar is reduced, a number of different problems can arise which prevent the mirror from functioning properly. First, the HCG bars can lift away from the underlying BARC during development, bending the bars or removing them from the substrate altogether. Next, narrow HCG bars can be partially exposed and eroded during development, reducing the thickness of the resist and causing the HCG etch to reduce the thickness of the bars. A narrow HCG bar is also required for a low duty cycle. In a low duty cycle grating, a larger dose of DUV illumination will reach the substrate due to the wider HCG air gaps. This causes the grating to be overexposed, further reducing the width of the HCG bars. If the duty cycle is too high, the opposite effect can cause the grating to be underexposed, which will slow down the grating etch due to aspect-ratio dependent etching (ARDE). If the grating etch is too slow, the etch will not reach the underlying OS layer, and water vapor can not diffuse into the grating during oxidation.

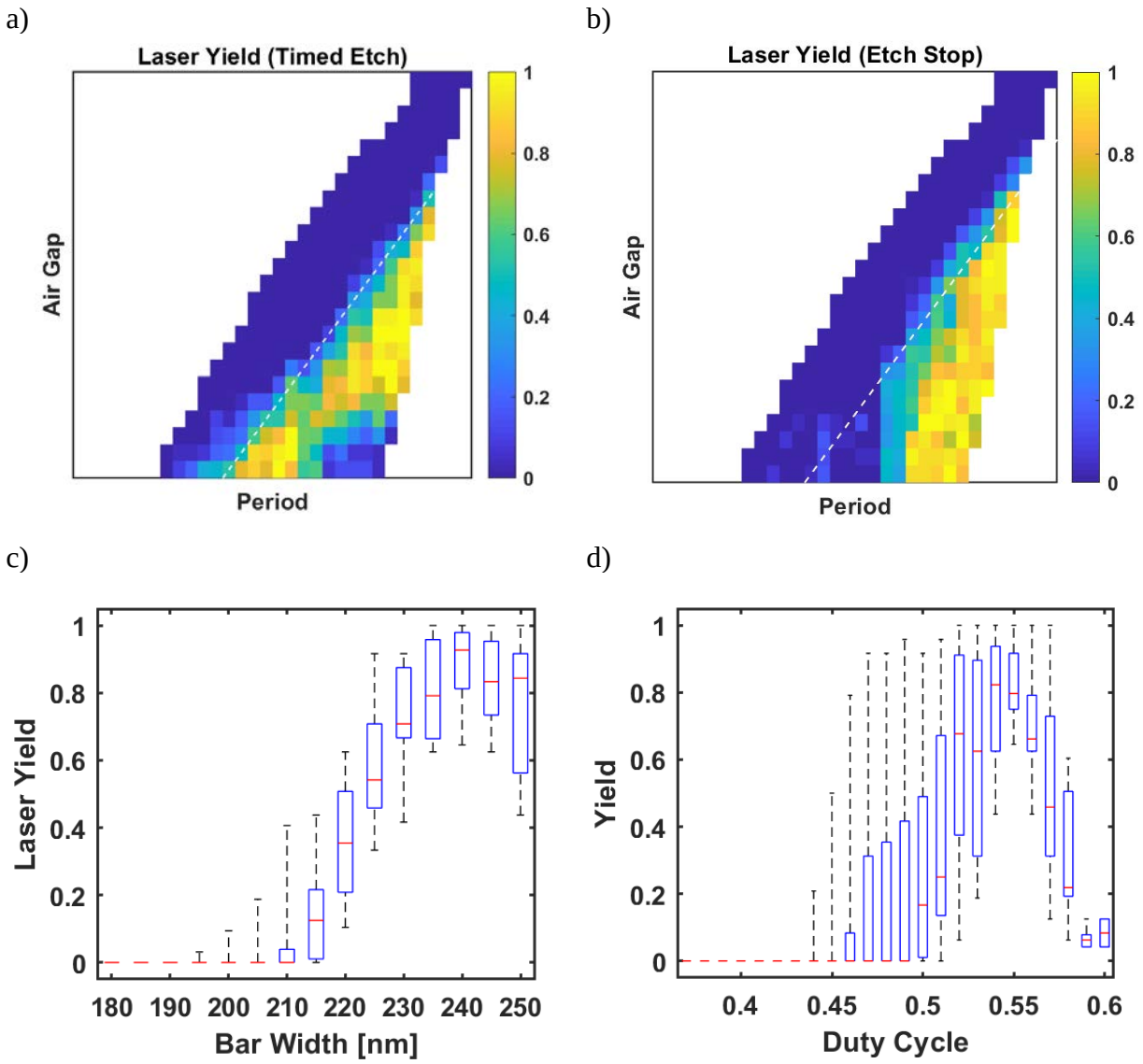


Figure 4.17. Laser yield using two different etch recipes: (a) a timed etch and (b) a selective etch that stops at the OS layer. HCG designs on the right half of the design space show higher yield than designs on the left half. White space indicates the region where no data was taken. (c) The median laser yield drops below 0.5 at a bar width of 220 nm, indicating the limit of the DUV stepper with the chosen exposure conditions. (d) The median laser yield shows a peak at an HCG duty cycle of 0.55, which is the duty cycle used to calibrate the exposure conditions. Higher duty cycles will be underexposed, and lower duty cycles will be overexposed.

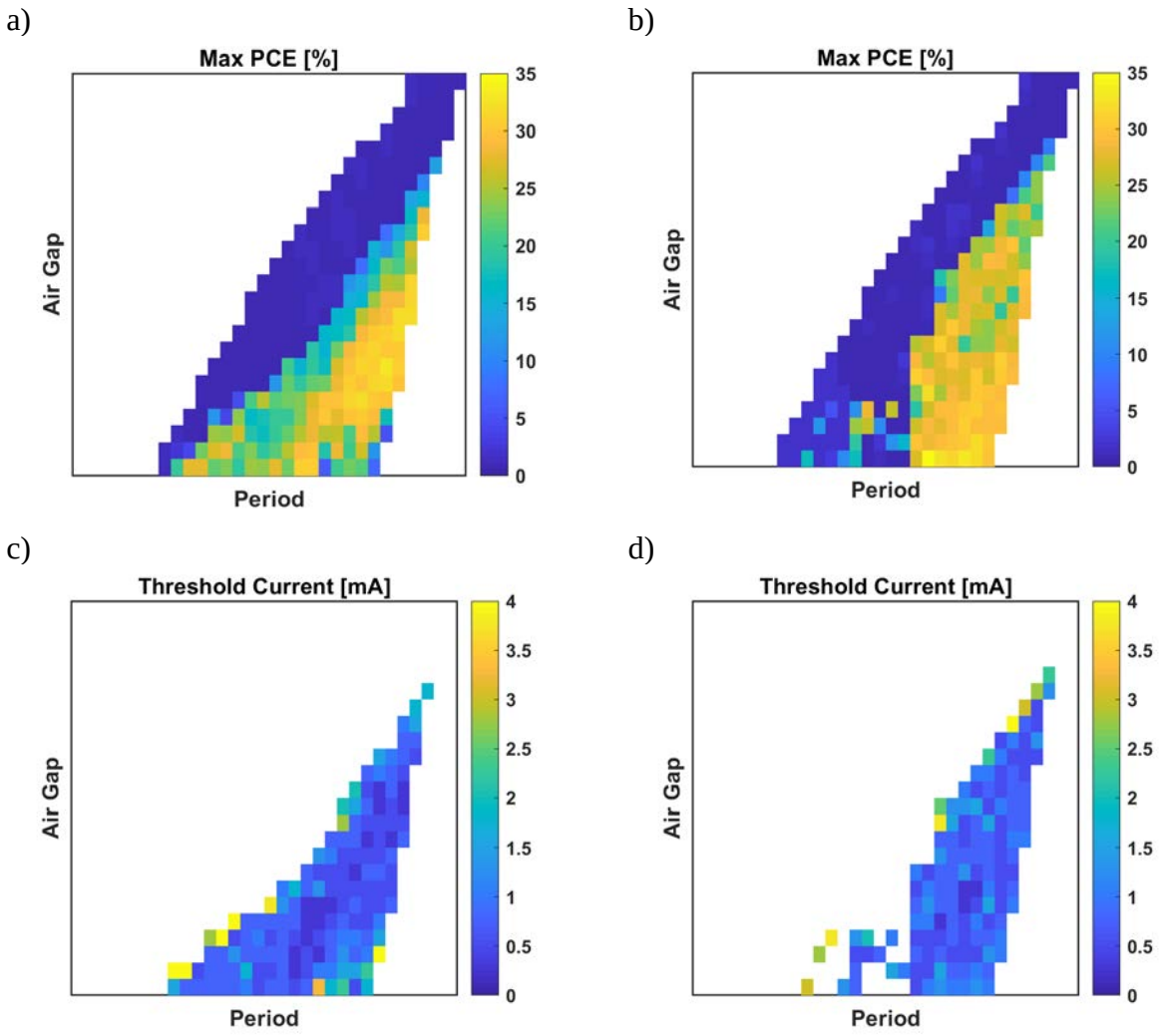


Figure 4.18. Highest peforming devices for each grating design. Figures (a) and (c) were measured from the timed grating etch sample, while figures (b) and (d) were measured from the selective etch sample. The highest measured efficiency is 32.9% using the timed grating etch and 34.8% using the selective etch. The threshold current for the highest performing devices ranges from 1 to 1.5 mA.

The highest performing VCSELs of each grating design are plotted in Figure 4.18. At the best set of HCG dimensions, the OS HCG VCSELs operated at a wall plug efficiency of 32.9% and 34.8% on the timed etch and selective etch samples, respectively. This performance is comparable to commercial DBR VCSELs and is the highest efficiency for an HCG VCSEL to date. The threshold current for the high performing devices ranges from 1 to 1.5 mA. At lower thresholds, the efficiency is reduced by the higher reflectance of the HCG reflector.

The average performance of each HCG design is shown in Figure 4.19. A minimum of 24 devices are used in the calculation of each average. For both of the two samples, there are regions with average WPE of more than 20%, with a maximum of 25.4% and 24.2% for the timed etch and selective etch, respectively. The average threshold current is also increased, likely due to imperfections in the HCGs.

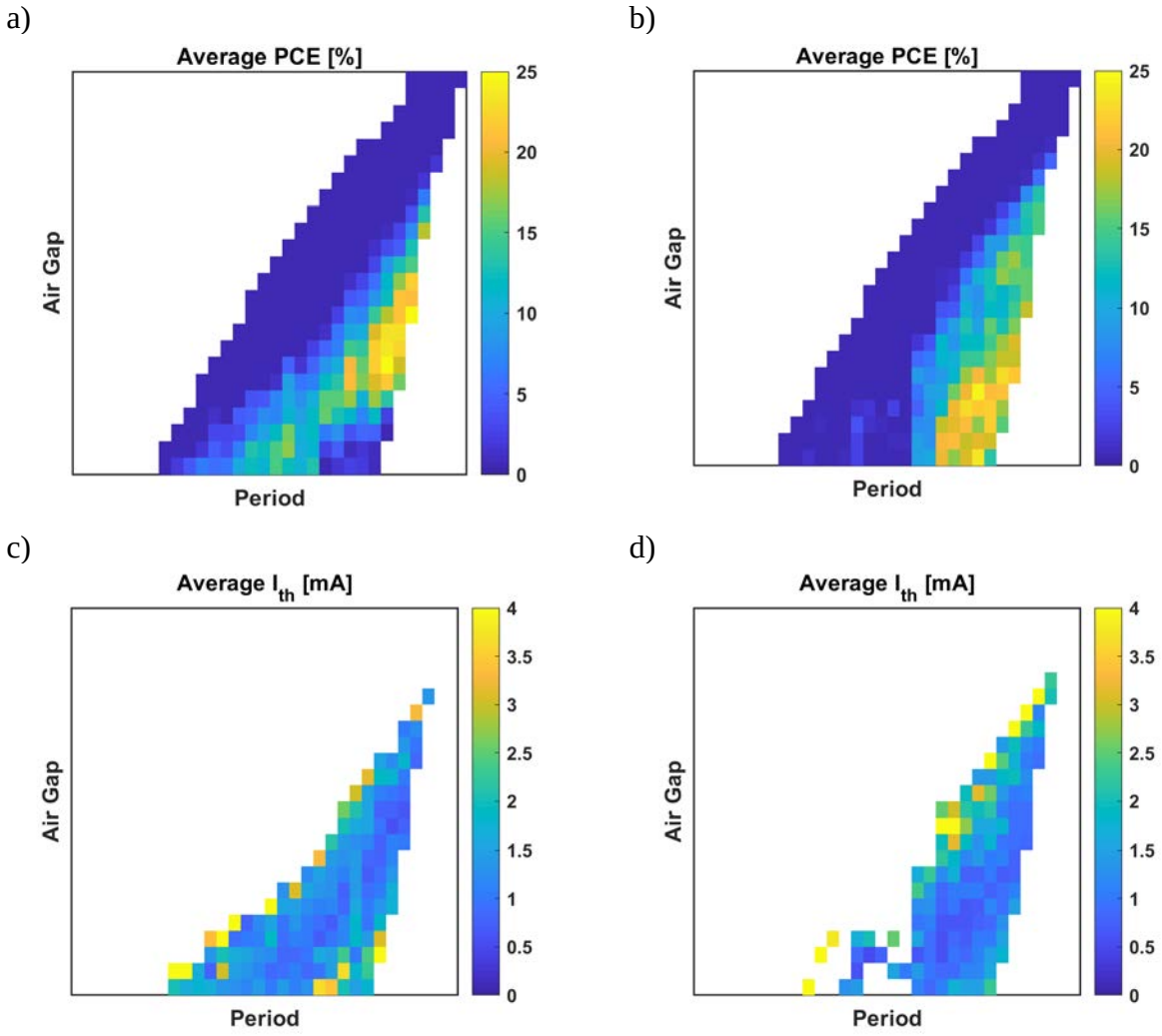


Figure 4.19. Average performance for each grating design. Figures (a) and (c) were measured from the timed grating etch sample, while figures (b) and (d) were measured from the selective etch sample. Data from at least 24 devices were used to calculate each average. The highest measured efficiency is 25.4% using the timed grating etch and 24.5% using the selective etch.

a) b)

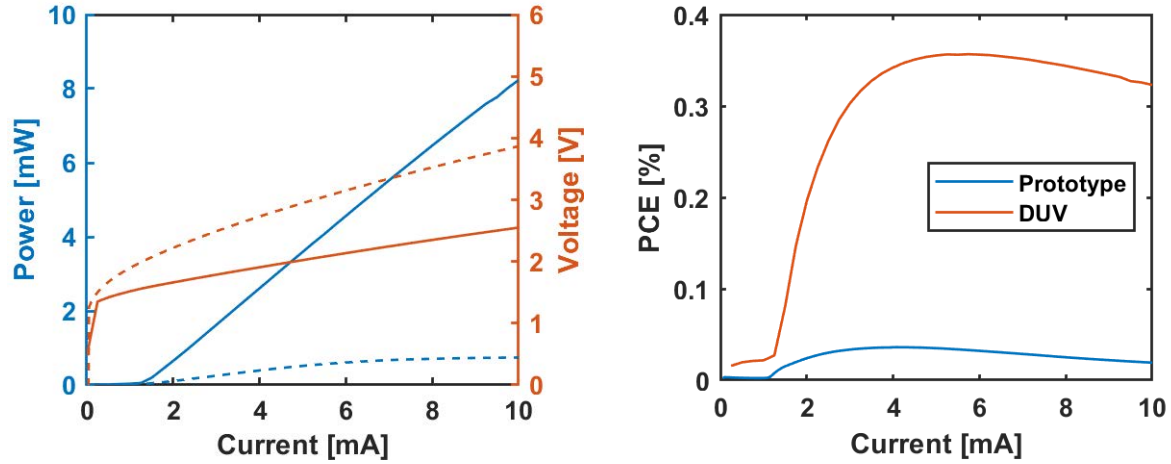


Figure 4.20. The DUV process produces devices with much higher performance than the prototype devices. (a) LIV comparison. The DUV device is shown with solid lines, and the prototype device is shown with a dashed line. The output power is ten times higher for the new device, and the voltage is decreased by 1V. (b) The WPE for the DUV device exceeds 35% at its peak. The old device delivered a maximum of 3.9%.

An LIV curve for a high power DUV device is compared to a high power prototype device in Figure 4.20. The DUV device emits 5.0 mW of light at the operating point of 6.5 mA, with continuous wave operation. The voltage drop is reduced by a full 1V due to the improved doping profile and thicker current spreading region. Together, these performance improvements amount to a WPE that is over 10 times higher than the prototype device at the operating point.

After proving the performance of single HCG VCSELs, the highest performing grating designs were used to produce HCG VCSEL arrays. The process is almost identical to the single VCSEL process, but the mask set is modified to produce single VCSELs alongside arrays of 7, 19, 56, and 100 elements The gratings are etched using the timed etch process. The array devices use triangular oxidation trenches between the emitters, and a large oxidation trench surrounding the entire mesa to isolate the arrays from one another. In comparison to a mesa etch, the surrounding trench produces a smaller ICP loading effect and can be etched to the same depth as the triangular trenches. The Ti/Au p-type contact is in direct contact with the p-type GaAs contact layer across the entire covered area, so the current can spread through the contact and the semiconductor between devices. The device pitch is 40 μm for all array sizes. Microscope images of each array size are shown in Figure 4.21.

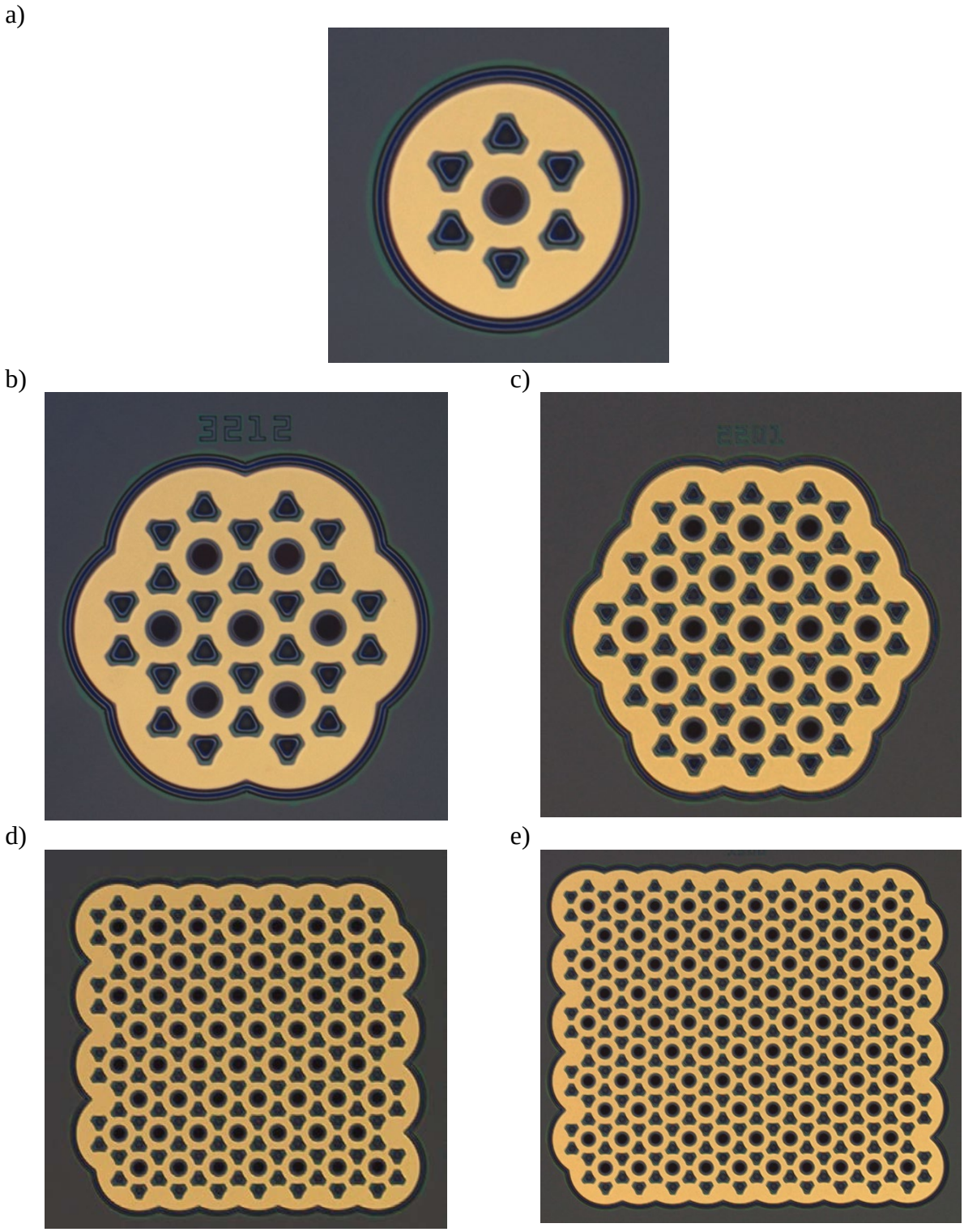


Figure 4.21 Oxide spacer HCG VCSEL arrays. Arrays are fabricated with 1, 7, 19, 56, and 100 emitters. Each pattern uses an identical unit cell containing a circular HCG, triangular oxidation trenches, and a gold ohmic contact. A trench traces the outer extent of the arrays, leaving space for probing the devices. The emitter pitch is 40 μm for all arrays.

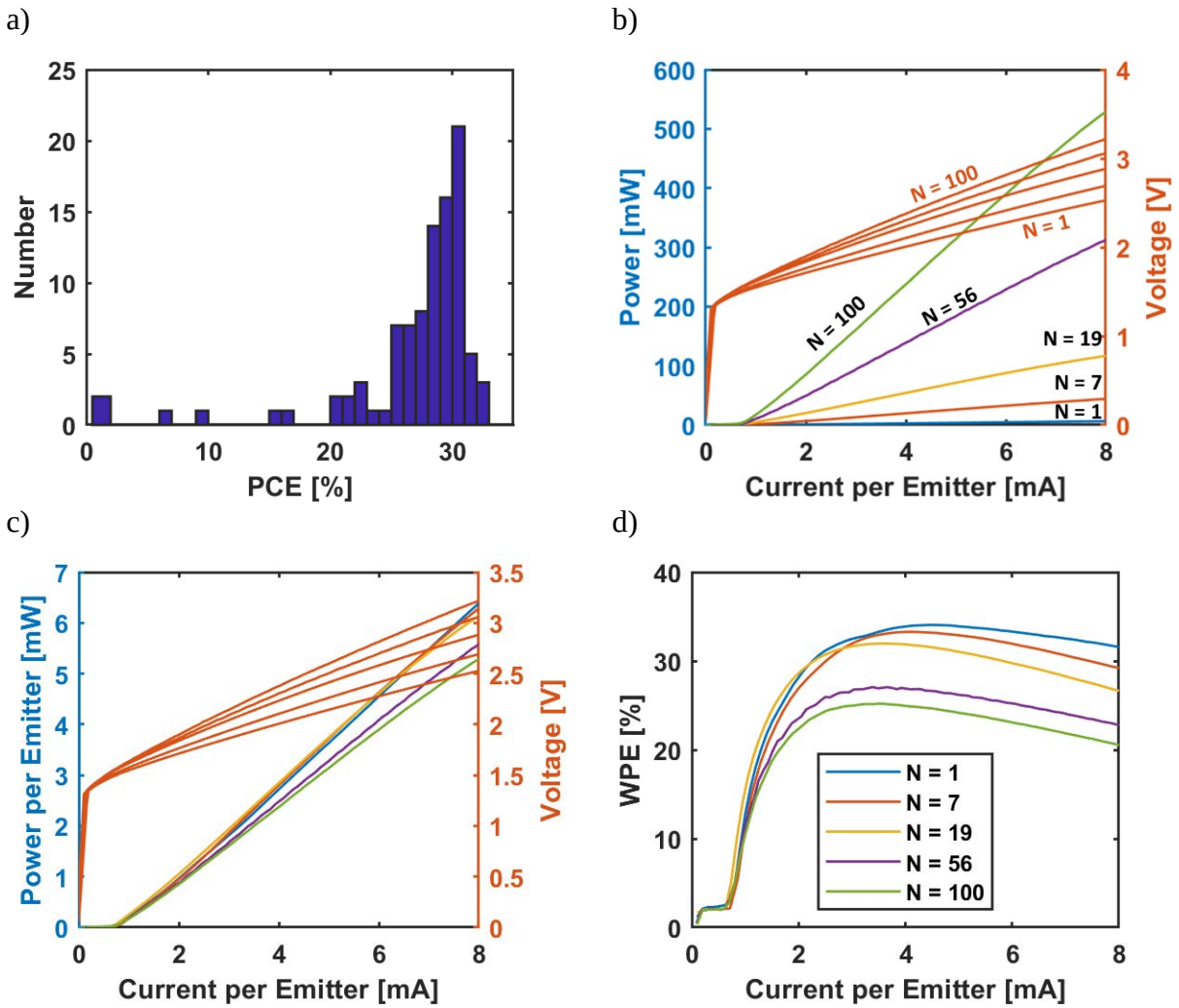


Figure 4.22. The DUV process can scale to produce high-efficiency arrays. (a) The process is verified with a larger number of single VCSELs with identical gratings, which have an average WPE of 27.1%. (b) The 100 element array emits over 500 mW of power. The resistance of the arrays increase with element number. (c) The output of the arrays scales linearly to 7 and 19 element arrays. 56 and 100 element arrays show slightly decreased power. (d) The WPE of the arrays is lower than the single device. The small arrays are lower due to the higher voltage. The larger arrays are affected by higher voltage and lower power.

The single VCSELs produced in the array fabrication batch match the expected performance from the initial DUV fabrication batch with an average WPE of 27.1% and a peak WPE of 32.9% at 6.5 mA. The single VCSEL WPE histogram in Figure 4.22(a) shows a large cluster with a peak at 30-31% WPE, with several less efficient devices lowering the average. This curve shows the process has the potential to be scaled to high volume production, where there would be a lower concentration of defective devices. The largest increase in yield would come from a

full 6” toolset, which would eliminate the need for dicing the wafer after performing the HCG lithography.

The LIV and WPE for the highest performing arrays are shown in Figure 4.22(b-d). The 7 and 19 element arrays exhibit nearly identical power output per emitter as the single VCSEL. The 56 and 100 element arrays show a reduced power output per emitter due to emitter yield and ohmic heating. Since a fraction of the HCGs are damaged during fabrication by particulate contamination and dicing, the larger arrays are subject to more variation and usually contain at least one emitter without a functioning HCG.

The series resistance of the arrays increases with array size. This is caused by the thin Ti/Au contact. In a commercial VCSEL array, electroplating is used to deposit several microns of gold on top of the VCSELs, providing a low resistance current distribution path. This leads to a reduction in WPE for the 7 and 19 element arrays, despite the excellent power scaling. In the 56 and 100 element arrays, the combination of increased resistance and reduced power output causes a significantly larger reduction in efficiency. Even so, all the array sizes are able to maintain a WPE of more than 20% across the entire operating range.

4.11 Conclusion

Oxide spacer high contrast gratings are a promising alternative to distributed Bragg reflectors in high power VCSEL arrays. The thinner epitaxy reduces the cost of producing each VCSEL array and can reduce the pitch and increase the uniformity of the array by requiring a shallower etch to form the oxidation trench. The HCG can be used to introduce new functionality to structured light and time of flight systems. By designing the polarization distribution within the array, the system can be modified to reduce noise or introduce new features to the reconstruction algorithm.

The fabrication process leverages the existing aperture oxidation step to form the oxide spacer, minimizing the amount of complexity that is added to the process. The OS HCG does require a lithographic critical dimension of roughly 200 nm, but this is achievable with a KrF stepper – a mature technology that has been used for decades in Si manufacturing. Alternative methods, such as electron beam lithography or nanoimprint lithography, could also be used to pattern the HCG.

The wall plug efficiency of the first two generations of devices is improved from only 3.9% to over 35%. The repeatability of the DUV lithography process is analyzed by the yield of lasing devices, and the results demonstrate the capability to produce HCGs with bar widths as small as 220 nm and air gaps as small as 200 nm. The HCG designs with the highest performance and yield are fabricated again to verify their reproducibility, and the results from the second chip supported the results of the initial fabrication. The first high-efficiency HCG VCSEL arrays demonstrate the scalability of the oxide spacer HCG architecture. The yield and uniformity of the DUV process still requires improvement, but this will come from design for manufacturing and process optimization for a single HCG design with a full 6” wafer toolset. Higher emitter yield will lead to better array power scaling, since the large arrays had reduced power output due to non-functioning emitters.

5 Conclusions and Future Work

The simulations and experimental results presented in this work demonstrate design improvements for VCSELs used in multiple systems for 3D sensing.

In swept-source optical coherence tomography, the tuning range of the light source places a limit on the resolution of the system. A tunable VCSEL makes an excellent light source in this application due to the wide free spectral range that is produced by the short Fabry-Perot cavity. By designing the semiconductor cavity to be antiresonant at the center of the tuning range and resonant at the edges of the tuning range, the effective length of the VCSEL cavity is made even shorter at the edges of the tuning range. This phenomenon increases the tuning range by a factor of up to two. Although the semiconductor cavity is antiresonant, the complete VCSEL cavity still supports a resonance with a low threshold material gain across the entire free spectral range of the cavity. The air cavity dominant design principle is extremely flexible, so it can be easily integrated with other features that increase free spectral range in the future. The free spectral range can be increased further by removing the upper DBR, replacing the lower DBR with a fully oxidized DBR, and shortening the active cavity to $\lambda/2$. The design can also be applied to optically pumped VCSELs, which can have even wider tuning ranges since they do not need contact layers or doping, which increase the length and internal loss of the cavity.

Time of flight and structured light sensing are popular choices for face and gesture recognition in hand-held devices. Since battery capacity and space are limited, these systems require highly efficient electrically pumped light sources that can be densely integrated into arbitrary arrays. By these criteria, VCSELs are the ideal choice for this application. By replacing the DBR with a thin oxide spacer HCG reflector, the epitaxial thickness and thus cost of a VCSEL arrays can be reduced significantly. This work experimentally demonstrates the first oxide spacer HCG VCSEL. Redesigning the HCG to consider fractional power output and manufacturability in addition to reflectance yields an HCG VCSEL with a wall plug efficiency over 35% - the highest efficiency to date. Finally, the oxide spacer HCG VCSEL process is used to demonstrate initial arrays of up to 100 emitters with a wall plug efficiency of more than 20%. In the future, by further refining the epitaxial structure, grating dimensions, and metallization process, the efficiency can be increased to match and even exceed the single device efficiency of 35%.

The oxide spacer HCG VCSEL also represents a new platform for VCSELs integrated with optics. The simplest quality to leverage is the polarization of the light emitted from an HCG VCSELs. If ambient light is unpolarized – as it often is indoors and in diffuse lighting conditions – then the ambient noise level can be reduced by a factor of two by placing a polarizer that matches the emission of the VCSEL in front of the camera. Alternatively, the HCG polarization can be assigned to different angles on different elements of the array, which could be used to introduce randomness or create points that can be used to originate the pattern recognition algorithm. More advanced designs could be used to tailor the far-field pattern of the VCSEL to produce narrow beams for structured light or uniform illumination patterns with a well-defined field of view for time of flight.

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