Design, Development and Applications of Portable Field Emission Devices

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Technical Report No. UCB/EECS-2021-224
http://www2.eecs.berkeley.edu/Pubs/TechRpts/2021/EECS-2021-224.html

December 1, 2021

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by

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A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering - Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Vivek Subramanian, Chair
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Fall 2019

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Abstract

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Vacuum tubes were integral to the rise of electronics in the 20th century, enabling the development of many core technologies, such as radar, television, radio and audio communications and early computers. However, the invention of the solid-state transistor, and subsequent integrated circuit technology, meant that electronics could be smaller, cheaper, faster and more reliable than vacuum tubes. Because of this, vacuum tubes were ultimately superseded by solid-state devices and thus began the trend of rapid miniaturization of electronics. Interestingly, although solid-state devices supplanted vacuum tubes in most domains, the trend towards miniaturization also enabled the emergence of vacuum microelectronics – a field that uses modern solid-state microfabrication techniques to develop micrometer-scale vacuum-based devices, or field emission devices. The emergence of this field was motivated by the desire to leverage some of the unique performance advantages offered by vacuum-based devices. Indeed, vacuum as an electron conduction medium offers some unique technical advantages over solid-state transport, such as ballistic electron transport, the ability to operate at high frequencies and robustness in harsh conditions, such as extreme temperatures, extreme pressures and high radiation environments. However, in order to leverage these features and enable widespread and practical use of field emission devices in electronics, on-chip ambient operation device architectures directly integrated on Si must be designed.

Here, the design and application of portable field emission devices that can operate in ambient conditions will be presented and discussed. This includes the first demonstration of vacuum-sealed fully integrated diode and triode field emission arrays that are developed in a scalable, BEOL-compatible process directly on Si. The device architectures demonstrate effective vacuum-sealing and gate-modulated field emission, with the ability to block voltages of up to 200 V. High operating voltages and low currents make these devices useful in high voltage drive circuits for MEMS actuators. Then, a novel device architecture for a portable electron source is presented. A fabrication process is developed to integrate graphene as an extraction electrode for field emission arrays on Si. Operation of this device is the first demonstration

of a fully integrated field emission array utilizing graphene as both an extraction electrode and electron-transparent vacuum seal, enabling in-air extraction of electrons. The type of on-chip portable electron source developed here presents a unique method for using field emission-based electron sources in non-ideal conditions, unlocking applications ranging from ion thrusters for microrobotics to environmental microscopy.

To those who struggle with anxiety,
and to those who support them

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Acknowledgments

This dissertation would not have been complete without the support of many individuals, both in my professional and personal life. Before I even understood what research was, Professor Andrea Armani took the time to mentor me as a rising sophomore in college. In hindsight, the three years I spent with her prepared me extremely well for graduate school and laid the foundation for the rest of my career. The opportunity to explore the novel ideas and concepts in this work was provided to me by my Ph.D. advisor, Professor Vivek Subramanian, who allowed me to study completely uncharted territory in his group. Under his tutelage, I gained a deep sense of confidence in both my academic and personal pursuits. I know now that if I want to get something done, I will get it done – a powerful lesson that I will always carry with me, particularly in times of doubt. I have also been fortunate enough to have had another great mentor in my co-advisor, Professor Kris Pister, who inspired me to explore my work in a playful manner. His guidance helped refine the ideas that resulted in some of the most interesting portions of this work, that I hope move him one step closer to his dreams. I also would not have made it through this journey without support from my friends. In particular, Carlos Biaou made all the late nights on campus enjoyable and became the little brother I never had; and Juan Pablo Llinás never failed to keep me entertained at any time of the day. I am also deeply indebted to all of my amazing friends outside of graduate school – no words are sufficient for expressing my gratitude. Our travels, adventures, and excursions meant more to me than I probably express and kept me sane during difficult times. Special thanks to Calvin Robert Lee, for making me believe I've never had anything to doubt in myself and for knowing me well enough to help me write my dedication. Finally, to my brother, Rishi, and my parents, Ruli and Bimal, for their truly unwavering support.

Chapter 1

Introduction

The miniaturization of electronics is a clear technological trend that has enabled the widespread use of electronics in all areas of society. Accelerated by the invention of the solid-state transistor, miniaturization has taken electronics from the early days of vacuum tubes to the integrated circuits that are ubiquitous today, in applications such as smartphones, televisions and computers. While integrated circuit technology has superseded vacuum tubes in many domains, the trend towards miniaturization also led to the emergence of vacuum microelectronics –a field that utilizes solid-state microfabrication techniques to develop devices based on electron transport in vacuum. The ability to use vacuum microelectronic devices alongside solid-state technology has the potential to not only address the limitations faced by solid-state technology, but also enable new applications in electronics. Thus, the focus of this work is to develop on-chip ambient operation micrometer-scale vacuum-based devices directly on Si, with the goal of enabling their widespread and practical use in electronics. In this chapter, the evolution of vacuum-based technology is discussed, including a section on the fundamental physics of electron emission to outline the principles upon which vacuum microelectronic devices operate. Emerging applications are reviewed and discussed in the context of other key technological platforms, such as microelectromechanical systems (MEMS). With these applications in mind, the fundamental motivation and key objectives of this work are introduced, and the chosen methodology of study is presented. This chapter concludes with an outline of the thesis organization.

1.1 Historical overview of vacuum microelectronics

Vacuum tubes were integral to the rise of electronics in the twentieth century. The simplest form of a vacuum tube is the diode, developed in 1904 by John Ambrose Fleming. In the diode, a heated filament, or cathode, in vacuum emits electrons that are attracted to a positively charged electrode, or anode, resulting in current flow between the cathode and anode. In 1906, Lee de Forest invented the triode with the addition of a third electrode, or grid, that enabled the flow of electrons between the cathode and anode to be modulated

Table 1.1: Comparison of Solid-state Devices and Vacuum Microelectronics [1]–[6]

Property	**Solid-state Devices**	**Vacuum Microelectronics**
Interface	solid/solid	solid/vacuum
Electron transport mechanism	Drift-diffusion, with velocity saturation (v$\sim 10^7$ cm/s)	Ballistic transport (v$\sim 10^{10}$ cm/s)
Electron energy	a few eV	a few eV to keV
Cutoff frequency	$<$ 90 GHz (Si), $<$ 500 GHz (SiGe), $<$ THz (SiGe FinFETs)	$>$ THz
Power handling	$<$ 30 kW (Si IGBTs)	kW to MW (klystron, magnetron)
Radiation hardness	1 kRad (Si), 700 MRad (SOI)	radiation-immune
Temperature sensitivity	$<$ 125°C	$\sim$ 500°C

by the potential at the grid. The triode enabled new operations like rectification, switching and amplification. These inventions became critical components in early electronic circuits, enabling the development of core technologies such as radar, television, radio and audio communications, and early computers. However, vacuum tubes were ultimately superseded by solid-state devices after the invention of the transistor in 1947, which used semiconductor materials to create an electronic switch. The development of integrated circuit technology soon followed, in which solid-state devices are assembled in high-throughput, inexpensive, fast processes to form electronic circuits. Vacuum tubes were large, inefficient, power-hungry and expensive in comparison to solid-state devices. As a result, solid-state electronics began to dominate in the 1980s, particularly in the areas of low-power electronics and computing [7]–[9].

It is important to note, however, that the transition from vacuum tubes to solid-state devices was driven by the increased reliability, small size and low cost of solid-state devices in comparison to vacuum tubes, not by the superiority of semiconductors as an electron transport medium. In fact, vacuum is an ideal medium for electron transport, given that there is nothing to disrupt charge flow. In contrast, electrons traveling in a semiconducting material experience collisions and scattering that cause power loss and reduce signal quality; this becomes increasingly problematic in high-frequency and high-power regimes. By leveraging vacuum as an electron transport medium, vacuum-based devices can offer several technical advantages over their solid-state counterparts: ballistic electron transport, the ability to sustain higher current densities and higher frequencies, and robustness in extreme conditions, such as high temperature or radiation [1], [2]. A comparison of solid-state devices and vacuum microelectronics is provided in Table 1.1. With these attractive features in

mind, a new generation of vacuum-based devices emerged beginning in the 1960s, catalyzed by two key breakthroughs [7]:

1. The development of solid-state microfabrication techniques for large-scale on-chip integration of micrometer-scale solid-state devices. The same techniques could now be applied to develop micrometer-scale vacuum-based devices.

2. The discovery and use of field emitters as an electron source in vacuum-based devices. In contrast to the heated filaments in traditional vacuum tubes, field emission cathodes emit electrons under high electric fields at room temperature, dramatically reducing their power consumption as compared to thermionic cathodes used in early vacuum tubes.

From these advancements and discoveries, the field of vacuum microelectronics emerged. The goals of this new technology are to build micrometer-scale devices that operate with ballistic electrons in vacuum by leveraging the microfabrication technology developed for the semiconductor industry. By combining the performance advantages of electron transport through vacuum with the scalability and manufacturability of integrated circuit technology, vacuum microelectronic devices enjoy the best of both worlds. This has generated a renewed interest in the development of vacuum-based devices for many new applications, to be discussed after a review of the fundamental physics of field emission.

1.2 Field emission fundamentals

The successful development of field emission cathodes played a critical role in the emergence of vacuum microelectronics by enabling a significant reduction in power, size and cost of the cathode as compared to traditional thermionic cathodes. In this section, a description of the various types of electron emission is provided and the fundamental physics of field emission is discussed in order to clearly outline the significance of field emission in the development of vacuum microelectronic devices.

1.2.1 Electron emission

Fundamentally, electron emission refers to a process by which an electron escapes from a solid or liquid surface into vacuum. There are multiple well-established mechanisms of electron emission, illustrated in Fig. 1.1. In some cases, electrons must acquire sufficient energy to overcome the workfunction barrier, which indicates the amount of energy required by an electron to escape a given surface. For example, in thermionic emission, the source is heated to very high temperatures, typically greater than 1000 K, such that the electrons gain enough kinetic energy to overcome the workfunction barrier [10]. In photo-electron emission, a surface is illuminated by photons with energies higher than the workfunction barrier; the

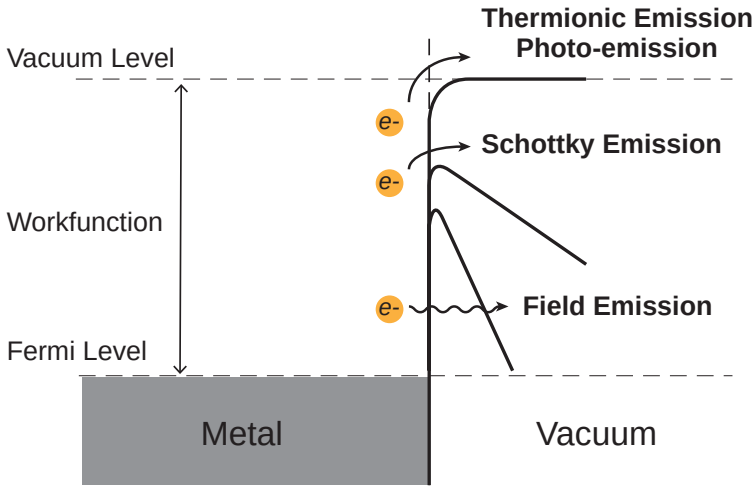


Figure 1.1: Various types of electron emission, adapted from [11].

energy transfer from the photons to the electrons enables the electrons to overcome the work-function barrier [11]. Field-electron emission, or field-emission, is different in that electron emission occurs due to quantum-mechanical effects that only occur under the application of a high electric field, on the order of 10^7 V/cm^{-1} [12]. At such high fields, the solid-vacuum potential barrier is reduced, as illustrated in Fig. 1.1. With only a narrow energy barrier remaining between the electrons and vacuum, the probability of quantum-mechanical tunneling from the solid into vacuum becomes significant and results in measurable electron emission. Schottky emission, or field-enhanced thermionic emission, occurs when both high electric fields and high temperatures are present such that the overall energy required to overcome the workfunction barrier is lower than that required by either thermionic emission or field emission alone [13].

It can now be seen that because traditional vacuum tubes used thermionic cathodes, the need for extremely high temperatures resulted in high power consumption that ultimately made them impractical when compared to the low power consumption of solid-state devices. In contrast, field emission devices operate at room temperature, enabling vacuum-based devices to once again compete with solid-state technology in some domains.

1.2.2 Fowler-Nordheim tunneling theory

The phenomenon of field emission was first modeled by Fowler and Nordheim in 1928 and aptly named Fowler-Nordheim theory [14]. The theory outlines a method for calculating the field emission current density as a function of the applied electric field and is based on the following assumptions [12]:

- The emitter source is a metal with an electron distribution that obeys the Sommerfeld free electron model with Fermi-Dirac statistics.
- The potential within the metal is constant and not affected by the external electric field.
- The metal is planar, so only the one-dimensional problem is considered. The accuracy of this assumption relies on the fact that the thickness of the potential barrier in the high fields considered here, on the order of 10^{-10} V/cm, is typically several orders of magnitude smaller than the radius of the emitter. Thus, the external electric field in the vacuum gap is taken to be uniform along the surface of the emitter.
- Only ordinary and low temperatures are considered, with the final calculation performed at the limit T = 0 K. This assumption allows the electron distribution to follow Sommerfeld's formula.

Given the assumptions above, the current density as a function of electric field is given by the following equation:

$$J = e \int_0^\infty n(E_x) D(E_x, F) dE_x \tag{1.1}$$

where J is the current density, e is the electron charge, $n(E_x)$ is the electron supply function, E_x is the part of the electron kinetic energy normal to the surface, and F is the applied electric field. $D(E_x, F)$ is the barrier transparency, or probability of electrons tunneling through the barrier, and is calculated using the semi-classical method of Wentzel-Kramers-Brillouin (WKB) approximation.

The result of the integral in (4.1) gives an equation for the tunneling current density in the following form, known as the Fowler-Nordheim equation:

$$J = aF^2 e^{-b/F} \tag{1.2}$$

where a and b are constants.

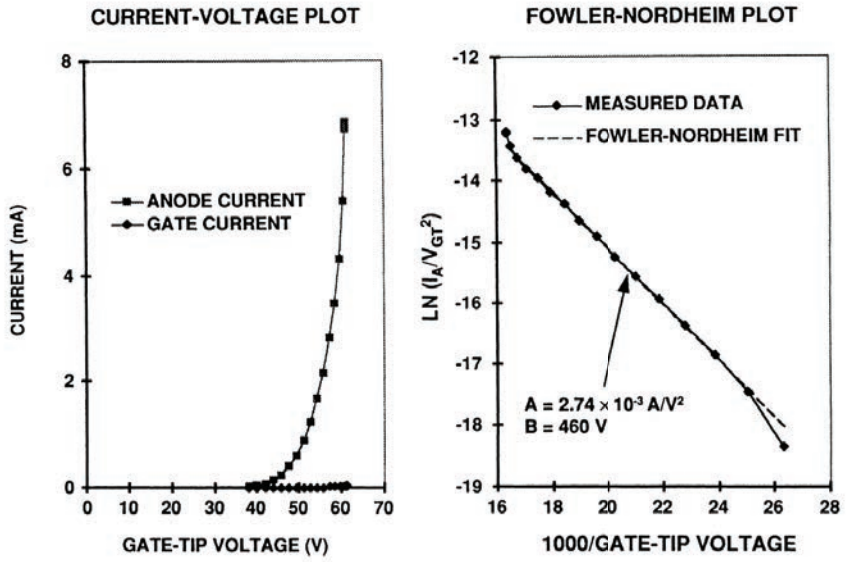
The current density is related to the current, I, by multiplying it by the total emission area, α:

$$J = \frac{I}{\alpha} \tag{1.3}$$

The applied electric field is related to the applied voltage, V, through the inter-electrode distance, d:

$$F = \frac{V}{d} \tag{1.4}$$

Using (1.3) and (1.4), the Fowler-Nordheim equation can be re-written to give the current as a function of applied voltage:



(a) (b)

Figure 1.2: Representative (a) current-voltage and (b) FN plot for a microfabricated field emitter array [16].

$$I = aV^2 \exp(-b/V) \tag{1.5}$$

$$a = \frac{A\alpha\beta^2}{1.1\phi} \exp\left[\frac{1.44 \times 10^{-7} B}{\sqrt{\phi}}\right] \tag{1.6}$$

$$b = \frac{0.95 B \phi^{3/2}}{\beta} \tag{1.7}$$

where I is the current [A], V is the applied voltage [V], and a and b are parameters defined by the workfunction ϕ [eV], the effective emission area α [m^2], the local field enhancement factor β [m^{-1}], and the constants A and B, equal to 1.54×10^{-6} and 6.87×10^7, respectively [15].

As can be seen from (1.5), the current has an exponential dependence on the applied voltage. Typical $I - V$ behavior for a field emission device is plotted in Fig. 1.2(a). Fig. 1.2(b) is a plot of the same data using $(1/V)$ as the x-variable and $ln(I/V^2)$ as the y-variable, known as a Fowler-Nordheim (FN) plot. By re-writing (1.5) as follows

$$\ln\left(\frac{I}{V^2}\right) = \ln a - \frac{b}{V} \tag{1.8}$$

it can be seen that a linear fit of the data in the FN plot enables device characterization through extraction of the coefficients, a and b, from the slope and y-intercept of the plot. FN plots are critical for confirming that the experimental data can be described by field emission, rather than thermionic emission, which shows a similar exponential growth in current, but as a function of temperature rather than voltage. The data in the FN plot will fall along a straight line only if the exponential growth in current is primarily due to the applied voltage and can be described by Fowler-Nordheim theory, thereby validating field emission as the observed conduction mechanism.

1.2.3 Modifications to the Fowler-Nordheim equation

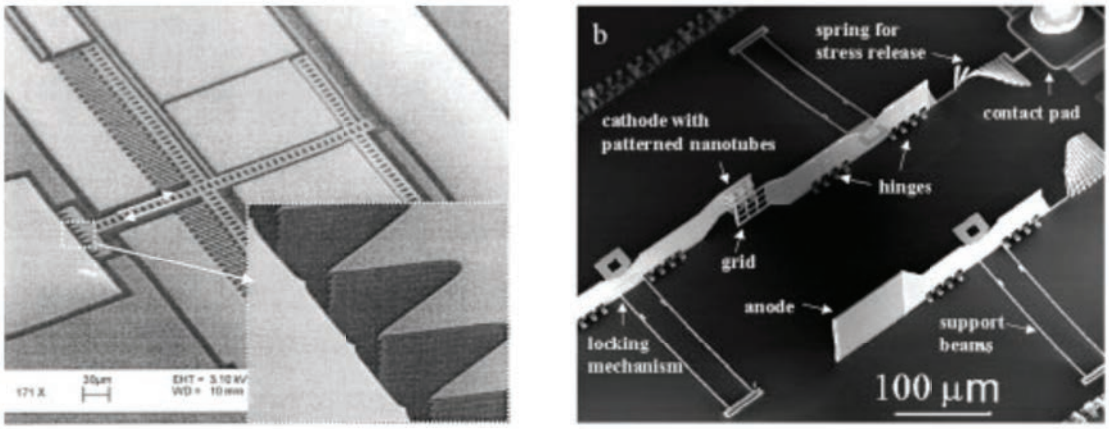
As discussed previously, field emission is a quantum-mechanical phenomenon that only occurs under high fields, on the order of 10^7 V/cm^{-1} for a flat metal surface, translating to extremely high applied voltages. In order to produce these fields at lower applied voltages, most field emission tips have a very small radius of curvature. This is designed to take advantage of the well-known geometrical enhancement of electrical fields around surfaces of high curvature [12]. The observed effect, known as field amplification, is represented by the field enhancement factor, β, [17] where:

$$F = \frac{\beta V}{d} \tag{1.9}$$

The use of geometrical structures exhibiting field enhancement at the tip means that the electric field region will be highest at the tip and quickly decrease moving away from the tip. It should be noted that this violates one of the assumptions in Fowler-Nordheim theory, which states that the external electric field in the vacuum gap is uniform along the entire surface. However, modifying the FN equation by including a field enhancement factor in the equation for the applied field enables its use in calculating emission from tips, rather than exclusively planar surfaces. Throughout this work, we will use (1.5) and (1.9) for device characterization.

1.3 Applications of vacuum microelectronics

Field emission devices have enabled many new applications, ranging from flat panel displays [19] to electron sources for microscopy, mass spectrometry and lithography [20]. Driven by the need for miniaturization, the development of field emission devices that can be integrated into existing CMOS and MEMS platforms has sparked significant interest in the vacuum microelectronics community. Within the vacuum microelectronics field, this has led to the development of many MEMS-compatible field emission technologies, including lateral field emission devices integrated with MEMS actuators [17], microtriodes for power amplification [18], and CNT-based neutralizers for micro-propulsion [21]. Here, we discuss two areas



(a) (b)

Figure 1.3: Examples of field emission devices built using MEMS design and fabrication principles. (a) Microelectromechanical field emission device (MEMFED) composed of lateral field emission tips with a cathode-anode separation that can be mechanically tuned using a comb-drive actuator [17]. (b) Carbon nanotube-based microtriode developed using silicon micromachining and assembled via polysilicon hinges [18].

of development for field emission devices with specific applications in MEMS technology in which field emission devices have the potential to outperform solid-state technology.

1.3.1 High voltage devices for MEMS actuators

The MEMS market has seen explosive growth over the last few decades, as MEMS-based technologies are in high demand for applications such as the Internet of Things (IoT) and portable electronics. Among these technologies are MEMS-based sensors and actuators, which comprise 80% of the $12.2 billion semiconductor sensor/actuator market [22]. The advent of MEMS-based actuators has enabled the success of many research and commercial endeavors, particularly in microrobotics systems, which rely on actuators to implement actions such as walking, crawling or flying [23]–[25]. Several different types of actuators exist that operate on varying actuation mechanisms, including electrostatic, electrothermal, electromagnetic and piezoelectric [26]. Among these, electrostatic and piezoelectric actuation methods are preferred for varying reasons –electrostatic actuators have fast response times and are easy to manufacture and integrate [23], while piezoelectric actuators have high bandwidth and power density [27].

Both of these actuation methods require high actuation voltages (ranging from 10 V to 300 V), albeit very low current (ranging from pA to nA) [23]. Such high actuation voltages

necessitate drive circuits that contain high voltage switches to implement topologies like boost and flyback converters [27]–[29]. This leads to significant switching and conduction losses that reduce overall efficiency and creates additional challenges in microrobotics applications where size and weight constraints are critical, as the high voltage drive circuits can account for a significant increase in the overall size of the system [27].

The high voltage switches utilized in these implementations rely on Si-based high voltage MOSFETs, which typically have high on-resistance in order to sustain higher voltages, leading to a large source of inefficiency and loss. While Si is an ideal candidate for ease of integration, it is best-suited for low-power and low-voltage applications, as the material properties of Si limit its ability to handle high voltages. The solid-state community has turned to GaN and SiC for high voltage applications, but these materials are costly and not easily integrated with silicon CMOS [30], [31]. Oftentimes, these high-performance technologies are discretely connected to Si-based control circuits, increasing packaging costs and reducing performance by introducing additional parasitic capacitances, as well as eliminating the advantages of a monolithic integrated circuit.

Field emission devices have the potential for achieving efficient, high voltage operation because vacuum can sustain much higher voltages than semiconductor materials; in addition, ballistic transport of electrons has the added benefit of fast switching times. This has led to studies of field emission devices for high voltage, high power and high frequency applications [32]–[34]. Therefore, developing field emission-based high voltage devices monolithically integrated on Si to drive MEMS actuators has the potential to increase the efficiency of existing implementations, while still maintaining excellent manufacturability and ease of integration.

1.3.2 Portable electron sources

The discovery of field emission also revolutionized the development of electron sources, enabling their use in low-power and low-voltage applications [35]. As we have seen from the previously cited examples, field emission devices can be readily miniaturized and integrated into CMOS and MEMS platforms, enabling the development of portable electron sources. As a result, there have been significant efforts to develop MEMS-compatible field emission electron sources, including space charge neutralizers [21], electron-impact ion sources [36], micro-ionizers for mass spectrometry [37], and x-ray sources [20], [38].

One of the major challenges in the development of on-chip field emission electron sources is operation of the system outside of high-vacuum environments to enable a portable solution. There have been some attempts to operate field emitters in atmospheric conditions, but only with limited success, as these solutions require highly specialized materials [39] or strict conditions for the operating ambient [21], [40]. In general, field emitter performance degrades rapidly outside of vacuum, as the emitted electrons ionize surrounding gas atoms that subsequently bombard the cathode, causing physical sputtering of the cathode material [7], [12]. Long-term reliability therefore requires field emitters to be maintained in a vacuum-sealed cavity. Attempts have been made utilizing various vacuum-sealing methods, but none

of these techniques allow for extraction of electrons outside of the vacuum-sealed cavity or package [41]–[43]

This has led to active research on the use of electron-transparent gas-impermeable membranes designed to maintain vacuum-sealing while still allowing the transmission of electrons, using materials like silicon nitride and graphene [44], [45]. While these materials have shown varying levels of gas impermeability and electron transparency, there has been no demonstration of a fully integrated system utilizing these membranes. Ultimately, developing a fully integrated on-chip field emission-based electron source that demonstrates air-ambient operation can unlock the widespread use of field emission devices for MEMS-based electron sources. This would enable the use of electron sources in applications ranging from portable mass spectrometry [46] to ion thrusters for microrobotics [47].

1.4 Methodology of study

Much of the research on field emission devices has focused on improving various field emission properties and characteristics, ranging from the original Spindt tips [15] to today's high performance nanomaterials [48]. In these studies, the emitters are characterized in non-integrated experimental setups, where the cathode, gate and anode are physically isolated electrodes. While this has enabled significant advancements in understanding field emission physics and identifying ideal cathode materials, it has delayed the use of field emission devices in Si-based applications. In order to truly utilize field emission devices in CMOS and MEMS technologies, fully integrated devices must be developed and characterized. This requires integration of the cathode, gate and anode on the same Si substrate as well as the ability to operate the system in ambient conditions rather than high-vacuum environments.

A survey of the literature indicates that there are very few reports of integrated field emission devices, with even fewer demonstrating operation in atmospheric conditions. Garner, et al., published one of the early demonstrations of an integrated field emission triode [49] and Natarajan, et al., demonstrated improved triode performance using carbon nanotubes [32]. However, both device structures require high vacuum for operation and were developed in processes that are difficult or impossible to integrate into conventional silicon integrated circuit fabrication flows. Driskill-Smith, et al., reported atmospheric operation of field emission diode and triode devices based on Au nanopillars in an integrated structure [39]. While moderate performance is demonstrated for low-voltage operation, no clear advantages to solid-state devices are indicated and the process utilizes materials and techniques that preclude Si integration. As discussed in Section 1.3.2, attempts to operate field emitters in non-vacuum environments generally result in poor performance and limited long-term viability. Other attempts have been made utilizing various vacuum-sealing methods to achieve atmospheric operation of the system, but these reports either do not demonstrate triode structures, utilize expensive or complex vacuum-sealing methods, or require high-temperature processing that precludes back-end-of-line (BEOL) compatibility [42], [43], [50], [51]. Moreover, these studies are few and far between. The lack of focus on the development of field emission

devices in real-world settings has ultimately delayed its use in applications [52].

This reality informs the fundamental motivation for this work: to enable the widespread and practical use of field emission devices in Si-based applications. Doing so requires the development of fully integrated structures utilizing methods for vacuum-sealing that are compatible with conventional silicon integrated circuit fabrication flows. Thus, this is the key objective of this thesis, which aims to develop practical, portable fully integrated on-chip field emission devices with air-ambient operation. To this end, we demonstrate the potential for using these devices in high voltage drive circuits and portable electron sources, which can be utilized for the aforementioned MEMS applications.

1.5 Organization

In Chapter 2, the Spindt-type field emitter is introduced as the foundation for the emitters developed in this work. The fabrication process for fully integrated diode arrays is outlined, highlighting critical features of the device geometry and key results from process optimization. The electrical performance is discussed and design guidelines for future generations of devices are provided.

Chapter 3 presents the three-terminal analog of the devices presented in Chapter 2, outlining the fabrication and characterization of fully integrated triode arrays. The electrical performance is discussed, with a focus on gate modulating capabilities, and design guidelines are provided. Together with Chapter 2, this demonstrates vacuum-sealed fully integrated diode and triode field emission arrays, with potential for use in high voltage drive circuits for MEMS actuators.

The same Spindt-type emitters are then integrated with graphene, which is utilized as an atmospheric seal and electron-transparent gate, to develop an on-chip portable electron source. Chapter 4 begins by discussing the development of the integration process, consisting of cathode preparation, graphene preparation and a dry transfer process, and presents the final device structure. Results from process characterization are presented and discussed. The second half of Chapter 4 presents the results of electrical characterization of the integrated graphene-Spindt device architecture. This is divided into three aspects of the device performance –electron extraction, atmospheric sealing and electron transparency. These results ultimately demonstrate in-air extraction of electrons from an on-chip electron source, with potential for use as ionizers for MEMS microrobotics or portable mass spectrometry.

A concluding chapter, Chapter 5, summarizes the contributions of this work. Recommendations for areas of further investigation are discussed and the potential future of vacuum microelectronics is outlined.

Chapter 2

Diode Field Emission Arrays: Design, Fabrication and Characterization

Vacuum nanoelectronics are a unique approach for achieving high voltage devices on Si for MEMS actuators, as discussed in the previous chapter. Vacuum has the potential to sustain higher voltages than semiconductor materials, making vacuum-based devices an attractive alternative to solid-state devices for high voltage applications. However, in order to truly utilize vacuum devices for MEMS technology, fully integrated devices must be developed and characterized; this requires integration of the cathode, gate and anode on the same Si substrate, with the ability to operate in ambient conditions rather than high-vacuum environments. The majority of research, however, has focused on non-integrated field emission structures. To date, there have been no reports of integrated field emitters that do not require high vacuum operation, are developed in a MEMS / CMOS compatible process and demonstrate a path towards scalability, let alone in the context of high voltage applications.

In this chapter, a fabrication process for the development of diode field emission arrays is developed and described in detail. Notable findings from extensive process characterization are discussed and key features of the final device geometry is highlighted. Then, the results of electrical characterization of the field emission arrays are presented to confirm field emission-based operation, effective vacuum-sealing and suitability for high voltage applications. The device structure developed here will then be used to develop triode field emission arrays, discussed in Chapter 3.

2.1 Background information

The goal of the first portion of this work is to develop a field emission-based device with the following features:

1. Fully integrated electrodes
2. Ambient operation

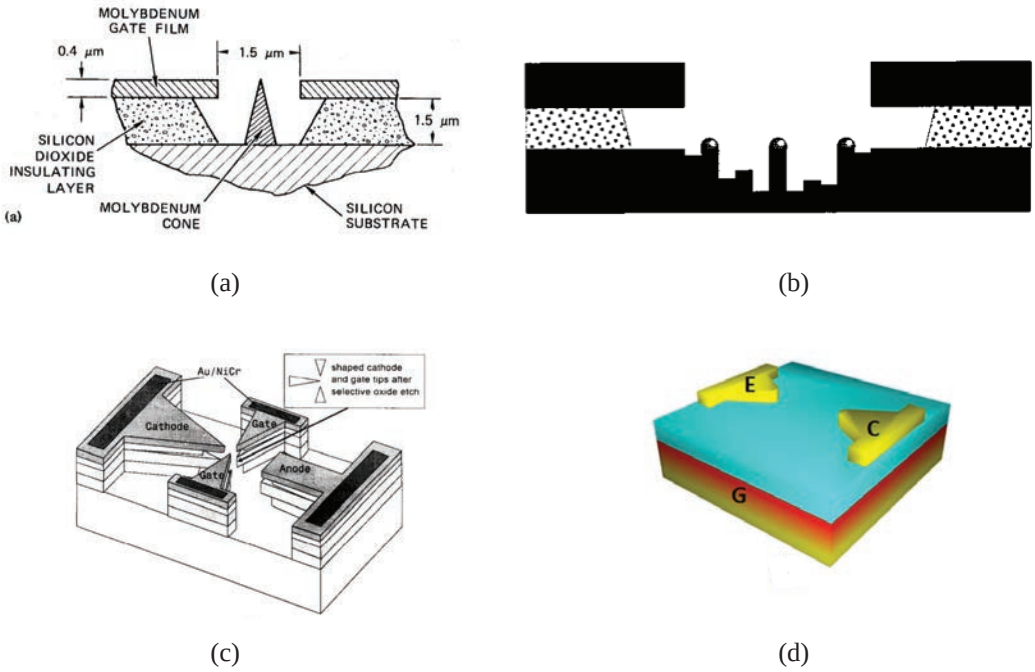


Figure 2.1: Examples of vertical and lateral field emission devices. Vertical designs include (a) metal tips, such as the Spindt-tip cathode and (b) nanostructures, such as AuPd nanopillars. Lateral designs typically consist of (c) Si_3N_4/SiO_2/poly-Si stack (d) SOI patterning.

3. High voltage capability
4. Scalability
5. CMOS compatibility

To develop such a device, either a vertical or lateral structure can be utilized. Two examples of vertical structures are shown in Fig. 2.1(a) and (b). Fig. 2.1(a) is the first demonstration of a microfabricated field emission device, called the Spindt cathode, which employs metal tips as electron sources [15]. A modification to this structure is to replace the metal cathodes with nanostructures, such as carbon nanotubes or nanopillars, such as that shown in Fig. 2.1(b) [39]. In addition to vertical designs, lateral structures have also been developed. Fig. 2.1(c) utilizes a silicon nitride, silicon dioxide and poly-silicon stack and the LOCOS process to define the anode, gate and cathode electrodes [53]. Fig. 2.1(d) utilizes an SOI wafer to form an insulated gate, while patterning the cathode and anode regions from the thin Si layer [2].

Of these configurations, the vertical Spindt-based structure is particularly well-suited for exploring the device concepts proposed in this work due to its manufacturability, scalability and compatibility with standard CMOS fabrication processes. The concept for this type of structure was first proposed by Shoulders in 1961, with the goal of developing large-area field emission sources based on microfabricated field emitters [54]. In 1968, Spindt, et al., published the first demonstration of a thin-film field emitter array, called the Spindt array [55]. The original Spindt geometry consisted of sharp molybdenum cones formed by e-beam evaporation of the metal into a cylindrical void in an alumina thin-film; as material is deposited, the aperture slowly shrinks in diameter, forming a cone with a sharp tip in the cavity. Extensive studies on Spindt-type emitters, both based on molybdenum as well as other metals, have demonstrated the ability to utilize reasonably small gate voltages (less than 100 V) to achieve high total emission currents (over 1 A) by leveraging field enhancement at the metal tips [15], [56]. In addition, Spindt-type emitters can be densely packed, resulting in high current densities (over 100 A/cm^2). The Spindt array has inspired many new devices, either utilizing hybrid structures with nanomaterials to enhance metal tip emission [57], [58] or utilizing a similar geometry of oxide cavities with novel field emitter materials, such as carbon nanotubes [39], [59].

The Spindt-based structure provides an excellent foundation for designing field emission-based high voltage devices for the following reasons:

1. It is a well-studied device in a non-integrated form factor, providing an excellent reference point for our studies.

2. The process is highly manufacturable, as the devices can be fabricated on Si using CMOS-compatible processing techniques and tools readily available in standard nanofabrication labs.

3. The Si substrate provides a built-in heat sink that may be critical for running at high voltages.

4. The insulation layer can be easily modified to increase blocking voltage capabilities.

5. The geometry is conducive to scaling, as it is designed to be a large-area field emission source.

Thus, the design of the devices fabricated in this work is based on the Spindt-type geometry, with a primary focus on developing fully integrated structures.

2.2 Device fabrication

2.2.1 Process flow

The starting substrate for the diode arrays is Arsenic-doped silicon with resistivity <0.005 Ω-cm. The fabrication sequence is illustrated schematically in Fig. 2.2 and follows the process

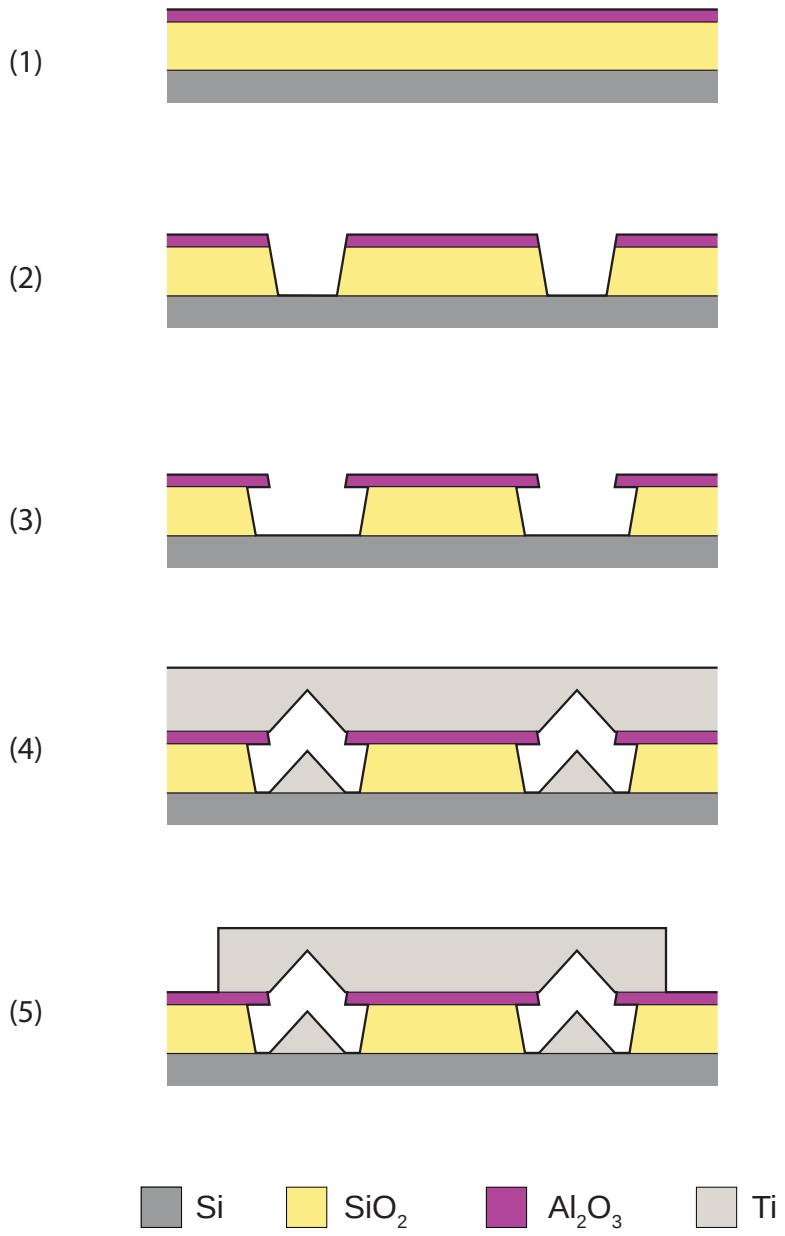


Figure 2.2: Schematic illustration of the fabrication process for the diode arrays.

outlined below:

1. Thin-film deposition: A layer of SiO_2 (thickness ranging from 500–800 nm) is thermally grown on the starting Si substrate at 1000 °C, followed by atomic layer deposition of a 140 nm thick layer of Al_2O_3 at 300 °C. Note that the thermal SiO_2 can be replaced a low temperature deposited SiO_2 to achieve BEOL-compatibility.

2. Patterning and reactive ion etch (RIE): Circular openings are patterned using deep UV (DUV) lithography, and cylindrical cavities are etched into the Al_2O_3 and SiO_2 films using RIE processes consisting of BCl_3/Cl_2 plasma and CHF_3/CF_4 plasma, respectively.

3. Lateral etch: The SiO_2 layer is laterally etched using HF vapor, leaving an alumina overhang at the top of the cavity.

4. Ti e-beam evaporation: An 800 nm thick layer of Ti is deposited by e-beam evaporation, during which the Ti emitters are formed as the cavities are sealed at the top at the evaporation process pressure of 10^{-7} Torr.

5. Device isolation: The top Ti layer is patterned and etched in an RIE process using BCl_3/Cl_2 plasma to isolate devices into arrays of 4x4, 16x16 and 32x32 emitters.

Fig. 2.3 shows the device layout for each die in the diode process. In addition to the varying array sizes mentioned above, additional design variables include the cavity aperture size and pitch (spacing between cavities). The aperture sizes chosen range from 700 nm to 1000 nm and the pitch is either 10 μm, 20 μm, or 40 μm. Excluding the lithography and processing steps required to etch standard alignment marks in the DUV stepper for alignment between layers, this process consists of two masks: one to define the cavities and one to pattern the Ti anode.

Fig. 2.4 shows a cross-sectional scanning electron micrograph (SEM) of an emitter in a diode geometry. The aperture size defines the height and width of the cathode, while the SiO_2 thickness defines the inter-electrode distance. The nature of the sealing process results in curvature in the anode that mirrors the shape of the cathode tip.

Fig. 2.5 is an image of a 6" wafer after all processing steps are complete. Each wafer holds 123 die, each containing multiple, electrically isolated device arrays of varying sizes. Our approach achieves wafer-level vacuum-sealing with high yield and excellent uniformity across the 6" wafer.

2.2.2 Process characterization

Extensive process characterization was done to achieve the desired geometries, with critical findings such as:

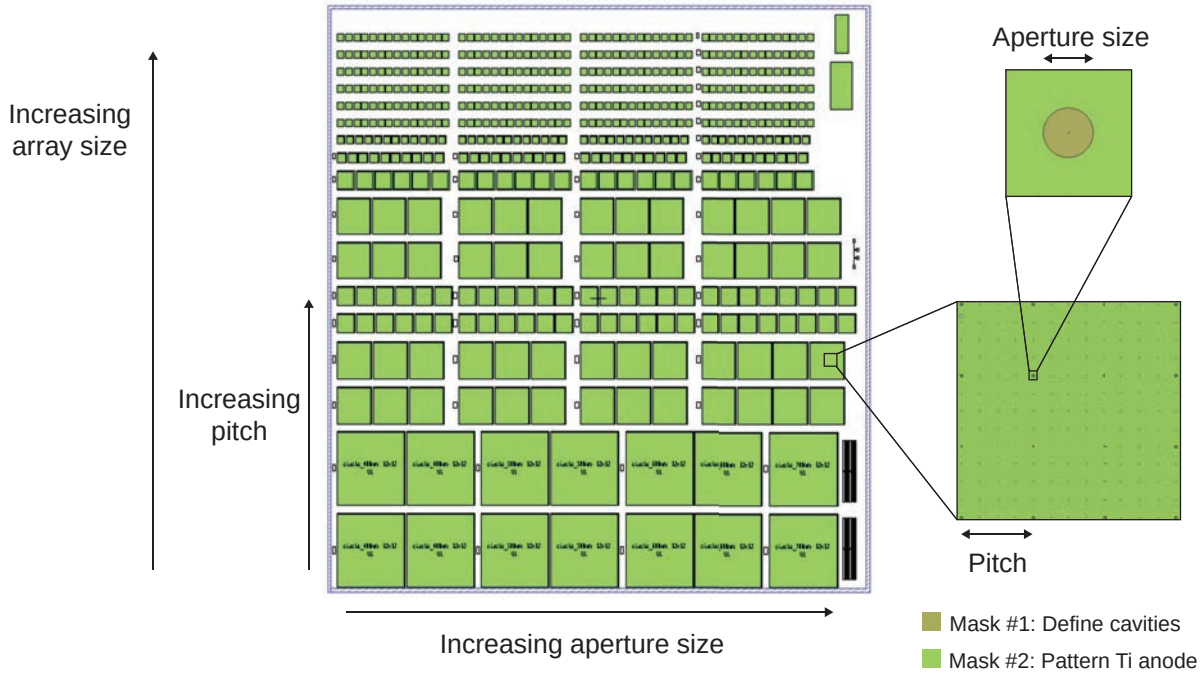


Figure 2.3: Mask layout for diode lithography steps.

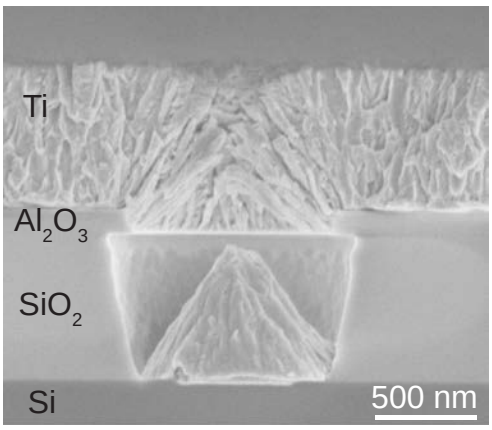


Figure 2.4: Cross-sectional SEM of a single emitter tip in a diode configuration.

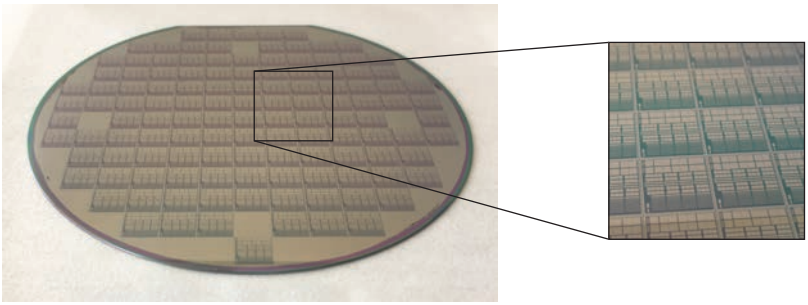


Figure 2.5: Top-down view of a 6" wafer after the full process sequence is completed; magnified views shows multiple, electrically isolated device arrays within each die.

1. Lateral etch time: The lateral etch of the SiO_2 (step 3) must be long enough to result in an alumina overhang at the top of the cavity. This is because the Ti is deposited at a perpendicular angle of incidence with respect to the substrate, as illustrated in Fig. 2.6(a). Thus, Ti will deposit on any portion of the SiO_2 not masked by the alumina layer. Cross-sectional SEMs for emitters formed using etch times of (b) 170 sec (c) 240 sec and (d) 480 sec are shown, with (d) resulting in the desired device geometry. The red arrows indicate the point along the sidewall that is not masked by the alumina layer, resulting in Ti deposition. The SEMs in (b) and (c) illustrate that an insufficient lateral etch results in Ti deposition along the cavity sidewalls, preventing proper formation of the emitters and shorting the cathode and anode.

2. Alumina thickness: The alumina layer must be greater than 90 nm to prevent pinholes from appearing in the film during the HF vapor etch, compromising the structural integrity of the layer.

3. Fluoropolymer removal process: An extensive cleaning process is required after the oxide etch, due to fluoropolymer deposition along the cavity sidewalls and across the surface of the wafer in the CHF_3/CF_4 plasma. The cleaning process utilized consists of a low-power O_2 plasma (75 W, 200 mTorr, 15 min) to break down the fluoropolymer, followed by immersion in solvent to remove resist from the etch step (Remover 1165 and PRS-3000 are used in this procedure). Failure to fully remove the deposited fluoropolymer compromises the quality, control and consistency of subsequent processing steps, such as etching and lithography, due to interference from the deposited film.

2.2.3 Key features of final geometry

The final device geometry utilizes Ti as the cathode material. During initial process development, however, Tungsten was used as the cathode material due to its lower resistivity.

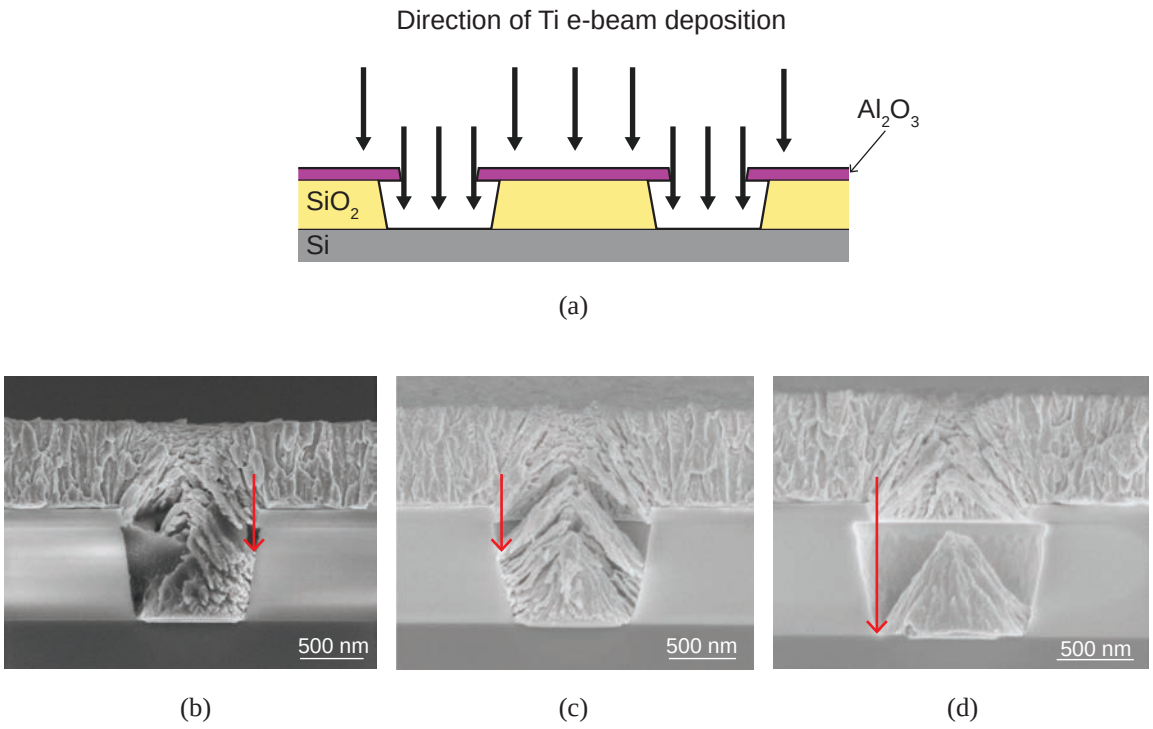


Figure 2.6: (a) Schematic illustration of Ti deposition direction with respect to substrate. Cross-sectional SEM of cavity and emitter after HF vapor etch of (b) 170 sec (c) 240 sec and (d) 480 sec. The direction of Ti deposition is indicated by the red arrows; it can be seen that the Ti deposits on the cavity sidewalls when the top of the cavity does not have an alumina overhang.

For the same aperture size, the Tungsten cathodes had a larger aspect ratio (height to width) than the Ti cathodes. However, Tungsten evaporation proved to be a difficult process due its high melting point and low vapor pressure, resulting in thin-films of poor quality. Thus, the choice of cathode material must be carefully considered, as this affects both the final size and shape of the cathode as well as ease-of-processing and compatibility with other processes.

It is also critical to use alumina as a masking layer, as it also serves to maintain the quality of the vacuum seal. In our initial experiments, we successfully fabricated diodes using doped poly-silicon in place of alumina. However, later characterization demonstrated that alumina is critical for maintaining vacuum-sealing. This will be discussed further in Section 2.3.

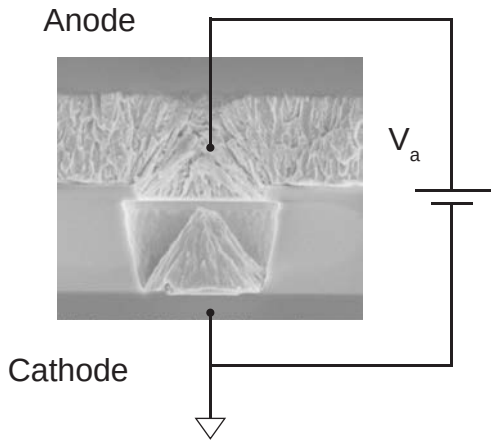


Figure 2.7: Test setup for diode configuration.

2.3 Results and discussion

2.3.1 Experimental setup

The diode arrays characterized in this work are biased per the configuration shown in Fig. 2.7. In the diode geometry, when a large positive voltage is applied to the anode while the cathode is grounded, electrons are emitted from the cathode towards the anode. Hence, the starting substrate is grounded and serves as the cathode contact, because it is electrically connected to the Ti cathode; the top Ti layer is positively biased and serves as the anode. All I–V measurements are carried out using a Keysight B1500A semiconductor device parameter analyzer. Measurements were taken in clean, dry air, as it was observed that surface leakage paths due to moisture could lead to shorting between the cathode substrate and Ti anode external to the device cavities in these unencapsulated devices.

2.3.2 On-state performance and trends

Fig. 2.8 shows typical I–V characteristics for a 32x32 array of emitters under forward bias and reverse bias. Diode operation is validated by the rectifying behavior of the profile. The exponential dependence of the current on applied voltage suggests a tunneling conduction mechanism is responsible for the forward current. The straight line characteristic of the FN plot, shown in Fig. 2.8 inset, confirms field emission as the tunneling conduction mechanism demonstrated by the diode arrays.

Measurements are also taken under 10^{-6} Torr vacuum at 77 K and 380 K to test the temperature dependence of the diodes. As can be seen from Fig. 2.9, the forward current does not increase with temperature, further validating that thermionic emission is not a

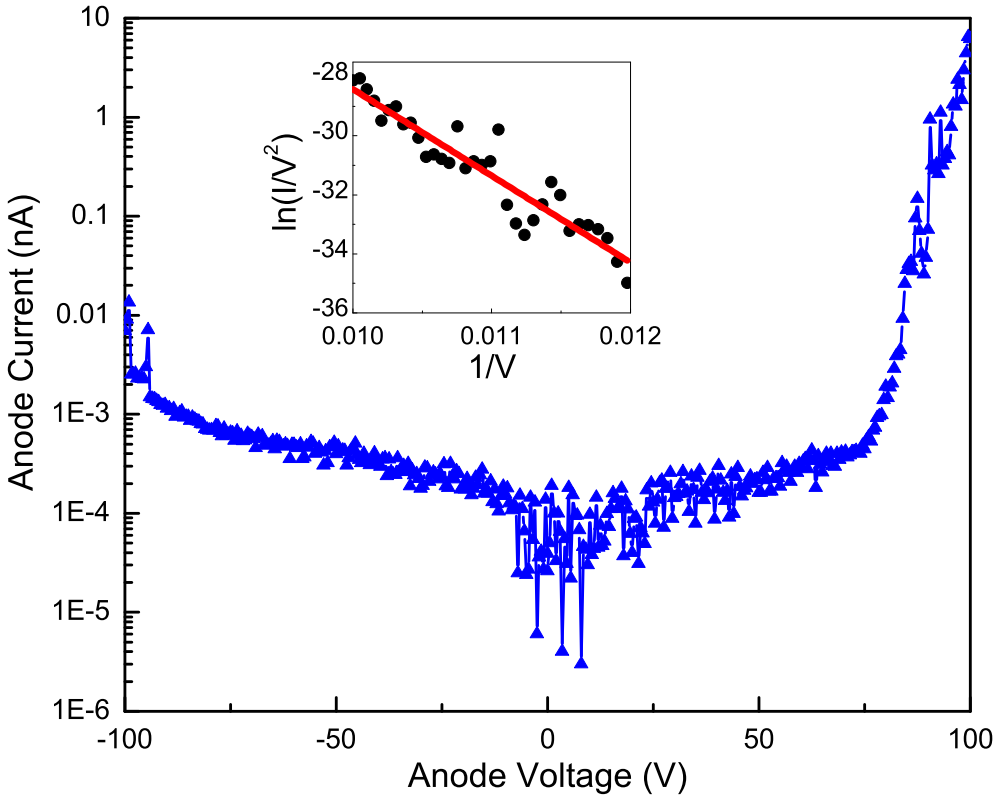


Figure 2.8: Measured I-V characteristics for a 32x32 diode array at room temperature in clean, dry air.

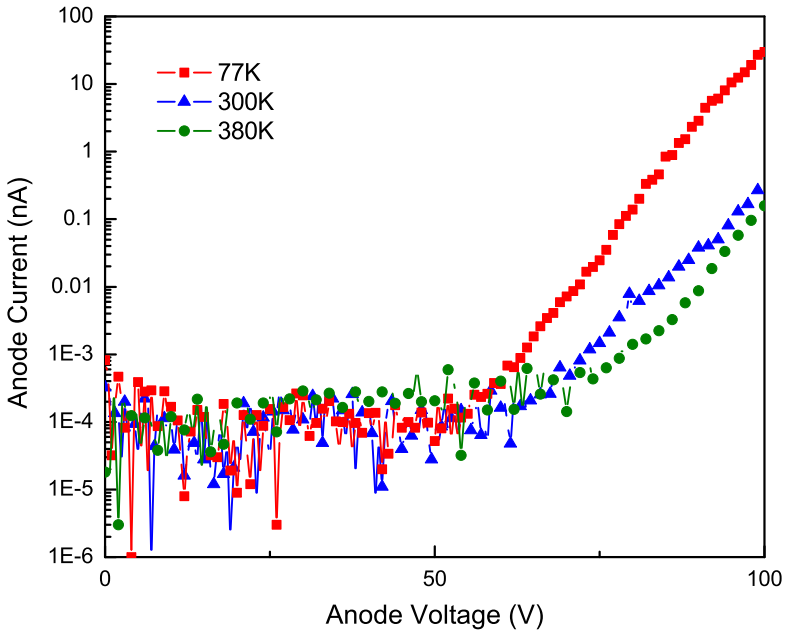


Figure 2.9: Measured I-V characteristics for a 32x32 diode array under 10^{-6} Torr vacuum at room temperature (300 K), low temperature (77 K) and high temperature (380 K).

strong component of the measured emission current. Rather, a slight negative temperature dependence is observed. The I–V profile at 77 K is cleaner and demonstrates significantly higher current for the same amount of applied voltage as compared to the measurements at 380 K and 300 K. The data in Fig. 2.9 suggest that the performance of the Ti cathodes is impacted by thermally-induced tip shape alteration, which will be discussed in more detail in Section 2.3.5.

Fig. 2.10 plots typical diode I–V characteristics in both air and 10^{-6} Torr vacuum. The similarity in the I–V profiles indicates the effectiveness of the in-situ vacuum-sealing step by demonstrating that device operation is independent of external test ambient. We expect this to be true if the cavities remain sealed under vacuum at the evaporation process pressure upon removal from the evaporation chamber in step (4) of the process sequence. Without a vacuum-sealed cavity, we would expect ionization of gas atoms and subsequent positive ion bombardment of the cathode, leading to rapid destruction of the field emitter tips, which we do not observe in our devices [7], [12], [60]. Measurements conducted as far as 1 year after device fabrication maintain the same electrical behavior. The slightly higher current level observed in air is attributed to device variation, observed on dozens of device arrays, rather

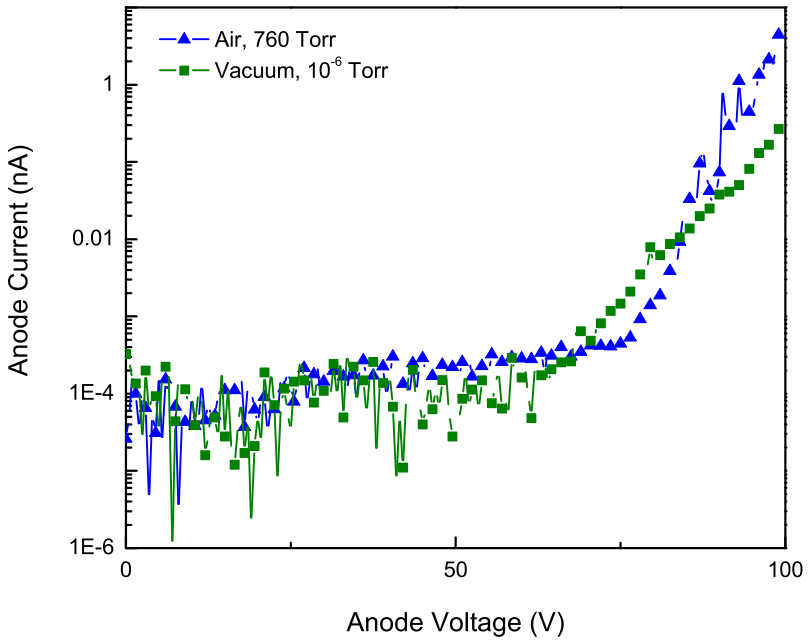


Figure 2.10: Measured I-V characteristics for a 32x32 diode array in air and 10^{-6} Torr vacuum.

than changes in the quality of the vacuum seal. It is believed that the presence of Ti helps maintain the quality of the vacuum seal, as evidenced by the Ti-based gettering solutions being developed for MEMS packaging [61]–[63]. Diode testing also reveals the necessity of alumina encapsulation to maintain vacuum-sealing. Diode devices that were cleaved to expose SiO_2 sidewalls to air resulted in worse performance and enhanced degradation, attributed to the gas permeability of SiO_2 [64]. Existing literature supports our belief that alumina is critical for maintaining the vacuum seal [65].

Table 2.1 lists the voltage required to reach the threshold current for 32x32 arrays with two aperture sizes and varying SiO_2 thicknesses. We utilize a method similar to [66] and define the threshold current as 2 pA, which indicates the onset of field emission for these arrays, as indicated by analysis of the I–V profiles. It can be seen that the threshold voltage increases with increasing SiO_2 thickness. The monotonically increasing trend follows from the relation between threshold voltage and inter-electrode distance, which is dictated by the SiO_2 thickness. As mentioned in Section 1.2.3, the field enhancement factor at the tip, β_{tip}, is related to the threshold field, E_{th}, threshold voltage, V_{th}, and anode-cathode inter-electrode distance, d, such that:

Table 2.1: Voltage to Reach Threshold Current (V)

Aperture Size	**SiO_2 Thickness**		
	507 nm	610 nm	713 nm
700 nm	50.04 ± 1.35	52.56 ± 0.83	62.33 ± 1.34
800 nm	59.23 ± 0.97	67.88 ± 1.84	78.74 ± 3.09

Measurements done on 32x32 arrays.

$$E_{th} = \frac{\beta_{tip} V_{th}}{d} \tag{2.1}$$

Re-organizing (2.1) leads to:

$$V_{th} = \frac{E_{th} d}{\beta_{tip}} \tag{2.2}$$

For a given cathode tip geometry, defined primarily by the aperture size for these devices, β and E_{th} are constant, so V_{th} is proportional to d and the two values increase monotonically, as seen in Table 2.1. It is important to also note that the two different aperture sizes result in different field enhancement factors at the tip due to changes in the tip geometry. This results in a difference in threshold voltage. The data suggest that β_{tip} is smaller for the larger aperture size. This is further supported by the low quality emission data observed from 900 nm and 1000 nm aperture size arrays, with SEM imaging showing more blunted tips and suggesting reduced field enhancement given the larger radius of curvature at the tips. However, it is important to note that larger apertures lead to taller emitters due to an increase in the amount of material deposited to seal the initial opening, which in turn affects the inter-electrode spacing.

2.3.3 Current drivability and limitations

Fig. 2.11 plots the current before breakdown in the forward regime for varying array sizes and SiO_2 thicknesses. This value, highlighted in Fig. 2.11 inset, roughly indicates the saturation current for the array and is sustained for tens of volts. Ultimately, once a peak amount of power is delivered at the tip, a destructive breakdown event occurs due to Joule heating, a known issue with Spindt-type cathodes [56], [67]. The data show that current drivability scales with array size, but is mostly independent of SiO_2 thickness. Therefore, as long as sufficient voltage can be supplied, the current is limited by the supply of electrons from the Ti tip. Normalizing the maximum current by the number of tips results in a current/tip of 70 pA, a relatively low on-state current that is attributed to the resistance of the Ti. The high operating voltages and low currents make these devices suitable for MEMS actuators, as discussed in Section 1.3.1. For applications requiring higher current density, the 40 μm pitch can be reduced significantly. Based on the data, in order to obtain a current

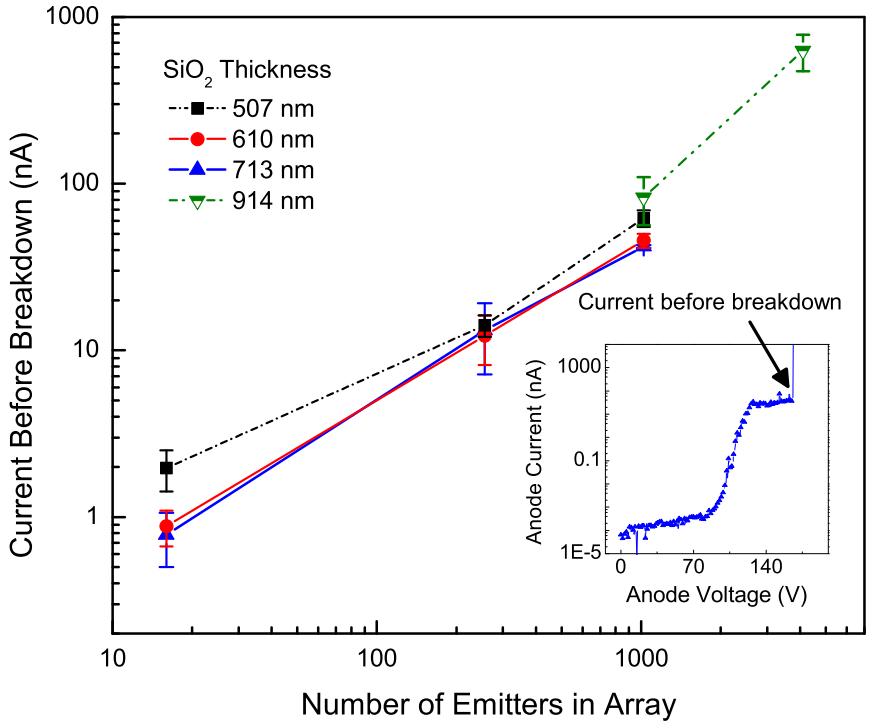


Figure 2.11: Current measured before breakdown, defined as shown in inset, for array sizes ranging from 16 to 4,096 emitters for varying SiO_2 thicknesses.

density of 2 mA/cm^2, a 120x120 array with 2 μm pitch is needed. In order for these devices to be suitable for high power applications that require high drive current and low threshold voltages, improvements in the field emitter tips are necessary. Shifting to the use of carbon nanotubes (CNTs) as field emitters will likely result in the most promising improvements, as CNTs have shown strong potential as ideal field emitters [68], [69].

Table 2.2 lists the punchthrough voltages for varying geometries, defined as the maximum forward voltage that can be sustained by the device before breakdown. We observe that punchthrough voltage increases with increasing SiO_2 thickness, but decreases with increasing array size. The data suggest that sidewall leakage contributes to overall leakage and has a more significant contribution as more emitters, and therefore cavity sidewalls, are added. This effectively reduces the observed punchthrough based on a constant current definition of punchthrough. Our measurements also indicate that the onset voltage for current saturation is roughly constant for a given aperture size and SiO_2 thickness, regardless of array size. Thus, because the punchthrough voltage decreases with increasing array size, the saturation

Table 2.2: Punchthrough Voltage (V)

Array Size	**SiO_2 Thickness**		
	507 nm	610 nm	713 nm
16	147.2 ± 4.77	176 ± 13.1	194.5 ± 5.5
256	138.7 ± 6.29	162.9 ± 2.89	177 ± 4.22
1024	128.4 ± 2.74	149.8 ± 2.54	160 ± 4.47

Measurements done on arrays with 700 nm aperture sizes.

regime decreases in range. This is attributed to the introduction of additional leakage paths as more emitters, and therefore more sidewall leakage paths, are added to the array. This suggests that while larger current can be delivered with a larger array, the subsequent effect of increased sidewall leakage must be carefully considered due to its impact on punchthrough voltage.

2.3.4 Off-state performance and trends

Another critical metric that ultimately enables the use of these devices in high power applications is the blocking voltage. Reverse characteristics are illustrated in Fig. 2.12. The plots show that off-state leakage decreases and breakdown voltage increases for increasing SiO_2 thickness. For the device arrays with 713 nm SiO_2 thickness or greater, up to 200 V blocking voltage is demonstrated (the 200 V limit comes from the maximum voltage that can be supplied by the test equipment, not due to device breakdown). It is important to note that the measured breakdown voltages are smaller than the theoretical breakdown voltage of SiO_2 for the given thicknesses, indicating that sidewall leakage paths also contribute to off-state leakage and reverse breakdown.

To investigate the effect of sidewall leakage further, Fig. 2.13 plots the leakage current at $V_a = -100$ V for varying array sizes and SiO_2 thicknesses. As shown in the plot, as the number of emitters in the array increases, the magnitude of the off-state leakage increases, with the overall magnitude of the off-state leakage decreasing for larger SiO_2 thicknesses. Therefore, similar to the effect of array size on punchthrough voltage due to the introduction of additional sidewall leakage paths, increasing the array size has an impact on off-state leakage and blocking voltage. These effects must be carefully considered when designing these devices for larger current drivability, if high blocking voltage is also required.

2.3.5 Design guidelines

The results of the electrical characterization for both the on-state and off-state performance highlight clear trends related to the design variables selected in the device design:

- Larger aperture sizes result in larger threshold voltages due to reduced field enhancement.

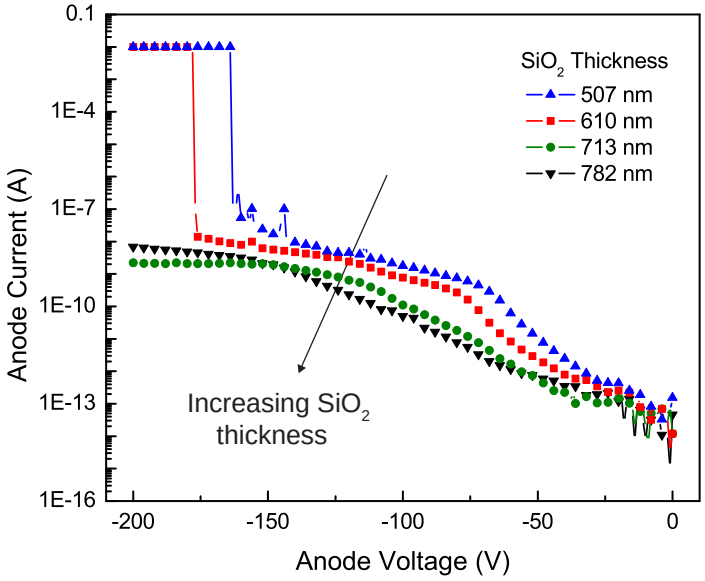


Figure 2.12: Reverse I-V characteristics for 32x32 diode arrays for varying SiO_2 thicknesses, showing off-state leakage current and reverse breakdown voltage.

- Scaling up the array size increases the drive current, but also increases sidewall leakage current.
- For the values selected, pitch has no effect on device performance; however, this may not be true as the pitch is scaled down to increase the density and the effect of closely packed cavities on device leakage must be considered.
- Increasing SiO_2 thickness has multiple effects: threshold voltage increases, punchthrough voltage increases, breakdown voltage decreases and off-state leakage decreases.

Finally, it is apparent that both Ti and alumina are materials that help maintain the quality of the vacuum seal and enable long-term ambient operation. The two main areas of improvement for future device designs are related to the cathode material and sidewall geometry.

Cathode material

The Ti tip is a clear limiting factor in the device performance, as evidenced by the fairly low maximum current/tip achievable by the Ti emitters. The low current is attributed to the high resistivity of Ti, as compared to other refractory metals such as W and Mo. Fig.

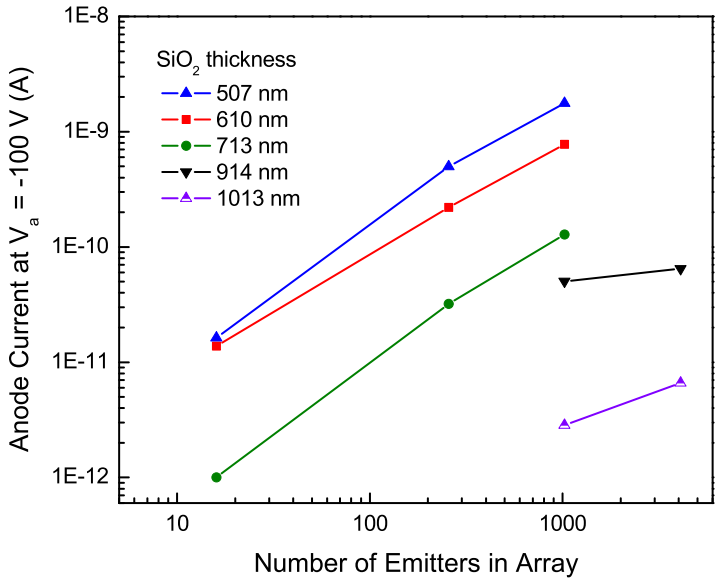


Figure 2.13: Off-state leakage current, measured at -100V anode bias, for array sizes ranging from 16 to 4,096 emitters for varying SiO_2 thicknesses.

2.14 plots the magnitude of the forward current at $V_a = 100$ V for consecutive sweeps on two different devices – one tested in clean, dry air and one tested under ideal vacuum conditions of 10^{-6} Torr. For both devices, the magnitude of the current varies from sweep to sweep, with an overall decrease as the number of sweeps increases. The trends observed here are also attributed to the high resistivity of the Ti tips, which result in Joule heating as current is drawn from the tip, according to the following relation:

$$Q = I^2 R \tag{2.3}$$

where Q is the heat produced at the tip, I is the current drawn from the tip and R is the resistance of the tip. Because resistance increases with temperature for metals and Joule heating increases the temperature at the tip, a positive feedback cycle is created between the resistance at the tip and amount of heat produced at the tip. This leads to thermal effects such as surface diffusion that alter the tip geometry, leading to tip sharpening and reduced emission areas that manifest as a reduction in current, as observed in Fig. 2.14 [67], [69]. Ultimately, Joule heating at the tip leads to an irreversible breakdown event, the result of which is shown in Fig. 2.15. For the set of devices plotted in Fig. 2.14, faster degradation is observed for the device tested in air, which has a higher current at $V_a = 100$ V. Again, this is likely due to increased Joule heating effects that are a result of the higher current

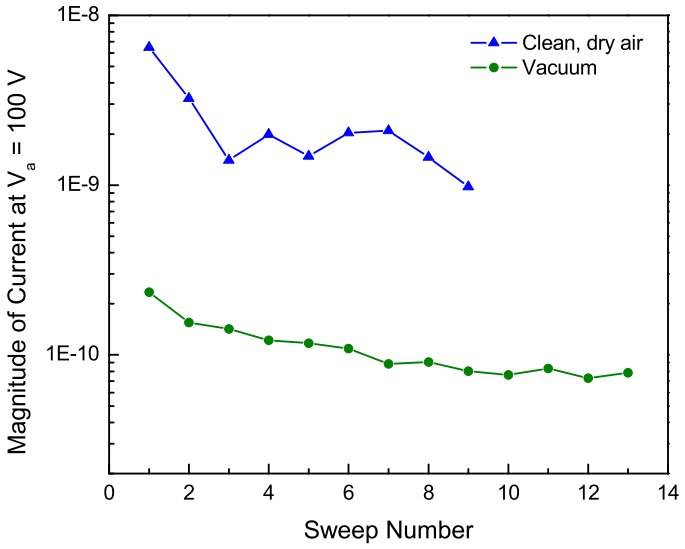


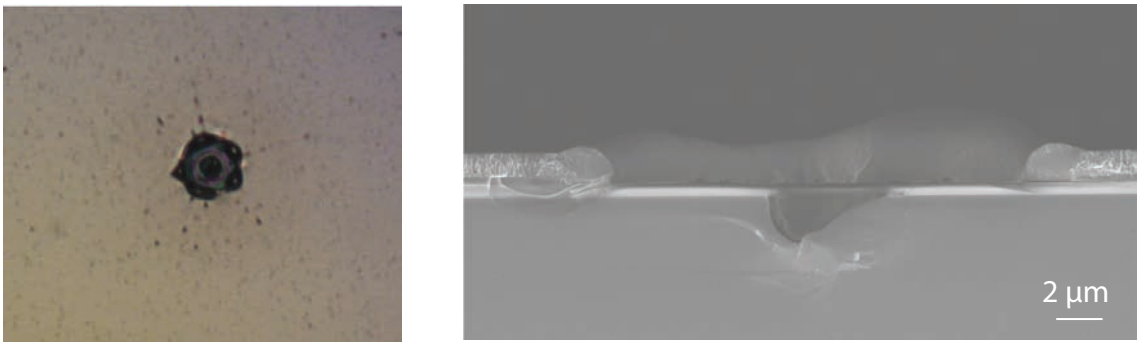
Figure 2.14: Current at $V_a = 100$ V as a function of sweep numbers, for a diode array tested in clean, dry air and at 10^{-6} Torr.

drawn from the tips. This explanation is consistent with the results from the low temperature experiments, which demonstrate higher currents at low temperatures. The thermally-induced effects responsible for current degradation are suppressed at low temperatures due to the reduced resistance of Ti at 77 K, and subsequent reduction in Joule heating, leading to improved performance and higher emission current.

The cathode performance must be improved in future generations to improve stability as well as to reduce threshold and operating voltages. Although Ti is a refractory metal, the resistivity of Ti is higher than that of other refractory metals, such as Mo and W, which should be more robust to thermal effects. However, shifting to the use of carbon nanotubes (CNTs) as field emitters will likely result in the most promising improvements. Unlike metals, the resistance of a nanotube decreases with temperature; coupled with their high mechanical strength, CNTs are significantly more resistant to Joule heating-induced tip degradation [69], [70].

Sidewall fortification

While the array size can be scaled to increase the drive current, the introduction of additional cavities and sidewall leakage paths affects both on-state and off-state performance through smaller punchthrough voltages and higher off-state leakage. Sidewall geometries with



(a) (b)

Figure 2.15: (a) Top-down view and (b) cross-sectional SEM of emitter and cavity after irreversible breakdown event.

improved electrical isolation and reduced leakage can lead to improved on/off ratios and the ability to handle larger magnitudes of voltage across the dielectric. A verified technique for improving high voltage compatibility is through the use of silicon nitride shield layers, which have been shown to result in reduced sidewall leakage and larger breakdown voltages [32], [71], [72].

2.4 Conclusions

In this chapter, vacuum-sealed fully integrated diode field emission arrays have been fabricated in a simple, scalable process integrated directly on Si. Results from electrical characterization confirm field emission and effective vacuum-sealing. Observed trends can be utilized to inform future device designs, with a primary focus on improving the cathode performance and reducing sidewall leakage. The high operating voltages and low currents make these devices suitable for MEMS applications, particularly in the design of power electronics systems for electrostatic and piezoelectric actuators, micro-robotics and micro-air vehicles. Table 2.3 lists examples of additional applications for these devices, along with specific performance needs and future work recommendations.

Table 2.3: Diode Arrays: Applications and Future Work Recommendations

System-Level Application	**Circuit Implementation**	**Performance Needs**	**Future Work Recommendations**
MEMS microrobotics, micro-air vehicles [23], [27]	Diodes in drive circuits for piezoelectric / electrostatic actuators	High operating voltage (>10V), low current (pA/nA)	High-reliability field emitters
Electric vehicle battery charging system [73]	Unidirectional AC-DC / DC-DC converters	High blocking voltage (600 V)	Increase SiO_2 thickness, sidewall fortification
High voltage power supplies	High voltage (kV) diodes	Low turn-on voltage, high current, high blocking voltage (kV)	Field emitters with low threshold field and high current, sidewall fortification

Chapter 3

Triode Field Emission Arrays: Design, Fabrication and Characterization

3.1 Introduction

In Chapter 1, the field of vacuum nanoelectronics was introduced, along with its relevance in specific applications. One area in which vacuum-based technology can contribute is in high voltage devices, given that vacuum as a conduction medium can sustain much higher voltages than semiconductor materials. However, in order to effectively utilize vacuum devices for MEMS applications, fully integrated devices that can operate in ambient conditions must be developed. In Chapter 2, a fabrication process for the development of vacuum-sealed fully integrated diode field emission arrays was presented, with results from electrical characterization. Ultimately, however, applications for diode configurations are limited due to the inability to internally modulate the output current of the device. Thus, while diodes are useful for rectifying voltages or isolating signals from a power supply, they cannot be used as switches in drive circuits. In this chapter, development and characterization of triode field emission arrays are presented, demonstrating modulation of the emission current using an additional electrode internal to the device, called the gate electrode. The implications of both output and transfer characteristics as well as low temperature measurements are discussed. This chapter concludes with a discussion on alternative applications for these devices based on the presented findings.

3.2 Background information

Fig. 3.1 is an illustration of the target geometry for the triode device. In this architecture, a third electrode, called the gate, must be integrated into the device such that it can be used to modulate the current between the cathode and anode. Thus, in the proposed structure, an integrated gate electrode is placed between the cathode and anode. By being further away, the anode electrode should have a reduced impact on electron extraction from the cathode.

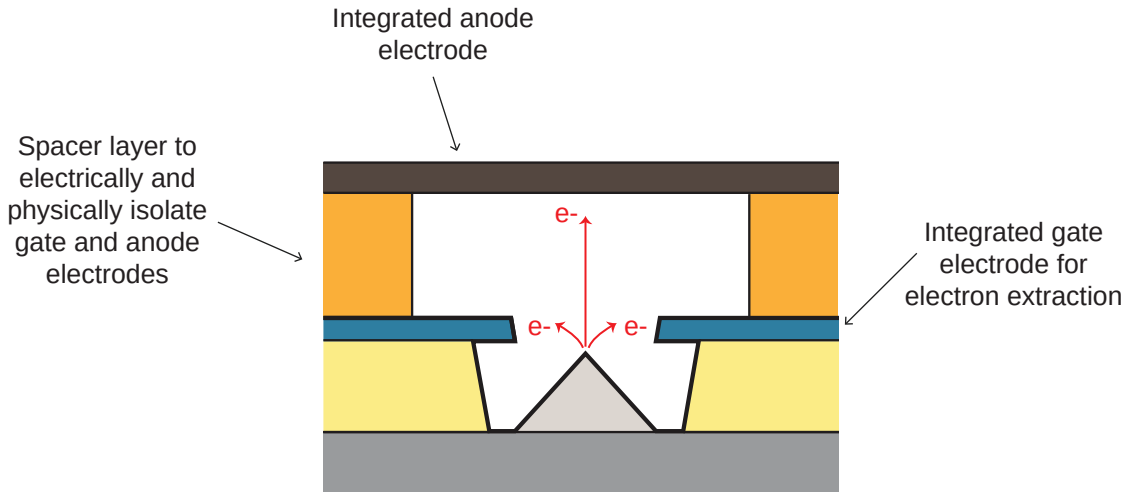


Figure 3.1: Schematic illustration of target device geometry for a fully integrated triode field emission array.

This gives the gate electrode primarily control of electron extraction, thus enabling use of the gate to control the flow of current between the cathode and anode. In order to maintain a fully integrated device, an additional spacer must be placed between the anode and newly added gate electrode for electrical and physical isolation.

3.3 Device fabrication

3.3.1 Process flow

To build the target device, a process sequence similar to that used for the diode arrays is employed to fabricate the triode arrays, with modifications to incorporate a poly-silicon gate electrode. Illustrated schematically in Fig. 3.2(a), the fabrication process for the triode arrays is:

1. Thin-film deposition: A 1 μm thick layer of SiO_2 is grown on the starting Si substrate at 1000 °C, followed by low pressure chemical vapor deposition (LPCVD) of a 200 nm thick layer of phosphorus-doped poly-silicon at 615 °C. A 350 nm thick layer of low temperature oxide (LTO) is then deposited by LPCVD at 450 °C, followed by atomic layer deposition of a 140 nm thick layer of Al_2O_3 at 300 °C.

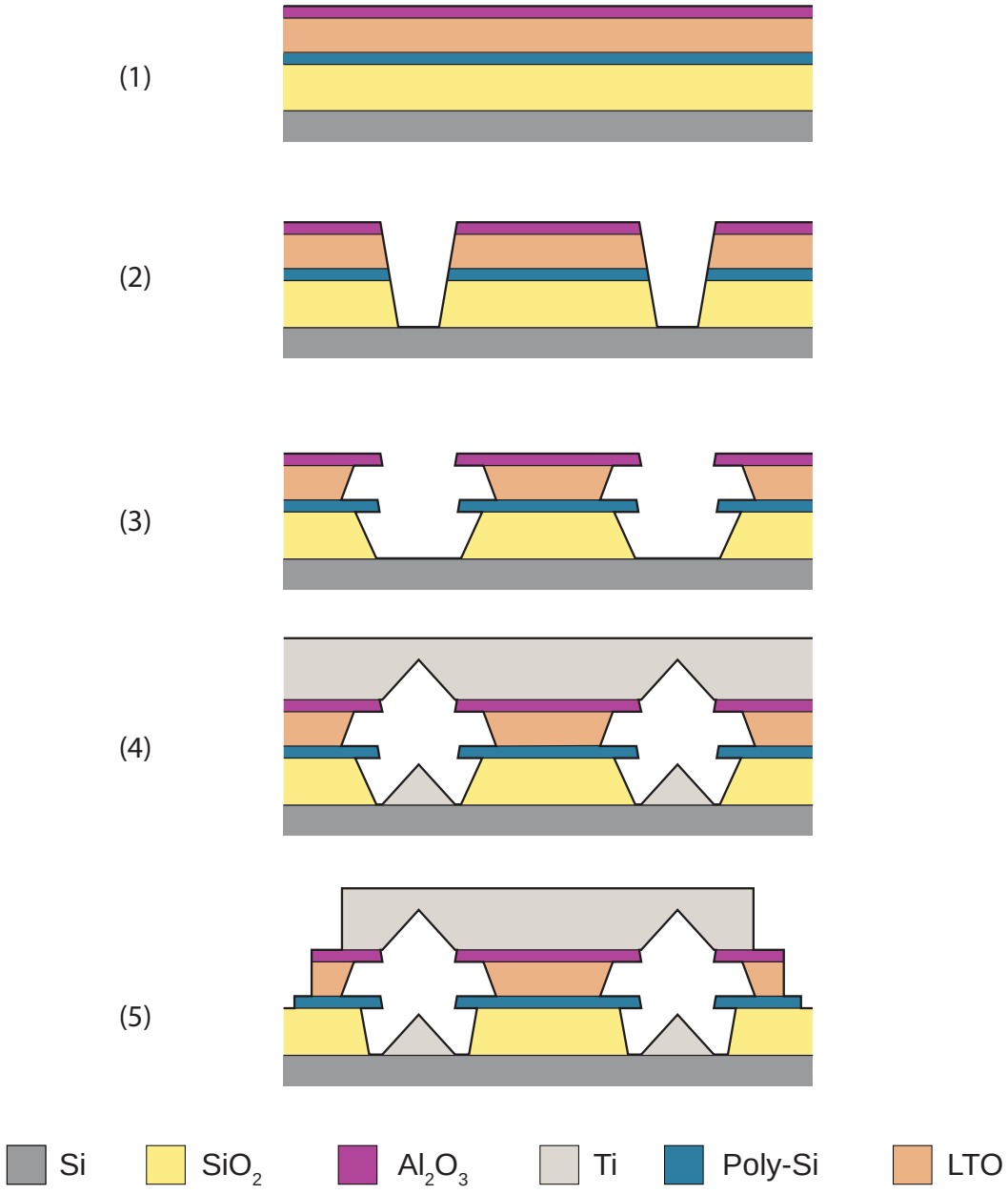


Figure 3.2: Schematic illustration of the fabrication process for the triode arrays.

2. Patterning and RIE: Circular openings are patterned using DUV lithography, and cylindrical cavities are etched into the multi-film stack using a series of RIE processes to etch the Al_2O_3, LTO, poly-silicon and SiO_2 films. As with the diode process, BCl_3/Cl_2 plasma is used to etch the Al_2O_3 film and CHF_3/CF_4 plasma is used to etch the LTO and SiO_2 films. HBr/Cl_2 plasma is used to etch the poly-silicon film.

3. Lateral etch: The SiO_2 and LTO layers are laterally etched using HF vapor. The poly-silicon layer is laterally etched using a 50 W, 100 mTorr SF6/O_2 plasma. Both lateral etches result in an alumina overhang at the top of the cavity, with the oxides being further recessed than the poly-silicon.

4. Ti e-beam evaporation: An 800 nm thick layer of Ti is deposited into the cavities by e-beam evaporation, during which the Ti emitters are formed as the cavities are sealed at the top at the evaporation process pressure of 10^{-7} Torr.

5. Device isolation: To isolate devices into arrays of 4x4, 16x16 and 32x32 emitters, multiple patterning steps are needed to electrically isolate both the top Ti layer and the poly-silicon layer. First, the top Ti layer is patterned and etched in an RIE process using BCl_3/Cl_2 plasma. To reduce external sidewall leakage, an additional patterning step is used to pattern and etch the Al_2O_3 and LTO layers such that they extend beyond the edge of the Ti layer. Finally, to isolate the poly-silicon layer, a final patterning and etching step is implemented.

The mask layout for the triode process, shown in Fig. 3.3, contains the same variables as that of the diode mask. The key difference is the addition of two masks and lithography steps to electrically isolate the Ti anode and poly-silicon gate layers.

Fig. 3.4 shows a cross-sectional SEM of an emitter in a triode geometry. The LTO film serves as electrical isolation between the Ti anode and poly-silicon gate, while the SiO_2 film isolates the poly-silicon gate and substrate, which serves as the cathode contact. The film thicknesses are chosen such that emitter tip sits below the poly-silicon gate layer in order for a bias applied to the gate to influence the electric field above the emitter and subsequent electrical performance.

3.3.2 Process characterization

In addition to the findings from diode process characterization, discussed in Section 2.2.2, the following process steps are critical in the fabrication of the triode arrays:

1. Lateral etch time: As with the diode arrays, an insufficient lateral etch of the oxide results in Ti deposition along the cavity sidewalls, preventing proper formation of the emitters and shorting the cathode and anode. However, for the triode process, the poly-silicon lateral etch must also be long enough such that the poly-silicon layer is also recessed with the respect to the alumina layer. An insufficient poly-silicon lateral

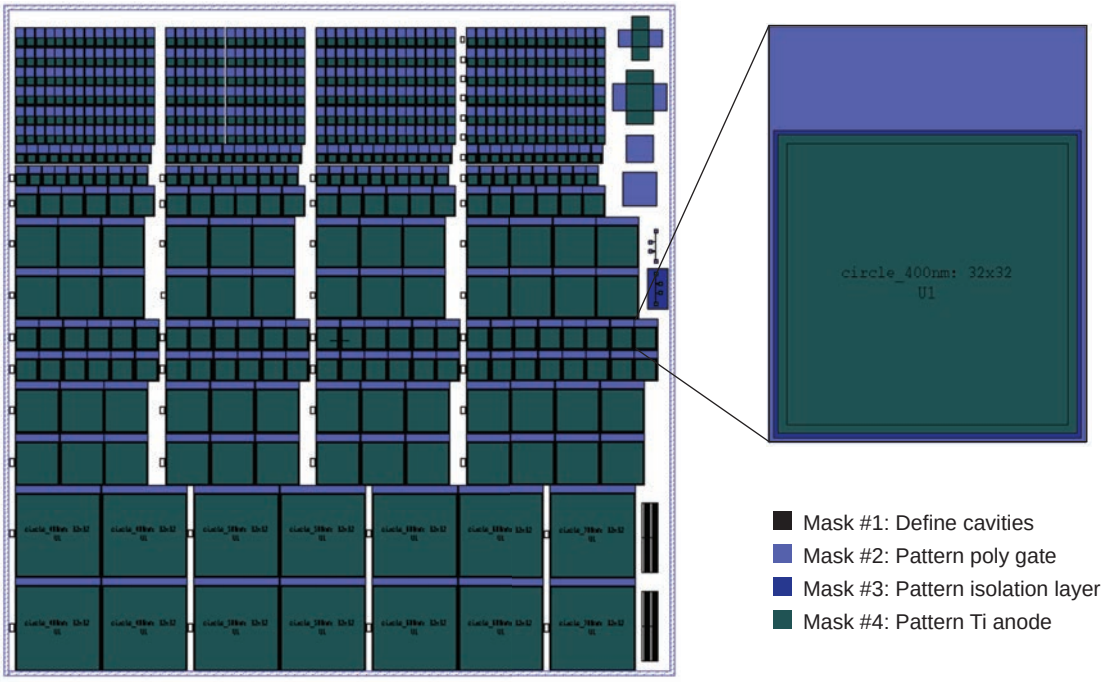


Figure 3.3: Mask layout for triode lithography steps.

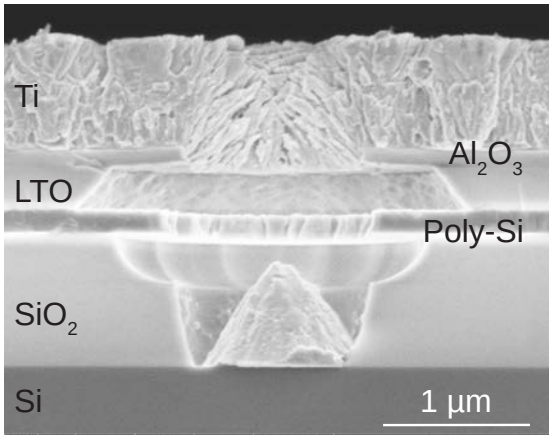
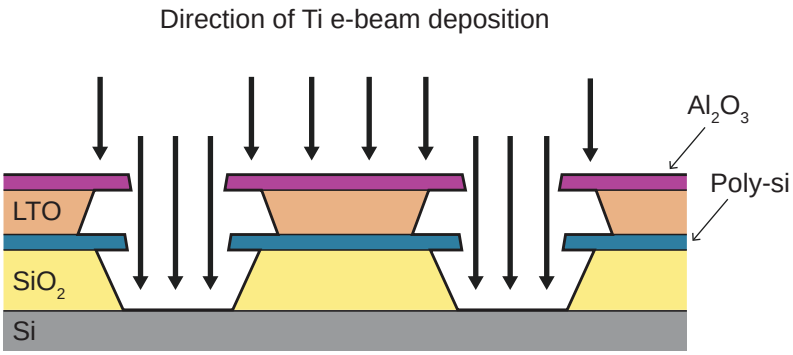
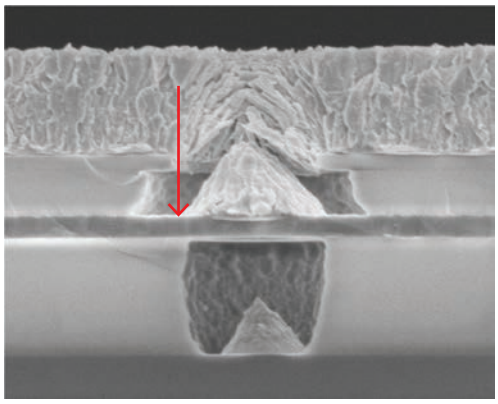


Figure 3.4: Cross-sectional SEM of a single emitter tip in a triode configuration.



(a)



(b)

Figure 3.5: (a) Schematic illustration of Ti deposition direction with respect to substrate. (b) Cross-sectional SEM of triode with insufficient poly-silicon lateral etch, resulting in the poly-silicon layer extending further inward than the alumina layer. The direction of Ti deposition for this geometry is indicated by the red arrow, showing that Ti is deposited on the poly-silicon layer.

etch results in deposition on the gate that alters the gate geometry entirely, as seen in Fig. 3.5.

2. Native oxide removal prior to poly-silicon lateral etch: A short, HF vapor etch is utilized prior to the poly-silicon lateral etch. This pre-etch step removes the native oxide layer on the poly-silicon that can interfere with the poly-silicon etch, which is not designed to remove oxides. By removing this layer just before the poly-silicon etch, we are able to maintain consistent control of the poly-silicon etch rate.

3.3.3 Key features of final geometry

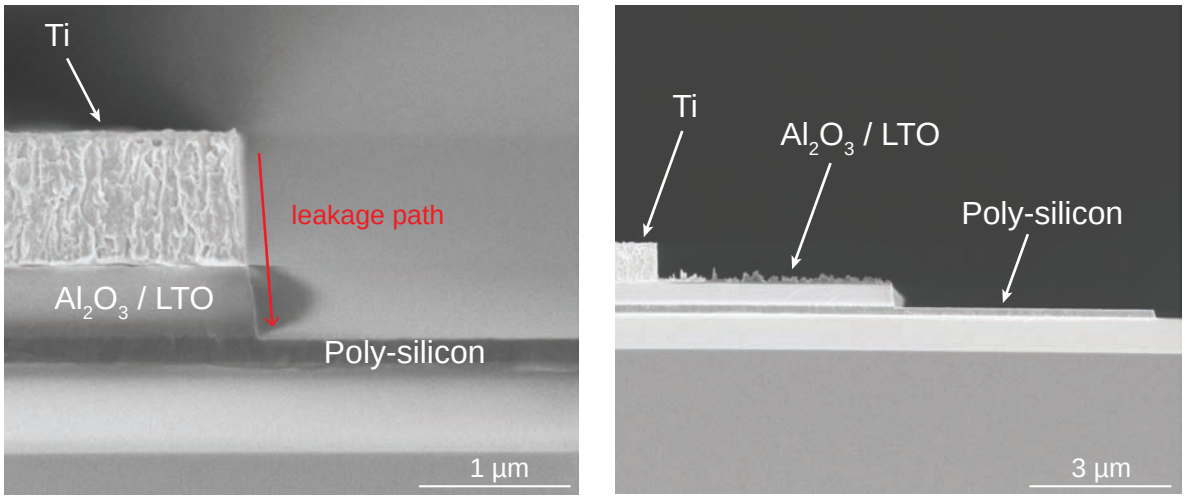
In addition to the key considerations for the diode device geometry, two additional features of the triode geometry are critical. First, the position of the poly-silicon gate in the triode configuration must be carefully controlled. The poly-silicon layer must be recessed far enough as per the discussion above on lateral etch time; however, recessing the poly-silicon layer too far will reduce gate control of the device. We explored several poly-silicon etch chemistries, most of which resulted in very fast etches (microns/minute). Ultimately, we found that a low-power (50 W), high-pressure (100 mTorr) $SF6/O_2$ plasma gave us the finest control over the etch, at a rate of 1 nm/sec. The height of the gate layer with respect to the emitter tip must be carefully controlled as well, since the poly-silicon gate must sit above the emitter tip in order to influence field emission from the tip. Thus, the SiO_2 thickness must be chosen such that the top of the emitter is vertically positioned below the poly-silicon gate.

Also critical is careful control of the electrical isolation external to the device. The final series of patterning and RIE steps are necessary for enabling electrical contact to the anode and gate electrodes for different device arrays located on the same wafer. However, careful isolation is required between the Ti anode and poly-silicon gate external to the device. Initial triode testing revealed that the geometry shown in Fig. 3.6(a), in which one mask was used to etch both the Ti, Al_2O_3, and LTO layers, created a sidewall leakage path that ultimately caused shorting between the anode and gate electrodes. Fig. 3.6(b) is an SEM cross-section of the final device geometry, in which the Al_2O_3 and LTO layers extend beyond the Ti anode to create additional physical separation between the Ti anode and poly-silicon gate layers.

3.4 Results and discussion

3.4.1 Experimental setup

The triode arrays characterized in this work are biased per the configuration shown in Fig. 3.7, with both the gate and anode electrodes positively biased with respect to the grounded cathode. In this configuration, electrons are emitted from the cathode towards both the gate and anode electrodes, with the gate intended to enhance electron extraction from the emitters. This is distinct from a traditional thermionic vacuum tube, in which the gate is



(a) (b)

Figure 3.6: Cross-sectional SEM of edge of device array showing (a) insufficient and (b) sufficient electrical isolation between the Ti anode and poly-silicon gate.

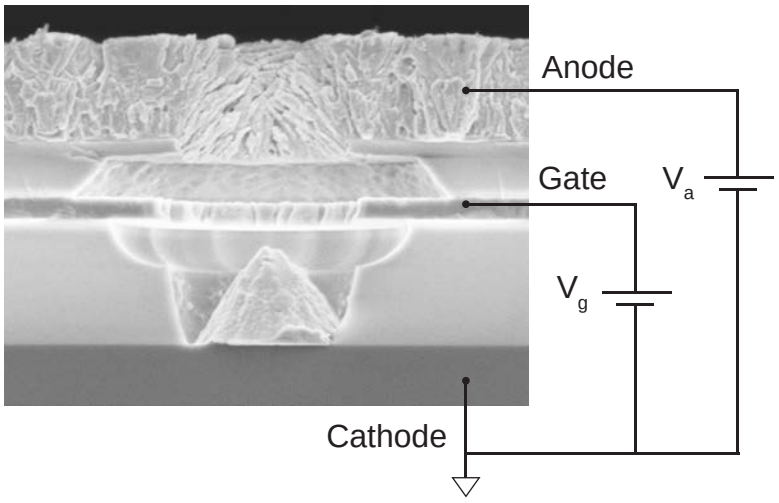


Figure 3.7: Test configuration for triode arrays, with grounded cathode and positive biases applied to gate and anode electrodes.

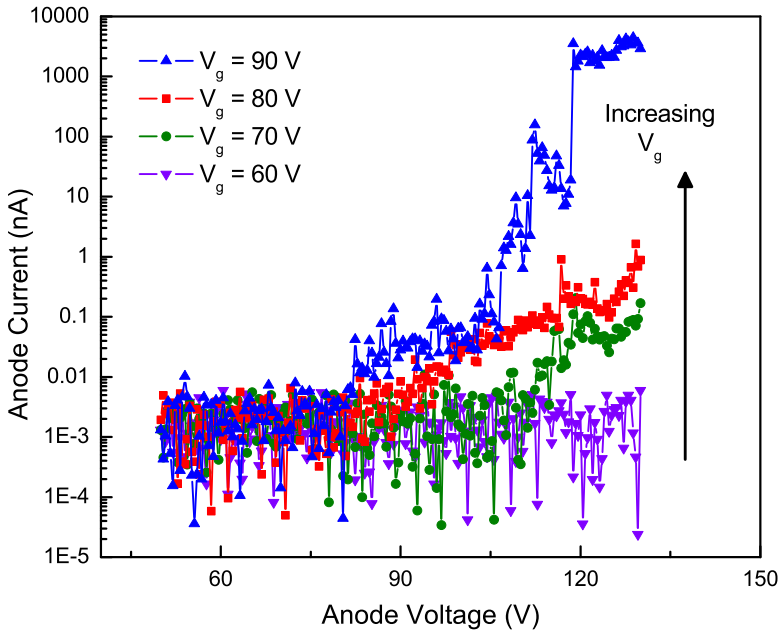


Figure 3.8: Output characteristics for a 32x32 triode array, with corresponding ratio of anode current (I_a) to gate current (I_g).

negatively biased to prevent thermionically emitted electrons from reaching the positively biased anode plate. As with the diode arrays, the starting substrate is grounded and serves as the cathode contact, as it is electrically connected to the Ti emitter. The top Ti layer is positively biased and serves as the anode, and the poly-silicon layer is positively biased and serves as the gate. All I–V measurements are carried out using a Keysight B1500A semiconductor device parameter analyzer. Because triode arrays are not fully encapsulated by alumina in order to electrically isolate device arrays (in other words, the alumina layer is fully etched in some regions to access the poly-silicon layer), the triode arrays are characterized in 10^{-5} Torr vacuum. By doing so, we can suppress external leakage and maintain the same level of vacuum as is present during device fabrication, enabling us to measure intrinsic device behavior.

3.4.2 Output characteristics

Output characteristics for a 32x32 triode array with 800 nm aperture size are shown in Fig. 3.8. At V_g = 60 V, no output current is measured. When V_g is increased to 70 V,

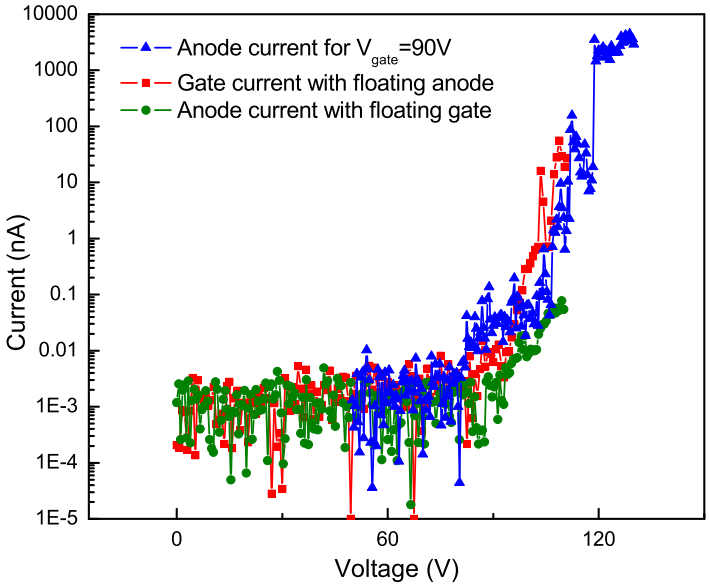


Figure 3.9: Measurements showing triode performance with and without bias applied to the gate.

we begin to measure field emission current at the anode. As the gate voltage is increased up to 90 V, the anode current continues to increase. Three-terminal operation of the device thereby demonstrates the modulating effect of the gate voltage on output current.

Output current can also be measured while operating the device in a two-terminal mode, where only the anode and cathode are biased. However, this results in 10-100x smaller output current, as shown in Fig. 3.9. Two-terminal operation also precludes output current modulation. In this mode, field emission from the cathode is solely dictated by the anode voltage since the potential at the floating gate is determined by the capacitive divider formed by the device geometry. For example, 120 V applied at the anode will cause the gate potential to float around 90 V and effectively turn on the device. By applying 60 V at the gate terminal, we are able to keep the device in an off state. Therefore, these plots demonstrate that the gate not only enhances electron extraction, but also provides modulating capability and the ability to turn the device on and off in a controllable manner.

Fig. 3.10 plots the DC gate to anode current, β_{dc}, which is the ratio of anode current, I_{a}, to gate current, I_{g}, using median filtering to remove noise in the data. As can be seen from the plot, a β_{dc} factor of several hundred can be achieved. Thus, a very small input current can control a much larger output current, making this a useful amplifying device for applications in which high current gain is needed. We also observe that the maximum

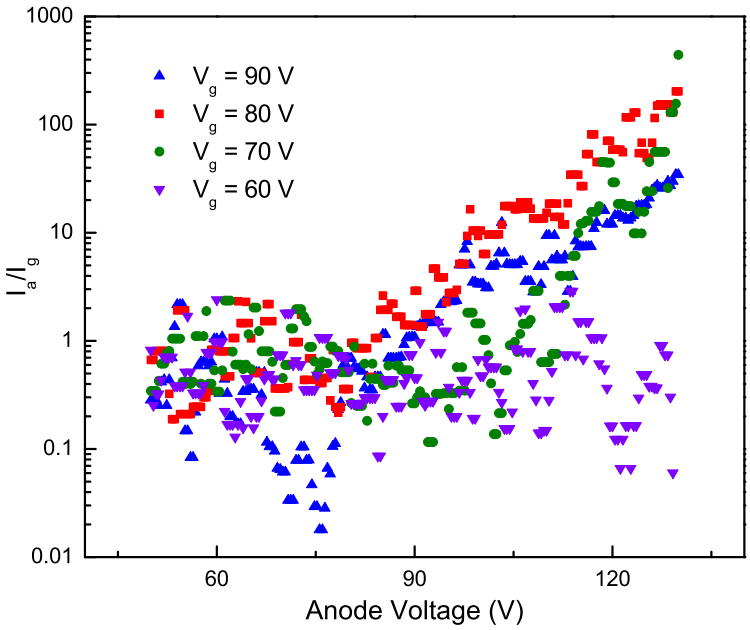


Figure 3.10: Output characteristics for a 32x32 triode array, with corresponding ratio of anode current (I_a) to gate current (I_g).

ratio of I_a to I_g occurs at $V_g = 80$ V. At this gate voltage, a minimum amount of current is intercepted by the gate, which is desirable for applications requiring large output current gain. However, the total current and power delivered at the anode is maximized at $V_g = 90$ V, which is desirable for applications that require high power amplification [74]. Therefore, the optimal gate and anode voltage that should be applied is dependent on the desired output characteristics and application.

3.4.3 Transfer characteristics

Fig. 3.11 plots the transfer characteristics for the triode array. As expected from the exponential nature of Fowler-Nordheim tunneling, both the gate and anode current increase exponentially as gate voltage increases, since field emitted electrons are transferred from the cathode to both the gate and anode electrodes, as illustrated in the schematics in Fig. 3.11. In Fig. 3.11(a), more cathode current is delivered at the gate compared to the anode. In Fig. 3.11(b), roughly equal amounts of cathode current are delivered to the gate and anode. In Fig. 3.11(c), when the anode voltage is increased to 120 V, a larger fraction of the cathode

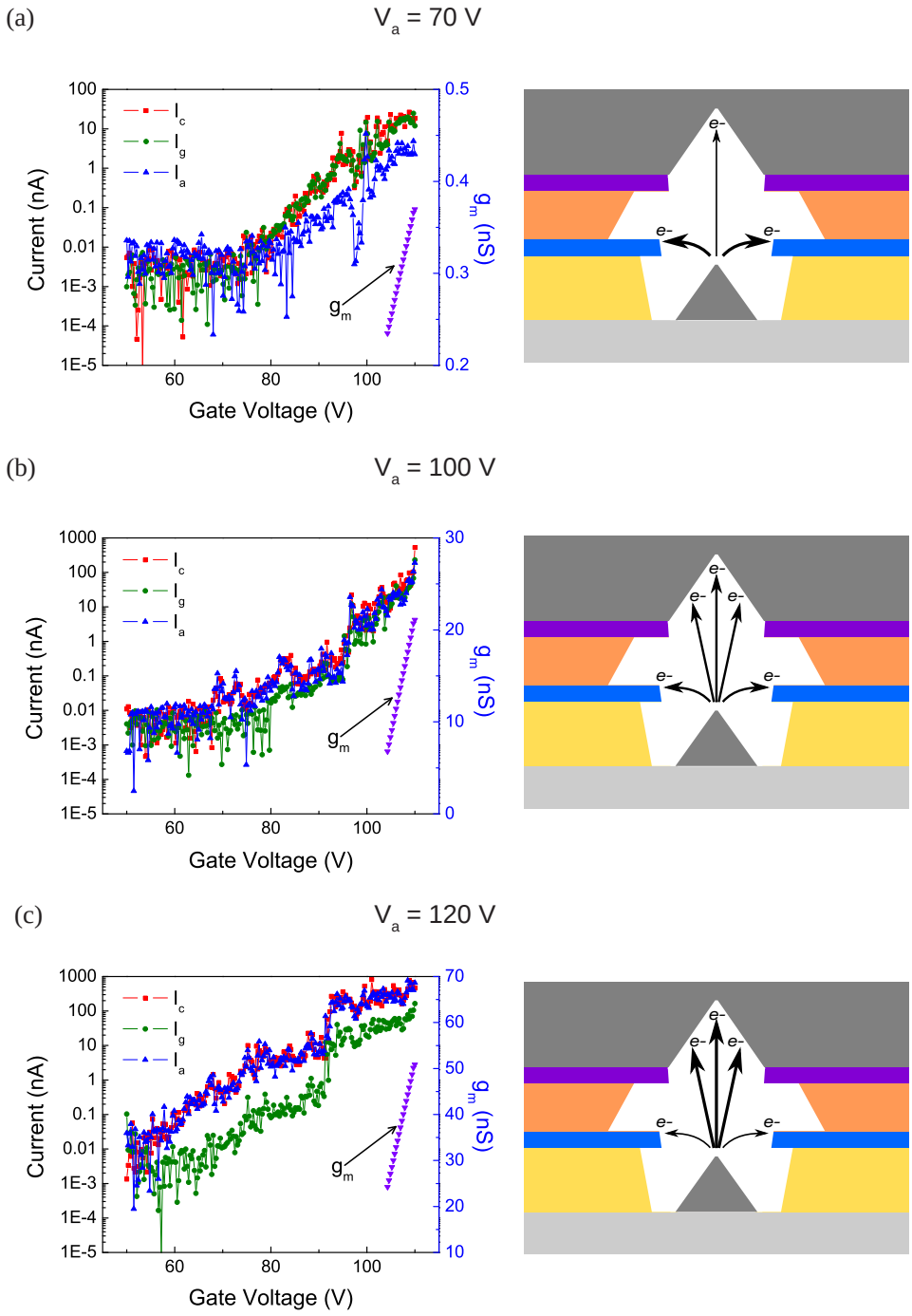


Figure 3.11: Transfer characteristics for a 32x32 triode array for anode held at (a) 70V, (b) 100V, and (c) 120V. Plots on left indicate total current measured at the three terminals and transconductance values. Schematics on right indicate path of electrons field emitting from cathode tip, with thicker arrows representing a larger fraction of electrons.

Table 3.1: Summary of Transfer Characteristics

Anode Voltage (V)	**I_a/I_g (median)**	**Max Cathode Current (nA)**	**g_m range (nS)**
70	0.35	26	0.23 – 0.37
100	2.22	103	6.79 – 21.10
120	18.04	765	24.24 – 50.87

current is now seen at the anode compared to the gate. These plots demonstrate that the anode voltage influences the trajectory of electrons emitted from the cathode. This results in an increase in the ratio of anode to cathode current and a decrease in the ratio of gate to cathode current as the anode voltage increases. These results are displayed in Table 3.1, which contains the median value of the I_a/I_g ratio for the three transfer curves in Fig. 3.11 and demonstrates that the ratio increases with increasing anode voltage. Moreover, the anode voltage also influences electron extraction from the tips. Ultimately, an increase in the anode voltage causes an increase in the magnitude of field emission from the cathode tips. Table 3.1 also lists the values for the total cathode current, which increases from from 15 nA to nearly 1 µA for the higher anode voltage, due to enhanced electron extraction from the tips.

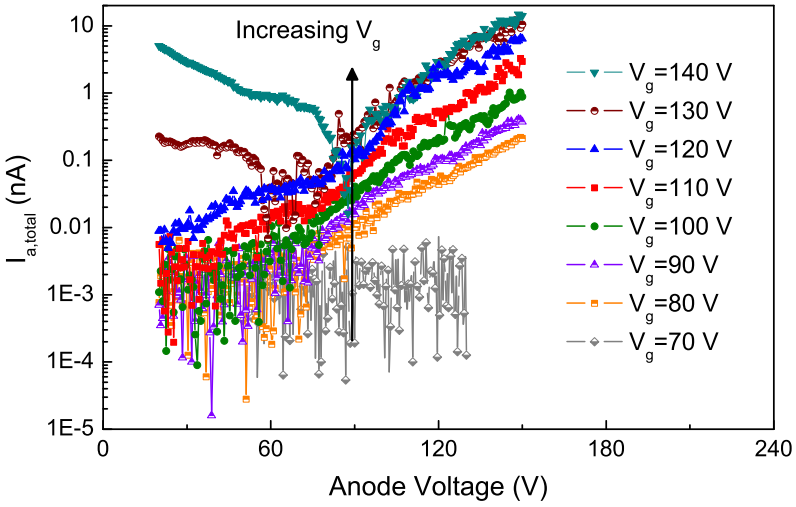
Fig. 3.11 also plots the transconductance, $g_m = \partial I_a/\partial V_g$, for the three transfer curves, indicating how quickly the output current increases with gate voltage. Because these are tunneling devices, we expect I_a to approximately increase exponentially with V_g, resulting in the linear profile for the transconductance. We also observe an increase in g_m for higher anode voltages.

3.4.4 Low temperature measurements

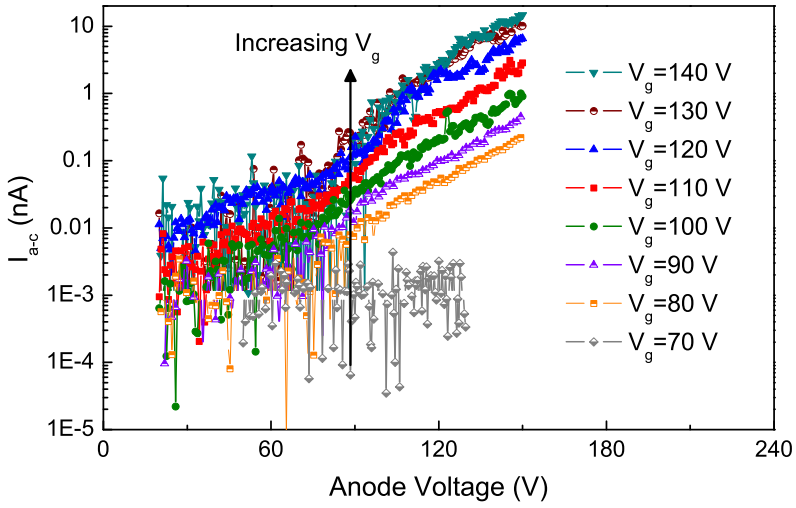
Fig. 3.12(a) shows measurements performed on triode arrays at 77 K. Higher currents and cleaner I–V characteristics, as compared to measurements taken at 300 K, are in agreement with the trends observed for the diode arrays and further validate that the performance of the Ti tip is limited by thermal effects that are suppressed at low temperatures.

The low temperature triode measurements also indicate the need for improved isolation between the anode and gate. As can be seen from Fig. 3.12(a), significant anode current is measured even at very low anode voltages (less than 60 V) when the gate voltage is greater than 120 V. By noting that the total current at each terminal consists of both field emission (FE) and sidewall leakage (SL) contributions between electrodes, the magnitude of the field emission contribution of the total current at the anode can be determined. First, the total current at each terminal is represented as follows:

$$I_{g,total} = I_{g-c,FE+SL} + I_{a-g,SL} \tag{3.1}$$



(a)



(b)

Figure 3.12: (a) Output characteristics for a 32x32 triode array under 10^{-6} Torr vacuum at 77 K, plotted as a function of total anode current versus applied anode voltage and re-plotted in (b) as a function of total anode-cathode current (indicating anode current solely due to field emission from cathode) versus applied anode voltage.

$$I_{a,total} = I_{a-g,SL} + I_{a-c,FE} \tag{3.2}$$

$$I_{c,total} = I_{g-c,FE+SL} + I_{a-c,FE} \tag{3.3}$$

where $I_{\text{g-c,FE+SL}}$ is the gate-cathode current due to field emission and sidewall leakage, $I_{\text{a-g,SL}}$ is the anode-gate current due to sidewall leakage, and $I_{\text{a-c,FE}}$ is the anode-cathode current due to field emission. By re-organizing the equations above, we can determine the magnitude of the field emission current between the anode and cathode:

$$I_{a-c,FE} = \frac{I_{a,total} + I_{c,total} + I_{g,total}}{2} \tag{3.4}$$

Fig. 3.12(b) plots the total anode-cathode current due to field emission and verifies that the high current at low voltage in Fig. 3.12(a) is caused by leakage between the anode and gate electrodes. Separation of current contributions is only necessary for the low temperature measurements at high gate voltages due to the higher voltage and current applied to the devices. Applying the same methodology to the room temperature measurements results in negligible contributions of anode-gate sidewall leakage to the anode-cathode current. The plots in Fig. 3.12 indicate that the electrical isolation between the anode and gate terminals must be fortified when running at high voltages and high currents for high power applications. A verified technique for improving high voltage compatibility is through the use of silicon nitride shield layers, which have been shown to result in reduced sidewall leakage and larger breakdown voltages [32], [71], [72]. Overall, the data from low temperature measurements indicate that performance can be substantially improved by addressing thermally-induced effects and modifying the geometry of the multi-film stack to improve electrode isolation and minimize sidewall leakage.

3.4.5 Design guidelines

Results from electrical characterization of the triodes indicate that the anode voltage affects the behavior of the device by influencing the electron trajectory and enhancing electron extraction from the cathode tip. The observed effects are analogous to short-channel effects such as drain-induced barrier lowering (DIBL) and channel length modulation (CLM) in MOSFET devices. An increase in anode bias results in field emission occurring at a reduced gate voltage, as observed in the output characteristics of Fig. 3.8 and analogous to DIBL, and an increase in the anode current, as observed in the transfer characteristics of Fig. 3.11 and analogous to CLM. This suggests that integrated triode structures with closely spaced electrodes are similar to short-channel MOSFETs, while non-integrated geometries, where the anode is typically hundreds of micrometers away from the gate and cathode, are analogous to long-channel MOSFETs [75], [76]. The differences in inter-electrode spacing ultimately affect the magnitude of the measured operating voltages. Non-integrated geometries with large gaps (millimeters) show differences of hundreds of volts between the gate

and anode, but for non-integrated geometries with smaller gaps (micrometers), the voltages become comparable again [17], [18]. In this work, the triode arrays operate at comparable gate and anode voltages. Therefore, the interplay between the anode and gate voltage and its effects on output current and dependence on inter-electrode spacing must be considered for future device designs.

Additionally, as with the diode arrays, low temperature measurements highlight the limitations of metal emitters as field emission cathodes. The data also indicate the need for sidewalls with reduced leakage, either by implementing new materials such as silicon nitride, or implementing new geometries, such as corrugated sidewalls.

3.5 Conclusions

In this chapter, the results of triode array characterization are presented and discussed. Notably, the triode arrays demonstrate gate-modulated field emission. Based on the results presented in this chapter, it is crucial that future designs take "short-channel" effects into consideration for integrated field emission geometries. With modifications to the physical device geometry and use of higher performance cathode materials, we expect these devices to achieve much higher blocking voltages and excellent on-state performance, enabling the use of these devices for high power applications.

Beyond high voltage and high power applications, the results of this report also indicate further opportunities to leverage the technical features of vacuum-based nanoelectronics for other applications, some of which are listed in Table 3.2. Features unique to vacuum devices, such as radiation-hardness and reduced temperature sensitivity, present an opportunity to build robust devices for harsh environments. Space exploration, for examples, requires the development of electronics for cold temperature and radiation-rich environments [77], [78]. While existing electronics can be protected by packaging, the need for additional payloads to the system can be eliminated by utilizing devices that can withstand extreme conditions. The low temperature measurements conducted here are encouraging and suggest the potential for using these devices in cold environments. On the other extreme are high-temperature environments encountered during oil and gas exploration, where there is a critical need for detecting rock formations during downhole sensing in order to improve drilling efficiency and prevent catastrophic events [79], [80]. By utilizing a cathode material with improved temperature resistance, such as CNTs, sensing systems based on vacuum nanoelectronics for in-situ detection of rock formations can be developed. As can be seen from the table, many of the applications require high-performance field emitters, with features ranging from low turn-on voltages to robustness at extreme temperatures, which can be met with CNT-based systems.

Table 3.2: Triode Arrays: Applications and Future Work Recommendations

System-Level Application	**Circuit Implementation**	**Performance Needs**	**Future Work Recommendations**
MEMS microrobotics, micro-air vehicles [23], [27]	Switches in drive circuits for piezoelectric / electrostatic actuators	High operating voltage (>10V), low current (pA/nA)	High-reliability field emitters
Electric vehicle battery charging system [73]	Converters: AC-DC / DC-DC, boost / buck	High blocking voltage (600 V)	Increase SiO_2 thickness, sidewall fortification
High voltage power supplies	High voltage (kV) switches	Low turn-on voltage, high current, high blocking voltage (kV)	High current field emitters, sidewall fortification
Motor controllers, sensor amplifiers	High load current power amplifier	High DC current gain	High-reliability field emitters
Oil & gas downhole drilling, aviation / automotive combustion chambers [80]	Switches for wireless sensors (i.e. digital inverter, op-amp)	Low turn-on voltage, robustness at high temperatures (600°C)	Thermally robust field emitters with low threshold field
Nuclear operating cores	Switches for wireless sensors	Low turn-on voltage, high radiation hardness (krad)	Field emitters with low threshold field
Satellites, space environments [78]	Switches for wireless sensors	Low turn-on voltage, high radiation hardness (krad), low temperature operation (<280K)	Thermally robust field emitters with low threshold field

Chapter 4

Portable Electron Sources: Design, Fabrication and Characterization

The previous chapters demonstrate that vacuum microelectronic devices can be designed to meet the strict demands of specific applications, such as high voltage switching. For these applications, the superior technical features of electron transport in vacuum offer significant benefits. However, applications of field emission devices are not limited solely to those in which solid-state devices have begun to hit limitations. Among the most critical technologies enabled by field emission devices are applications utilizing electron sources. Field emission-based electron sources have enabled the development of numerous commercial applications, such as electron microscopy and nanolithography [42], [69]. However, because field emitters operate best in high vacuum environments, many of these applications require bulky, power-hungry, high vacuum equipment. In order to use field emission-based electron sources for a wider range of applications, portable electron sources must be developed. Therefore, the motivation of the next two chapters is to develop a portable electron source that demonstrates operation in air and ambient conditions.

This chapter begins with a brief discussion of the key considerations in designing a truly portable electron source. This is followed by a survey of the literature on the unique properties of a novel two-dimensional material, graphene, that make it an ideal material to be used in such a design. Then, a novel method for integrating graphene with Spindt-type emitters is outlined, along with the results of process characterization. This establishes a method for integrating graphene as an electron transparent gate and vacuum seal for a field emission array, with the goal of implementing the device as a portable electron source.

4.1 Design considerations

The development of a truly portable electron source imposes a unique set of design constraints: low-power and low-voltage operation, fully integrated electrodes and vacuum-sealed cavities for the emitters without confining the field emitted electrons. The target

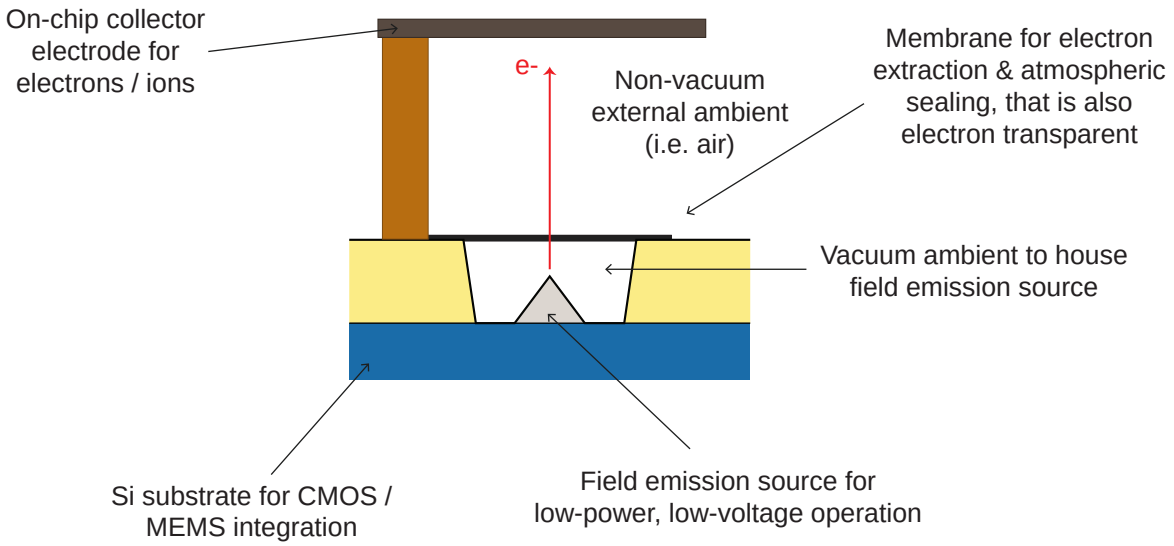


Figure 4.1: Schematic illustration of the target device architecture, with key features annotated.

device architecture is drawn in Fig. 4.1. The use of field emitters and nanomaterials enables these constraints to be met.

4.1.1 Role of field emission devices

Field emission devices can be readily miniaturized for low-power and low-voltage applications, making field emitters ideal in the development of portable electron sources. Indeed, there have been significant efforts and successes in developing MEMS-compatible field emission-based electron sources for a number of applications, including space charge neutralizers [21], electron-impact ion sources [36], micro-ionizers for mass spectrometry [37], and x-ray sources [20], [38].

4.1.2 Role of graphene

Miniaturization of electron sources has been limited by the performance of the field emission source in non-vacuum environments. Because field emitters degrade rapidly when exposed to other ambients and gases, their usefulness outside of high vacuum conditions is extremely limited. The ability to maintain a high vacuum environment for the field emission source while utilizing the field emitted electrons in non-vacuum environments would unlock the use of field emission-based electron sources for a plethora of commercial applications outside of a lab environment. This would enable the use of electron sources in applications

ranging from portable mass spectrometry for a wide range of gases [46] to ion thrusters for microrobotics requiring fully integrated systems [47].

Potential solutions preclude methods like metal sealing, which are effective for maintaining vacuum-sealed cavities, but confine the field emitted electrons to the cavity. A different approach is to use electron-transparent and gas-impermeable materials that are designed to maintain vacuum-sealing while still enabling the transmission of electrons. In 2005, Haase, et. al, conducted a study on a number of materials, such as alumina and silicon nitride, to serve this purpose; however, these materials require electron energies on the order of keV, making these systems infeasible for on-chip, low-voltage applications [44]. In recent years, however, graphene - an allotrope of carbon that comes in the form of single atom thick monolayers - has emerged as a material exhibiting a number of properties that make it attractive in the development of portable electron sources.

Gas impermeability of graphene

Despite being only one atom thick, graphene is impermeable to gases and can withstand pressure differences as high as 6 atm [45], [81]. In one of the seminal studies on the impermeability of graphene sheets in 2008, Bunch, et. al, tested the permeance of several gases through a silica microchamber sealed with a graphene sheet. The microchamber was kept under vacuum (0.1 Pa) for several days and then exposed to different gases at atmospheric pressure. AFM measurements showed that the graphene sheet depresses and stretches, with the microchamber eventually equilibrating to the pressure of the external ambient at a leak rate indicative of diffusion through the silica microchamber. The gas impermeability of graphene can be attributed to its π-orbitals, which form a dense and delocalized cloud that blocks the gap within its aromatic rings, preventing even molecules as small as helium and hydrogen from passing through, even at extremely high pressure differences [45]. The high breaking strength (42 N/m) and Young's modulus (1 TPa) of graphene enable it to withstand such large pressure differences (cite Bunch references). The ability to separate vacuum from atmosphere makes graphene an ideal candidate for sealing field emitters under vacuum while utilizing the electron source in non-vacuum environments.

Electron transparency of graphene

A number of studies have been conducted over the last few years investigating the use of graphene as a gate electrode in vacuum triode devices, due to its high electron transparency. In 2014, Li, et. al, studied the transmission of high-energy ($\sim$1 keV) electrons emitted from a nanocarbon field emission source through a graphene/Mo hybrid gate electrode and found the effective transmission efficiency to be around 97%. Moreover, there was a significant improvement in beam focusing and amplification, as compared to conventional metal gate electrodes [82]. These findings were extended with studies on the transparency of graphene for low energy electrons [83]. Thus, graphene can be used to seal a device, while still allowing transmission of electrons to an environment outside the sealed cavity.

Applications of graphene membranes

The unique properties discussed above have been leveraged for applications previously unachievable with existing material systems. Graphene membranes have been used to demonstrate atmospheric operation SEMs, enabling high-resolution electron imaging of samples in non-vacuum environments, by utilizing the graphene as an impermeable membrane and electron transparent window [81]. Graphene membranes have also enabled a new type of photoelectron spectroscopy. By separating the high vacuum detection systems from the sample of interest, detection of samples in various environments (liquid, gaseous) and under a wide range of pressures is now achievable [84], [85].

Given these properties, graphene as a gate electrode for vacuum triode devices offers significant performance advantages over conventional metal gate electrodes. Conventional metal gate electrodes consist of circular apertures surrounding the field emission source; naturally, this geometry causes electron beam divergence towards the gate and high gate losses. Because graphene is both conductive and electron transparent and can be integrated into a vacuum triode as a sheet over the field emission source, significant improvements in beam focusing have been observed that lead to improvements in device efficiency and reduction in gate losses [82], [86]. Finally, the high mechanical strength and thermal conductivity of graphene add to its robustness as a gate electrode material.

Combined with its impermeability to standard gases, this unique set of properties makes graphene an ideal candidate as a gate electrode in portable electron sources, able to seal emitters in vacuum while using the electron source in non-vacuum environments, something unachievable with metal gate electrodes. As seen from the examples above, graphene has been studied in the context of field emission triodes utilizing both sealing and transparency properties, but never in a fully integrated field emission device demonstrating air-ambient operation, which will be the focus of the remainder of this work.

4.2 Device fabrication

4.2.1 Cathode preparation

To fabricate a field emission device with an integrated graphene gate, we first fabricate the cathode, or emitter, tips. To do this, we utilize the fabrication process developed and outlined in Chapter 2 for the fully integrated vacuum-sealed diodes. We use the same starting substrate of Arsenic-doped silicon with resistivity <0.005 Ω-cm. The fabrication sequence is illustrated schematically in Fig. 4.2 and follows the process outlined below:

1. Thin-film deposition: A layer of SiO_2 (thickness ranging from 800–1000 nm) is thermally grown on the starting Si substrate at 1000 °C, followed by atomic layer deposition of a 140 nm thick layer of Al_2O_3 at 300 °C.

2. Patterning and reactive ion etch (RIE): Circular openings are patterned using deep UV (DUV) lithography, and cylindrical cavities are etched into the Al_2O_3 and SiO_2

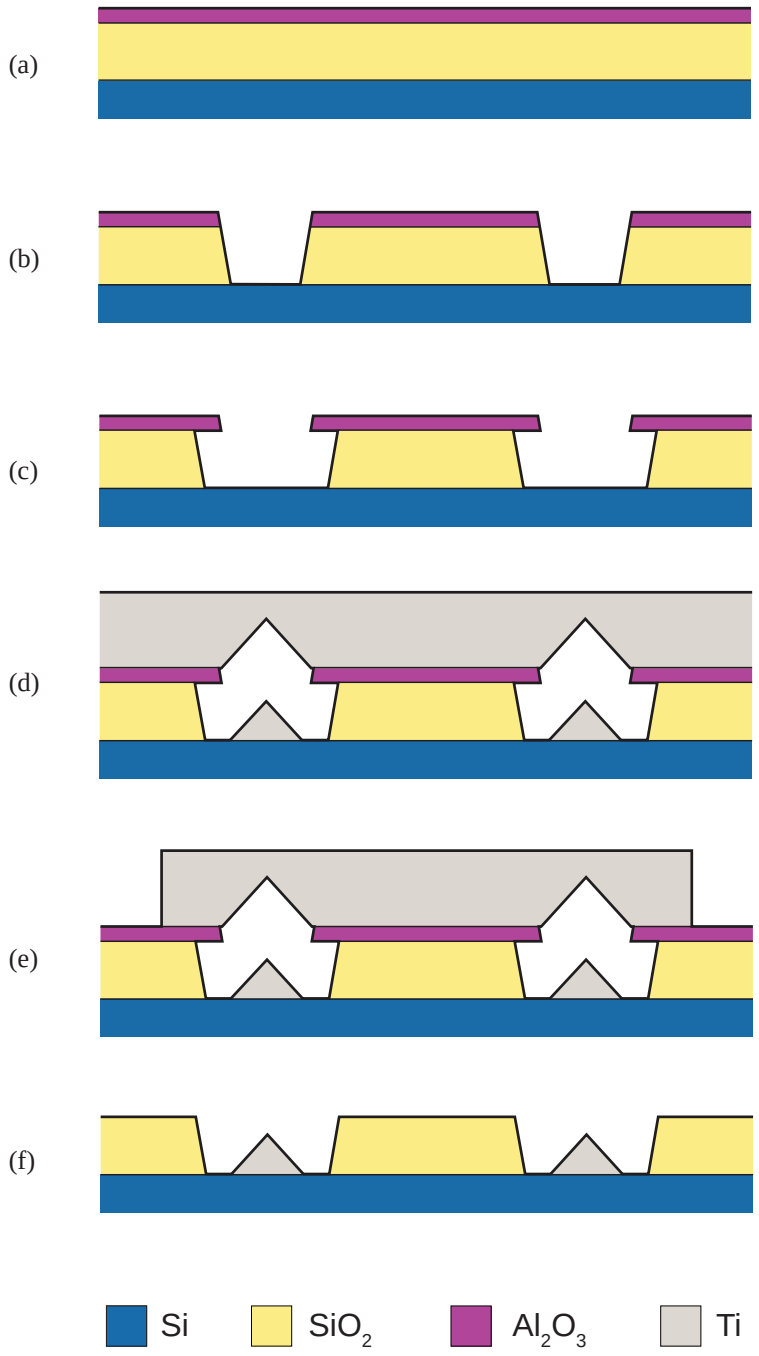
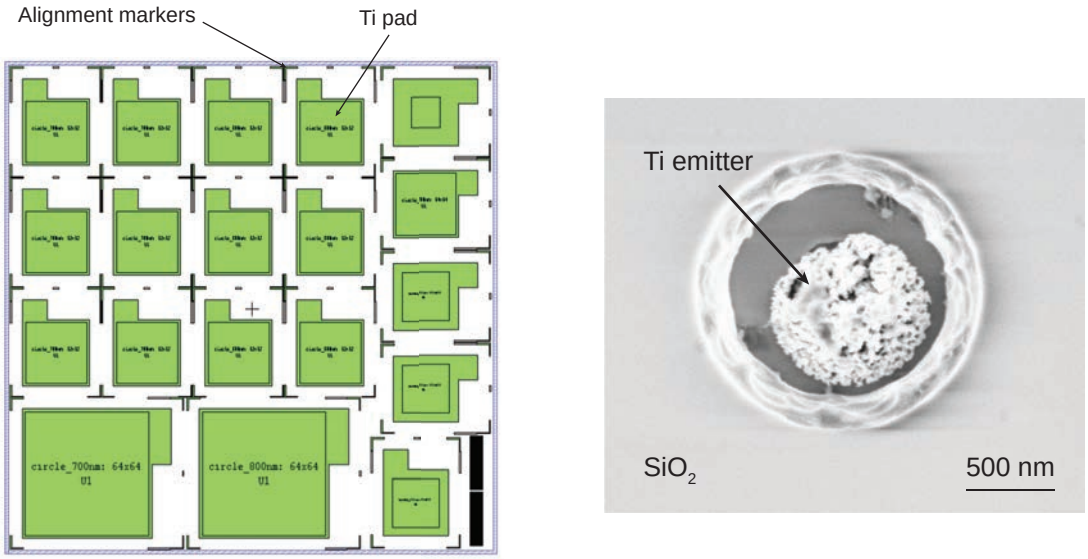


Figure 4.2: Schematic illustration of the fabrication process for preparing the cathode.



(a) (b)

Figure 4.3: (a) Layout of mask in first iteration of lithography for cathode fabrication process, with top-down SEM of emitter shown in (b) indicating visible damage to the emitter.

films using RIE processes consisting of BCl_3/Cl_2 plasma and CHF_3/CF_4 plasma, respectively.

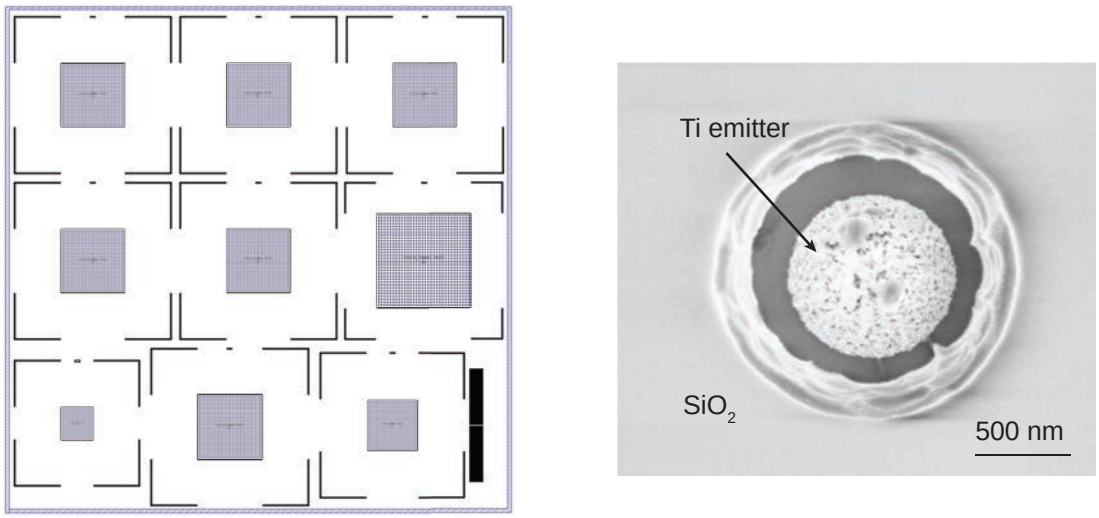
3. Lateral etch: The SiO_2 layer is laterally etched using HF vapor, leaving an alumina overhang at the top of the cavity.

4. Ti e-beam evaporation: An 800 nm thick layer of Ti is deposited by e-beam evaporation, during which the Ti emitters are formed as the cavities are sealed at the top at the evaporation process pressure of 10^{-7} Torr.

5. Device isolation: The top Ti layer is patterned and etched in an RIE process consisting of BCl_3/Cl_2 plasma in order to expose the alumina.

6. Release of top layer: The 6" wafer is diced and the die are then immersed in Al etchant (Transene Type A) at 65 °C to etch the Al_2O_3 layer, lifting off the Ti pads. The die are subsequently immersed in 3 water baths, rinsed with DI water and blow dried with a N_2 gun.

Fig. 4.3(a) shows the first iteration of the mask layout used to pattern the cavities and arrays. Only 700 nm and 800 nm aperture sizes are included, as these showed the best



(a) (b)

Figure 4.4: (a) Layout of mask in second iteration of lithography for cathode fabrication process, with top-down SEM of emitter shown in (b) indicating no damage to the emitter.

field emission characteristics for the diode arrays discussed in Chapter 3. 12/19 devices are 32x32 arrays with 40 μm pitch, to prevent low current from becoming a limiting factor in device characterization. For test purposes, a small sample of 64x64 and 100x100 arrays are also included. The most notable change from the mask layout shown in Fig. 2.3 is that the spacing between device arrays is increased and alignment markers are added. The purpose of both these modifications is to assist with the graphene transfer process, which will be discussed in Section 4.2.3.

The first set of devices fabricated using this mask layout demonstrated poor field emission characteristics. A top-down view of the emitter under SEM, shown in Fig. 4.3(b), indicates visible damage to the emitter. This is attributed to exposure of the Ti emitters to Al etchant during the 6.5 hour etch required to fully attack the Al_2O_3 and release the Ti pad. To address this issue, the mask layout for the Ti layer is modified such that a Ti pad covers each individual cavity and emitter, rather than a single Ti pad covering the entire device array. This results in a significantly larger area of the Al_2O_3 layer exposed to Al etchant upon immersion in the Al etch bath, allowing the etch process to occur more rapidly. The design for the second mask is shown in Fig. 4.4(a). The resulting Al etch process is 2.5 hours and causes minimal damage to the Ti emitters, as can be seen from the SEM in Fig. 4.4(b). In addition to a modified Ti layer, the spacing between arrays is increased further to

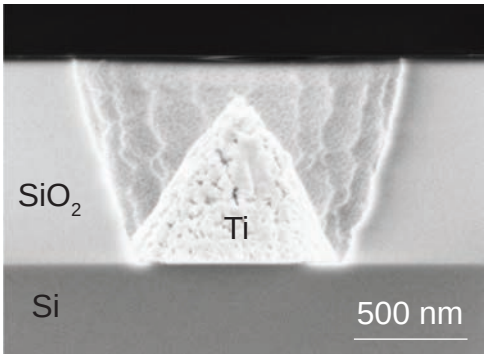


Figure 4.5: Cross-sectional SEM of emitter in silicon dioxide cavity.

make room for metal contacts, due to difficulty probing graphene directly with the probe tip without puncturing the graphene. Ultimately, only 800 nm aperture size arrays are included in this layout due to space constraints.

Fig. 4.5 shows a cross-sectional SEM of the emitter after release of the Al_2O_3 and Ti layers. The inter-electrode distance is defined by the SiO_2 thickness and must be large enough such that the emitter tip is below the top of the SiO_2 layer. For the chosen SiO_2 thicknesses of 822 nm, 918 nm and 1041 nm, SEM analysis showed inter-electrode distance of 121 nm, 171 nm and 276 nm, respectively. With proper modifications to the diode process discussed in Chapter 2, we are thus able to fabricate an unsealed array of cavities in SiO_2 containing Ti Spindt-type field emitter tips.

4.2.2 Graphene preparation

To integrate graphene as a gate layer on the unsealed arrays, graphene was prepared separately prior to transferring the graphene to the cathode chips. Characterization of the transfer process demonstrated that tri-layer graphene is required in order to achieve uniform monolayer coverage over the target substrate after transfer, the results of which are discussed in more detail at the end of this chapter, in Section 4.2.4. The preparation sequence to achieve tri-layer graphene is illustrated schematically in Fig. 4.6 and follows the process outlined below:

(a) Commercially-grown monolayer graphene on Cu foil is cut into 2 cm x 2 cm pieces, taped to a glass slide and placed into a low-power O2 plasma to etch graphene from one side of the Cu foil.

(b) The Cu foil is removed from the slide and flipped over, and a 200 nm layer of PMMA is spin-coated onto the graphene, then baked at 95 °C for 3 minutes.

(c) The sample is placed into a $Na_2S_2O_8$ solution to etch the Cu, for approximately 3 hours.

(d) The PMMA/graphene sample is transferred into a series of water baths.

(e) Step (a) is repeated with another piece of monolayer graphene on Cu foil and is used to scoop the PMMA/graphene sample from the water bath. The PMMA/graphene stack is left to dry for 1 hour, then baked at 95 °C for 5 min.

(f) Steps (c) and (d) are repeated, leaving a PMMA/bi-layer graphene sample floating in the water bath. Step (e) is then repeated with a third piece of monolayer graphene on Cu foil and the PMMA/tri-layer graphene/Cu stack is cut into 2 mm x 2 mm pieces.

(g) Steps (c) and (d) are repeated once again, leaving a PMMA/tri-layer graphene sample in the water bath.

(h) The PMMA/tri-layer graphene sample is scooped onto a PDMS stamp that is supported by a glass slide. The sample is left to dry for 1 hour, followed by a 45 °C bake for 5 min and 95 °C bake for 10 min to cure the PMMA.

(i) The PMMA/tri-layer graphene/PDMS/glass slide stack is placed into an acetone bath for 10 min to remove the PMMA layer.

(j) The sample is then cleaned with IPA for 2 min and dried with a N_2 gun, leaving a stack of tri-layer graphene on PDMS, supported by a glass slide.

4.2.3 Transfer process

A dry transfer stage equipped with a heating pad was used to transfer the tri-layer graphene onto the device chip after cleaning the chip with O_2 plasma. The transfer process is illustrated schematically in Fig. 4.7 and follows the process outlined below:

(a) The device chip is loaded face up onto the transfer stage, while the tri-layer graphene/PDMS sample (still supported by a glass slide that is not shown) is loaded face down onto another platform above the chip. The sample is aligned to the appropriate location over the device chip using the alignment markers on the device chip as a guide.

(b) The sample is lowered onto the device chip until the graphene is in contact with the SiO_2 layer. The structure is heated to 90 °C for 1 minute to increase the fluidity of the PDMS and encourage adhesion of the graphene to the SiO_2 region of the device chip.

(c) The stage is then allowed to cool at room temperature. After cooling, the adhesion of the graphene to the SiO_2 is strong enough to peel off the PDMS without delaminating the graphene.

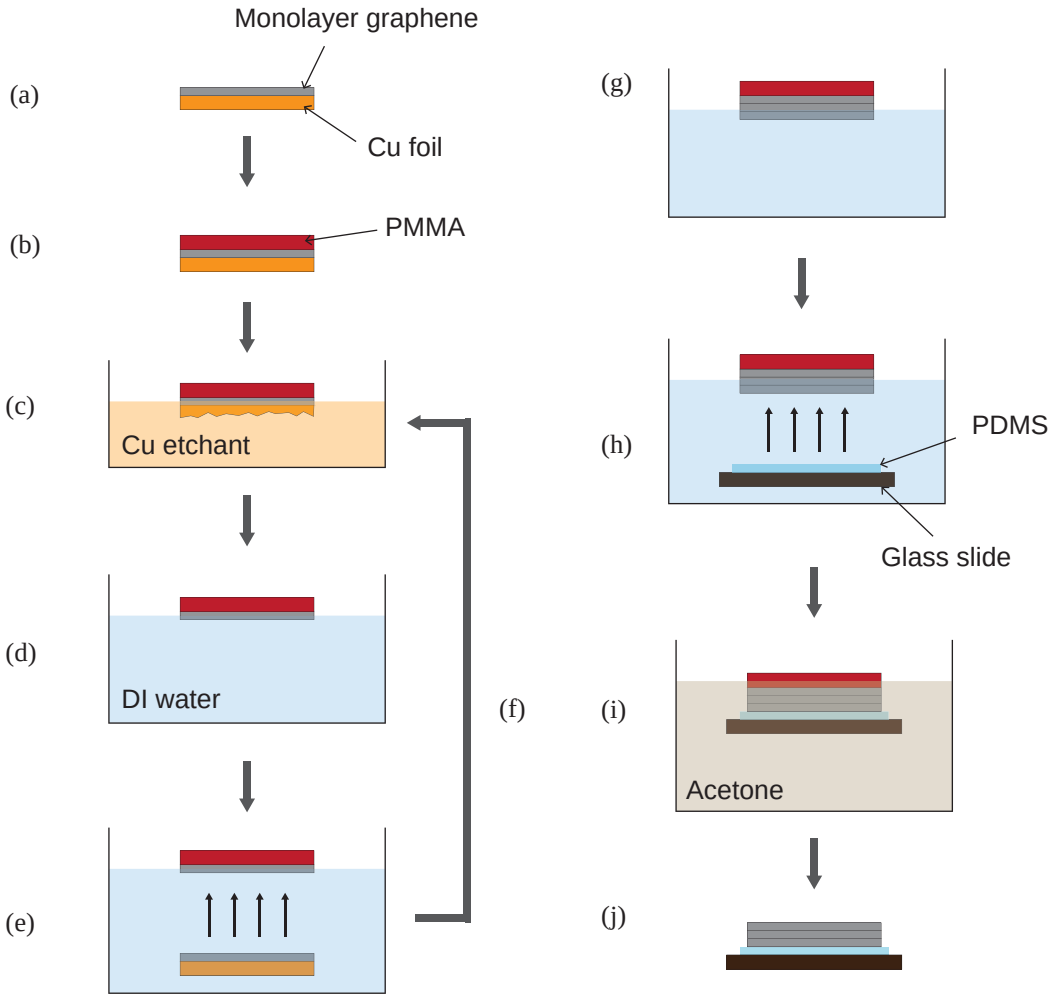


Figure 4.6: Schematic illustration of process sequence for preparation of tri-layer graphene on PDMS, supported by a glass slide.

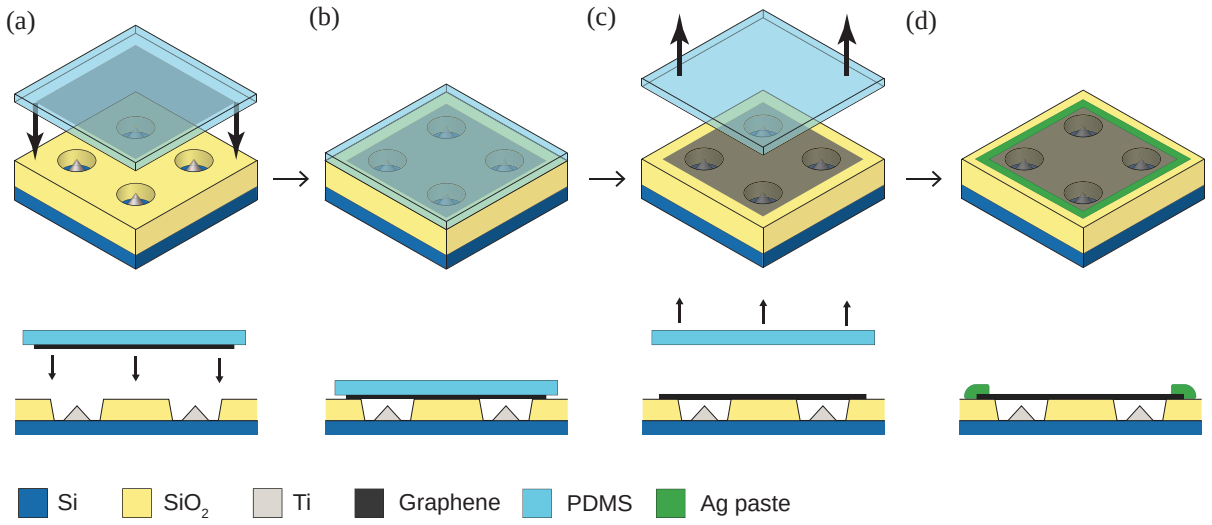


Figure 4.7: Schematic illustration of process for transferring graphene to the cathode chip.

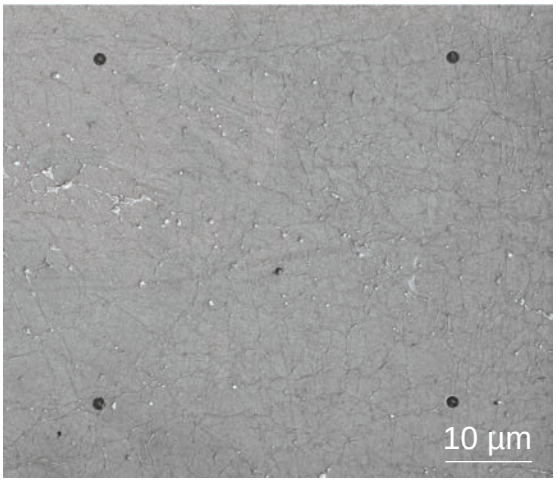
(d) Ag paste is applied around the perimeter of the graphene and cured for use as an electrical contact to the graphene gate.

Fig. 4.8(a) is an SEM of four cavities containing Ti Spindt-type emitters covered with graphene, with a magnified view shown in Fig. 4.8(b) in which the graphene membrane is visibly covering the cavity.

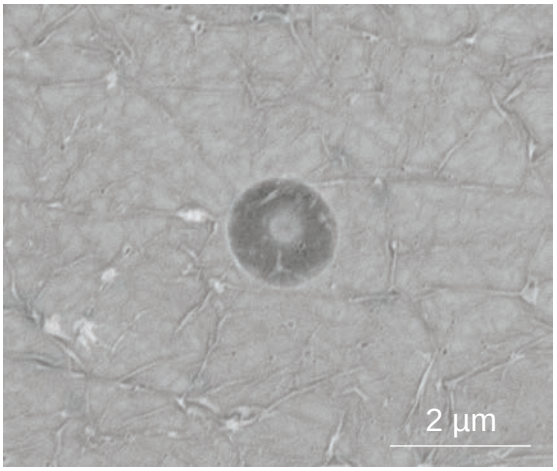
4.2.4 Process characterization

As can be seen from the process flows just described, the goal of the graphene preparation process is to obtain tri-layer graphene on PDMS by stacking three layers of monolayer graphene. It was determined experimentally that three layers are needed to achieve uniform monolayer coverage over the device chip.

Fig. 4.9 shows SEMs of SiO_2 substrates after the graphene transfer process using (a) monolayer, (b) bi-layer and (c) tri-layer graphene. As can be seen from the SEMs, both monolayer and bi-layer graphene result in minimal and sparse coverage over the SiO_2 substrate. This is confirmed by electrical tests indicating poor conductivity across the graphene and Raman measurements indicating several areas over the cavities where no graphene is detected. The transfer process with tri-layer graphene results in much more uniform coverage, with Raman measurements confirming the presence of graphene. These findings suggest that the process of lifting the PDMS stamp from the target substrate causes delamination of graphene from the SiO_2 when only monolayer graphene on PDMS is used. The addition of an intermediate layer of graphene results in minimal improvement, suggesting that the



(a)



(b)

Figure 4.8: (a) SEM of emitter array sealed by graphene, with magnified view shown in (b).

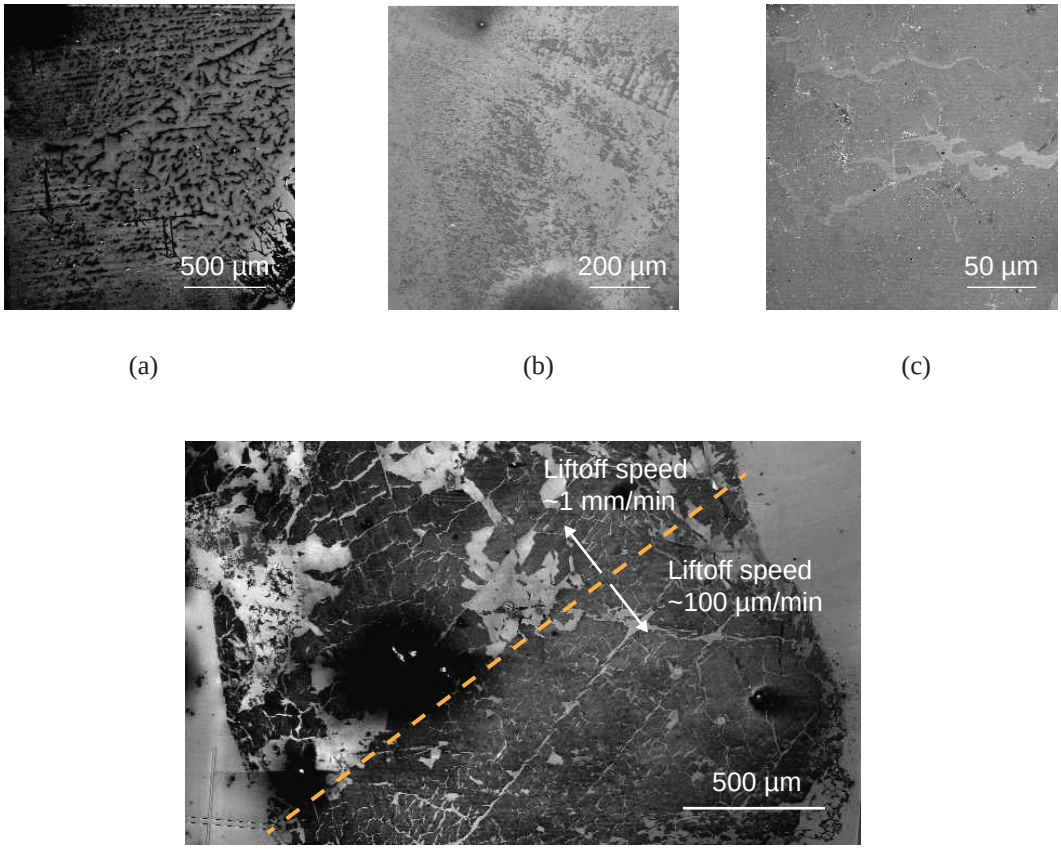


Figure 4.9: SEM of chip after graphene transfer with (a) monolayer, (b) bi-layer and (c) tri-layer graphene, indicating differences in uniformity and coverage. (d) SEM of chip after graphene transfer starting with a tri-layer graphene stack under two different liftoff speeds.

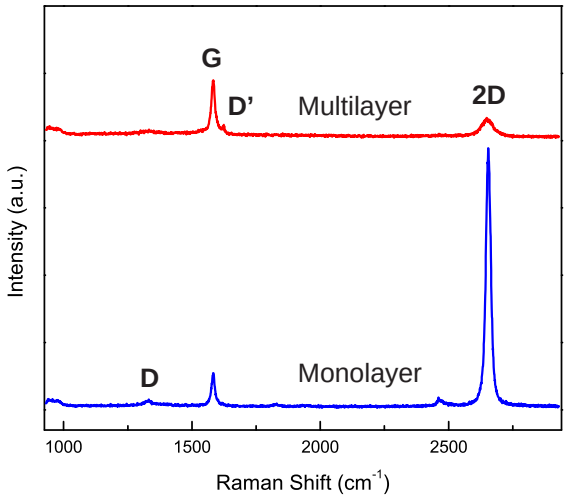


Figure 4.10: Raman spectra of graphene after transfer onto cathode chip.

adhesion of graphene to itself and to PDMS is still stronger than the adhesion of graphene to SiO_2 in the process utilized here. The addition of a third layer of graphene results in good monolayer coverage, suggesting that the adhesion of graphene to SiO_2 now exceeds the adhesion of graphene to itself.

A notable finding from the tri-layer graphene transfer process is that mostly monolayer graphene is left on the target substrate after the transfer process. To further characterize this, Raman spectra were taken on ∼50 different membranes on a number of device arrays. The bottom spectra in Fig. 4.10 is indicative of ∼80% of the membranes measured. The presence of a single, sharp peak at the 2D band, with a smaller peak at the G band and a minimal peak at the D band indicates monolayer graphene with few defects [87]. An enhanced peak intensity ratio (I_{2D}/I_G) of 7.4 is observed for the spectra in the plot and is representative of suspended monolayer graphene, as compared to standard ratios of 2-4 for supported monolayer graphene [88]. The top spectra in Fig. 4.10 is indicative of ∼20% of the membranes measured. A smaller, broader peak at the 2D band and stronger, sharper peak at the G band, as compared to the bottom spectra, indicates the presence of multilayer graphene. A small peak appears at the D' band, which indicates disorder in the graphene [89]. Therefore, Raman measurements across the sample reveal mostly monolayer coverage with some areas of bi-layer and tri-layer coverage, suggesting that more careful and extensive characterization is required to understand the fundamental mechanisms and process details impacting the results of the transfer process.

The speed at which the tri-layer graphene/PDMS sample is lifted off the device chip also affects coverage quality. Fig. 4.9(d) shows a sample with tri-layer graphene transferred at two different liftoff speeds, illustrating the significant improvement in uniformity and coverage for the smaller liftoff speed. We estimated the minimum speed for the transfer stage to be 100 Âµm/minute and maintain this speed in the transfer process.

4.3 Results and discussion

The device fabricated in Section 4.2 can be utilized as a portable electron source upon demonstration of three key capabilities:

1. The use of graphene as an electron extraction electrode for Ti Spindt-type field emitters, in both a diode and triode configuration.
2. The use of graphene as a vacuum seal for a $\sim$1.5 μm-wide opening in a $\sim$1 μm thick SiO_2 film.
3. The transparency of graphene to electrons at energy levels corresponding to the energy levels of the electrons extracted from the Ti Spindt-type field emitters.

A series of experiments was conducted to demonstrate these capabilities, the results of which are presented and discussed in this section. All I–V measurements are done using a Keysight B1500A semiconductor device parameter analyzer.

4.3.1 Electron extraction

Experimental setup

The first key objective is to test the use of graphene as an electron extraction electrode for the field emitter tips, which can be done by testing the device in a diode configuration under ideal vacuum conditions. To set up this experiment, the devices are first held at 10^{-6} Torr for $\sim$18 hours to achieve vacuum in the cavities. The pumpdown procedure is necessary because the graphene transfer process is done in air, sealing the cavities at atmospheric pressure. By keeping the devices under vacuum for a sustained period of time, the cavities are pumped down through the area of SiO_2 that is exposed to air. After pumpdown, the devices are biased per the configuration shown in Fig. 4.11 and measured in a vacuum probe station held at 10^{-6} Torr. The graphene serves as the anode electrode and is contacted through the Ag paste, while the substrate serves as the cathode contact and is electrically connected to the emitters. By applying a positive voltage to the graphene and grounding the substrate, electrons should emit from the cathode towards the graphene anode in a manner representative of Fowler-Nordheim tunneling.

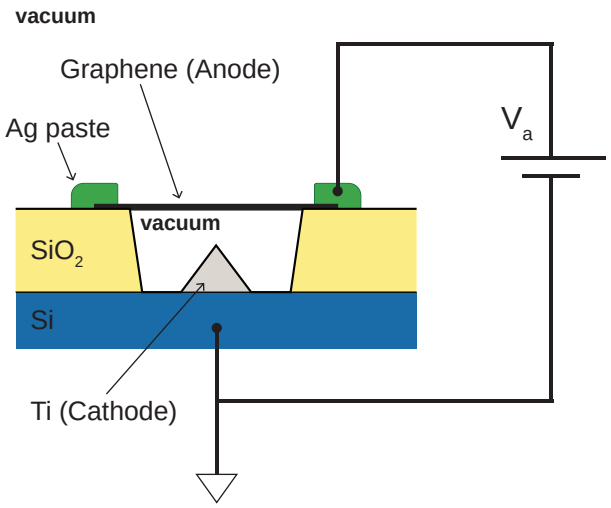


Figure 4.11: Test setup for diode configuration, under ideal vacuum conditions.

Field emission measurements

Fig. 4.12 shows typical I–V characteristics for a 32x32 array of emitters, for a device with 822 nm thick SiO_2. The onset of field emission is observed around 11 V, confirmed by the linearity of the measured data in the FN plot, shown in Fig. 4.12 inset. Current saturation is observed at around 1 μA, giving an estimated current / tip of $\sim$1 nA. Fig. 4.13 shows typical I–V characteristics for a 32x32 array of emitters, for a device with 1041 nm thick SiO_2. The onset of field emission is observed at 8 V, with the current saturating at 1 μA. Measurements taken for multiple devices with varying SiO_2 thicknesses demonstrate saturation currents between 1 and 10 μA and threshold voltages between 8 and 30 V. Similarities to the I–V profiles for the diode arrays characterized in Chapter 2 validate the effectiveness of graphene as an electron extraction electrode.

Lack of a clear trend between threshold voltage and oxide thickness suggests that there may be performance effects due to device variation that can be reduced by optimizing the fabrication process. In addition, it is feasible that the field lines between the graphene anode and Ti tip are primarily a function of the graphene and tip curvatures rather than the inter-electrode distance, resulting in a threshold voltage that is somewhat independent of the inter-electrode distance. This has been observed to be true for carbon nanotubes, in cases where the inter-electrode distance is much greater than the nanotube diameter. This results in a field enhancement effect that is independent of inter-electrode distance and primarily a function of the nanotube height and tip diameter [90].

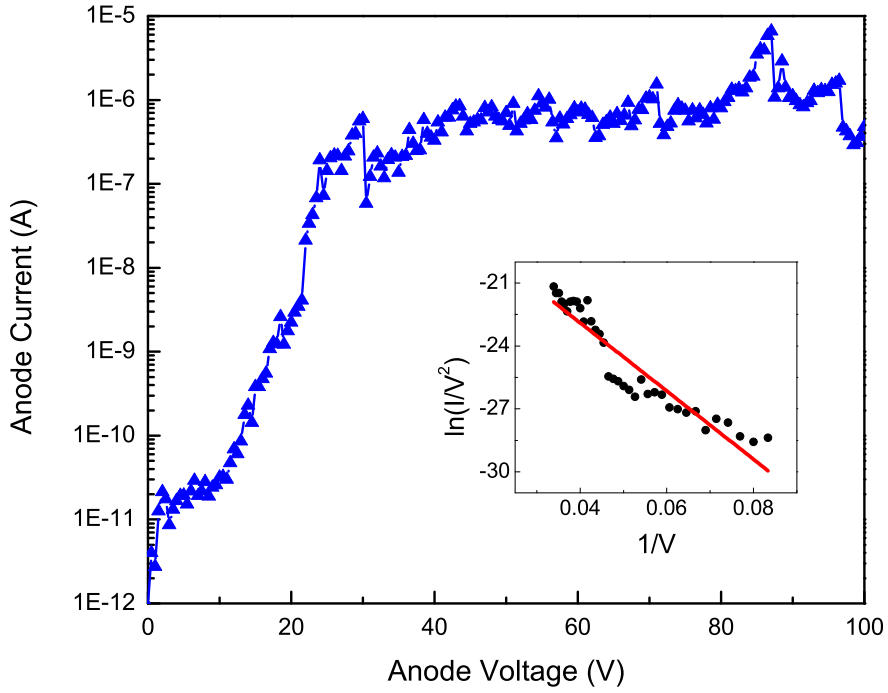


Figure 4.12: Measured I-V characteristics for a 32x32 diode array with 822 nm thick SiO_2 under 10^{-6} Torr vacuum.

4.3.2 Atmospheric sealing

Experimental setup

The next objective is to validate that the transferred graphene is effectively vacuum-sealing the cavities. To do this, a series of measurements are done under different vacuum conditions in the cavity, which are expected to have an effect on field emission performance. For all tests, the devices are biased per the configuration shown in Fig. 4.14 and measured in clean, dry air. The graphene anode is positively biased, while the emitter cathode is grounded through the substrate. As a control, measurements are taken after the graphene transfer process, when the cavity is still at atmospheric pressure. The devices are then held under 10^{-6} Torr vacuum for several hours to achieve vacuum in the cavities and additional measurements are done.

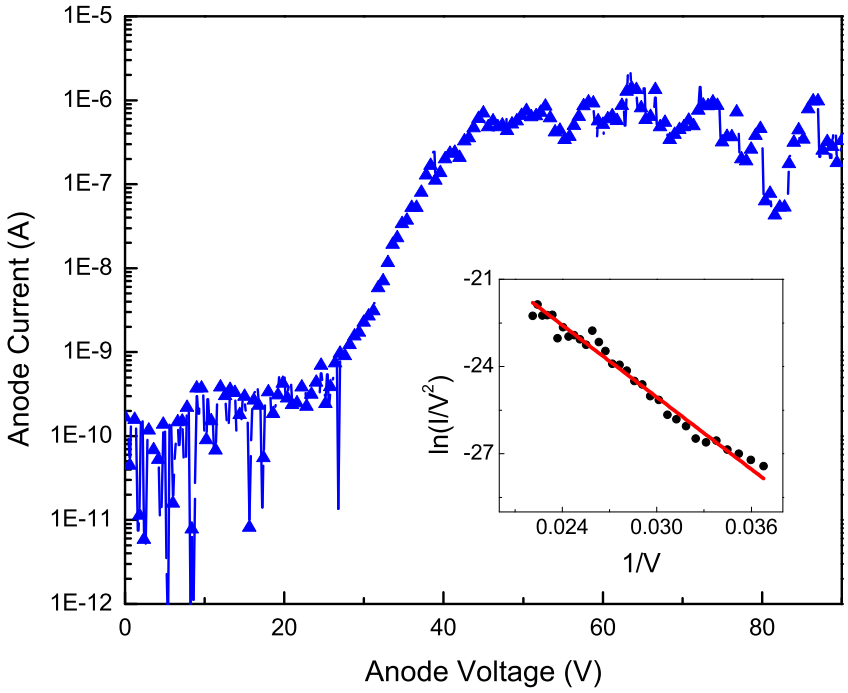


Figure 4.13: Measured I-V characteristics for a 32x32 diode array with 1041 nm thick SiO_2 under 10^{-6} Torr vacuum.

Field emission measurements

Fig. 4.15 displays representative I–V characteristics for devices measured under different initial conditions. Fig. 4.15(a) plots two sweeps of a device after transfer, when the cavities are at atmospheric pressure. In the first sweep, the onset of field emission is observed at ∼15 V. The corresponding FN plot is provided in the inset, characterized from 15 V to 25 V, resulting in a goodness of fit with an r-squared value of 96%.

Despite the cavity containing air, field emission is expected to occur due to the small inter-electrode gap, on the order of 100 to 200 nm (as indicated by deflection measurements discussed in Section 4.3.2). The mean free path of electrons in air is on the order of 1 micrometer, making it significantly larger than the inter-electrode gap and therefore feasible that electrons will be collected at the graphene anode without experiencing collisions along the way [91]. However, it is important to note that successful FN analysis is only done for the voltage range corresponding to the region of the I–V profile with fairly linear behavior; this starts at 15 V and ends around 25 V, when the current drops and exhibits unstable

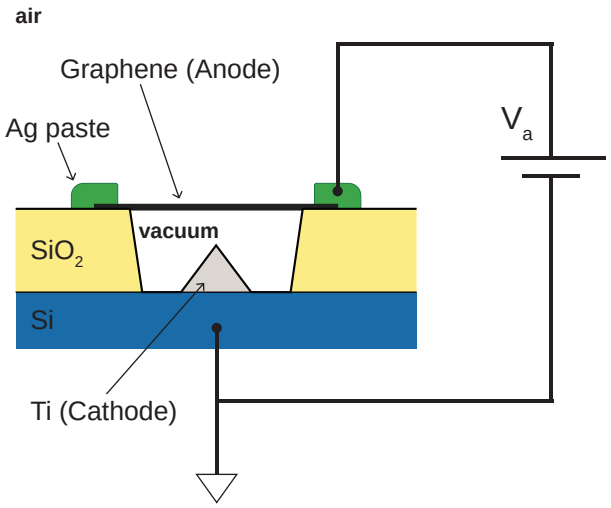


Figure 4.14: Test setup for diode configuration, tested in clean, dry air after vacuum pump-down of the cavities.

behavior as the sweep continues up to 50 V. FN analysis outside of this region results in a very poor linear fit of the data. The non-linear regimes in the plot suggest that processes other than field emission may be occurring, particularly those related to air ionization, which will be discussed in detail in Section 4.3.4.

Due to operation in air, significantly worse performance is observed in subsequent sweeps, an example of which is shown in the I–V profile labeled sweep 2. If air ionization is occurring, the ionized atoms as well as other gaseous species in the air can cause degradation of the cathode. In addition, a significant amount of leakage is seen at low voltages that does not follow a profile characteristic of Fowler-Nordheim tunneling. This suggests that another conductive path, such as sidewall leakage between the substrate and the graphene, is masking intrinsic device behavior and dominates the measured current between the cathode and anode contacts. Because of this, intrinsic device behavior and field emission performance is difficult to quantify. Clean device performance cannot be replicated more than once for the devices with cavities held at atmospheric pressure.

Fig. 4.15(b) plots the emission characteristics of a device measured in air after being held under 10^{-6} Torr vacuum for ∼15 hours. In the first sweep, the onset of field emission is observed at ∼2.5 V and the current saturates at 6 V. The corresponding FN plot is provided in the inset, characterized from 2.5 V to 6 V, resulting in a goodness of fit with an r-squared value of 89.2%. Sweep 2 shows slightly worse performance, but the data can still be fit to a straight line, with an r-squared value of 69.7%.

Comparing Fig. 4.15(a) to Fig. 4.15(b), instabilities are seen in both sets of plots. How-

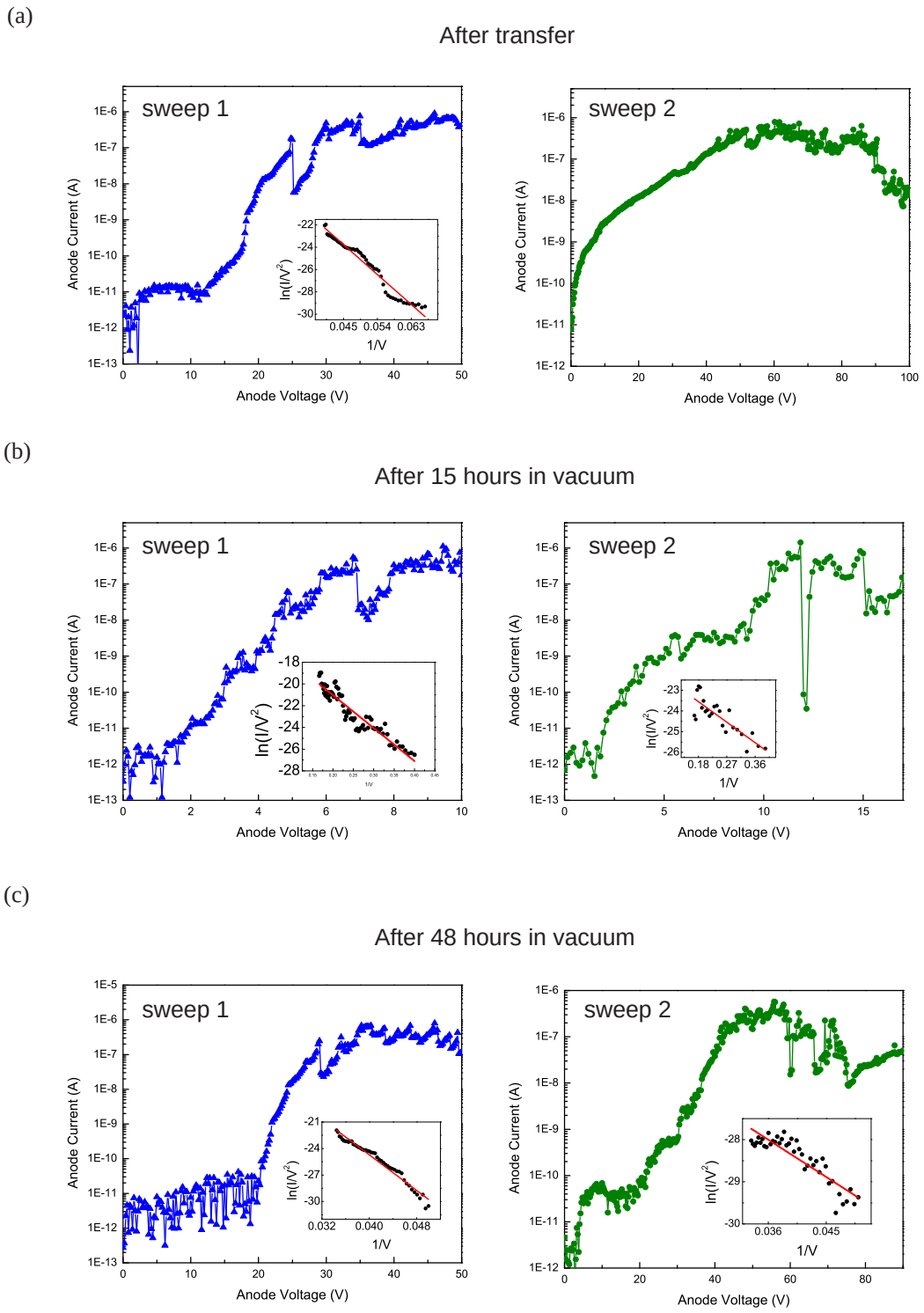


Figure 4.15: Representative I-V characteristics for 32x32 diode arrays tested in clean, dry air after being held at 10^{-6} Torr vacuum for (a) 0 hours, (b) 15 hours and (c) 48 hours.

ever, cleaner Fowler-Nordheim tunneling characteristics are observed in Fig. 4.15(b). In addition, the first and second sweeps are more consistent for the devices held under vacuum, and field emission performance can be measured more than once. The measurements suggest that improved, repeatable device performance can be achieved by operating the emitters in vacuum. More importantly, this confirms that the graphene membrane is able to maintain vacuum within the cavity after the pumpdown procedure, manifesting in improved device performance.

Fig. 4.15(c) plots the emission characteristics of a device measured in air after being held under 10^{-6} Torr vacuum for ∼48 hours. Sweep 1 demonstrates very clean turn-on characteristics, with clearly defined regions indicating a steep onset of field emission and the onset of current saturation, with few instabilities. The data in the FN plot are fit to a straight line, from 20 V to 30 V, with an r-squared value of 96.7%. Sweep 2 also shows clean field emission performance, albeit some instabilities after 60 V. Fitting the data from 20 V to 30 V on an FN plot results in an r-squared value of 78.6%, suggesting a worse fit than that of sweep 1, but better than the decline in fit from sweep 1 to sweep 2 for Fig. 4.15(b). The clean, repeatable performance of Fig. 4.15(c) indicates that there is a change in device performance when the cavity is held under vacuum for an increasing number of hours. This is attributed to an increase in the vacuum level of the cavity, which is sealed by the graphene membrane. In addition, other leakage paths are suppressed when the cavity is in vacuum, evidenced by the low noise floor prior to onset of field emission.

Comparing the three sets of plots, clear observations can be made. First, it can be seen that the worst performance is measured right after transfer with no pumpdown while the best performance is measured after 48 hours of pumpdown. Second, device performance cannot be repeatably measured without vacuum pumpdown of the cavity. Therefore, higher vacuum levels in the cavity result in improved and repeatable device performance in air. Most importantly, these improvements are made possible by the vacuum-sealing properties of the graphene membrane. Indeed, if the graphene membrane were not effectively vacuum-sealing the cavities after the devices were removed from vacuum and tested in air, no difference in device performance should be detected. The effectiveness of the seal is demonstrated in the measured changes in device performance. Thus, we have validated that the graphene is able to seal the cavity in vacuum, enabling device operation in air.

AFM measurements

When the internal cavity of the device is in vacuum but the external ambient is at atmospheric pressure, a pressure difference exists across the graphene membrane. Prior literature has shown that this pressure difference exerts a force that causes the membrane to deflect either upward or downward, depending on the direction of pressure, as illustrated in Fig. 4.16 [45]. To validate that the observed changes in diode device performance are due to changes in the cavity vacuum, atomic force microscope (AFM) images are taken to detect corresponding deflections in the membrane as the cavity conditions are varied.

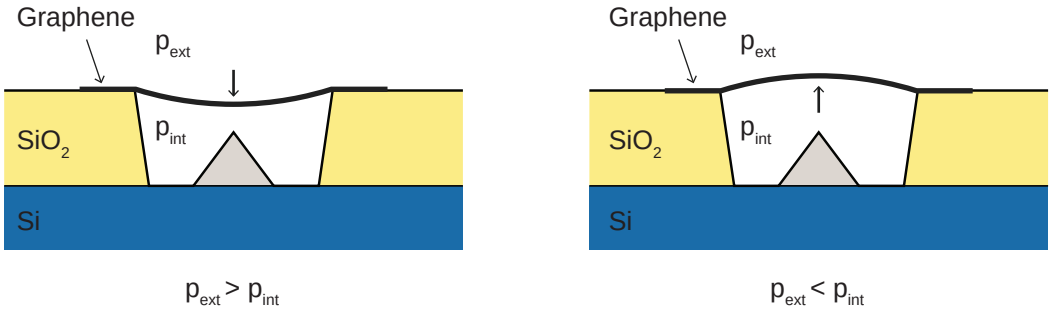


Figure 4.16: Schematic illustration of graphene membrane deflection under different pressure conditions. In scenario (a), the pressure external to the cavity is greater than the internal cavity pressure, resulting in a downward deflection of the membrane. In scenario (b), the pressure external to the cavity is lower than the internal cavity pressure, resulting in an upward deflection of the membrane.

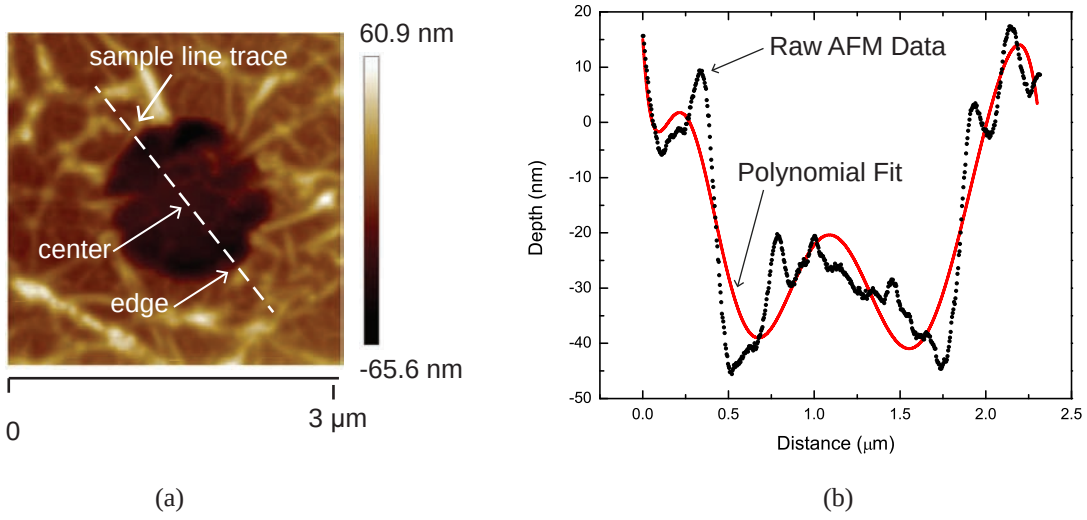


Figure 4.17: (a) Tapping-mode AFM image of a graphene membrane suspended over a single cavity. (b) Plot of a single line trace of the AFM data, along with a best fit polynomial curve for analysis.

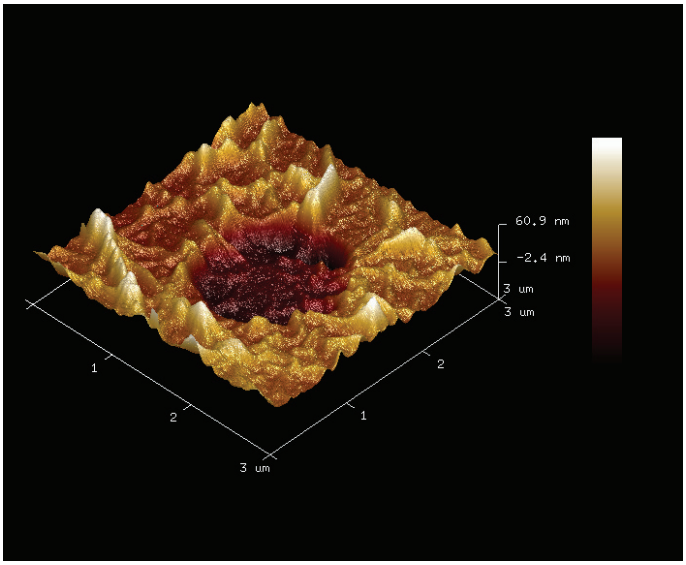


Figure 4.18: 3D image of AFM scan indicating variation in depth across surface of sample.

Table 4.1: AFM Data for Graphene Membranes After Varying Pumpdown Times

	Device A2		Device C2	
Pumpdown Time (Hours)	**Depth from edge to center (nm)**	**Rate of curvature change at center**	**Depth from edge to center (nm)**	**Rate of curvature change at center**
0	13.65	-250	23.09	-445
15	15.99	-219	26.69	-326
48	22.86	-177	28.78	-229

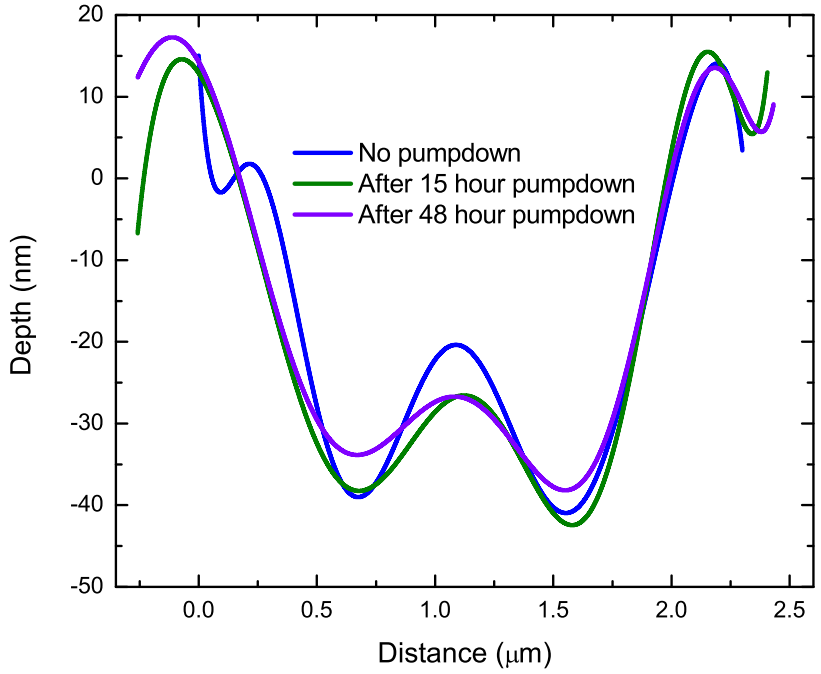


Figure 4.19: Representative plot of graphene membrane deflection measured in air after device pumpdown for 0 hours, 15 hours and 48 hours. As the pumpdown time increases, the internal cavity pressure decreases.

Fig. 4.17(a) shows a representative tapping-mode AFM image of a suspended graphene membrane taken over a single cavity in the device array. The dotted line indicates a line trace taken through the center of the graphene membrane, the data for which is plotted in Fig. 4.17(b), along with a polynomial curve that best fits the data. A corresponding 3D image of the scan is shown in Fig. 4.18. The line trace and AFM images indicate a ∼55 nm dip in the membrane at the edge of the SiO_2 cavity. This feature is consistent with that of the AFM plots in the study by Bunch, et. al, and is attributed to the strong van der Waals forces between the graphene membrane and SiO_2 sidewalls.

To determine the effect of increased cavity vacuum on membrane deflection, AFM scans are done in air over membranes after transfer and after being held under 10^{-6} Torr vacuum for 15 hours and 48 hours; these conditions correspond to the same experimental conditions as the results shown in Fig. 4.15. Fig. 4.19 is a representative plot of the three polynomial fits for a suspended graphene membrane. The plots show that as the pumpdown time increases, the membrane is pulled downwards, closer to the cathode, as a result of the higher pressure

external to the cavity. This effect is illustrated schematically in Fig. 4.16(a). This validates that leaving the device to pump down in vacuum results in a lower pressure in the cavity; the lower pressure causes a downward deflection of the graphene membrane when measured in air. This trend is consistent for measurements taken on multiple membranes/cavities for multiple devices.

Table 4.1 displays additional results of AFM scans for two selected membranes on different devices to illustrate other key parameters that validate the presence of a pressure difference across the membrane. Each of the results displayed here represent the average of the results for three different line traces taken across the same membrane. For both devices, the vertical distance from the top of the SiO_2 to the center of the graphene membrane increases as the pumpdown time increases. This suggests that as cavity vacuum increases, the membrane is pulled closer to the cathode and further from the top surface of the SiO_2. Also displayed is the rate of change of curvature of the membrane around the center of the cavity. To calculate this rate, the curvature of the best fit line is calculated for a subset of data around the center of the membrane. Then, a linear fit is performed and the slope is calculated to determine how quickly the curvature changes in the selected region. It can be seen that there is a decrease in this rate as the pumpdown time increases, with the smallest curvature change seen for the sample held under vacuum for 48 hours. This suggests that the membrane also becomes flatter as the level of vacuum increases.

Thus, the AFM results suggest the following:

1. As the pumpdown time increases, the level of vacuum in the cavity increases.

2. The graphene membrane seals the cavity, as evidenced by measured downward deflections in the membrane.

3. The observed changes in membrane deflections correlate with the improvements in field emission performance, as shown in Fig. 4.15.

It should be noted that while the analysis above enables comparisons of the suspended graphene membrane under varying cavity vacuum conditions, it does not enable specific conclusions to be made regarding the amount of deflection for a given pressure differential across the membrane. First, the exact level of vacuum in the cavity is not measured, preventing calculation of the magnitude of the pressure difference across the membrane. Second, although the overall profile and shape of the membrane are clearly seen from the AFM scans, there are areas of surface roughness that reduce our confidence in drawing conclusions regarding the exact magnitude of the deflection for a given pressure differential. This surface roughness is attributed to both non-uniformities in membrane thickness as well as surface impurities from the fabrication and transfer processes.

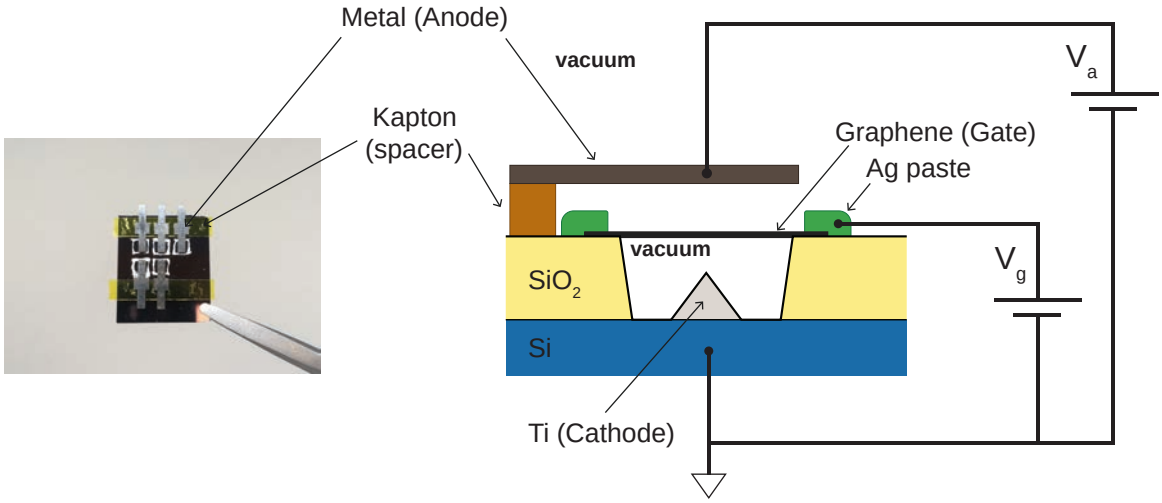


Figure 4.20: (a) Single device chip after preparation for triode testing. (b) Test setup for triode configuration, under ideal vacuum conditions.

4.3.3 Electron transparency

Experimental setup

The final objective is to validate the electron transparency of the suspended graphene membrane, so that electrons can be extracted into a non-vacuum ambient external to the vacuum-sealed cavity. For this measurement, the devices are modified to add a third electrode for collecting electrons transmitted through the graphene. To add the third electrode, 100 μm thick pieces of double-sided Kapton tape are first placed at the edges of the sample, as shown in Fig. 4.20(a). Then, laser cut stainless steel pieces are placed on top of the Kapton and over the device arrays, to serve as a metal anode. The width of the metal anode is equivalent to the width of the 32x32 emitter array, approximately 1.2 mm; the metal anode covers the area of the device array without covering the Ag paste, which is needed to probe the graphene. The Kapton tape acts as a physical spacer that also provides extremely high electrical and thermal insulation between the metal anode and the device chip.

For this set of experiments, the devices are tested under ideal vacuum conditions to measure intrinsic device behavior. First, the devices are first pumped down at 10^{-6} Torr for $\sim$18 hours to achieve vacuum in the cavities. After pumpdown, the devices are biased per the configuration shown in Fig. 4.20(b) and measured in a vacuum probe station held at 10^{-6} Torr. The substrate is grounded and serves as the cathode contact, while the graphene and metal are positively biased and serve as the gate and anode electrodes, respectively. As with

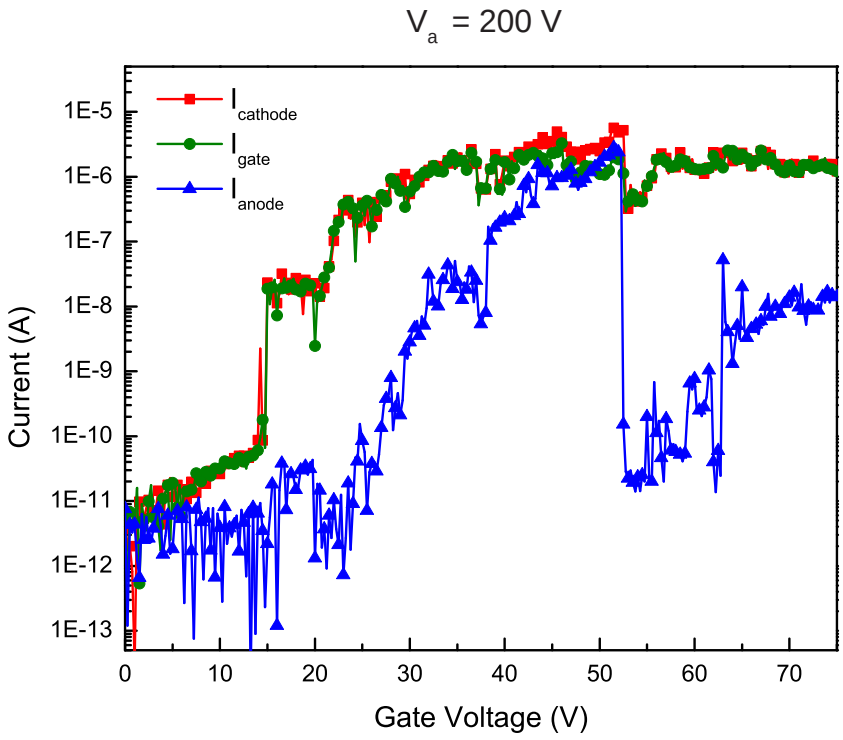


Figure 4.21: Transfer characteristics for a triode array, with an anode voltage of 200 V.

the triode arrays in Chapter 3, electrons emit from the cathode towards both the gate and anode electrodes, with the graphene gate being used as an electron extraction electrode.

Transfer characteristics

Fig. 4.21 is a plot of the transfer characteristics for a 32x32 device array with 822 nm thick SiO_2. The onset of field emission occurs around $V_g = 15$ V, indicated by an exponential increase in gate current as the gate voltage increases. Initially, the majority of the cathode current is captured at the gate. However, starting around $V_g = 25$ V, the anode current also begins to increase in an exponential manner. The detection of both gate and anode currents indicates that the extracted electrons travel to both the gate and anode electrodes, as illustrated schematically in Fig. 4.22. Most importantly, the detection of anode current validates the transparency of graphene to electrons with energies in the operating voltage range for these devices. These results are consistent with previous findings by Hassink, et. al, on the electron transparency of graphene to electrons with energies ranging from 2-40 eV [83].

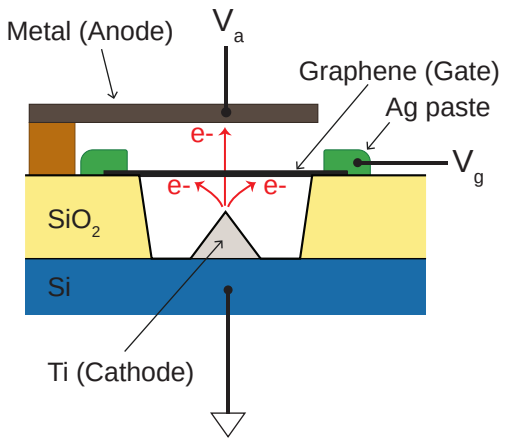


Figure 4.22: Schematic illustration of electron trajectory during operation of triode devices.

As seen in the plot, detection of anode current requires a higher gate voltage than the detection of gate current. This suggests that the extracted electrons have to be of a high enough energy such that they transmit through the graphene membrane and travel across the 100 μm inter-electrode gap between the anode and gate electrodes. Past this energy level, many of the extracted electrons pass through the gate. Indeed, between 25 V and 50 V, the cathode current continues to increase, but rather than observing a corresponding increase in the gate current, we observe a relatively constant gate current and a steep increase in the anode current. This suggests that as more electrons are emitted from the cathode with higher energies at higher gate voltages, these additional electrons are not intercepted by the gate, but instead pass through the gate and contribute to the output current of the device.

The transfer characteristics elucidate a clear relationship between the gate voltage and cathode, gate and anode currents. For the cathode, increasing the gate voltage results in emission of a larger number of electrons from the tip, as evidenced by a steady increase in the cathode current. This is consistent with the idea that the application of a larger field around the cathode tip results in an increase in electron emission, which eventually saturates due to material limitations of the cathode as we have seen previously.

For the gate, an increase in gate voltage initially results in an increase in gate current, but after $\sim$45 V, the gate current saturates. This suggests that as more electrons are emitted from the cathode due to the application of a higher electric field, a larger number of electrons are initially captured at the gate but above a certain voltage, the electrons are more likely to pass through the graphene. This results in a steady increase in anode current, resulting in the ratio of anode current to gate current, plotted in Fig. 4.23. Indeed, the ratio of anode current to gate current increases rapidly, with a peak current gain of nearly 2 despite a

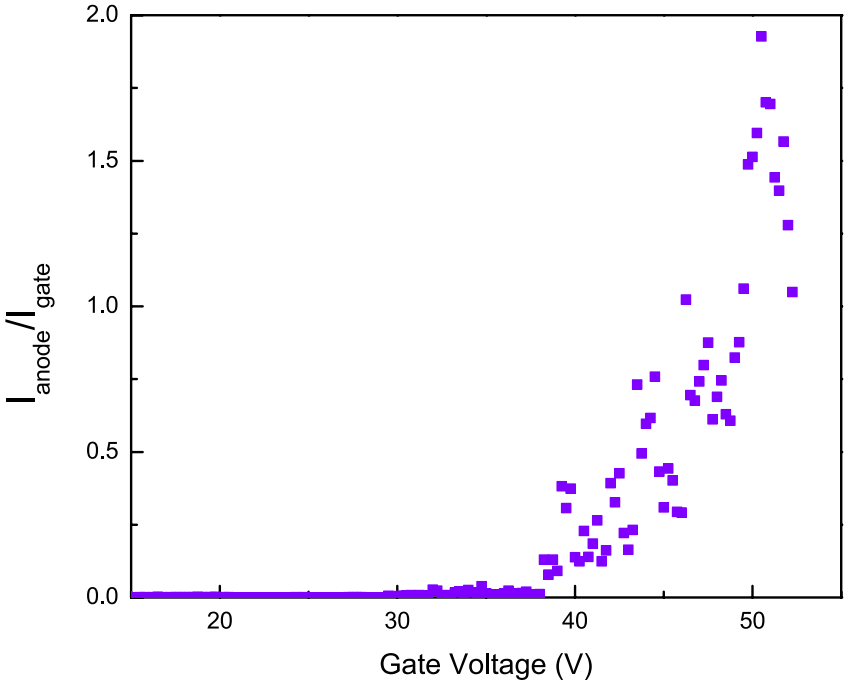


Figure 4.23: Ratio of anode current (I_a) to gate current (I_g) plotted as a function of gate voltage.

large inter-electrode gap of 100 μm. The peak power gain can also be calculated using the following formula:

$$A_v = \frac{I_a V_a}{I_g V_g} \tag{4.1}$$

where I_a and V_a are the anode current and anode voltage, respectively, and I_g and V_g are the gate current and voltage, respectively. Using $I_a/I_g = 2$, $V_a = 200$ V, and $V_g = 50$ V, this results in a power gain of 8. However, the anode voltage is not limited to 200 V, as the spacer is able to sustain much higher voltages if needed. The application of a 200 V bias across the anode and gate electrodes results in no measured current between the electrodes, confirming that the measured anode current is due to intrinsic device behavior and cannot be attributed to leakage across the spacer.

To determine the influence of anode voltage on electron extraction, devices are also tested in a two-terminal mode, with the cathode grounded, the gate floating and the anode voltage swept from 0 V to 200 V. No current is detected at the anode in this configuration, both

before and after the transfer measurements above, demonstrating that the anode does not have an effect on electron extraction from the cathode. The application of 200 V across a 100 μm gap results in an electric field on the order of 10^4 V/cm, which is insufficient for field emission to occur. Thus, the only configuration in which anode current is measured is when the gate is positively biased to extract electrons from the cathode, which ultimately pass through the graphene and land at the anode.

The increase in anode current despite a constant anode voltage demonstrates that the variation in gate voltage, and subsequent variation in energy levels of the emitted electrons, causes non-linear changes in the electron transparency of the graphene membrane. The non-linear manner in which the electrons are absorbed by and transmit through the graphene has been observed in prior literature [82], [83]. Variations in membrane thickness, as evidenced by the Raman spectra analysis, could easily result in non-linear changes in the proportion of electrons intercepted by and passing through the graphene.

The role of the graphene membrane as an electron-transparent gate is further validated by instabilities seen in the cathode current that are replicated in both the gate and anode currents. For example, at $V_{\mathrm{g}} = 52.5$ V, the cathode current rapidly drops, likely due to a breakdown event, as we have seen in Section 2.3.5. Fewer electrons are emitted from the array, leading to a corresponding reduction in gate current and a very rapid reduction in anode current. Post-testing inspection under SEM indicates that breakdown events such as these cause the emitters to rupture, as we have also seen in Section 2.3.5, and also damage the graphene. Once the graphene is damaged, the electrons do not need to pass through the graphene to reach the anode; however, damage to the membrane is only caused by ruptured emitters, which can no longer contribute current.

Additional analysis of the currents measured at each terminal in the triode configuration indicates that the total amount of gate and anode current does not account for all the cathode current. Fig. 4.26(a) plots the additional component of current coming from the cathode that is not accounted for at either the gate or anode electrodes. The profile of this current shows that even at the onset of field emission, not all of the electrons are captured at the gate. Therefore, some proportion of electrons are lost to other parts of the device or test setup. Eventually as more electrons are emitted as the gate voltage increases, a larger fraction of the emitted electrons are captured at the anode. The output plots suggest that as the anode voltage increases, fewer electrons are lost elsewhere in the test setup. Some of this current loss could be due to misalignments between the metal anode and emitter array surfaces, resulting in electron emission by emitters that are not directly under the metal anode and thereby escaping collection at the anode. Fig. 4.26(b) performs the same analysis for the diode arrays tested in vacuum. In this configuration as well, not all of the electrons emitting from the cathode are collected by the graphene, which serves as the anode electrode in this setup. Interestingly, the diode measurements confirm that electron transparency is observed even without validation from the triode measurements.

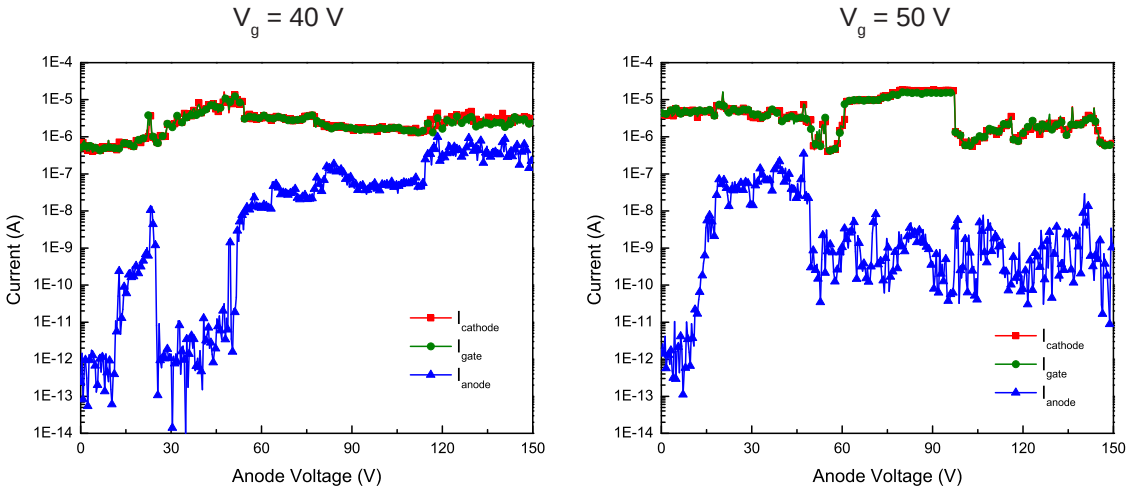


Figure 4.24: Output characteristics for a triode array with 822 nm thick SiO_2 for V_g equal to (a) 40 V and (b) 50 V.

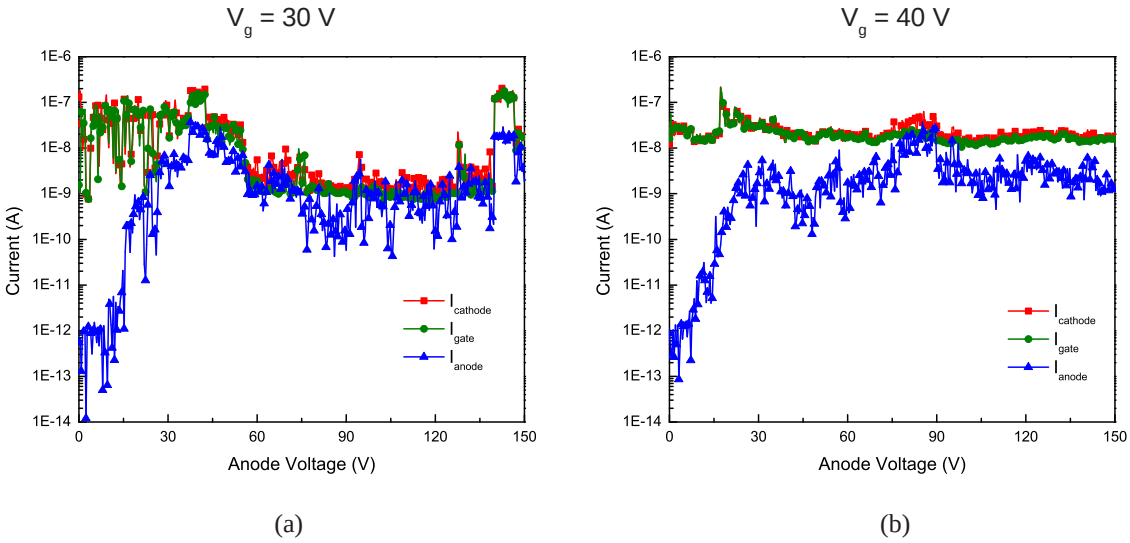
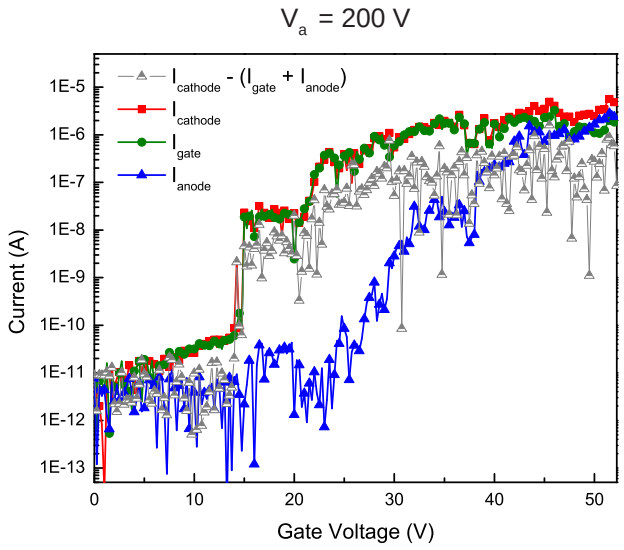
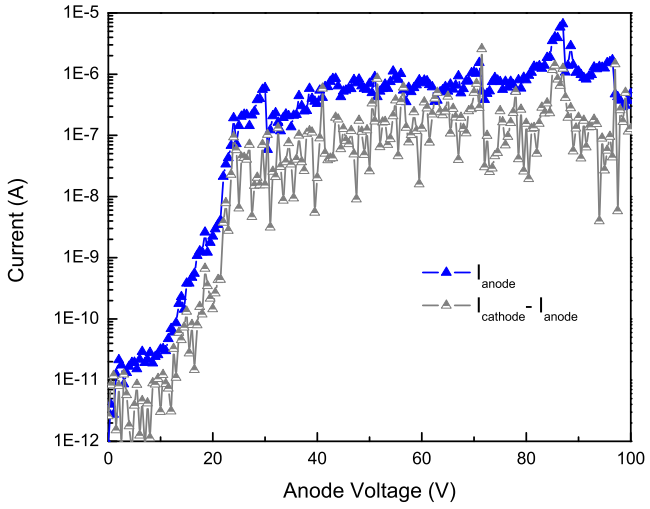


Figure 4.25: Output characteristics for a triode array with 1042 nm thick SiO_2 for V_g equal to (a) 30 V and (b) 40 V.



(a)



(b)

Figure 4.26: (a) I-V characteristics for triode arrays, under ideal vacuum conditions, showing additional component of current from the cathode that is not seen at the gate or anode electrodes. This illustrates that some fraction of electrons are not intercepted by the gate, but also do not reach the anode. (b) I-V characteristics for diode arrays, under ideal vacuum conditions, with additional component of current from the cathode that is not seen at the anode electrode.

Output characteristics

Fig. 4.24 is a plot of the output characteristics for a 32x32 device array with 822 nm thick SiO_2. For $V_g = 40$ V, as the anode voltage increases, fewer electrons are intercepted by the gate. Because we have confirmed that the anode voltage does not influence electron extraction from the tip, the increase in anode current for a constant gate voltage indicates that the trajectory of the electrons after transmission through the graphene is impacted by the anode voltage. As the gate voltage increases from 40 V to 50 V, the initial gate current increases from just under 1 μA to 5 μA. The anode current initially increases rapidly, suggesting that many of the higher energy electrons are being collected at the anode. However, there is a rapid drop in the anode current around 45 V, suggesting another possible breakdown event. Thus, the optimal amount of anode current is achieved at the lower gate voltage.

Fig. 4.25 is a plot of the output characteristics for another device with the same physical parameters. In this case, as the gate voltage increases from 30 V to 40 V, both the gate and anode currents are sustained for a longer period of time in a more stable manner, but without a significant increase in magnitude as the gate voltage increases. The anode current does reach a magnitude comparable to the gate current, indicating the potential for current gain at specific bias points with further device optimization. In both cases, operating the device at a lower gate voltage results in higher anode current, suggesting that there is an optimal gate voltage at which electrons pass through the graphene without being captured at the gate.

Although fairly low anode voltage must be applied to begin collecting electrons at the anode ($V_a > 30$ V is sufficient), a fairly large anode voltage is required to observe current gain, as the trajectory of the electrons after emission is influenced by the anode voltage. In the case of Fig. 4.24, $V_a > 120$ V must be applied to measure anode current comparable in magnitude to the gate current. Fig. 4.25 indicates that $V_a > 60$ V is sufficient. The analysis of current losses demonstrate that high anode voltages reduce current losses to other parts of the setup.

Overall, data from the triode configuration confirm that utilizing the graphene membrane as a gate electrode allows a subset of electrons emitted from the cathode to travel to the region outside of the vacuum-sealed cavity. Ultimately, this property is critical in enabling the use of this device structure as a portable electron source.

4.3.4 In-air extraction of electrons

The measurements thus far validate the proposed concept for using a graphene membrane with a field emitter cathode to build a portable electron source. A multitude of applications for this device structure arise from its ability to utilize the electron source in non-vacuum ambients. As a final experiment, the devices are tested in the triode configuration outside of vacuum. For this test, the devices are pumped down at 10^{-6} Torr for $\sim$48 hours to achieve vacuum in the cavities. After, the devices are biased per the configuration shown in Fig. 4.27 and measured in air, rather than vacuum.

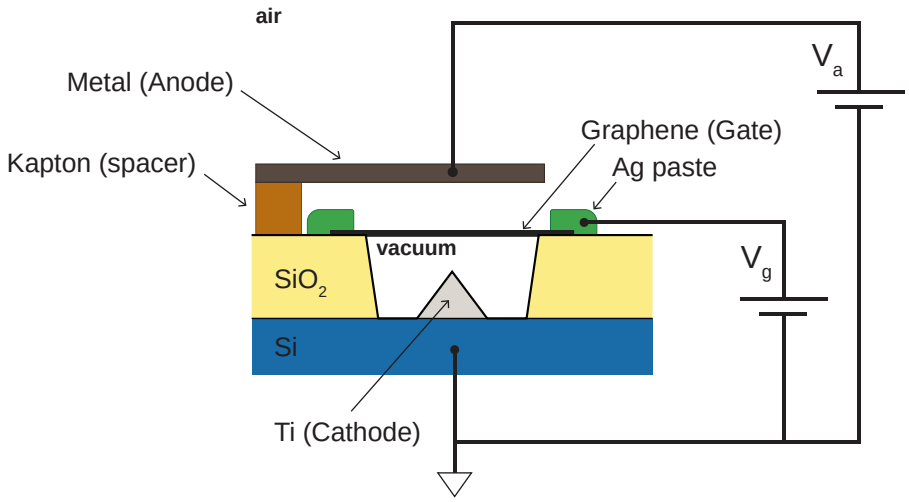


Figure 4.27: Test setup for triode configuration for devices tested in air after vacuum pump-down.

Fig. 4.28 plots the transfer characteristics for a 32x32 device array with 1041 nm thick SiO_2. The most salient feature of this plot is the detection of anode current at ~100V, demonstrating that some number of electrons emitting from the cathode are collected at the anode even in air. Given that the mean free path of electrons in air is on the order of 1 μm [91], the detection of anode current at a distance of 100 μm away from the extraction region suggests that additional processes are occurring in the air gap that contribute to the anode current.

One possible theory is that gas ionization is occurring in the gap. Fig. 4.29 shows the possible regions that may be represented in the plot, according to gas ionization theory, with schematic illustrations presented in Fig. 4.30. These additional regions include an ionization region, a proportional region or Townsend avalanche, a limited proportional region and Geiger-Müller region [92], [93]. The ionization region occurs as the gate voltage is increased initially, causing electron emission and subsequent ionization. Due to the large mean free path of electrons in air, these primary electrons are unable to reach the anode. As the gate voltage continues to increase, the electrons are emitted at higher energies and accelerated by the electric field in the air gap, causing them to collide with gas molecules and free additional electrons. The additional electrons are also accelerated by the field and free more electrons, resulting in an avalanche multiplication process referred to as Townsend avalanche and annotated as the proportional region. The rapid multiplication of electrons in this region enables electrical conduction through the air, resulting in the rapid onset of anode current. As more and more electrons are freed and accelerated, ionization of the gas molecules also

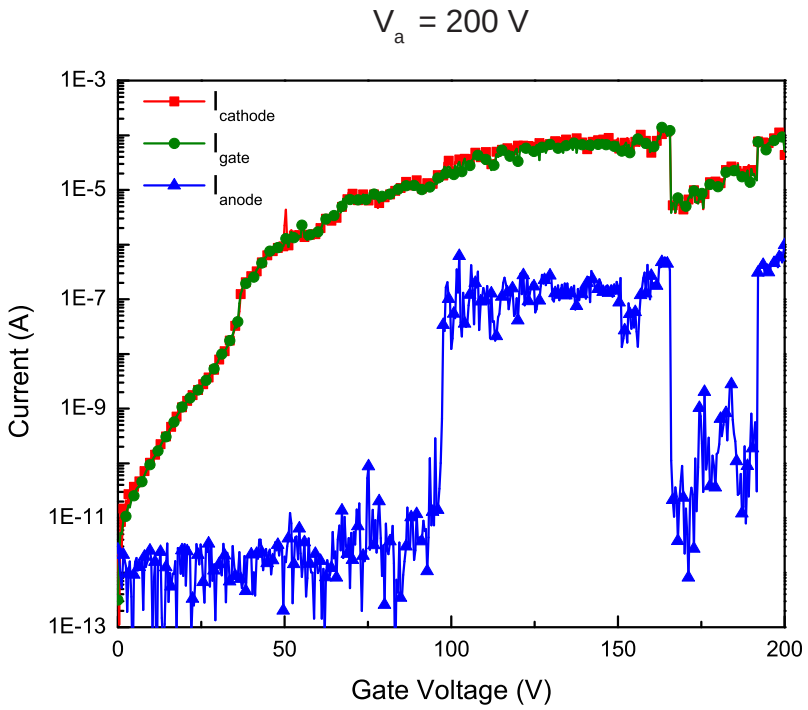


Figure 4.28: Transfer characteristics for triode array measured in air after vacuum pump-down, illustrating in-air extraction of electrons.

occurs.

As the voltage is increased further, additional electrons are freed at higher energies, resulting in increased ionization and the spread of the Townsend avalanche along the anode. Due to the positive polarity at both the gate and anode electrodes, however, the ions remain in the air gap, impacting the electric field seen by the electrons. In addition, the applied field between the anode and gate decreases as the gate voltage increases, since the anode voltage remains constant. The amplification process begins to saturate and the number of electrons collected at the anode saturates. Based on previous measurements with these tips, saturation is also attributed to limitations in the cathode material. At ∼160 V, a drop in the gate current is observed, likely due to a potential breakdown event or emitter rupture; this causes a subsequent drop in the anode current, confirming that anode current is due to electron emission from the cathode.

Comparing transfer plots for the triode configuration in air and vacuum, it can be seen that minimal anode voltage is required to collect electrons in vacuum, but a high voltage is needed to collect electrons in air. This is again attributed to the difference in electron mean

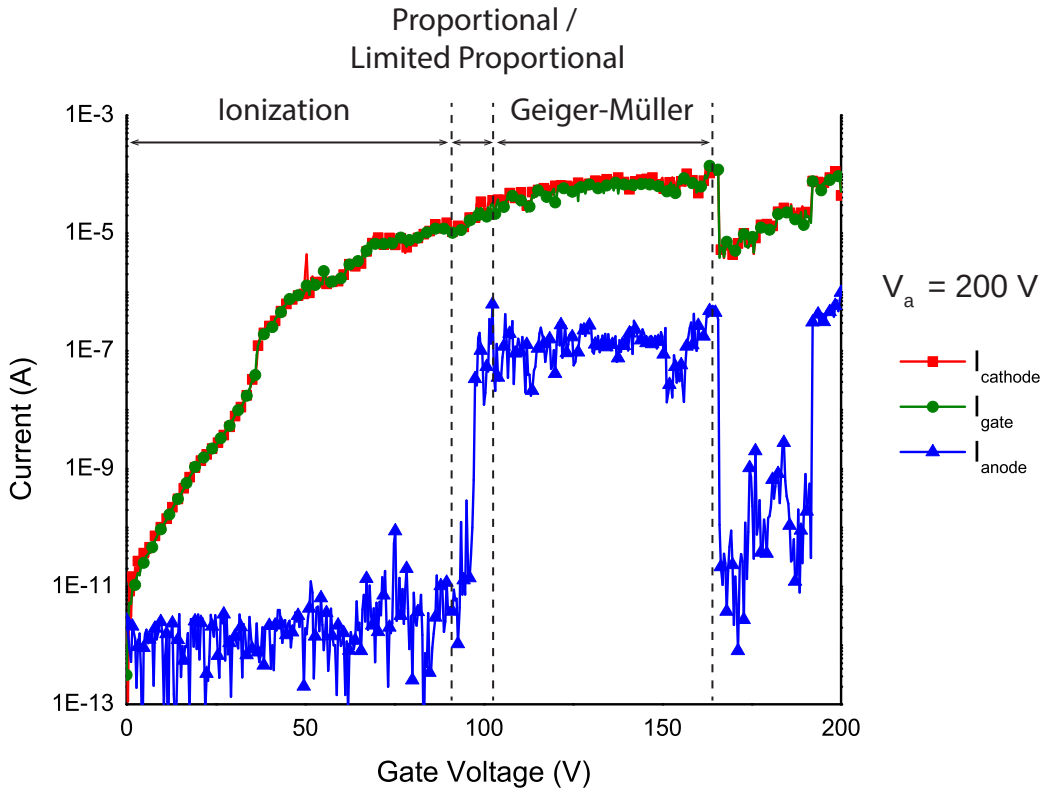


Figure 4.29: Transfer characteristics for triode measurement in air, with gas ionization regions annotated.

free paths in air and vacuum as well as the likely occurrence of gas ionization processes in air, resulting in differences in device operation. The gate current measured in air is also higher than the gate current measured for the same devices tested in vacuum, indicating that there may be a source of leakage contributing to the gate current detected in air. The application of 200 V across the gate and anode electrodes, with the cathode floating, results in no current detected at either electrode, eliminating the possibility of leakage between the gate and anode that may be contributing to either the gate or anode current. No leakage also confirms that the anode current is a result of electron emission processes from the cathode tip, rather than another source. Therefore, the high gate current is attributed to leakage between the cathode and gate, that may be a result of issues with the fabrication and transfer process.

To the best of our knowledge, this is the first demonstration of in-air extraction of electrons using a device structure consisting of a field emission source sealed by a suspended

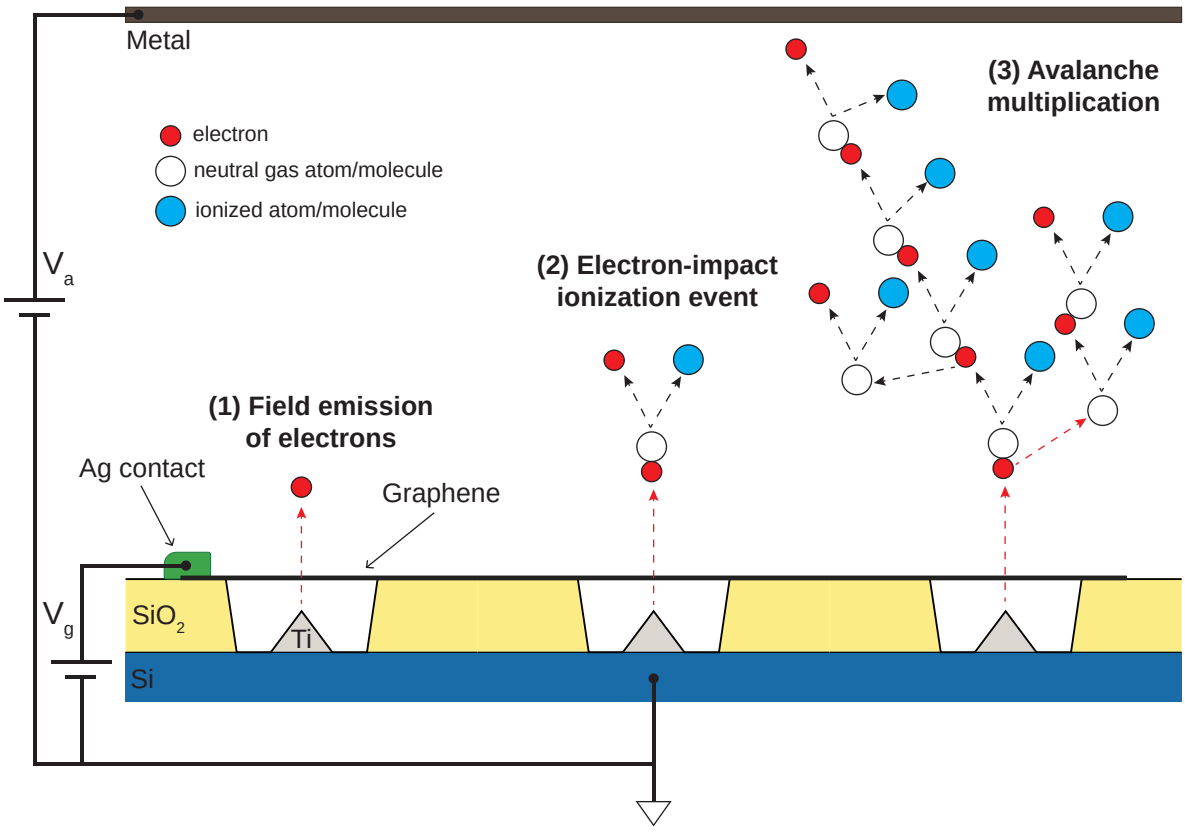


Figure 4.30: Illustration of processes occurring in the triode air measurement. First, field emission of electrons occurs, shown in (1), followed by ionization events caused by electron impact, as shown in (2). As the gate voltage increases, additional electrons are emitted and both primary and secondary electrons continue to cause ionization events, creating an avalanche multiplication of electrons that enables electrical conduction through the air.

graphene membrane that acts an electron-transparent extraction electrode.

4.3.5 Design guidelines

Below is a summary of the key findings from extensive device characterization that should be considered in future device designs:

1. Graphene is an effective electron extraction electrode that can be used to enable low-voltage operation. The devices tested in this work demonstrate threshold voltages as low as 3 V. By altering parameters such as the aperture size and SiO_2 thickness, the distance between the emitter tip and graphene membrane can be altered to tune the threshold voltage. This is critical for applications such as microrobotics, in which low-voltage operation is desired.

2. Graphene is an effective vacuum seal that results in improved field emission performance as the level of vacuum in the cavity increases. A method for cavity pumpdown is essential unless the graphene transfer process can be modified to be done in vacuum.

3. Graphene membranes deflect on the order of tens of nanometers as a result of pressure differences across the membrane, with the membrane becoming flatter and moving closer to the cavity as the level of vacuum in the cavity increases. The deflection affects the inter-electrode gap, or the distance between the emitter tip and gate, which has impacts on threshold voltage and device performance.

4. Graphene is a highly efficient gate electrode that demonstrate the potential for both high current gain and high power gain. As additional electrons are extracted from the cathode by applying higher gate voltages, a larger fraction are collected at the anode rather than the gate. This reduces gate losses and increase output current, resulting in current gain. Despite the large inter-electrode distance between the anode and gate in the configuration tested here, both current and power gain are observed. Thus, the use of graphene as a gate, rather than metals as in conventional triodes, could result in devices with much higher efficiency and gain.

5. Graphene is transparent to electrons with energy levels corresponding to the gate voltages used for the devices studied in this work. Further study on the transparency of graphene to a wider range of electron energies is essential if the transparency property is to be utilized for applications outside of the bias points used in this work.

The following are important areas to improve in future device designs:

1. Cathode material: As discussed previously, the current and reliability of the devices are limited by the Ti tip and can be significantly improved through the use of more robust, high-performing field emitter materials, such as CNTs. Instabilities due to the cathode material manifest in rapid drops in current seen in the device plots.

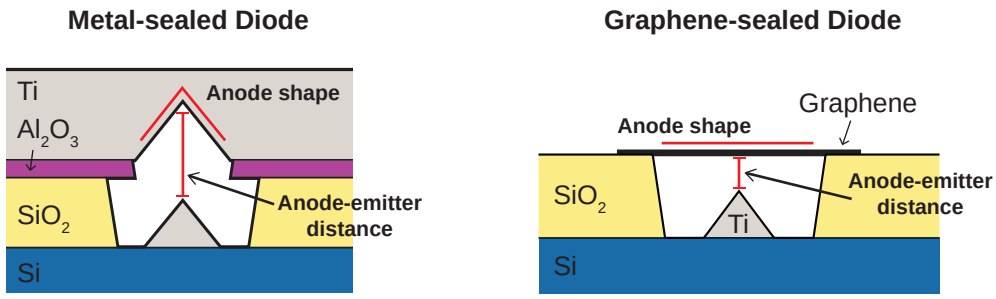


Figure 4.31: Schematic illustrations of the two diode geometries presented in this work, with key differences annotated. The metal-sealed diode is shown in (a) and the graphene-sealed diode is shown in (b). The key differences between these two device architectures are the anode shape and material as well as the inter-electrode distance between the anode and cathode.

2. Optimization of the graphene preparation and transfer process: Although a tri-layer graphene stack is utilized in this work, further optimization should enable transfer of monolayer graphene. This would simplify the fabrication process and reduce device variation, leading to more consistent device performance.

3. Surface cleanliness: Roughness in the AFM profile indicates that cleanliness can be improved. For this work, all of the steps outside of cathode fabrication are not performed in a cleanroom. Through additional sample cleaning steps as well as fabrication in a cleanroom environment, fewer surface impurities should be seen.

4. Long-term vacuum-sealing technique: For long-term device operation outside of vacuum, vacuum must be maintained in the cavity housing the field emitters. Given that the transfer process is done in air, the devices must be pumped down in vacuum and then sealed with another material in the area with SiO_2 not covered by graphene. One solution would be to evaporate alumina on the exposed SiO_2 areas, based on previous findings that alumina is an effective vacuum seal.

4.3.6 Comparison to metal-sealed field emission arrays

The use of the same cathode with different electrode materials and geometries presents a unique opportunity to discuss differences in device performance that can be attributed to physical differences in the rest of the device geometry. Fig. 4.31 highlights the geometrical

Table 4.2: Metal vs. Graphene in Diode Configuration

	Metal-sealed Devices	**Graphene-sealed Devices**
Anode shape	Concave	Planar
Anode material	Ti	Graphene
Minimum anode-cathode distance	297.7 nm*	81.2 nm**

Measurements done on 32x32 arrays with 800 nm aperture sizes.
*SiO_2 thickness of 714 nm.
**SiO_2 thickness of 822 nm. Assumes graphene membrane deflects downward by 40 nm. Corresponding values for 914 nm and 1041 nm SiO_2 thickness are 131.2 nm and 236.2 nm.

differences between the two diode devices studied in this work, with the metal-sealed diodes annotated in (a) and the graphene-sealed diodes annotated in (b). Details on device materials and dimensions are provided in Table 4.2. For the metal-sealed device, the Ti anode has a curved shape that results in a much larger anode-cathode gap than that of the graphene-sealed device, which is far more planar in comparison despite the deflection induced in the membrane. Because of this, lower threshold voltages are observed for the graphene-sealed devices (as low as 8 V) than for the metal-sealed diodes (on the order of 80 V) for comparable SiO_2 thicknesses. This results in higher currents at lower voltages. The average current / tip is also higher in the graphene device, as estimated from the data ($\sim$1 nA / tip versus 70 pA / tip). These improvements in device performance indicate that the graphene electrode and planar geometry extracts electrons from the cathode much more efficiently than the curved metal electrode.

Fig. 4.32 highlights the differences between the two triode devices studied here, with the metal-sealed triodes shown in (a) and the graphene-sealed triodes shown in (b). Details on device materials and dimensions are provided in Table 4.3. The first key difference is in the anode shape, anode material and anode-gate distance. The metal-sealed device uses a curved anode made of Ti and has a fairly small anode-gate distance of 350 nm, separated by thermally deposited low-temperature oxide. In contrast, the graphene-sealed triode uses a planar stainless steel anode separated by a polyimide film with a very large anode-gate gap of 100 μm. The gap for the graphene-sealed triode is two orders of magnitude larger than the gap in the metal-sealed triode. Because of this, the bias applied to the stainless steel anode has no impact on electron extraction from the cathode, as discussed in Section 4.3.3. Two-terminal tests applying 200 V across the anode and cathode for the graphene-sealed device results in no emission current. In contrast, the anode has a significant impact on device performance in the metal-sealed diodes; two-terminal tests applying 200 V across the anode and cathode for this device do result in field emission. These effects are likened to short-channel effects in MOSFETs and are critical to take into account when designing devices with closely spaced electrodes.

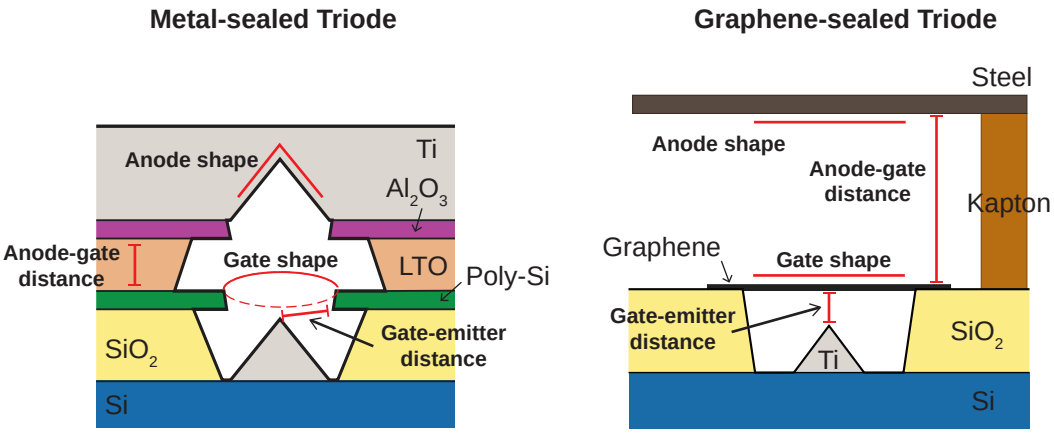


Figure 4.32: Schematic illustrations of the two triode geometries presented in this work, with key differences annotated. The metal-sealed triode is shown in (a) and the graphene-sealed triode is shown in (b).

Table 4.3: Metal vs. Graphene in Triode Configuration

	Metal-sealed Devices	**Graphene-sealed Devices**
Anode shape	Concave	Planar
Anode material	Ti	Stainless steel
Minimum anode-gate distance	490 nm	100 μm
Anode-gate spacer material	LTO	Polyimide
Gate shape	Circular ring	Planar
Gate material	Doped Poly-silicon	Graphene
Minimum gate-cathode distance	650.8 nm*	236.2 nm**

Measurements done on 32x32 arrays with 800 nm aperture sizes.
*SiO_2 thickness of 1 μm
**SiO_2 thickness of 1041 nm. Assumes graphene membrane deflects downward by 40 nm. Corresponding values for 822 nm and 914 nm SiO_2 thickness are 81.2 nm and 131.2 nm.

The gate geometries and materials are also different for these two devices. In the metal-sealed triode, the poly-silicon gate forms a ring around the edges of the cavity to surround the emitter; the minimum physical distance between the gate and cathode is ∼651 nm. In contrast, the graphene-sealed triode uses the graphene membrane as the gate, with a minimum gate-cathode distance of ∼236 nm, for a device of similar SiO_2 thickness. The planar shape, and subsequently smaller gate-cathode separation, of the graphene membrane make it a much more efficient gate electrode, resulting in the same device performances achieved by the graphene-sealed diode: higher current at lower voltages, lower threshold voltages and overall higher current / tip extracted. For the triode devices, this results in current gain between the anode and gate, despite the large anode-gate separation. The transconductance values of the transfer plots for the graphene-sealed triode are also higher than those of the metal-sealed triodes.

In conclusion, the graphene membrane is an extremely efficient gate for the triode configuration, resulting in improvements in device performance. These results highlight that the gate electrode geometry and material are among the most critical components in such a device. Not only does a graphene gate enable operation outside of a vacuum environment, the geometry of the membrane and the properties of graphene make it a much more efficient gate in comparison to the ring-like geometry of the metal or doped poly-silicon gates used in traditional field emission triodes.

4.4 Conclusions

In this chapter, a process has been developed to integrate graphene with field emission arrays for a portable electron source. A discussion of the literature is provided to elucidate the fundamental motivation behind the use of graphene. Then, the fabrication process is discussed in detail, including cathode preparation, graphene preparation and graphene transfer. The final device structure consists of a fully integrated on-chip field-emission-based electron source utilizing a graphene gate electrode. Results from device characterization confirm that the graphene functions as a highly efficient gate electrode. The graphene is also an effective vacuum seal that is electron transparent, allowing the extracted electrons to be used outside of a high vacuum environment. The results presented here have significant implications in the use of graphene as an electron-transparent gate electrode and vacuum seal for a number of applications, particularly those that require operation in high pressure and various gases.

Table 4.4 lists examples of electron source applications, along with specific performance needs and future work recommendations. As can be seen from the table, the combined properties of high gate efficiency, vacuum-sealing and electron transparency unlock the use of graphene-gated field emission devices in a number of electron source applications that require operation in non-ideal conditions. Coupled with a field emission source that is capable of low-voltage, room temperature operation, miniaturization and on-chip integration becomes feasible.

For the triode applications discussed in Section 3.5, the replacement of the doped polysilicon gate with a graphene membrane can improve gate efficiency and overall device performance. As we have seen in this chapter, current gain and output currents comparable to those of the metal-sealed triodes is obtained despite a much larger inter-electrode gap, suggesting inherently better device performance is possible with the graphene-sealed triodes.

Beyond the application-specific future work recommendations listed in Table 4.4, additional scientific study is essential to understand the fundamental physics enabling the observed device performance. Potential areas of further study include understanding the transparency of graphene to electrons at various energy levels, the impact of graphene layer thickness on transparency and the robustness of the graphene membrane to continuous electron transmission.

Table 4.4: Portable Electron Source Applications and Future Work Recommendations

Application	**Type of Electron Source Required**	**Performance Needs**	**Operating Conditions**	**Future Work Recommendations**
MEMS microrobotics / micro-air vehicles [47]	Ion thruster	Low turn-on voltage (<5V), low operating voltage, on-chip integration, low mass	Atmospheric pressure, air	Ultra-low voltage field emitters [39], optimize inter-electrode gap, long-term sealing
Hall thruster, ion engine [21]	Space charge neutralizer	High-density electron beam	Low-pressure O_2, high pressure reactive gases	High-current field emitters
Portable mass spectrometer [36], [37]	Electron-impact ion source	High-density electron beam, portability	High pressure, various gases	High-current field emitters, long-term sealing
Handheld x-ray spectrometer [20], [38]	Mini x-ray source	High operating voltage (kV), transparency to high energy electrons, high-density electron beam (mA), high beam focusing, portability	Atmospheric pressure, air	Sidewall fortification, study of keV electron transparency, high-current field emitters, long-term sealing
Environmental microscopy / spectroscopy [84], [85]	High voltage electron source	High operating voltage (kV), transparency to high energy electrons, high beam focusing	Atmospheric pressure, air	Sidewall fortification, study of keV electron transparency

Chapter 5

Conclusions

5.1 Summary

In this work, two different device architectures for fully integrated vacuum-sealed field emission arrays have been designed, developed and characterized, with a focus on specific applications in which vacuum-based devices offer unique performance advantages or new functionalities. The studies and results presented here are:

- The design, fabrication and characterization of vacuum-sealed fully integrated diode field emission arrays, consisting of Ti Spindt-type emitters and a Ti anode. The arrays are fabricated in a simple, scalable process integrated directly on Si and demonstrate both field emission and effective vacuum-sealing. The high operating voltages and low currents observed for the Ti Spindt-type emitters used in this work meet the performance needs of several MEMS applications, including drive circuits for electrostatic and piezoelectric actuators, micro-robotics systems and micro-air vehicles.

- The design, fabrication and characterization of vacuum-sealed fully integrated triode field emission arrays. The device geometry is similar to that of the diode arrays described above, with an additional integrated poly-silicon gate. The arrays demonstrate gate-modulated field emission at high voltages, enabling their use as a three-terminal switch in high voltage applications. With additional modifications, such as sidewall fortification and use of high current field emitters, the triodes can be used for high power applications. This is the first demonstration of on-chip vacuum-sealed triodes that outline a viable path towards the use of vacuum devices for Si integrated high voltage applications.

- The design, fabrication and characterization of an on-chip portable electron source, consisting of graphene-gated field emission arrays. A novel process is developed and optimized to directly transfer the graphene onto SiO_2 chips containing Ti Spindt-type emitters. Device characterization demonstrates that the graphene simultaneously

serves as a highly efficient electron extraction electrode and electron-transparent atmospheric seal that enables the use of these devices outside of a high-vacuum environment. This is the first demonstration of a graphene-sealed field emission device integrated directly on Si, with the potential for in-air extraction of electrons. The capabilities presented here indicate a path towards the development of a high-performance on-chip electron source utilizing novel nanomaterials.

- The use of CMOS and MEMS-compatible fabrication techniques and substrates in the development of novel vacuum microelectronic devices. In doing so, the results in this work demonstrate a unique opportunity to utilize vacuum microelectronic devices alongside today's integrated circuit technologies, taking advantage of the unique performance advantages offered by vacuum-based devices. Vacuum-based devices are particularly robust for high voltage and high power applications, as well as operation in harsh environments, ranging from extreme temperatures and pressures to extremely high radiation. Ultimately, we view the results presented in this work as a foundation for further study on the design and development of vacuum microelectronic devices that are monolithically integrated on Si.

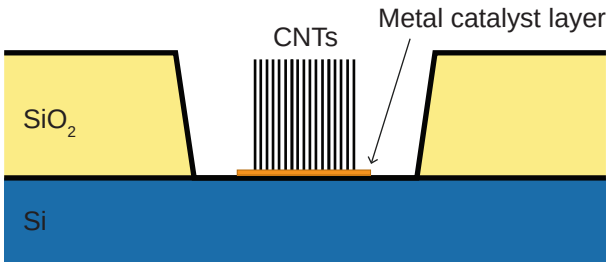
5.2 Recommendations for future work

This work explores the design and application of on-chip field emission devices, setting a foundation for the additional work required to realize the full potential of vacuum microelectronics in existing and future applications. Recommended areas of further work can be divided into areas of applied research, with a focus on device engineering and optimization, as well as basic research, with a focus on further fundamental understanding of the underlying physics driving the performance of the devices.

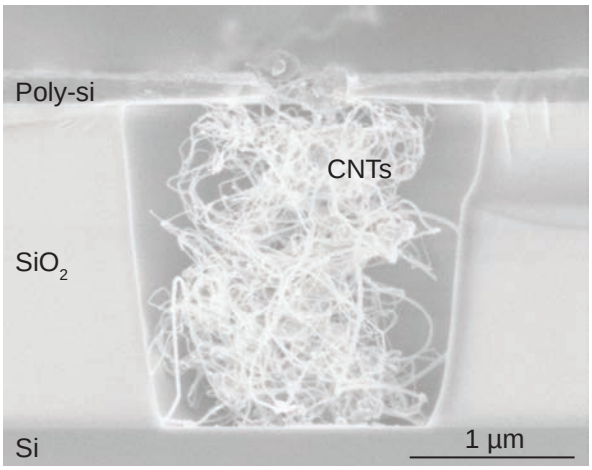
5.2.1 Applied research

Areas of further study focused on improving device performance for specific applications include:

- Integration of high-performance field emitters –The low currents from the Ti Spindt-type emitters used in this work are not suitable for high current applications. Instead, integration of high-performance field emitters is desirable. One approach is to use carbon nanotubes (CNTs). Fig. 5.1(a) is a schematic illustration of the target device geometry and Fig. 5.1(b) is a cross-sectional SEM of CNTs grown in SiO_2 cavities with an integrated poly-silicon gate. Further process optimization is needed to ensure CNTs with sub-micron heights can be grown in a controllable manner, if device dimensions similar to the Spindt diodes and triodes in this work are desired.



(a)



(b)

Figure 5.1: (a) Schematic illustration of CNTs integrated in SiO_2 cavities. (b) Cross-sectional SEM of CNT forest grown in SiO_2 cavity with integrated poly-silicon gate, using a 5 nm Fe catalyst layer.

- 'Short-channel'effects in fully integrated vacuum microelectronics –All of the devices in this work are fully integrated on Si, with all electrodes on the same substrate. Results from characterization show that close inter-electrode spacings (on the order of micrometers) impact device performance in ways that have not been observed with non-integrated configurations. Because monolithic integration is required to enable widespread use, particularly for CMOS and MEMS applications, further study on 'short-channel'effects in fully integrated field emission devices is critical.

- Impact of novel nanomaterials on device performance –Novel nanomaterials, such as CNTs and graphene, exhibit properties atypical of standard materials used in early solid-state devices. Careful study of how these materials behave and their impact on key device performance metrics, such as threshold voltage, current density, gain and field emission, will be critical given that hybrid devices offer extremely attractive opportunities for the development of devices with new functionalities, unlocking a plethora of new applications in electronics.

- Development of long-term sealing techniques –Areas of SiO_2 exposed to air in the device geometries in this work result in loss of vacuum-sealing internal to the cavities. Processes must be developed to integrate materials, such as alumina, into the fabrication process such that the vacuum-sealing in the cavities is maintained.

- Robustness of graphene membrane as a vacuum seal –The results here demonstrate the ability to use graphene as an atmospheric seal. Additional work on the robustness of the seal to continuous device operation and electron transmission is important to elucidate device lifetimes when using graphene in this manner.

- Performance in extreme environments –The low temperature measurements presented in this work are one of many extreme operating conditions that can be handled by vacuum microelectronic devices. In order to enable new functionalities for electronic circuits made possible by the use of vacuum-based devices, experiments validating device performance in extreme temperatures, pressures and high radiation environments is critical. These studies will indicate the range of applications in which vacuum-based devices can be used, particularly ones that are not suitable for semiconductor-based integrated circuits.

- System-level / circuit implementations –The devices here indicate some of the new and interesting performance advantages that can achieved by on-chip vacuum microelectronics. To explore this area further, system-level demonstrations of integrated circuits created with these components must be done. Examples include developing a buck or boost converter using high voltage field emission arrays, high temperature (600 °C) wireless sensors, and radiation hard electronic circuits.

5.2.2 Basic research

In addition to research focused on device engineering and optimization for specific application needs, there are several interesting areas of fundamental research:

- Electron transparency of graphene at various energy levels –This work confirms that graphene, observed to be mostly monolayer, is transparent to electrons emitting from field emitters at extraction voltages as high as 100 V. However, more careful study is required to clearly understand how and why the transparency changes for different electron energies, with only a few reports existing in the literature today. Such studies should include impacts of graphene layer thickness on electron transparency, as these findings may inform device fabrication and process techniques.

- Spatial distribution of field emission of electrons in large-area array –By replacing the metal anode in the graphene-sealed triode configuration with a phosphor anode, which can emits photons upon electron-impact, the spatial distribution of the field emitters in the array can be visualized. This is important for understanding variation in tip performance for large-area arrays. Focusing efficiency as a function of parameters such as graphene membrane thickness, transfer technique and inter-electrode distance can also be studied in this setup.

- Energy distribution of field emission of electrons in large-area array –A more detailed understanding of the energy levels of the field emitted electrons and their relation to extraction voltage is needed. One way to do this is to measure the energy of emission from the graphene-sealed diode in a low-energy electron microscope (LEEM), which can detect energies ranging from 1-100 eV. This requires modification of the standard LEEM setup to enable emission of electrons from the field emitters, rather than an external electron source. Similar setups have been used for ev-TEM measurements, in which an ion gauge filament is used as the electron source and low energy electron transmission through graphene is measured [94].

Further study in these areas will not only elucidate how to leverage these materials to enable new functionalities, but could also reveal new interesting properties.

In summary, the results of this dissertation show that field emission devices can be effectively used alongside solid-state technology to not only address the limitations faced by solid-state devices, but also enable entirely new applications in electronics. By designing and developing field emission devices for integration and use in CMOS and MEMS technologies, the unique performance advantages of vacuum microelectronics can be leveraged effectively. Though much of the literature on field emission devices has focused on the basic science of field emission, this work also emphasizes importance of an engineering perspective on the development of field emission devices. Such work is what will ultimately enable widespread use of vacuum microelectronics in today's technologies. Ultimately, by leveraging the best features of field emission devices and solid-state microfabrication techniques, we believe significant advancement can be made in a variety of applications.

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