Circuits and Systems for Decentralized Power Conversion

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Circuits and Systems for Decentralized Power Conversion

by

Jason Poon

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Committee in charge:

Professor Seth R. Sanders, Chair
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Abstract

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This dissertation explores circuit, control, and optimization techniques for power electronics with the objective of enabling high performance electric networks for a variety of important applications. The motivation for this work is driven in part by societal-scale trends towards systems that are increasingly dominated by power electronics, including applications such as renewable energy integration, vehicle electrification, power management for mobile devices, and data center power delivery. A key approach demonstrated in this dissertation is the design of switching power converter circuits that naturally coordinate with larger networks in order to achieve system-level benefits, whether with respect to efficiency, power quality, or reliability. A central goal of this work is to have this coordination realized in a decentralized or autonomous fashion, such that scalability, modularity, and resiliency can be achieved inherently. In the first part of this dissertation, we explore techniques for improving the power quality of electric networks with high penetrations of switching power converters, in particular, techniques that can minimize aggregate power converter harmonics in an optimal sense while also eliminating the need for communication between distributed converters. In the second part of this dissertation, we explore methods for improving the reliability and fault tolerance of such networks, in particular, model- and estimation-based strategies that transform power converters into active probes that can detect, identify, and diagnose faults in real-time. Together, these contributions demonstrate how power electronics can be designed and collectively controlled and optimized to enable highly efficient, robust, and resilient electric networks.

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Chapter 1

Introduction

This dissertation presents contributions in power electronics circuits and systems that facilitate more efficient, reliable, and decentralized power conversion.

Power electronics regulate and transform the flow of electrical energy. For many applications, power electronics enable systems with greater efficiency and performance compared with those that have passive electrical sources or loads. Consider, for instance, the lighting application illustrated in Fig. 1.1. For many decades, incandescent light bulbs have been ubiquitous in consumer lighting, with a 60 W light bulb being a de facto standard in households in the United States. An incandescent light bulb consists of a thin filament of wire, essentially a resistor (i.e. a passive load), that produces light when electricity is passed through it. Such a light bulb can produce light with virtually any form of electricity, whether ac or dc, since power will be dissipated by the filament regardless. Therefore, incandescent light bulbs can be directly connected to the 60 Hz ac grid without the need for a power conversion device. A key drawback of incandescent lighting, however, is efficiency. Since these light bulbs are essentially resistors, in addition to producing light, heat is produced as a byproduct. To quantify this inefficiency, consider an alternative lighting product based on light-emitting diodes (LEDs), e.g. [1]. These LED products can produce the same amount of light as an incandescent light bulb (often marketed as a 60 watt equivalent), but consume an order-of-magnitude less power, often in the range of five to ten watts. Unlike an incandescent light bulb, LEDs require a precisely regulated current at low voltage, typically in the range of 1.8 and 3.3 Vdc, in order to operate. Similarly, many commercial applications utilize multiple LEDs in series that require a precisely regulated current with a string voltage in the range of 12 to 80 V. Therefore, in order to connect to the 60 Hz ac grid, a power conversion

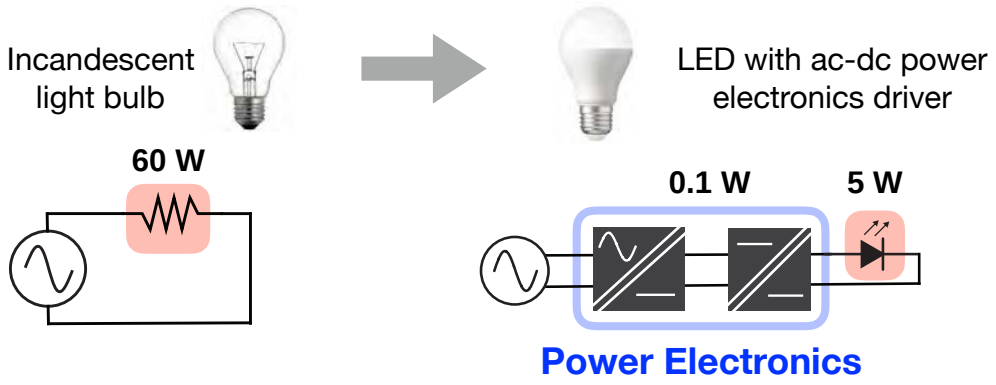


Figure 1.1: An incandescent light bulb (left) produces the same amount of light as a light-emitting diode (LED) (right), but requires an order-of-magnitude more power. However, LEDs, unlike incandescent light bulbs, require power electronics in order for a precisely regualted voltage and current.

stage is needed that will 1) rectify the ac voltage from the grid into a dc quantity, and 2) down convert this dc voltage to the low dc voltage range required by the LED. Supported by extensive research and development and government subsidies that have helped manufacturers scale the technology, LEDs and their requisite power conversion components, circa 2010, have largely reached capital cost parity with incandescent light bulbs. In 2020, LEDs are expected to comprise approximately 61 percent of the global lighting market (consumer, industrial, retail) with a continuing upward trend expected in the years that follow [2].

The LED market is an illustrative example of how power electronics can enable new technologies and new markets that are higher performing, have higher efficiency, and offer greater functionality to end users. Beyond the LED market, other example industries where power electronics have offered benefits are in large-scale renewable energy integration [3], net-zero and net-positive energy buildings [4] (e.g. Fig. 1.2), data center power delivery [5], and power management for mobile devices [6]. The transformative impact of power electronics is evident in a 2005 Oak Ridge National Lab prediction that by 2030, 80 percent of all electrical power will be processed at least once by a power electronics device [7].

However, the proliferation of power electronics into many of these applications can produce detrimental effects as well. In particular, such devices can introduce new challenges with respect to the high frequency harmonics and associated stability issues that originate from their inherent switching and non-linear dynamical behavior. These challenges are exacerbated as networks scale organically and need to accommodate increasingly greater amounts of power converter-interfaced electrical sources and loads.

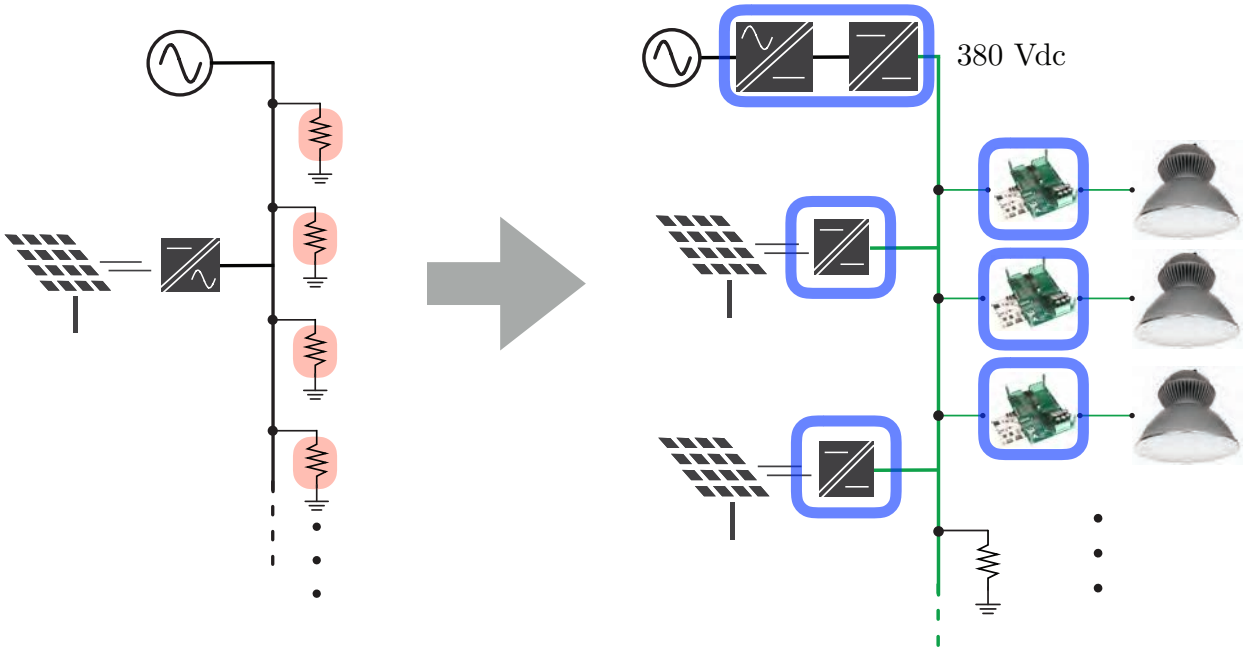


Figure 1.2: Illustration of the evolution of power distribution networks from relatively passive networks (left) to networks that are dominated with power conversion devices for both electrical sources and loads (right).

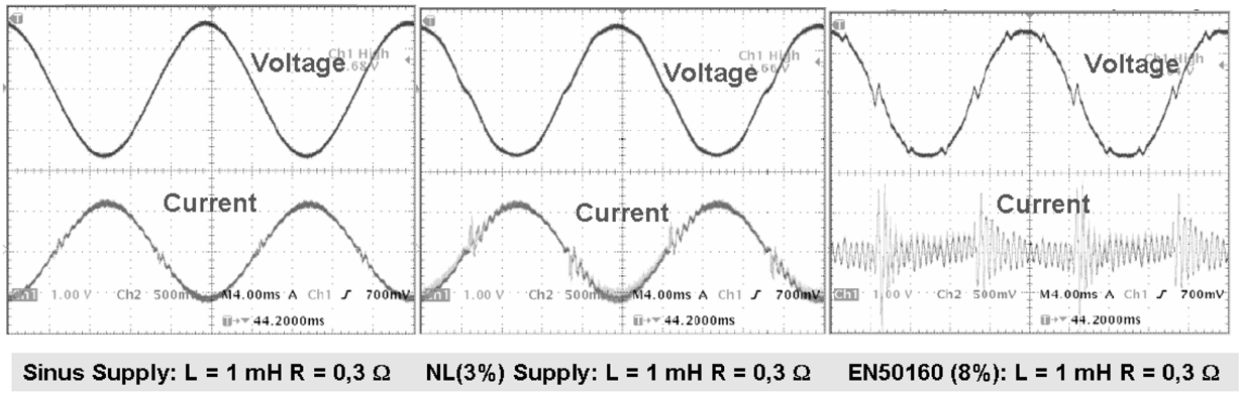


Figure 1.3: Result from [8] that explored the response of commercial photovoltaic (PV) inverters under typical levels of background voltage distortion that would be present on a distribution network.

As an example of these detrimental impacts, consider a study from [8] in which the authors explore the response of commercial photovoltaic (PV) inverters under typical levels of background voltage distortion that would be present on a distribution network. As shown in Fig. 1.3, the inverter was tested with a pure sinusoidal grid (left), a grid with distortion that would be considered average in the Netherlands (middle), and a grid with the maximum level of distortion allowed under European grid interconnection standard EN50160 (right).

Of note is that the inverter tripped and stopped working at distortion conditions that are still allowed under EN50160. This simple example highlights a need for new ways of handling the complexity of distributed and soon-to-be ubiquitous power electronics devices. Moreover, this need will become more critical with the increasing proliferation of electrical sources and loads that are interfaced through power electronics.

1.1 Primary Contributions

This dissertation approaches this broad space of problems from the following perspective:

Dissertation Statement — *By controlling and optimizing the collective dynamics of interconnected power electronics circuits, we can build electric networks that are more reliable, efficient, and stable with increasing device integration.*

The motivation for this approach is driven by the trend towards systems that are increasingly dominated by power electronics, including applications such as renewable energy integration, electrified transportation, power management for mobile devices, and data center power delivery. Conventionally, one may surmise that such systems will become more complex and exhibit greater instabilities due to higher penetration of switching power devices. However, we will show that the opposite can be true—that is, by coordinating the actions of distributed switching power converters, we can realize electric networks with greater performance and reliability.

Towards this end, the contributions of this dissertation can be discussed in two parts:

Contribution 1

The first contribution of this dissertation, presented in Part I, discusses new techniques for improving power quality through control. We will present techniques that optimally minimize aggregate harmonics of interconnected power converters, and can improve stability and reduce filtering requirements. Moreover, we will discuss decentralized control strategies that obviate the need for communication between distributed switching power converters. In particular, we will introduce *Minimum Distortion Point Tracking (MDPT)*: a control paradigm for series- or parallel-connected dc-dc converters where switching waveforms are optimally phase shifted to minimize the total dc-bus ripple power. Also, we will present the design and demonstration of a communication-free strategy for symmetric switch interleaving in parallel-connected dc-dc converters. Taken together, this contribution aims to demonstrate

practical methods of enhancing power quality for networks of power converters through the application of decentralized control and optimization.

Contribution 2

The second contribution of this dissertation, presented in Part II, discusses new strategies for fault diagnosis in large-scale power electronics systems in order to enhance reliability and fault tolerance. Specifically, we develop a class of algorithms that can classify faults in real-time, enabling greater situational awareness and prompt fault remedial actions. Moreover, we will demonstrate a series of fault prediction mechanisms which can provide metrics on the overall health of a power electronics system, and predict when faults are more likely to occur. These algorithms are executed locally at each power converter, and leverage the high-bandwidth sensing and computational capabilities available at each device. In this way, each power converter is not only self-monitoring, but can also probe the surrounding network for potential faults. The class of algorithms developed is flexible, computationally efficient, and precise in its ability to detect and classify faults of interest. Moreover, we will show how such techniques can be applied in a variety of emerging, high-impact applications in beneficial ways that improve system robustness.

1.2 Outline and Previously Published Work

The remainder of this dissertation proceeds as follows. Chapter 2 motivates the need for improving power quality through control, in particular, highlighting strategies that do not add to the cost, volume, or hardware complexity of an overall system design. Chapter 3 discusses a new technique for optimizing and controlling the dynamics of distributed, interconnected power converters in order to substantially minimize aggregate harmonics. Chapter 4 presents a decentralized control architecture that enables coordination between distributed power converters in the absence of communication; notably, the first demonstration of a fully decentralized strategy for symmetric pulse width modulation (PWM) interleaving is demonstrated. Chapter 5 motivates the need for robust fault diagnosis in a variety of emerging, high-impact applications. Chapter 6 discusses the modeling and estimation framework used in the proposed fault diagnosis strategies presented in Chapters 7 and 8. Chapter 7 discusses the analysis, design, and experimental validation of a novel model-based fault detection and identification (FDI) method for switching power converters using a model-based state estimator approach. Chapter 8 demonstrates a method for fault prognosis for power

electronics systems using an adaptive parameter identification approach. Chapter 9 concludes the dissertation with a discussion of lessons learned, directions for future research, and closing thoughts.

Chapter 2 summarizes and expands material from [9, 10]. Chapter 3 revises material from [9]. Chapter 4 revises material from [10, 11]. Chapters 5 and 6 summarize and expand material from [3, 12, 13]. Chapter 7 revises material from [12]. Chapter 8 revises material from [13].

Part I

Control Techniques for Improved Power Quality

Chapter 2

State-of-the-Art Techniques and Key Limitations

In this chapter, we discuss the motivation for improving power quality through control. First, we will discuss three applications that highlight ongoing and emerging needs to improve power quality in ways that do not add to the cost, volume, or hardware complexity of an overall system design. Next, we will review existing state-of-the-art techniques that are used to address these challenges and identify their limitations in meeting the requirements of many of these applications. This discussion will motivate the need for new techniques that are more robust and generalized that can provide enhanced power quality for a variety of high-impact applications.

2.1 Series- and Parallel-Connected Multistage Architectures

Many applications require power delivery that is scalable, tolerant to failure, and highly efficient. These applications range from small-scale systems in the range of milliwatts, such as mobile and Internet-of-Things (IoT) devices, to large-scale systems, such as high-voltage direct current (HVDC) transmission and renewable energy integration. Multistage parallel- and series-connected architectures are increasingly emerging as the norm in a variety of applications including (but not limited to): dc front-end converters in renewable energy systems and microgrids [14, 15, 16], voltage regulator modules [17, 18, 19], and power-factor correction circuits [20, 21]. Many compelling reasons underscore the widespread adoption of

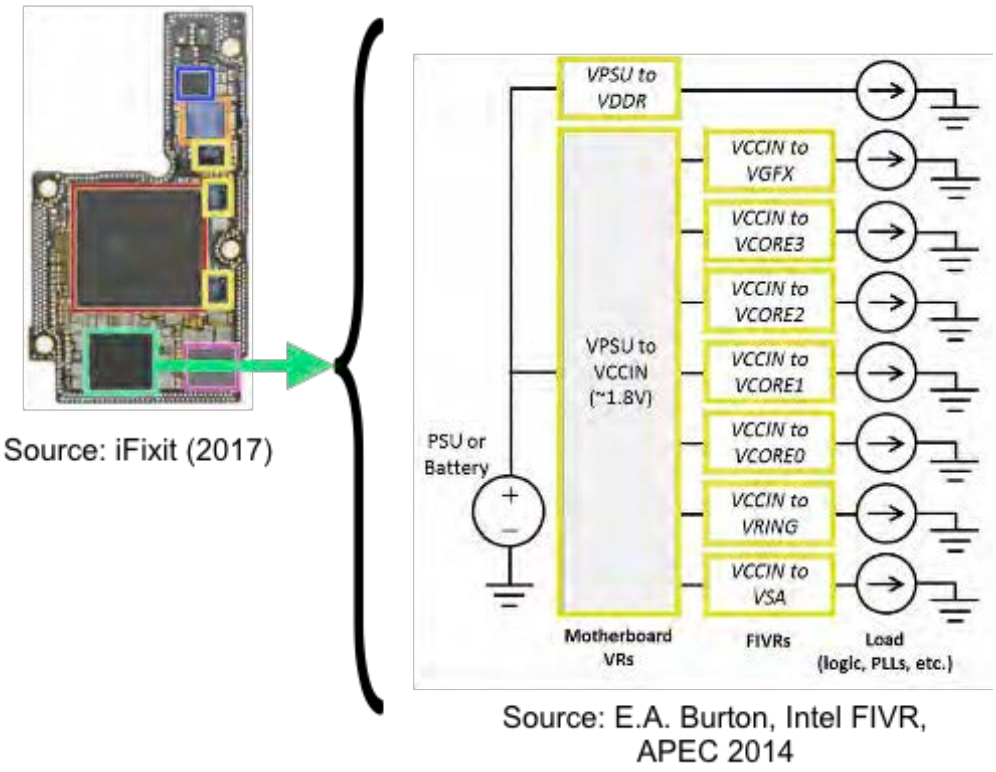


Figure 2.1: Illustration of an example power management integrated circuit within a mobile phone.

multistage converters including: cost (canceling ripple reduces the requirements for passive filters), reliability (bulk electrolytic capacitors used in filters can have lifetime issues particularly under high temperatures), modularity (the system can operate in a lower power mode with a reduced number of converters), power ratings (current-handling capacity of parallel systems is higher than an individual converter), and efficiency (converters can be turned on/off to minimize losses depending on the load to be served; this is commonly referred to as *phase shedding*). In this section, we will discuss three specific applications that highlight the various requirements, constraints, and emerging needs of series- and parallel-connected multistage architectures.

2.1.1 Power Management Integrated Circuits for Mobile Applications

The market for power management integrated circuits (PMIC) for mobile applications, such as phones, tablets, smart watches, and fitness devices, is predicted to exceed 58.4 billion

USD by 2026 [6]. PMIC devices are the power conversion chips used to process power from the battery of a device to produce the various voltage rails that will be used by various subsystems within the phone, such as the display, camera, application processor, sensors, and so on. An illustrative example architecture is demonstrated in Fig. 2.1, where the circuit board on the left highlights the primary PMIC in green, and the circuit diagram on the right highlights a candidate single-input, multiple-output power delivery architecture. As shown, multiple power converters are connected to the input (the battery), and each converter produces the required voltage for the end load.

As end-use applications demand longer battery life, smaller form factors, and higher performance, the associated PMICs for these devices need to be simultaneously highly efficient and miniaturized. In conventional PMICs, bypass and filtering capacitors can comprise a substantial portion of the size of the overall IC and board area. This capacitance is necessary for handling load and input transients, and also for attenuating the switching transients of each power converter. In many emerging applications, the number of end loads connected to a single input bus is dramatically increasing due to the integration of new sensors, subprocessors, and other devices that require regulated power. As such, the size of the PMIC package can comprise a large potion of the overall circuit board area, as shown in Fig. 2.1. Towards this end, circuit and control techniques for minimizing the size of the PMIC package while maintaining power quality and power integrity are active areas of research.

2.1.2 Lighting and IoT Loads in a Dc Power Distribution Network

Dc power delivery in buildings, while a nascent technology, has demonstrated the potential to provide efficiency savings over ac power delivery and simplified integration pathways for renewable energy and storage [4]. As shown in Fig. 2.2, a candidate architecture consists of a 380 Vdc distribution bus, which facilitates lower wiring losses, and a collection of dc-dc power converters which will step down the 380 Vdc to some lower voltages required by end loads. These loads could be light-emitting diode (LED) loads, as shown, or other devices as part of the Internet-of-Things (IoT). In many cases, these loads require dc voltage and current, which makes dc distribution a natural choice, since a conversion from ac to dc is generally more complex due to the need for an additional rectification stage and potentially the need to implement power factor correction circuits and controls. On the other hand, a dc to dc power conversion can be a single stage process, and generally have high efficiency

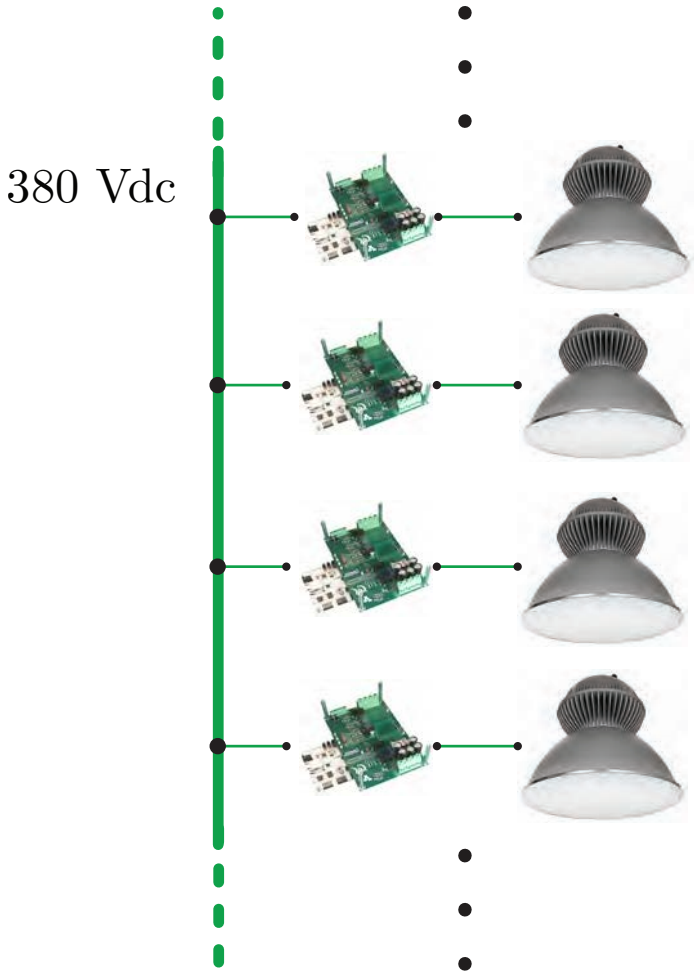


Figure 2.2: A candidate 380 Vdc distribution architecture with LED loads.

and small size. However, the proliferation of end loads can introduce challenges with respect to stability and power quality of the overall network. Each dc power converter will introduce new harmonics to the point of common coupling, and as more loads are added, the associated harmonics of the interconnected loads can potentially constructively interfere. The aggregate impact of these harmonics can potentially detrimentally affect the performance, efficiency, and operation of every load connected to the distribution bus.

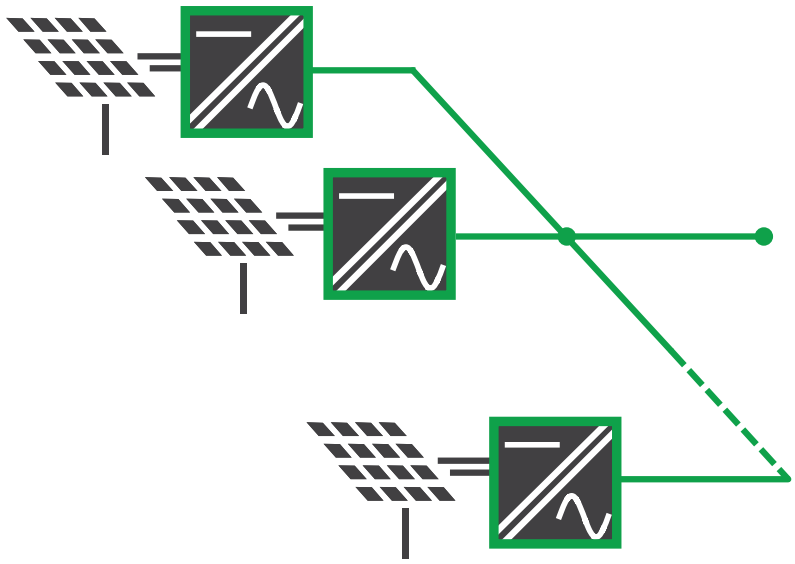


Figure 2.3: Parallel-connected ac microinverter-based architecture for photovoltaic systems integration.

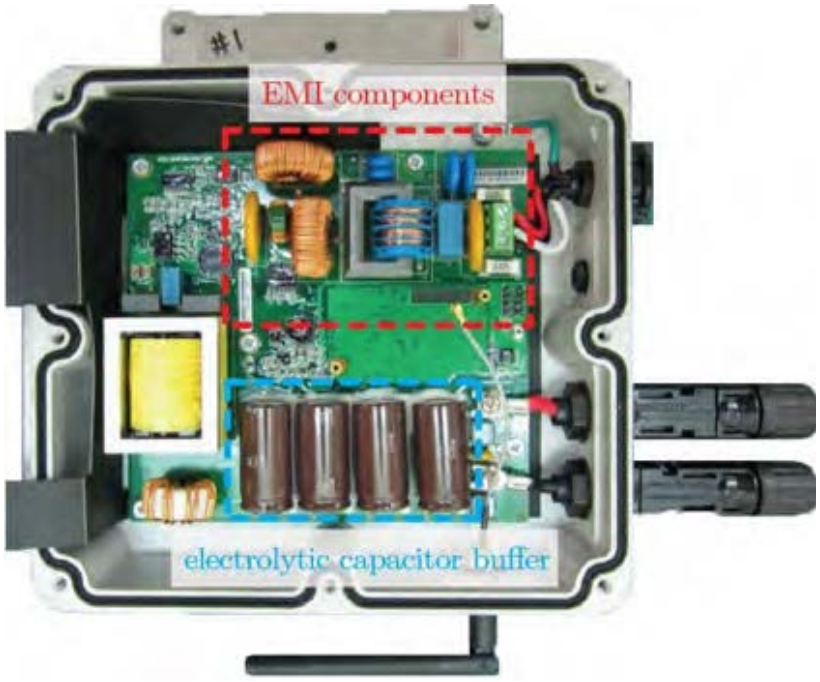


Figure 2.4: Teardown of a 250W Ubiquiti Energy SM-MI-250 sunMAX Microinverter. As shown, components related to EMI and filtering comprise the majority of the size of the overall converter.

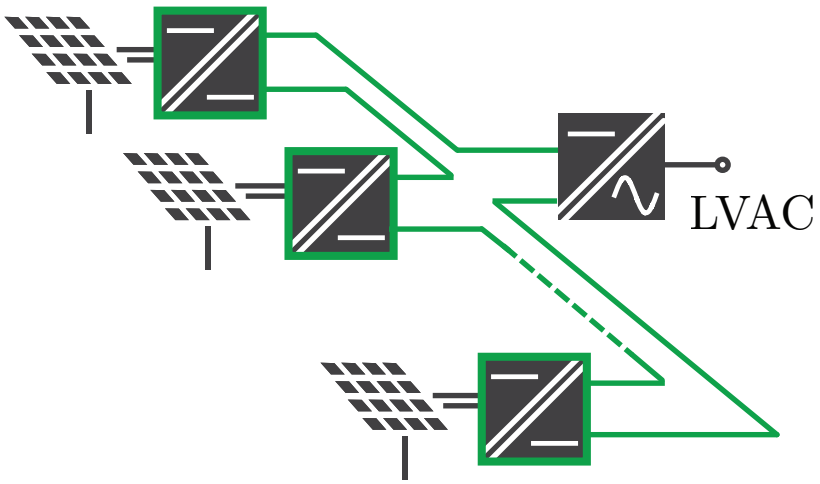


Figure 2.5: Series-connected dc power optimizer-based architecture for photovoltaic systems integration.

2.1.3 Microinverters and Dc Power Optimizers for Solar Photovoltaic Systems

Large amounts of photovoltaic (PV) penetration now exist at the residential and utility scale for grid-connected and islanded microgrid systems. Power electronics associated with PV systems integration, such as microinverters and dc power optimizers, introduce new challenges with respect to the high frequency harmonics and associated stability issues that originate from their inherent switching and non-linear dynamical behavior. These challenges are exacerbated as networks scale organically and need to accommodate increasingly greater amounts of power converter-interfaced renewables.

In microinverter-based architectures (Fig. 2.3), power electronics generate harmonics on the grid-connected ac side, which require filters to suppress and comply with regulatory grid codes (e.g. IEEE 1547). These filters can comprise nearly half of the overall cost, size, and weight of the microinverter, as shown in Fig. 2.4. Similarly, in dc power optimizers-based architectures (Fig. 2.5), power electronics generate harmonics (switching ripple) on the intermediate dc bus, which potentially require electrolytic capacitors to filter and maintain an acceptable ripple. These capacitors are bulky, failure-prone, and degrade the reliability and lifetime of the overall system. Taken as a whole, networks must be overdesigned to safely operate at the worst case scenario when the higher order harmonics of each power converter constructively interfere; otherwise system instabilities and damage to grid-connected equipment can occur. Ultimately, these challenges result in a hidden fundamental bottleneck that limit the feasibility of large-scale, distributed PV systems that are low-cost, scalable, and

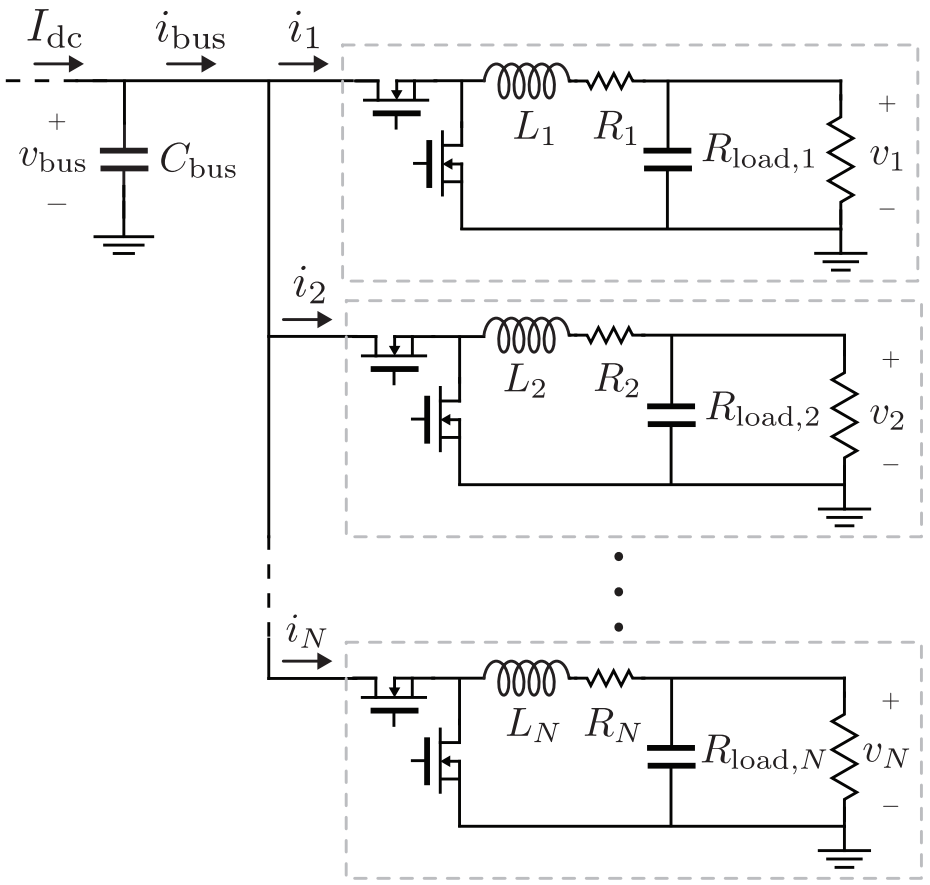


Figure 2.6: N input-parallel connected dc-dc buck converters with independent output voltages $v_1, \ldots, v_N$ and load resistances $R_{\text{load},1}, \ldots, R_{\text{load},N}$.

offer high power quality.

2.2 Conventional Interleaving Techniques

In series- and parallel-connected multistage architectures, various hardware and software techniques can be used to mitigate the detrimental effects of interconnecting numerous switching power converters. In this section, we will focus on control-based strategies that are commonly used to address these effects, in particular, symmetric interleaving.

Consider the topology shown in Fig. 2.6 which consists of N input-parallel connected dc-dc buck converters with independent output voltages $v_1, \ldots, v_N$ and load resistances $R_{\text{load},1}, \ldots, R_{\text{load},N}$. We will reference this topology in the analysis that follows, but the analysis can, in theory, be generalized to any combination of input/output and parallel/series

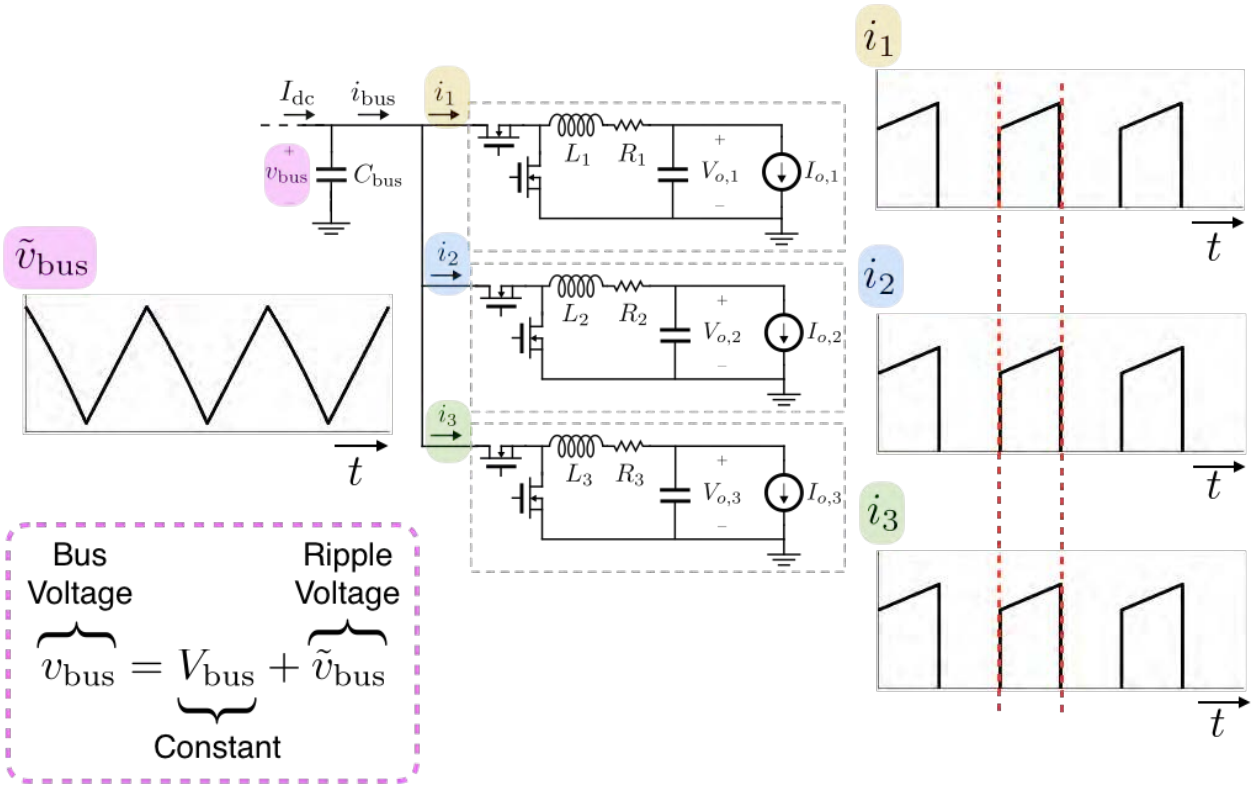


Figure 2.7: Illustration of converter waveforms when loads $I_{o,1}$, $I_{o,2}$, and $I_{o,3}$ are identical and switch timing is synchronized to be in-phase.

connected dc-dc converters, including combinations in which a subset of converters are connected to other subsets of converters.

Fig. 2.7 illustrates operating waveforms of this circuit topology. Of particular interest is the *ripple voltage* ($\tilde{v}_{\text{bus}}$), that is, the ac component of the bus voltage. The magnitude of the ripple voltage corresponds to the aggregate harmonics and distortion of every power converter connected to the bus, and is the quantity we seek to minimize in the following analysis. As discussed, the attenuation of the ripple voltage can rely on electrolytic capacitors in many applications, which add to the volume, cost, and reliability challenges of the end-use application. Even in integrated circuit applications, the need for buffer capacitance for ripple attenuation and transient response can dominate the layout area of a chip.

Note that C_{bus} represents the aggregate input capacitance at every converter (e.g. $C_{\text{bus}} = C_1 + C_2 + \cdots + C_N$), and is not necessarily a separate capacitance on the bus of the distribution system. Additionally, each converter would typically have some amount of capacitance at its input, which we aggregate into the C_{bus} quantity.

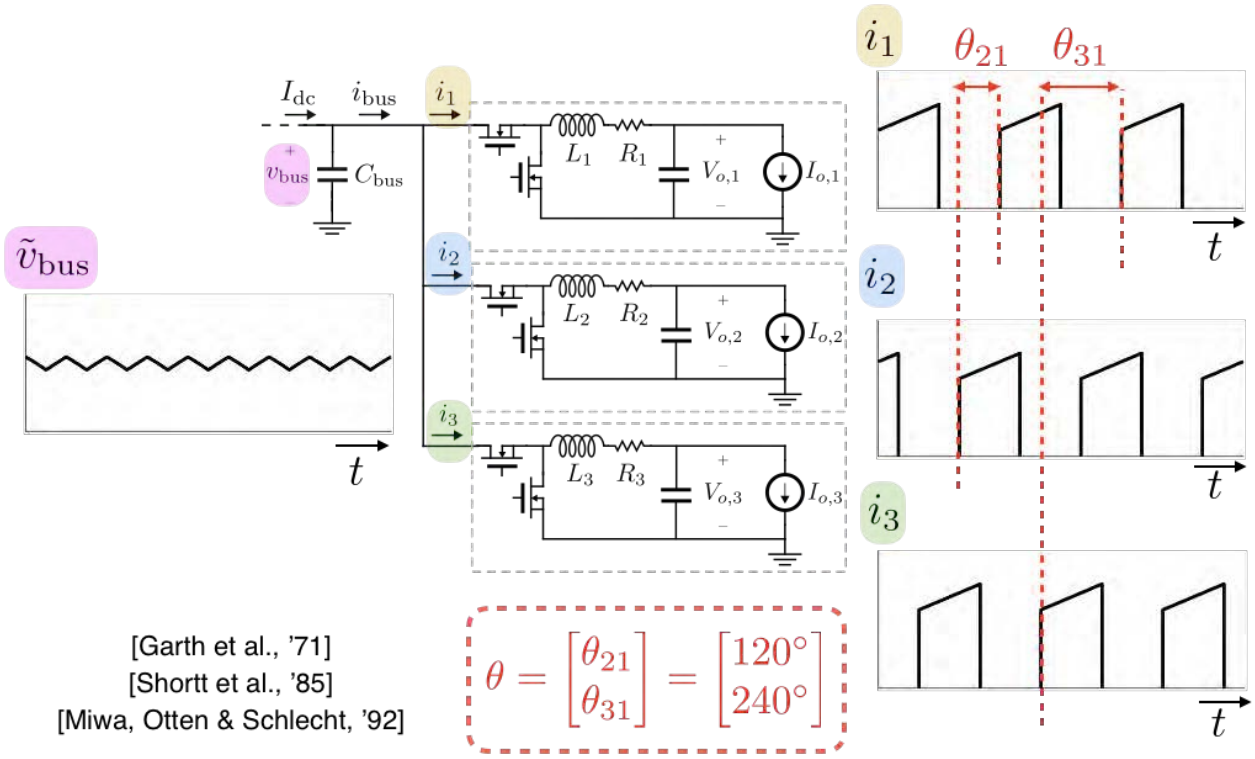


Figure 2.8: Illustration of converter waveforms when loads $I_{o,1}$, $I_{o,2}$, and $I_{o,3}$ are identical and switch timing is interleaved.

As shown on the right of Fig. 2.7, the input current (i_n) to each buck converter is a pulse-like waveform that is non-zero when the high-side switch is turned on, and is zero when the high-side switch is turned off. Kirchhoff's circuit laws dictate that the aggregate current at the input of all the converters (i_{bus}) is the sum of the currents to each converter. Correspondingly, the ripple voltage $\tilde{v}_{\text{bus}}$ can be determined by this aggregate current i_{bus} flowing into and out of C_{bus}. In the example shown, because the loads $I_{o,1}$, $I_{o,2}$, and $I_{o,3}$ are identical and switch timing of each converter is synchronized to be in-phase, the ripple voltage has periodicity approximately equal to that of a single converter.

Now, consider the operation of the same circuit topology with the same identical loads $I_{o,1}$, $I_{o,2}$, and $I_{o,3}$ but with the phase spacing of i_1, i_2, and i_3 as shown in Fig. 2.8. In this scenario, classically called *symmetric interleaving*, the pulse width modulation (PWM) carrier waves of every converter are phase shifted such that they are equally spaced over a single switching period. Thus, the input currents i_n are $360°/N$ phase shifted from each other (e.g. the PWM of five power converters would be spaced apart with a 72° phase shift).

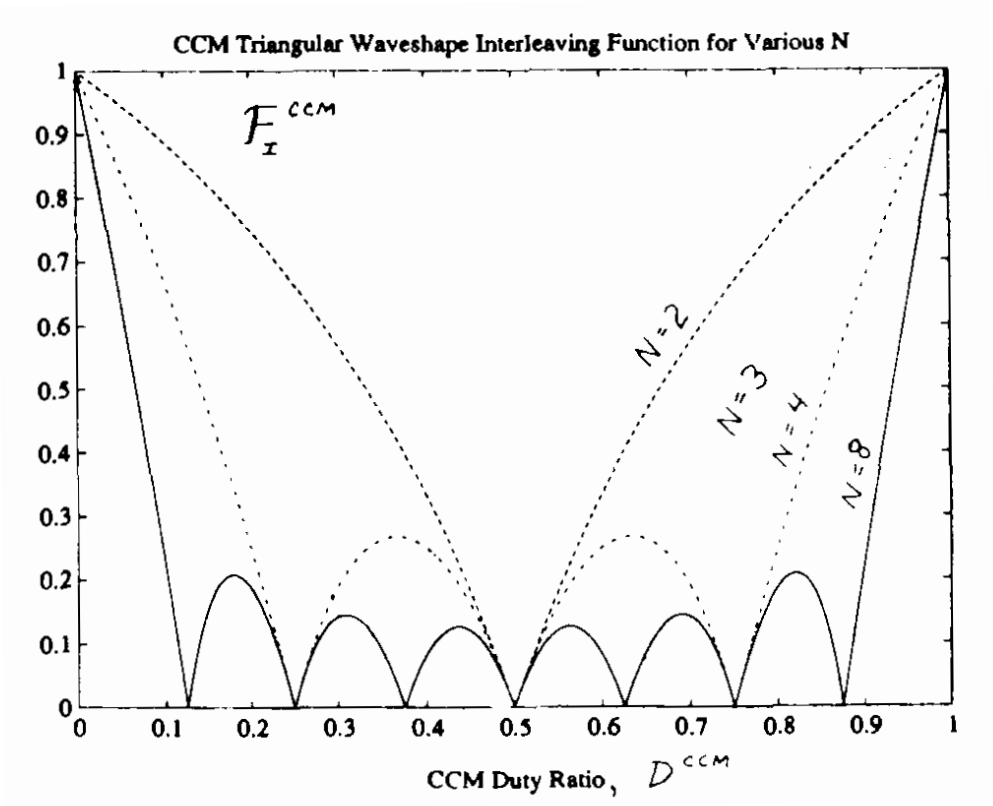


Figure 2.9: Result from [22] which illustrates the "normalized interleaving function" $\mathcal{F}$ as the number of interleaved converters is varied from $N = 2$ to $N = 8$ and plotted as a function of the duty ratio. Of note is that the value never exceeds one–that is, applying symmetric interleaving to a symmetric circuit will never result in a net current ripple that is higher than the current ripple of a single converter.

As a result of this phase spacing, the resulting ripple voltage now has a waveform that can be seen as the waveform on the left of the figure. As shown, the periodicity of this waveform has increased by a factor of three compared with the periodicity of the switching waveforms of each individual converter. Moreover, the peak-to-peak magnitude of the waveform has been attenuated compared to the waveform from Fig. 2.7 when the phase currents were synchronized to be in phase. These two factors—increased effective switching frequency and small ripple magnitude—serve as strongly effective mechanisms for reducing the impact of the ripple voltage as well as reducing the amount (and size) of the capacitance needed to maintain an acceptable amount of harmonics or ripple on the common bus. It is also a mechanism for improving the overall system efficiency, as smaller ac currents will reduce losses in the buffer capacitor(s).

It has been shown extensively in literature that symmetric interleaving is the optimal

method to minimize the ripple voltage—in an $\mathcal{L}_2$-norm sense— when the loads are symmetric (i.e. when the steady state dynamics of each converter are identical) [23, 24, 22]. For instance, a key result from [22] is duplicated in Fig. 2.9, which illustrates some important properties of symmetric interleaving. The figure plots what the author calls the "normalized interleaving function" $\mathcal{F}$, which is a function of the waveform type, the duty ratio, and the number of symmetrically interleaved converters. For a single converter, the value of this function is one. There are a few interesting conclusions that can be deduced from this plot. First, for any number of interleaved converters at any duty ratio, $\mathcal{F}$ never exceeds one–that is, applying symmetric interleaving to a symmetric circuit will never result in a net current ripple that is higher than the current ripple of a single converter. Second, for certain topologies at specific duty ratios, $\mathcal{F}$ can be zero–that is, the ripple can be completely eliminated. Third, the net ripple can be analytically determined with information about the waveform, duty ratio, and number of interleaved cells.

Because of the many benefits discussed here, symmetric interleaving is widely used in applications ranging from sub-mW on-chip power delivery [25] to multi-MW HVDC power converters [26]. However, there are a number of limitations which constrain the applicability of symmetric interleaving to specific topologies and/or operating scenarios. We will focus on two such limitations in the following subsections, specifically, 1) operating and circuit asymmetries and 2) the centralization of control. Indeed, in order to adequately address many of the power quality concerns discussed in Section 2.1, we must address these limitations in ways that will generalize the optimality of symmetric interleaving to this broad class of applications.

2.2.1 Limitation #1: Operating and Circuit Asymmetries

The first limitation we will discuss is associated with operating and circuit asymmetries. The optimality of symmetric interleaving is guaranteed when symmetry exists in the circuit, that is, when the current handled by each converter is identical. This scenario presumes identical input and output voltages at each converter, as well as identical dc current handled by each converter. While this scenario is common in input- and output-parallel connected dc-dc converters (e.g. multiphase dc-dc converters), it does not accurately depict most of the operating scenarios described in Section 2.1. For instance, in a power management integrated circuits, many different output voltages are typically required by end loads, as well as different current and power requirements. Moreover, even in scenarios that presume symmetric operation, non-idealities in passive or active components, such as the direct current

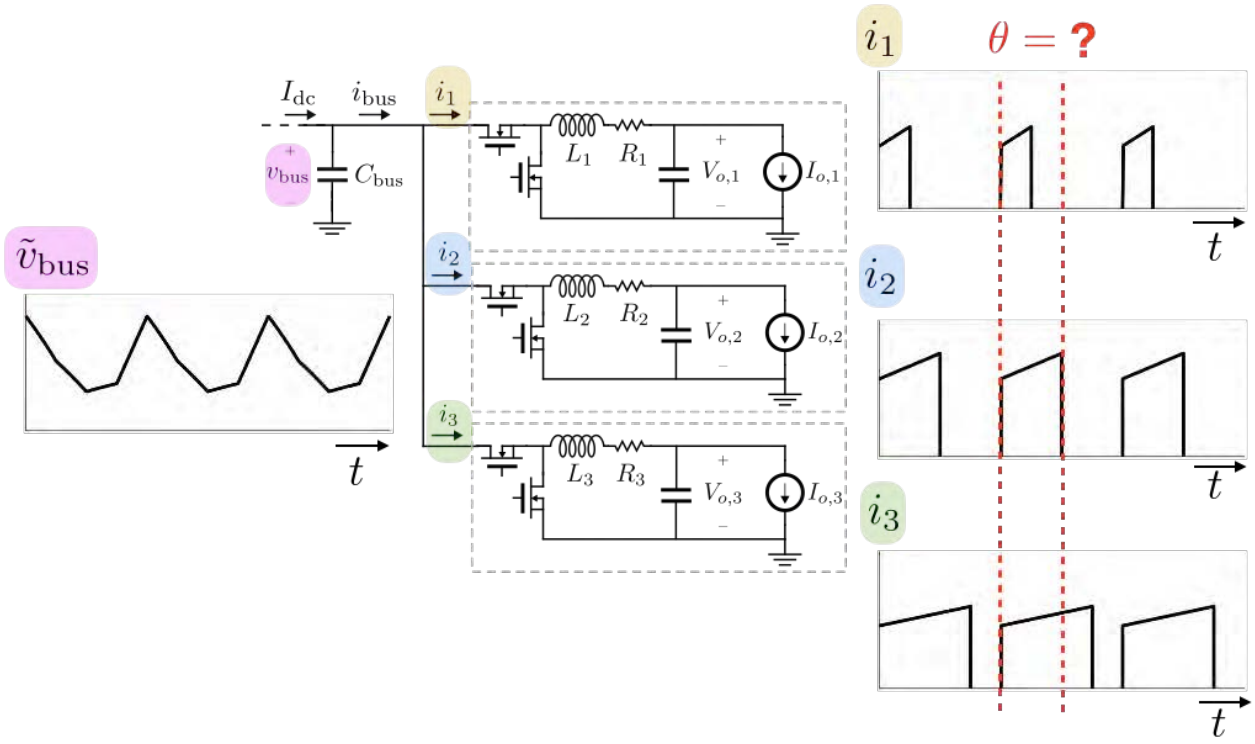


Figure 2.10: Illustration of converter waveforms when loads $I_{o,1}$, $I_{o,2}$, and $I_{o,3}$ are not identical and switch timing is synchronized to be in-phase.

resistance (DCR) of the inductor, can introduce non-negligible operating asymmetries.

Thus, in these applications, the duty cycles and dc load currents in each converter will be different. Consider Fig. 2.10 which illustrates converter waveforms when such asymmetries exist in the system. As shown on the right of the figure, the duty cycle and dc average values of the current waveforms can be asymmetric across each converter. As a result of these asymmetries and the in-phase switch timing, there is some ripple voltage which will have a relatively large magnitude. Unlike the symmetric case scenario where it is well-known that symmetric interleaving will optimally minimize this ripple voltage, for this asymmetric scenario, it is an open question as to which phase shifting should be used. Existing literature has focused on first harmonic elimination techniques [27] and randomized modulation schemes [28, 29], among others. However, determining the *optimal* phase shift across any range of asymmetries and circuit topologies could offer dramatic improvements in ripple voltage reduction and could support many practical applications. For instance, if we consider the example shown in Fig. 2.11, we see that if symmetric interleaving is applied to a circuit with asymmetries, the resulting ripple voltage does not exhibit significant attenuation.

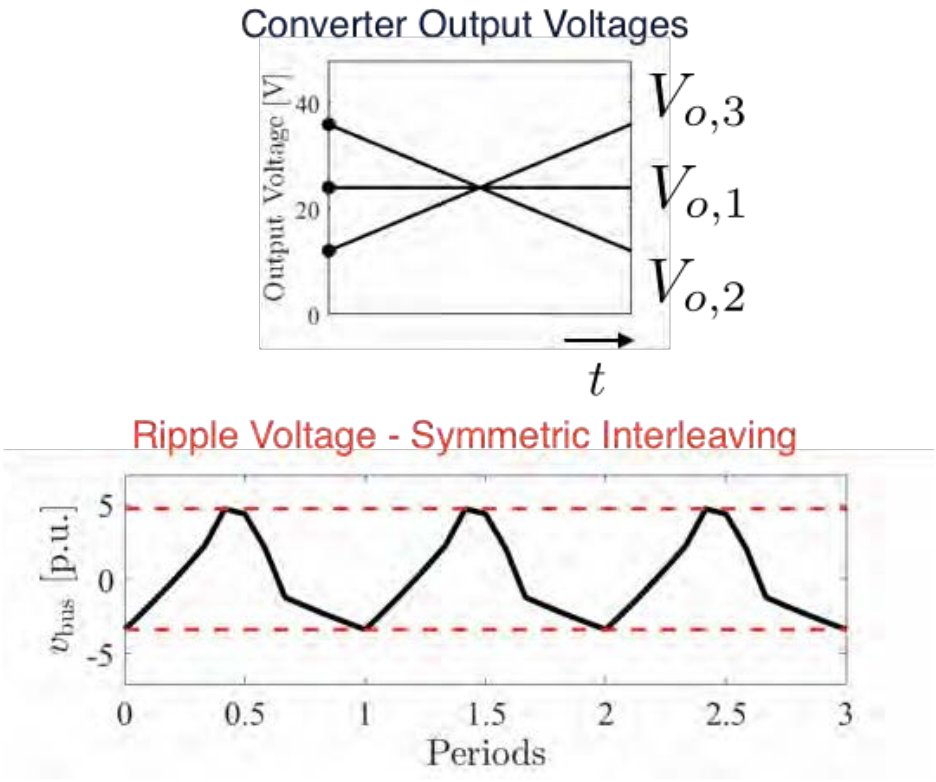


Figure 2.11: An illustration of three periods of v_{bus} when the output voltages of each converter are swept as shown in the top subfigure and the circuit is operated with symmetric interleaving. v_{bus} is normalized to the magnitude of v_{bus} when the output voltages are identical (the symmetric operating scenario).

2.2.2 Limitation #2: Centralization of Control

The second limitation we will discuss is associated with the need for centralized control and/or communication in existing systems for symmetric switch interleaving. State-of-the-art approaches can be divided into two categories: 1) distributed and 2) centralized, as shown in Fig. 2.12.

Distributed methods, to date, require a local controller at every converter as well as an explicit communication bus which carries analog or digital information between every converter. The local controller is responsible for voltage/current regulation of the converter along with generating the necessary PWM signals, while the communication bus facilitates coordination with neighboring converters in order to effect the appropriate phase shifting of the PWM [30, 31]. These methods have an advantage in that the controllers are distributed and can be added or removed as needed, but they have a disadvantage in that the communication bus serves as a single-point-of-failure within the system.

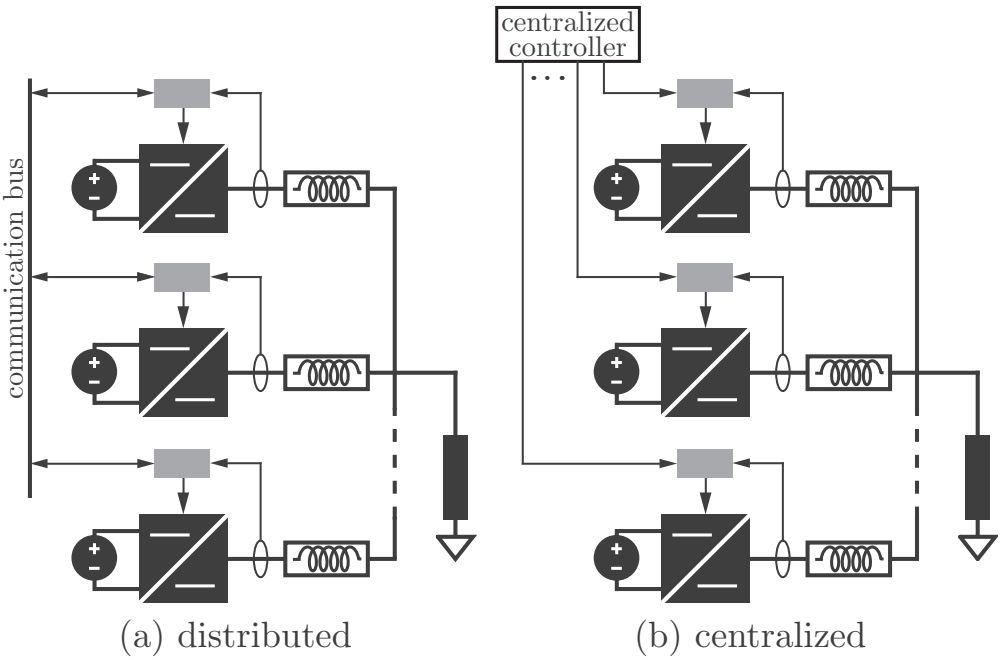


Figure 2.12: State-of-the-art methods for symmetric interleaving are (a) distributed, requiring a communication bus [30, 31]. Majority of the literature on interleaving focuses on switch timing managed (b) centrally [16, 32, 33, 34, 35, 36].

Centralized methods, on the other hand, require a single controller that will either explicitly govern the phase shifting of individual converters or generate the necessary PWM for each converter as to guarantee symmetric interleaving. Indeed, a majority of existing literature has focused on methods of this approach [16, 32, 33, 34, 35, 36]. Similarly, a centralized control mechanism will introduce a single point-of-failure within a system and also limit the modularity and scalability of the power conversion system. Additionally, in many applications (e.g. distributed ad-hoc microgrids), it is unrealistic to implement such a controller as communication latencies will inhibit the precise control timing needed to facilitate symmetric interleaving. Even in on-chip applications, the generation of high-precision clocks can consume non-negligible amounts of power and also complicate the system design particularly when multiple phase shifting configurations are required (e.g. for phase shedding applications).

2.3 Summary

This chapter has discussed applications that require scalable, fault-tolerant, and efficient power delivery. Many of these applications rely on series- or parallel-connected multistage power conversion architecture, which can benefit from control mechanisms that can improve power quality, stability, and efficiency. One such method discussed is symmetric interleaving, which optimally minimizes aggregate harmonics in systems comprised of identical series- or parallel-connected power converters. Two limitations of symmetric interleaving are discussed. The first limitation arises from systems that are asymmetric in topology or operation. The second limitation arises from the need for centralized communication or control among distributed power converters within a system. Solutions to both of these limitations are developed in Chapters 3 and 4.

Chapter 3

Optimization & Control of Distributed Power Converters

This chapter introduces the notion of *Minimum Distortion Point Tracking (MDPT)*: a control architecture for networks of dc-dc converters that are connected in series or parallel at the input or output where switching waveforms are optimally phase shifted to minimize the aggregate ripple power. In a sense, MDPT generalizes the ubiquitous concept of interleaving in balanced systems to a broad class of asymmetric series- or parallel-connected dc-dc converters. For networks of up to one hundred interconnected power converters, MDPT demonstrates a one to two order of magnitude reduction (-14 dB to -22 dB) in distortion power. Realizing power-quality improvement with control design implies that significant reductions in passive filtering can be achieved. We present and experimentally verify three algorithms that can dynamically solve the MDPT optimization problem on a network of three input-parallel connected dc-dc buck converters handling 1.8 kW. The experimental results illustrate an up to 3.06$\times$ reduction in the peak-to-peak ripple of the parallel-side bus voltage and convergence close to an optimal steady state solution in 5 ms. MDPT represents a new control mechanism to dramatically improve the power quality of large-scale power conversion networks.

3.1 Overview of Minimum Distortion Point Tracking

We introduce a new control architecture, termed *Minimum Distortion Point Tracking* (MDPT), which generalizes the notion of interleaving in balanced systems to a broad class of asym-

metric networks of dc-dc converters that are connected in parallel or series at the input or output. We present the concept of the *Minimum Distortion Point* (MDP), which establishes a first principles limit on the minimum distortion, or ac ripple power, that is attainable with phase shifting for a network of interconnected dc-dc converters. In particular, the MDP is defined as the phase shift across the converters that globally minimizes the aggregate distortion in an ℓ_p-norm sense. Minimization of this ac power is desirable in that it is precisely this quantity that determines the minimum filtering needed to satisfy a maximum ripple constraint in a given circuit. Using this definition, we develop three practical algorithms for MDPT, that is, real-time optimization methods of identifying and perturbing the system towards the MDP. Each MDPT algorithm is experimentally verified on a network of three input-parallel connected dc-dc buck converters handling a total power of 1.8 kW. The results will illustrate that peak-to-peak ripple reductions up to 3.06× are possible, as well as convergence close to a globally optimal steady state solution in 5 ms. Moreover, numerical analysis on networks of up to one hundred interconnected power converters indicate that MDPT can enable a one to two order of magnitude reduction (-14 dB to -22 dB) in distortion power relative to distortion power obtained with uncoordinated converter operation. Compared to existing literature, Minimum Distortion Point Tracking distinguishes itself in its: i) *generality*—the theory, analyses, and techniques can be applied to any asymmetric network of dc-dc converters regardless of whether the asymmetry arises from the topology or the operating condition, and ii) *optimality*—it establishes a first principles limit on the minimum ac ripple power that is attainable with phase shifting.

The remainder of this chapter is organized as follows. Section 3.2 presents the mathematical principles of the *Minimum Distortion Point* (MDP). We present numerical analyses that discuss the performance enhancements that can be realized when operating at the MDP. Section 3.3 presents a conceptual overview of *Minimum Distortion Point Tracking* (MDPT), an unconstrained optimization problem that seeks to find the phase shifting across a generalized network of power converters that will globally minimize the aggregate distortion, that is, bring the system to the MDP. Algorithms for implementing MDPT based on the gradient method, the nonlinear Gauss-Seidel method, and a metaheuristic optimizer are presented in Sections 3.4, 3.5, and 3.6, respectively. Experimental results on a network of three input-parallel connected dc-dc buck converters validate the performance of each algorithm. Section 3.7 presents analysis and comparisons of the characteristics of each algorithm with respect to computational complexity, convergence speed, decentralization of control, and the optimality of the steady state solution. Section 3.8 provides a conclusion and summary of

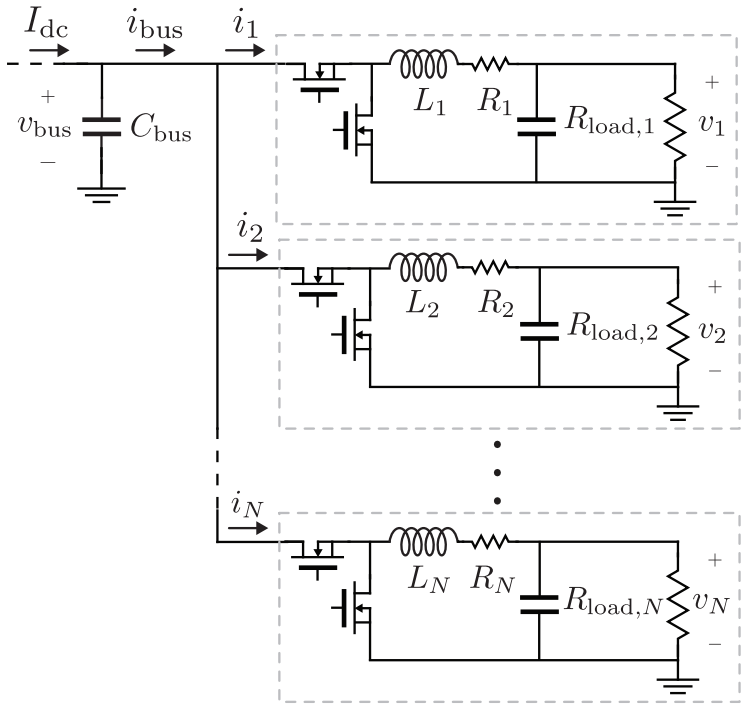


Figure 3.1: N input-parallel connected dc-dc buck converters with independent output voltages $v_1, \ldots, v_N$ and load resistances $R_{\text{load},1}, \ldots, R_{\text{load},N}$.

the contribution.

3.2 Characterizing the Minimum Distortion Point (MDP)

In this section, we define the Minimum Distortion Point (MDP) in a mathematical sense. The MDP can be defined for any network of dc-dc converters that are connected in series or parallel at the input or output. In particular, the MDP is well-defined for: i) different dc-dc converter topologies, ii) different interconnection architectures, including converters connected in series or parallel and radial, loop, or network systems, and iii) network models capturing parasitics and line impedances. In the following developments, we consider the specific scenario for a system of N dc-dc buck converters operating in continuous conduction mode at periodic steady state with identical switching frequencies, f_s, and connected in parallel at the input (see Fig. 3.1).

Following this mathematical definition, we will present numerical simulations that demon-

strate the achievable reductions in aggregate distortion that are possible when operating at the MDP for a candidate system with three interconnected converters. Then, we will present a Monte Carlo numerical simulation that illustrates how the achievable reductions in aggregate distortion scale with the number of interconnected power converters.

3.2.1 Definition and Interpretation of Distortion

Distortion, $\mathcal{D}$, is defined as any ℓ_p-norm of the ac harmonics of a particular signal of interest. For the purposes of this work, we consider a specific scenario when $\mathcal{D}$ is the squared ℓ_2-norm of the ac harmonics of the dc bus voltage, that is, v_{bus} in Fig. 3.1. With the selection of this norm, $\mathcal{D}$ is a metric that quantifies the ac (ripple) power associated with this voltage, and is closely related to the total harmonic distortion (THD) of the signal. The minimization of this quantity is desirable in that it is proportional to the ac power handled by the capacitor(s) C_{bus}, and thus, dictates the volumetric size of the components as well as the losses associated with handling the ac power. Note that C_{bus} models the aggregate paralleled input capacitance of each dc-dc buck converter. While the squared ℓ_2-norm is chosen for this work, in other applications, the minimization of other ℓ_p-norms may be more relevant. For instance, in integrated circuit applications, operating below the maximum voltage ratings of devices at all times is a key consideration, and, thus, the minimization of the ℓ_∞-norm could be considered.

3.2.2 Mathematical Principles of the MDP

The MDP refers to the operating point of a collection of interconnected switching power converters such that $\mathcal{D}$ is globally minimized. In the derivation that follows, we will develop an analytic closed-form unconstrained optimization problem that explicitly defines the MDP.

For a system of N dc-dc converters, collect the relative phase spacings between converters in the length $N-1$ vector $\boldsymbol{\theta} := [\theta_{21}, \theta_{32}, \ldots, \theta_{N(N-1)}]^{\mathrm{T}}$, with θ_{jk} denoting the phase spacing between the switching waveforms of the j^{th} and k^{th} converter, respectively. Furthermore, denote $\tilde{v}_{\text{bus}}$ as the ac voltage across C_{bus}, and $\mathcal{D}$ as the distortion of this voltage. The MDP is characterized by the $\boldsymbol{\theta}$ that globally minimizes an unconstrained optimization problem whose cost function is the quantity $\mathcal{D}$. Precisely, the MDP is the converter operation with the following phase spacing:

$$\boldsymbol{\theta}^{\star} = \arg\min_{\boldsymbol{\theta}} \mathcal{D}. \tag{3.1}$$

The explicit parametric dependence of $\mathcal{D}$ on $\boldsymbol{\theta}$ can be obtained by calculating the squared ℓ_2-norm of the Fourier coefficients of $\tilde{v}_{\text{bus}}$. From Parseval's theorem, it is also possible to determine $\mathcal{D}$ from the squared $\mathcal{L}_2$-norm of the time-series function $\tilde{v}_{\text{bus}}(t)$. However, this would not allow us to, in general, uncover the parametric dependence on $\boldsymbol{\theta}$ in an analytical fashion. For the particular example of the input-parallel connected buck converters illustrated in Fig. 3.1, the Fourier coefficients can be obtained by computing the Fourier series of each input current, i_ℓ, $\forall \ell = 1, \ldots, N$, taking the sum of these series to obtain the corresponding series for i_{bus} and then scaling by the capacitive impedance $1/\left(\mathrm{j}\omega C_{\text{bus}}\right)$. It emerges that the closed-form analytical expression for $\mathcal{D}$ is:

$$\mathcal{D} = \sum_{k=1}^{K} \sum_{n=1}^{N} (\beta_n^k)^2 + 4 \sum_{k=1}^{K} \sum_{j=1}^{N} \sum_{i=1}^{j-1} \beta_i^k \beta_j^k \cos(\theta_{ij}), \tag{3.2}$$

where β_ℓ^k is a scaled version of the k^{th} Fourier-series coefficient of i_ℓ, α_ℓ^k. The precise definitions of α_ℓ^k and β_ℓ^k as well as the complete derivation of the above expression are given in Appendix A.

3.2.3 Numerical Analysis of the MDP with a Network of Three Converters

We will now analyze the system performance at the MDP using a numerical simulation. In particular, we will attempt to quantify the achievable improvement in power quality that is obtainable when operating at the MDP. Here, and in the experimental results that follow in Section 3.3, we will use the *symmetric interleaved state* as a baseline for comparison. The symmetric interleaved state (when N converters are $360°/N$ phase shifted apart) results in the optimal minimization of $\mathcal{D}$ when symmetry exists in a circuit, and, thus, is equivalent to the MDP at these operating points. While symmetric interleaving is typically only applied to symmetric systems, we will use it as a baseline for characterizing the distortion in asymmetric systems.

Consider the topology in Fig. 3.1 for the particular case of $N = 3$ converters and with component parameters and operating conditions indicated in Table 3.1. We will operate this system to induce asymmetry with different output voltages, v_1, v_2, and v_3, since the component parameters and resistive loads in each phase are otherwise identical. We perform two different operating sweeps on this system. First, we fix $v_1 = 24\ V$ and sweep both v_2 and v_3 independently from $12\ V$ to $36\ V$. We record the reduction in $\mathcal{D}$ between the

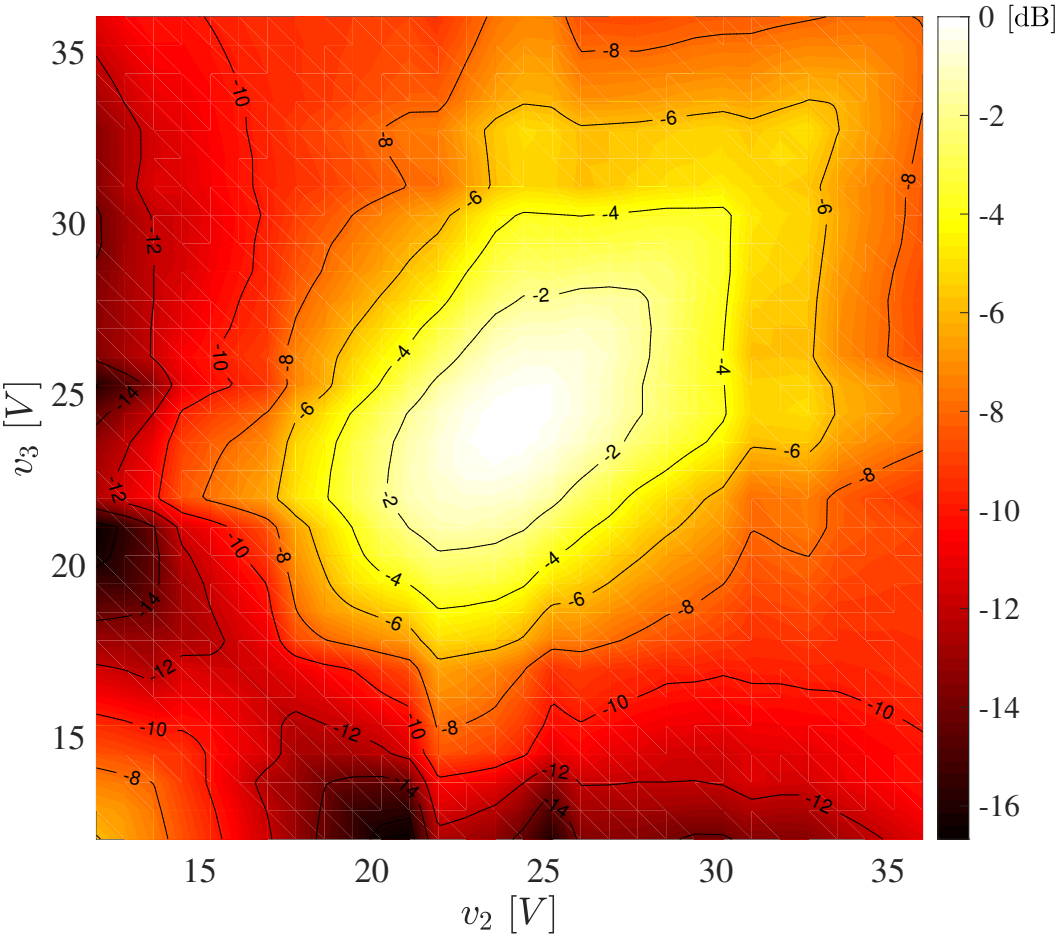


Figure 3.2: Achievable reduction in $\mathcal{D}$ (in dB) when operating at the MDP compared to operating at the symmetric interleaved state. Plot shows reduction in $\mathcal{D}$ when $v_1 = 24\ V$ and v_2 and v_3 are independently swept from 12 V to 36 V with identical fixed resistive loads on the output of each converter. The darker areas indicate regions where greater reductions in $\mathcal{D}$ are possible.

symmetric interleaved state and the MDP. The results of this sweep are shown in Fig. 3.2. Since $\mathcal{D}$ is essentially a metric of power, it is natural to express reductions or changes in $\mathcal{D}$ on a decibel scale. We observe that, at certain operating points, the reduction in $\mathcal{D}$ exceeds 16 dB. This reduction is promising in that it can facilitate improvements in power quality and the minimization of components needed for filtering or EMI compliance. Moreover, $\mathcal{D}$ is lower at the MDP across every operating point in this sweep. Also, note that at the point of symmetry, $v_1 = v_2 = v_3 = 24\ V$, symmetric interleaving indeed provides the optimal $\mathcal{D}$ and is equivalent to the MDP at this particular point.

Next, we perform a sweep in which v_1 is held constant at 24 V while v_2 and v_3 are

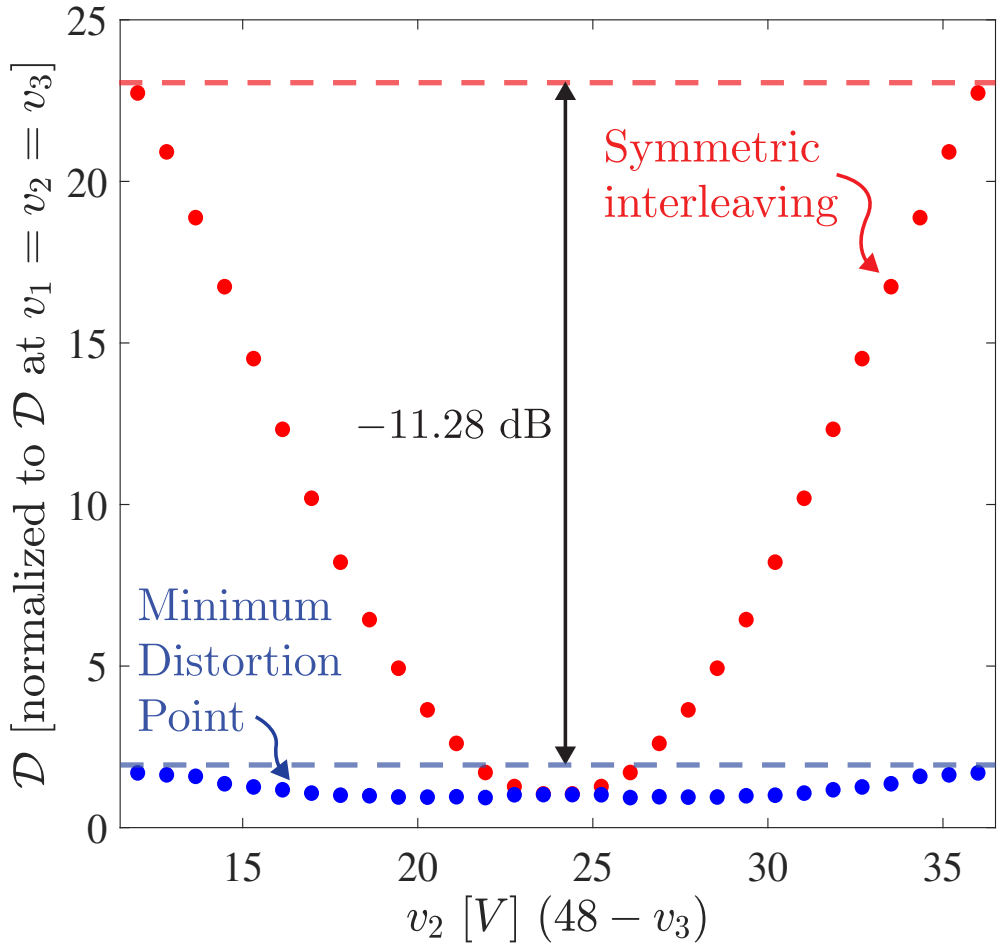


Figure 3.3: Reduction in $\mathcal{D}$ between the symmetric interleaved state and the MDP when $v_1 = 24\ V$ and $v_3 = 48 - v_2$.

swept such that $v_3 = 48 - v_2$. The results of this sweep are shown in Fig. 3.3, where $\mathcal{D}$ is normalized to the value of $\mathcal{D}$ obtained when $v_1 = v_2 = v_3 = 24\ V$ (at this point, the symmetric interleaved state and the MDP are identical). Across this sweep range, the worst case $\mathcal{D}$ at the MDP is −11.28 dB lower than the worst case $\mathcal{D}$ at the symmetric interleaved state. One practical implication of this result is that the capacitance requirement for C_{bus} to achieve the same output voltage ripple in v_{bus} is reduced by a factor of approximately 3.6×.

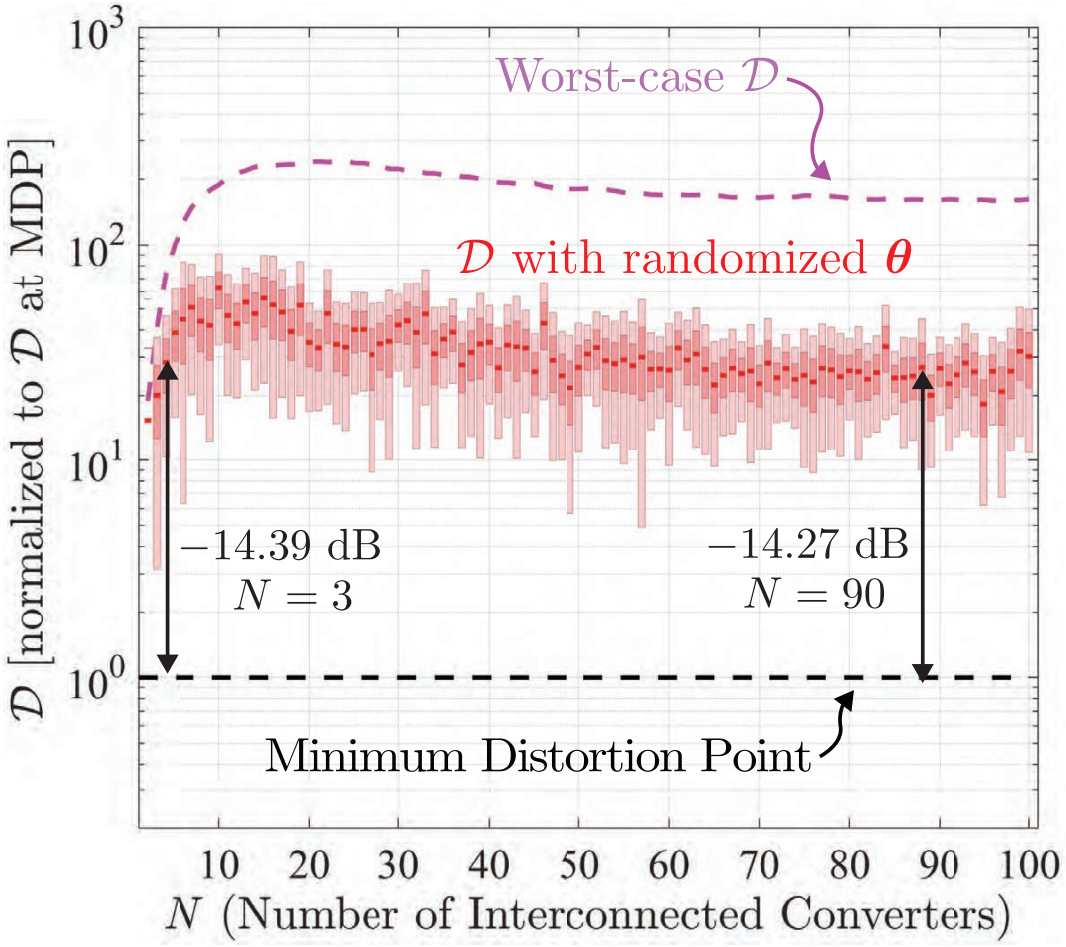


Figure 3.4: A Monte Carlo simulation that illustrates $\mathcal{D}$ obtained at various phase shifting scenarios, including the MDP (dashed black line), the worst-case phase shifting (dashed magenta line), and at a uniformly distributed random phase spacing across the N converters (red box plot indicating median, 25^{th} percentile, and 75^{th} percentile). For each N, one hundred Monte Carlo scenarios are simulated, and the output voltage, the average output current, and the inductor size of each of the N converters are randomized variables.

3.2.4 Numerical Analysis of the MDP with a Network of N Converters

We have shown that operating at the MDP can be beneficial for networks of just three interconnected power converters. Now, we will analyze how this improvement in performance can scale as more converters are added to the network. In the following analysis, we perform a Monte Carlo simulation for networks of up to one hundred interconnected power converters. For each network of N interconnected power converters (Fig. 3.1), we run one hundred scenarios with the randomized inputs as follows: 1) the output voltage v_ℓ, 2) the average

output current, and 3) the inductor size L_ℓ of each of the N converters. For each scenario, $\mathcal{D}$ is calculated at: i) the MDP, ii) a uniformly distributed random phase spacing across the N converters, and iii) the phase spacing across the N converters that globally maximizes $\mathcal{D}$, that is, the worst-case $\mathcal{D}$ that is possible. Additional details of the Monte Carlo simulation setup are provided in Appendix B.

The results of the Monte Carlo simulation are shown in Fig. 3.4. The data is normalized to the value of $\mathcal{D}$ at the MDP. The magenta dashed line indicates $\mathcal{D}$ obtained at the worst-case phase shifting. $\mathcal{D}$ obtained at the uniformly distributed random phase spacing across the N converters is shown with a box plot that presents the median, the 25^{th} percentile, and the 75^{th} percentile of the Monte Carlo simulation.

When compared with operation at the worst-case phase shifting, the MDP enables a -15.85 dB reduction in $\mathcal{D}$ when $N = 3$ and an approximately two orders of magnitude (-22 dB) reduction when $N > 10$. Since it is statistically unlikely that an uncoordinated network of power converters would ever reach this worst-case phase shifting, it is appropriate to also consider a comparison with $\mathcal{D}$ obtained at the uniformly distributed random phase spacing, which represents a more realistic model of such a network. Note that for this particular analysis, the symmetric interleaved state is not considered since its interpretation and implementation become largely infeasible particularly for larger networks of converters. Compared with operation at a randomized phase spacing, when $N = 3$, the achievable reduction in $\mathcal{D}$ is -14.39 dB from the median value, which approximately corroborates the analysis from Section 3.2.3 (Fig. 3.2). This amount of reduction in $\mathcal{D}$ remains relatively constant as $N \to 100$. This analysis suggests that both small and large networks of interconnected power converters can significantly benefit from operating at the MDP, potentially achieving upwards of an order of magnitude reduction in distortion power.

3.3 Minimum Distortion Point Tracking (MDPT)

With the MDP formally introduced and characterized, we now present *Minimum Distortion Point Tracking* (MDPT). Conceptually, MDPT encompasses control and optimization techniques whose objective is to bring a system towards the MDP; that is, to uncover the phase spacing according to equation (3.1). Because the unconstrained optimization problem of equation (3.1) is non-convex and of the nondeterministic polynomial time (NP) class, it does not admit an analytical solution even for $N = 2$. Thus, in this section, we develop and experimentally verify three MDPT algorithms that computationally solve equation (3.1) and

Table 3.1: Parameters and components for numerical simulations and experimental prototype.

Parameters/Component	Value
v_{bus}	48 V
C_{bus}	300 μF
L_ℓ	141.6 μH
R_ℓ	13.7 mΩ
Switching frequency	20 kHz
Control device	Xilinx Artix-7 XC7A35T

can be practically integrated into dc-dc buck converters controllers.

First, we will present an MDPT algorithm based on the gradient method (Section 3.4). We will see that this method is conceptually simple and easy to implement, but relies on universal real-time knowledge of the entire network, has moderate convergence speed, and can only converge to local minima and not necessarily the MDP. We will analyze how local minima will affect the steady state performance of the algorithm. Second, we will present an MDPT algorithm based on the nonlinear Gauss-Seidel algorithm (Section 3.5). It will be shown that this algorithm can be completely decentralized, that is, the controller can be integrated at the level of each dc-dc buck converter and does not require peer-to-peer or centralized communication. The trade-off, however, is that the algorithm is more computationally intensive than the gradient method and, similarly, can only converge to local minima. Third, we will present an MDPT algorithm based on a metaheuristic optimizer, in particular, the particle swarm optimization (PSO) computational method (Section 3.6). We will see that this method enables the closest convergence to the global minimum (the MDP), but relies on universal real-time knowledge of the entire network and is the most computationally intensive of all three algorithms. As alluded to, each of the three presented algorithms has associated advantages and disadvantages, and these are discussed in detail and compared in Section 3.7.

3.3.1 Experimental Prototype

In order to experimentally validate the three MDPT algorithms, a hardware prototype consisting of three input-parallel connected dc-dc buck converters is used, as shown in Fig. 3.5. Each converter is rated for 600 W resulting in an overall power handling capability of 1.8 kW. Table 3.1 presents the parameter and component values for this hardware prototype. Each ℓ^{th} buck converter can locally sample the bus voltage v_{bus}, its output voltage v_ℓ, and its average output current. The bus capacitance C_{bus} is chosen as to yield a bus voltage ripple

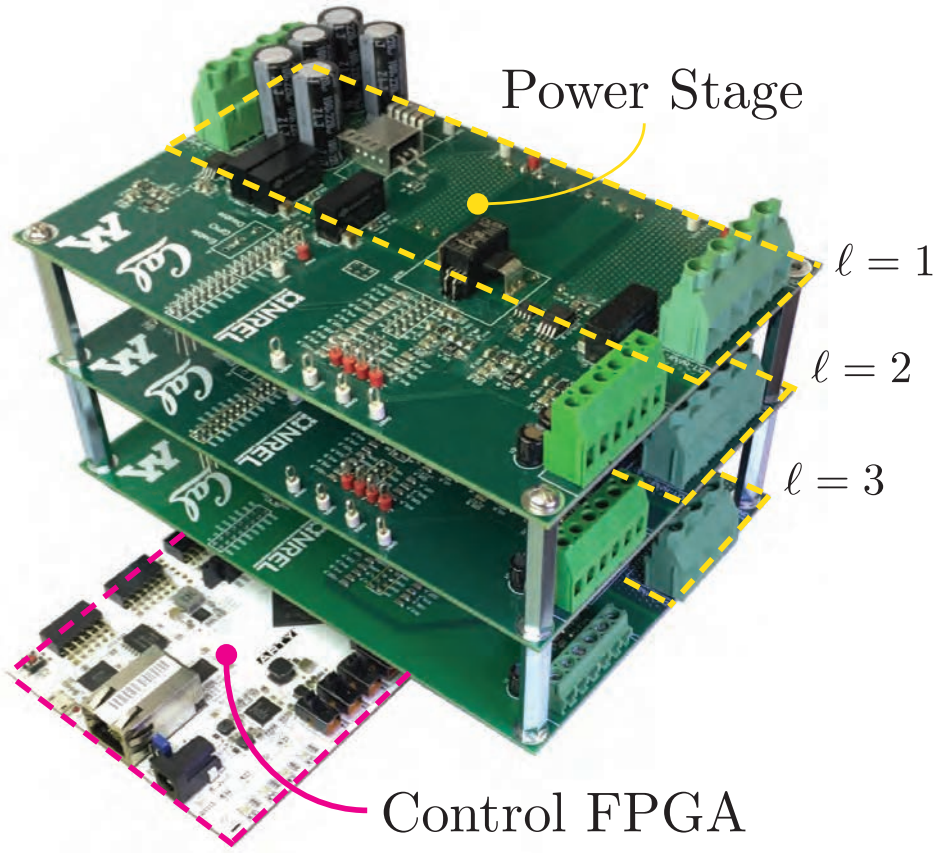


Figure 3.5: Hardware prototype consisting of three 600 W input-parallel connected dc-dc buck converters with 48 Vdc input bus.

ratio of approximately 6% under worst-case operating conditions. Note that this ripple ratio can be smaller, but is made intentionally large in these experiments as to clearly illustrate the voltage ripple waveform. For algorithms that require a controller for each buck converter (Section 3.5), three separate field-programmable gate array (FPGA) controller boards are used. For algorithms that require a centralized controller (Sections 3.4 and 3.6), a single FPGA controller board is used (as depicted in Fig. 3.5).

3.4 MDPT Algorithm #1: Gradient Method

3.4.1 Algorithm Principles and Design

The gradient-based MDPT algorithm uses the gradient of $\mathcal{D}$ to determine a direction and magnitude in which to perturb $\boldsymbol{\theta}$ [37]. By perturbing $\boldsymbol{\theta}$ iteratively using this technique, the

Algorithm 1 Gradient Method-Based MDPT Algorithm

1: Input: $v_{\text{bus}}, v_1 \dots v_N, I_1 \dots I_N, D_1 \dots D_N, C_{\text{bus}}$
2: Output: Steady state minimum of equation (3.2).
3: **repeat**
4: Calculate $\mathcal{D}$ from equation (3.2)
5: Calculate gradient $\nabla\mathcal{D}(\boldsymbol{\theta}[q])$
6: Calculate gradient step $\boldsymbol{\theta}[q+1]$ from equation (3.3)
7: **until** stopping criterion is met

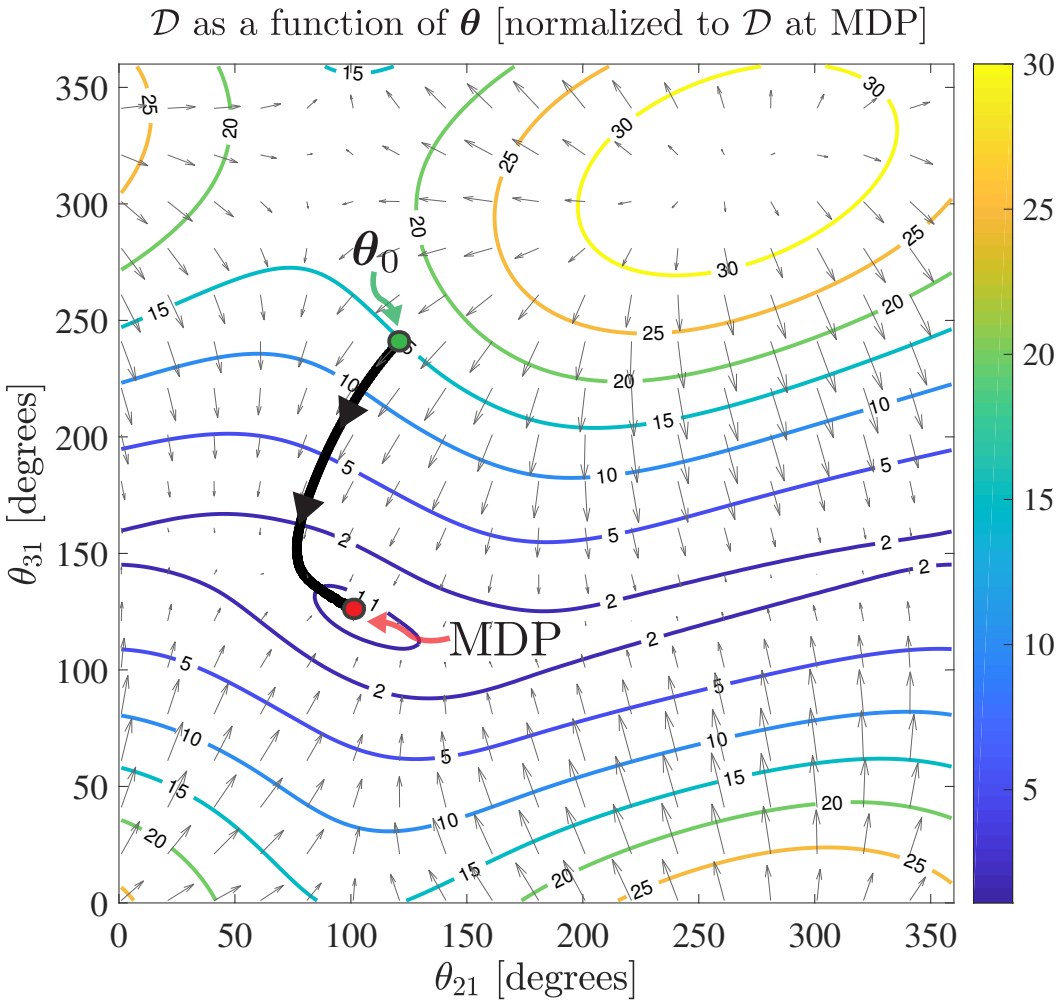


Figure 3.6: Numerical simulation of the gradient-based MDPT algorithm. Contour lines of $\mathcal{D}$ (normalized to $\mathcal{D}$ at the MDP) and arrows depicting $\nabla\mathcal{D}$ are shown.

system converges to the operating point that locally minimizes $\mathcal{D}$. In particular, we adopt

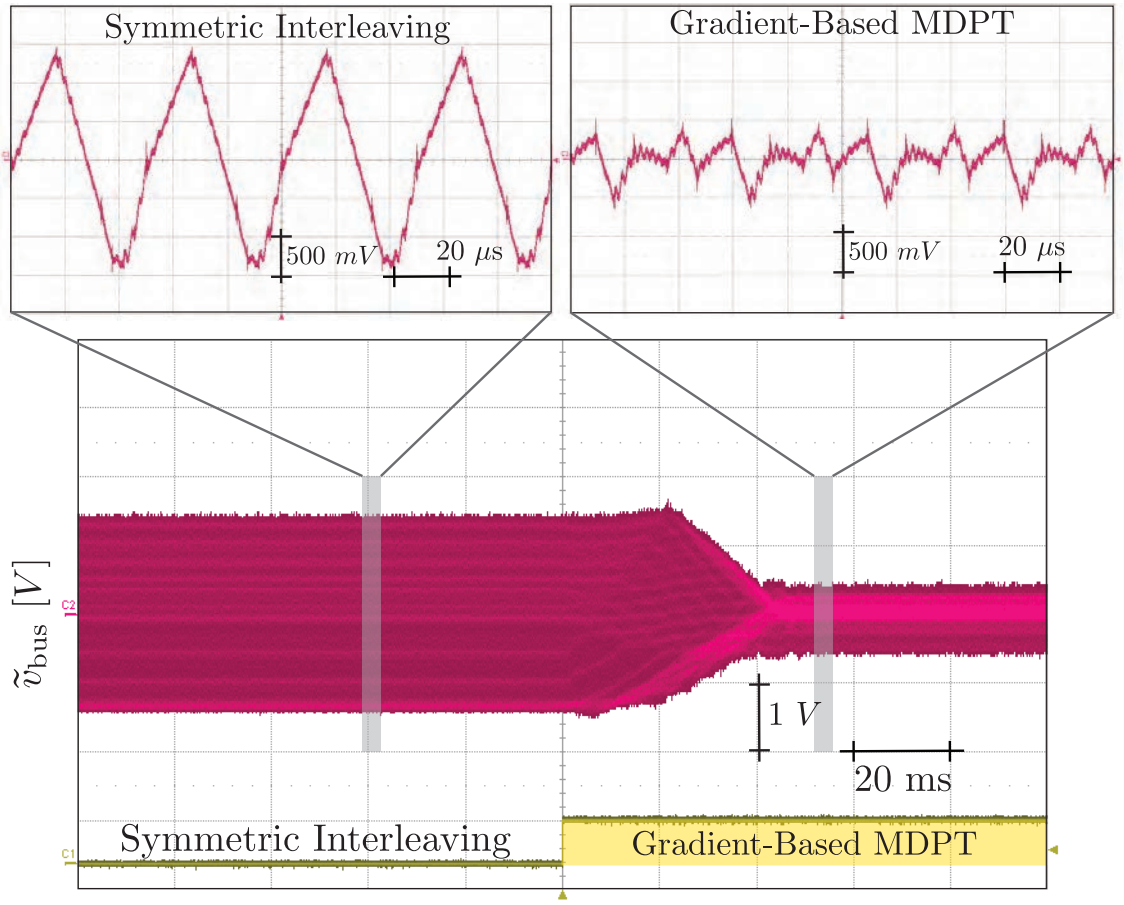


Figure 3.7: Experimental validation of the convergence speed and performance of the gradient-based MDPT algorithm. As shown, the algorithm converges in approximately 100 iterations (40 ms) and enables a 2.91× reduction in the peak-to-peak ripple of $\tilde{v}_{\text{bus}}$ compared to the peak-to-peak ripple at the symmetric interleaved state.

the following update rule for the $q+1$ update of $\boldsymbol{\theta}$:

$$\boldsymbol{\theta}[q+1] = \boldsymbol{\theta}[q] - \kappa \nabla \mathcal{D}(\boldsymbol{\theta}[q]) \tag{3.3}$$

where $\nabla \mathcal{D}(\boldsymbol{\theta}[q])$ is the gradient of $\mathcal{D}$ with respect to $\boldsymbol{\theta}$ at the q update instant, and κ is a scalar that can be empirically determined to trade off between numerical stability and convergence speed. Since $\mathcal{D}$ is not a convex function of $\boldsymbol{\theta}$, the gradient descent-based MDPT will track local minima depending on the initial condition. Analysis of these minima are presented in Section 3.4.3.

Next, we perform a numerical simulation to verify the operation of the gradient descent-based MDPT. Again, consider the topology in Fig. 3.1 for $N = 3$ and with the component

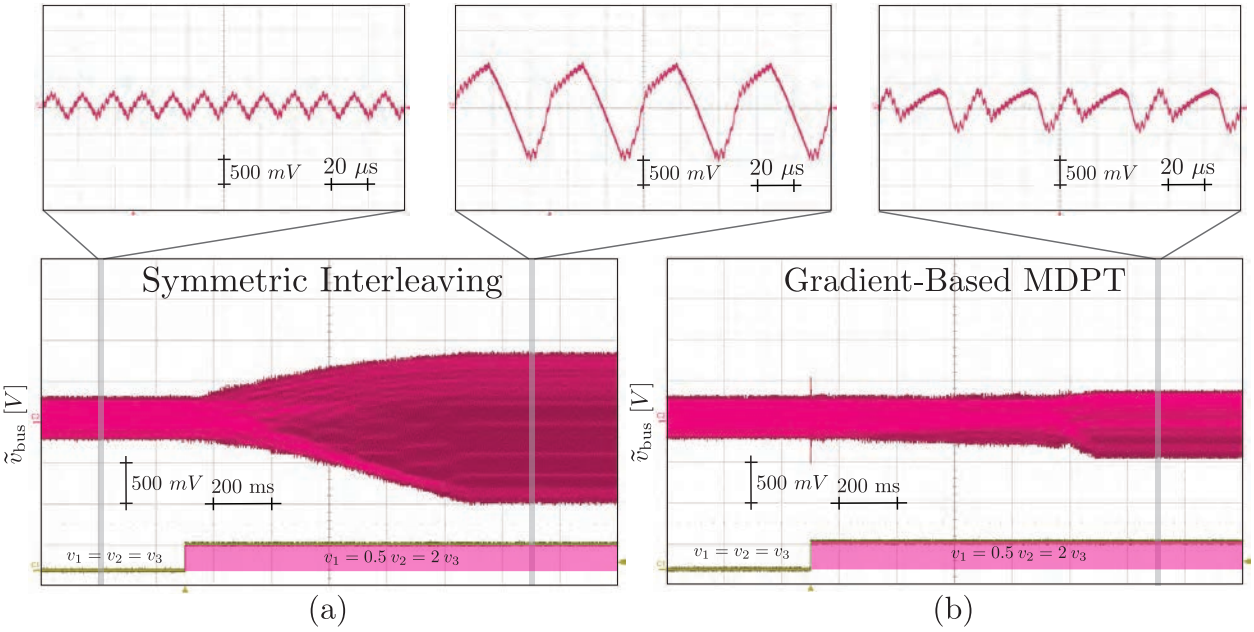


Figure 3.8: Experimental validation of the tracking capability of the gradient-based MDPT algorithm. When asymmetries in the output voltages are introduced, (a) symmetric interleaving results in a 3.28× larger peak-to-peak ripple of $\tilde{v}_{\text{bus}}$ at the worst case, while (b) the gradient-based MDPT algorithm enables ripple minimization throughout the asymmetric loading transient and results in only 1.48× larger peak-to-peak ripple of $\tilde{v}_{\text{bus}}$ at the worst case.

parameters and operating conditions as indicated in Table 3.1. We consider a static operating scenario in which $v_1 = 36\ V$, $v_2 = 24\ V$, and $v_3 = 12\ V$.

The system is initialized at the symmetric interleaved state (i.e. $\theta_{21} = 120°$ and $\theta_{31} = 240°$). We use the gradient update function in equation (3.3) to perturb $\boldsymbol{\theta}$ iteratively from the symmetric interleaved initial condition. Figure 3.6 shows the results of the numerical simulation: $\boldsymbol{\theta}$ is perturbed orthogonally to the contour lines of $\mathcal{D}$ and the algorithm converges to the MDP, in this case, at $\theta_{21} = 103°$ and $\theta_{31} = 123°$. For the particular system, $\mathcal{D}$ is reduced by 11.6 dB (14.6×) at the MDP compared to operation at the symmetric interleaved state.

3.4.2 Experimental Verification

The gradient-based MDPT algorithm is implemented on the experimental setup shown in Fig. 3.5. We introduced asymmetry in the resistive loads of each converter ($R_{\text{load},1} = 2.4\ \Omega$, $R_{\text{load},2} = 1.2\ \Omega$, and $R_{\text{load},3} = 1.2\ \Omega$) and also in the output voltages of each converter ($v_1 = 36\ V$, $v_2 = 24\ V$, and $v_3 = 12\ V$).

In the first test scenario, the system is initialized at the symmetric interleaved state, and the MDPT algorithm is turned on at $t = 0$. We observe the ac ripple component of v_{bus}, denoted $\tilde{v}_{\text{bus}}$, and also the time required for the system to reach steady state. The algorithm operates at an update rate of 2.5 kHz, eight times slower than the switching frequency of each converter. As shown in Fig. 3.7, when the algorithm is initialized $t = 0$, the magnitude of $\tilde{v}_{\text{bus}}$ begins decreasing, and after about 40 ms (100 gradient iterations), the system is at steady state. At this point, the peak-to-peak ripple of $\tilde{v}_{\text{bus}}$ is reduced 2.91× compared to the peak-to-peak ripple at the symmetric interleaved state.[1]

Second, we validated the tracking capability of the MDPT algorithm in scenarios when the converter operating condition and the MDP are changing with respect to time. In this experiment, the resistive loads of each converter are identical ($R_{\text{load},1} = R_{\text{load},2} = R_{\text{load},3} = 2.4\ \Omega$), and the output voltages are initialized identically such that $v_1 = v_2 = v_3 = 24$ V. Then, v_2 is changed linearly from 24 to 36 V at a rate of 24 V/s, while v_3 is changed linearly from 24 to 12 V at the same rate. The voltage v_1 is held constant at 24 V.

As shown in Fig. 3.8(a), when symmetric interleaving is applied to this scenario, the voltage ripple in v_{bus} is minimized when the output voltages are identical, as expected. However, when the asymmetries in the output voltages are introduced, the voltage ripple increases monotonically, and reaches a maximum when $v_2 = 36$ V and $v_3 = 12$ V. At this point, the peak-to-peak ripple of $\tilde{v}_{\text{bus}}$ is 3.28× larger than when the output voltages are identical.

When the MDPT algorithm is applied to this scenario, as shown in Fig. 3.8(b), the peak-to-peak ripple of $\tilde{v}_{\text{bus}}$ stays relatively constant, even as the asymmetries in the output voltages are introduced. At the point when $v_2 = 36$ V and $v_3 = 12$ V, the peak-to-peak ripple of $\tilde{v}_{\text{bus}}$ is only 1.48× larger than when the output voltages are identical. This translates to a 2.20× reduction in the peak-to-peak ripple at this operating point.

3.4.3 Analysis of Local Minima

As mentioned above, since equation (3.2) is non-convex, the gradient-based MDPT algorithm and the algorithm presented in Section 3.5 will track local minima of $\mathcal{D}(\boldsymbol{\theta})$ depending on the initial condition of $\boldsymbol{\theta}$. For instance, in Fig. 3.6, a second minima can be seen around

[1]The peak-to-peak voltage ripple in v_{bus} is mathematically similar to the $\mathcal{L}_\infty$-norm of $\tilde{v}_{\text{bus}}(t)$. By Parsevel's theorem and the equivalence of norms, the reductions in the square root of $\mathcal{D}$ are proportional to this peak-to-peak voltage ripple measurement by a constant scalar.

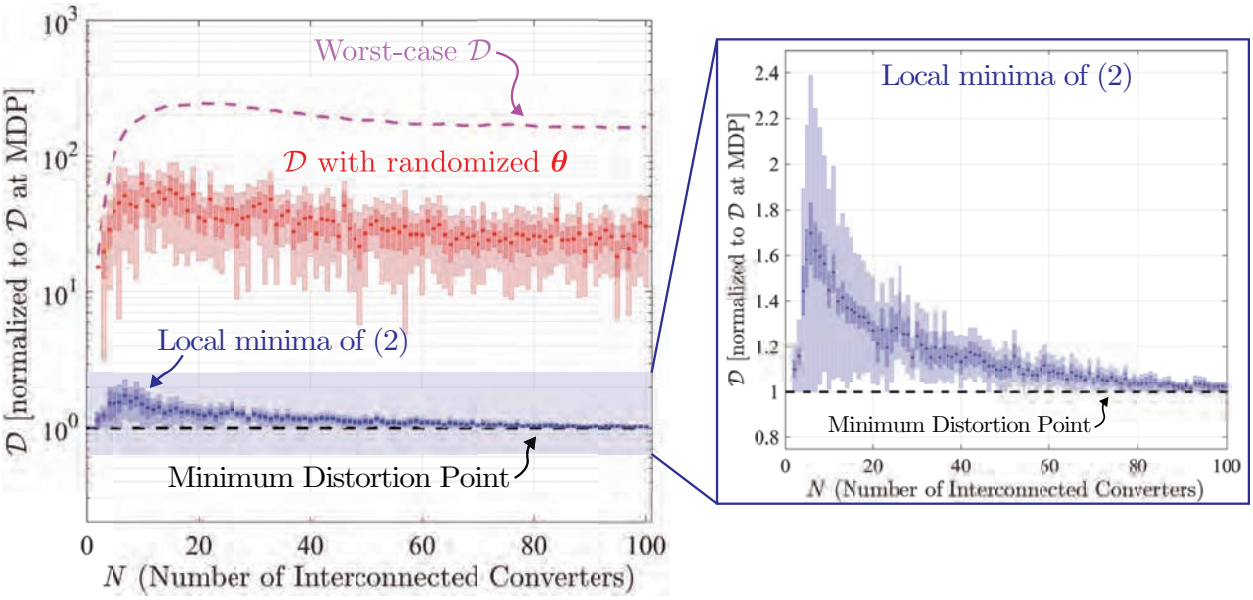


Figure 3.9: A Monte Carlo simulation that illustrates $\mathcal{D}$ obtained at the worst-case phase shifting (dashed magenta line), at a uniformly distributed random phase spacing across the N converters (red), and at various local minima of the non-convex function $\mathcal{D}(\boldsymbol{\theta})$ (blue), all normalized to $\mathcal{D}$ at the MDP, and plotted as a function of the number of interconnected power converters N. For each N, one hundred scenarios are simulated, and the 25th and 75th percentile values of $\mathcal{D}$ are shown with shaded bars.

$\theta_{21} = 275°$ and $\theta_{31} = 325°$, and if $\boldsymbol{\theta}$ were initialized closer to this region, then convergence to this suboptimal minima would be likely. Thus, it is important to study if these local minima are sufficiently 'good' as to justify the use of optimization algorithms that can only track such minima.

Towards this end, we performed another Monte Carlo simulation for analyzing the distortion $\mathcal{D}$ obtained at these local minima in relation to $\mathcal{D}$ obtained at the MDP. The setup details of the Monte Carlo simulation are identical to those in Section 3.2.4 and in Appendix B. A local minimum is identified through the selection of a uniformly distributed random initial condition. We run one hundred scenarios with the randomized inputs for each network of N interconnected power converters (Fig. 3.1). The results are shown in Fig. 3.9, where the magenta dashed line is $\mathcal{D}$ obtained at the worst-case phase shifting, the data in red is $\mathcal{D}$ obtained at the uniformly distributed random phase spacing across the N converters, and the data in blue is $\mathcal{D}$ obtained at the randomly selected local minima. The values of $\mathcal{D}$ have been normalized to the value of $\mathcal{D}$ at the MDP and plotted on a logarithmic scale. Again, the shaded regions around each data point indicate the 25th and 75th percentiles of the Monte Carlo simulation, while the dark line represents the median value.

Algorithm 2 Decentralized Nonlinear Gauss-Seidel-Based MDPT Algorithm

1: Output: Steady state minimum of equation (3.2).
2: **for** $\ell = 1$ to N **do**
3: Input: $v_{\text{bus}}, v_\ell, I_\ell, D_\ell, C_{\text{bus}}$
4: Output: Phase spacing $\theta_\ell^\star$ corresponding to the minimizer of $\mathcal{D}$
5: **repeat**
6: Assume constant $\boldsymbol{\theta}$ vector except for θ_ℓ component
7: Calculate $\mathcal{D}$ from inputs
8: Computation of $\theta_\ell^\star$ that minimizes $\mathcal{D}$
9: **until** stopping criterion is met

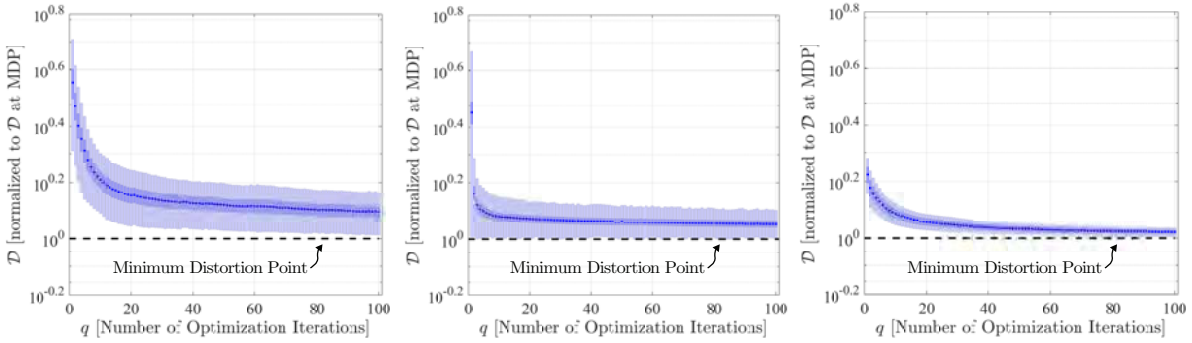
The right sub-figure illustrates a zoomed version of $\mathcal{D}$ obtained at the local minima on a linear scale in relation to $\mathcal{D}$ at the MDP.

The results indicate that for networks composed of $N < 20$ interconnected power converters, the distortion $\mathcal{D}$ obtained at local minima are generally in the range of 1 to 2.5× the distortion obtained at the MDP. This can still be considered a significant reduction, particularly in relation to $\mathcal{D}$ obtained at the worst-case phase shifting, which, for this range of network size, results in 5 to 10× higher $\mathcal{D}$ than the local minima. Interestingly, for larger networks ($N > 20$), we see that $\mathcal{D}$ obtained at local minima begin to converge to the value of $\mathcal{D}$ obtained at the MDP. Indeed, at $N = 100$, the minima are essentially identical. This is due to the fact that the degrees of freedom in the optimization problem scale linearly with the number of converters in the network. Thus, as N increases, there will be more local minima that are closer to the global minimum of equation (3.2). The analysis suggests that optimization methods that track local minima are adequate for the MDPT problem, and can be particularly effective at obtaining close-to-optimal performance when applied to larger networks.

3.5 MDPT Algorithm #2: Decentralized Nonlinear Gauss-Seidel

3.5.1 Algorithm Principles and Design

A limitation of the gradient-based MDPT algorithm is the need for information from all N converters, including output voltages, duty cycles, and average output currents. In some applications, it is desirable to have a local controller at each power converter that only samples



(a) $N = 3$ (b) $N = 20$ (c) $N = 100$

Figure 3.10: A Monte Carlo simulation that illustrates the value of $\mathcal{D}$, normalized to $\mathcal{D}$ at the MDP, obtained for q iterations of the NL-GS MDPT algorithm. As shown, the NL-GS MDPT algorithm converges asymptotically towards local minima identified in Section 3.4.3, while increasing the number of interconnected converters (N) yields a more optimal steady state solution.

and utilizes local information. These decentralized techniques have benefits in modularity, scalability, and tolerance to faults.

Here, we present an MDPT algorithm based on a decentralized nonlinear Gauss-Seidel (NL-GS) technique. Conceptually, the NL-GS MDPT algorithm minimizes equation (3.2) one 'component' at a time, where a component is the phase shift θ_ℓ of a single converter. For the ℓ^{th} converter, we calculate the $\theta_\ell^\star$ that globally minimizes $\mathcal{D}$ under the assumption that all other components of the vector $\boldsymbol{\theta}$ are constant. Because this is a one-dimensional optimization problem, it is simple to compute, and the global minimum can be obtained using a brute-force method. Note that this global minimum is different from the MDP since it constrains the other $N-1$ components of $\boldsymbol{\theta}$. By successively calculating $\theta_\ell^\star$ for all N converters and iterating the calculations, it can be proven that this successive component-wise minimization will yield convergence to a *local* minima of $\mathcal{D}$ [38]. These local minima will be identical to the minima obtained by the gradient-based MDPT algorithm, and the analysis presented in Section 3.4.3 still applies.

The local minimization of each component only requires information that can be sampled by the ℓ^{th} converter, namely $v_{\text{bus}}, v_\ell, I_\ell, D_\ell$, and C_{bus}. In this way, the algorithm can be implemented locally at each converter and requires no communication with any other controller. We assume that each converter calculates and updates its $\theta_\ell^\star$ asynchronously, which enables us to make the needed assumption that every phase shift other than θ_ℓ is constant. The experimental results that follow validate the practicality of this assumption.

Next, we perform a numerical Monte Carlo simulation to verify the operation and con-

vergence of the NL-GS MDPT algorithm. The setup details of the Monte Carlo simulation are identical to those shown previously in Sections 3.2.4 and 3.4.3. Fig. 3.10 illustrates the value of $\mathcal{D}$ obtained after q iterations of the NL-GS MDPT algorithm for $N = 3, 20$, and 100. One iteration q includes the successive calculations of $\theta_\ell^\star$ for all N converters once.

The results of the simulation demonstrate that the NL-GS MDPT algorithm indeed asymptotically converges towards the local minima identified in Section 3.4.3. Moreover, as our previous analysis indicated, the local minima of larger networks (e.g. $N = 100$) are closer to the MDP and can yield better steady state solutions. The convergence rate of the NL-GS MDPT algorithm also has a dependence on the size of the network, with smaller networks having longer convergence times to steady state, and also having larger variance in the value of $\mathcal{D}$, as indicated by the shaded regions in Fig. 3.10 indicating the 25^{th} and 75^{th} percentile values of Monte Carlo simulation. For networks of most sizes, the analysis suggests that the NL-GS MDPT algorithm will obtain an adequate solution in approximately fifty iterations.

3.5.2 Experimental Verification

We implemented the NL-GS MDPT algorithm on the experimental setup shown in Fig. 3.5. The setup is modified such that each dc-dc buck converter has a separate FPGA controller that runs Algorithm 2. The same circuit and asymmetric operating parameters from the first test in Section 3.4.2 are used, that is, $R_{\text{load},1} = 2.4\ \Omega$, $R_{\text{load},2} = 1.2\ \Omega$, and $R_{\text{load},3} = 1.2\ \Omega$ and $v_1 = 36\ V$, $v_2 = 24\ V$, and $v_3 = 12\ V$. Each converter calculates and updates it corresponding θ_ℓ at a rate of 2.5 kHz. The clocks of each controller are not synchronized with each other, and successive θ_ℓ updates are considered asynchronous due to inherent clock drift.

Again, the system is initialized at the symmetric interleaved state, and the NL-GS MDPT algorithm is turned on at $t = 0$. We observe the ac ripple component $\tilde{v}_{\text{bus}}$ in Fig. 3.11. When the algorithm is initialized $t = 0$, the peak-to-peak ripple magnitude of $\tilde{v}_{\text{bus}}$ begins decreasing. After about 30 ms (75 component-wise iterations), the system is at steady state. At this point, the peak-to-peak ripple of $\tilde{v}_{\text{bus}}$ is reduced 2.82× compared to the peak-to-peak ripple at the symmetric interleaved state.

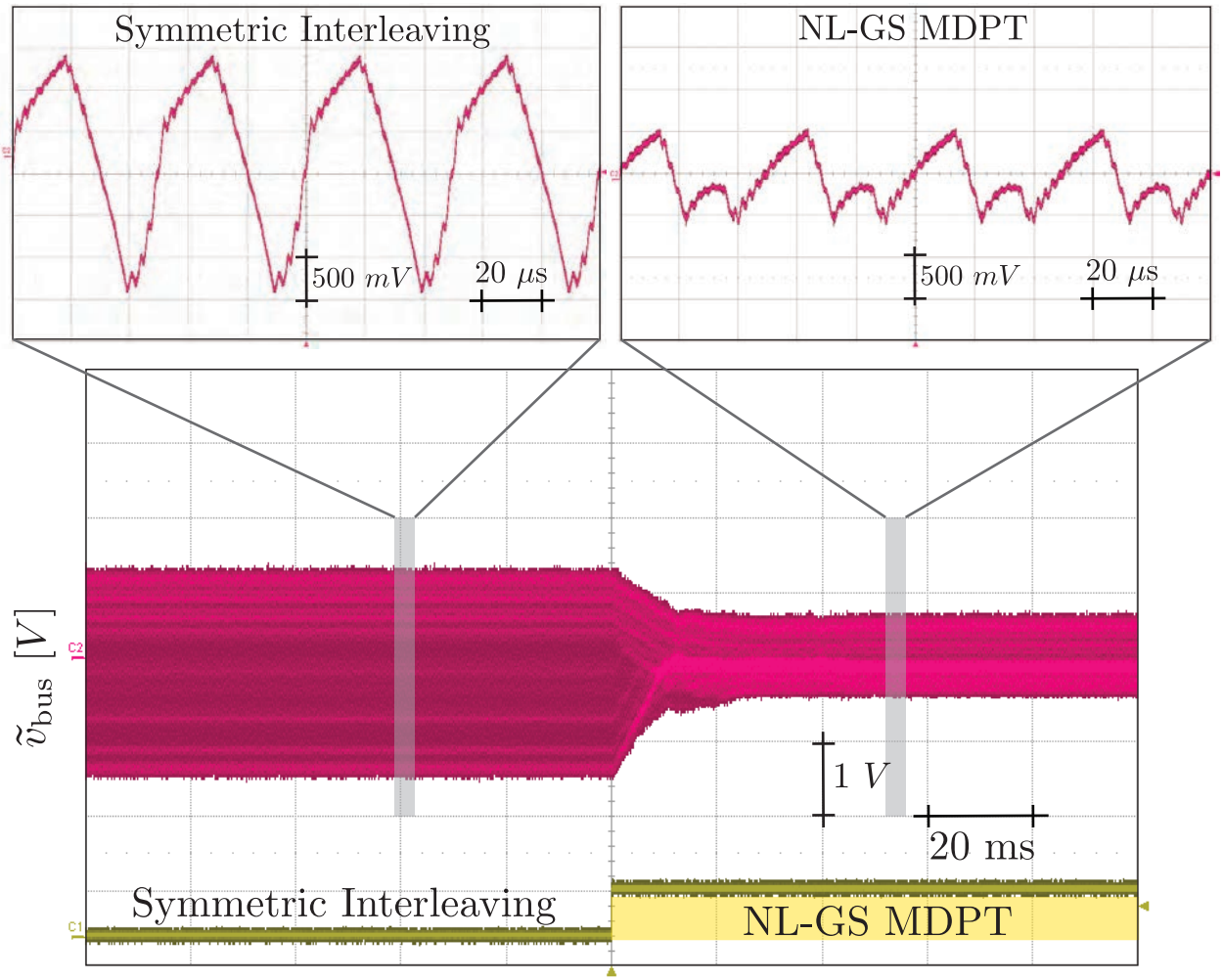


Figure 3.11: Experimental validation of the convergence speed and performance of the decentralized nonlinear Gauss-Seidel-based MDPT algorithm. As shown, the algorithm converges in approximately 75 iterations (30 ms) and enables a 2.82× reduction in the peak-to-peak ripple of $\tilde{v}_{\text{bus}}$ compared to the peak-to-peak ripple at the symmetric interleaved state.

3.6 MDPT Algorithm #3: Metaheuristic Optimizer

3.6.1 Algorithm Principles and Design

Metaheuristic optimization techniques are generally empirical in nature and do not have theoretical guarantees of convergence or optimality. However, in optimization problems with large feasible solution spaces, metaheuristics can, in some cases, find reasonably good solutions with less computational effort than a brute force search. We explore the application of metaheuristics for the MDPT problem by implementing a metaheuristic technique, specifi-

Algorithm 3 Metaheuristic Optimizer (Particle Swarm Optimizer) MDPT Algorithm

Input: $v_{\text{bus}}, v_1 \dots v_N, I_1 \dots I_N, D_1 \dots D_N, C_{\text{bus}}$
Output: Steady state minimum of equation (3.2).
Generate $\mathcal{I}$ particles of $\boldsymbol{\theta}$, $\boldsymbol{\theta}^i$, that are initialized at uniformly distributed random points within the domain $\theta_\ell \in [0, 2\pi)$
Associate velocity $\mathbf{V}^i$, personal best $\mathbf{p}^i$, velocity update rule $\boldsymbol{\mu}^i(\boldsymbol{\theta}^i, \mathbf{V}^i)$, and position update rule $\boldsymbol{\xi}^i(\boldsymbol{\theta}^i, \mathbf{V}^i)$ vectors with every i^{th} particle
repeat
    for $i = 1$ to $\mathcal{I}$ **do**
        Calculate $\mathcal{D}(\boldsymbol{\theta}^i)$ from equation (3.2)
        if $\mathcal{D} < \min(\mathbf{p}^i)$ **then**
            Update $\mathbf{p}^i$ with $\mathcal{D}$
        Update $\boldsymbol{\theta}^i$ from $\boldsymbol{\xi}^i(\boldsymbol{\theta}^i, \mathbf{V}^i)$
        Update $\mathbf{V}^i$ from $\boldsymbol{\mu}^i(\boldsymbol{\theta}^i, \mathbf{V}^i)$
until stopping criterion is met

cally the particle swarm optimization (PSO) computational method [39, 40].

A sketch of the PSO MDPT algorithm is presented in Algorithm 3. As shown, the algorithm generates $\mathcal{I}$ 'particles,' or instances, of $\boldsymbol{\theta}$, denoted as $\boldsymbol{\theta}^i$, and are initialized with a uniform random distribution. The distortion $\mathcal{D}$ is calculated at each of the $\mathcal{I}$ particles from equation (3.2). Similar to the gradient-based MDPT algorithm, this requires information from all N converters, including output voltages, duty cycles, and average output currents. Thus, unlike the NL-GS MDPT algorithm, it is not a decentralized technique. Once $\mathcal{D}$ is calculated, each particle stores the lowest $\mathcal{D}$ it has computed thus far in a 'personal best' vector $\mathbf{p}^i$. New values for $\boldsymbol{\theta}^i$ are then calculated based on 'velocity' and 'position' update rules, $\boldsymbol{\mu}^i(\boldsymbol{\theta}^i, \mathbf{V}^i)$ and $\boldsymbol{\xi}^i(\boldsymbol{\theta}^i, \mathbf{V}^i)$, respectively.

The PSO MDPT can be computational intensive since the number of evaluations of $\mathcal{D}$ scale linearly with the number of particles $\mathcal{I}$. However, increasing the number of particles is generally desirable since it increases the probability of obtaining a minimum at or close to the global minimum of the objective function and avoiding suboptimal local minima.

3.6.2 Experimental Verification

We implemented the PSO MDPT algorithm on the experimental setup shown in Fig. 3.5 with a single FPGA controller as shown. The same circuit and asymmetric operating parameters from the first test in Section 3.4.2 and Section 3.5.2 are used, that is, $R_{\text{load},1} = 2.4\ \Omega$,

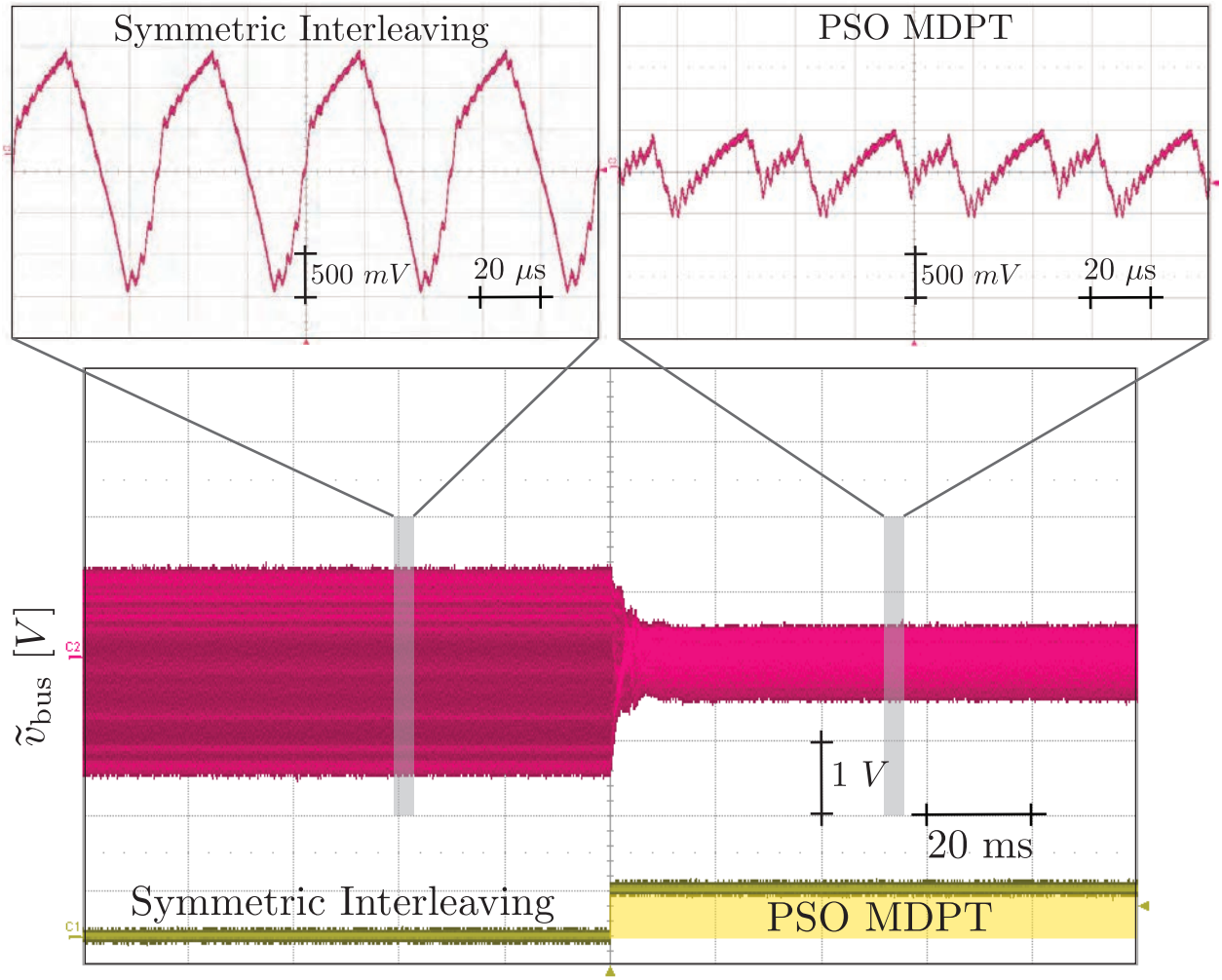


Figure 3.12: Experimental validation of the convergence speed and performance of the metaheuristic optimizer-based MDPT algorithm. As shown, the algorithm converges in approximately 12 iterations (5 ms) and enables a 3.06× reduction in the peak-to-peak ripple of $\tilde{v}_{\text{bus}}$ compared to the peak-to-peak ripple at the symmetric interleaved state.

$R_{\text{load},2} = 1.2\ \Omega$, and $R_{\text{load},3} = 1.2\ \Omega$ and $v_1 = 36\ V$, $v_2 = 24\ V$, and $v_3 = 12\ V$. The PSO algorithm is implemented with $\mathcal{I} = 128$, and updates the optimal phase spacing $\boldsymbol{\theta}^\star$ at a rate of 2.5 kHz. As shown in Fig. 3.12, the system is initialized at the symmetric interleaved state, and the PSO MDPT algorithm is turned on at $t = 0$. Within 5 ms (12 PSO iterations), a steady state value is reached where the peak-to-peak ripple of $\tilde{v}_{\text{bus}}$ is reduced 3.06× compared to the peak-to-peak ripple at the symmetric interleaved state.

Table 3.2: A quantitative comparison of the three MDPT algorithms presented in this chapter.

	Gradient-Based MDPT	NL-GS MDPT	PSO MDPT
Computational Complexity[1,2] [Slice LUT Instances/Slice Register Instances] [Percent Utilization of FPGA Resources]	483 / 137 (2.32% / 0.33%)	609 / 306 (2.93% / 0.74%)	16905 / 4795 (81.3% / 11.5%)
Convergence Speed[1,3]	40 ms (100 algorithm iterations)	30 ms (75 algorithm iterations)	5 ms (12 algorithm iterations)
Decentralized?	No	Yes	No
Minima Obtained Compared to MDP[1,4]	1.2	1.2	1.0

[1]Lower is better.
[2]For algorithm block only on Xilinx Artix-7 XC7A35T.
[3]From experimental results in Sections 3.4.2, 3.5.2, and 3.6.2.
[4]From median value of analysis in Section 3.4.3 for $N = 3$; 1.0 is optimal.

3.7 MDPT Algorithm Analysis and Trade-offs

With three candidate algorithms for MDPT presented in Sections 3.4, 3.5, and 3.6, we will now analyze the advantages and disadvantages of each, as well as discuss candidate application areas where a particular algorithm would be better suited than the others. Table 3.2 presents a comparison of the three MDPT algorithms—the gradient-based algorithm, the NL-GS algorithm, and the metaheuristic PSO algorithm—according to four performance metrics: 1) computational complexity, 2) convergence speed, 3) decentralization of control, and 4) achievable minima compared to the globally optimum MDP.

First, we analyze the computational complexity of each of the algorithms. To quantify this, we refer to the slice lookup table (LUT) instances and slice register instances used by the algorithm on the Xilinx Artix-7 XC7A35T FPGA. The XC7A35T contains 20800 slice LUTs and 41600 slice registers. Of the three algorithms, the gradient-based MDPT algorithm has the lowest complexity, utilizing only 2.32% of the slice LUTs and 0.33% of the slice registers. The NL-GS MDPT algorithm has slightly higher complexity; however, a key difference is that the NL-GS MDPT algorithm requires an FPGA for *each* of the N power converters. The PSO-based MDPT algorithm is by far the most computationally complex of the three algorithms, requiring 81.3% of the slice LUTs and 11.5% of the slice registers. While the PSO algorithm itself is simple to implement in principle and also practically on an FPGA, the large number of computations make the algorithm resource intensive. In particular, the number of evaluations of $\mathcal{D}$ scale linearly with the number of particles $\mathcal{I}$ to evaluate. Thus, a trade-off between resource utilization and algorithm performance is necessary, since more particles will improve the optimality of the algorithm. Here, we conclude that for resource-constrained computational systems, the gradient-based and NL-GS MDPT algorithms are most attractive, while the PSO MDPT algorithm is better suited to high performance computational systems and networks with lower N.

The second metric we compare is the convergence speed of each algorithm to steady state. We reference the experimental results obtained in Sections 3.4.2, 3.5.2, and 3.6.2 that verified the convergence of each algorithm when initialized from the symmetric interleaved state for a particular system asymmetry. The gradient-based MDPT algorithm has the slowest convergence rate, requiring 100 algorithm iterations to converge. As discussed, the scalar value κ in equation (3.3) dictates the numerical stability and convergence speed. Here, κ was selected to maximize the convergence speed while ensuring numerical stability over a wide operating range. Note that similar Newton's method techniques, such as the secant method,

may provide improvements in convergence speed and stability for gradient-type algorithms. The NL-GS MDPT algorithm provides moderate improvements in convergence speed compared to the gradient-based MDPT algorithm, but is similarly limited in performance since each calculation only perturbs a single component (i.e. one dimension of $\boldsymbol{\theta}$) at a time. The PSO MDPT algorithm has the fastest convergence speed, requiring only 12 algorithm iterations to achieve steady state. This can be attributed to the nature of the metaheuristic optimization, which does not perturb $\boldsymbol{\theta}$ smoothly, but can instantaneously shift $\boldsymbol{\theta}$ to a more optimal point in the feasible search space.

Third, we compare the centralized or decentralized nature of each algorithm. Both the gradient-based and PSO MDPT algorithms are centralized; that is, they required information from all N converters, including output voltages, duty cycles, and average output currents. While this may be practical in some applications, such as in point-of-load converters and on-die power conversion, it is unrealistic in others, such as in microgrids and building power distribution networks. The spatially distributed nature of these latter applications make it challenging to communicate information in real-time to a centralized controller. Moreover, this centralized controller introduces a single point of failure in the system. To overcome these limitations, the NL-GS MDPT algorithm offers a decentralized approach that only requires information that is local to each power converter. Thus, for applications that are inherently spatially separated or that require high degrees of scalability, modularity, or fault tolerance, the NL-GS MDPT algorithm offers compelling benefits.

The last metric we compare is the steady state minima obtained by each algorithm compared to the MDP. As discussed previously, both the gradient-method and NL-GS MDPT algorithms converge to *local* minima of $\mathcal{D}$. Analysis of these minima were presented in detail in Section 3.4.3. For networks of size $N = 3$, it was shown that the minimum $\mathcal{D}$ obtained by the algorithms is, on average, approximately 1.2× higher than the value of $\mathcal{D}$ at the MDP. While this still represents a significant reduction in relation to $\mathcal{D}$ obtained at the worst-case phase shifting, the analysis indicated that these local minima are generally in the range of 1 to 2.5× the distortion obtained at the MDP depending on the size of the network, with larger networks converging towards 1×. Here, the PSO-based MDPT algorithm has a key advantage in that, due to the stochastic nature of particle position and velocity, it is significantly less likely to become trapped in local minima. Moreover, increasing the number of particles enables faster identification of solutions that are, in practice, identical to the MDP. However, since the PSO-based MDPT algorithm (or most metaheuristic optimization techniques in general) does not have theoretical guarantees of stability or convergence to

a global minimum, and numerical simulations should be used to verify performance and convergence under expected operating conditions.

3.8 Summary

We have introduced the notion of *Minimum Distortion Point Tracking* (MDPT) as a means to optimally minimize distortion in networks of series- or -parallel connected dc-dc converters. Our analysis for networks of up to one hundred interconnected power converters indicated that a one to two order of magnitude reduction (-14 dB to -22 dB) in distortion power is possible when operating at the Minimum Distortion Point (MDP), resulting in reduced aggregate ripple. We presented and experimentally verified algorithms that can dynamically solve the MDPT optimization problem. The three algorithms—based on the gradient method, the nonlinear Gauss-Seidel method, and a metaheuristic optimizer—each have unique properties that make them well-suited for a variety of diverse applications. Practically, MDPT can enable improvements in power quality and reductions in filter requirements (and subsequent volume) for a broad array of use cases, including point-of-load conversion systems, dc microgrids, and power management integrated circuits.

Chapter 4

Architectures for Decentralized Control

This chapter presents a decentralized control strategy that yields symmetric switch interleaving for parallel-connected dc-dc buck converters. The contributions of this chapter aim to address the second limitation of existing symmetric interleaving methods discussed in Chapter 2, namely, the need for centralized control and/or communication. Compared to such state-of-the-art methods that are distributed at best, the proposed architecture requires no communication and hence presents a variety of advantages with regard to reliability, modularity, and cost. The method is based on the digital implementation of the dynamics of a Liénard-type oscillator circuit as the controller for the converters. Each controller only requires the locally measured output current to synthesize the pulse width modulation (PWM) carrier waveform. The intrinsic electrical coupling between converters drives the nonlinear oscillator-based controllers to converge to an interleaved state with uniform phase-spacing across PWM carriers, independent of the number of converters, the load, and initial conditions. We provide analytical guarantees for existence and stability of the interleaved state as well as extensive hardware results for a system of five 120 W, 48 V to 12 V dc-dc buck converters that demonstrate convergence to the interleaved state in the face of a variety of large-signal disturbances.

4.1 Overview of Interleaving

We present a decentralized switch-interleaving control strategy for multiphase dc-dc buck converters serving a common load. The architecture presents no single point of failure and requires no communication between the converters. The proposed controller is grounded on the dynamics of a type of nonlinear oscillator, engineered such that the interleaved state is characterized by the minimum stored energy in a collection of such nonlinear oscillators. Convergence to the interleaved state is spontaneously driven by the intrinsic interconnection of the underlying nonlinear dynamical systems through the electrical network and without the need for an explicit communication bus. In addition to establishing analytical guarantees for convergence and stability, we provide experimental results for a parallel connected buck converter setup to validate the concept.

Decentralized interleaving realizes all the benefits of multiphase dc-dc converter systems mentioned previously, with the bonus that interleaving can be guaranteed with no single point of failure and independent of load fluctuations and initial conditions. Furthermore, the decentralized nature of the proposed controller enables a decoupling of the real-time interleaving operation from supervisory-level routines such as droop control or phase shedding which can then be realized with low-bandwidth signals during normal operation.

Nonlinear oscillator dynamics form the basis of the proposed control strategy. In particular, we program the discretized second-order dynamics of a particular type of nonlinear oscillator—called the Liénard oscillator—on the digital controller of each converter. The locally measured inductor current for each converter acts as an input to the oscillator, and the oscillator dynamical states are used to generate the corresponding triangular PWM carrier (see Fig. 4.1 for details). Liénard oscillator dynamics have been examined in a variety of scientific and engineering disciplines [41]. Tangentially related to the application at hand, they have been used to realize decentralized real-time synchronization of ac voltages for inverters in microgrids [42, 43, 44, 45, 46], adaptive synchronization of grid-connected three-phase inverters [47], and carrier wave synchronization for three-phase parallel-connected inverters to suppress circulating currents [48]. While these studies examined *synchronization* of waveforms in the context of *ac* systems, here, we focus on the dual problem of *interleaving* PWM waveforms for *dc* systems. Theoretical foundations for this work are grounded on passivity-based frameworks to examine the networked dynamics of nonlinear oscillators. This is an expansive research topic, see, e.g., [49, 50, 51, 52, 53].

The theoretical and experimental results in this chapter are presented with buck convert-

ers serving as the topology of choice in the parallel-connected multiphase system. However, it must be noted that the analytical approach and feedback-synthesis method developed here can conceivably be applied to other converter topologies and network architectures. Focusing on the application at hand, while the proposed nonlinear controllers generate the interleaved PWM carriers, we leverage outer-loop droop controllers to ensure decentralized proportional power sharing [16]. From a theoretical vantage point, the main contribution of this chapter is to establish analytical guarantees for the existence and stability of the interleaved solutions. To that end, we build a model for the parallel-connected converter system based on the collective dynamics of the oscillators, buck converters, and the electrical network. Then, we leverage a coordinate transformation of the system dynamics to polar coordinates to extract amplitude and phase information of the PWM waveforms. Following this, we enumerate and discuss the stability of equilibria that result from the involved dynamics.

This chapter builds on our preliminary work in [54], where a similar feedback strategy was validated with numerical simulations for an idealized setup involving an ideal voltage-source load. Here, we provide several extensions with regard to both theory and application. First, we propose an alternative to an acausal derivative term that was a part of the feedback strategy in [54]. Furthermore, we generalize the load model from an ideal voltage source to a more realistic *RC* load behind a Thévenin resistance. Patently, the most significant contribution over [54] is experimental validation of the proposed control strategy on a hardware testbed comprising five identical 48 V to 12 V buck converters rated at 120 W switching at 20 kHz. Experimental results demonstrate spontaneous convergence to the interleaved state through a variety of large-signal disturbances including: startup from arbitrary initial conditions, load steps, and converter addition. While the analysis considers an ideal, symmetric, and uniform setting with equal dc-bus voltages and equal values for filter elements, the exhaustive experimental validation establishes robustness of the control strategy to parasitics, and parametric and input variations that are inescapable in any hardware implementation.

The remainder of this chapter is organized as follows. Section 4.2 develops a model for the system of buck converters. Building upon that, we establish the nature and stability of solutions in Section 4.3. We validate our analysis using a hardware prototype that implements our controller for parallel-connected buck converters in Section 4.4. Finally, we summarize the chapter in Section 4.5 by providing a few key directions for future work.

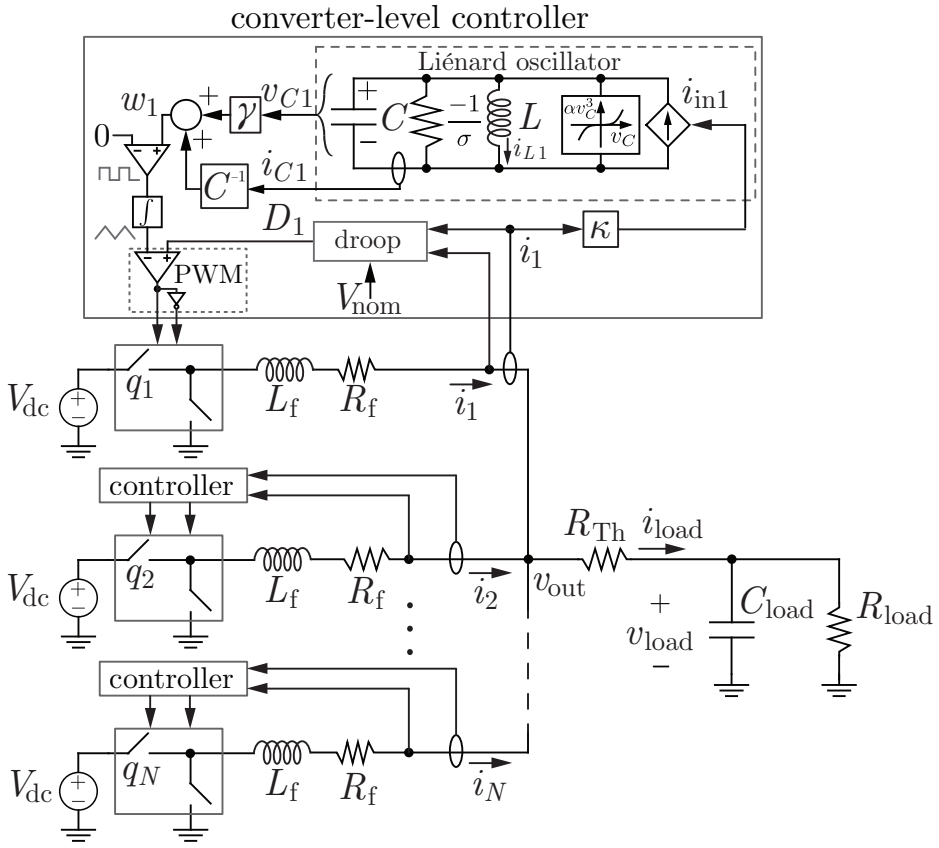


Figure 4.1: System of parallel-connected buck converters with local controllers. The proposed controller has the dynamics of a nonlinear Liénard-type oscillator circuit which takes the converter output current as feedback and generates the triangular PWM carrier at each converter by using a linear combination of its states. Droop control ensures decentralized power sharing.

4.2 System Description and Modeling

In this section, we describe the model of the oscillator-controlled dc-dc buck converters that are connected in parallel and are supplying a common load. Using circuit laws and dynamics of the oscillators, we derive a coupled-oscillator model and then transform it to polar coordinates to extract phase information of the PWM waveforms.

4.2.1 Controller Description

The system architecture is illustrated in Fig. 4.1. It is composed of N parallel dc-dc buck converters indexed in the set $\mathcal{N}$ supplying a common load. The controller for each converter, labeled *converter-level controller* for the first converter and simply as *controller* for the others, is decentralized and composed of two parts: i) a discretized version of the second-order

differential equation which describes Liénard-type oscillators, labeled as *Liénard oscillator* for the first converter, that is responsible for switch interleaving, and ii) a slower-timescale droop-control-based voltage-regulation method, labeled as *droop* for the first converter.

The virtual-oscillator inductor and capacitor, L and C, are selected such that the oscillator resonant frequency coincides with the switching frequency $\omega_{\rm sw} = 1/\sqrt{LC}$ (the switching period is denoted by $T_{\rm sw} = 2\pi/\omega_{\rm sw}$). Furthermore, a high Q oscillator ensures that the j-th oscillator voltage, $v_{Cj}(t)$, will be nearly sinusoidal [43]. The oscillator further consists of a negative conductance, $-\sigma$, and a voltage dependent current source, αv_{Cj}^3, where $\alpha \in \mathbb{R}$ is a positive real constant. Next, the j-th comparator and integrator act on a scaled sum of $v_{Cj}(t)$ and $i_{Cj}(t)$ to yield the PWM carrier (the comparator creates a square wave and the integrator produces the carrier). Lastly, the switch pulses are generated in a typical fashion where the carrier and duty ratio, D_j, are fed to a comparator and associated logic. This proposed structure for carrier generation is independent of the controller that governs the duty ratio. The outer-loop controller that generates the duty ratio runs on a much slower time scale. Here, we consider a prototypical droop controller that yields the duty ratio for each converter. Each converter has an inductive output filter $L_{\rm f}$ with parasitic resistance, $R_{\rm f}$, and dc input voltage, $V_{\rm dc}$. The load is modeled as a parallel combination of a resistor, $R_{\rm load}$, and a capacitor, $C_{\rm load}$, behind a Thévenin resistance, $R_{\rm Th}$.

4.2.2 Parallel-converter System Model in Polar Coordinates

To analyze interleaving, it is necessary to describe the evolution of the phases corresponding to the switching signals of the converters controlled as shown in Fig. 4.1. Kirchhoff's laws yield the following dynamics for the inductor current, i_{Lj}, and capacitor voltage, v_{Cj}, for the j-th oscillator in each controller:

$$L\frac{di_{Lj}}{dt} = v_{Cj}, \quad C\frac{dv_{Cj}}{dt} = (\sigma v_{Cj} - \alpha v_{Cj}^3) - i_{Lj} + i_{{\rm in}j}. \tag{4.1}$$

Above, $i_{{\rm in}j}$ denotes the input current that serves as feedback to the oscillator. (See Fig. 4.1.) Defining $\varepsilon := \sqrt{L/C}$, $x_j := \varepsilon i_{Lj}$, and $y_j := v_{Cj}$, the above dynamics can be rewritten as

$$\dot{x}_j = \omega_{\rm sw} y_j, \quad \dot{y}_j = -\omega_{\rm sw} x_j + \varepsilon\left(\sigma y_j - \alpha y_j^3\right) + \varepsilon i_{{\rm in}j}. \tag{4.2}$$

To extract the phase dynamics, we define the amplitude and instantaneous phase angle corresponding to (4.2) as below:

$$r_j = \sqrt{x_j^2 + y_j^2}, \quad \phi_j = \arctan\left(\frac{x_j}{y_j}\right). \tag{4.3}$$

To simplify analysis, we will focus on the phase-angle offset $\theta_j = \phi_j - \omega_{\text{sw}} t$, which quantifies the angle difference with respect to a nominal reference frame rotating at the switching frequency, ω_{sw}. Algebraic and trigonometric manipulations applied to (4.2) yield the following amplitude and phase-offset dynamics:

$$\begin{aligned}
\dot{r}_j &= \varepsilon\omega_{\text{sw}}\sigma r_j \cos^2(\omega_{\text{sw}} t + \theta_j) - \varepsilon\omega_{\text{sw}}\alpha r_j^3 \cos^4(\omega_{\text{sw}} t + \theta_j) \\
&\quad + \varepsilon\omega_{\text{sw}} i_{\text{in}j} \cos(\omega_{\text{sw}} t + \theta_j), \\
\dot{\theta}_j &= -\frac{\varepsilon\omega_{\text{sw}}}{2}\left(\sigma - \alpha r_j^2 \cos^2(\omega_{\text{sw}} t + \theta_j)\right) \sin(2\omega_{\text{sw}} t + 2\theta_j) \\
&\quad - \frac{\varepsilon\omega_{\text{sw}}}{r_j} i_{\text{in}j} \sin(\omega_{\text{sw}} t + \theta_j).
\end{aligned} \tag{4.4}$$

Given that (4.4) is time varying, it is difficult to analyze. We average it over one switch cycle to obtain the following averaged model:[1]

$$\begin{aligned}
\dot{\overline{r}}_j &= \frac{\varepsilon\omega_{\text{sw}}}{2}\left(\sigma\overline{r}_j - 3\alpha\overline{r}_j^3\right) + \frac{\varepsilon\omega_{\text{sw}}^2}{2\pi}\int_0^{T_{\text{sw}}} i_{\text{in}j}\cos(\omega_{\text{sw}} t + \overline{\theta}_j)dt, \\
\dot{\overline{\theta}}_j &= -\frac{\varepsilon\omega_{\text{sw}}^2}{2\pi\overline{r}_j}\int_0^{T_{\text{sw}}} i_{\text{in}j}\sin(\omega_{\text{sw}} t + \overline{\theta}_j)dt,
\end{aligned} \tag{4.5}$$

where $\overline{r}_j$, $\overline{\theta}_j$ are the averaged states. The derivation of (4.5) uses integration by parts and ignores second order (i.e., $\mathcal{O}(\varepsilon^2)$) terms (see [56] for details on a similar proof for a different application). Furthermore, it can be shown that in the parametric regime $\varepsilon \ll 1$ where waveforms are sinusoidal, the original oscillator dynamics can be approximated by the averaged model with $\mathcal{O}(\varepsilon)$ error [55, 56, 46, 57].

4.2.3 Feedback and Coupled-oscillator Dynamical Model

The feedback for the oscillators is through the current $i_{\text{in}j}$, which, as shown in Fig. 4.1, is constructed as follows:

$$i_{\text{in}j} = \kappa i_j, \tag{4.6}$$

[1]For a time-varying dynamical system $\dot{x} = \varepsilon f(x,t,\varepsilon)$ where vector field $f(x,t,\varepsilon)$ is time periodic with period $T > 0$ (i.e., $f(x,t,\varepsilon) = f(x,t+T,\varepsilon)$), and $0 < \varepsilon \ll 1$, the associated *time-averaged dynamical system* is given by $\dot{\overline{x}} = \varepsilon\overline{f}(\overline{x}) = \varepsilon\frac{1}{T}\int_{\tau=0}^{T} f(\overline{x},\tau,0)d\tau$. The solution of the averaged system is $\mathcal{O}(\varepsilon)$ *close* to the solution of the original system, i.e., $||x(t,\varepsilon) - \overline{x}(\varepsilon t)||_2 = \mathcal{O}(\varepsilon), \quad \forall t \in [0, t^*]$, for some $t^* > 0$ for which unique solutions exist for both systems and assuming $||x(0,\varepsilon) - \overline{x}(0)||_2 = \mathcal{O}(\varepsilon)$ [55].

where $\kappa > 0$ is a feedback gain and i_j is the output current of the buck converter. Furthermore, the signal used to generate the PWM carrier wave, w_j, is built as the following linear combination of the virtual-oscillator dynamic states:

$$w_j = \frac{1}{C} i_{Cj} + \gamma v_{Cj}, \tag{4.7}$$

where

$$\gamma := \frac{R_\mathrm{f}}{L_\mathrm{f}}. \tag{4.8}$$

It turns out that the above strategy is equivalent to constructing the feedback as:

$$i_{\mathrm{in}j} = \kappa \left(\gamma i_j + \frac{di_j}{dt} \right), \tag{4.9}$$

with the PWM carrier wave picked to be the virtual-capacitor voltage and the coefficient of nonlinearity for the voltage-dependent current source in the oscillator accordingly rescaled as follows:

$$w_j = v_{Cj}, \quad \alpha' = \frac{\alpha}{\sqrt{\omega_\mathrm{sw}^2 + \gamma^2}}. \tag{4.10}$$

For subsequent developments we transition to work in this equivalent system for analytical convenience since the feedback in (4.9) brings forth the coupling between the oscillators (see (D.2)). However, while the feedback and PWM carrier wave generation through (4.9)–(4.10) facilitate analysis, they involve an acausal derivative term that challenges implementation. Therefore, the hardware implementation is built with the priorly introduced feedback and PWM carrier wave generation method in (4.6)–(4.7). We prove the equivalence of (4.6)–(4.7) and (4.9)–(4.10) in Appendix C.

The duty-ratio commands for the individual oscillators are generated using droop control. The droop relation for the jth buck converter yields the following voltage reference:

$$V_{\mathrm{ref}j} = V_\mathrm{nom} - m i_j, \tag{4.11}$$

where $m > 0$ is the droop slope, and V_nom is the nominal output voltage. The buck converter achieves the target voltage ($V_{\mathrm{ref}j}$) through a proportional-integral (PI) regulator with a feedthrough term. In particular, the duty cycle is governed by

$$V_\mathrm{dc} D_j = k_p \left(V_{\mathrm{ref}j} - v_\mathrm{out} \right) + \int k_i \left(V_{\mathrm{ref}j} - v_\mathrm{out} \right) dt + V_{\mathrm{ref}j}, \tag{4.12}$$

where k_p and k_i are the proportional and integral gains respectively, and v_out is the output voltage (see Fig. 4.1). In typical implementations, k_p and k_i are picked so that the duty-ratio commands vary on a much slower timescale in comparison to the switching period [16].

A variety of other advanced outer-loop control techniques have been proposed in the literature that improve attributes such as transiest response, current distribution, and output-voltage regulation [58, 59]. Along these lines, accurate current sharing is critical in multiphase architectures since it can prevent inductor saturation and limit thermal stress [60]. With that being said, our approach to interleaving the switching waveforms is decoupled from—and hence agnostic to—outer-loop control strategies; in this work, we adopt the classical droop-control strategy discussed above without loss of generality.

With the feedback strategy adopted in (4.6)–(4.7), and droop control for generating the duty cycle shown in (4.12), it emerges that the dynamics in (4.5) boil down to the following:

$$\begin{aligned}\dot{\overline{r}}_j &= h_j(\overline{r}_j) \;\; - \varepsilon\omega_{\rm sw} R_{\rm Th}\sqrt{\xi^2+\chi^2}\sum_{k=1}^{N}\zeta_k\cos(\overline{\theta}_{jk}+\delta),\\ \dot{\overline{\theta}}_j &= \frac{\varepsilon\omega_{\rm sw}R_{\rm Th}\sqrt{\xi^2+\chi^2}}{\overline{r}_j}\sum_{k=1}^{N}\zeta_k\sin(\overline{\theta}_{jk}+\delta),\end{aligned} \tag{4.13}$$

where we define $\overline{\theta}_{jk} := \overline{\theta}_j - \overline{\theta}_k$, and

$$\zeta_j := \frac{V_{\rm dc}\sin(D_j\pi)\kappa}{\pi L_{\rm f}}\frac{L_{\rm f}^2}{(\omega_{\rm sw}L_{\rm f})^2+R_{\rm f}^2}, \tag{4.14}$$

$$h_j(\overline{r}_j) := \frac{\varepsilon\omega_{\rm sw}}{2}\left(\sigma\overline{r}_j - 3\alpha\overline{r}_j^3 + 2\zeta_j\right), \tag{4.15}$$

$$\xi := \frac{\psi_1\left(1+\eta\right)^{-1}}{\omega_{\rm sw}L_{\rm f}\left(1-\psi_1\left(1+\eta\right)^{-1}\psi_2\right)}, \tag{4.16}$$

$$\chi := \frac{\left(1-\eta\right)^{-1}}{\omega_{\rm sw}L_{\rm f}\left(1-\psi_1\left(1+\eta\right)^{-1}\psi_2\right)}, \tag{4.17}$$

$$\delta := \sin^{-1}\left(\frac{\xi}{\sqrt{\xi^2+\chi^2}}\right), \tag{4.18}$$

with η, ψ_1, and ψ_2 given by:

$$\eta := \left(1-\frac{1}{\omega_{\rm sw}^2 R_{\rm load}C_{\rm load}}\right)^{-1}\frac{N}{\omega_{\rm sw}^2 C_{\rm load}L_{\rm f}}, \tag{4.19}$$

$$\psi_1 := \frac{R_{\rm f}+NR_{\rm Th}}{\omega_{\rm sw}L_{\rm f}} - \frac{\eta}{\omega_{\rm sw}R_{\rm load}C_{\rm load}}, \tag{4.20}$$

$$\psi_2 := -\frac{R_{\rm f}+NR_{\rm Th}+NR_{\rm load}}{\omega_{\rm sw}L_{\rm f}} + \eta\omega_{\rm sw}R_{\rm load}C_{\rm load}. \tag{4.21}$$

The derivation of the model in (4.13) hinges on the equivalence between the feedback and PWM carrier wave construction in (4.6)–(4.7) to that in (4.9)–(4.10) as shown in Appendix C.

Building on this, we use integration by parts and a suite of circuit-theoretic notions including: i) Kirchhoff's voltage law to describe the network dynamics, ii) dynamics of the load voltage, iii) a Fourier-series representation of the switching signal, and iv) the input-output behavior of the dc-dc buck converters to arrive at (4.13). A sketch of this derivation is provided in Appendix D.

4.3 Equilibria and Stability

In this section, we enumerate different equilibria that result from the collective dynamics in (4.13) and comment on the stability of each. To that end, we will first establish a dynamical model that collects and compactly represents all the individual oscillator dynamics in (4.13).

To evaluate stability of different equilibria, we make the assumption that $D_j = D_k,\ \forall j, k \in \mathcal{N}$, which is true in the averaged sense and for time horizons pertinent to stability analysis of the interleaved state. From (4.14), we see that this implies $\zeta_j = \zeta_k =: \zeta,\ \forall j, k \in \mathcal{N}$, which further renders $h_j(\overline{r}_j) =: h(\overline{r}_j),\ \forall j \in \mathcal{N}$. Furthermore, we also assume $\delta = 0$, which translates to an ideal setup where the Thévenin resistance on the load side is negligibly small, and the switching frequency is high (see (4.18)). With these assumptions in place, the dynamics (4.13) can be compactly and collectively expressed as:

$$\dot{\overline{r}} = H - \rho C 1_N\,, \quad \dot{\overline{\theta}} = \rho R^{-1}\ S 1_N, \tag{4.22}$$

where $\overline{r} = [\overline{r}_1, \ldots, \overline{r}_N]^{\mathrm{T}}$, $\overline{\theta} = [\overline{\theta}_1, \ldots, \overline{\theta}_N]^{\mathrm{T}}$, and $H \in \mathbb{R}^N$, $N \times N$ real matrices R, C, S, and $\rho\ \in \mathbb{R}$ are given by:

$$[H]_j = h(\overline{r}_j), \quad R = \mathrm{diag}\{\overline{r}\}\,, \tag{4.23}$$

$$[C]_{j\ell} = \cos(\overline{\theta}_{jl}), \quad [S]_{j\ell} = \sin(\overline{\theta}_{jl})\,, \tag{4.24}$$

$$\rho = \varepsilon \omega_{\mathrm{sw}} R_{\mathrm{Th}} \zeta \sqrt{\xi^2 + \chi^2}. \tag{4.25}$$

To clarify the notation above, $[X]_{jk}$ represents the entry in the jth row and kth column of matrix X; for vector x, $\mathrm{diag}\{x\}$ denotes the diagonal matrix obtained by stacking elements of x on the main diagonal; and 1_N denotes the length-N vector with all ones.

Notice that the phase dynamics in (4.22) are not defined for $\overline{r}_j = 0$; and indeed, the very notion of a radius is ill-posed when $\overline{r}_j \leq 0$. Hence, we first establish conditions such that the radii remain greater than zero. In particular, when the number of oscillators are upper bounded as follows:

$$N < \frac{1}{R_{\mathrm{Th}} \sqrt{\xi^2 + \chi^2}}, \tag{4.26}$$

the set

$$\mathcal{I} := \{(\overline{r}, \overline{\theta}) \in \mathbb{R}^N_{\geq 0} \times \mathbb{T}^N : \overline{r}_j > 0, \forall j \in \mathcal{N}\}, \tag{4.27}$$

where $\mathbb{T}^N$ denotes the N-dimensional torus is positively invariant with the designed feedback (4.6). To see this, consider that from the amplitude dynamics in (4.22) we get:

$$\begin{aligned} \dot{\overline{r}}_j &= \varepsilon\omega_{\text{sw}} \left(\frac{\sigma\overline{r}_j - \alpha\overline{r}_j^3}{2} + \zeta - R_{\text{Th}}\sqrt{\xi^2+\chi^2} \sum_{k=1}^{N} \zeta \cos(\overline{\theta}_{jk}) \right) \\ &\geq \frac{\varepsilon\omega_{\text{sw}}}{2} \left(\sigma\overline{r}_j - \alpha\overline{r}_j^3\right) + \varepsilon\omega_{\text{sw}}\zeta \left(1 - NR_{\text{Th}}\sqrt{\xi^2+\chi^2}\right). \end{aligned} \tag{4.28}$$

So, if (4.26) holds then

$$\dot{\overline{r}}_j \geq \frac{\varepsilon\omega_{\text{sw}}}{2} \left(\sigma\overline{r}_j - \alpha\overline{r}_j^3\right) + r_\circ, \tag{4.29}$$

where $r_\circ$ is a positive constant. Clearly $\forall\ \overline{r}_j < \sqrt{\sigma/\alpha}$, $\dot{\overline{r}}_j > 0$, which renders $\mathcal{I}$ to be positively invariant.

From the above discussion, we can conclude that R has all positive entries. At equilibrium, where $\dot{\overline{\theta}} = 0_N$ (0_N denotes the length-N vector with all zeros), we have from (4.22) that

$$S1_N = 0_N. \tag{4.30}$$

Given the definition of matrix S in (4.24), one can identify different types of equilibria that satisfy the constraint in (4.30) (sketched on the phase plane in Fig. 4.2): a) bi-cluster synchronous state, b) phase-synchronous state, c) generalized interleaved state, and d) symmetric-interleaved state: the desired state where the phases of the PWM carriers are uniformly spaced apart. We formally define and study these next, and in each case, we *validate* that the phases indeed satisfy the constraint for equilibria, namely (4.30). We also comment on the *stability* of each.

4.3.1 Bi-cluster Synchronous State

The coupled system is said to be in the bi-cluster synchronous state if the phases evolve as

$$\overline{\theta}_j - \overline{\theta}_k = m\pi,\ \forall j, k \in \mathcal{N}, \forall m \in \mathbb{Z}. \tag{4.31}$$

The bi-cluster synchronous state is illustrated in Fig. 4.2(a).

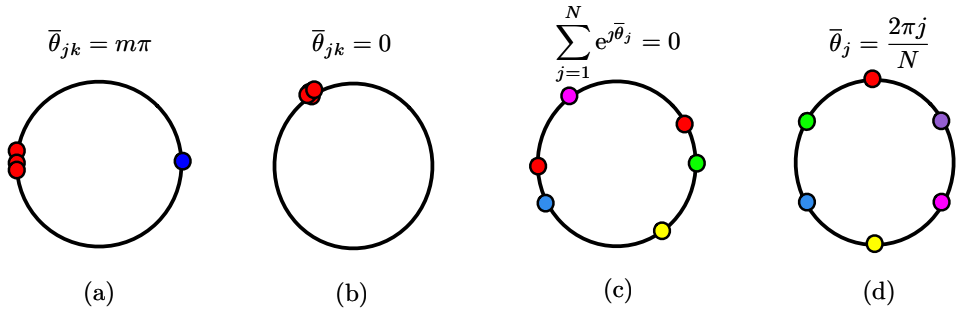


Figure 4.2: Equilibria for the coupled oscillator dynamics (4.22): a) bi-cluster synchronous state, b) phase-synchronous state, c) generalized interleaved state, and d) symmetric-interleaved state. Recall that $\overline{\theta}_j$ is the averaged phase-angle offset (with respect to a nominal reference frame rotating at the switching frequency) corresponding to the voltage of the virtual capacitor, v_{Cj} (and hence of its corresponding carrier waveform) for the j-th oscillator. Furthermore, $\overline{\theta}_{jk} = \overline{\theta}_j - \overline{\theta}_k$.

4.3.1.1 Validity

To see that this is indeed an equilibrium, note from (4.24) that $[S]_{j\ell} = \sin(\overline{\theta}_{jl}) = 0$, $\forall j, k \in \mathcal{N}$ when $\overline{\theta}_j - \overline{\theta}_k = m\pi$, $\forall m \in \mathbb{Z}$. This further implies that phases defined by (4.31) satisfy $S1_N = 0_N$, and hence the bi-cluster synchronous state is an equilibrium of the dynamics (4.22).

4.3.1.2 Stability

Using linearization-based arguments, we show that this bi-cluster synchronous state is locally unstable unless the number of oscillators in the two clusters are equal. To establish this, consider that the Jacobian of the linearized version of (4.22) around equilibria $\overline{\theta}_j - \overline{\theta}_k = m\pi$, where $m \in \mathbb{Z}$, has the following block-diagonal form:

$$J = \left[\begin{array}{c|c} J_{\mathrm{A}} & 0_{N\times N} \\ \hline 0_{N\times N} & J_{\mathrm{D}} \end{array}\right], \tag{4.32}$$

where $0_{N\times N}$ is the $N \times N$ matrix with all entries equal to 0. The entries of J_{A} and J_{D} are specified as:

$$\begin{aligned} \Big[J_{\mathrm{A}}\Big]_{j\ell} &= \begin{cases} h'(\overline{r}_j^*) & \text{if } j = \ell \\ 0 & \text{if } j \neq l \end{cases} \\ \Big[J_{\mathrm{D}}\Big]_{j\ell} &= \begin{cases} -\frac{\rho}{\overline{r}_j^*} & \text{if } j \neq l\,,\ \overline{\theta}_{j\ell} = 2m\pi \\ \frac{\rho}{\overline{r}_j^*} & \text{if } j \neq l\,,\ \overline{\theta}_{j\ell} = (2m+1)\pi \\ -\sum_{\ell=1,\ell\neq j}^{N} [J_{\mathrm{D}}]_{j\ell} & \text{if } j = \ell, \end{cases} \end{aligned} \tag{4.33}$$

where $m \in \mathbb{Z}$ and $\overline{r}_j^*$ is the equilibrium radius for the jth oscillator. Since J is block diagonal, its eigenvalues are those of J_{A} and J_{D}. In the following, we focus the analysis on the eigenvalues of J_{D}. Since $\overline{\theta}_j - \overline{\theta}_k = m\pi$, the phases of the oscillators belong to one of the two clusters on the circle (depending on whether m is odd or even). Two cases need attention:

i) The sizes of the two clusters differ by more than one: Denote e_j to be the length-N unit basis vector with 1 at the jth entry and zeros elsewhere. Denote ℓ to be the index of any node in the bigger cluster. The diagonal entries of J_{D} corresponding to oscillators in the bigger cluster are positive, and since $e_\ell^{\mathrm{T}} J_{\mathrm{D}} e_\ell > 0$, it is not negative semidefinite, therefore J_{D} must have at least one positive eigenvalue [61].

ii) The sizes of the clusters differ by one: The diagonal entries are either 0 (for the nodes in the bigger cluster) or -2 (for the nodes in the smaller cluster). Thus, there exists a symmetric principal minor of order 2 (corresponding to two nodes in distinct clusters) of the form

$$\frac{\rho}{2} \cdot \begin{bmatrix} 0 & \pm 1 \\ \pm 1 & -2 \end{bmatrix}$$

which features a positive eigenvalue. Therefore J_{D} cannot be negative semidefinite [61] in this case as well.

In conclusion, J_{D} (and hence, J) has at least one eigenvalue with positive real part. This establishes the local instability of clusters where the phase equilibria satisfy: $\overline{\theta}_j - \overline{\theta}_k = m\pi$ and the number of oscillators in each cluster is not the same.

4.3.2 Phase-synchronous State

This corresponds to the state where the phases of all oscillators are perfectly synchronized:

$$\overline{\theta}_j = \overline{\theta}_k, \ \forall j, k \in \mathcal{N}. \tag{4.34}$$

This state is illustrated in Fig. 4.2 (b). Note that it is recovered as a special case from the bi-cluster synchronous state for $m = 0$.

4.3.2.1 Validity

To see that this is indeed an equilibrium, note from (4.24) that $[S]_{j\ell} = \sin(\overline{\theta}_{jl}) = 0$, $\forall j, k \in \mathcal{N}$ when $\overline{\theta}_j = \overline{\theta}_k$. This further implies that phases defined by (4.34) satisfy $S1_N = 0_N$, and hence the phase-synchronous state is indeed an equilibrium of the dynamics (4.22).

4.3.2.2 Stability

Notice that the phase-synchronous state is recovered from the bi-cluster synchronous state when $m = 0$. Therefore, the stability result from Section 4.3.1 applies in this case as well. In particular, for the case $m = 0$, J_{D} in (4.33) is a Laplacian matrix of a complete graph and therefore is positive semidefinite. This establishes that the phase-synchronous state is locally unstable.

4.3.3 Generalized Interleaved State

This is a generalized notion of the symmetric interleaved state, and captures the setting where the phases of the oscillators evolve functionally constrained as follows

$$\sum_{j=1}^{N} \mathrm{e}^{\jmath\bar{\theta}_j} = 0, \tag{4.35}$$

where $\jmath = \sqrt{-1}$. This state is also known as the phase-balanced state, and it is widely studied in the coupled-oscillator literature [62]. Closer to the application at hand, it was investigated for an asymmetric interleaving application [35] where the first harmonic was eliminated to minimize the current ripple. The generalized interleaved state is illustrated in Fig. 4.2 (c).

4.3.3.1 Validity

Unlike the bi-cluster synchronous state and the phase-synchronized state, in this case, S is not a null matrix and therefore condition (4.30) is not satisfied trivially. Nonetheless, it turns out that when S is not a null matrix then $S1_N = 0_N$ if and only if $C1_N = 0_N$. (See Proposition 2 in [52].) For the generalized interleaved state where $\sum_{j=1}^{N} \mathrm{e}^{\jmath\bar{\theta}_j} = 0$, it is true that $C1_N = 0_N$ *and* $S1_N = 0_N$, and therefore, this indeed corresponds to an equilibrium of the phase dynamics in (4.22).

4.3.3.2 Stability

We construct a directed graph to establish the nature of equilibria in the oscillator dynamics (4.22). Let N nodes of the graph denote the oscillators and if the vector field governing $\dot{\bar{\theta}}_j$ has a $\bar{\theta}_{jk}$ term (i.e., the evolution of the jth oscillator dynamics depends on the dynamics of the kth oscillator), then there is an edge between nodes j and k. The phase dynamics

in (4.22) can be compactly recast as follows:

$$\dot{\overline{\theta}} = R^{-1} B \sin(B^{\mathrm{T}} \overline{\theta}), \tag{4.36}$$

where $B \in \mathbb{R}^{N \times \binom{N}{2}}$ is the edge-oriented incidence matrix of the underlying complete graph. Furthermore, with regard to notation, for $\theta = [\theta_1, \ldots, \theta_N]^{\mathrm{T}} \in \mathbb{T}^N$, $\sin(\theta) := [\sin(\theta_1), \ldots, \sin(\theta_N)]^{\mathrm{T}}$, and $\cos(\theta) := [\cos(\theta_1), \ldots, \cos(\theta_N)]^{\mathrm{T}}$.

We introduce a coordinate change to $\widetilde{\theta} = B^{\mathrm{T}} \overline{\theta} \in \mathbb{R}^{\binom{N}{2}}$, that captures angle differences between the oscillators. In this new set of coordinates, the phase dynamics can be written as:

$$\dot{\widetilde{\theta}} = \rho B^{\mathrm{T}} R^{-1} B \sin \widetilde{\theta}. \tag{4.37}$$

Consider the following potential function

$$V(\overline{r}, \widetilde{\theta}) = -\sum_{j=1}^{N} \int_0^{\overline{r}_j} h(s) ds + 1_N^{\mathrm{T}} R B \cos \widetilde{\theta}, \tag{4.38}$$

from which, it follows that

$$\dot{V}(\overline{r}, \widetilde{\theta}) = -\left(H - \rho B \cos \widetilde{\theta}\right)^2 - \rho (\sin \widetilde{\theta})^{\mathrm{T}} B^{\mathrm{T}} R R^{-1} B \sin \widetilde{\theta}.$$

Notice that $\dot{V}(\overline{r}, \widetilde{\theta}) \leq 0$, since it is the sum of two quadratic terms with a negative leading sign. Thus, the sublevel sets of V are compact (closed due to continuity and bounded as $V(\overline{r}, \widetilde{\theta})$ is radially unbounded).

Finally, by LaSalle's invariance principle [55], all trajectories starting in $\mathcal{I}$ (defined in (4.27)) converge to the subset identified by $\dot{V} = 0$, i.e., amplitudes and phases are such that $B \sin \widetilde{\theta} = 0_N$ (which is true if and only if $S1_N = 0_N$ which implies $C1_N = 0$ when S is not a null matrix) and $H - \rho C 1_N = 0$ (which gives $H = 0_N$ when S is not a null matrix). As discussed earlier, $S1_N = 0_N$, either gives rise to the bi-cluster synchronous state (of which the phase-synchronous state is a special case) or the generalized interleaved state. We have already established that the bi-cluster synchronous state is locally unstable. Therefore, almost all trajectories must eventually converge to the generalized interleaved state.

4.3.4 Symmetric-interleaved State

The multiphase system is said to be in a symmetric interleaved state if the phases of the coupled oscillators evolve uniformly spaced apart as follows:

$$\overline{\theta}_j = j \frac{2\pi}{N} + \theta_\circ \pmod{2\pi}, \forall j \in \mathcal{N}, \quad 0 \leq \theta_\circ \leq 2\pi. \tag{4.39}$$

The symmetric interleaved state is illustrated in Fig. 4.2(d).

4.3.4.1 Validity

We established previously that the generalized interleaved state (where phases are governed by (4.35)) is indeed an equilibrium of the phase dynamics (4.22). Notice that the symmetric-interleaved state, where phases are governed by (4.39) is a special case of the generalized interleaved state, and therefore satisfies the condition (4.30) as well.

4.3.4.2 Stability

To establish whether the interleaved state is locally stable, we begin by shifting the amplitude and phase dynamics from (4.22) to the origin as follows:

$$\mu_j = \overline{r}_j - \overline{r}^*, \quad \varphi_j = \overline{\theta}_j - j\frac{2\pi}{N}, \tag{4.40}$$

where $\overline{r}^*$ denotes the equilibrium radius which solves $h(\overline{r}^*) = 0$. Now, the dynamics of the coupled system (4.22) around this equilibrium can be written as:

$$\begin{aligned} \dot{\mu}_j &= h(\overline{r}^* + \mu_j) \ - \rho \sum_{k=1}^{N} \cos\left(\frac{2\pi(j-k)}{N} + \varphi_{jk}\right), \\ \dot{\varphi}_j &= \frac{\rho}{\overline{r}^* + \mu_j} \sum_{k=1}^{N} \sin\left(\frac{2\pi(j-k)}{N} + \varphi_{jk}\right), \end{aligned} \tag{4.41}$$

where $\varphi_{jk} := \varphi_j - \varphi_k$. We focus on the phase dynamics and leverage the fact μ_j and φ_{jk} are small quantities as we are interested in the behavior around the neighborhood of the interleaved state, and therefore, $\sin\varphi_{jk} \approx \varphi_{jk}$, $\cos\varphi_{jk} \approx 1$ and $(\overline{r}^* + \mu_j)^{-1} \approx \frac{1}{\overline{r}^*}(1 - \frac{\mu_j}{\overline{r}^*})$. With these simplifications in place and ignoring second-order terms like $\mu_j\varphi_{jk}$, the phase dynamics reduce to:

$$\dot{\varphi} = \frac{\rho}{\overline{r}^*} J\varphi, \tag{4.42}$$

where $\varphi := [\varphi_1, \ldots, \varphi_N]^{\mathrm{T}} \in \mathbb{T}^N$ and J is a symmetric circulant matrix with entries given by:

$$[J]_{j\ell} = \begin{cases} -1 & \text{if } j = \ell \\ -\cos\left(\frac{2\pi}{N}(j-\ell)\right), & \text{if } j \neq \ell. \end{cases} \tag{4.43}$$

Since J is a circulant matrix, its eigenvalues are given by

$$\lambda_j(J) = \sum_{k=0}^{N-1} \cos\left(\frac{2\pi k}{N}\right) \Omega_j^k, \tag{4.44}$$

Table 4.1: Specifications, parameters, and ratings for the experimental prototype.

Power Stage Hardware	48 V to 12 V step-down, 120 W per converter
L_f	141.6 μH $\pm$10%
R_f	13.70 mΩ
C_load	1100 μF $\pm$20%
R_Th	0.1 Ω $\pm$5%
R_load	1.6 Ω $\pm$10%
R_par	50 mΩ $\pm$5%
Switching frequency	20 kHz
MOSFET	Fairchild FDB035N10A
Gate driver	Silicon Labs SI8234
Current sensors	Allegro ACS730KLCTR
Voltage sensors	Broadcom ACPL-C87AT
Control Stage Hardware	
Device	Xilinx Artix-7 XC7A35T-L1CSG324I FPGA
Controller time step	150 ns
ADC sampling rate	500 kHz
Oscillator parameters	
σ	$90\,\Omega^{-1}$
α	$60\,\mathrm{A/V^3}$
L	$0.61\,\mu$H
C	$16.67\,\mu$F
Droop controller parameters	
k_p	$0.32\,\mathrm{V/V}$
k_i	$0.06\,\mathrm{s^{-1}}$
m	$1.5\,\mathrm{V/A}$
V_nom	$12\,\mathrm{V}$

where $\Omega_j = \mathrm{e}^{\jmath 2\pi j/N}$ denotes one of the N-th roots of unity. Notice that two of these eigenvalues are $-N/2$ and the rest are zero. Thus, the linearized phase dynamics around the symmetrically interleaved equilibrium are marginally stable.

4.4 Experimental Validation

The proposed approach is validated with a hardware prototype of parallel-connected dc-dc buck converters with independent FPGA controllers as shown in Fig. 4.4. The prototype consists of five independent converters rated at 120 W each, stepping down from 48 V to

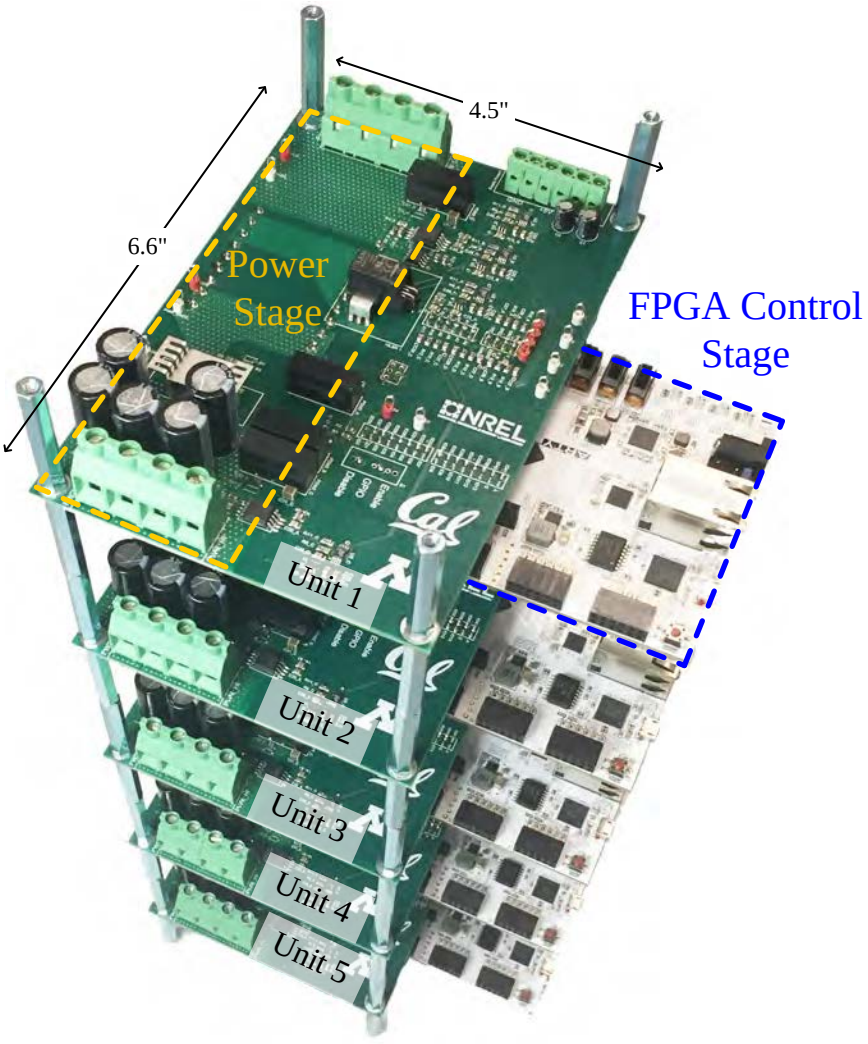


Figure 4.3: Photograph of the experimental prototype: five dc-dc converters and associated controller boards. Note that there is no communication between controllers.

12 V at 20 kHz. The parameters for the controllers along with specifications and ratings of the prototype are listed in Table 4.1. In this section, we first outline the design procedure that was followed to select the oscillator (controller) and converter parameters, following which we provide experimental results.

4.4.1 System Parameters and Controller Design

In this section, we discuss the rationale for the design choices listed in Table 4.1. The oscillator parameters L and C are tuned to the switching frequency, i.e. $1/\sqrt{LC} = \omega_{\text{sw}} =$

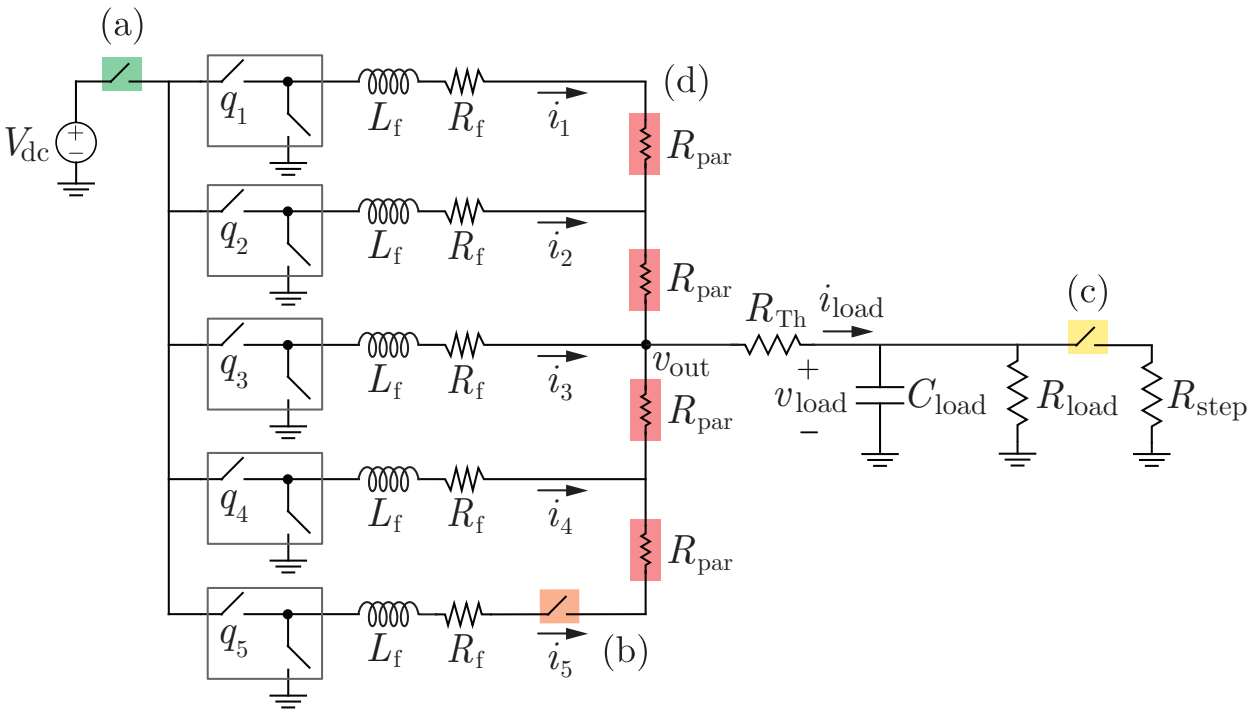


Figure 4.4: Circuit diagram illustrating experiments performed: (a) start up from arbitrary initial conditions, (b) addition of one converter to system, (c) load step, (d) unit addition in non-symmetric network with parasitics (in this case, converters continue to sense local output voltages for droop control even though this is not explicitly depicted in the figure).

$2\pi \times 20\,\mathrm{rad/s}$ while maintaining the quasi-harmonic regime, i.e., $\sqrt{L/C} = \varepsilon \ll 1$. We chose $\varepsilon = 0.19$ in our implementation. Setting $\sigma > 0$ satisfies the Liénard condition for sustaining oscillations [41], and $\alpha = 2\sigma/3$ yields a sinusoidal oscillation of unit amplitude for the oscillators which aids in regularizing the design. The current gain $\kappa > 0$ is necessary for interleaving and is chosen to be 10. (Empirically, we observe that very small values of κ result in slow convergence to the equilibrium state, while very large values of κ induce non-sinusoidal oscillator states with no convergence guarantees.) The droop controller gains k_p and k_i are selected so that the time constant of the controller is about 5 s and there is a clear time-scale separation from the switching period. Furthermore, for each individual buck converter, L_{f} was selected to guarantee continuous conduction mode at the selected operating point and C_{load} is just sufficiently large to establish a constant voltage at the load side. Finally, we also verify that the sufficient positive invariance condition (4.26) derived in Section 4.3 is met so that phase dynamics are well-posed, i.e., $NR_{\mathrm{Th}}\sqrt{\xi^2+\chi^2} < 1$. Notice that in the ideal setup as $R_{\mathrm{Th}} \to 0$, the condition is always satisfied for all N. The current setup with the chosen physical parameters satisfies this condition up to 41 units.

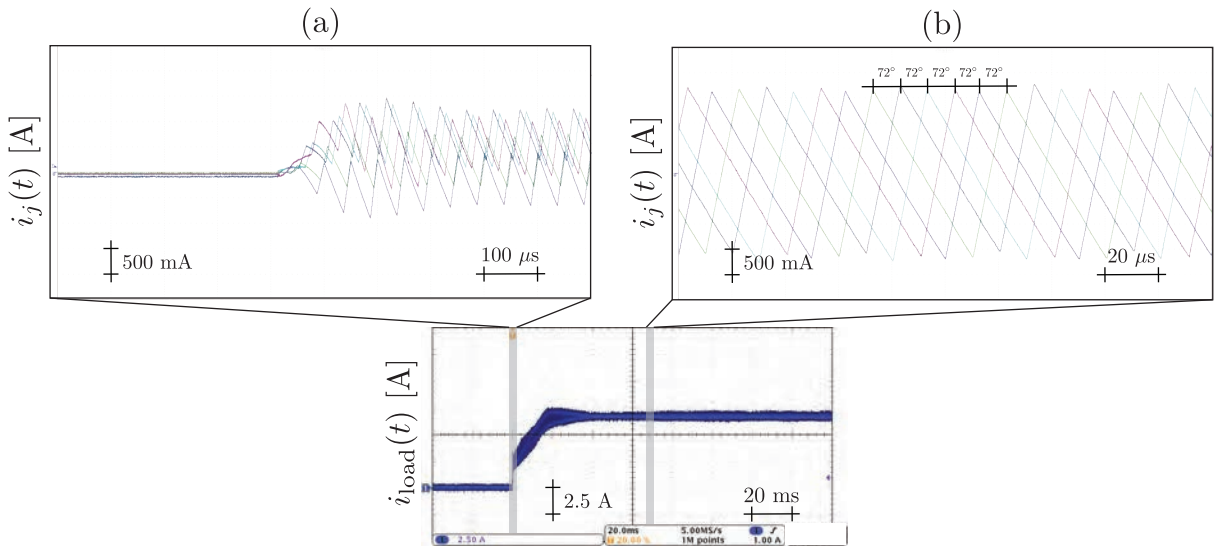


Figure 4.5: Five buck converters are started from arbitrary initial conditions with the designed oscillator-based controllers (a). The system achieves symmetric interleaving with $72° = 360°/5$ phase spacing and the droop controller maintains balanced currents in each of the five units in steady state (b).

Tolerances of various components utilized in the hardware setup are also listed alongside nominal values in Table 4.1. While the anlaysis presumed an ideal and symmetric setup, the experimental results provided subsequently establish the robustness of the approach to a variety of parametric variations (including the ones in Table 4.1 that are readily quantifiable through values from datasheets).

We conducted four experimental tests to validate the performance and robustness of the proposed interleaving control method: a) start up of five units from arbitrary initial conditions, b) addition of one unit to four units in steady state, c) a load step applied to five units in steady state, d) unit addition to a non-symmetric network with lossy lines. The setup and experiments performed listed above are sketched in Fig. 4.3. Next, we provide results from these experiments and demonstrate that, in each case, the proposed controller ensures interleaving in steady state without any communication between converters.

4.4.2 Start Up from Arbitrary Initial Conditions

First, we consider the start-up scenario in which five units are initiated simultaneously, each with arbitrary initial conditions. The dynamics of the load current and the ac components of the phase currents for this case are shown in Fig. 4.5. The phase currents, i_j, of the individual converters at the turn-on instant are arbitrarily spaced, which results in a larger

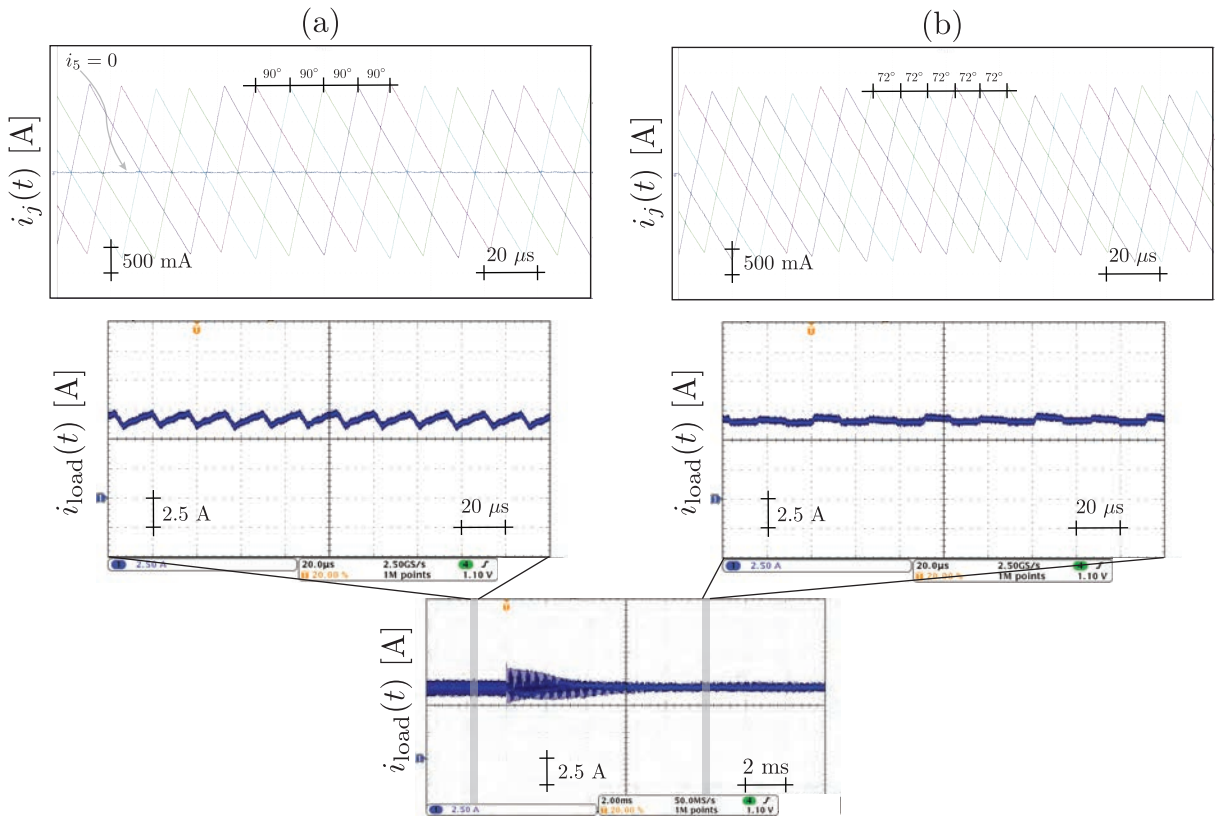


Figure 4.6: One additional buck converter unit is added to four functioning units. The phase currents i_j automatically transition from having $90° = 360°/4$ phase shift (a) to $72° = 360°/5$ phase shift (b).

ripple in i_{load}. After approximately 40 ms, the phase currents of the five converters settle to the interleaved state with $72° = 360°/5$ phase offset and the ripple in i_{load} is visibly reduced.

4.4.3 Unit Addition

Next, to demonstrate the plug-and-play nature of the proposed control strategy, we investigate system performance when an additional converter is added. As shown in Fig. 4.6, the system is initialized in steady state with four parallel units with phase currents that are $90° = 360°/4$ out of phase with adjacent units. After adding an additional fifth unit, the system reaches the interleaved state in approximately 6 ms with each phase current now 72° (360°/5) out of phase with adjacent units. The benefits of interleaving with additional units are also evident in reducing load-current ripple. Again, the droop controller successfully maintains current sharing before and after the addition of the fifth unit.

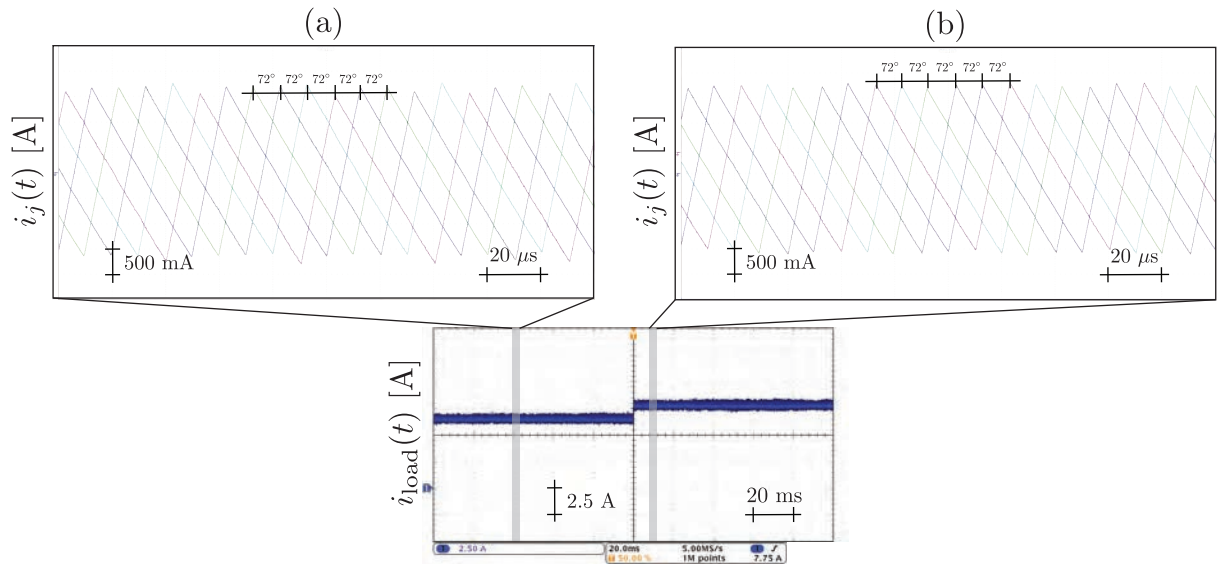


Figure 4.7: To evaluate the robustness to load variations, a load step from $R_{\text{load}} = 1.6\ \Omega$ (a) to $R_{\text{load}} = 1.3\ \Omega$ (b) at $t = 0$ is introduced with five units in steady state. The convergence to the new steady state is almost instantaneous and the system maintains the symmetric interleaved state with $72° = 360°/5$ phase spacing between converters.

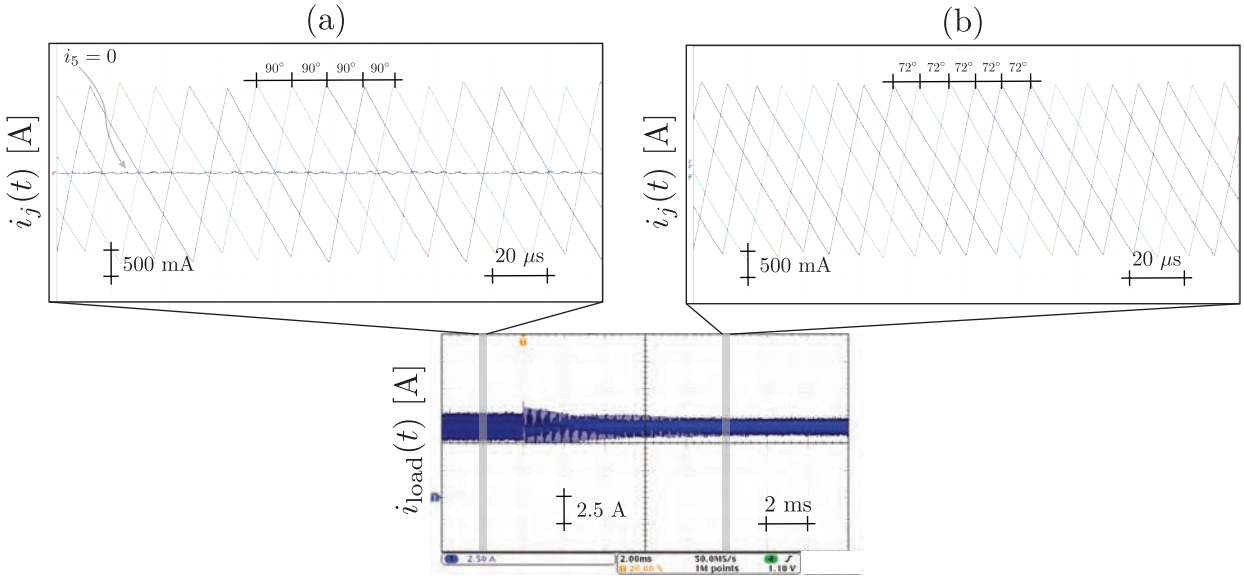


Figure 4.8: Addition of one unit to four units in steady state with the non-symmetric setup and lossy network shown in Fig. 4.3. The phase currents i_j automatically transition from having $90°(360°/4)$ phase shift (a) to $72°(360°/5)$ phase shift (b).

4.4.4 Load Step

We experimentally implemented a load step to validate the robustness of the control method to typical operating transients. As shown in Fig. 4.7, the load is changed from $R_{\text{load}} = 1.6\ \Omega$ to $R_{\text{load}} = 1.3\ \Omega$ at $t = 0$ with five units connected. The system maintains the interleaved state before and after the transient, as indicated by the unchanged ripple magnitude in i_{load} and the unchanged 72° phase shift in phase currents i_j.

4.4.5 Non-ideal Output Parallel Configuration

Lastly, in order to validate the robustness of the proposed method to non-idealities in the parallel output configuration, we implemented the circuit shown in Fig. 4.3, where deliberately introduced resistors R_{par} induce a nontrivial output impedance to each converter. This eliminates the ideal parallel connection between the dc-dc converters. With this circuit, we executed the task of adding one unit to four units in steady state. As shown in Fig. 4.8, four units are initially interleaved with $90° = 360°/4$ degree phase shift in currents. When the fifth unit is added, the system reaches the new interleaved state after approximately 8 ms, at which point the phase shifts automatically adjust to $72° = 360°/5$. Notice from the figure that the ripple in load current reduces with the additional unit. The presence of the non-idealities does increase the ripple (compared to the test shown in Fig. 4.6) by approximately 50%. Regardless, this test has demonstrated the robustness of the method to achieve interleaving even in the presence of modestly large non-idealities in the output loading configuration. Moreover, these non-idealities have minimal impact on the droop controller and its ability to ensure current sharing between the units.

4.5 Summary

In this chapter, we proposed a decentralized control strategy to achieve interleaving in a system of parallel-connected buck converters. Our approach utilized a nonlinear oscillator-based controller that processes a local current measurement to generate the PWM carrier waveform. It offers enhanced reliability and flexibility compared to existing algorithms for modular architectures that are at best distributed in nature since there is no need for external communication. A system of parallel-connected buck converters with droop control was built as a hardware prototype and we experimentally demonstrated the efficacy of the proposed control algorithm for modular plug-and-play operation as well as robustness to

load variations. Extending the analysis to other dc-dc converter topologies and network architectures is the focus of ongoing investigations.

Part II

Reliability Considerations

Chapter 5

Fault Diagnosis: Landscape and Motivation

In this chapter, we discuss the need for robust fault diagnosis in a variety of emerging, high-impact applications. Additionally, we review existing state-of-the-art strategies for achieving fault diagnosis and discuss their limitations. Finally, we argue that there is a critical need for a new framework for fault diagnosis that is flexible, computationally efficient, and precise in its ability to detect and classify faults of interest.

5.1 Applications of Interest

Many current- and next-generation power distribution architectures rely on multiple power conversion stages in order to improve energy efficiency, to maximize resource utilization, and to meet increasingly stringent end-use power quality requirements. In this section, we discuss two such power distribution architectures: 1) a nanogrid for the built environment that enables integration of local electricity generation, storage, and usage, and 2) a dc-based microgrid architecture for enabling cost-effective electrification in emerging regions. We discuss the motivations and advantages that can be realized by these power distribution architectures, as well as the inherent need to ensure safety and reliability.

5.1.1 Building Nanogrids

Commercial buildings consume nearly one-fifth of the primary energy in the United States. In recent years, the concept of a zero-energy building has emerged as an important in-

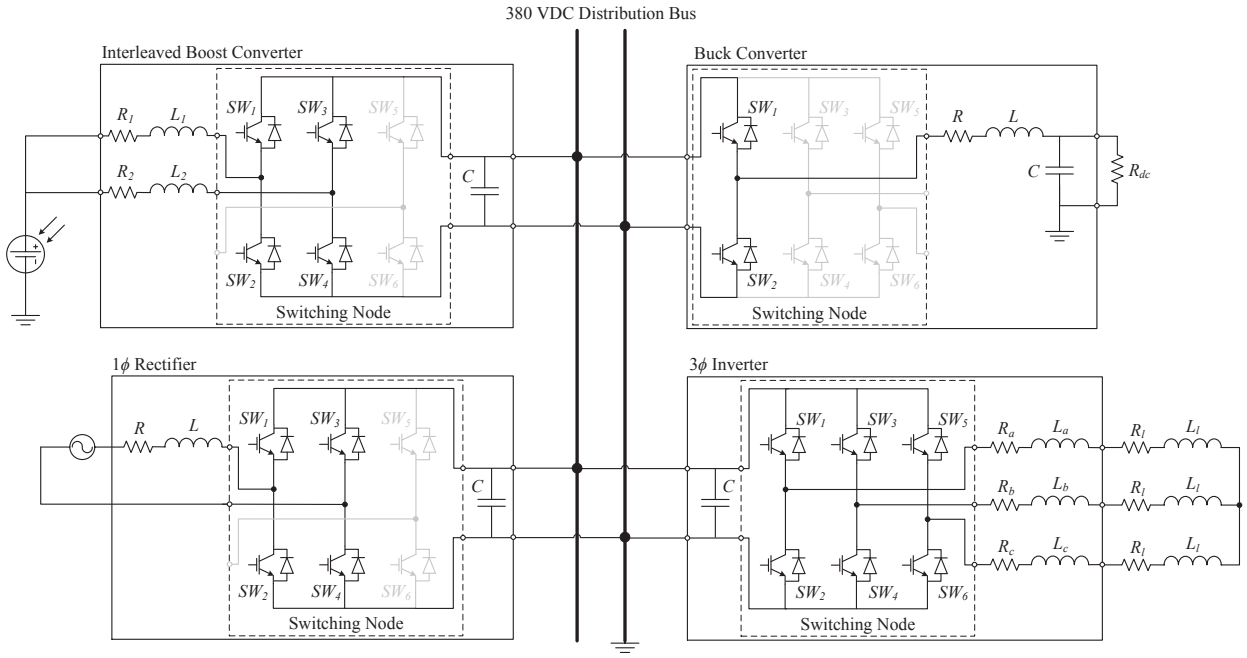


Figure 5.1: A DC-based power distribution nanogrid.

Source: Institute of Applied Sustainability to the Built Environment (ISAAC), Swiss BiPV Competence Centre Campus, Trevano CH-6952 Canobbio, www.bipv.ch

Figure 5.2: Rooftop and BIPV system for a variety of building types [63].

dustrial effort towards realizing significant improvements in building energy efficiency, user comfort, and intelligence [64, 65]. Integral to the concept of a zero-energy building is its power distribution network, or *nanogrid*, as shown in Fig. 5.1. As opposed to buildings that purely consume energy, these nanogrids can contain on-site microgeneration resources, such as rooftop photovoltaics or wind turbines. Energy storage buffers, such as batteries or mechanical flywheels, store excess generated energy, which can be used for building loads or sold back to the utility. Additionally, electrical loads can be scheduled based on dynamic energy pricing, enabling demand response. Indeed, zero-energy building nanogrids introduce a new paradigm of how buildings consume, generate, and store energy.

Similarly, photovoltaic (PV) energy conversion architectures based on panel or subpanel-level distributed power electronic converters are increasingly ubiquitous for rooftop and building-integrated PV (BIPV) systems, as shown in Fig. 5.2 [66, 67, 68, 64]. The unique advantages of a distributed power electronic-based PV system include higher energy yield (particularly, in partial shading conditions), higher performance reliability, lower installation costs, plug-and-play operation, and enhanced system flexibility, modularity, and scalability [67, 69, 70, 71].

However, the confluence of power electronics systems and buildings in these nanogrids has introduced new challenges, particularly with respect to availability, reliability, and system security and safety [72]. Switching power converters introduce new failure points in a power distribution network. Moreover, the interactions between converters and the propagation or cascading effect of faults through a nanogrid remain open research questions.

For instance, distributed PV systems are vulnerable to a variety of faults due to their complex outdoor installations, increased number of power electronic converters at the PV panel-level, harsh mission profiles, manufacturing defects, and aging. A comprehensive analysis of common failure modes that could occur in these PV systems and their impacts on performance and reliability are given in [73, 74, 75]. These failures degrade system performance, and endanger the safety and security of the buildings and its occupants. Moreover, these failures are difficult to locate and repair in building applications because rooftop and BIPV systems have a very large number of PVECUs which can be physically inaccessible due to complex installations (exacerbating maintenance and inspection that incur high cost). Thus, robust and cost-effective methods for ensuring their dependability and fault tolerance are necessary.

5.1.2 Electrification for Emerging Regions

There are over 1.3 billion people worldwide lacking access to electricity. This energy poverty has a large adverse effect on economic development and education outcomes. In addition, many of these populations rely on fossil fuels (kerosene and wood) for their primary lighting needs; fossil fuels are an inefficient source of lighting and their use has significant detrimental impacts on the environment and on public health. Unelectrified populations are located predominantly in rural emerging regions that are unconnected to the central electricity grid. These presently unelectrified households are expected to drive most of the medium-term (next 20-30 years) growth in energy consumption [82, 83]. Grid extension to meet their

Table 5.1: Common failure modes in BIPV systems.

Components	Common failure modes
PV panel [75, 76, 77]	Soiling Continuous/repetitive partial shading conditions Cells breakage EVA browning Bypass diode failures Potential induced degradation (PID) Interconnect faults Internal faults related to PV shunt and series resistances
Power converter [78, 79, 80]	Switch open circuit Switch short circuit Capacitor or inductor degradation
Electrical sensors [81]	Open circuit Wear-out (tuning parameter drift)

energy needs is not viable because of high connection costs. In addition, grid operators face structural disincentives to providing grid-connectivity—such as high transmission losses, and electricity theft [84]. Furthermore, studies show that grid extension does not guarantee access to reliable electricity; there is a high degree of load-shedding and service-unreliability for rural customers [85, 86].

In previous works [87], we have presented the design, implementation, and experimental validation of a scalable dc microgrid with distributed storage. The dc microgrid has been designed to meet the electricity needs of households within a 1 km radius, and has the following features:

1. **Dc power generation and distribution:** Line distribution losses will be minimized by using a variable 380V for distribution. Electricity will be converted to an intermediate 48V bus, then to 12V for household consumption.

2. **Household Power Management Units (PMUs):** The dc distribution lines will be connected to each household via a dc-dc converter integrated into the PMU that provides the power for all household appliances. PMUs also integrate scalable distributed storage that is owned by the individual households. In addition, the PMUs can digitally communicate information such as price, charge-state of households, credits, and usage.

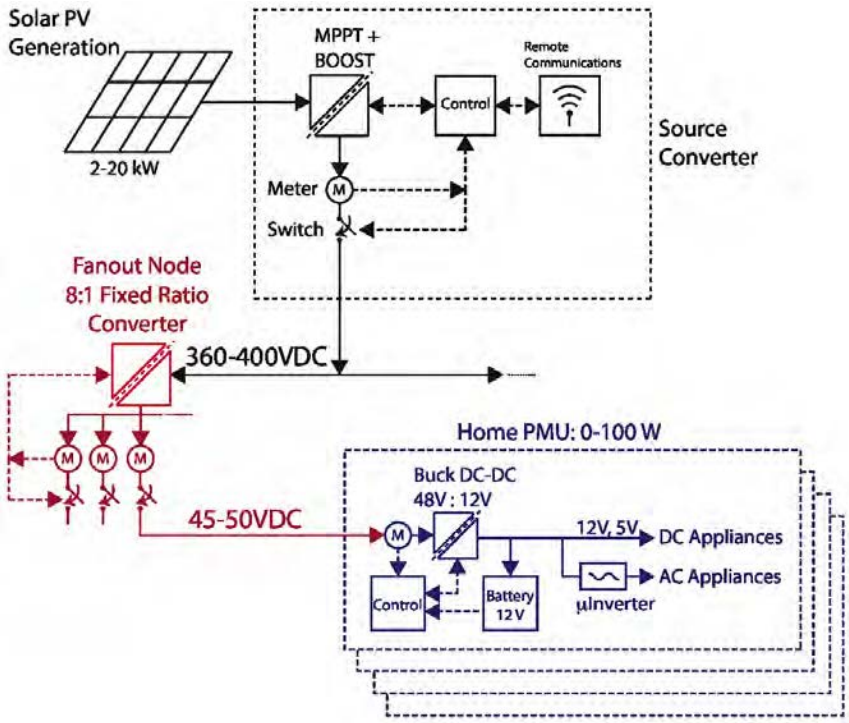


Figure 5.3: Dc microgrid system overview. There are three main functional component to the microgrid: Source converter, fanout nodes, and home power management units (PMUs).

3. **Distributed control scheme to mitigate variability in grid power:** A droop-voltage power-sharing scheme is implemented, wherein the microgrid distribution-bus voltage droops in response to low-supply/high-demand. The PMUs in turn respond by reducing the power that they are drawing from the grid by reducing their battery charging load. The control of grid voltage is thereby distributed to the PMUs connected to the grid. This feature is enabled by the combination of dc voltage distribution, and distributed storage. Since the PMUs are able to communicate digitally to the power station, we are also able to do more advanced scheduling and load-management.

4. **High-efficiency Dc Appliances:** PMUs have dc-dc converters that provide power to efficient dc appliances (such as LED lighting). Small-scale, point-of-load inverters are used for ac appliances.

5. **Scalable Distributed Storage:** Batteries integrated into individual PMUs reduces losses of stored energy by minimizing conversion steps, and line-losses. Distributed storage also allows for household loads to be decoupled from the grid-supply as required. Furthermore, household ownership of batteries allows for flexible, demand-

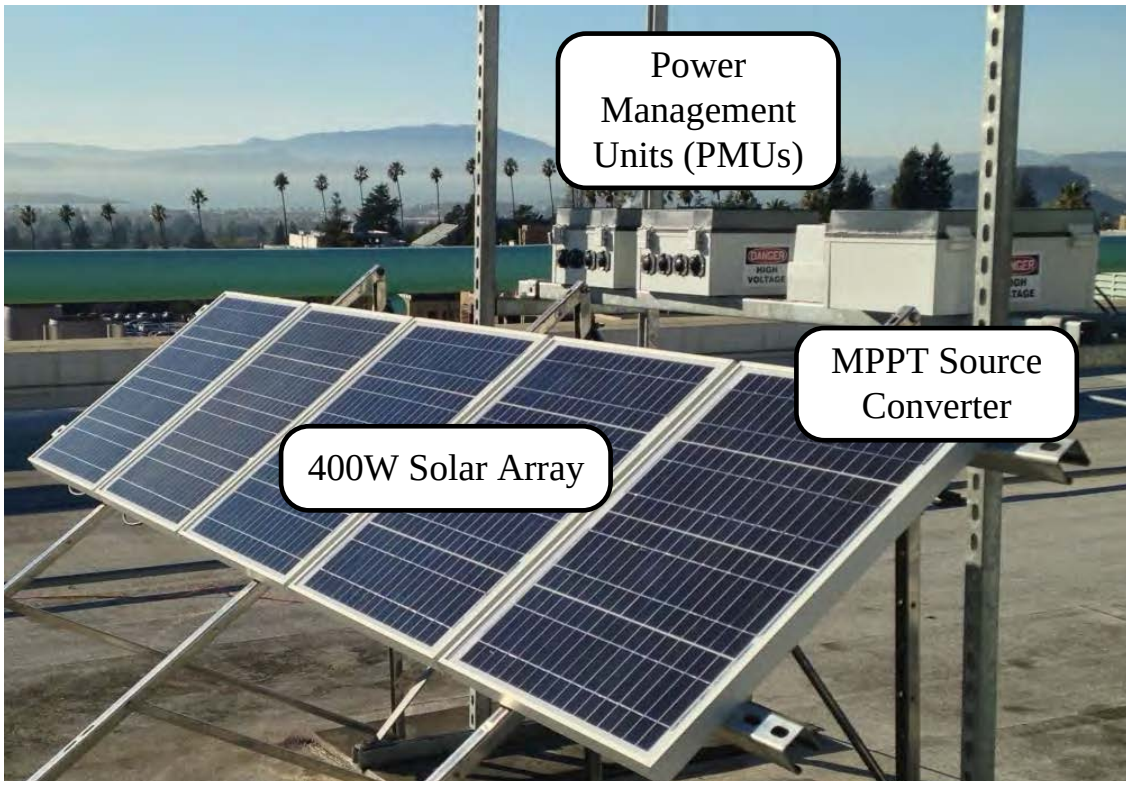


Figure 5.4: Rooftop setup with 400 W solar PV installation. Source converter and two PMUs are shown

driven growth of storage in the grid; each household makes decisions about the size of their storage-capacity based on desired night-time usage.

The architecture of this microgrid makes fault diagnosis and reliability a critical aspect for consideration. Firstly, in any power distribution system that humans can interact and come into contact with, safety needs to be ensured. Secondly, unlike a traditional, centralized power distribution model, the proposed distributed microgrid model introduces many more switching power converters at various parts of the network. Thus, the opportunity for failure is considerably higher due to the increased number of devices. Lastly, the distributed nature of the power converters makes regular maintenance more challenging. Therefore, such a microgrid could benefit from online diagnostics and condition monitoring, which could provide operators with forecasts of anticipated failures before they occur or provide precise information about specific faults if and when they occur.

5.2 State-of-the-Art Strategies for Fault Diagnosis

Here, we will review existing state-of-the-art strategies for enabling fault diagnosis in power conversion systems. First, we will address techniques for: 1) *fault detection and identification* and 2) *fault prognosis*.

5.2.1 Fault Detection and Identification

In general, systems with critical dependability requirements are designed with mechanisms for *fault tolerance*. Fault tolerance is the ability of a system to adapt and compensate, in a systematic way, to faults in components, sensors, or inputs, while providing completely or partially its intended functionality. There are three key elements to any fault tolerant system design: (1) component redundancy, (2) a fault detection and identification (FDI) system [88, 89, 90], and (3) a remediation or reconfiguration system that, once a fault has been detected and identified, substitutes the faulty component with a redundant one, or reconfigures the control to compensate for the fault.

An FDI system is advantageous in that it can contribute to the fault tolerance of a system with minimal additional cost and system complexity (as opposed to an approach using component redundancy). An FDI system executes two tasks: (1) detection, which makes a binary decision whether or not a fault has occurred, and (2) identification, which determines the location of the faulty component [88]. It is important to note that an FDI system, in general, does not replace hardware-based fault protection devices, such as fuses, circuit breakers, and internal semiconductor module protection. Instead, an FDI system provides on-line granular information about the converter state and health, which can be used for monitoring, prognosis, and automated fault remediation.

Table 5.2: A review of existing literature in FDI methods for switch faults in power electronics systems.

	Switch fault
Hardware-based (analog circuits)	[91, 92, 93, 94, 95, 96, 97]
Model-based	[98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108]
Signal processing (time domain)	[109, 110, 111]
Signal processing (frequency domain)	[112, 113, 114, 115, 116, 117]
Statistical	[114, 118]
Machine learning	[119, 120, 113, 97, 121, 122, 117, 123]
Hidden Markov model	[124]

Table 5.3: A review of existing literature in FDI methods for multiple switch, open-phase, sensor, and passive element faults in power electronics systems.

	Multiple switch fault	Open-phase	Sensor fault	Passive element fault
Hardware-based (analog circuits)	[94]	[92]	-	-
Model-based	[125, 126]	[102]	[127]	[128, 129, 130, 131]
Signal processing (time domain)	[132, 133, 134, 135, 136, 137]	[138]	-	-
Signal processing (frequency domain)	[106]	[114]	[115]	-
Statistical	-	[114]	-	-
Machine learning	[106, 139, 137]	[140]	-	-
Hidden Markov model	[141]	-	-	-

Fault detection and identification for power electronics systems has been explored in literature before (see Tables 5.2 and 5.3), primarily for specific converter topologies and for specific converter faults. For instance, in [99, 100, 119, 120, 101, 102, 110, 132, 133, 103, 126, 127, 113, 139, 114, 118, 142, 125, 136, 97, 106, 117, 143], the authors investigate FDI techniques specifically for three-phase drives in electric vehicles. In other works, authors have focused on detecting and identifying specific component faults (e.g. open- and short-circuit switch faults, gate driver faults, capacitor faults) in DC-DC converters [111, 138, 94, 95, 96], grid-connected AC-DC converters and DC-AC converters [98, 109, 115, 116, 92, 105, 122, 137, 112], and in modular multilevel converters [108, 144, 104]. Some literature has focused on detecting faults in current and voltage sensors in converter systems [115, 127].

However, to the best of our knowledge, no work has been reported towards a generalized FDI approach for components and sensors that is suitable for an arbitrary switching power converter. The majority of the existing FDI techniques are specialized for a specific converter topology and cannot be easily ported from one converter to another. Indeed, such a generalized FDI approach would be particularly beneficial in a nanogrid setting, which could feature an array of DC-DC, DC-AC, or AC-DC converters.

Methodologies used for fault detection and identification can be broadly classified into *model-based* and *model-free* approaches. Model-based approaches use analytical knowledge of the system and are generally based on residual generation using parameter estimation, parity equations, or state observers [98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 125, 126, 127, 128, 129, 130, 131]. Signal processing techniques, which are a subset of model-based methods, monitor the difference between nominal and faulty states of signals to indicate abnormalities. Signal processing FDI approaches can either be in the time domain (see e.g. [109, 110, 111, 132, 133, 134, 135, 136, 137, 138]) or in the frequency domain (see e.g. [112, 113, 116, 117, 106, 114, 115]). However, in general, signal processing techniques require a relatively long time (10 to 20 ms) to identify faults depending on the computational complexity of the algorithm and the latency of the computing platform.

Model-free approaches rely on artificial intelligence-based techniques, such as machine learning, artificial neural networks, or fuzzy logic, to develop an expert system that once trained, can identify specific faults [120, 114, 118, 119, 113, 97, 121, 122, 117, 123, 106, 139, 137, 140]. Drawbacks of these approaches are the excessive computational requirements and large data sets required to train the algorithms.

Finally, the FDI techniques can be further classified into analog or digital implementation.

It is evident that analog implementations can identify faults relatively fast (around 1-100 μs) (see e.g. [91, 92, 93, 94, 95, 96, 97]). However, the analog implementations are both converter and fault specific. Digital implementations generally provide more flexibility in terms of reconfigurability (see e.g. [98, 109, 101, 102, 110, 132, 103, 138, 136, 106, 107]). Additionally, field-programmable gate array (FPGA) implementations have demonstrated fault identification at speeds comparable to analog implementations in some applications [98, 106, 109].

5.2.2 Fault Prognosis

Many mission-critical power electronics systems, including renewable energy integration, data center power delivery, and motor drives applications, require high reliability and availability of service [145, 86]. In many of these scenarios, techniques for *fault prognosis* are commonly employed, that is, methods for actively monitoring the system condition and predicting when failures or faults will occur. A central technology that enables fault prognosis is *parameter identification*, or identifying the values of system parameters in a real-time and online manner. By tracking the values of important system parameters in real-time, operators can actively monitor the overall health of a system and anticipate when maintenance or repairs will be needed. Moreover, fault prognosis can be achieved by monitoring if estimated parameter values are above or below an accepted tolerance range.

The failure modes and mechanisms for power electronics systems have been widely investigated, for instance in [146, 147, 148, 79, 80]. Passive components, such as capacitors and inductors, are a key failure point. Table 5.4 provides an overview of the common failure modes of passive components in a power electronics systems and the effect that these failures have on the resulting parameter value and ESR. The reasons for these failures vary widely, and include manufacturing defects, harsh environmental conditions (e.g. temperature and humidity), aging, high voltage stress, insulation failures, interconnection failures, mechanical wear, and vibrations and shocks [147, 79, 80, 149]. Moreover, the effect of the failures can be classified as either 'hard' or 'soft' faults. A hard fault is one that causes a sudden and catastrophic effect in the system (e.g. a short circuit), while a soft fault is one that causes a gradual effect or degradation in the system, generally related to lifetime wear or aging.

Parameter identification has been investigated previously in the context of power electronics systems. One salient application for parameter identification in power electronics systems has been for estimating the capacitance or equivalent series resistance (ESR) of a

Table 5.4: Typical fault modes for capacitors (electrolytic, ceramic, and film) and inductors (air inductors, ferrites, and iron-core) in power electronics systems [80, 147].

Component	Fault modes	Fault type	Parameter drift direction
Capacitors	Open circuit (OC)	Hard	C = 0, ESR = ∞
	Short circuit (SC)	Hard	C = 0, ESR = 0
	Wear out	Soft	C = $\downarrow$, ESR = $\uparrow$
Inductors	Open circuit	Hard	L = 0, ESR = ∞
	Full-winding SC	Hard	L = 0, ESR = 0
	Inter-turn SC	Soft	L = $\downarrow$, ESR = $\downarrow$
	Core to winding SC	Soft	L = $\downarrow$, ESR = $\uparrow$
	Wear out	Soft	L = $\downarrow$, ESR = $\uparrow$

dc-link capacitor [150, 151, 152, 153, 154, 155]. In many converters, the dc-link capacitor, particularly electrolytic capacitors, is one of the primary points of failure in the converter. Actively monitoring the capacitance or ESR of the capacitor enables detection and prediction of when these failures will occur.

In general, most algorithms for parameter identification compare measurements from the physical system (e.g. voltage, current, temperature) with a model structure. This model structure could be a black-box (e.g. neural networks [156, 157, 158, 159]) or based on a physical model (e.g. Kalman filter, state observers [160, 161, 162, 163, 164, 165, 151]).

These existing approaches in literature, however, have certain characteristics that limit that effectiveness and applicability of the methods. Some of these limitations include: (1) high computational requirements (e.g. requires an external PC or graphical processing unit), (2) custom analog implementations, (3) techniques based on heuristic analysis that are only applicable to a specific switching converter, (4) injection of external voltage or current signals, or (5) need for extensive data sets and training.

5.3 Summary

In this chapter, we reviewed emerging applications in which new techniques for fault diagnosis are necessary to ensure safe and reliable power delivery. We discussed state-of-the-art techniques for achieving fault diagnosis and their associated applications and limitations. In the remainder of Part 2 of this dissertation, we will present new techniques that seek to fill these voids and provide robust fault diagnosis for a wide variety of high-impact applications.

Chapter 6

Modeling and Estimation Framework

In this chapter, we present the modeling and estimation framework used to describe the dynamics of a switching power converter in nominal and faulted operating conditions. First, we will discuss the modeling techniques used to capture the switched linear dynamics of power converters in a compact form that is amenable for efficient real-time numerical solvers. Next, we will discuss estimators that can be designed based on the proposed modeling techniques, including estimators for tracking state and parameter values within a system of interest. The modeling and estimation framework is an essential component to the proposed fault diagnosis methods that are discussed in Chapters 7 and 8.

6.1 Converter and Fault Modeling Framework

6.1.1 Nominal System Model

The switching power converters under consideration are those that can be modeled as a *switched linear system*, that is, a collection of linear state space models (*modes*) and a continuous-time *switching signal*, which indicates the active mode of the system at every time instant. The state space model for each mode can be obtained by considering every open/closed position for the switches in a converter (e.g. diodes, IGBTs, MOSFETs, etc.) and applying Kirchhoff's circuit laws for the resulting *linear* circuit. The switching signal can be obtained by considering a logical union of the dynamics of 'controlled' switches (e.g. PWM applied to IGBTs or MOSFETs) and the dynamics of 'uncontrolled' switches (e.g. diodes) whose open/closed position depends on the state of the system (e.g. the polarity of current flowing through a diode). In general, the dynamics of an arbitrary switching power

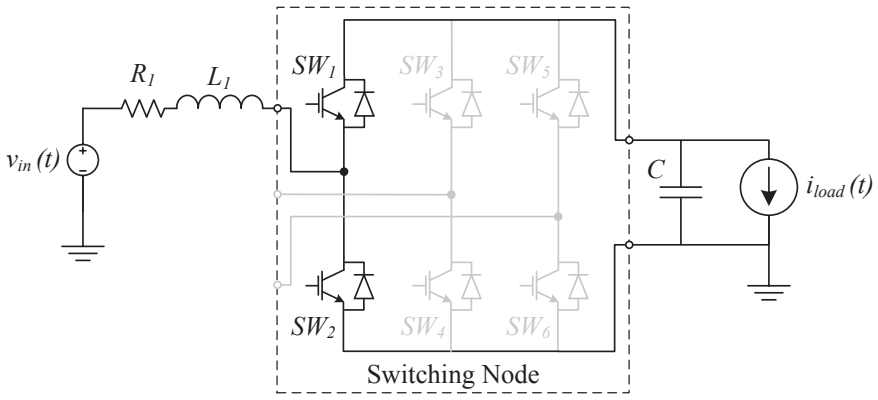


Figure 6.1: Boost converter topology.

Table 6.1: Possible open/close switch positions for the boost converter in continous conduction mode.

$\sigma(t)$	1	2
s_1	0	1
s_2	1	0

converter can be modeled as a switched linear system of the form [166]:

$$\dot{\mathbf{x}}(t) = \mathbf{A}_{\sigma(t)}\mathbf{x}(t) + \mathbf{B}_{\sigma(t)}\mathbf{u}(t) \tag{6.1}$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) \tag{6.2}$$

where $\mathbf{A}_{\sigma(t)}$, $\mathbf{B}_{\sigma(t)}$, and $\mathbf{C}$ are the collection of linear state space models, and $\sigma(t)$ is the continuous-time switching signal that indicates the active mode.

Example 1. Consider the boost converter topology in Fig. 6.1. In the continuous conduction mode of operation, the mode of the system is determined explicitly by the PWM applied to SW_2. It follows that:

$$\mathbf{x}(t) = \mathbf{y}(t) = \begin{bmatrix} i_{L_1}(t) \\ v_C(t) \end{bmatrix}, \mathbf{u}(t) = \begin{bmatrix} v_{in}(t) \\ i_{load}(t) \end{bmatrix}$$

$$\mathbf{A}_{\sigma(t)} = \begin{bmatrix} -\frac{R}{L} & -\frac{s_1}{L} \\ \frac{s_1}{C} & 0 \end{bmatrix}, \mathbf{B}_{\sigma(t)} = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}, \ \mathbf{C} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

The possible values for the switching signal $\sigma(t)$ are given in Table 6.1, where $s_k = 0$ indicates switch SW_k is open, and $s_k = 1$ indicates switch SW_k is closed.

Table 6.2: Possible open/close switch positions for the interelaved boost converter in continous conduction mode.

$\sigma(t)$	1	2	3	4
s_1	0	1	0	1
s_2	0	0	1	1
s_3	1	0	1	0
s_4	1	1	0	0

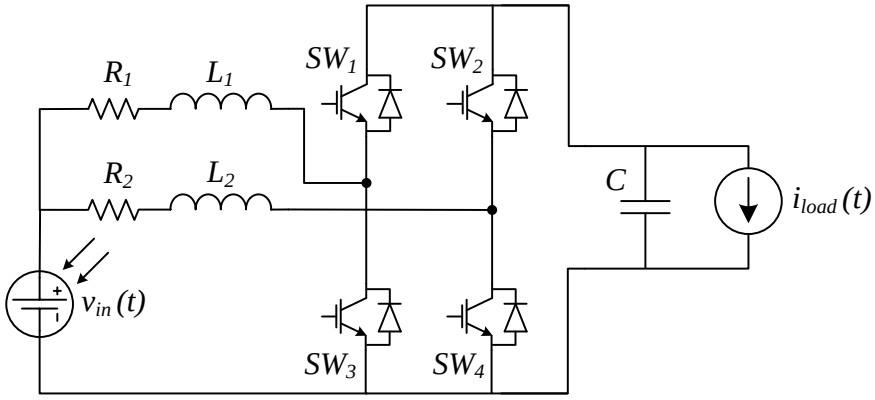


Figure 6.2: Circuit topology of an interleaved boost dc-dc converter.

Example 2. Consider the interleaved boost converter topology in Fig. 6.2. In the continuous conduction mode of operation, the mode of the system is determined explicitly by the PWM applied to SW_1 and SW_2. We can construct an open-loop state estimator of the system as follows:

$$\mathbf{z}(t) = \begin{bmatrix} \hat{i}_{L_1}(t) \\ \hat{i}_{L_2}(t) \\ \hat{v}_C(t) \end{bmatrix}, \ \mathbf{u}(t) = \begin{bmatrix} v_{in}(t) \\ i_{load}(t) \end{bmatrix}, \ \mathbf{y}(t) = \begin{bmatrix} i_{in}(t) \\ v_{out}(t) \end{bmatrix}$$

$$\mathbf{A}_{\sigma(t)} = \begin{bmatrix} -\frac{R_1}{L_1} & 0 & -\frac{s_1}{L_1} \\ 0 & -\frac{R_2}{L_2} & -\frac{s_2}{L_2} \\ \frac{s_1}{C} & \frac{s_2}{C} & 0 \end{bmatrix}, \ \mathbf{B}_{\sigma(t)} = \begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

The inputs to the estimator are admitted in the vector $\mathbf{u}(t)$, and the component parameters in the matrices $\mathbf{A}_{\sigma(t)}$ and $\mathbf{B}_{\sigma(t)}$ are treated as known constants. The possible values for

the switching signal $\sigma(t)$ are given in Table 6.2, where $s_k = 0$ indicates switch SW_k is open, and $s_k = 1$ indicates switch SW_k is closed.

6.1.2 Post-Fault System Model

We consider two types of converter faults—(1) *components faults*, that is, faults that manifest in passive or switching elements, and (2) *sensors faults*, that is, faults that cause the measured values in $\mathbf{y}(t)$ to deviate from the actual values of $\mathbf{x}(t)$.

6.1.2.1 Component faults

Generally, component faults that affect passive or switching elements manifest as additive deviations $\Delta\mathbf{A}(t)$ and $\Delta\mathbf{B}(t)$ from the nominal $\mathbf{A}_{\sigma(t)}$ and $\mathbf{B}_{\sigma(t)}$, respectively, in (6.1). Thus, the state dynamics in the faulted condition can be modeled as:

$$\dot{\mathbf{x}}(t) = \tilde{\mathbf{A}}_{\sigma(t)}\mathbf{x}(t) + \tilde{\mathbf{B}}_{\sigma(t)}\mathbf{u}(t) \tag{6.3}$$

where $\tilde{\mathbf{A}}_{\sigma(t)} \triangleq \mathbf{A}_{\sigma(t)} + \Delta\mathbf{A}(t)$ and $\tilde{\mathbf{B}}_{\sigma(t)} \triangleq \mathbf{B}_{\sigma(t)} + \Delta\mathbf{B}(t)$. With algebraic manipulation, we can rewrite (6.3) as the sum of (6.1) and the product of a time-varying *scalar* component fault magnitude function $\phi_i(\mathbf{x}, \mathbf{u})$ and a time-invariant *vector* component fault signature $\mathbf{f_i}$, that is:

$$\dot{\mathbf{x}}(t) = \mathbf{A}_{\sigma(t)}\mathbf{x}(t) + \mathbf{B}_{\sigma(t)}\mathbf{u}(t) + \phi_i(\mathbf{x}, \mathbf{u})\mathbf{f_i} \tag{6.4}$$

where $i = 1, ..., \mathcal{I}$ and $\mathcal{I}$ is the number of possible types of component faults.

Example 3. Consider a fault in the output capacitor C of the boost converter in Fig. 6.1 that causes the value of the capacitance to change by a quantity ΔC. Thus, the dynamics of the converter in the presence of this fault are:

$$\tilde{\mathbf{A}}_{\sigma(t)} = \begin{bmatrix} -\frac{R_1}{L} & -\frac{s_1}{L} \\ \frac{s_1}{C+\Delta C} & 0 \end{bmatrix}, \tilde{\mathbf{B}}_{\sigma(t)} = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C+\Delta C} \end{bmatrix}$$

The fault magnitude function $\phi_1(\mathbf{x}, \mathbf{u})$ and component fault signature $\mathbf{f_1}$ from (6.4) are as follows:

$$\phi_1(\mathbf{x}, \mathbf{u}) = \frac{\Delta C}{C(C + \Delta C)}(i_{load} - s_1 i_L),$$
$$\mathbf{f_1} = [0, 1]^T$$

6.1.2.2 Sensor faults

Sensor faults manifest as affine deviations in the output readout map in (6.2). That is, the output readout map in the faulted condition can be modeled as:

$$\mathbf{y}(t) = (\mathbf{C} + \Delta\mathbf{C}(t))\mathbf{x}(t) + \Delta\mathbf{E}(t) \tag{6.5}$$

where $\Delta\mathbf{C}(t)$ and $\Delta\mathbf{E}(t)$ capture the affine dynamics of the sensor fault. Similar to the steps performed for the component fault model in Section 6.1.2.1, we can rewrite (6.5) as the sum of (6.2) and the product of a *scalar* sensor fault magnitude function $\theta_j(\mathbf{x})$ and a *vector* sensor fault signature $\mathbf{g_j}$, that is:

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \theta_j(\mathbf{x})\mathbf{g_j} \tag{6.6}$$

where $j = 1, ..., \mathcal{J}$ and $\mathcal{J}$ is the number of possible types of sensor faults.

Example 4. Consider a fault in the input inductor L_1 current sensor of the boost converter in Fig. 6.1 that causes a perturbation in the sensor gain $c_1(t)$ and in the sensor offset $e_1(t)$. This perturbation can be modeled as:

$$\Delta\mathbf{C}(t) = \begin{bmatrix} c_1(t) & 0 \\ 0 & 0 \end{bmatrix}, \Delta\mathbf{E}(t) = \begin{bmatrix} e_1(t) \\ 0 \end{bmatrix}$$

The fault magnitude function $\theta_1(\mathbf{x})$ and sensor fault signature $\mathbf{g_1}$ from (6.6) are as follows:

$$\theta_1(\mathbf{x}) = c_1(t)i_{L_1}(t) + e_1(t),$$
$$\mathbf{g_1} = [1, 0]^T$$

6.2 Estimation Framework

6.2.1 State Estimator Design

We can build a switched linear state estimator of the system from (6.1) as follows:

$$\dot{\mathbf{z}}(t) = \mathbf{A}_{\sigma(t)}\mathbf{z}(t) + \mathbf{B}_{\sigma(t)}\mathbf{u}(t) \tag{6.7}$$
$$\boldsymbol{\gamma}(t) = \mathbf{y}(t) - \mathbf{C}\mathbf{z}(t), \tag{6.8}$$

where $\mathbf{z}(t)$ is an estimate of the state vector $\mathbf{x}(t)$ from (6.1), and $\boldsymbol{\gamma}(t)$ is the *residual* of the difference between the measured output $\mathbf{y}(t)$ and the estimated output $\mathbf{C}\mathbf{z}(t)$. $\mathbf{A}_{\sigma(t)}$ and $\mathbf{B}_{\sigma(t)}$ are obtained by solving Kirchhoff's circuit laws for the ideal circuit topology.

Example 5. Consider the interleaved boost converter topology in Fig. 6.1. In the continuous conduction mode of operation, the mode of the system is determined explicitly by the PWM applied to SW_1 and SW_2. We can construct an open-loop state estimator of the system as follows:

$$\mathbf{z}(t) = \begin{bmatrix} \hat{i}_{L_1}(t) \\ \hat{i}_{L_2}(t) \\ \hat{v}_C(t) \end{bmatrix}, \ \mathbf{u}(t) = \begin{bmatrix} v_{in}(t) \\ i_{load}(t) \end{bmatrix}, \ \mathbf{y}(t) = \begin{bmatrix} i_{in}(t) \\ v_{out}(t) \end{bmatrix}$$

$$\mathbf{A}_{\sigma(t)} = \begin{bmatrix} -\frac{R_1}{L_1} & 0 & -\frac{s_1}{L_1} \\ 0 & -\frac{R_2}{L_2} & -\frac{s_2}{L_2} \\ \frac{s_1}{C} & \frac{s_2}{C} & 0 \end{bmatrix}, \ \mathbf{B}_{\sigma(t)} = \begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

The possible values for the switching signal $\sigma(t)$ are given in Table 6.1, where $s_k = 0$ indicates switch SW_k is open, and $s_k = 1$ indicates switch SW_k is closed.

6.2.2 Estimator Design for Systems with Unknown Parameters

Consider the case when $\mathbf{A}_{\sigma(t)}$ and $\mathbf{B}_{\sigma(t)}$ are not precisely known. Let $\delta\mathbf{A}_{\sigma(t)} \triangleq \hat{\mathbf{A}}_{\sigma(t)} - \mathbf{A}_{\sigma(t)}$ where $\hat{\mathbf{A}}_{\sigma(t)}$ is an estimate of $\mathbf{A}_{\sigma(t)}$, and $\delta\mathbf{B}_{\sigma(t)} \triangleq \hat{\mathbf{B}}_{\sigma(t)} - \mathbf{B}_{\sigma(t)}$ where $\hat{\mathbf{B}}_{\sigma(t)}$ is an estimate of $\mathbf{B}_{\sigma(t)}$. The open-loop state estimator is now given by:

$$\dot{\mathbf{z}}(t) = \hat{\mathbf{A}}_{\sigma(t)}\mathbf{z}(t) + \hat{\mathbf{B}}_{\sigma(t)}\mathbf{u}(t) \tag{6.9}$$

The dynamics of the error $\mathbf{e}(t) = \mathbf{z}(t) - \mathbf{x}(t)$ are governed by:

$$\dot{\mathbf{e}}(t) = \mathbf{A}_{\sigma(t)}\mathbf{e}(t) + \delta\mathbf{A}_{\sigma(t)}\mathbf{z}(t) + \delta\mathbf{B}_{\sigma(t)}\mathbf{u}(t) \tag{6.10}$$

Let $\boldsymbol{\theta}^*$ be a vector containing the actual value of the unknown parameters of interest, and let $\boldsymbol{\theta}(t)$ be an estimate of $\boldsymbol{\theta}^*$. With appropriate parametrization, the state space model can be reorganized as follows:

$$\mathbf{A}_{\sigma(t)}\mathbf{x}(t) + \mathbf{B}_{\sigma(t)}\mathbf{u}(t) = \mathbf{W}_{\sigma(t)}(\mathbf{x}, \mathbf{u})\boldsymbol{\theta}^* \tag{6.11}$$

where $\mathbf{W}(\mathbf{x}, \mathbf{u})$ is a time-varying matrix that depends on the state and inputs.

We define $\boldsymbol{\phi}(t) \triangleq \boldsymbol{\theta}(t) - \boldsymbol{\theta}^*$ as the difference between the estimate and the actual value of the unknown parameters. Using this, we can rewrite (6.10) as:

$$\dot{\mathbf{e}}(t) = \mathbf{A}_{\sigma(t)}\mathbf{e}(t) + \mathbf{W}_{\sigma(t)}(\mathbf{z}, \mathbf{u})\boldsymbol{\phi}(t) \tag{6.12}$$

We can solve for the time domain evolution of $\dot{\mathbf{e}}(t)$ as follows:

$$\mathbf{e}(t) = \boldsymbol{\Phi}(t_0, t)\mathbf{e}(t_0) + \boldsymbol{\phi}\int_{t_0}^{t} \boldsymbol{\Phi}(t, \tau)\mathbf{W}_{\sigma(t)}(\mathbf{z}, \mathbf{u})\mathrm{d}\tau \tag{6.13}$$

Note that we assume the term $\boldsymbol{\phi}(t)$ evolves slowly (essentially constant) compared to the state dynamics such that they appear essentially constant; this allows us to bring the term outside of the integral. The corresponding error in the output $\boldsymbol{\gamma}(t) \triangleq \mathbf{C}\left(\mathbf{z}(t) - \mathbf{x}(t)\right)$ implies that:

$$\boldsymbol{\gamma}(t) = \mathbf{C}\left(\boldsymbol{\Phi}(t_0, t)\mathbf{e}(t_0) + \boldsymbol{\phi}\int_{t_0}^{t} \boldsymbol{\Phi}(t, \tau)\mathbf{W}_{\sigma(t)}(\mathbf{z}, \mathbf{u})\mathrm{d}\tau\right) \tag{6.14}$$

Finally, the term $\boldsymbol{\Phi}(t_0, t)\mathbf{e}(t_0)$ asymptotically decays to zero due to open loop stability, so the evolution of $\boldsymbol{\gamma}(t)$ is as follows:

$$\boldsymbol{\gamma}(t) = \mathbf{H}(t)\boldsymbol{\phi} \tag{6.15}$$

where $\mathbf{H}(t) = \mathbf{C}\int_{t_0}^{t} \boldsymbol{\Phi}(t, \tau)\mathbf{W}_{\sigma(t)}(\mathbf{z}, \mathbf{u})\mathrm{d}\tau$.

Example 6. Again, consider the interleaved boost converter topology in Fig. 6.1. The unknown parameters to be estimated are L_1, L_2, and C. The resulting expressions for $\mathbf{z}(t)$, $\boldsymbol{\theta}(t)$, and $\mathbf{W}_{\sigma(t)}(\mathbf{z}, \mathbf{u})$ are:

$$\mathbf{z}(t) = \begin{bmatrix} \hat{i}_{L_1}(t) \\ \hat{i}_{L_2}(t) \\ \hat{v}_C(t) \end{bmatrix}, \boldsymbol{\theta}(t) = \begin{bmatrix} \frac{1}{L_1(t)} \\ \frac{1}{L_2(t)} \\ \frac{1}{C(t)} \end{bmatrix},$$

$$\mathbf{W}_{\sigma(t)}(\mathbf{z}, \mathbf{u}) = \mathrm{diag}\begin{pmatrix} -R_1\hat{i}_{L_1}(t) - s_1\hat{v}_C(t) - v_{in}(t) \\ -R_2\hat{i}_{L_2}(t) - s_2\hat{v}_C(t) - v_{in}(t) \\ s_1\hat{i}_{L_1}(t) + s_2\hat{i}_{L_2}(t) - i_{load}(t) \end{pmatrix}$$

6.3 Summary

This chapter presented the modeling and estimation framework used to describe the dynamics of a switching power converter in nominal and faulted operating conditions. We described modeling techniques and state and parameter estimators for a broad class of power electronics circuits. The modeling and estimation framework are fundamental tools necessary for the proposed fault diagnosis methods that are discussed in Chapters 7 and 8.

Chapter 7

State Estimation-Based FDI Techniques

In this chapter, we discuss the analysis, design, and experimental validation of a model-based fault detection and identification (FDI) method for switching power converters using a model-based state estimator approach. The proposed FDI approach is general in that it can be used to detect and identify arbitrary faults in components and sensors in a broad class of switching power converters. The FDI approach is experimentally demonstrated on a nanogrid prototype with a 380 V DC distribution bus. The nanogrid consists of four different switching power converters, including a buck converter, an interleaved boost converter, a single-phase rectifier, and a three-phase inverter. We construct a library of fault signatures for possible component and sensor faults in all four converters. The FDI algorithm successfully achieves fault detection in under 400 μs and fault identification in under 10 ms for faults in each converter. The proposed FDI approach enables a flexible and scalable solution for improving fault tolerance and awareness in power electronics systems.

We present a generalized model-based methodology for fault detection and identification in switching power converters. The proposed FDI approach is general in that it can be used to detect and identify arbitrary faults in components and sensors in a broad class of switching power converters. More importantly, the modeling and implementation of the proposed FDI approach is flexible for both the converter topology and faults of interest; that is, one would require minimal effort to reconfigure an existing FDI implementation for a different converter topology or fault type. The proposed FDI method can be integrated with the existing control system of the switching power converter, requiring no additional electrical or computation

hardware. In essence, the FDI method enables a layer of intelligence on top of existing hardware protection such as fuses and circuit breakers.

The proposed FDI approach uses switched linear state estimator to generate a real-time error residual which captures the difference between the measured and estimator outputs (i.e. voltages and currents) of an arbitrary switching power converter. When a fault occurs in the converter, the error residual becomes non-zero, which enables fault detection. We show that the dynamics of the error residual can be used to achieve fault identification.

We present an experimental demonstration of the FDI approach on a nanogrid prototype with a 380 V DC distribution bus. The FDI algorithm is implemented on four different switching power converters–a buck converter, an interleaved boost converter, a single-phase rectifier, and a three-phase inverter. We validate the performance and speed of the FDI algorithm for a variety of component and sensor faults for each converter. We show that the FDI approach enables fast fault detection and fault identification with speed on the order of application-specific implementations in literature, but with the advantage of being converter- and fault-agnostic in terms of modeling and implementation.

The remainder of the chapter is organized as follows. Section 7.1 presents the proposed algorithm for fault detection and identification. Section 7.2 presents a simulation of the proposed FDI algorithm, and demonstrates its robustness in the presence of converter non-idealities such as switch and passive component parasitics and component parameter variations due to aging and degradation. In Section 7.3, we describe the nanogrid testbed used to experimentally validate the FDI algorithm. We present the techniques used to implement the FDI algorithm in real-time. Section 7.4 presents experimental results that verify the FDI algorithm on four different switching power converters. Section 7.5 concludes the chapter.

7.1 FDI Algorithm Design

In this section, we present the proposed algorithm design for fault detection and identification. The objectives of the algorithm are two-fold—(1) make a binary decision as to whether a component or sensor fault has occurred or not, and (2) if a fault has been detected, identify precisely the type and location of the faulted component or sensor.

Fundamentally, the proposed FDI algorithm consists of a switched linear state estimator that calculates an *error residual* between the measured output of the converter and

the estimated output. In the fault-free (nominal) condition, the residual approaches zero. However, when a component or sensor fault occurs, the residual becomes non-zero, enabling fault detection. Moreover, we show that for different faults, the residual vector evolves in a deterministic direction, which enables fault identification.

7.1.1 Fault detection

We can build a switched linear state estimator of the system from (6.1) as follows:

$$\dot{\mathbf{z}}(t) = \mathbf{A}_{\sigma(t)}\mathbf{z}(t) + \mathbf{B}_{\sigma(t)}\mathbf{u}(t) \tag{7.1}$$

$$\boldsymbol{\gamma}(t) = \mathbf{y}(t) - \mathbf{C}\mathbf{z}(t), \tag{7.2}$$

where $\mathbf{z}(t)$ is an estimate of the state vector $\mathbf{x}(t)$ from (6.1), and $\boldsymbol{\gamma}(t)$ is the *residual* of the difference between the measured output $\mathbf{y}(t)$ and the estimated output $\mathbf{C}\mathbf{z}(t)$. Fault detection is achieved by monitoring the norm of the residual $\boldsymbol{\gamma}(t)$ at each time step and comparing it with a predefined *fault detection threshold* Γ; the value of Γ is determined empirically. When $\|\boldsymbol{\gamma}(t)\|_2 > \Gamma$, the algorithm detects a fault.

7.1.1.1 Fault-free (nominal) condition

Let $\mathbf{e}(t) \triangleq \mathbf{z}(t) - \mathbf{x}(t)$. In the fault-free (nominal) condition, the dynamics of $\mathbf{e}(t)$ are governed by:

$$\dot{\mathbf{e}}(t) = \mathbf{A}_{\sigma(t)}\mathbf{e}(t) \tag{7.3}$$

$$\boldsymbol{\gamma}(t) = \mathbf{C}\mathbf{e}(t) \tag{7.4}$$

The open-loop error dynamics of the state estimator are stable (see [167]). Moreover, due to losses in the converter and corresponding model, the error residual is zero in the steady state for a fault-free system. Thus, $\boldsymbol{\gamma}(t) \to 0$ as $t \to \infty$, and no fault will be detected.

7.1.1.2 Component faults

When the i^{th} component fault occurs, the dynamics of the faulted converter can be modeled as in (6.4). Thus, in this case, the dynamics of $\mathbf{e}(t)$ are governed by:

$$\dot{\mathbf{e}}(t) = \mathbf{A}_{\sigma(t)}\mathbf{e}(t) - \boldsymbol{\phi_i}(\mathbf{x}, \mathbf{u})\mathbf{f_i} \tag{7.5}$$

$$\begin{aligned}\boldsymbol{\gamma}(t) = \mathbf{C}\mathbf{e}(t) = \mathbf{C}e^{-\mathbf{A}_{\sigma(t)}t}\mathbf{e}(0) + ... \\ ... + \mathbf{C}\,\mathbf{f_i}\int_0^t e^{-\mathbf{A}_{\sigma(t)}(t-\tau)}\phi_i(\mathbf{x}, \mathbf{u})\mathrm{d}\tau\end{aligned} \tag{7.6}$$

The term $\mathbf{C}e^{-\mathbf{A}_{\sigma(t)}t}\mathbf{e}(0)$ vanishes as $t \to \infty$, and thus $\mathbf{e}(t)$ is zero in the fault-free scenario. However, the (scalar) integral term $\int_0^t e^{-\mathbf{A}_{\sigma(t)}(t-\tau)}\phi_i(\mathbf{x},\mathbf{u})\mathrm{d}\tau$ will become non-zero depending on the dynamics of $\phi_i(\mathbf{x},\mathbf{u})$. Thus, when the magnitude of this term causes $\|\boldsymbol{\gamma}(t)\|_2 > \Gamma$, the algorithm will detect a fault.

7.1.1.3 Sensor faults

When the j^{th} sensor fault occurs, the dynamics of the faulted converter can be modeled as in (6.6). Thus, the dynamics of $\mathbf{e}(t)$ are governed by:

$$\dot{\mathbf{e}}(t) = \mathbf{A}_{\sigma(t)}\mathbf{e}(t) \tag{7.7}$$

$$\boldsymbol{\gamma}(t) = \mathbf{C}\mathbf{e}(t) - \theta_j(\mathbf{x})\mathbf{g_j} \tag{7.8}$$

The term $\mathbf{C}\mathbf{e}(t)$ vanishes as $t \to \infty$. However, the term $\theta_j(\mathbf{x})$ will become non-zero depending on the dynamics of $\theta_j(\mathbf{x})$. Thus, when the magnitude of this term causes $\|\boldsymbol{\gamma}(t)\|_2 > \Gamma$, the algorithm will detect a fault.

7.1.2 Fault identification

Fault identification is achieved via a two step process. First, prior to running the FDI algorithm, a collection of component fault signatures $\mathbf{f_i}$ and sensor fault signatures $\mathbf{g_j}$ are assembled into a *fault signature library*, as shown in Tables 7.1 and 7.2. The fault signatures are obtained by modeling faults of interest and extracting $\mathbf{f_i}$ and $\mathbf{g_j}$ mathematically via (6.4) and (6.6).

Second, over a time window of length W, we integrate the L^2-inner product between the residual $\boldsymbol{\gamma}(t)$ and every element of the fault signature library. Intuitively, this L^2-inner product will reveal which fault signature the residual most closely aligns with.

In the case of the i^{th} component fault, we see from (7.6) that $\boldsymbol{\gamma}(t)$ will align with $\mathbf{C}\,\mathbf{f_i}$. This can be calculated as follows:

$$\langle \boldsymbol{\gamma}(t), \mathbf{C}\,\mathbf{f_i}\rangle_{L^2} = \int_{t-W}^{t} \boldsymbol{\gamma}^T(\tau)\mathbf{C}\,\mathbf{f_i}\,\mathrm{d}\tau \tag{7.9}$$

where W is the window size of the inner product calculation. Similarly, for the j^{th} sensor fault, we see from (7.8) that $\boldsymbol{\gamma}(t)$ will align with $\mathbf{g_j}$. This can be calculated as follows:

$$\langle \boldsymbol{\gamma}(t), \mathbf{g_j}\rangle_{L^2} = \int_{t-W}^{t} \boldsymbol{\gamma}^T(\tau)\mathbf{g_j}\,\mathrm{d}\tau \tag{7.10}$$

When the magnitude of an inner product calculation result exceeds the predefined *fault identification threshold* Λ, the algorithm identifies the fault as the one associated with the appropriate fault signature.

In the instances when a component fault signature or sensor fault signature is not unique, the magnitude of the L^2-inner product can be used to identify the appropriate fault. Moreover, a frequency domain analysis of the residual $\boldsymbol{\gamma}(t)$ can also be used in order to identify the fault (as shown in [98]). However, the fault detection method remains unchanged.

Table 7.1: Component fault signature library.

Library element	Fault event	$\boldsymbol{\phi_i}(\mathbf{x}, \mathbf{u})$	$\mathbf{f_i}$
Buck converter			
$i = 1$	Change in capacitance by ΔC	$\frac{\Delta C}{C(C+\Delta C)}(i_{load}(t) - i_L(t))$	$[0, 1]^T$
$i = 2$	Open circuit fault in SW_1	$-\frac{s_1}{L}v_{in}(t)$	$[1, 0]^T$
Interleaved boost converter			
$i = 3$	Change in capacitance by ΔC	$\frac{\Delta C}{C(C+\Delta C)}(i_{load} - s_2 i_{L_1} - s_4 i_{L_2})$	$[0, 0, 1]^T$
$i = 4$	Change in phase 1 series resistance by ΔR_1	$-\frac{\Delta R_1}{L} i_{L_1}(t)$	$[1, 0, 0]^T$
$i = 5$	Change in phase 2 series resistance by ΔR_2	$-\frac{\Delta R_2}{L} i_{L_2}(t)$	$[0, 1, 0]^T$
$i = 6$	Open circuit fault in SW_2	s_2	$[\frac{v_C(t)}{L_1}, 0, -\frac{i_{L_1}}{C}]^T$
$i = 7$	Open circuit fault in SW_4	s_4	$[0, \frac{v_C(t)}{L_2}, -\frac{i_{L_2}}{C}]^T$
Single-phase rectifier			
$i = 8$	Change in capacitance by ΔC	$\frac{\Delta C}{C(C+\Delta C)}(i_{load}(t) - i_L(t))$	$[0, 1]^T$
Three-phase inverter			
$i = 9$	Change in phase a series resistance by ΔR_a	$\frac{\Delta R_a}{3L} i_a(t)$	$[-2, 1, 1]^T$
$i = 10$	Change in phase b series resistance by ΔR_b	$\frac{\Delta R_b}{3L} i_b(t)$	$[1, -2, 1]^T$
$i = 11$	Change in phase c series resistance by ΔR_c	$\frac{\Delta R_c}{3L} i_c(t)$	$[1, 1, -2]^T$

Table 7.2: Sensor fault signature library.

Library element	Fault event	$\boldsymbol{\theta_j}(\mathbf{x})$	$\mathbf{g_j}$
Buck converter			
$j = 1$	Fault in $i_L(t)$ sensor	$\Delta c_1(t) i_L(t) + \Delta e_1(t)$	$[1, 0]^T$
$j = 2$	Fault in $v_C(t)$ sensor	$\Delta c_2(t) v_C(t) + \Delta e_2(t)$	$[0, 1]^T$
Interleaved boost converter			
$j = 3$	Fault in $i_{L_1}(t)$ sensor	$\Delta c_3(t) i_{L_1}(t) + \Delta e_3(t)$	$[1, 0, 0]^T$
$j = 4$	Fault in $i_{L_2}(t)$ sensor	$\Delta c_4(t) i_{L_2}(t) + \Delta e_4(t)$	$[0, 1, 0]^T$
$j = 5$	Fault in $v_C(t)$ sensor	$\Delta c_5(t) v_C(t) + \Delta e_5(t)$	$[0, 0, 1]^T$
Single-phase rectifier			
$j = 6$	Fault in $i_L(t)$ sensor	$\Delta c_6(t) i_L(t) + \Delta e_6(t)$	$[1, 0]^T$
$j = 7$	Fault in $v_C(t)$ sensor	$\Delta c_7(t) v_C(t) + \Delta e_7(t)$	$[0, 1]^T$
Three-phase inverter			
$j = 8$	Fault in $i_{L_a}(t)$ sensor	$\Delta c_8(t) i_{L_a}(t) + \Delta e_8(t)$	$[1, 0, 0]^T$
$j = 9$	Fault in $i_{L_b}(t)$ sensor	$\Delta c_9(t) i_{L_b}(t) + \Delta e_9(t)$	$[0, 1, 0]^T$
$j = 10$	Fault in $i_{L_c}(t)$ sensor	$\Delta c_{10}(t) i_{L_c}(t) + \Delta e_{10}(t)$	$[0, 0, 1]^T$

7.2 Simulation and Robustness Analysis

In this section, we present a simulation of the FDI algorithm using the boost converter as an illustrating example. The FDI algorithm uses the 'ideal' model shown in Fig. 6.1 and developed in Example 1. However, the boost converter plant is simulated using the model shown in Fig. 7.1, which accounts for switch and passive component parasitics and also component parameter variations in the output capacitance C, the input inductance L_1, and the ESR of the output capacitance R_{esr}. These parasitics and parameter variations are used to test the robustness of both the fault detection and fault identification algorithms in the presence of such converter non-idealities. Fig. 7.2 shows the dyanmics of the parasitic model in steady state with nominal component parameters. Variations in the input voltage $v_{in}(t)$ and the load current $i_{load}(t)$ do not influence the FDI algorithm as these variables are explicitly measured from the plant and fed into the state estimator via the input vector $\mathbf{u}(t)$.

The implementation details of the simulation are as follows. The converter and FDI algorithm are co-simulated at the minimum and maximum of each parameter variation, that is, at the corners of the accepted parameter space of (L_1, C, R_{esr}). The residual $\boldsymbol{\gamma}(t)$ is normalized to the appropriate V_{base} and I_{base} shown in Table 7.3. The dimensionless fault detection threshold Γ is selected such that the worst-case voltage and current transients

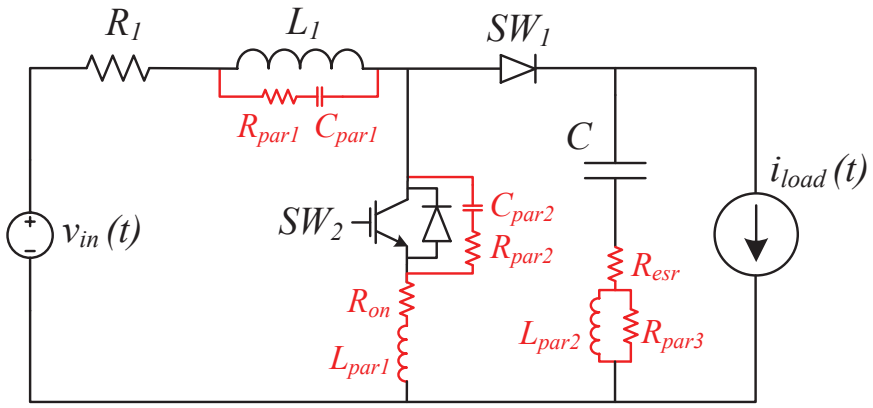
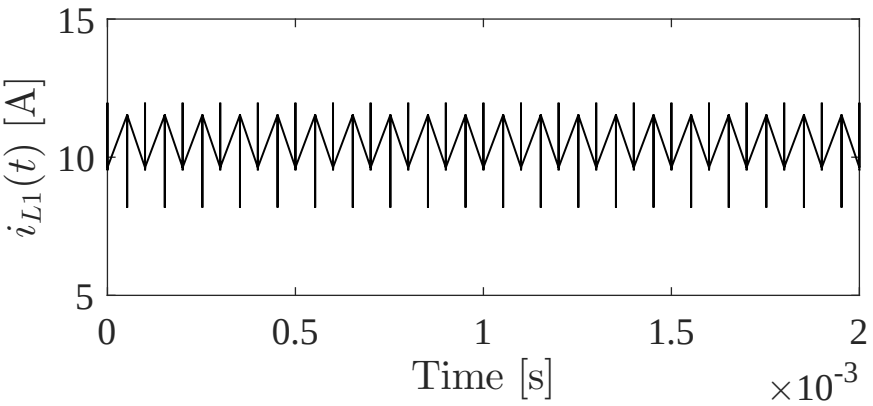


Figure 7.1: Boost converter model with switch and passive component parasitics.

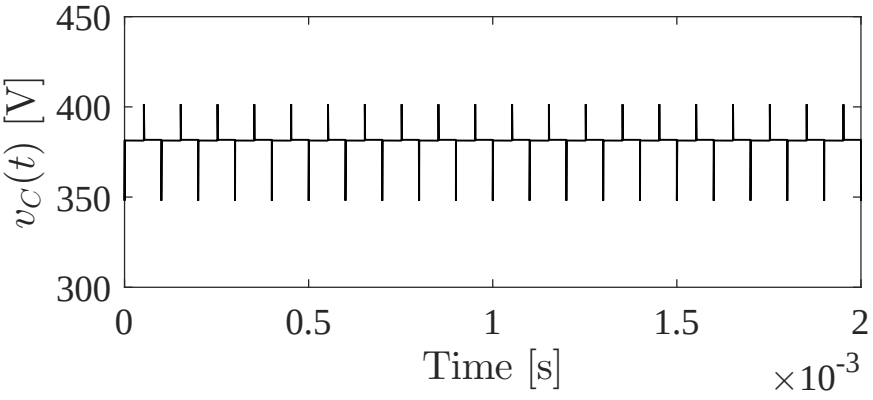
Table 7.3: Simulation parameters for boost converter.

Component parameters	
C	2200 μF $\pm$20%
L_1	5.00 mH $\pm$20%
R	25 mΩ
Parasitic parameters	
R_{esr}	38 mΩ $\pm$50%
R_{on}	1 mΩ
$R_{par1,2}$	100 Ω
R_{par3}	5 Ω
C_{par1}	1 pF
C_{par2}	1 nF
L_{par1}	5.00 nH
L_{par2}	1 nH
Operating point	
$v_{in}(t)$	190 V
$i_{load}(t)$	5 A
Switching frequency	10 kHz
V_{base}	380 V
I_{base}	10 A

related to circuit parasitics do not cause $\|\boldsymbol{\gamma}(t)\|_2$ to exceed the fault detection threshold Γ. Similar design considerations are used to select the dimensionless fault identification threshold Λ. For the simulations, we select $\Gamma = 0.5$ and $\Lambda = 0.1$. Of the eight corners of the accepted parameter space that are simulated, the worst-case scenario with respect to dynamics adversely affecting $\boldsymbol{\gamma}(t)$ occurs at $(\min(L_1), \max(C), \max(R_{esr})$. Our selection of



(a) Inductor current $i_{L_1}(t)$.



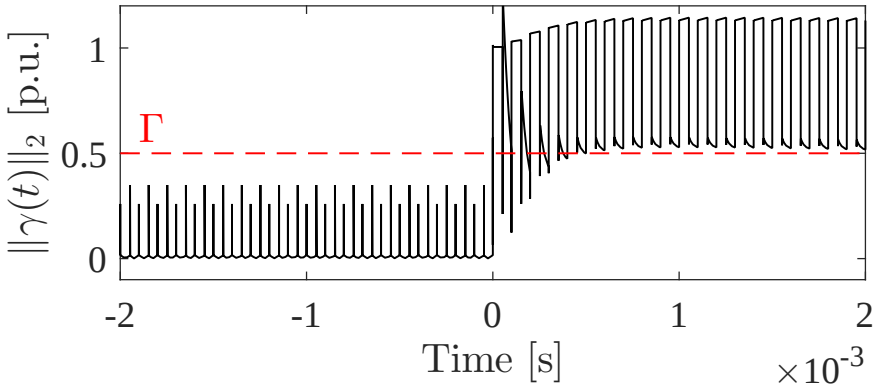
(b) Capacitor voltage $v_C(t)$.

Figure 7.2: Steady state dynamics of boost converter model with switch and passive component parasitics (Fig. 7.1) with nominal component parameters.

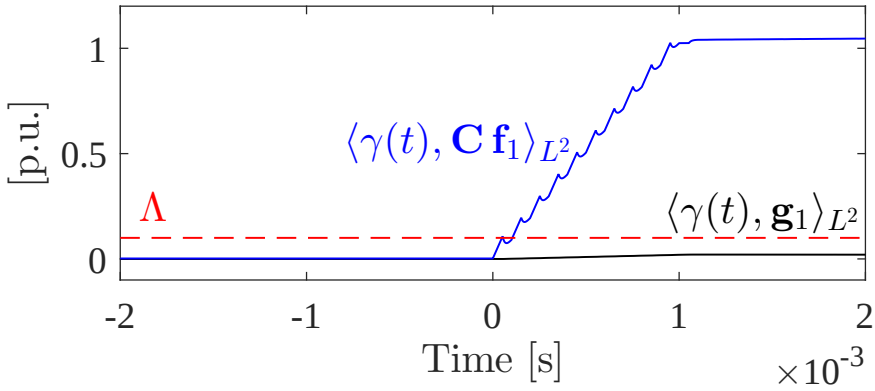
Γ and Λ provide sufficient tolerance to prevent false positives while still ensuring minimal time to fault detection and identification.

The fault signature library for the simulation contains two fault signatures: (1) $\mathbf{f_1}$, the component fault signature for a fault in the output capacitor C, as derived in Example 3, and (2) $\mathbf{g_1}$, the sensor fault signature for a fault in the input inductor L_1 current sensor, as derived in Example 4.

First, we simulate a fault in the output capacitor causing $C \to 0$. The fault emulates the dynamics of a capacitor open circuit fault, which can be caused by a rapid increase of R_{esr}. As shown in Fig. 7.3a, fault detection occurs essentially instantaneously as $\|\boldsymbol{\gamma}(t)\|_2$ exceeds the fault detection threshold Γ at $t = 0$. Fig. 7.3b shows the L^2-inner product between $\boldsymbol{\gamma}(t)$ and $\mathbf{C}\,\mathbf{f_1}$ and $\mathbf{g_1}$. As shown, the residual correctly aligns with $\mathbf{C}\,\mathbf{f_1}$, and exceeds the fault



(a) Plot of $\|\boldsymbol{\gamma}(t)\|_2$ and the fault detection threshold Γ.



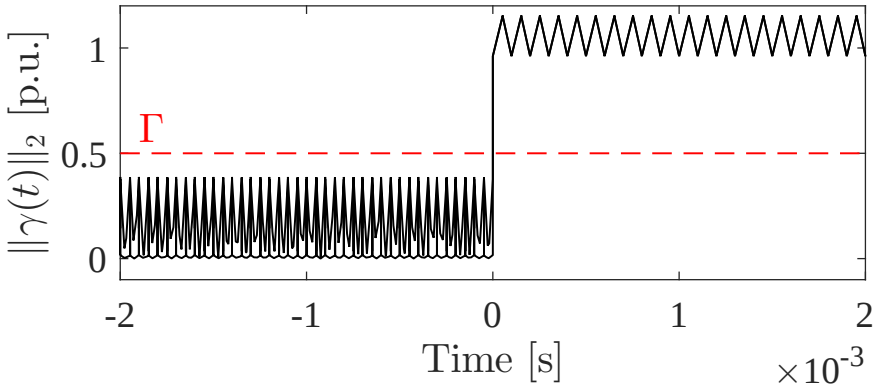
(b) Plot of $\langle \boldsymbol{\gamma}(t), \mathbf{C}\,\mathbf{f_1} \rangle_{L^2}$, $\langle \boldsymbol{\gamma}(t), \mathbf{g_1} \rangle_{L^2}$, and the fault identification threshold Λ.

Figure 7.3: Simulation of the FDI algorithm for a capacitor fault injected at $t = 0$ causing $C \to 0$. Shown is the worst-case scenario caused by parameter variation $(\min(L_1), \max(C), \max(R_{esr})$.

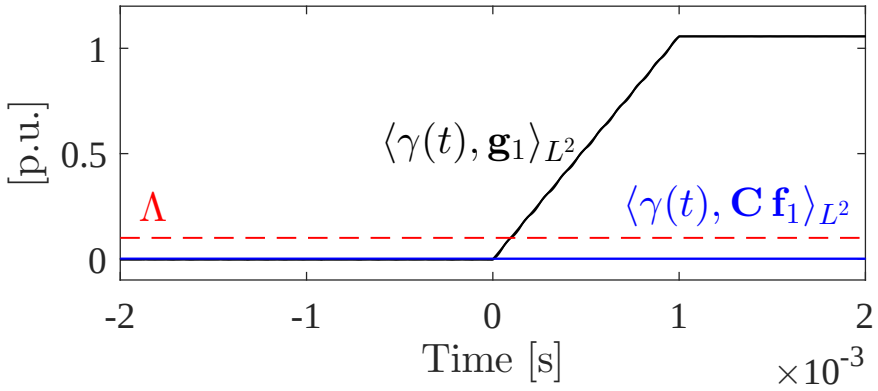
identification threshold Λ in 0.2-0.3 ms. Conversely, the L^2-inner product between $\boldsymbol{\gamma}(t)$ and $\mathbf{g_1}$ remains at zero, demonstrating the selectivity of the method.

Second, we simulate a fault in the input inductor L_1 current sensor causing the sensor gain $c_1(t) \to 0$. Again, fault detection occurs essentially instantaneously as shown in Fig. 7.4a. Fault identification occurs in 0.1 ms, as the residual correctly aligns with $\mathbf{g_1}$ as shown in Fig. 7.4b. The L^2-inner product between $\boldsymbol{\gamma}(t)$ and $\mathbf{C}\,\mathbf{f_1}$ remains at zero.

In both fault cases, the FDI algorithm is able to correctly detect and identify the appropriate fault even in the preswence of the non-ideal plant dynamics. For fault detection, the threshold Γ prevents any dynamics caused by parasitics or component parameter variation from raising a false fault detection flag. For fault identification, the moving window W of the L^2-inner product provides an added benefit as a natural low-pass filter that removes the effects of parasitic ringing and transients. The fault identification threshold Λ accounts for



(a) Plot of $\|\boldsymbol{\gamma}(t)\|_2$ and the fault detection threshold Γ.



(b) Plot of $\langle \boldsymbol{\gamma}(t), \mathbf{C}\,\mathbf{f_1} \rangle_{L^2}$, $\langle \boldsymbol{\gamma}(t), \mathbf{g_1} \rangle_{L^2}$, and the fault identification threshold Λ.

Figure 7.4: Simulation of the FDI algorithm for a fault in the input inductor L_1 current sensor injected at $t = 0$. Shown is the worst-case scenario caused by parameter variation $(\min(L_1), \max(C), \max(R_{esr})$.

dynamics caused by variations in component parameters.

7.3 Implementation and Nanogrid Testbed

In this section, we present a prototype nanogrid used to validate the FDI algorithm on four switching power converters. Moreover, we discuss the real-time implementation of the FDI algorithm proposed in Section 7.1. A photograph of the prototype nanogrid and FDI computing platform is shown in Fig. 7.5. The complete specifications and ratings are presented in Table 7.4.

Table 7.4: Specifications and ratings for nanogrid testbed.

PV emulator ratings	150 V, 40 A, 2 kW
AC grid emulator ratings	305 V_{rms}, 11 A_{rms}, 1 kVA
Controlled DC load	150 V, 33 A, 165 W
Three-phase AC load	220 V_{rms}, 8.7 A_{rms}, 3.3 kW
Switching node ratings	1200 V, 25 A, IP67 enclosure
IGBT module	Infineon FS25R12W1T4
Gate driver	Semikron SKHI 61R
Current sensors	LEM LA25-NP
Voltage sensors	LEM LV25-P
Buck and interleaved boost converter	
L, per phase	5.00 mH
R, per phase	0.82 Ω
C	2200 μF
Rectifier and three-phase inverter	
L, per phase	5.00 mH
R, per phase	25 mΩ
C	2200 μF
FDI computing platform	
Model	dSPACE DS1103 controller
Controller time step	100 μs
Converter switching frequency	10 to 20 kHz
Real-time model-based estimator	
Model	Typhoon HIL602
Simulation time step	500 ns
PWM sampling interval	20 ns
ADC/DAC sampling rate	1 MHz

7.3.1 Nanogrid testbed

The prototype nanogrid testbed consists of four converters that interface two sources—a PV emulator and a single phase AC grid emulator—with two loads—a controlled DC load and a resistive three-phase load—through an intermediate 380 VDC distribution bus. The circuit schematics of all four converters are shown in Fig. 5.1. An MPPT-controlled interleaved boost converter interfaces the PV emulator with the DC distribution bus. A single-phase rectifier interfaces the AC grid emulator to the DC bus. A buck converter and three-phase inverter are used to interface the DC load and three-phase AC load, respectively.

The design of each converter is modularized by using a standardized *switching node*.

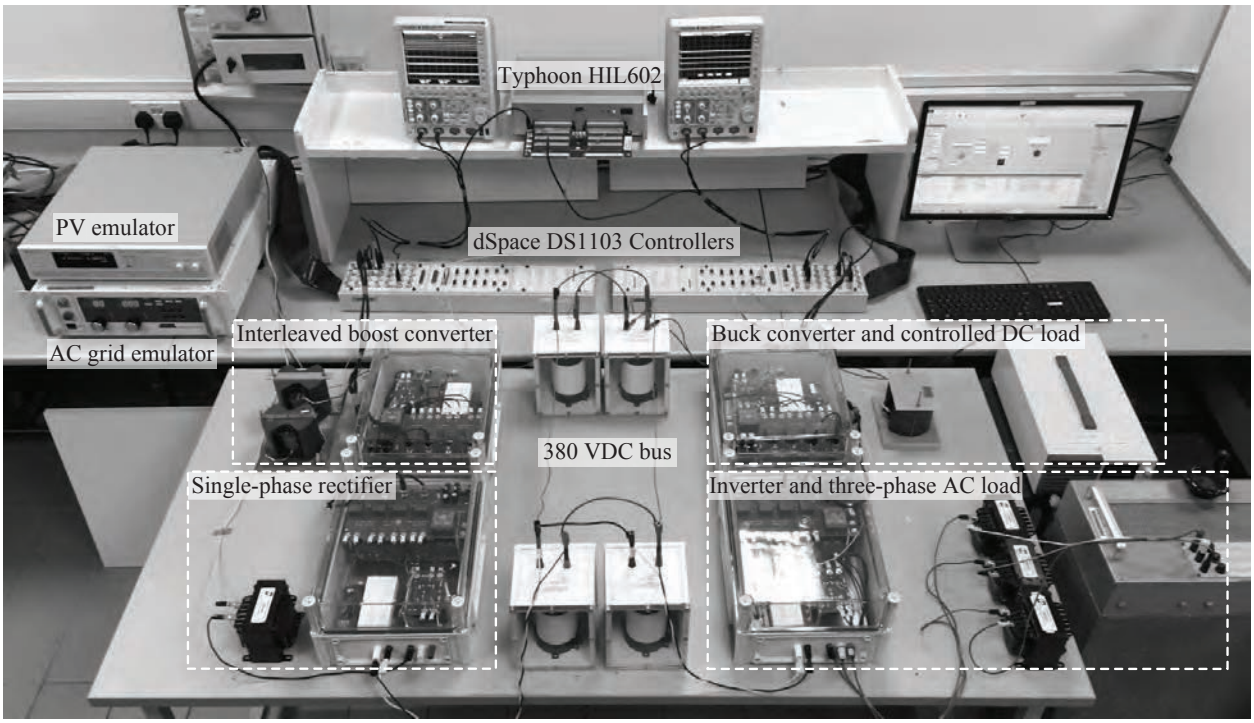


Figure 7.5: Photograph of the FDI computing platform and prototype nanogrid testbed.

A switching node consists of a sixpack IGBT module configured as three half-bridges, a gate driver module, and four current and four voltage sensors all enclosed in an IP67 rated enclosure. The implementation of the switching node is shown in Fig. 7.6. A switching node is configured with appropriate passive elements to form each of the four converters.

Finally, two dSPACE D1103 controller boards implement the closed-loop control for each converter. It is worth noting that the converters are controlled individually, that is, there is no supervisory controller for the entire nanogrid testbed.

7.3.2 FDI computing platform

The FDI algorithm is implemented on two separate real-time computing devices. First, the state estimator discussed in Section 7.1 is implemented on a Typhoon HIL602. The FPGA processor architecture of this device is tailored for solving switched linear state space models of power electronics systems with a fixed simulation time step of 500 ns, including input-output latency [168]. Moreover, the multi-core architecture enables multiple state estimators of independent converters to be solved simultaneously. This allows us to run the state estimation algorithm for each of the four converters in parallel on a single device.

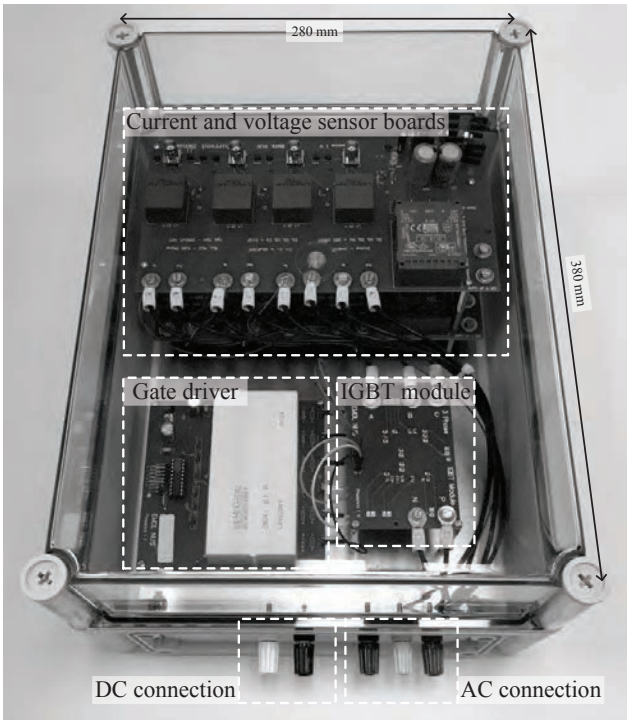
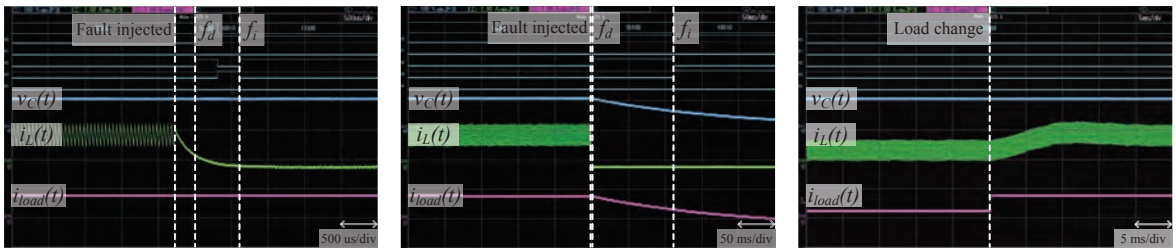


Figure 7.6: Switching node implementation.

Second, the fault detection and identification algorithms are implemented on the dSPACE DS1103 controller boards. These devices, in addition to operating the closed-loop control for each converter, execute the FDI algorithm discussed in Sections 7.1.1 and 7.1.2. That is, for each converter, the DS1103 performs the following tasks: (1) stores the fault signature library, (2) generates an error residual based on signals from the converter sensors and the state estimator output, and (3) generates fault detection and fault identification flags based on the magnitude of the error residual and the L^2-inner product calculation.

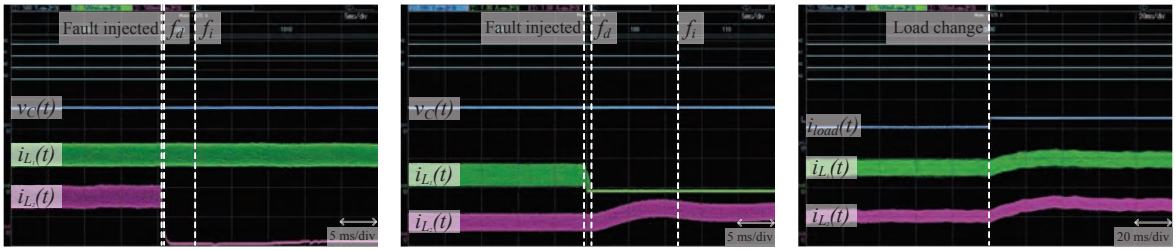
7.4 Experimental Results

In this section, we present experimental results of the proposed FDI algorithm on the testbed presented in Section 7.3. Figs. 7.7, 7.8, 7.9, and 7.10 show the dynamics of various faults and load changes in four different converters, where f_d indicates the instance of fault detection, and f_i indicate the instance of fault identification. For each converter, we choose the fault detection threshold $\Gamma = 0.5$ and the fault identification threshold $\Lambda = 0.1$. In every test case, these values provide sufficient tolerance to dynamics caused by converter non-idealities, such



(a) Sensor fault in $i_L(t)$ sensor. (b) Open switch fault in SW_1. (c) Load step change in $i_{load}(t)$.

Figure 7.7: Verification of the FDI method for a variety of fault and operating scenarios for a buck converter. In each scenario, the fault or event is injected at the instant as labeled, and the times to fault detection and fault identification are indicated by the digital traces. Analog waveforms shown are the capacitor voltage $v_C(t)$, the inductor current $i_L(t)$, and the load current $i_{load}(t)$.



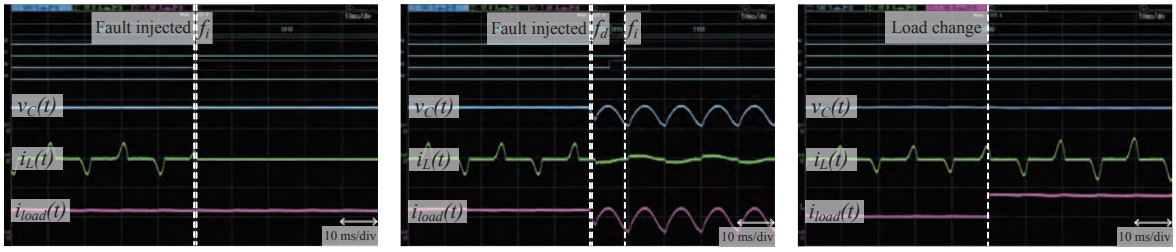
(a) Sensor fault in $i_{L_2}(t)$ sensor. (b) Open phase fault in phase 1. (c) Load step change in $i_{load}(t)$.

Figure 7.8: Verification of the FDI method for a variety of fault and operating scenarios for an interleaved boost converter. In each scenario, the fault or event is injected at the instant as labeled, and the times to fault detection and fault identification are indicated by the digital traces. Analog waveforms shown are the capacitor voltage $v_C(t)$ and the inductor currents $i_{L_1}(t)$ and $i_{L_2}(t)$.

as parasitics and parameter variation.

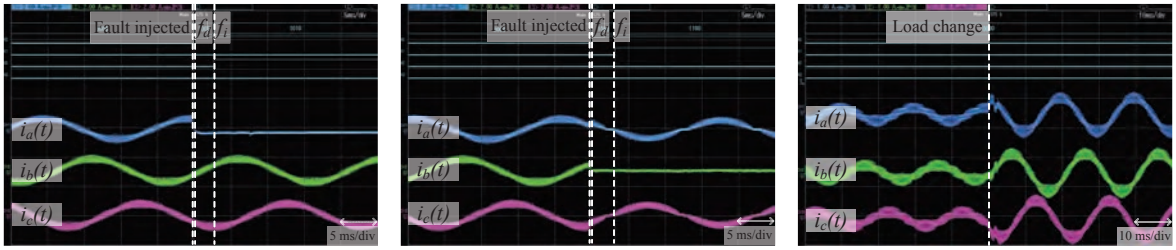
Table 7.5 presents the experimentally measured time to fault detection (t_d) and time to fault identification (t_i) for each fault. For most faults, the time to fault detection is one or two time steps of the real-time FDI computing platform (in this case, fixed time step is 100 μs for the dSPACE DS1103 controller). The time to fault identification generally depends on the dynamics of the particular fault and how fast the fault signature evolves.

Additionally, for each converter, we test load changes in order to demonstrate that the FDI algorithm is immune to events external to the switching power converter, such as changes in load or input power, or faults in elements external to the converter. In this way, fault or events in one converter will not influence the FDI algorithm in a separate converter.



(a) Sensor fault in $i_L(t)$ sensor. (b) Capacitor fault causing $C \to 0$. (c) Load step change in $i_{load}(t)$.

Figure 7.9: Verification of the FDI method for a variety of fault and operating scenarios for a single-phase rectifier. In each scenario, the fault or event is injected at the instant as labeled, and the times to fault detection and fault identification are indicated by the digital traces. Analog waveforms shown are the output capacitor voltage $v_C(t)$, the input inductor current $i_L(t)$, and the load current $i_{load}(t)$.



(a) Sensor fault in $i_a(t)$ sensor. (b) Open phase fault in phase b. (c) Balanced load change in R_l.

Figure 7.10: Verification of the FDI method for a variety of fault and operating scenarios for a three-phase inverter. In each scenario, the fault or event is injected at the instant as labeled, and the times to fault detection and fault identification are indicated by the digital traces. Analog waveforms shown are the three phase currents $i_a(t)$, $i_b(t)$, and $i_c(t)$.

7.4.1 Buck converter (Fig. 7.7)

The dynamics of a fault in the current sensor ($i_L(t)$) that force the sensor gain to zero are shown in Fig. 7.7a. As shown, when the fault is injected, the measured $i_L(t)$ begins to exponentially decay, while the dynamics of $v_C(t)$ and $i_{load}(t)$ remain unchanged. The FDI algorithm detects the current sensor fault in 280 μs, and correctly identifies the fault in 880 μs.

Fig. 7.7b shows the dynamics of an open switch fault in SW_1. The current in the inductor $i_L(t)$ immediately becomes zero, while the capacitor begins discharging across the output load. This fault is detected in 360 μs. The time to fault identification depends on the RC time constant of the output capacitor and resistive load, as this will determine how fast the fault signature evolves. In this case, fault identification requires 113 ms.

Finally, Fig. 7.7c shows the response of the system to a step change in the load current. As shown, the step change causes the inductor current $i_L(t)$ to increase. However, the FDI

Table 7.5: Experimentally measured time to fault detection (t_d) and time to fault identification (t_i).

		t_d	t_i
Buck converter			
Current sensor fault	Fig. 7.7a	280 μs	880 μs
Open circuit fault	Fig. 7.7b	132 μs	113 ms
Load change	Fig. 7.7c	-	-
Interleaved boost converter			
Current sensor fault	Fig. 7.8a	360 μs	4.4 ms
Phase open circuit fault	Fig. 7.8b	340 μs	8.65 ms
Load change	Fig. 7.8c	-	-
Single-phase rectifier			
Current sensor fault	Fig. 7.9a	146 μs	456 μs
Capacitor fault	Fig. 7.9b	400 μs	9.3 ms
Load change	Fig. 7.9c	-	-
Three-phase inverter			
Current sensor fault	Fig. 7.10a	220 μs	2.90 ms
Phase open circuit fault	Fig. 7.10b	170 μs	3.45 ms
Load change	Fig. 7.10c	-	-

algorithm recognizes this as an external event to the switching power converter, and does not raise a fault flag.

7.4.2 Interleaved boost converter (Fig. 7.8)

Fig. 7.8a shows the dynamics of a sensor fault in $i_{L_2}(t)$ that force the sensor gain to zero. The measured current in $i_{L_2}(t)$ becomes zero, while $v_C(t)$ and $i_{L_1}(t)$ remain unchanged. The fault is detected in 360 μs, and is identified in 4.4 ms.

The dynamics of an open phase 1 fault are shown in Fig. 7.8b. As shown, the current $i_{L_1}(t)$ immediately becomes zero, and the current $i_{L_2}(t)$ increases in order to compensate for the lost phase. The output voltage $v_C(t)$ remains unchanged. The FDI algorithm detects this fault in 340 μs, and identifies it in 8.65 ms.

Fig. 7.8c shows the response of the system to a step change in the load current $i_{load}(t)$. The load increase causes a balanced increase in the currents flowing through both phases ($i_{L_1}(t)$ and $i_{L_2}(t)$). Again, since this is a normal external event, the FDI algorithm does not detect it as a fault.

7.4.3 Single-phase rectifier (Fig. 7.9)

The dynamics of a current sensor fault ($i_L(t)$) are shown in Fig. 7.9a. As shown, the measured current becomes zero, while the remaining measured outputs ($v_C(t)$ and $i_{load}(t)$) remain unchanged. This fault is detected in 146 μs, and identified in 456 μs.

Fig. 7.9b shows the response of the system when the output capacitance C of the rectifier becomes 0. As shown, the fault causes a large periodic ripple in the output voltage $v_C(t)$, while subsequently causing a distorted waveform in the inductor current $i_L(t)$. The FDI algorithm detects the capacitor fault in 400 μs, and correctly identifies the fault in 9.3 ms.

Finally, Fig. 7.9c shows the response of the system to a step change in the output load. As shown, the periodic current pulses in $i_L(t)$ become larger, while the output voltage $v_C(t)$ remains unchanged. The FDI algorithm does not raise a fault flag for this external event.

7.4.4 Three-phase inverter (Fig. 7.10)

Fig. 7.10a shows the dynamics of a current sensor fault in phase a of the three-phase inverter. As shown, the measured current $i_a(t)$ immediately becomes zero, while the current in the remaining two phases are unchanged. The FDI algorithm detects the fault in 220 μs, and identifies it in 2.90 ms.

Next, Fig. 7.10b shows the response of the system during the phase b open circuit fault. This fault can be modeled as a sharp increase in the series resistance R_b. The current in phase b immediately becomes zero, while the currents in phase a and c become 180 degrees out of phase. The fault is detected in 170 μs, and is correctly identified in 3.45 ms.

Lastly, the dynamics of a balanced load change are shown in Fig. 7.10c. As shown, the load change causes a balanced increase in the currents in all three phases of the inverter. Again, the FDI algorithm does not raise a fault flag for this external event.

7.5 Summary

This chapter has demonstrated an approach to model-based fault detection and identification for arbitrary switching power converters. The approach is experimentally implemented and validated for four different converter topologies that demonstrate the applicability of the FDI method for a nanogrid setting. The experimental results show the efficacy of the proposed approach for fast fault detection and identification for a variety of common fault

events in switching power converters. In this way, the proposed fault FDI method enables a flexible solution for improving reliability and fault tolerance in an array of power electronics applications.

Chapter 8

Parameter Estimation-Based FDI Techniques

This chapter presents the design, implementation, and experimental validation of a method for fault prognosis for power electronics systems using an adaptive parameter identification approach. The adaptive parameter identifier uses a generalized gradient descent algorithm to compute real-time estimates of system parameters (e.g. capacitance, inductance, parasitic resistance) in arbitrary switching power electronics systems. These estimates can be used to monitor the overall health of a power electronics system, and predict when faults are more likely to occur. Moreover, the estimates can be used to tune control loops that rely on the system parameter values. The parameter identification algorithm is general in that it can be applied to a broad class of switching power converters if the parameters of interest can be formulated as linear inputs to a linear ordinary differential equation. We present a real-time experimental validation of the proposed fault prognosis method on a 3 kW solar photovoltaic interleaved boost dc-dc converter system for tracking changes in passive component values. The proposed fault prognosis method enables a flexible and scalable solution for condition monitoring and fault prediction in power electronics systems.

We present a technique for fault prognosis for power electronics systems using an adaptive parameter identifier approach. The fundamental algorithm (proposed in [163]) uses a switched linear model of a switching power converter and a generalized gradient descent algorithm to dynamically track the values of passive components, such as capacitors and inductors, in a power electronics converter. The algorithm is digitally implemented in real-time on the same embedded processor as the control system, and is used to monitor when

passive component parameter values are above or below a predefined tolerance range, which would indicate a fault scenario.

The design advantages of the proposed method compared to state-of-the-art is threefold. First, the modeling and identification algorithm is general to encapsulate arbitrary switching power converters in which parameters of interest can be formulated as linear inputs to a linear ordinary differential equation. Thus, although the focus of this work is on dc-dc converters for solar photovoltaic applications, the technique can also be applied in the context of motor drive applications, cable integrity monitoring, among others. Second, the real-time algorithm is implemented *digitally*, as opposed to techniques that require custom analog implementations for each converter or estimated parameter. Moreover, the algorithm has low computational overhead, which enables it to be implemented on the same computing platform as the control system. Third, the proposed approach requires no additional sensors or computing devices (aside from those already used for closed-loop control purposes), or injection of external signals into the system.

The remainder of the chapter is outlined as follows. Section 8.1 presents the modeling approach and algorithm design of the proposed adaptive parameter identifier. Section 8.2 presents a simulation of the identifier algorithm for an interleaved boost dc-dc converter. The simulation tests a variety of operating points and parameter perturbations, and provides a simulation analysis of the robustness of the algorithm to measurement noise and converter non-idealities. Section 8.3 describes the hardware implementation and experimental testbed. Section 8.4 presents experimental results which validate the real-time implementation of the algorithm on a 3 kW dc-dc converter. Section 8.5 concludes the chapter.

8.1 Adaptive Parameter Identifier Design

In this section, we present a gradient descent algorithm that is used to track perturbed parameter values and reconstruct estimates of the actual parameter values.

The objective of the adaptive parameter identifier is to perturb the parameter estimate vector $\boldsymbol{\theta}(t)$ as to drive the measured output error $\boldsymbol{\gamma}(t)$ to zero. In this way, we expect $\boldsymbol{\theta}(t)$ to converge to the actual parameter values $\boldsymbol{\theta}^*$.

There are a number of algorithms available for adaptive parameter identification [169]. For purposes of simplicity in design and implementation, we propose the use of a generalized gradient descent algorithm [169, 163]. The structure of the gradient descent algorithm is as

follows:

$$\dot{\boldsymbol{\theta}}(t) = -\mathbf{G}\,\mathbf{H}^T(t)\,\boldsymbol{\gamma}(t) \tag{8.1}$$

where $\mathbf{G} \succ 0$ is a positive definite matrix gain which is used to control the rate of convergence of the error term $\boldsymbol{\gamma}(t)$ to zero. The structure of $\mathbf{G}$ can be of the form $\text{diag}(\epsilon_1, ..., \epsilon_n)$, where n is the number of terms to be identified, and each ϵ term is parameter update gain for the associated unknown parameter.

The matrix gain $\mathbf{G}$, in general, influences the rate of convergence and the stability of the gradient descent algorithm. The design of $\mathbf{G}$ depends on a number of factors (see [163] for a mathematical analysis). Among these include:

1. *Persistency of excitation of* $\mathbf{H}(t)$. The gradient descent algorithm requires that $\mathbf{H}(t)$ satisfies a persistency of excitation condition [169]. Practically, this implies that the input $\mathbf{u}(t)$, the input voltage and load current in Examples 1 and 2, are varying with time sufficiently such that the dynamics of the system make the parameter identification possible. This condition is satisfied in many practical applications where the pulse width modulation of switching power converters can provide a sufficiently rich excitation. Similarly, in a solar photovoltaic system, the time-varying irradiation and temperature of the solar panel can cause variations in the input voltage and load current, providing further excitation and information for the estimation.

2. *Number of measurements versus number of unknown parameters.* The number of measurements available can influence the excitation of $\mathbf{H}(t)$. Likewise, as the number of unknown parameters increases, the amount of excitation in $\mathbf{H}(t)$ required for the gradient descent algorithm to converge also increases. Thus, it is can be straightforward to achieve convergence when the number of unknown parameters is less than or equal to the number of available measurements. Applying the gradient descent problem to the scenario with more unknown parameters than available measurements can be an ill-posed problem if sufficiently rich inputs are not applied.

3. *Desired convergence rate.* Each ϵ is chosen such that the dynamics of $\dot{\boldsymbol{\theta}}(t)$ evolve much slower than the state dynamics, in order to satisfy the assumption made in Eq. (6.13). Moreover, in the case of multiple unknown parameters, ϵ can be chosen such that all parameters exhibit similar convergence rates so certain parameters do not converge much faster than others.

Finally, we require an estimate of $\mathbf{H}(t)$ as follows:

$$\hat{\mathbf{H}}(t) = \mathbf{C} \int_{t_0}^{t} \hat{\mathbf{\Phi}}(t,\tau)\mathbf{W}_{\sigma(t)}(\mathbf{z},\mathbf{u})\mathrm{d}\tau \tag{8.2}$$

where $\hat{\mathbf{\Phi}}$ uses updated parameters from $\dot{\boldsymbol{\theta}}(t)$ to provide an estimate of the state transition matrix $\mathbf{\Phi}$.

The complete adaptive parameter observer is shown here:

$$\dot{\mathbf{z}}(t) = \hat{\mathbf{A}}_{\sigma(t)}\mathbf{z}(t) + \hat{\mathbf{B}}_{\sigma(t)}\mathbf{u}(t) \tag{8.3}$$

$$\boldsymbol{\gamma}(t) = \mathbf{C}\,\mathbf{z}(t) - \mathbf{y}(t) \tag{8.4}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\hat{\mathbf{H}}(t) = \hat{\mathbf{A}}_{\sigma(t)}\hat{\mathbf{H}}(t) + \mathbf{W}(\mathbf{z},\mathbf{u}) \tag{8.5}$$

$$\dot{\boldsymbol{\theta}}(t) = -\mathbf{G}\,\mathbf{H}^{T}(t)\,\boldsymbol{\gamma}(t) \tag{8.6}$$

8.2 Simulation and Analysis

In this section, a variety of MATLAB simulations are used in order to validate the performance and robustness of the proposed adaptive parameter identifier for a number of test cases and operating conditions. The interleaved boost dc-dc converter of Fig. 6.1 is used as the device-under-test. Table 8.1 presents the converter parameters and operating point for the nominal simulation cases.

In order to implement the adaptive parameter identifier in a simulation environment, Eqs. (8.3), (8.4), (8.5), and (8.6) are discretized using the Euler method, and executed in a simulation loop with a fixed 500 ns time step. We inject perturbations in the output capacitor and a series input inductor of the plant converter using additional shunt and series elements. For the purposes of fault monitoring, one can define a lower and upper bound of the acceptable range of parameter value. When the estimated parameter value leaves the acceptable range, a fault flag can be raised.

The output measurements, unknown parameter vector, and gain matrix from Examples 1 and 2 are used in the simulation; that is:

$$\mathbf{y}(t) = \begin{bmatrix} i_{in}(t) \\ v_{out}(t) \end{bmatrix}, \; \mathbf{C} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

Table 8.1: Simulation and experiment parameters.

Component parameters	
$R_{1,2}$	0.082 Ω
$L_{1,2}$ (nominal)	5.0 mH
C (nominal)	2.85 mF
Simulated parasitic parameters (Section 8.2.4)	
R_{esr}	38 mΩ ±50%
R_{on}	1 mΩ
$R_{par1,2}$	100 Ω
R_{par3}	5 Ω
C_{par1}	1 pF
C_{par2}	1 nF
L_{par1}	5.00 nH
L_{par2}	1 nH
Nominal operating point	
$v_{in}(t)$	100 V
$v_{out}(t)$	380 V
$i_{load}(t)$	2.5 A + 1 A, 10 Hz ripple
Converter switching frequency	10 kHz
Adaptive parameter identifier gains	
ϵ_1, ϵ_2 ($L_1(t)$, $L_2(t)$)	$1 \cdot 10^6$
ϵ_3 ($C(t)$)	$3 \cdot 10^6$
Embedded computing platform	
Device	Zynq-7000 SoC XC7Z020
Fixed computation time step	500 ns
Voltage sensor bandwidth	100 kHz
Current sensor bandwidth	200 kHz

$$\boldsymbol{\theta}(t) = \begin{bmatrix} \frac{1}{L_1(t)} \\ \frac{1}{L_2(t)} \\ \frac{1}{C(t)} \end{bmatrix}, \ \mathbf{G} = \begin{bmatrix} \epsilon_1 & 0 & 0 \\ 0 & \epsilon_2 & 0 \\ 0 & 0 & \epsilon_3 \end{bmatrix}$$

For simulation and experiments, we estimate either one or two parameters at a time. For these scenarios, the ϵ_i associated with the i^{th} desired parameter(s) to be estimated are set to the value shown in Table 8.1, and the j^{th} parameter(s) not being estimated has $\epsilon_j = 0$.

Moreover, in all simulation cases, a 1 A peak-to-peak ripple at 10 Hz is added to the 2 A load current $i_{load}(t)$. In addition to emulating time-varying load dynamics, this ripple introduces the persistency of excitation to $\mathbf{H}(t)$ that is necessary for the convergence of the error term $\boldsymbol{\gamma}(t)$ to zero. A similar perturbation could be added to the input voltage $v_{out}(t)$

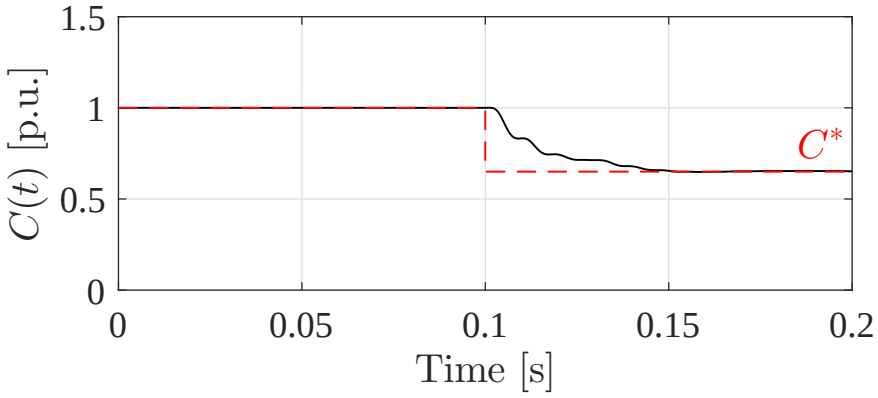


Figure 8.1: Simulation of the adaptive parameter identifier tracking a step perturbation in capacitance C ($t = 0.1$s from C to $0.65\,C$).

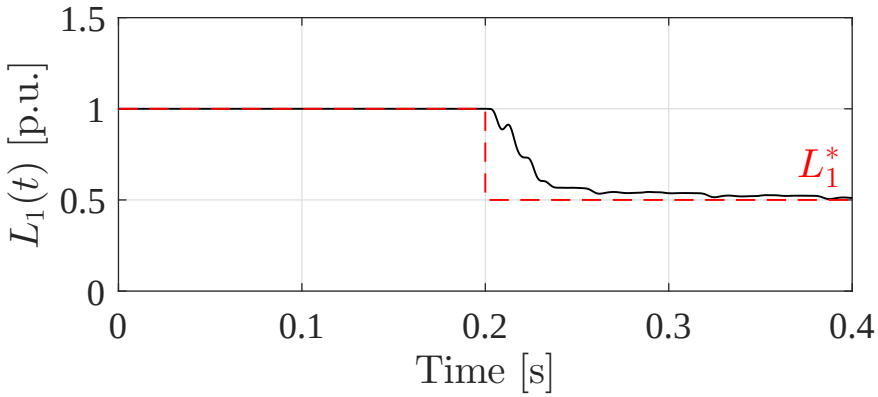


Figure 8.2: Simulation of the adaptive parameter identifier tracking a step perturbation in inductance L_1 ($t = 0.2$s from L_1 to $0.5\,L_1$).

that would emulate the time-varying photovolatic irradiation.

8.2.1 Step perturbation in single parameter

One application of the proposed adaptive parameter identifier is the tracking of 'hard' faults in passive components, that is drastic changes in the parameter value indicative of a catastrophic component failure. To simulate these types of faults, we introduced a step perturbation in the parameter value of passive components in the plant. As shown in Fig. 8.1, when a 35% step perturbation introduced in the capacitance C, the estimate $C(t)$ converges to the correct value in around 50 ms. Similarly, when a 50% step perturbation introduced in the series inductance L_1 in Fig. 8.2, the estimate $L_1(t)$ converges to the correct value in around 100 ms.

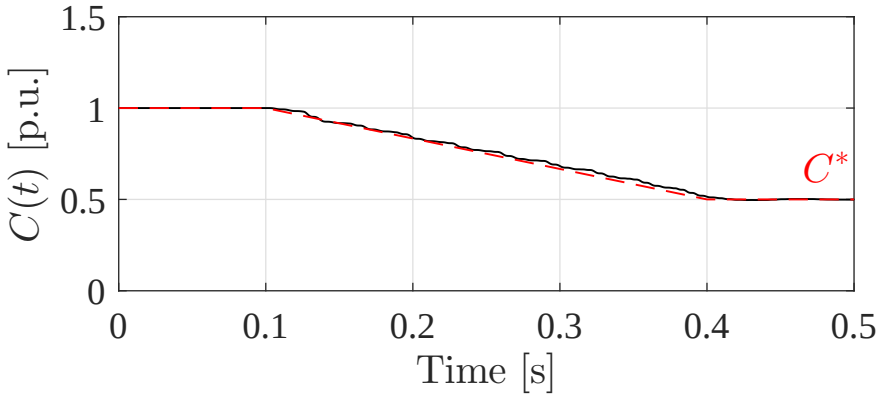


Figure 8.3: Simulation of the adaptive parameter identifier tracking a ramp perturbation in capacitance C (-166.7 μF/s from C to $0.5\,C$).

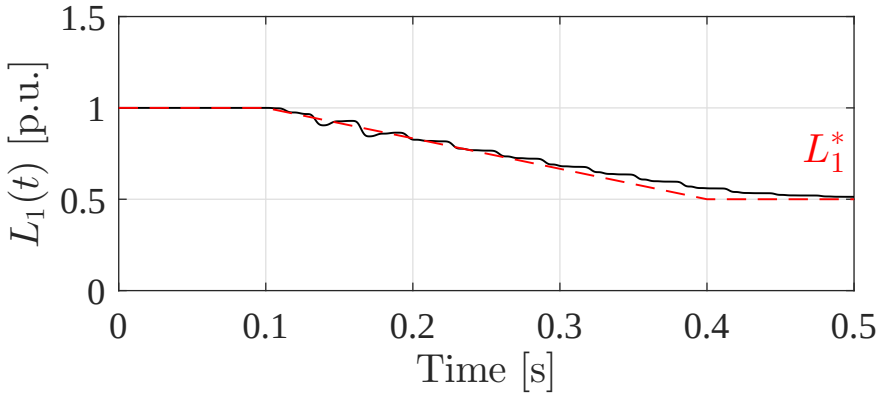


Figure 8.4: Simulation of the adaptive parameter identifier tracking a ramp perturbation in inductance L_1 (-16.7 mH/s at $t = 0.1$s from L_1 to $0.5\,L_1$).

8.2.2 Ramp perturbation in single parameter

Another application of the proposed adaptive parameter identifier is the tracking of slow varying perturbations in the parameter values of passive components. These types of slow varying changes occur on the time scale of hours to years, and represent a type of 'soft' fault, that is, gradual changes indicative of lifetime wear or aging.

We simulated ramp perturbations in the model to emulate these types of faults. First, a ramp perturbation of -166.7 μF/s is introduced in the output capacitor C. This is a relatively fast perturbation meant to identify the upper limit of accuracy of the adaptive parameter identifier. Slower perturbations are tracked at equal or better accuracy. As shown in Fig. 8.3, the adaptive parameter identifier tracks the correct value of this perturbation with unnoticeable error. Similarly, we introduced a ramp perturbation of -16.7 mH/s in a

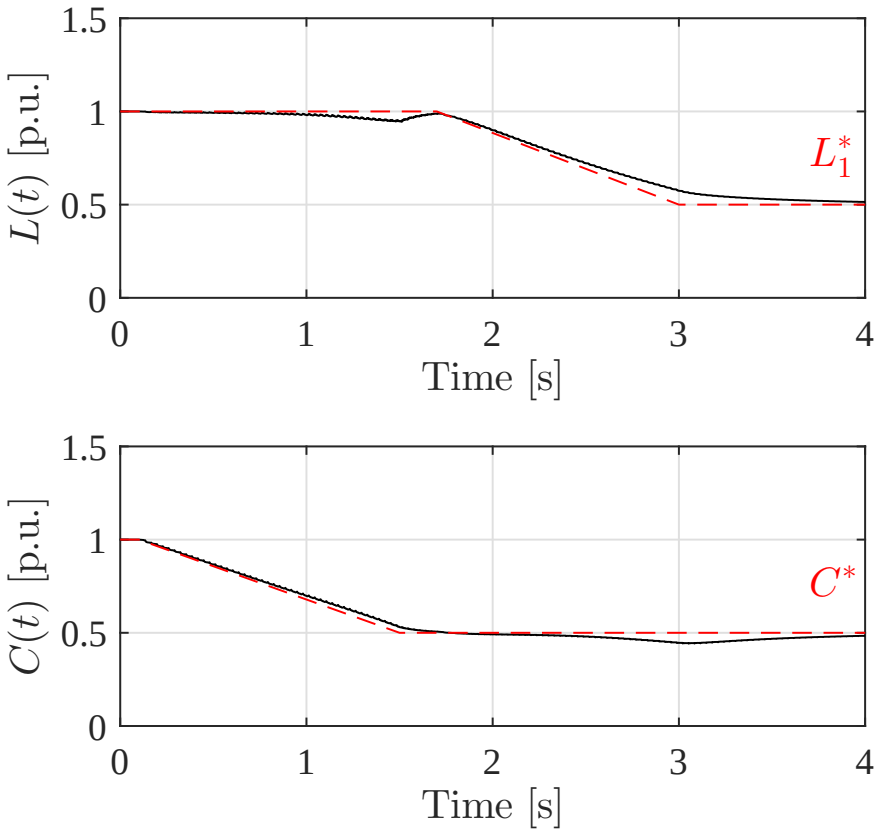


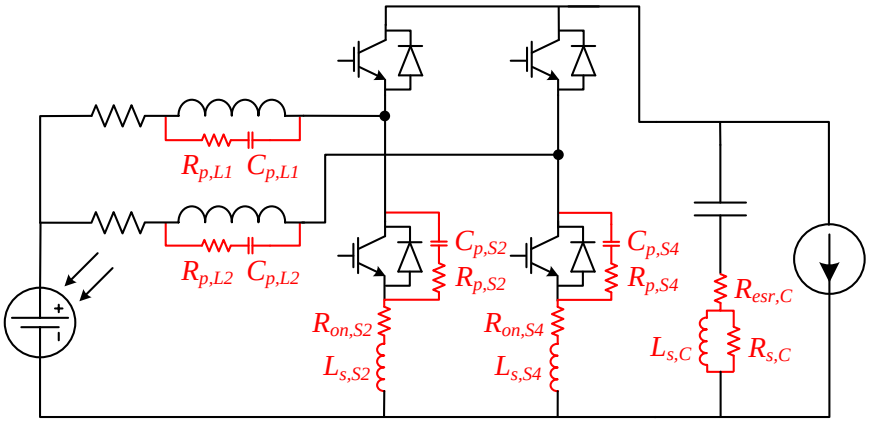
Figure 8.5: Simulation of adaptive parameter identifier tracking simultaneous ramp perturbations in inductance L_1 (-1.9 mH/s at $t = 1.75$ s) and capacitance (-35.7 μF/s from C to $0.5\,C$ at $t = 0.2$ s).

series input inductor L_1. As shown in Fig. 8.4, the adaptive parameter identifier again tracks the correct value of this perturbation.

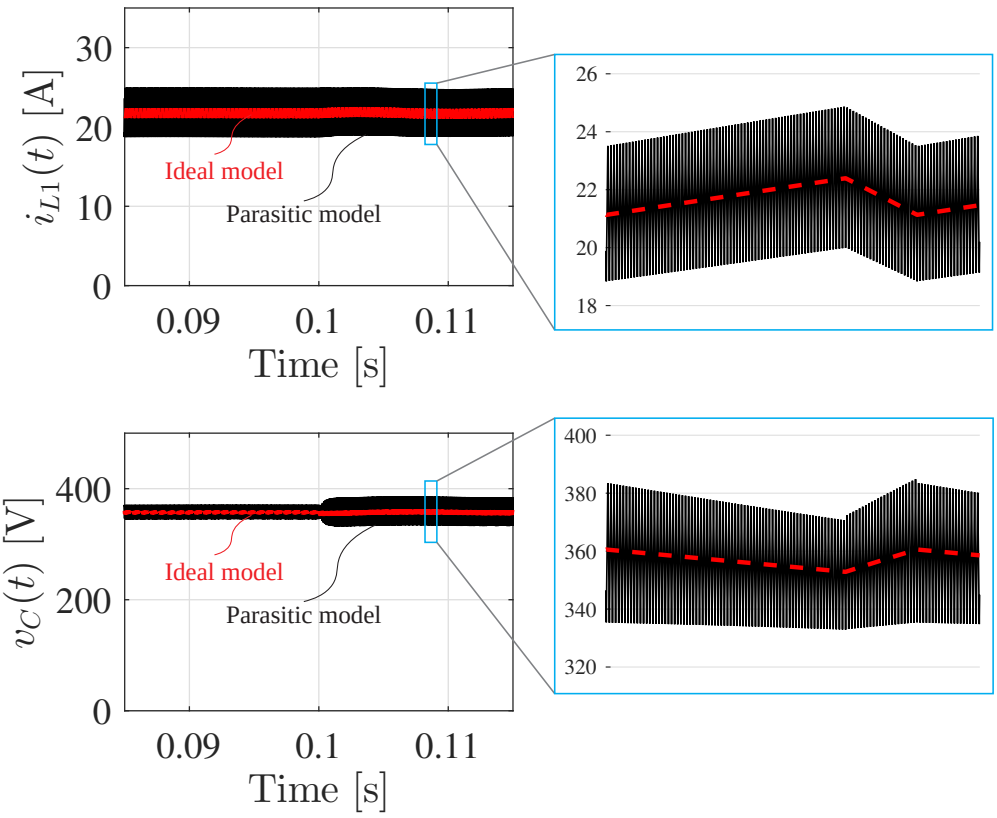
8.2.3 Simultaneous perturbation in multiple parameters

In general, more than one unknown parameter will be of interest in the system. From the analysis in Section 8.1, we expect that the convergence rate of $\boldsymbol{\theta}(t)$ will be slower than if only one parameter is being estimated. This is due to the corresponding increase in the error $e(t)$ and decrease in the excitation in $\mathbf{H}(t)$.

To test this scenario, we simulated a simultaneous ramp perturbation in both the output capacitor C and a series input inductor L_1. The rate of change of these parameter values was set at -1.9 mH/s and -35.7 μF/s, respectively. As shown in Fig. 8.5, the adaptive parameter identifier tracks the correct value of this perturbation with unnoticeable error. Slower perturbations are tracked at equal or better accuracy.

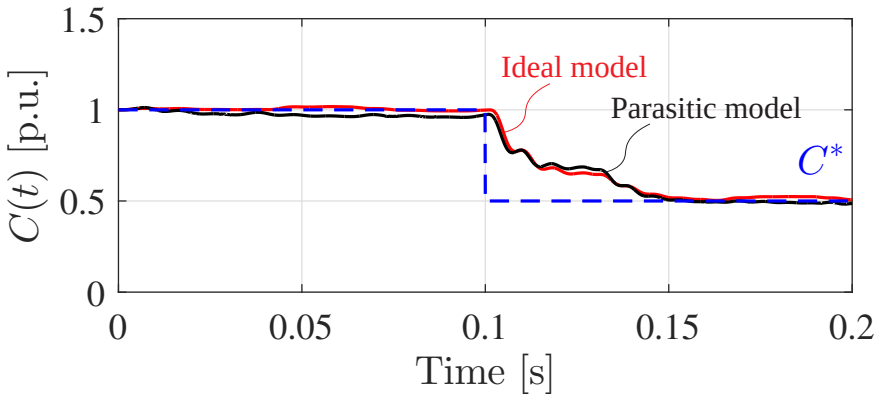


(a) Circuit topology of the parasitic simulation model.

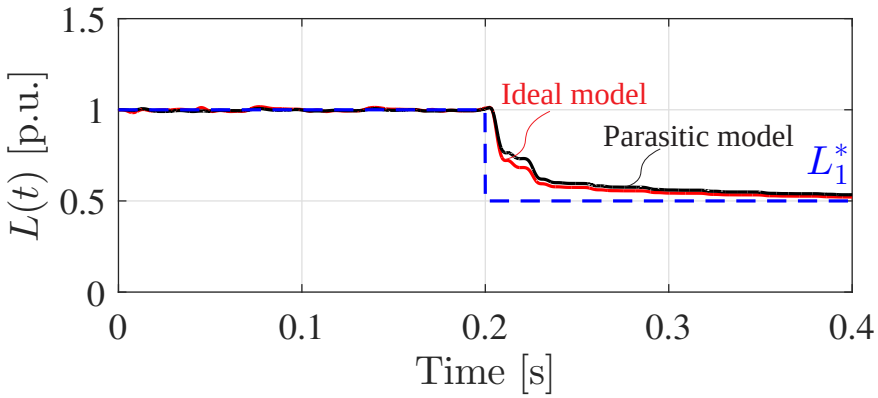


(b) Steady state dynamics of the ideal (from Fig. 6.1) and parasitic simulation model.

Figure 8.6: A simulation of an interleaved boost dc-dc converter incorporating switch and passive component parasitics and non-idealities is used to validate the robustness of the proposed adaptive parameter identifier.



(a) Step perturbation at $t = 0.1$s from C to $0.5\,C$.



(b) Step perturbation at $t = 0.2$s from L_1 to $0.5\,L_1$.

Figure 8.7: Comparison of the adaptive parameter identifier convergence when applied to the ideal model (Fig. 6.1) versus parasitic model (Fig. 8.6a).

8.2.4 Effect of measurement noise and circuit non-idealities

Simulation was also used to test the robustness of the proposed adaptive parameter identifier to measurement noise and parameter and model non-idealities. The modified circuit model in Fig. 8.6a is used to test this scenario. Note that the adaptive parameter identifier still uses the 'ideal' circuit model in Fig. 6.1, while the modified circuit model provides the measurement vector $\mathbf{y}(t)$. As shown, the modified circuit model incorporates switch and passive component parasitics, including the ESR of the output capacitance $R_{esr,C}$. The steady state dynamics are shown in Fig. 8.6b. As shown, when compared with the steady state dynamics of the ideal model, the parasitic model introduces high frequency current transients of approximately 4 A_{pk-pk} in the series inductor currents $i_L(t)$, and voltage transients of approximately 20 V_{pk-pk} in the output capacitor voltage $v_C(t)$.

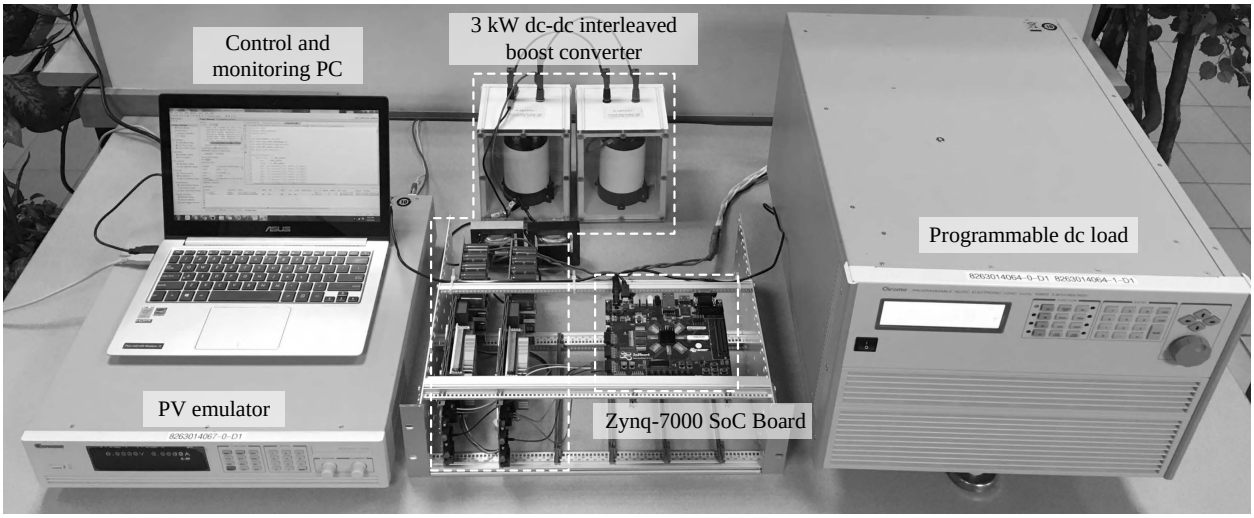


Figure 8.8: Photograph of the experimental testbed, including the interleaved dc-dc converter and the Zynq-7000 SoC board.

We study the impact of the parameter and model non-idealities and parasitics on the convergence of the adaptive parameter identifier. The parameter step perturbation from Section 8.2.1 is used as a baseline to compare the ideal and parasitic models. As shown in Fig. 8.7, the parasitic model causes minimal difference in the dynamics of the adaptive parameter identifier for parameter step changes in both the output capacitor C and a series inductor L_1. This provides evidence that the algorithm is robust to the non-ideal dynamics introduced by the parasitics.A central reason for this is the design of the adaptive parameter identifier. In (6.13), we assumed that the $\boldsymbol{\phi}(t)$ evolves slowly (essentially constant) compared to the state dynamics. Dynamics introduced by parasitics or measurement noise occur on a time scale faster than that of the state dynamics and are ignored by the parameter identification.

8.3 Hardware Implementation and Experimental Testbed

In this section, we present the hardware implementation and experimental testbed for the proposed fault prognosis algorithm. The complete testbed is shown in Fig. 8.8. The complete specifications for the experimental testbed and computing platform are given in Table 8.1.

8.3.1 Real-time digital implementation

The fault prognosis algorithm is implemented in real-time on the same computing device as the control system, in this case, a ZedBoard system-on-chip (SoC) device, a relatively low-cost development board for the Xilinx Zynq-7000 SoC XC7Z020. A central feature of this SoC is the integration programmable logic and a dual-core ARM Cortex-A9 processor. It is worth noting that our implementation only utilized 11 percent of the programmable logic slices of the device. Moreover, the ARM core was not used in the design. Thus, the algorithm could be implemented on a much lower cost FPGA. In general, however, a programmable logic device is preferred for implementation (as opposed to a standard microcontroller) due to the tight constraints on latency and computation time imposed by the fault prognosis algorithm.

The adaptive parameter identifier in Eqs. (8.3), (8.4), (8.5), and (8.6) is discretized and solved in real-time with a fixed time step (including input/output latency) of 500 ns. This time step, which is an order of magnitude faster than the switching frequency of the converter (10 kHz), is necessary to adequately model the switching dynamics of the converter.

Moreover, a highlight of the approach and implementation is that it maintains the flexibility to be reconfigured for different converters simply by changing the contents of the $\hat{\mathbf{A}}_{\sigma(t)}$, $\hat{\mathbf{B}}_{\sigma(t)}$, and $\mathbf{W}(\mathbf{z}, \mathbf{u})$ matrices. The selection of the $\boldsymbol{\theta}(t)$ vector indicates the parameters of interest to be estimated.

8.3.2 Experimental testbed

We experimentally validate the proposed fault prognosis method on a 3 kW interleaved dc-dc converter as shown in Fig. 8.8. The input of the converter is connected to a programmable photovoltaic (PV) emulator, and the output is connected to a programmable dc load. Prior to running the experiments, the values of passive components are measured using an LCR meter. The setup is equipped such that the value of the output capacitor C and a series inductor L_1 can be changed in real-time by controlling solid-state switches that introduce series or parallel elements into the circuit.

8.4 Experimental Results

This section presents experimental results which validate the proposed fault prognosis algorithm under a variety of operating conditions.

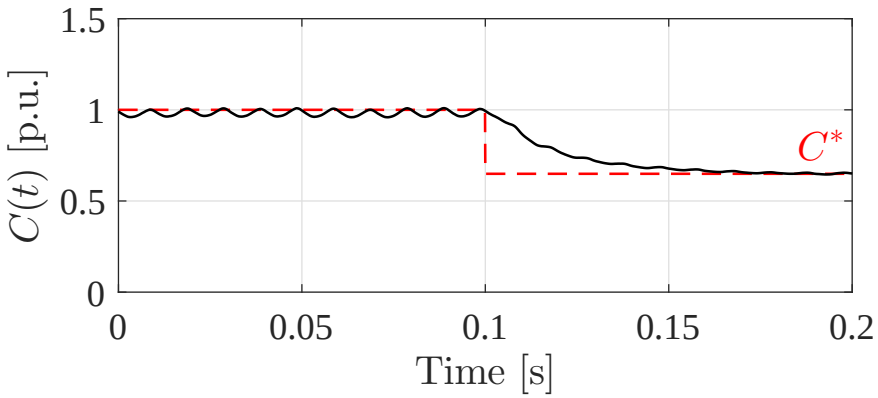


Figure 8.9: Experiment of adaptive parameter identifier tracking a step perturbation in capacitance C. Step perturbation at $t = 0.1$ s from C to $0.65\,C$.

We test step changes in the value of the output capacitor C and a series inductor L_1. Similar to the simulations performed in Section 8.2.1, the hard fault instantaneously changes the value of the capacitor and the inductor, and we monitor the convergence of the adaptive parameter identifier to the new value. Moreover, we test the effect of changing the dynamics of the load current $i_{load}(t)$ on the speed of convergence of $\boldsymbol{\theta}(t)$.

For the following experiments, the same output measurements, unknown parameter vector, and gain matrix are used as in Section 8.2. Relevant parameter values and operating points can be found in Table 8.1.

8.4.1 Step perturbation in C and L_1

Fig. 8.9 shows a fault that causes the output capacitance C to decrease from 2.85 mF to 1.85 mF, a decrease of 35%. As shown, the adaptive parameter identifier converges to the new value of C in approximately 50 ms. Similarly, Fig. 8.10 shows a fault that causes a series inductor L_1 to decrease by 50%. Convergence to the new value of L_1 takes approximately 100 ms. These values match the expected time of convergence from simulations in Section 8.2.1.

8.4.2 Effect of dynamic operating conditions

Next, we varied the frequency of the load current $i_{load}(t)$ and observed its effect on the convergence of $\boldsymbol{\theta}(t)$. We expect that a lower $i_{load}(t)$ frequency will result in less excitation in $\mathbf{H}(t)$. Thus, with a constant matrix gain $\mathbf{G}$, the rate of convergence of $\boldsymbol{\theta}(t)$ will be slower.

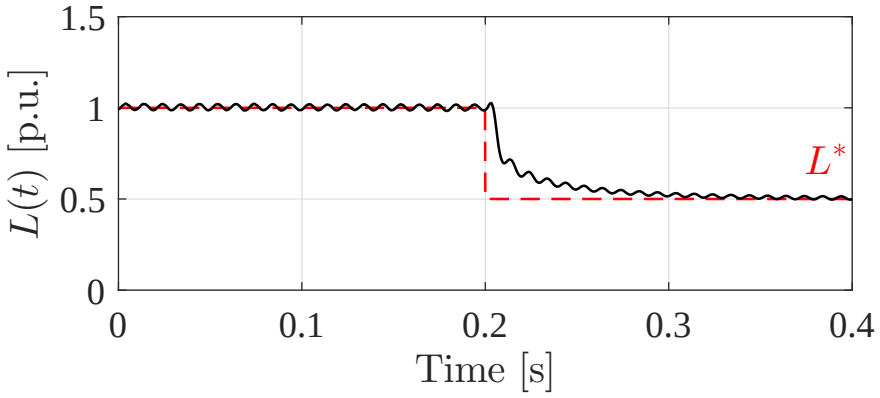


Figure 8.10: Experiment of adaptive parameter identifier tracking a step perturbation in inductance L_1. Step perturbation at $t = 0.2$ s from L to $0.5\,L$.

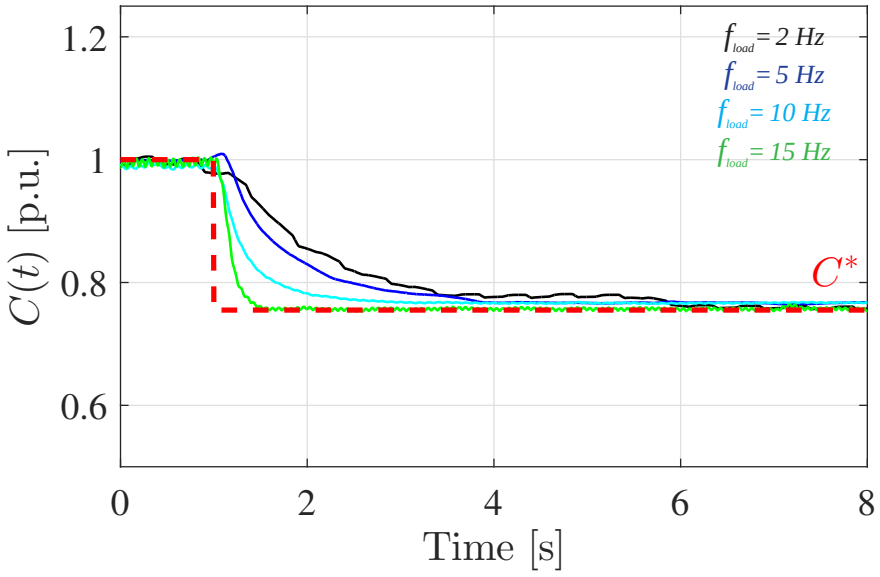


Figure 8.11: Experiment of adaptive parameter identifier tracking step perturbations in capacitance C for a set of $i_{load}(t)$ ripple frequencies: 2 Hz, 5 Hz, 10 Hz, and 15 Hz. Step perturbation at $t = 1$ s from C to $0.65\,C$.

For higher $i_{load}(t)$ frequencies, we expect the converse to be true.

We inject a step change in the output capacitance C from 2.85 mF to 1.85 mF for a set of $i_{load}(t)$ ripple frequencies: 2 Hz, 5 Hz, 10 Hz, and 15 Hz. Fig. 8.11 shows the results of this test. As shown, when the load has a 15 Hz ripple, convergence to the new value of C takes approximately 50 ms. At slower ripple frequencies (e.g. 2 Hz), convergence to the new value of C can take as long as 3 s. These results match our expectations, and also provide an empirical method for determining the rate of convergence of $\boldsymbol{\theta}(t)$ given a certain input

vector $\mathbf{u}(t)$.

8.5 Summary

This chapter presented a method for fault prognosis using an adaptive parameter identification approach. The salient advantages of the approach include application flexibility and the obviated need for additional sensors, computing devices, or injected signals. The proposed technique can be applied in domains including motor drive applications (for stator or rotor resistance estimation), cable integrity monitoring, or other applications where parameter or system identification is a useful technique for fault prognosis or prediction.

Chapter 9

Conclusions

This dissertation presented circuit, control, and optimization techniques for power electronics that can naturally coordinate with larger networks in order to achieve system-level benefits. We presented two avenues of this research theme: first, with the objective of improving power quality, and second, with the objective of enhancing reliability and fault tolerance. The key results of this dissertation demonstrate that there is an unrealized opportunity in leveraging the capabilities of distributed, interconnected switching power converters, from both a power processing and also a computational perspective. By more fully utilizing the capabilities of power converters, as well as through the careful design and optimization of the power converters themselves, electric networks can become more robust, scalable, and resilient with increasing penetration of power converters. The need for such electric networks cannot be overstated, as indicated by the emerging global demand for more sustainable electric power, transportation, and information systems. As such technologies evolve, the integration of power electronics and the systems or networks they comprise will become increasingly intertwined. By addressing these problems simultaneously from a 'bottom-up' circuits approach and a 'top-down' systems approach, we can better optimize performance, efficiency, and functionality than by designing from either approach exclusively.

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Appendix A

Uncovering the dependence of $\mathcal{D}$ on $\boldsymbol{\theta}$

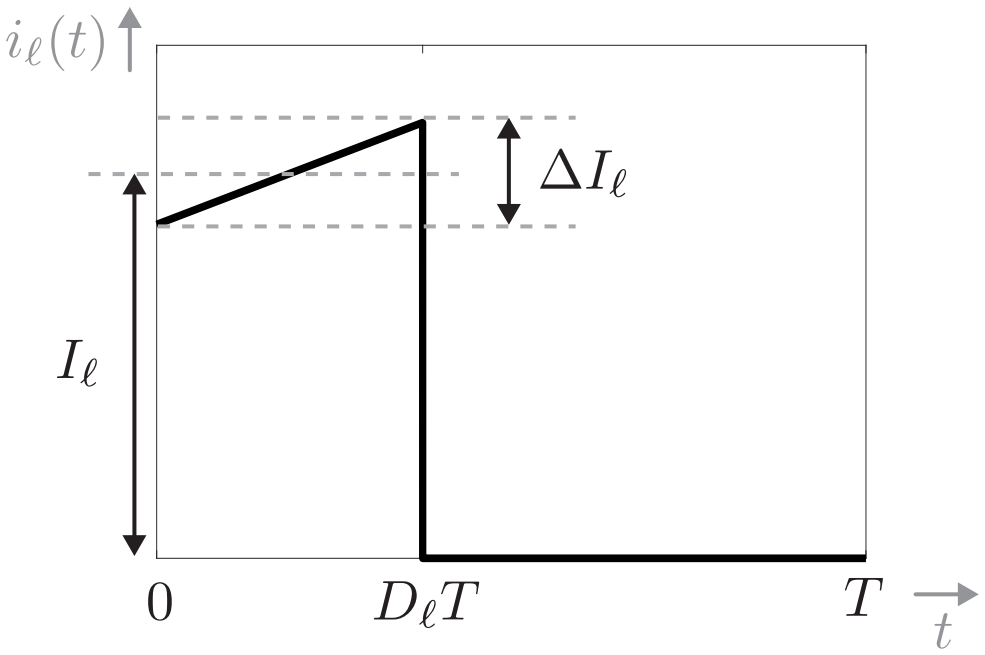

Figure A.1: Time domain sketch of one period of $i_\ell(t)$.

Consider the topology in Fig. 3.1. Let $\tilde{v}_{\text{bus}}$ be the ripple (ac) voltage across C_{bus}. We assume that I_{dc} contributes the dc component of i_{bus}, while C_{bus} contributes the ac component of i_{bus}. In this way, $\tilde{v}_{\text{bus}}$ is a function of the ac component of i_{bus}. The input current to each converter i_ℓ has a real-form Fourier series:

$$i_\ell(t) = \frac{a_\ell^0}{2} + \sum_{k=1}^{\infty} a_\ell^k \cos(2\pi k t) + b_\ell^k \sin(2\pi k t). \tag{A.1}$$

The Fourier coefficients a_ℓ^k and b_ℓ^k are given by:

$$a_\ell^k = \frac{2}{D_\ell \xi_k^2}\Delta I_\ell \cos(D_\ell \xi_k) + \frac{1}{\xi_k}(\Delta I_\ell + 2I_\ell)\sin(D_\ell \xi_k), \tag{A.2}$$

$$b_\ell^k = \frac{2}{D_\ell \xi_k^2}\Delta I_\ell \sin(D_\ell \xi_k) + \frac{1}{\xi_k}\left(\Delta I_\ell - 2I_\ell + (\Delta I_\ell + 2I_\ell)\cos(D_\ell \xi_k)\right), \tag{A.3}$$

where $\xi_k = 2\pi k T$ and ΔI_ℓ, I_ℓ, D_ℓ, and T are pictorially defined in Fig. A.1. We can express equation (A.1) in complex-exponential form as:

$$i_\ell(t) = \sum_{k=-\infty}^{\infty} \alpha_\ell^k \mathrm{e}^{\mathrm{j}2\pi k t}, \tag{A.4}$$

where $\alpha_\ell^k := \left|\alpha_\ell^k\right| \mathrm{e}^{\mathrm{j}\psi_\ell^k}$, with

$$\left|\alpha_\ell^k\right| := \frac{1}{2}((a_\ell^k)^2 + (b_\ell^k)^2)^{\frac{1}{2}}, \tag{A.5}$$

$$\psi_\ell^k := -\arctan\left(\frac{b_\ell^k}{a_\ell^k}\right). \tag{A.6}$$

With this in place, let us now derive the Fourier-series coefficients of i_{bus}. We get:

$$i_{\text{bus}}(t) = \sum_{\ell=1}^{N} i_\ell(t) \tag{A.7}$$

$$= \sum_{\ell=1}^{N}\sum_{k=-\infty}^{\infty} (\alpha_\ell^k \mathrm{e}^{\mathrm{j}2\pi k t})\mathrm{e}^{-\mathrm{j}\xi_k \theta_\ell}, \tag{A.8}$$

where θ_ℓ is the phase shift of i_ℓ with reference to an arbitrary reference angle. Note that equation (A.7) follows from KCL, while in equation (A.8), we have substituted for each i_ℓ from equation (A.4), and the factor $\mathrm{e}^{-\mathrm{j}\xi_k\theta_\ell}$ accounts for the phase shift θ_ℓ [170]. Since i_{bus} and $\tilde{v}_{\text{bus}}$ are linearly related by the capacitive impedance, we can obtain the Fourier series of $\tilde{v}_{\text{bus}}$ as follows:

$$\tilde{v}_{\text{bus}}(t) = \sum_{\ell=1}^{N}\sum_{k=-\infty}^{\infty} \frac{1}{\mathrm{j}2\pi k C_{\text{bus}}}\alpha_\ell^k \mathrm{e}^{\mathrm{j}2\pi k t}\mathrm{e}^{-\mathrm{j}\xi_k\theta_\ell}.$$

$$=: \sum_{\ell=1}^{N}\sum_{k=-\infty}^{\infty} \beta_\ell^k \mathrm{e}^{\mathrm{j}2\pi k t}\mathrm{e}^{-\mathrm{j}\xi_k\theta_\ell}. \tag{A.9}$$

Applying Parseval's theorem [170] and terminating the pertinent summation to some finite $K \in \mathbb{Z}^+$, we get the expression for $\mathcal{D}$ in equation (3.2).

Appendix B

Monte Carlo simulation setup

Consider the topology in Fig. 3.1. The ℓ^{th} converter has an input current waveform that is pictorially represented in Fig. A.1. We assume operation in periodic steady state and that the bus voltage v_{bus} and the output voltage of each converter v_ℓ are constant. Parameters are normalized for convenience (i.e. $T = 1$ and $I_\ell = 1$ nominally). For each scenario of the Monte Carlo simulation, the follow inputs are generated:

1. The duty cycle D_ℓ is a uniformly distributed random number in the interval $(0.2, 0.8)$. Given the assumptions made, the selection of D_ℓ will define the output voltage v_ℓ.

2. The ripple magnitude ΔI_ℓ is a uniformly distributed random number in the interval $(0.5, 1.5)$. The selection of ΔI_ℓ can be interpreted as the relative size of the inductance L_ℓ; that is, a larger ΔI_ℓ corresponds to a smaller L_ℓ, and vice versa.

3. The dc output current I_ℓ is a uniformly distributed random number in the interval $(0.5, 1.5)$. The selection of I_ℓ is interpreted as the average load on the output of the ℓ^{th} converter.

Appendix C

Equivalence of (4.6)–(4.7) to (4.9)–(4.10)

Figure C.1 illustrates the closed-loop system as described by the system of equations (4.6)–(4.7): we refer to this as "system (a)" subsequently. The capacitor voltages of the oscillators, collected in the vector y, are used to generate signals in w, which dictate the switching in the buck converters. This is done using the linear time invariant filter $s + \gamma$. (See (4.7) in Section 4.2.3.) Furthermore, $\Delta = G_{\mathrm{L}}(s) I_N$ captures the linear component of the nonlinear-oscillator dynamics, with $G_{\mathrm{L}}(s)$ given by:

$$G_{\mathrm{L}}(s) := \frac{\varepsilon s}{s^2 - \varepsilon\sigma s + \omega_{\mathrm{sw}}^2}. \tag{C.1}$$

The oscillator dynamics are obtained by placing this in feedback with the cubic nonlinearity αy_j^3 (4.1). The approach to decompose the dynamics of Liénard-type oscillators into linear and nonlinear subsystems is commonly used for analysis since it permits the application of describing-functions approaches that extend frequency-domain methods to nonlinear systems [169]. In this particular case, the describing function for the feedback static nonlinearity, αy_j^3, is denoted by $G_{\mathrm{NL}}(y_j)$. All of these are collected in $G_{\mathrm{NL}}(y) = \mathrm{diag}\{G_{\mathrm{NL}}(y_1), \ldots, G_{\mathrm{NL}}(y_N)\}$. Finally, w feeds into a signum function with windowed integrators, a droop controller that generates the requisite duty command for power sharing, and a comparator with a carrier wave that generates the switching signals $q(t)$, which when multiplied by the dc-input voltage V_{dc} gives the switched voltages, $v_{\mathrm{sw}} = \mathrm{diag}\{V_{\mathrm{dc}} q_1, \ldots, V_{\mathrm{dc}} q_N\}$. These dynamics described above are captured in the frequency domain via the scalar transfer function block $s + \gamma$ and the describing function $G_{\mathrm{PWM}}(w)$. Notice that $G_{\mathrm{PWM}}(w)$ has

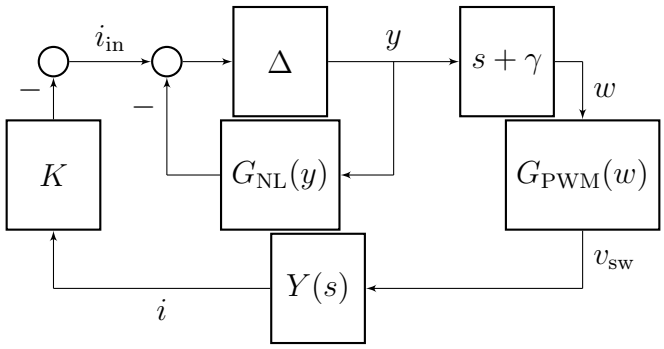

Figure C.1: Block-diagram representation of interconnected system with the equivalent coupled oscillator model dynamics (4.13) used in hardware implementation.

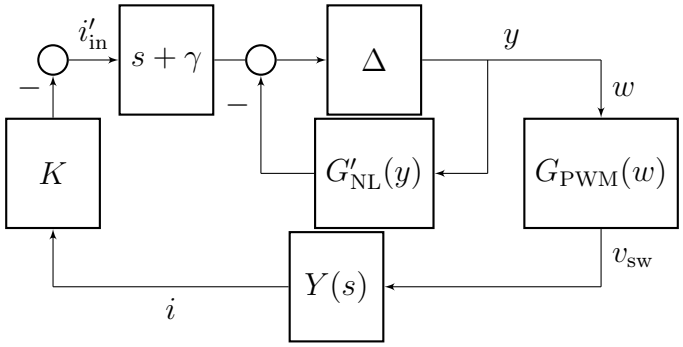

Figure C.2: Block-diagram representation of interconnected system with the equivalent coupled oscillator model dynamics (4.13) used in analysis.

a similar decoupled structure like $G_{\text{NL}}(y)$, and it collects the individual describing functions on the diagonal, i.e., $G_{\text{PWM}}(w) = \text{diag}\{G_{\text{PWM}}(w_1), \ldots, G_{\text{PWM}}(w_N)\}$. To close the loop, the feedback (function of the inductor currents, i, in the buck converters) is described by Kirchhoff's current laws, captured by the admittance of the electrical network, denoted by $Y(s)$, and matrix $K = \kappa I_N$, which is a diagonal static transfer function that incorporates the current gains (see (4.6)).

Fig. C.2 shows the block diagram of the equivalent system (from an input-output standpoint), described by the system of equations (4.9)–(4.10): we refer to this as "system (b)" subsequently. Notice that it differs from the original system Fig. C.1 in two aspects: i) the placement of the filter block $s + \gamma$, which now filters the feedback currents instead of the output voltages, and ii) the describing function for the nonlinearity, denoted by $G'_{\text{NL}}(y)$. This is due to the fact that the systems have different coefficients α and α' for their nonlinearities. Next, we will derive the relationship between α and α' to ensure the input-output behavior of the systems are the same.

Observe that the i_j to w_j relation in system (a) is given by

$$\frac{\kappa G_{\mathrm{L}}(s) i_j(s)}{(s+\gamma)} = \left(1 + G_{\mathrm{L}}(s)\,(s+\gamma)\,G_{\mathrm{NL}}\left(\frac{w_j(s)}{(s+\gamma)}\right)\right) w_j(s), \tag{C.2}$$

and, similarly, the i_j to w_j relation in the equivalent system (b) is described by:

$$\kappa G_{\mathrm{L}}(s)(s+\gamma) i_j(s) = \left(1 + G_{\mathrm{L}}(s) G'_{\mathrm{NL}}\left(w_j\right)\right) w_j(s)\,. \tag{C.3}$$

Since $G_{\mathrm{L}}(s)$ is a linear block, it commutes with the scalar block $s+\gamma$. Thus, for the systems in (C.2) and (C.3) to be equivalent,

$$(s+\gamma) G_{\mathrm{NL}}\left(\frac{w_j(s)}{(s+\gamma)}\right) = G'_{\mathrm{NL}}(w_j(s)). \tag{C.4}$$

Since $\varepsilon \ll 1$ by design, $G_{\mathrm{L}}(s)$ has bandpass characteristics with resonant frequency ω_{sw}. Therefore, we can assume $w_j = A\cos\omega_{\mathrm{sw}} t$. Using the sinusoidal input describing function approach as outlined in [171, 172], we have

$$G_{\mathrm{NL}}(y_j) = \frac{3\alpha A^2}{4}\,, G'_{\mathrm{NL}}(y_j) = \frac{3\alpha' A^2}{4}\,. \tag{C.5}$$

At $s = \jmath\omega_{\mathrm{sw}}$,

$$\begin{aligned}(s+\gamma) G_{\mathrm{NL}}\left(\frac{w_j(s)}{(s+\gamma)}\right) &= \frac{3\alpha A^2(\jmath\omega_{\mathrm{sw}}+\gamma)}{4(\omega_{\mathrm{sw}}^2+\gamma^2)} \mathrm{e}^{\tan^{-1}(-\gamma/\omega_{\mathrm{sw}})} \\ &= \frac{3\alpha A^2}{4\sqrt{\omega_{\mathrm{sw}}^2+\gamma^2}}\,.\end{aligned} \tag{C.6}$$

Thus, for

$$\alpha' = \frac{\alpha}{\sqrt{\omega_{\mathrm{sw}}^2+\gamma^2}}\,, \tag{C.7}$$

both the systems (a) and (b) have equivalent input-output behavior.

Appendix D

Derivation of (4.13)

Denote the switching signal of the j-th buck converter as $q_j(t) \in \{0, 1\}$. Kirchhoff's voltage law indicates that:

$$V_{\mathrm{dc}} q_j(t) - R_{\mathrm{f}} i_j(t) - L_{\mathrm{f}} \frac{di_j}{dt} - R_{\mathrm{Th}} i_{\mathrm{load}} = v_{\mathrm{load}}, \tag{D.1}$$

where $i_{\mathrm{load}} := \sum_{j=1}^{N} i_j$. Recognizing (4.9), we can write:

$$i_{\mathrm{in}j} = \kappa \left(\frac{R_{\mathrm{f}}}{L_{\mathrm{f}}} i_j + \frac{di_j}{dt} \right) = \kappa \left(V_{\mathrm{dc}} q_j(t) - R_{\mathrm{Th}} i_{\mathrm{load}} - v_{\mathrm{load}} \right). \tag{D.2}$$

Substituting for $i_{\mathrm{in}j}$ from (D.2) in (4.5) yields:

$$\begin{aligned}
\dot{\overline{r}}_j = \frac{\varepsilon\omega_{\mathrm{sw}}}{2} &- \int_0^{T_{\mathrm{sw}}} \frac{\varepsilon\omega_{\mathrm{sw}}^2\kappa v_{\mathrm{load}}}{2\pi L_{\mathrm{f}}} \cos(\omega_{\mathrm{sw}}t + \overline{\theta}_j)dt \\
&+ \frac{\varepsilon\omega_{\mathrm{sw}}^2\kappa}{2\pi L_{\mathrm{f}}} \int_0^{T_{\mathrm{sw}}} V_{\mathrm{dc}} q_j(t) \cos(\omega_{\mathrm{sw}}t + \overline{\theta}_j)dt \\
&- \frac{\varepsilon\omega_{\mathrm{sw}}^2 R_{\mathrm{Th}}\kappa}{2\pi L_{\mathrm{f}}} \int_0^{T_{\mathrm{sw}}} i_{\mathrm{load}} \cos(\omega_{\mathrm{sw}}t + \overline{\theta}_j)dt, \qquad \text{(D.3)} \\
\dot{\overline{\theta}}_j = -\frac{\varepsilon\omega_{\mathrm{sw}}^2\kappa}{2\pi\overline{r}_j L_{\mathrm{f}}} &\int_0^{T_{\mathrm{sw}}} V_{\mathrm{dc}} q_j(t) \sin(\omega_{\mathrm{sw}}t + \overline{\theta}_j)dt \\
&+ \frac{\varepsilon\omega_{\mathrm{sw}}^2 R_{\mathrm{Th}}\kappa}{2\pi\overline{r}_j L_{\mathrm{f}}} \int_0^{T_{\mathrm{sw}}} i_{\mathrm{load}} \sin(\omega_{\mathrm{sw}}t + \overline{\theta}_j)dt \\
&- \frac{\varepsilon\omega_{\mathrm{sw}}^2\kappa}{2\pi L_{\mathrm{f}}} \int_0^{T_{\mathrm{sw}}} v_{\mathrm{load}} \sin(\omega_{\mathrm{sw}}t + \overline{\theta}_j)dt. \qquad \text{(D.4)}
\end{aligned}$$

The PWM switching signal, $q_j(t)$, can be written as the following series for a particular duty ratio, D_j [173]

$$q_j(t) = D_j + \sum_{m=1}^{\infty} \frac{2}{m\pi} \sin(D_j m\pi) \cos(m(\omega_{\mathrm{sw}}t + \theta_j)). \qquad \text{(D.5)}$$

Substituting for $q_j(t)$ from (D.5) in (D.3) yields

$$\begin{aligned}\dot{\overline{r}}_j &= \frac{\varepsilon\omega_{\rm sw}}{2}\left(\sigma\overline{r}_j - 3\alpha\overline{r}_j^3\right) - \frac{\varepsilon\omega_{\rm sw}^2\kappa}{2\pi L_{\rm f}}\int_0^{T_{\rm sw}} v_{\rm load}\sin(\omega_{\rm sw}t+\overline{\theta}_j)dt \\ &+ \frac{\varepsilon\omega_{\rm sw}^2 R_{\rm Th}\kappa}{2\pi\overline{r}_j L_{\rm f}}\int_0^{T_{\rm sw}} i_{\rm load}\sin(\omega_{\rm sw}t+\overline{\theta}_j)dt + \frac{\varepsilon\omega_{\rm sw}^2\kappa V_{\rm dc}}{2\pi L_{\rm f}}\times \\ &\sum_{m=1}^{\infty}\int_0^{T_{\rm sw}} \frac{2\sin D_j m\pi}{m\pi}\cos(m(\omega_{\rm sw}t+\theta_j))\cos(\omega_{\rm sw}t+\overline{\theta}_j)dt \qquad \text{(D.6)} \\ &= \frac{\varepsilon\omega_{\rm sw}}{2}\left(\sigma\overline{r}_j - 3\alpha\overline{r}_j^3\right) + \frac{\varepsilon\omega_{\rm sw}^2\kappa V_{\rm dc}\sin(D_j\pi)}{\pi L_{\rm f}} \\ &+ \frac{\varepsilon\omega_{\rm sw}^2 R_{\rm Th}\kappa}{2\pi\overline{r}_j L_{\rm f}}\int_0^{T_{\rm sw}} i_{\rm load}\sin(\omega_{\rm sw}t+\overline{\theta}_j)dt \\ &- \frac{\varepsilon\omega_{\rm sw}^2\kappa}{2\pi L_{\rm f}}\int_0^{T_{\rm sw}} v_{\rm load}\sin(\omega_{\rm sw}t+\overline{\theta}_j)dt. \qquad \text{(D.7)}\end{aligned}$$

In simplifying the second integral on the first line of (D.7), we have leveraged the following: i) $\overline{\theta}_j(t)$ is $\mathcal{O}(\varepsilon)$ close to $\theta_j(t)$, ii) since integrals of sines and cosines evaluate to zero over their period, only the fundamental harmonic remains in the $q_j(t)$ expansion and the average of $\cos^2(\omega_{\rm sw}t+\overline{\theta}_j)$ over its time period is $1/2$. Similarly, we get the following for the phase dynamics:

$$\begin{aligned}\dot{\overline{\theta}}_j &= \frac{\varepsilon\omega_{\rm sw}^2 R_{\rm Th}\kappa}{2\pi\overline{r}_j L_{\rm f}}\int_0^{T_{\rm sw}} i_{\rm load}\sin(\omega_{\rm sw}t+\overline{\theta}_j)dt \\ &- \frac{\varepsilon\omega_{\rm sw}^2\kappa}{2\pi L_{\rm f}}\int_0^{T_{\rm sw}} v_{\rm load}\sin(\omega_{\rm sw}t+\overline{\theta}_j)dt. \qquad \text{(D.8)}\end{aligned}$$

Finally, note that the load current and voltage, $i_{\rm load}$ and $v_{\rm load}$, are governed by the following dynamics:

$$L_{\rm f}\frac{di_{\rm load}}{dt} + (R_{\rm f}+NR_{\rm Th})\,i_{\rm load} = \sum_{j=1}^{N} V_{\rm dc}q_j(t) - Nv_{\rm load}. \qquad \text{(D.9)}$$

$$C_{\rm load}\frac{dv_{\rm load}}{dt} + \frac{v_{\rm load}}{R_{\rm load}} = i_{\rm load}. \qquad \text{(D.10)}$$

While (D.10) follows straightforwardly from the circuit laws for an RC tank, (D.9) is derived by summing up all N instances of (D.1). Going back to (D.7) and (D.8), we use integration by parts for integrals involving i_{load} and v_{load} where we substitute appropriately from (D.9)-(D.10) to compute the requisite derivatives. Algebraic simplifications then yield (4.13).