Evaluation of Scaled Segmented Channel MOSFETs for Analog/RF Applications

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Evaluation of Scaled Segmented Channel MOSFETs
for Analog/RF Applications

by Lars Prospero Tatum

Research Project

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May 28, 2020

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Abstract

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by

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While advanced transistor structures have enabled gate length scaling below 20 nanometers and consequently enabled digital integrated circuits to increase in complexity with advancements in semiconductor manufacturing, they have not enabled similar improvement in analog IC performance due to degraded transconductance and increased gate leakage. Because of this, most analog ICs are manufactured using older-generation technology with long-channel transistors. The long channel length limits the transistor maximum oscillation frequency, however. In this study, technology computer-aided design simulations are used to assess the potential benefits of a quasi-planar segmented-channel transistor (SegFET) design for enhanced analog/RF performance, based on a mature 65 nm generation CMOS transistor technology.

To all those who have believed in me and made this wild ride possible.

This one's for you

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Chapter 1 - Introduction

1.1) MOSFET Scaling

For over 50 years, the semiconductor industry has followed Moore's law (visualized in figure 1-1), a guiding outlook which states that the number of transistors in the leading-edge microprocessor "chip" should double every two years [1]. This transistor density scaling has been primarily achieved by scaling down the size of the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) that comprise digital integrated circuits (ICs), allowing for improved computational performance at relatively low incremental cost.

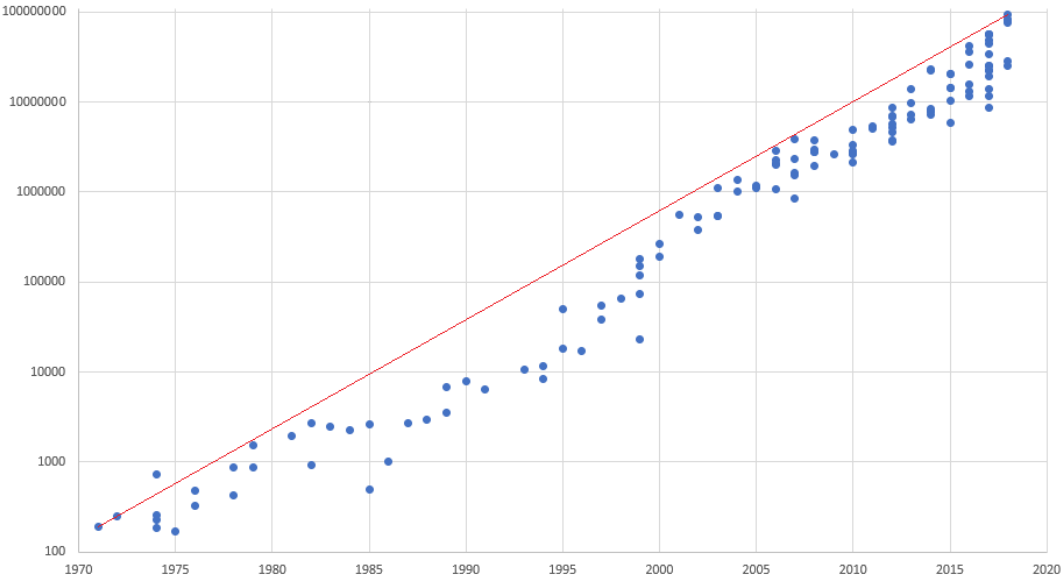

Figure 1-1: Transistors per square millimeter in various ICs, 1970-2020 [2].

Multiple innovations allowed the minimum lateral dimension (the gate length, Lg) of a planar bulk-silicon (bulk-Si) MOSFET structure to be scaled down from ~50 microns in 1965 to 30 nanometers (nm) in 2009; these include channel strain engineering to boost electron mobility and the use of high-permittivity (high-k) dielectric and metallic gate stack materials for improved gate voltage (V_g) control and hence transistor performance (on/off current ratio) and scalability, respectively. For even shorter

gate lengths, gate control of the channel potential relative to drain voltage (V_d) control is insufficient to provide for high on/off current ratio, *i.e*., electrostatic integrity is degraded [3]. Therefore, alternative MOSFET structures with superior electrostatic integrity are necessary for gate lengths less than 25 nm. These include the planar fully depleted silicon-on-insulator (FD-SOI) MOSFET [4] and the three-dimensional (3D) "FinFET" [5] which each rely on an ultra-thin body region to reduce drain voltage control and to enhance gate voltage control to achieve superior electrostatic integrity.

Short-channel effects (symptoms of poor electrostatic integrity) include increased drain-induced barrier lowering (DIBL) – that is, a decrease in threshold voltage (V_t) with increasing drain-to-source voltage (V_{ds}) – and degraded subthreshold swing (SS) [3]. SS is defined as the steepest inverse slope of the transistor current (I_d) *vs*. gate voltage on a semi-log plot; it indicates how strongly a change in gate voltage modulates the transistor current in the subthreshold region of operation, *i.e.* in the off state, where V_{ds} is typically non-zero; smaller SS is desirable for achieving high on/off current ratio. At room temperature, the fundamental lower limit of SS is approximately 60 mV/decade[6].

While the aforementioned advanced transistor structures have enabled L_g scaling below 20 nm to enable digital ICs to continue to increase in complexity and functionality with advancements in semiconductor manufacturing, they have not provided for continued improvement in analog IC performance due to degraded transconductance, as well as increased gate leakage [7]. Also, FD-SOI technology requires the use of more expensive SOI wafers. The high-frequency performance of FinFETs is limited by lower electron mobility along the fin sidewalls, larger parasitic source/drain resistance, and larger parasitic gate-fringing capacitance due to the 3D structure [8]. Because of this, most analog ICs are manufactured using older-generation technology with long-channel transistors. The long channel length limits the transistor maximum oscillation frequency, however.

1.2) The Segmented-Channel MOSFET

The Segmented-Channel MOSFET (SegFET), which was inspired by the Vertex Channel Array Transistor [9], was first proposed in 2008 [10] as an alternative to the FinFET for improved scalability and performance in both digital and analog/radio-frequency (RF) IC applications [11]. In contrast to the FinFET, the SegFET comprises low-aspect-ratio silicon channel stripes as shown in figure 1-2, *i.e.*, it is a quasi-planar structure.

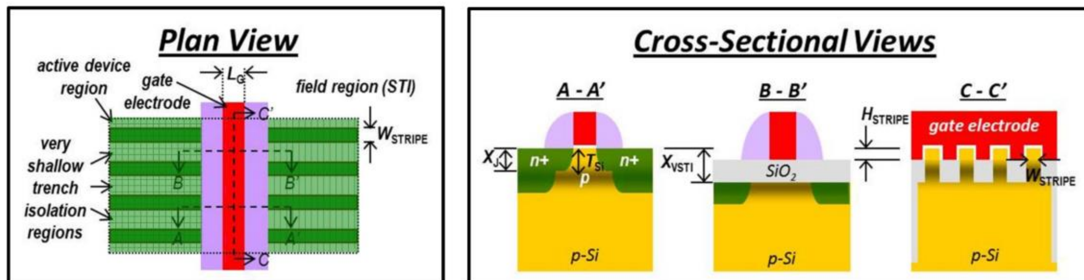

Figure 1-2: SegFET Device Structure [12]

The channel region of a SegFET comprises one or more parallel semiconductor stripes of equal width, typically greater than or equal to the gate length for relative ease of fabrication. Within each stripe, the doping profiles are similar to those for a planar bulk-Si MOSFET. The stripes within a single multi-stripe transistor are isolated by Very Shallow Trench Isolation (VSTI) dielectric material, which extends to a depth below the source/drain extension regions [13], [14] but which is shallower than the source/drain contact regions, *i.e*., the source/drain regions are not segmented.

Unlike the FinFET, the SegFET can be fabricated using a conventional planar bulk-Si MOSFET process flow, starting with a corrugated semiconductor substrate (figure 1-3). The VSTI/STI dielectric material surrounding the active-area stripe(s) is recessed by a small amount H_{Stripe} (the resultant height

of the gated portion of each stripe) just prior to gate stack formation so that the gate electrode wraps around the top portion of each stripe, resulting in a tri-gate structure [12].

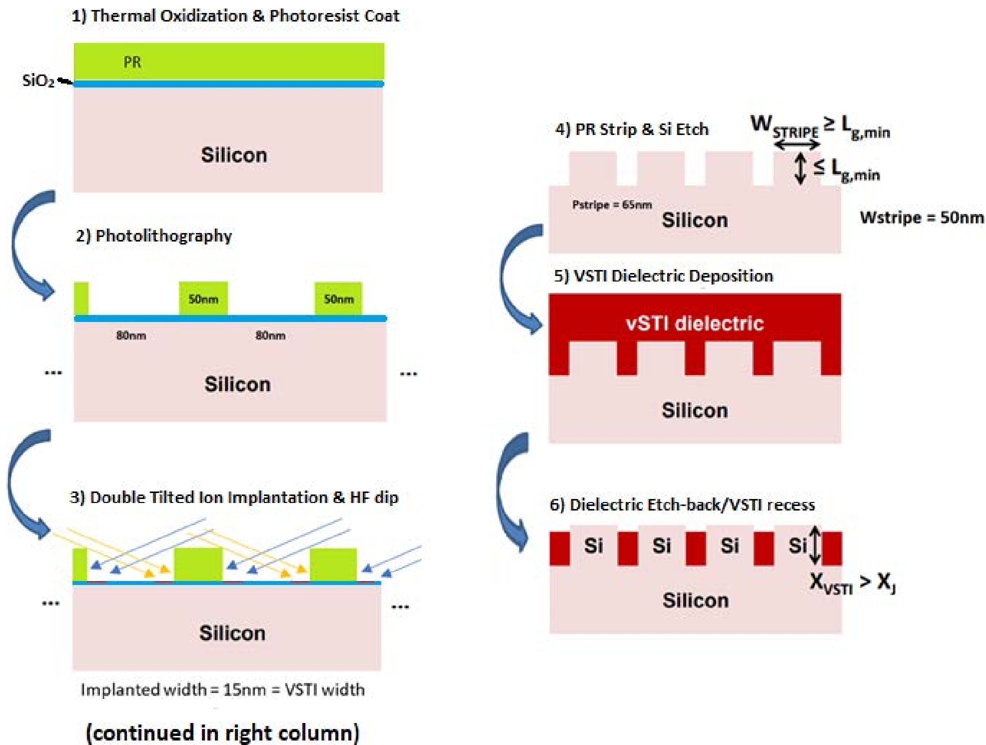

Figure 1-3: Corrugated Substrate Process Flow

Electrostatic integrity is enhanced by the tri-gate structure and fringing electric fields through the VSTI dielectric, providing for reduced DIBL and steeper subthreshold swing, as well as larger transconductance due to lower average transverse electric field in the inversion-layer channel. This allows for further gate-length scaling to achieve improved high-frequency performance.

In this work, technology computer aided design (TCAD) simulations are used to explore the benefit of the SegFET for improving transistor cutoff frequency (f_T). A mature 65 nm-generation (“65 nm node”) bulk-Si complementary MOS (CMOS) technology serves as the baseline for comparison.

Chapter 2 - Experimental Approach

2.1) Baseline Planar Bulk-Si MOSFET Design

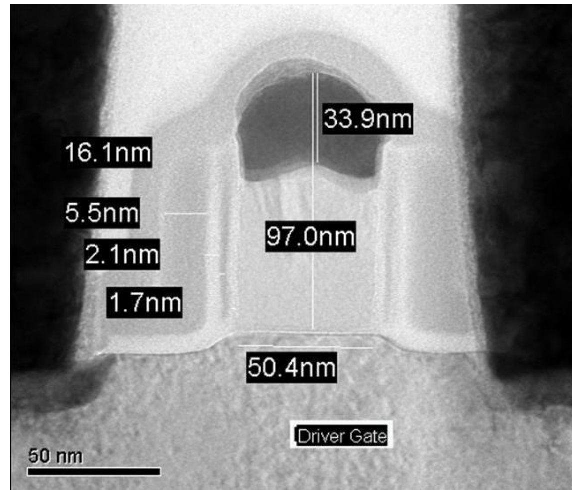

Figure 2-1: XSEM of 65nm node planar transistor structure, provided by Texas Instruments (TI)

Conventional bulk-Si n-channel (NMOS) and p-channel (PMOS) transistors fabricated using the Texas Instruments (TI) 65 nm CMOS process were modeled using Sentaurus Device [15]. For simplicity, uniform body doping was assumed. The physical gate oxide thickness (T_{ox}) was estimated from the given electrical inversion oxide thickness, $T_{ox,\,inv}$. The body dopant concentration (N_{sub}) was adjusted to roughly match specified on- and off-state currents. The values for the gate length (L_g) and gate-sidewall spacer length (L_{sp}) were selected based on the cross-sectional electron micrograph (figure 2-1). The gate material for the NMOS transistor is heavily n-type doped (N++) polysilicon, and the gate material of the PMOS is heavily p-type doped (P++) polysilicon, which determines the gate work function (WF) for both types of transistors. The source/drain (S/D) design parameters were chosen within reasonable constraints for the 65 nm process, to minimize parasitic resistance. The transistor width (W) was chosen to be equal to the minimum half-pitch, 65 nm. Parasitic gate-to-source capacitance (C_{gs}) illustrated in figure 2-2 is included in order to match the f_T specifications provided by TI.

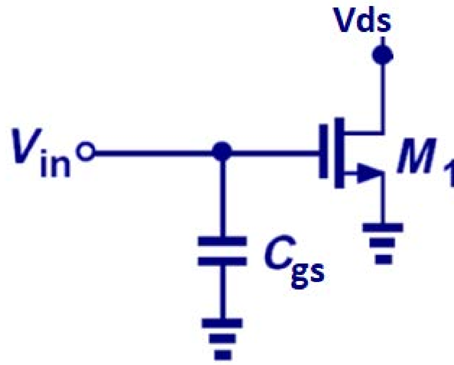

Figure 2-2: Transistor configuration used to characterize high-frequency performance. Note the parasitic C_{gs}.

Baseline Transistor Performance Specifications

The tables below summarize the MOSFET performance specifications provided by TI. Off-state current was specified for the stressed condition V_{ds} = 1.1 x V_{DD}.

NMOS Specifications (V_{DD} = 1.2 V)

On-state Current	$T_{ox, inv}$ (angstroms)	Stressed I_{off} (A/µm)	f_T @ 20µA/µm	f_T @ 200µA/µm
570µA/µm	26.5	3.98e-10	50GHz	150GHz

PMOS Specifications (V_{DD} = 1.2V)

On-state Current	$T_{ox, inv}$ (angstroms)	Stressed I_{off} (A/µm)	f_T @ 20µA/µm	f_T @ 200µA/µm
303µA/µm	27.6	3.98e-10	38GHz	70GHz

Simulated NMOS Baseline Device

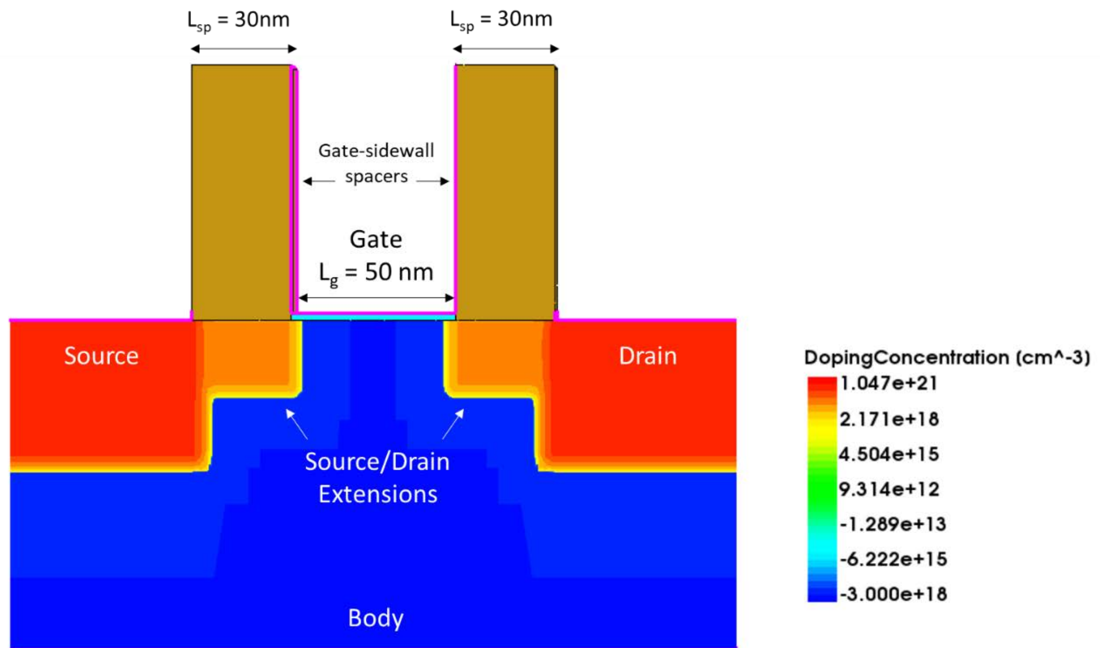

Figure 2-3: Cross-section of simulated baseline n-channel MOSFET

The tables below summarize the transistor design parameters and simulated performance parameter values for the baseline NMOS transistor.

Device Design Parameter Values

L_g	L_{eff}	L_{sp}	T_{ox}	W	S/D height	S/D extension height	Gate WF	Substrate Doping	S/D Doping	S/D extension doping	Parasitic C_{gs}
50	49.56	30	2.35	65	40	20	4.05eV	3e18/cm^3	1e21/cm^3	5e19/cm^3	0.215fF

All lengths/widths/heights are in nm, unless otherwise specified

Simulated Device Performance Parameter Values

Stressed I_{off} (A/µm)	Drive Current (µA/µm)	SS (mV/dec)	$V_{t, saturation}$ (V)	$V_{t, linear}$ (V)	DIBL (mV/V)	Peak f_T (GHz)
1.06E-10	831	85.27	0.382	0.515	113	202.62

Simulated Baseline PMOS Device

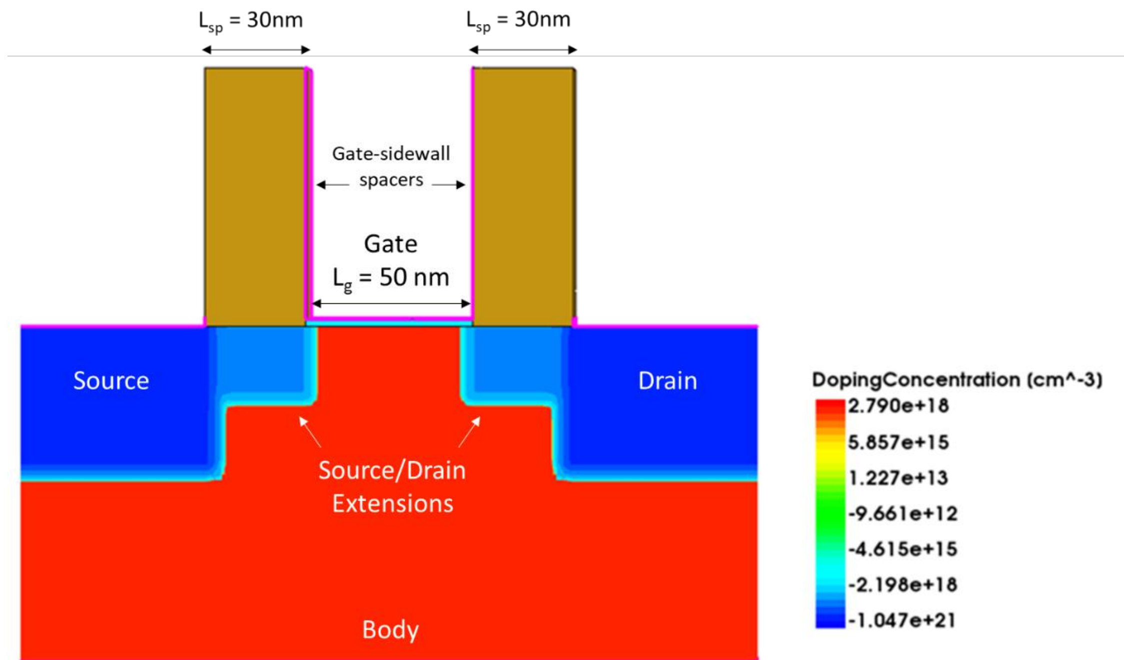

Figure 2-4: Cross-section of simulated baseline p-channel MOSFET

The tables below summarize the transistor design parameters and simulated performance parameter values for the baseline PMOS transistor.

Device Design Parameter Values

L_g	L_{eff}	L_{sp}	T_{ox}	W	S/D height	S/D extension height	Gate WF	Substrate Doping	S/D Doping	S/D extension doping	Parasitic C_{gs}
50	49.56	30	2.35	65	40	20	5.12eV	2.79e18/cm^3	1e21/cm^3	5e19/cm^3	0.184fF

All lengths/widths/heights in nm, unless otherwise specified

Simulated Device Performance Parameter Values

Stressed I_{off} (A/µm)	Drive Current (µA/µm)	SS (mV/dec)	$V_{t,\ saturation}$ (V)	$V_{t,\ linear}$ (V)	DIBL (mV/V)	Peak f_T (GHz)
1.03E-10	4.04E-04	85.501	-0.392	-0.557	139	116.01

2.2) SegFET Design

The SegFETs in this study have the same body and S/D doping profiles as their baseline planar MOSFET counterparts. The stripe pitch was set to be equal to the minimum half-pitch (65 nm) and the stripe width was set to be 50 nm (*i.e.*, no smaller than L_g, in contrast to the 3D FinFET). Various stripe height (H_{Stripe}) values were studied, ranging from 0 nm to 20 nm. To investigate scaling benefits, various L_g values were studied, ranging from 50 nm down to 35 nm. The figures below show the simulated SegFET structure with 50 nm L_g and 20 nm H_{Stripe}. Note that the gate electrode and S/D contact plugs are not pictured for clarity; only their interfaces with the transistor structure are indicated, by pink lines. The parasitic gate-to-source capacitance is assumed to be the same for the SegFETs as for the baseline devices.

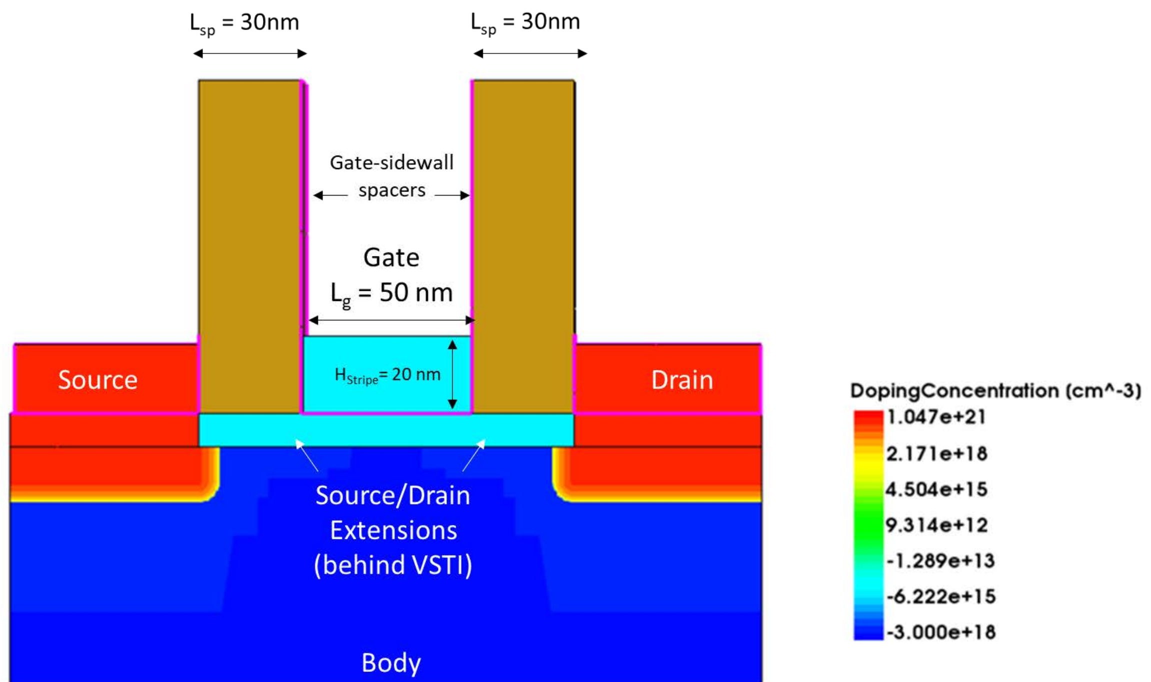

Figure 2-5: Cross-section of simulated SegFET along the channel direction

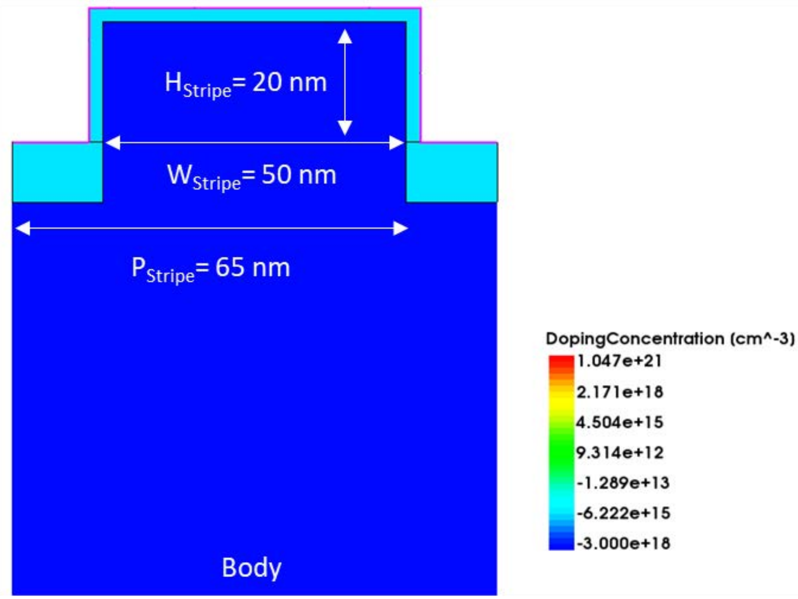

Figure 2-6: Cross-section of simulated SegFET across a gated channel stripe

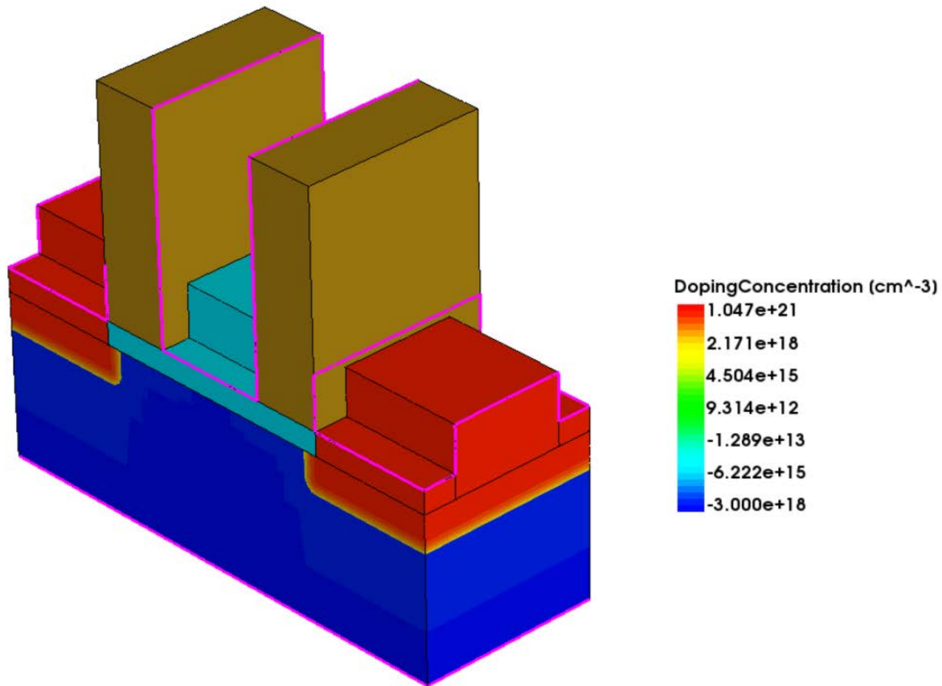

Figure 2-7: Perspective view of the simulated SegFET structure

For identical doping profiles, the threshold voltage (V_t, defined as the gate voltage at which the transistor current reaches 100 nA x W_{layout}/L_g) of a SegFET is smaller than that of its planar counterpart because of improved gate control (smaller subthreshold swing) and also because of smaller depletion charge per unit channel width due to the effect of sidewall gating [12]. Therefore, the SegFET will have higher off-state leakage current (I_{off}) at V_{gs} = 0 V, as shown in figure 2-7. This issue can be remedied by adjusting the gate work function (WF), applying a body bias voltage (to reverse-bias the body-source junction), and/or increasing the dopant concentration in the channel region to increase V_t.

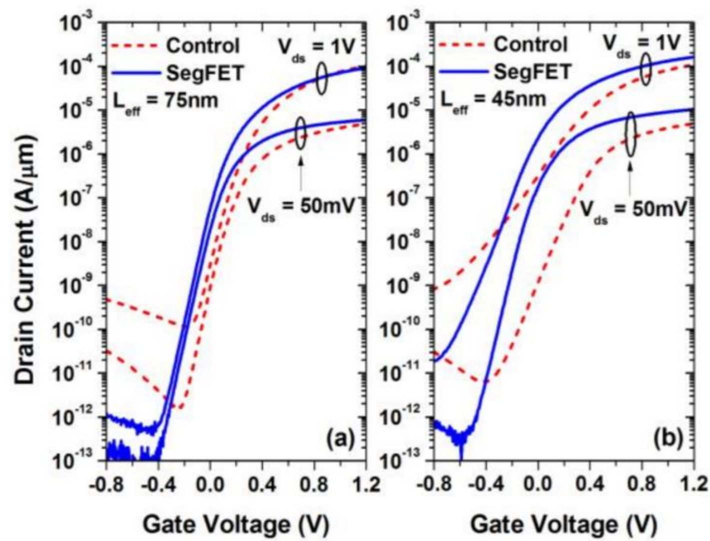

Figure 2-8: Experimental SegFET results show reduced threshold voltage and increased off-state leakage current at V_{gs} = 0 V [12]

2.3) Transistor performance comparison methodology

A change in the gate work function simply shifts the I_d-V_g curve by the amount of the WF change. Therefore, additional simulations are not needed to determine the SegFET performance parameter values for the WF-tuning approach of meeting the off-state current specification. All that is needed is to find the value of V_{gs} that corresponds to the off-state current specification, V_{off}, and then to set the maximum operating value of V_{gs} to be $V_{off} + V_{DD}$ (at which the maximum on-state current is reached).

One of the advantages of the SegFET compared to the FinFET is that its threshold voltage can be adjusted with body biasing. In this work, the value of reverse body bias voltage (V_{sb}) necessary to increase V_t to meet the off-state current specification was determined as an alternative approach.

As yet another approach to match the off-state current specification, the value of (uniform) body dopant concentration necessary to increase V_t to meet the off-state current specification also was determined.

Values of on-state current, threshold voltage, subthreshold swing, DIBL, and cutoff frequency (f_T) were extracted from simulated transistor performance characteristics. To determine f_T, a frequency sweep from 10MHz to 1THz was performed for various values of V_{gs}, and the transistor drain current was monitored to determine the device's current gain |h21| at each frequency. f_T was extrapolated from the -20 dB point assuming a 20dB/decade rolloff (see figure 2-8), as is common experimental practice for radio-frequency (RF) characterization [15], [16]. (If f_T is taken to be the frequency at which unity gain is reached, this would be an overestimate due to the existence of transfer function zeros at high frequency.)

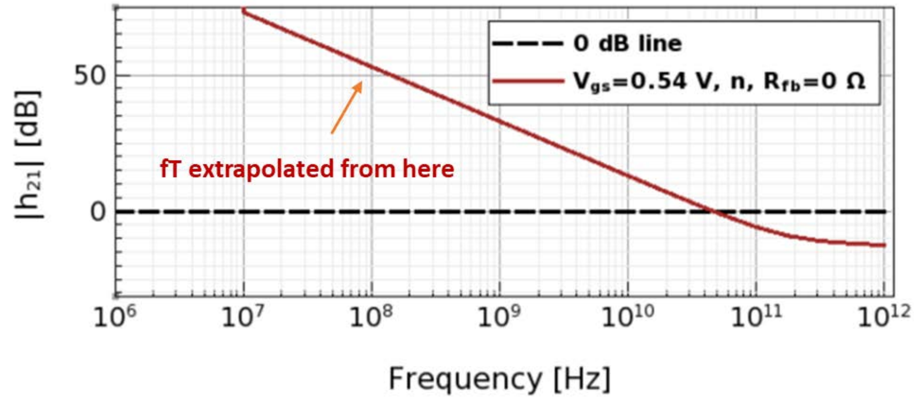

Figure 2-9: Sample h21 plot used to extrapolate f_T

Chapter 3 - Results and Discussion

3.1) SegFET IV Characteristics

Figure 3-1 compares the transfer characteristics for 50 nm L_g MOSFETs, including SegFETs of various H_{Stripe} values.

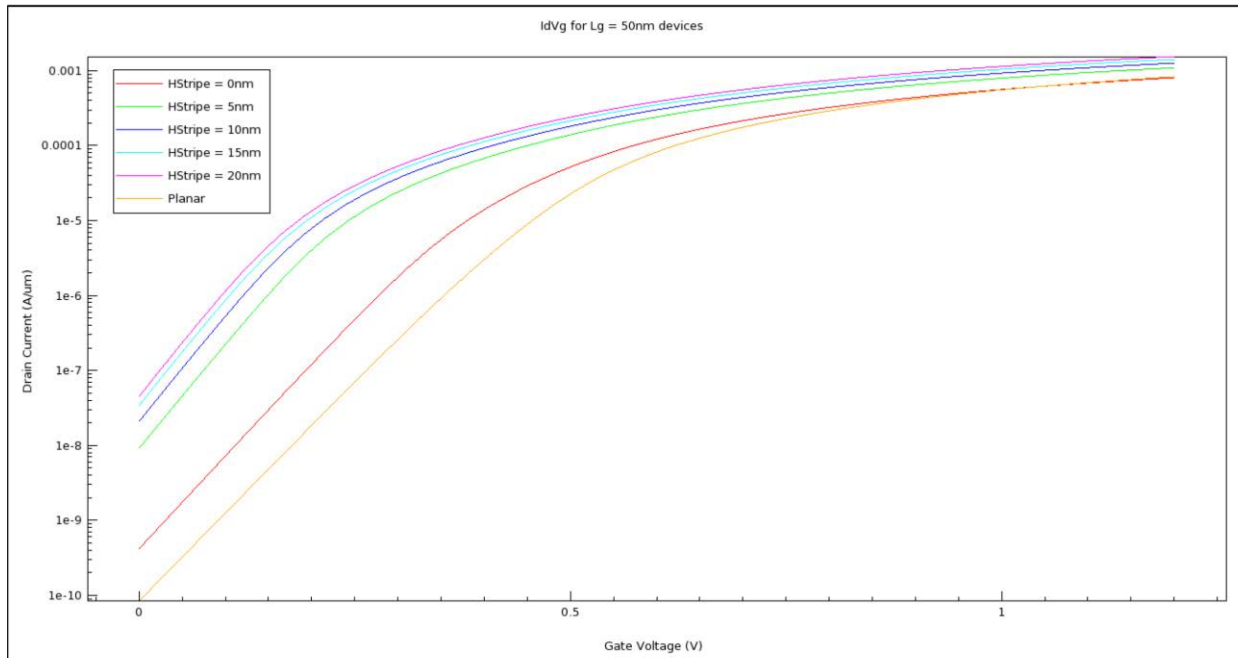

Figure 3-1: Simulated transfer characteristics for n-channel SegFETs and baseline planar MOSFET. (L_g = 50 nm, $V_{ds} = V_{DD}$ = 1.2V.)

Reduction in V_t with improved gate control for the SegFET results in larger off-state leakage current at V_{gs} = 0 V and necessitates one (or more) of the aforementioned measures for increasing V_t. As will be shown below, on-state performance is compromised with reverse body biasing and with increased channel doping, due to degraded charge-carrier effective mobilities, so for those approaches only two values of gate length, 50 nm and 40 nm, were considered. In the tabulated results below, the first row is for the planar baseline MOSFET design, denoted by "PLANAR" in the H_{Stripe} field.

SegFETs with V_t Adjusted Using Gate Work Function Tuning

The most effective method of adjusting V_t is to tune the gate work function. In practice this requires modification of the material composition of the gate electrode and/or its interface with the gate dielectric [17], [18]. Figures 3-2 and 3-3 compare the transfer characteristics for 50 nm L_g MOSFETs that have different gate work functions to achieve the same off-state leakage current at V_{gs} = 0V.

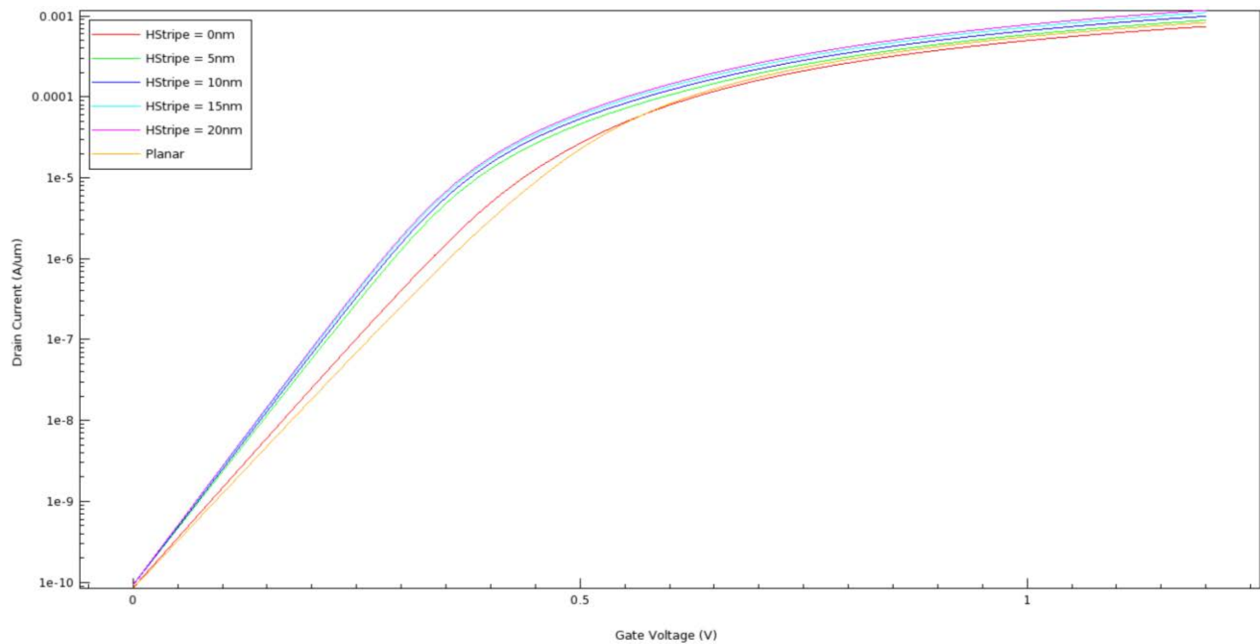

Figure 3-2: Simulated transfer characteristics for n-channel transistors with matched I_{off} achieved via gate work function tuning. (L_g = 50 nm, V_{ds} = V_{DD} = 1.2V.)

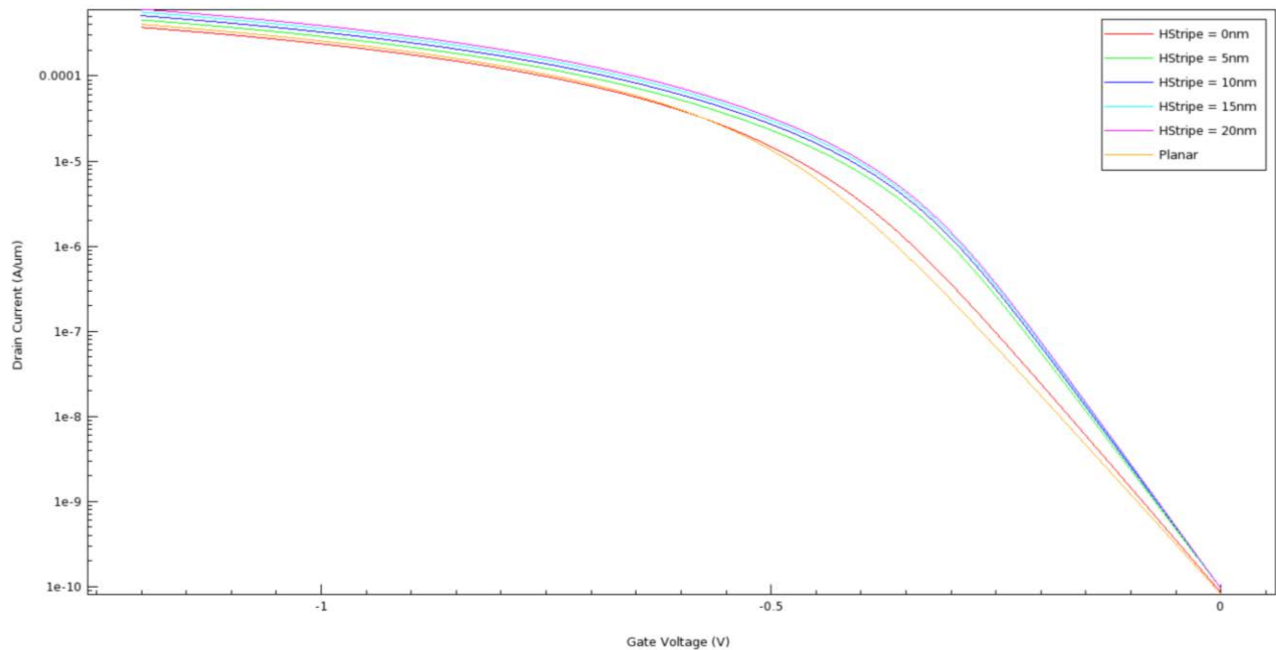

Figure 3-3: Simulated transfer characteristics for p-channel transistors with matched I_{off} achieved via gate work function tuning. (L_g = 50 nm, $V_{ds} = V_{DD}$ = -1.2V.)

It can be seen from these plots that the SegFETs have steeper subthreshold swing, due to enhanced electrostatic integrity (which improves with increasing H_{Stripe}), and hence superior on-state drive current for H_{Stripe} > 0 nm. Superior electrostatic integrity allows for further scaling of L_g to improve digital and analog/RF IC performance. Figures 3-4 and 3-5 show that the on-state current (I_{on}), defined as the transistor current I_d for $V_{gs} = V_{ds} = V_{DD}$, generally increases with H_{Stripe} and gate length scaling. The summary tables below provide quantitative comparisons between the SegFET and baseline planar MOSFET. As a point of reference, an n-channel SegFET with L_g = 40 nm and H_{Stripe} = 20 nm has about the same subthreshold swing and better DIBL than the planar baseline n-channel MOSFET with L_g = 50 nm, with over 56% higher drive current. The improvement in drive current is even greater, over 75%, for a p-channel SegFET. The greater benefit of the SegFET design for p-channel devices is due to higher hole mobility (*vs*. electron mobility) along the <110> oriented stripe sidewalls [19].

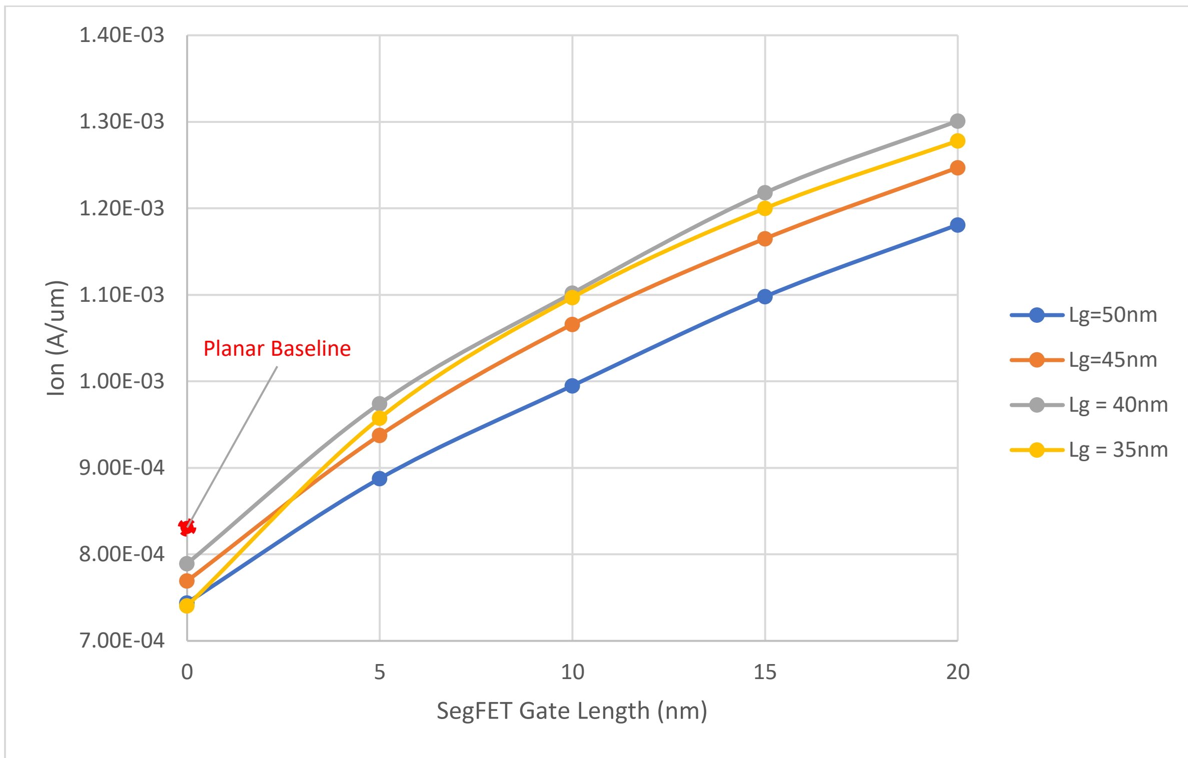

Figure 3-4: I_{on} vs. Stripe Height for n-channel SegFETs with V_t adjusted via gate work function tuning.

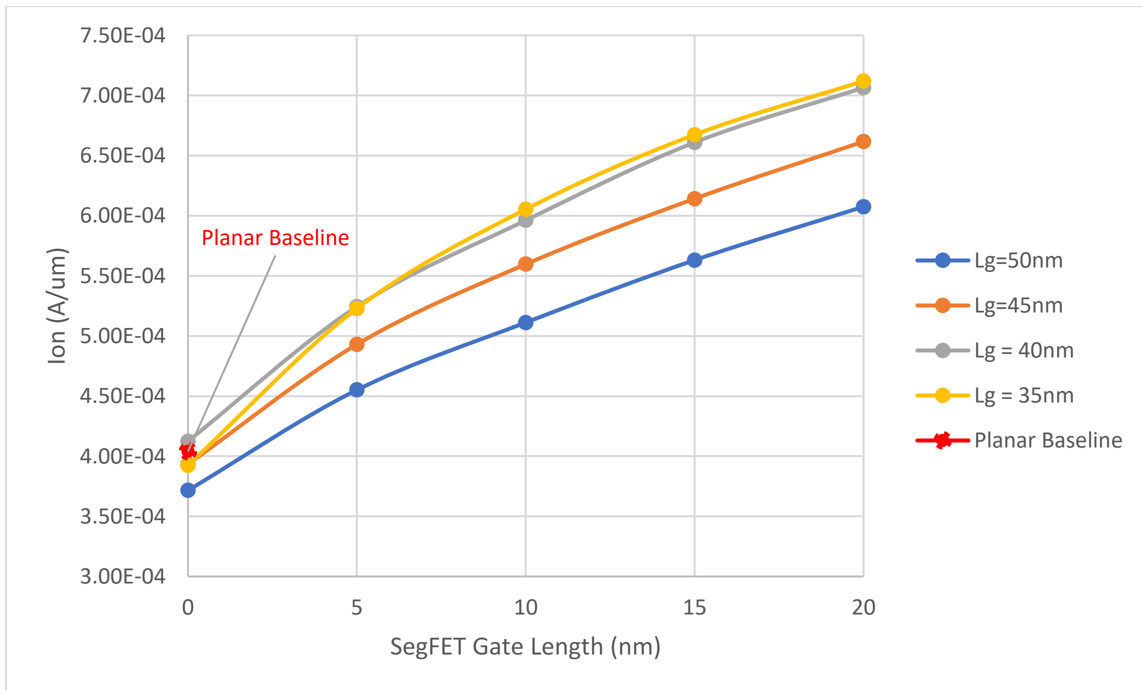

Figure 3-2: I_{on} vs. Stripe Height for p-channel SegFETs with V_t adjusted via gate work function tuning.

Results for n-channel SegFETs with V_t tuned by gate work function engineering

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	WF (eV)	Stressed I_{off} (A/µm)	I_{on} (A/µm)	I_{on} increase	SS (mV/dec)	DIBL (mV/V)
50	49.56	PLANAR	4.05	1.06E-10	8.31E-04	0.00%	85.27	113
50	49.56	0	4.106	1.03E-10	7.44E-04	-10.48%	80.77	94
50	49.56	5	4.193	1.05E-10	8.88E-04	6.80%	71.43	61
50	49.56	10	4.214	1.02E-10	9.95E-04	19.71%	69.67	56
50	49.56	15	4.226	1.03E-10	1.10E-03	32.10%	68.69	54
50	49.56	20	4.234	1.03E-10	1.18E-03	**42.08%**	68.16	53
45	44.56	0	4.172	1.05E-10	7.69E-04	-7.45%	83.56	112
45	44.56	5	4.235	1.03E-10	9.38E-04	12.81%	73.41	72
45	44.56	10	4.250	1.05E-10	1.07E-03	28.25%	71.25	64
45	44.56	15	4.261	1.02E-10	1.17E-03	40.16%	70.30	62
45	44.56	20	4.268	1.02E-10	1.25E-03	**50.02%**	69.84	62
40	39.56	0	4.266	1.03E-10	7.89E-04	-5.03%	88.62	137
40	39.57	5	4.291	1.03E-10	9.74E-04	17.20%	78.21	88
40	39.57	10	4.303	1.02E-10	1.10E-03	32.58%	75.30	78
40	39.57	15	4.310	1.04E-10	1.22E-03	46.54%	73.97	76
40	39.57	20	4.315	1.06E-10	1.30E-03	**56.52%**	73.48	75
35	34.57	0	4.417	1.04E-10	7.41E-04	-10.91%	102.48	174
35	34.57	5	4.405	1.05E-10	9.58E-04	15.19%	92.05	112
35	34.57	10	4.403	1.05E-10	1.10E-03	31.98%	87.65	100
35	34.57	15	4.405	1.03E-10	1.20E-03	44.37%	85.54	96
35	34.57	20	4.409	1.03E-10	1.28E-03	**53.75%**	84.69	96

Results for p-channel SegFETs with V_t tuned by gate work function engineering

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	WF (eV)	Stressed I_{off} (A/µm)	I_{on} (A/µm)	I_{on} increase	SS (mV/dec)	DIBL (mV/V)
50	49.51	PLANAR	5.170	1.03E-10	4.04E-04	0.00%	85.50	139
50	49.51	0	5.121	1.03E-10	3.72E-04	-7.95%	81.26	137
50	49.52	5	5.042	1.05E-10	4.55E-04	12.73%	71.85	114
50	49.52	10	5.021	1.06E-10	5.11E-04	26.63%	70.08	102
50	49.52	15	5.008	1.04E-10	5.63E-04	39.48%	69.11	96
50	49.52	20	5.001	1.04E-10	6.08E-04	**50.48%**	68.57	93
45	44.51	0	5.052	1.03E-10	3.93E-04	-2.58%	84.54	155
45	44.51	5	4.998	1.05E-10	4.93E-04	22.12%	74.25	124
45	44.51	10	4.982	1.02E-10	5.60E-04	38.64%	72.07	110
45	44.51	15	4.972	1.04E-10	6.14E-04	52.14%	71.08	104
45	44.51	20	4.965	1.03E-10	6.62E-04	**63.91%**	70.60	101
40	39.51	0	4.955	1.05E-10	4.13E-04	2.18%	90.45	180
40	39.53	5	4.936	1.05E-10	5.24E-04	29.90%	80.08	140
40	39.53	10	4.925	1.03E-10	5.96E-04	47.68%	76.96	124
40	39.53	15	4.918	1.04E-10	6.61E-04	63.74%	75.54	117
40	39.53	20	4.912	1.03E-10	7.07E-04	**75.01%**	75.02	114
35	34.53	0	4.788	1.04E-10	3.93E-04	-2.77%	110.35	216
35	34.53	5	4.806	1.05E-10	5.23E-04	29.50%	98.91	164
35	34.53	10	4.812	1.06E-10	6.05E-04	49.96%	93.41	145
35	34.53	15	4.811	1.05E-10	6.67E-04	65.32%	90.86	138
35	34.53	20	4.808	1.04E-10	7.12E-04	**76.37%**	89.90	135

SegFETs with V_t Adjusted Using Body Biasing

While body biasing is useful for dynamically adjusting V_t to optimize the tradeoff between high performance and low standby power consumption, the sub-linear dependence of V_t on V_{sb} makes this less effective for large V_t adjustment. Figures 3-6 and 3-7 show this challenge is exacerbated by the enhanced gate control (*i.e.*, reduced body control) of the channel potential in a SegFET. For L_g = 50 nm, body biases larger than 9 V are needed to achieve the specified off-state leakage current. As the stripe height increases and gate length decreases, the body coefficient (defined as the change in V_t for a

change in V_{sb}) degrades. For a SegFET with L_g = 40 nm and H_{Stripe} = 20 nm, a reverse body bias of 20V is needed to increase V_t by 0.258 V to achieve the specified off-state leakage current. For a SegFET with L_g = 35 nm and H_{Stripe} = 20 nm, a reverse body bias >30V is required.

Another issue with the body bias approach is a degradation in on-state drive current and transconductance due to degraded carrier effective mobility. This is because the transverse electric field within the inversion-layer channel in the on-state is greatly enhanced when a large reverse body bias is applied. As a result, the body-biased SegFET can have worse on-state drive current than the planar MOSFET with zero body bias, despite having enhanced electrostatic integrity. Larger body biases are required for SegFETs with shorter gate lengths, resulting in further degraded performance; hence, results for gate length below 40 nm are not included here.

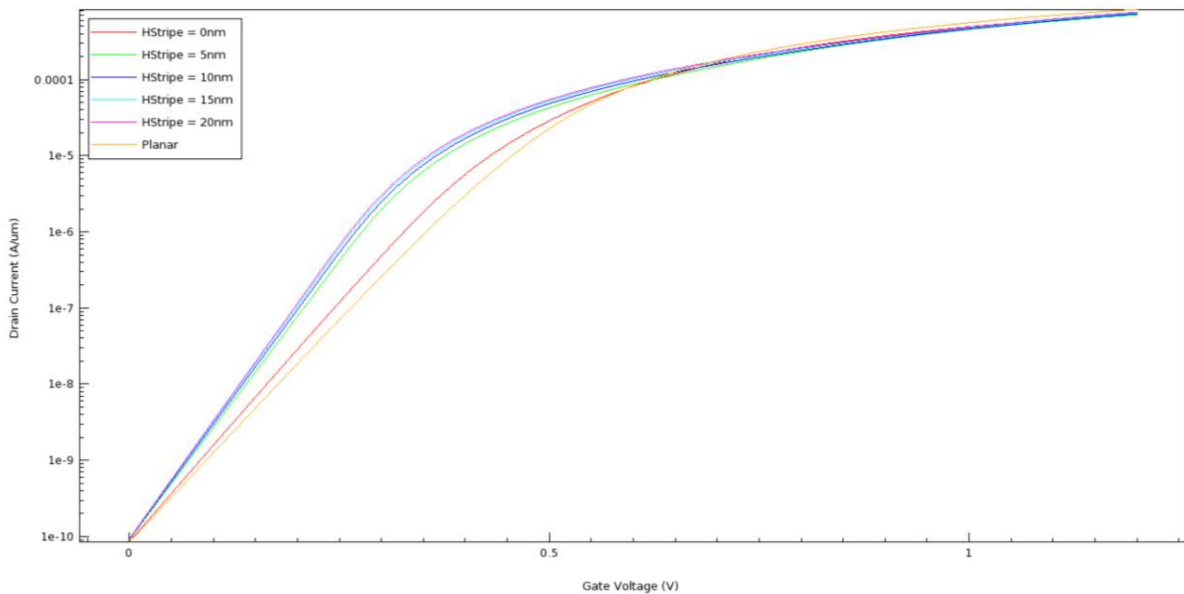

Figure 3-6: Simulated transfer characteristics for n-channel transistors with matched I_{off} achieved via reverse body biasing. (L_g = 50 nm, V_{ds} = V_{DD} = 1.2V.) Note the degraded transconductance for the body-biased SegFETs

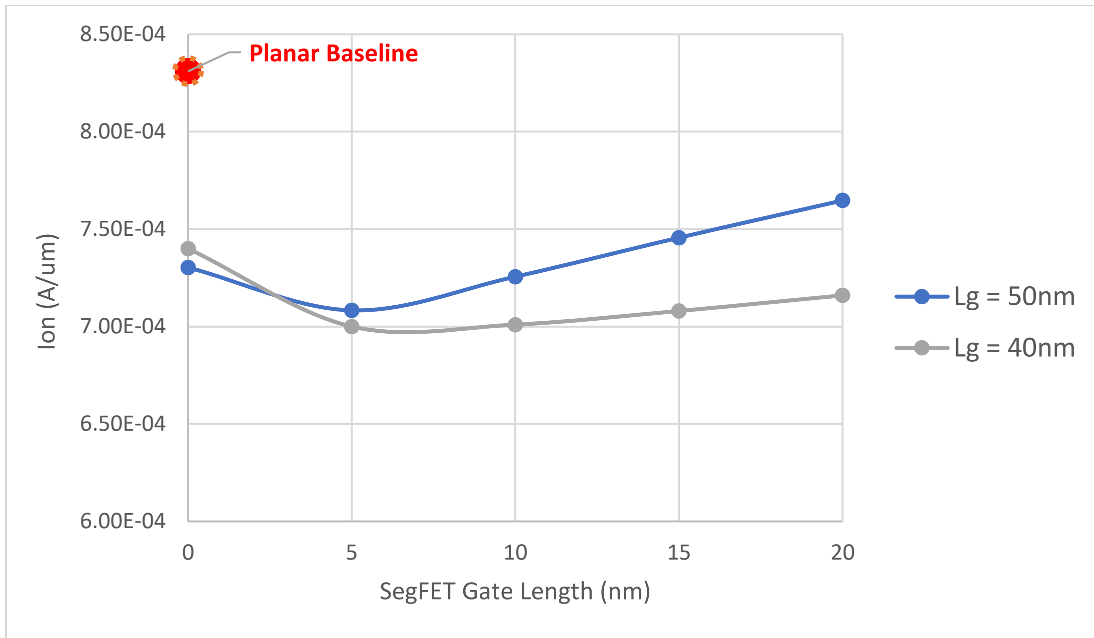

Figure 3-7: I_{on} vs. Stripe Height for n-channel SegFETs with V_t adjusted via body biasing.

Results for n-channel SegFETs with V_t tuned by reverse body biasing

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	V_{sb} (V)	Stressed I_{off} (A/µm)	I_{on} (A/µm)	I_{on} increase	SS (mV/dec)	DIBL (mV/V)
50	49.56	PLANAR	0	1.06E-10	8.31E-04	0.00%	85.27	113
50	49.56	0	-0.367	1.06E-10	7.30E-04	-12.12%	79.01	99
50	49.56	5	-2.428	1.06E-10	7.08E-04	-14.77%	68.03	74
50	49.56	10	-4.146	1.06E-10	7.26E-04	-12.68%	66.21	68
50	49.56	15	-6.65	1.06E-10	7.46E-04	-10.28%	65.19	64
50	49.56	20	-9.791	1.06E-10	7.65E-04	-7.98%	64.59	61
40	39.56	0	-2.37	1.06E-10	7.40E-04	-10.96%	82.42	155
40	39.57	5	-6.924	1.06E-10	7.00E-04	-15.78%	69.93	105
40	39.57	10	-11.47	1.06E-10	7.01E-04	-15.62%	67.70	89
40	39.57	15	-16.08	1.06E-10	7.08E-04	-14.86%	66.67	81
40	39.57	20	-20.93	1.06E-10	7.16E-04	-13.79%	66.10	155

Generally, the PMOS SegFETs need a smaller body bias to meet the off-state leakage specification as compared with the NMOS SegFETs; figures 3-8 and 3-9 show that even for H_{Stripe} = 20 nm, however, the body-biased PMOS SegFETs barely surpass the drive current of the planar p-channel MOSFET.

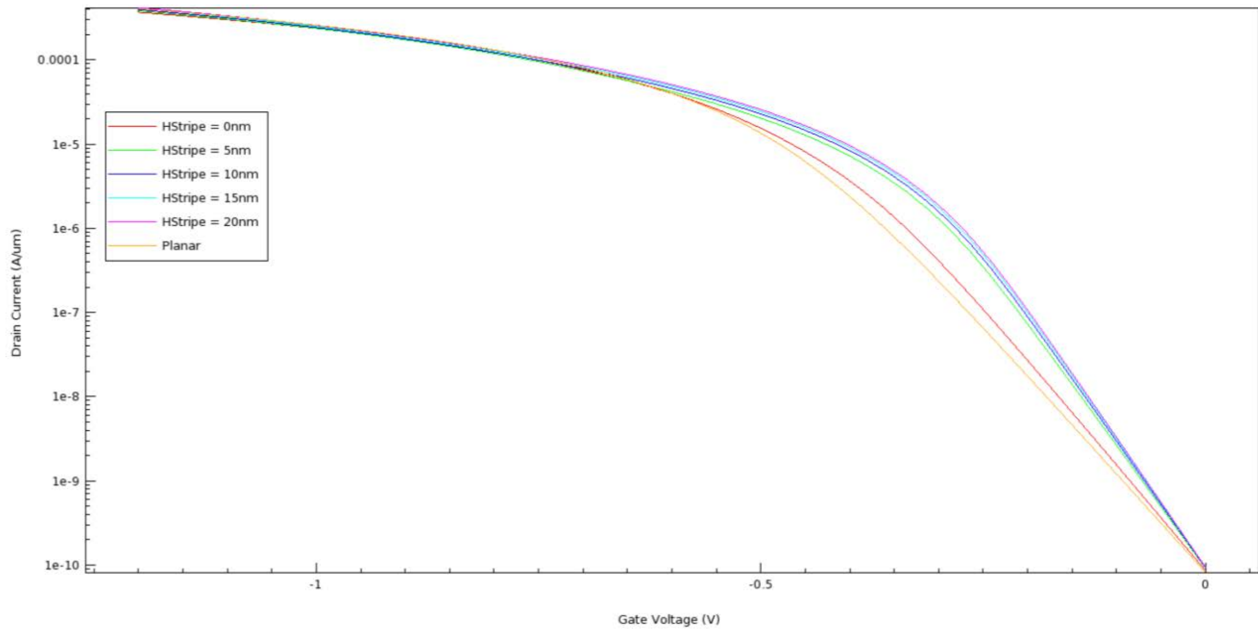

Figure 3-83-3: Simulated transfer characteristics for p-channel transistors with matched I_{off} achieved via reverse body biasing. (L_g = 50 nm, V_{ds} = V_{DD} = -1.2V.) Note the degraded transconductance for the body-biased SegFETs.

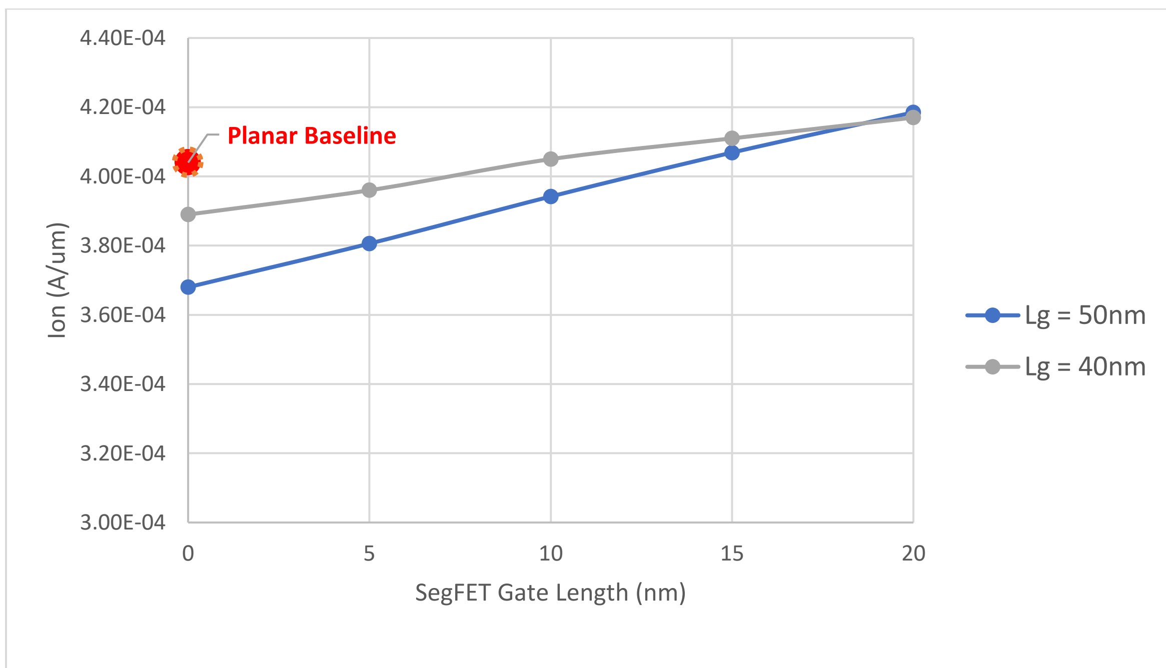

Figure 3-93-4: I_{on} vs. Stripe Height for p-channel SegFETs with V_t adjusted via body biasing.

Results for p-channel SegFETs with V_t tuned by reverse body biasing

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	V_{sb} (V)	Stressed I_{off} (A/µm)	I_{on} (A/µm)	I_{on} increase	SS (mV/dec)	DIBL (mV/V)
50	49.51	PLANAR	0	-1.03E-10	4.04E-04	0.00%	85.50	139
50	49.51	0	0.334	-1.06E-10	3.68E-04	-8.91%	79.75	144
50	49.52	5	2.231	-1.06E-10	3.81E-04	-5.79%	68.49	142
50	49.52	10	3.842	-1.06E-10	3.94E-04	-2.43%	66.58	133
50	49.52	15	6.177	-1.06E-10	4.07E-04	0.72%	65.55	126
50	49.52	20	9.115	-1.06E-10	4.19E-04	**3.59%**	64.94	122
40	39.51	0	1.871	-1.06E-10	3.89E-04	-3.69%	83.40	201
40	39.53	5	5.467	-1.06E-10	3.96E-04	-2.10%	70.54	187
40	39.53	10	11.102	-1.06E-10	4.05E-04	0.12%	68.21	165
40	39.53	15	15.401	-1.06E-10	4.11E-04	1.66%	67.15	154
40	39.53	20	19.98	-1.06E-10	4.17E-04	**3.29%**	66.56	148

SegFETs with V_t Adjusted via Body Doping

To increase V_t, the body dopant concentration was increased until the stressed off-state leakage current reached the specified value. The resultant larger body depletion charge results in larger transverse electric field in the inversion-layer channel in the on-state, degrading the carrier effective mobility and hence on-state drive current and transconductance. Although PMOS device performance is degraded less than NMOS device performance, figures 3-10 through 3-13 show that none of the SegFETs can match the on-state drive current of their baseline planar MOSFET counterpart, even with the largest stripe height.

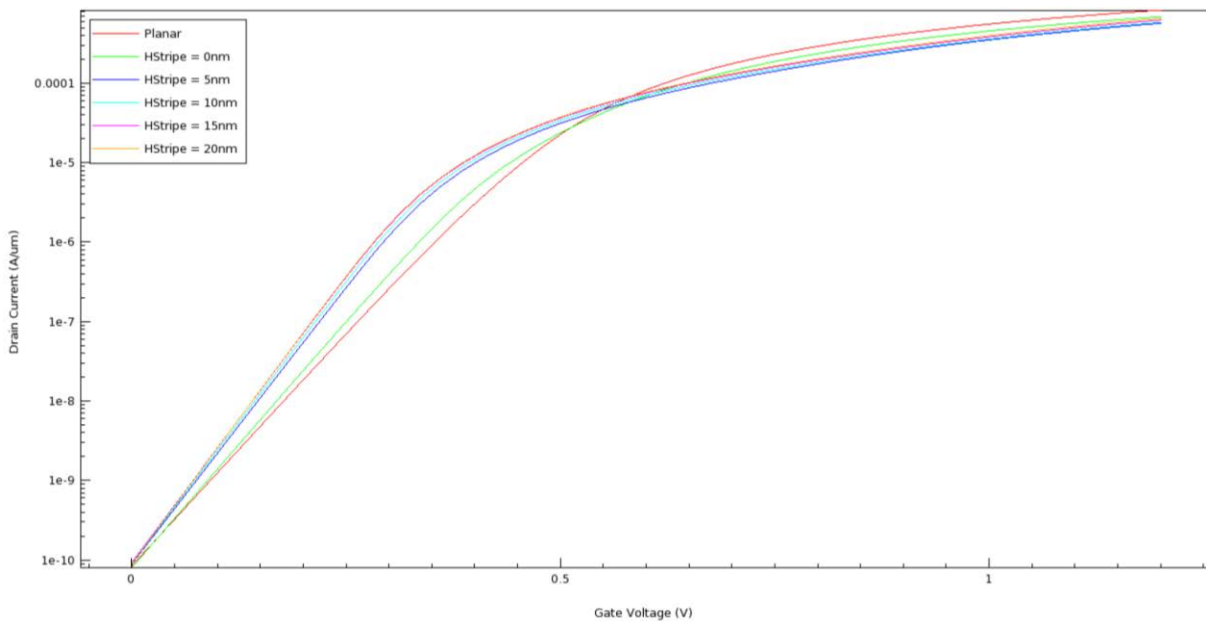

Figure 3-5: Simulated transfer characteristics for n-channel transistors with matched I_{off} achieved via body doping. (L_g = 50 nm, V_{ds} = V_{DD} = 1.2V.) Note the degraded transconductance.

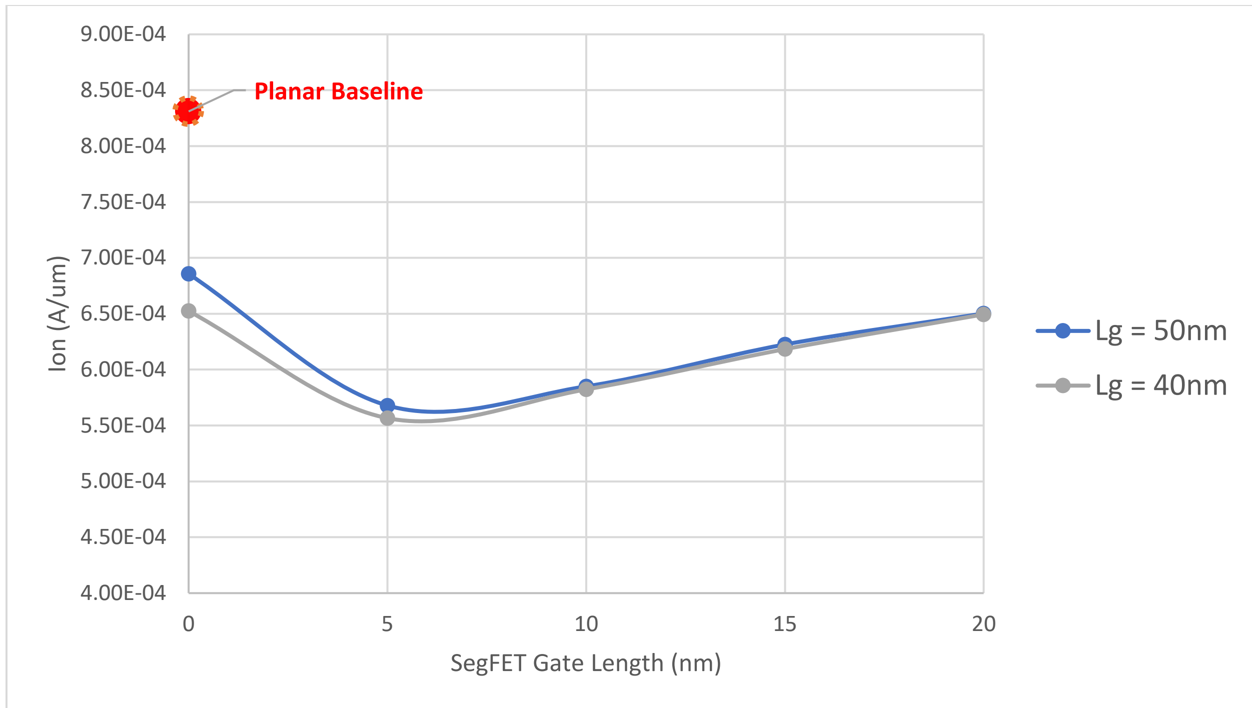

Figure 3-61: I_{on} vs. Stripe Height for n-channel SegFETs with V_t adjusted via body doping.

Results for n-channel SegFETs with V_t tuned by body doping

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	N_{sub} (cm^-3)	Stressed I_{off} (A/µm)	I_{on} (A/µm)	I_{on} increase	SS (mV/dec)	DIBL (mV/V)
50	49.56	PLANAR	3.00E+18	1.06E-10	8.31E-04	0.00%	85.27	113
50	49.67	0	3.52E+18	9.44E-11	6.86E-04	-17.48%	80.52	91
50	50.11	5	5.50E+18	9.52E-11	5.68E-04	-31.66%	71.69	61
50	50.25	10	6.15E+18	9.55E-11	5.85E-04	-29.60%	70.17	57
50	50.32	15	6.45E+18	9.84E-11	6.23E-04	-25.09%	69.20	56
50	50.35	20	6.60E+18	9.56E-11	6.50E-04	-21.76%	68.76	56
40	39.96	0	4.80E+18	9.72E-11	6.52E-04	-21.49%	83.91	123
40	40.37	5	6.70E+18	9.12E-11	5.57E-04	-33.02%	72.95	81
40	40.52	10	7.40E+18	9.53E-11	5.82E-04	-29.93%	71.01	74
40	40.58	15	7.70E+18	9.38E-11	6.18E-04	-25.60%	70.06	71
40	40.61	20	7.80E+18	9.42E-11	6.49E-04	-21.85%	69.62	71

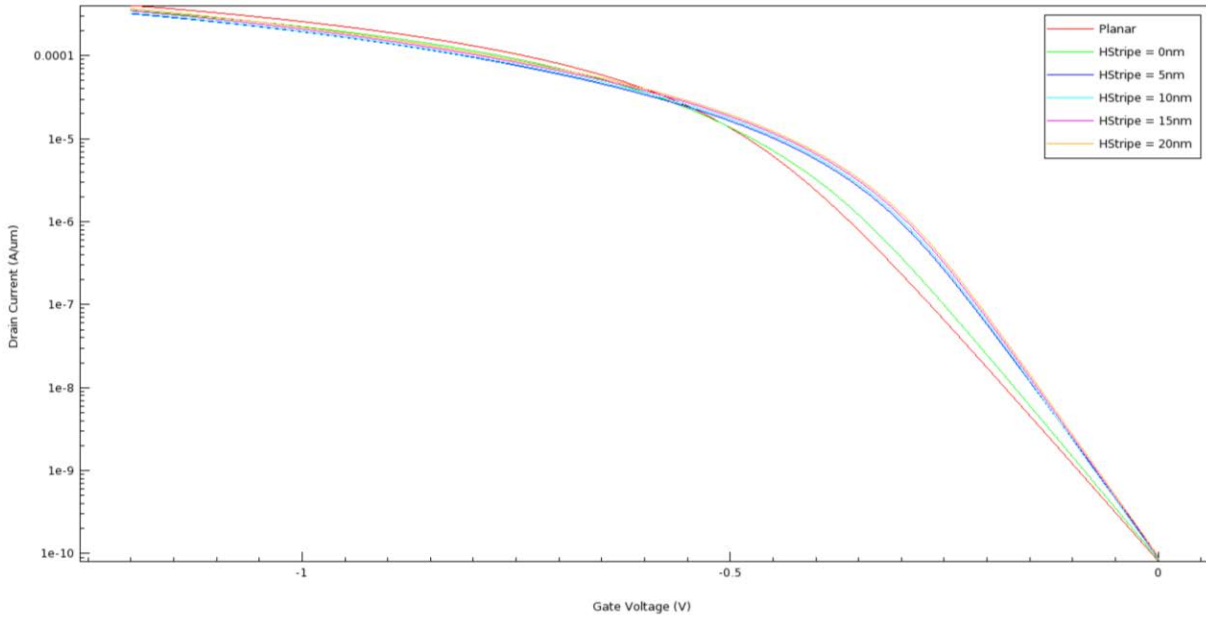

Figure 3-12: Simulated transfer characteristics for p-channel transistors with matched I_{off} achieved via body doping. (L_g = 50 nm, V_{ds} = V_{DD} = -1.2V.) Note the degraded transconductance.

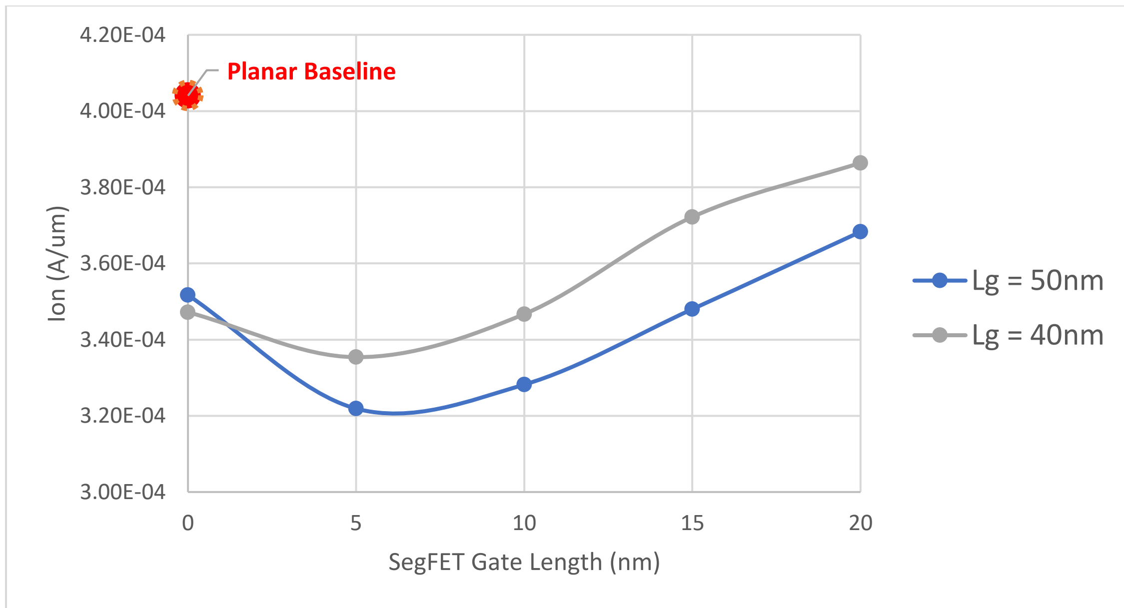

Figure 3-13: I_{on} vs. Stripe Height for p-channel SegFETs with V_t adjusted via body doping.

Results for p-channel SegFETs with V_t tuned by body doping

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	N_{sub} (cm^-3)	Stressed I_{off} (A/µm)	I_{on} (A/µm)	I_{on} increase	SS (mV/dec)	DIBL (mV/V)
50	49.51	PLANAR	2.79E+18	1.03E-10	4.04E-04	0.00%	85.50	139
50	49.6	0	3.20E+18	1.01E-10	3.52E-04	-12.95%	80.84	137
50	49.97	5	4.85E+18	1.01E-10	3.22E-04	-20.32%	71.38	130
50	50.11	10	5.50E+18	9.16E-11	3.28E-04	-18.76%	69.86	123
50	50.18	15	5.80E+18	9.34E-11	3.48E-04	-13.86%	68.92	119
50	50.2	20	5.90E+18	9.80E-11	3.68E-04	-8.84%	68.43	118
40	39.89	0	4.50E+18	8.93E-11	3.47E-04	-14.06%	84.44	181
40	40.22	5	6.00E+18	1.03E-10	3.35E-04	-16.98%	73.01	163
40	40.37	10	6.70E+18	9.61E-11	3.47E-04	-14.18%	71.01	150
40	40.42	15	6.90E+18	1.03E-10	3.72E-04	-7.87%	70.01	145
40	40.46	20	7.10E+18	9.70E-11	3.86E-04	-4.36%	69.54	144

3.2) SegFET Peak Cutoff Frequency

The peak f_T was found by performing a frequency sweep for various gate biases and extrapolating from a midband frequency for meaningful benchmarking against experimental results.

SegFETs with V_t Adjusted Using Gate Work Function Tuning

As shown in the plot below, f_T increases as the gate length is scaled down, as expected. For the zero stripe height devices, the gate length must be scaled significantly to achieve an increase in f_T as compared with the planar baseline device, due to the loss of conductive area and increase in parasitic capacitance from the corrugated substrate. f_T generally increases with stripe height, with diminishing returns as the stripe grows taller. This is because for large stripe heights, the incremental increase in drive current is outweighed by the increase in gate capacitance.

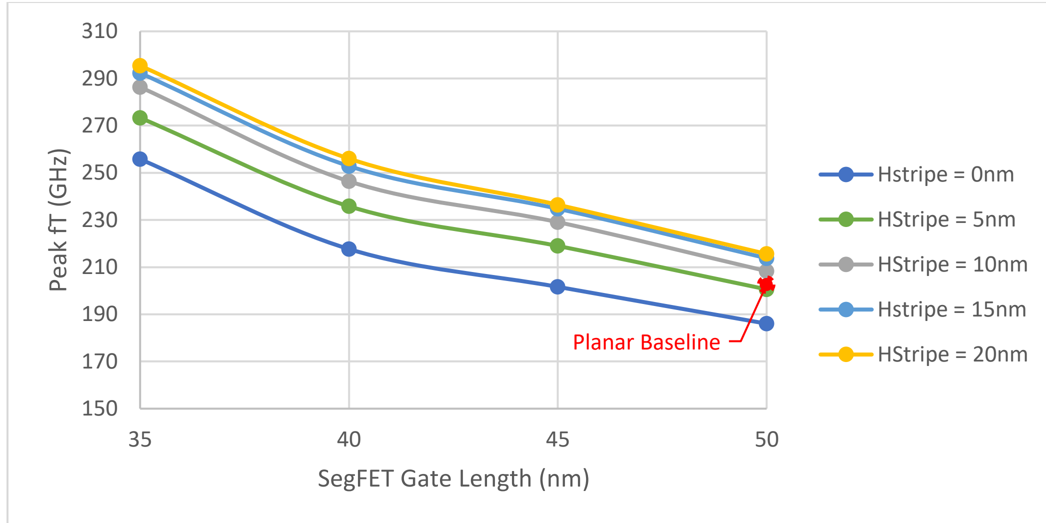

Figure 3-7: f_T improvement with gate length scaling for n-channel SegFETs

Results for n-channel SegFETs with V_t tuned by gate work function engineering

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	V_{gs} @ Peak f_T (V)	Peak f_T (GHz)	f_T increase
50	49.56	N/A	1.080	202.62	0.00%
50	49.56	0	1.076	186.05	-8.18%
50	49.56	5	1.142	200.59	-1.00%
50	49.56	10	1.144	208.32	2.81%
50	49.56	15	1.136	213.79	5.51%
50	49.56	20	1.2	215.6	**6.41%**
45	44.56	0	1.142	201.65	-0.48%
45	44.56	5	1.145	219	8.08%
45	44.56	10	1.140	229.11	13.07%
45	44.56	15	1.141	234.78	15.87%
45	44.56	20	1.138	236.47	**16.71%**
40	39.56	0	1.146	217.68	7.43%
40	39.57	5	1.141	235.8	16.38%
40	39.57	10	1.143	246.41	21.61%
40	39.57	15	1.140	252.87	24.80%
40	39.57	20	1.135	256.03	**26.36%**
35	34.57	0	1.2	255.79	26.24%
35	34.57	5	1.2	273.34	34.90%
35	34.57	10	1.2	286.34	41.32%
35	34.57	15	1.2	292.32	44.27%
35	34.57	20	1.2	295.44	**45.81%**

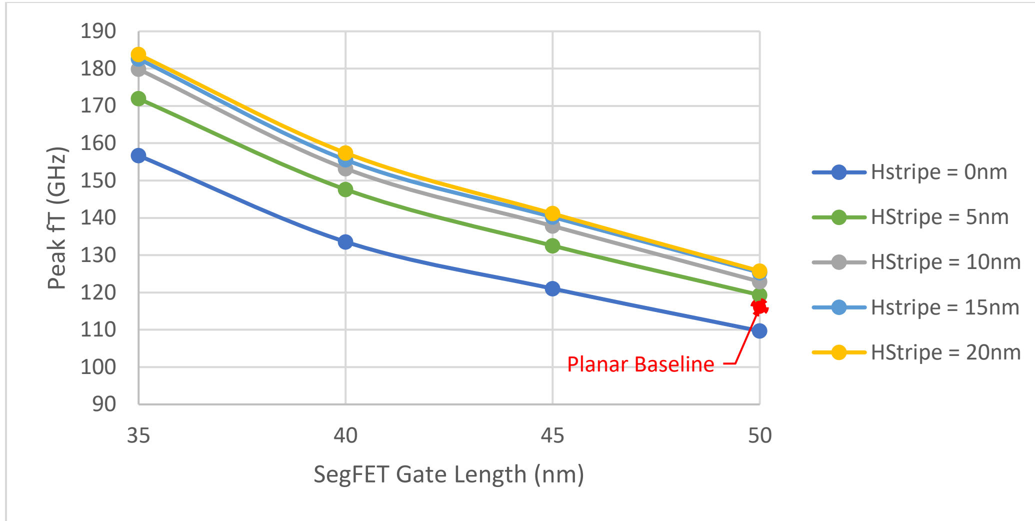

Figure 3-15: f_T improvement with gate length scaling for p-channel SegFETs

<u>Results for p-channel SegFETs with V_t tuned by gate work function engineering</u>

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	V_{gs} @ Peak f_T (V)	Peak f_T (GHz)	f_T increase
50	49.51	PLANAR	-1.2	116.01	0.00%
50	49.51	0	-1.2	109.66	-5.47%
50	49.52	5	-1.2	119.31	2.84%
50	49.52	10	-1.2	122.9	5.94%
50	49.52	15	-1.2	125.33	8.03%
50	49.52	20	-1.2	125.73	**8.38%**
45	44.51	0	-1.2	121.03	4.33%
45	44.51	5	-1.2	132.54	14.25%
45	44.51	10	-1.2	137.81	18.79%
45	44.51	15	-1.2	140.21	20.86%
45	44.51	20	-1.2	141.13	**21.65%**
40	39.51	0	-1.2	133.57	15.14%
40	39.53	5	-1.2	147.61	27.24%
40	39.53	10	-1.2	153.21	32.07%
40	39.53	15	-1.2	155.54	34.07%
40	39.53	20	-1.2	157.39	**35.67%**
35	34.53	0	-1.2	156.68	35.06%
35	34.53	5	-1.2	171.93	48.20%
35	34.53	10	-1.2	179.82	55.00%
35	34.53	15	-1.2	182.59	57.39%
35	34.53	20	-1.2	183.77	**58.41%**

SegFETs with V_t Adjusted Using Body Biasing

Since reverse body-biased SegFETs suffer from degraded carrier mobility, they generally have degraded f_T as compared with their planar baseline MOSFET counterparts. The 40nm gate length PMOS SegFETs can achieve higher f_T for stripe heights 10 nm and *below*, however. For both PMOS and NMOS SegFETs, the increase in on-state current with increasing stripe height is not enough to outweigh the effect of increased gate capacitance.

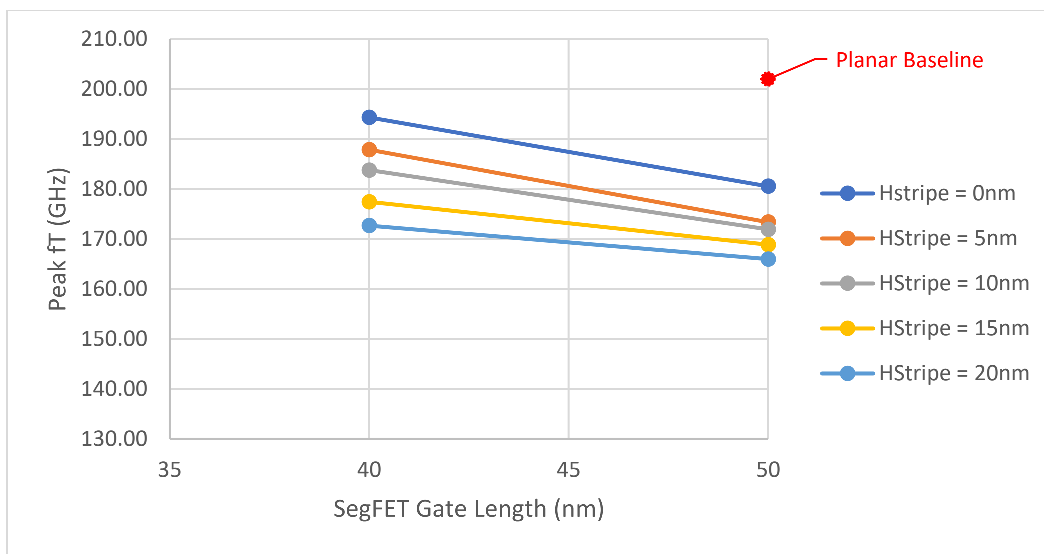

Figure 3-16: f_T improvement with gate length scaling for n-channel SegFETs with reverse body biasing

Results for n-channel SegFETs with V_t tuned by reverse body biasing

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	V_{sb} (V)	V_{gs} @ Peak f_T (V)	Peak f_T (GHz)	f_T increase
50	49.56	PLANAR	0.00	1.08	202.04	0.00%
50	49.56	0	-0.37	1.08	180.53	-10.65%
50	49.56	5	-2.43	1.20	173.35	-14.20%
50	49.56	10	-4.15	1.20	171.92	-14.91%
50	49.56	15	-6.65	1.20	168.85	-16.43%
50	49.56	20	-9.79	1.20	165.96	-17.86%
40	39.56	0	-2.37	1.08	194.32	-3.82%
40	39.57	5	-6.92	1.20	187.86	-7.02%
40	39.57	10	-11.47	1.20	183.78	-9.04%
40	39.57	15	-16.08	1.20	177.43	-12.18%
40	39.57	20	-20.93	1.20	172.66	-14.54%

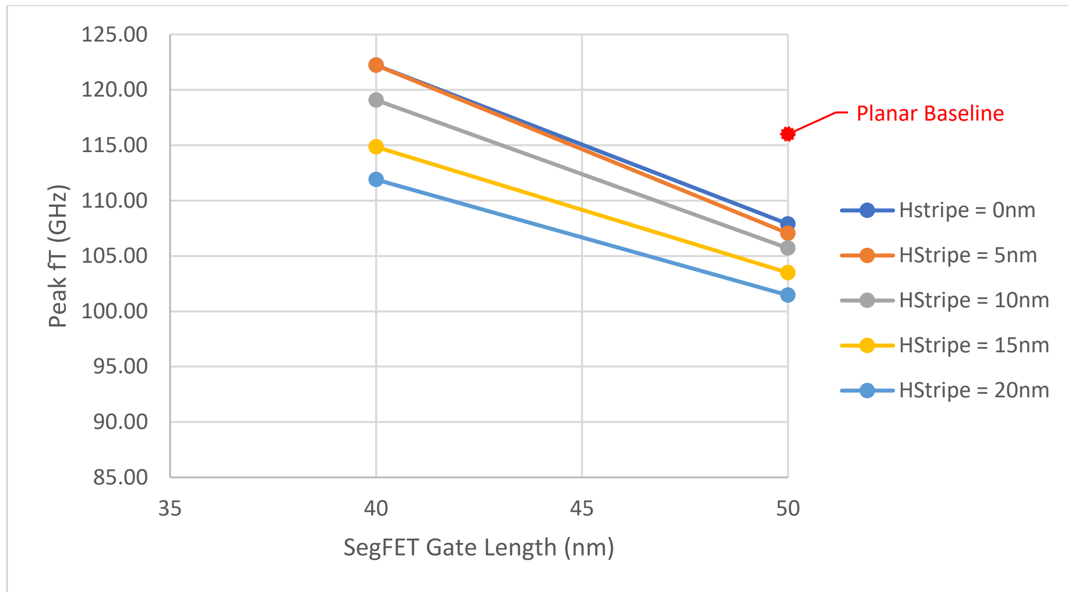

Figure 3-17: f_T improvement with gate length scaling for p-channel SegFETs with reverse body biasing

Results for p-channel SegFETs with V_t tuned by reverse body biasing

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	V_{sb} (V)	V_{gs} @ Peak f_T (V)	Peak f_T (GHz)	f_T increase
50	49.51	PLANAR	0.00	-1.20	115.95	0.00%
50	49.51	0	0.33	-1.20	107.89	-6.95%
50	49.52	5	2.23	-1.20	107.05	-7.68%
50	49.52	10	3.84	-1.20	105.70	-8.84%
50	49.52	15	6.18	-1.20	103.49	-10.75%
50	49.52	20	9.11	-1.20	101.45	-12.51%
40	39.56	0	1.87	-1.20	122.23	5.42%
40	39.57	5	5.47	-1.20	122.23	5.42%
40	39.53	10	11.10	-1.20	119.08	2.70%
40	39.53	15	15.40	-1.20	114.85	-0.95%
40	39.53	20	19.98	-1.20	111.90	-3.49%

SegFETs with V_t Adjusted via Body Doping

Since the on-state drive currents of the SegFET devices with higher levels of body doping are even worse than for the reverse body-biased ones, it logically follows that their f_T values would also be worse.

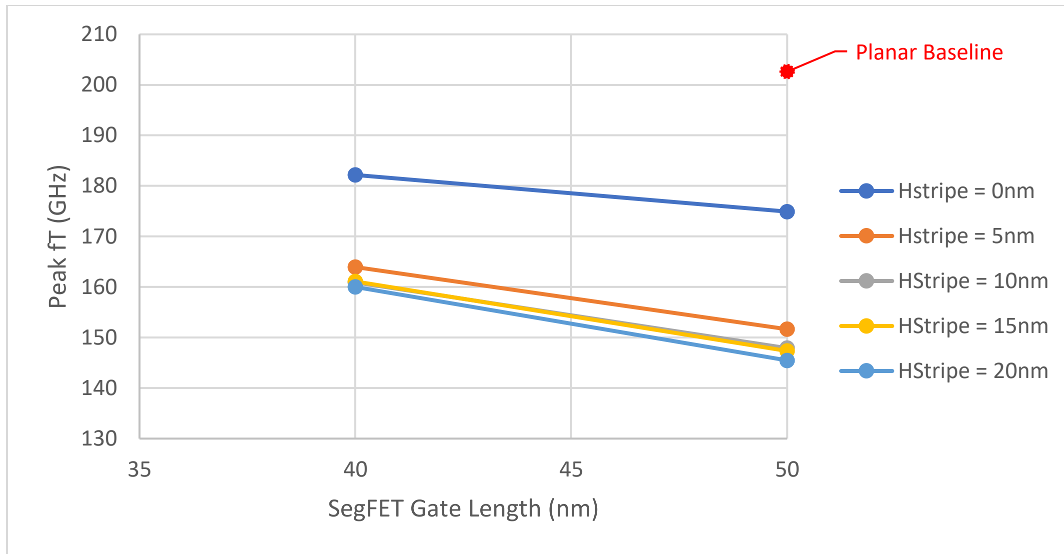

Figure 3-18: f_T improvement with gate length scaling for n-channel SegFETs with increased body doping

Results for n-channel SegFETs with V_t tuned by body doping

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	N_{sub} (cm^-3)	V_{gs} @ Peak f_T (V)	Peak f_T (GHz)	f_T Increase
50	49.56	PLANAR	3.00E+18	1.08	202.62	0.00%
50	49.67	0	3.52E+18	1.08	174.92	-13.67%
50	50.11	5	5.50E+18	1.2	151.64	-25.16%
50	50.25	10	6.15E+18	1.2	147.9	-27.01%
50	50.32	15	6.45E+18	1.2	147.34	-27.28%
50	50.35	20	6.60E+18	1.2	145.47	-28.21%
40	39.96	0	4.80E+18	1.14	182.17	-10.09%
40	40.37	5	6.70E+18	1.2	163.94	-19.09%
40	40.52	10	7.40E+18	1.2	160.9	-20.59%
40	40.58	15	7.70E+18	1.2	161.09	-20.50%
40	40.61	20	7.80E+18	1.2	160	-21.03%

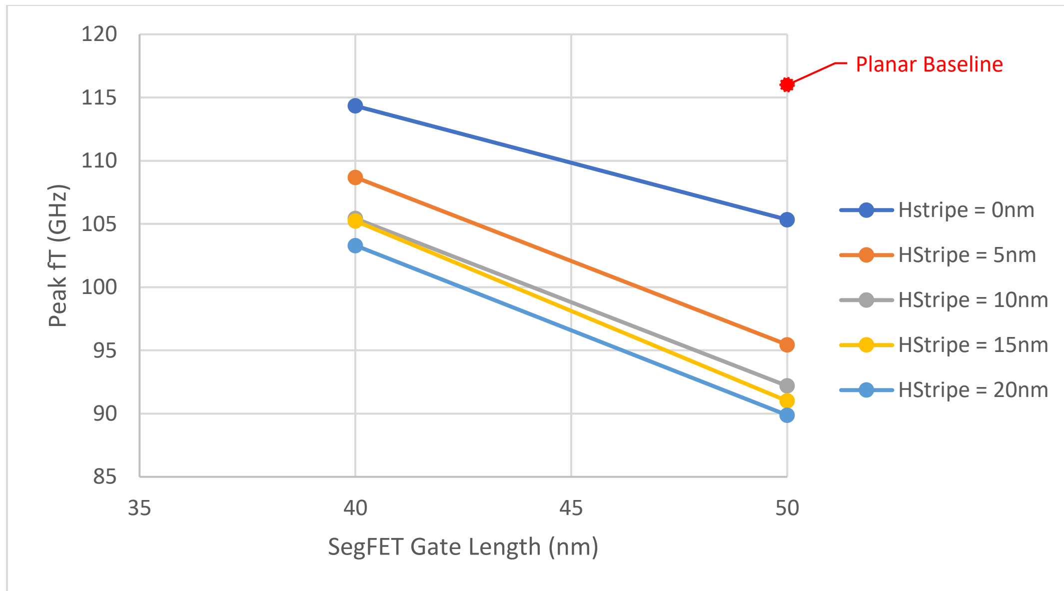

Figure 3-19: f_T improvement with gate length scaling for p-channel SegFETs with increased body doping

Results for p-channel SegFETs with V_t tuned by body doping

L_g (nm)	L_{eff} (nm)	H_{Stripe} (nm)	N_{sub} (cm^-3)	V_{gs} @ Peak f_T (V)	Peak f_T (GHz)	f_T increase
50	0.04951	PLANAR	2.79E+18	-1.2	116	0.00%
50	0.0496	0	3.20E+18	-1.2	105.34	-9.19%
50	0.04997	5	4.85E+18	-1.2	95.45	-17.72%
50	0.05011	10	5.50E+18	-1.2	92.19	-20.53%
50	0.05018	15	5.80E+18	-1.2	91	-21.55%
50	0.0502	20	5.90E+18	-1.2	89.88	-22.52%
40	0.03992	0	4.50E+18	-1.2	114.34	-1.43%
40	0.04033	5	6.00E+18	-1.2	108.69	-6.30%
40	0.04037	10	6.70E+18	-1.2	105.43	-9.11%
40	0.04041	15	6.90E+18	-1.2	105.24	-9.28%
40	0.04054	20	7.10E+18	-1.2	103.3	-10.95%

Chapter 4 - Conclusions and Future Work

4.1) SegFET design optimization for high-frequency performance

Gate work function tuning is the best approach for tuning V_t to meet the off-state leakage current specification. For NMOS, the SegFET has a maximum 56.5% drive current advantage (at L_g = 40 nm, H_{Stripe} = 20 nm) and 45.8% f_T advantage (at L_g = 35 nm, H_{Stripe} = 20 nm) over the baseline planar MOSFET (L_g = 50 nm). For PMOS, performance gains are even greater: SegFET has a maximum 76.37% drive current advantage (at L_g = 35 nm, H_{Stripe} = 20 nm) and 45.8% f_T advantage (at L_g = 35 nm, H_{Stripe} = 20 nm).

Modern metal gate CMOS process technologies are ideal for implementation of SegFET devices. In older polysilicon gate CMOS process technologies, work function tuning may not be an option. For analog ICs in which a transistor is always on, such as those used for RF data transmission/reception, the circuits in principle could be designed to operate with smaller gate bias voltages to compensate for the lower V_t values of SegFETs.

4.2) Future Work

The SegFET designs investigated in this work had a few limitations. For starters, a constant channel/body doping profile was used to conform to TI's baseline specifications. Further studies should use a more realistic two-dimensional channel and body doping profiles to more accurately predict electrostatic integrity improvement and V_t shift for the SegFET structure.

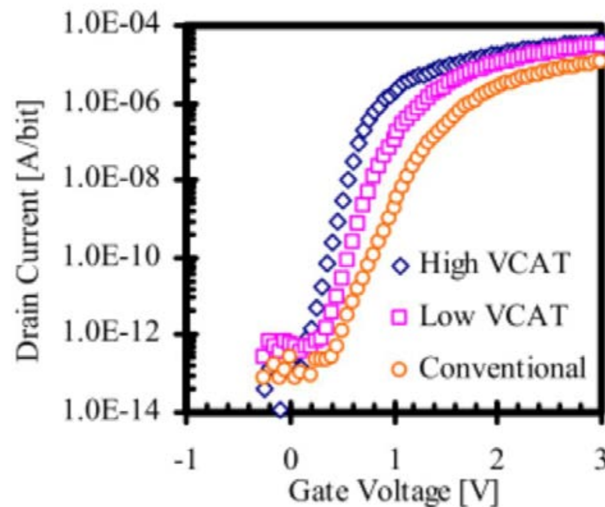

Figure 4-1: Transfer characteristics for a commercial foundry implementation of the SegFET [9]

Previous experimental work with commercial foundries [9], [13] has shown that when switching to the SegFET structure the off-state leakage can be kept constant without any need for threshold voltage adjustment, in contrast to the work of B. Ho [12]. In practice, figure 4-1 suggests the off-state leakage current may be dominated by drain-substrate junction leakage unrelated to the gate bias [9], [13]. Simulation of the SegFET structure with a realistic doping profile and accounting for band-to-band tunneling leakage would capture this effect. And finally, fabrication and characterization of sub-50 nm SegFET structures would help to calibrate our TCAD models for more accurate projections of device performance improvements.

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