Enhancing Performance of Analog Mixed Signal Circuits using Integrated Silicon-Photonics

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by

Nandish Mehta

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Professor Vladimir Stojanović, Chair
Professor Eli Yablonovitch
Professor Jie Yao

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Abstract

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Silicon-photonics (SiPh) has emerged as a viable solution to handle exponentially growing data traffic in today's data centers. It transfers data faster and over a distance longer than that possible with traditional electronics, while leveraging efficiency and cost benefits of existing high-volume CMOS manufacturing infrastructure. As the SiPh platforms mature, new high-performance photonics blocks integrated close to CMOS transistors are made available. By moving certain functionality to these optical blocks, the performance of conventional analog mixed-signal circuits can be improved to enable exciting new integrated applications like LiDAR, biosensing, high-performance computing, etc.

This thesis demonstrates an optical SiPh link with a reduced laser power requirement and an optically sampled analog-to-digital converter. Both of these systems benefit from the availability of integrated SiPh blocks next to CMOS transistors. The laser power used by a SiPh link can be reduced by improving the optical receiver (Rx) sensitivity and reducing the optical path loss. To improve the Rx sensitivity, a differential detector is monolithically integrated with the low-noise CMOS analog frontend (AFE), while the optical path loss is reduced by adopting a laser-forwarded architecture. The differential detector enables the fully differential operation of AFE to suppress power supply and common-mode noise. Measurement and performance comparison of two variants of differential detector implemented on two test-chips is presented. The proposed microring resonator differential detector enables the receiver to achieve a record OMA sensitivity of -18 dBm at 12 Gb/s. Modeling and characterization of this detector are also covered in this thesis. Further, a coherent laser-forwarded binary-phase-shift-keying (BPSK) link at 10 Gb/s is shown with all the required photonic blocks, like phase modulator, 3-dB coupler, and balanced detectors, fully integrated into a monolithic zero-change 45nm SOI CMOS. This link operates with 3 dB less laser power than state-of-the-art NRZ monolithic SiPh links.

Lastly, the performance of conventional CMOS ADCs is often limited by sampling clock-jitter, input sampling bandwidth, and routing of input and clock to the sub-ADCs. To overcome these limitations, this thesis demonstrates an optically sampled ADC that moves

the sampling function to the optical domain where ultra low-jitter (<10 fs_{rms}) optical pulses from a mode-locked laser sample an RF input signal with very high sampling bandwidth. An ADC prototype, realized in a 3D integrated silicon-photonic platform, achieves 37 dB SNDR (6b ENOB) for 45GHz input with <36fs estimated sampling jitter. Circuit techniques used for overcoming issues like single-ended to differential conversion and cross-talk are described in detail.

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Acknowledgements

I was introduced to the fascinating field of integrated circuit design by stumbling upon the video lectures of Prof. Bob Broderson and Prof. Jan Rabaey hosted on the UC Berkeley webcast. Since then I harbored a dream of pursuing research at Berkeley. Years later, as my aspirations turn to reality, I look back to realize they weren't have been fulfilled without the support and help of many wonderful individuals. I take this opportunity to thank them.

Foremost, I wish to express my thanks and appreciation to my advisor Professor Vladimir Stojanović. He taught me by example how to persevere for what you believe and how not to let setbacks (like the rejection of research papers) deter you from achieving the final goal. His ability to identify the right path forward and his foresight to avoid stepping on potential landmines is simply amazing. I am grateful to him for empowering me to look further by letting me stand on his shoulders.

I am grateful to Professors Eli Yablonovitch and Jie Yao for their invaluable feedback on my research proposal and for serving on my thesis committee. I also thank them and Professor Borivoje Nikolić for serving on my qualifying exam committee. During my Ph.D., I had the pleasure of consulting with Professor Ming Wu on topics ranging from component procurement to measurement methods for device characterization. He also taught me a wonderful course on how optical components work and was very kind to share his lab equipment whenever I had the need. I thank him from the bottom of my heart. I would also like to thank Professor Johan Huijsing from the Delft University of Technology for his enthusiastic support and guidance that I received while designing a test-chip for a hobby project. I am infinitely grateful to him for teaching me the finer nuances of analog circuits. I would also like to express my gratitude to Professor Ali Niknejad for teaching me two courses on RF circuits and letting me serve as a GSI for one of them. I will always remember him for the high standards he applies to teaching and for being humble and down to earth person. I also gratefully acknowledge the financial support I received from Prof. Bernard Boser during the first year of my Ph.D.

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The test setups presented here to demonstrate the proposed electro-optic systems would not have been possible without active support from our industry partners. The generosity of Joel Nelson and Kenn Wildnauer from Keysight Technologies knew no bounds. Joel went out of his way to arrange a high-frequency PSG signal generator when I was caught in a time-critical situation, while Kenn was kind enough to provide an optical transceiver module

for DCA which was used extensively to demonstrate the coherent link.

Developing the test-bench for optically sampled ADC was one of the most challenging tasks I undertook during my Ph.D. I am deeply grateful to all who made the accompanying stress and frustration bearable. I am thankful to Simon Kocur (Menlo Systems Inc) for loaning mode-locked laser source, Max Wang (Lightel Technologies) for designing the optical de-mux on a short notice, and folks at Integra Technologies: Kirk Feyerabend, Joe Foerstel, and Chau Vu, for their help with wafer-probing and dicing, chip assembly complying my unwieldy requirements, and wirebonding. I am indebted to Russell Wilcox (ATAP, LBNL) for teaching me how to measure mode-locked laser phase noise, how to be methodical in assembling the test-setup, and how to handle sensitive optical components. I would also like to thank Guan-Lin and Jean-Etienne from Professor Ming Wu's group for openheartedly sharing the lab components. A huge thanks are reserved for Terence Collier (CV Inc) for flip-chip assembly of several of my test-chips. His willingness to work on my project timeline helped me enormously to meet several deadlines.

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Making new friends is by far the most valuable perks of grad school. I was very fortunate to be a part of the Integrated Systems Group (ISG), which is as much of a research group as its a family. The culture of collectively tackling tough problems is inscribed in the core of ISG. When I joined, I was greeted by Chen Sun who had to spend enormous time to get me to speed. Throughout my Ph.D. I used some of the digital IPs and testing codes that he developed. I am also greatly indebted to him for offering me an internship in his startup Ayar labs. I was fortunate to have colleagues like Sen Lin, Sajjad Moazeni, Krishna Settaluri, Taehwan Kim, and Pavan Bhargava. I owe them my heartfelt gratitude for being an amazing company. Sen is the nicest person I came across. His approach to any problem and the clarity of thinking is something I aspire to emulate. Sajjad was very kind to teach me how to drive and how to avoid the *lane to heaven* (driving on top of lane marker). I owe it to Krishna for teaching me the importance of living a healthy lifestyle and the several debates we had around this topic. I worked with Taehwan and Pavan on a couple of test-chips, and I thank them for their immense help in meeting the tape-out deadline. Specifically, I am indebted to Taehwan. During our first chip tape-out, his last-minute decision to retain one of my IP blocks at the top-level gave me the first paper of my Ph.D. I also would like to

wish all the very best to current ISG members: Christos, Panos, Kourosh, Bohzi, Daniel, and others, in carrying out pioneering research that ISG is known for.

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I owe my deepest gratitude to my wife Varsha for her love and care, and for making me see the brighter side when dark clouds of bleakness closed in. I have heavily relied on her resourcefulness and ability to think outside the box when I couldn't see a path forward. I simply cant imagine how I would have survived grad school without her not being on my side. I am also grateful to my brother Boris for running errands for me on several occasions.

Today, I badly miss my loving grandpa, who passed away last year. He will be eternally in my memory and his lessons on the value of family, health, and time in one's life, will guide me in time to come.

Finally, and most importantly, I owe my heartfelt gratitude to my parents. If I have braved through uncharted waters, it was for my parents who always encouraged me to pursue my dreams. Their unending love is a reminder that no matter what, if I stumble or get knocked down, they will be always there for me. Their unwavering support has been a continual source of strength. This work is the product of their endless love and blessings, and I dedicate it to them.

Chapter 1

Introduction

Since the invention of integrated circuits in the 1960s transistors have scaled from 50 μm minimum feature size with 10's of components on a die to a feature size of less than 10 nm with billions of transistors. Historically, a new generation of process technology node is developed on a two-year cadence with the minimum feature size scaling approximately by 0.7x and the area scaling by 0.5x. Thus, the density of transistors has been doubling every two years, which was famously predicted by Gordon Moore [1, 2]. The primary drivers behind this technology scaling (or Moore's law) have been the dramatic reduction in the cost-per-transistors and enhanced functionality. However, owing to the limitations imposed by electrostatic control, power, device density, and process variability the process is getting complex and the number of photomasks is increasing. Subsequently, technology scaling is slowing down with recent technology nodes such as 14 nm and 10 nm are taking longer to develop and are getting prohibitively expensive for all but highest-volume (100s of millions of parts) applications [3].

While the cost-benefit of technology scaling is diminishing, the functional benefit can be enhanced by complementing transistors with beyond-silicon counterparts. This phase-2 of Moore's law is often referred to as More-than-Moore scaling, where the goal is to realize new systems that provide functional benefits by integrating new devices in silicon and adopting new integration approaches. The benefits afforded by these new systems that are enabled by the beyond-silicon devices can far exceed the benefits any improved device by itself could achieve. Figure 1.1 shows a few examples of such More-than-Moore systems. As shown in Fig. 1.1(a), back in 1990, researchers in [4] integrated an inductor in conventional CMOS process, which enabled full CMOS radios [5] that lead to the mobile revolution. Along the same vein, integration of optical blocks enabled the world's first RISC-V microprocessor that communicates with on-chip memory using optical links as shown in Fig. 1.1(b). Recently, researchers in [6] integrated two computation layers directly on top of a conventional silicon imager, forming a 3D structure in Fig. 1.1(c), using carbon nanotubes. This enables the imager to convert the raw image data to actionable information for low-latency image classification or object detection. Thus, embracing the More-than-Moore scaling enhances the system functionality, and improves the processing speed and capacity. However, this

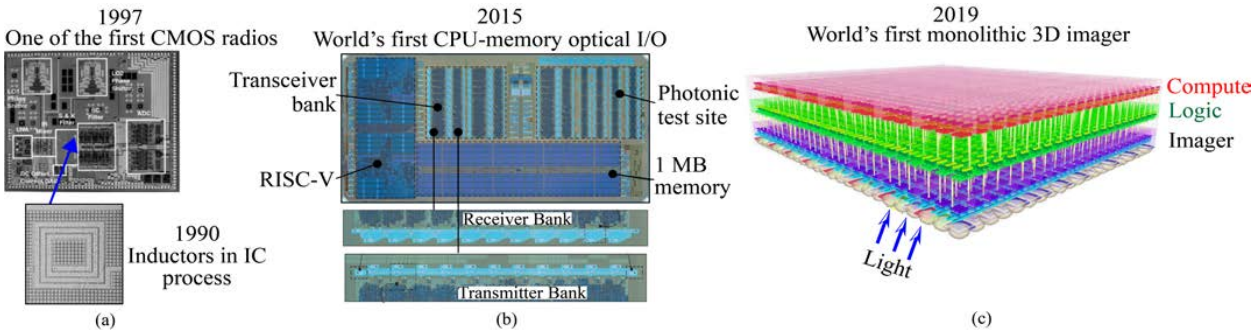


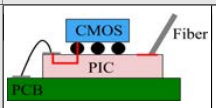
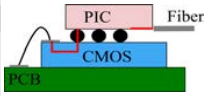
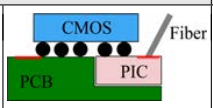
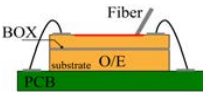
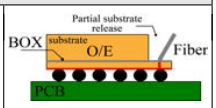
Figure 1.1: Examples of More-than-Moore scaling: (a) integrating inductors in IC process [4] and the world's first CMOS radios made using them [5] (b) World's first processor-memory communication using light [7] (c) Monolithic 3D integrated CMOS imagers [6].

must be done by enabling heterogeneous integration technologies that are compatible with the mainstream CMOS manufacturing process as it can result in much tighter integration of silicon and beyond-silicon devices.

The integration of Silicon-Photonics (Si-Ph) with CMOS can have a practical and profound impact on several applications from data movement to RF signal processing and sensing to analog and mixed-signal circuits. The photonic devices fabricated on semiconductor-based chips, often referred to as photonic integrated circuits (PICs), offer low-cost, improved matching, and high-reliability. There are various ways in which Si-Ph can be integrated with CMOS. Table 1.1 summarizes various Si-Ph platforms reported in literature. In a hybrid approach the PIC and CMOS chips are vertically integrated either using C4 BGA bumps or even Cu pillars/μ-bumps [8, 9, 10]. Typically, this approach often has challenges in terms of packaging and limited interconnect pitch. To overcome it, photonic blocks can be monolithically integrated next to CMOS in a silicon-on-insulator (SOI) process [11, 12] or the photonic wafer and CMOS wafer can be 3D integrated at wafer-scale [13]. With small adjustments to the underlying CMOS process, it is also possible to integrate photonics in a bulk CMOS [14].

Whether it is hybrid or monolithic, the goal of both of these platforms is to bring Si-Ph in close proximity to CMOS. Subsequently, interesting analog and mixed-signal applications such as large-bandwidth high-resolution ADCs,low-phase noise signal sources, energy-efficient communication links, and photonic phase arrays, etc., can be realized. Because the photonics is close to CMOS, some of the functions limiting the performance of CMOS-only circuit can be moved to the photonic domain, and vice versa - CMOS can help alleviate some impairments of photonic devices (such as thermal tuning, equalizing limited bandwidth of the detector, etc). The goal of this thesis is to demonstrate such improvement in performance in an optical communication link and an analog-to-digital converter.

Table 1.1: Overview of various Si-Ph platforms

Integration	**Hybrid**			**Monolithic**	
Structure†					
Example	Xilinx [8]	Oracle [9]	Fujitsu [10]	Luxtera [11]	Ayar Labs [12]
Integration Density	High Density	Low Density	Moderate Density	Low Density	Very-high Density
Process Optimization	Independent to choose	Independent to choose	Independent to choose	Constrained	Constrained
Signal/Supply connection	Wirebond	Wirebond	Bumping e.g.C4 BGA	Wirebond	Bumping e.g.C4 BGA
Fiber-to-chip assembly	Moderate	Difficult	Easy	Moderate	Easy
Packaging	Moderate	Difficult	Difficult	Easy	Easy

†PIC: Photonic Integrated Chip, O/E: Optical/Electronics transceiver

1.1 Research Goal and Contributions

This thesis attempts to solve performance bottlenecks in traditional analog and mixed-signal systems by leveraging the availability of silicon-photonics blocks close to CMOS circuits. The resulting system achieves performance which is better than that of a traditional CMOS-alone solution. To this end, this thesis demonstrates, first, an optical Si-Ph link that needs lesser laser power and, second, an optically sampled ADC.

Improving Rx sensitivity is crucial to reduce Si-Ph link laser power requirement. For this purpose, a high-sensitivity optical Rx is realized using a differential receiver with a low-noise analog front-end (AFE). Initial findings from version-1 test-chip appeared in the following article:

- [15] N. Mehta, C. Sun, M. Wade, S. Lin, M. Popovic and V. Stojanović, "A 12Gb/s, 8.6App input sensitivity, monolithic-integrated fully differential optical receiver in CMOS 45nm SOI process," *42nd European Solid-State Circuits Conference (ESSCIRC)*, Lausanne, Sept 2016, pp. 491-494.

Several monolithic Si-Ph platforms with varying performance are reported in the literature. A review and comparison of these state-of-the-art platforms, categorized by volume (i.e. research foundry or high-volume), are summarized in the reference below:

- [16] V. Stojanović, R. Ram, M. Popović, S. Lin, S. Moazeni, M. Wade, C. Sun, L. Alloatti, A. Atabaki, F. Pavanello, N. Mehta, and P. Bhargava, "Monolithic silicon-photonic platforms in state-of-the-art CMOS SOI processes," *Optical Express* 26, 13106-13121 (2018).

The limitations of version-1 test-chip are addressed in a re-spin version-2 test-chip. It uses a novel microring resonator (MRR) based differential split detector that achieves high responsivity and occupies a small footprint while being amenable to DWDM. A comprehensive measurement and characterization of MRR-based split photodetector (MRR split-PD) are published in the article below:

- [17] N. Mehta, C. Sun, M. Wade and V. Stojanović, "A Differential Optical Receiver With Monolithic Split-Microring Photodetector," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2230-2242, Aug. 2019.

The following paper covers design and characterization MRR PD along with a procedure to extract equivalent SPICE model parameters:

- [18] N. Mehta, S. Buchbinder, and V. Stojanović, "Design and characterization of monolithic microring resonator-based photodetector in 45nm SOI CMOS," in *45th European Solid-State Circuits/Devices Conference (ESSCIRC/ESSDERC)*, Krakow, Sep. 2019, pp. 206-209

In addition to improving Rx sensitivity, reducing optical path loss is equally important to reduce the minimum laser power required by Si-Ph link. To do so, the article below demonstrates an integrated laser-forwarded coherent link whose architecture is first proposed in [19]. The SNR benefits from coherent detection are experimentally validated in this paper.

- [20] N. Mehta, S. Lin, B. Yin, S. Moazeni and V. Stojanović, "A Laser-forwarded Coherent 10Gb/s BPSK Transceiver using Monolithic Microring Resonators in 45nm SOI CMOS," *Symposium on VLSI Circuits*, Kyoto, Japan, 2019, pp. C192-C193.

In the last half of this thesis, an optically sampled ADC (O-ADC) is demonstrated that addresses the sampling clock jitter and the limited input bandwidth problem of conventional CMOS ADCs. A test-chip in a heterogeneous 3D integrated platform with Si-Ph and 65-nm CMOS connected using high-density TOVs is realized. A test-bench that uses MLL to generate the optical pulses is set up to characterize the performance of O-ADC. Subsequently, the O-ADC chip is extensively characterized for static and dynamic performance. The optical pulse sources were measured to have less than 26 fs_{rms} jitter, while the sampling bandwidth measured, was 45 GHz, which is substantially higher than state-of-the-art CMOS ADCs.

1.2 Thesis Organization

Chapter 2 of the thesis articulates laser power as a bottleneck to improving Si-Ph link energy-efficiency and subsequently motivates the need for high-sensitivity optical receivers. Various error sources that degrade Rx sensitivity are explained. It also introduces 45-nm SOI CMOS monolithic Si-Ph platform and provides implementation details of version-1 test-chip that realizes a fully-differential receiver using an on-chip 3dB optical power splitter.

The limitation of version-1 test-chip, viz. poor responsivity, sizeable footprint, need for calibration, and nonconformity to DWDM, are addressed by the version-2 test-chip as detailed in Chapter-3. Design, modeling, and characterization of the microring resonator (MRR) based photodetector are also covered. Further, using the design techniques from chapter-2 and 3, a coherent receiver is realized in chapter 4, which is used in a laser-forwarded coherent link. Chapter 4 also discusses the architecture of the laser-forwarded link and its capabilities to improve overall link energy efficiency by lowering the required laser power.

Chapter 5 explains the performance limitation of conventional CMOS ADCs and discusses the architecture of O-ADC that can provide a potential solution. The limitations and various design tradeoffs of O-ADC are detailed. Chapter 6 discusses the design details of the AFE that integrates, amplifies, and quantizes the current pulse output from the photodetector.

An O-ADC test-chip is implemented in a heterogeneous 3D integration Si-Ph platform. An overview of this process along with packaging and test-chip assembly details are covered in Chapter 7. The measurement results that demonstrate high input sampling bandwidth of the O-ADC are also shown. Lastly, chapter 8 concludes this thesis and outlines future opportunities and new applications enabled by the integration of CMOS with silicon-photonics.

Chapter 2

Monolithic Silicon-Photonic link using Microring Resonators

With the proliferation of machine-learning workloads and cloud computing applications, the IP-data traffic in the hyper-scale data centers has increased rapidly. Many of these applications try to analyze and compute extremely large data sets to reveal patterns, trends, and associations, especially relating to human behavior and interactions. As a result, data traffic between the optical transceivers shown in Fig. 2.1(a) is increasing rapidly. Over the next few years, this data traffic within the rack is expected to increase by a factor of 3x [21]. Figure 2.1(b) shows this trend between 2016-2021.

Moving the high volume of data is starting to get limited by the input/output ports' (I/O) bandwidth. The traditional electrical I/Os (input/output) has hit the physical limit requiring the reach to decrease as the data rate increases. The optical I/Os one the other hand, do not suffer from the same limitation. Subsequently, they have emerged as a viable replacement for the electrical I/Os. However, for ubiquitous adoption, along with high bandwidth density, the optical I/Os should provide high energy efficiency at low cost. To meet these challenges, as shown in Fig. 2.2(a), the optical I/Os have evolved from conventional pluggables to optics on-board to co-packaging of optics with high-performance SoCs like a switch ASIC. With each generation, the optics moves closer to the SoC reducing the reach for the electrical I/Os from 200 mm down to <10 mm. As a result, the electrical I/Os get denser with shorter-reach, and thus, more energy efficient reducing the total system-level power by >30% [22]. To enable this, increased level of integration between the optical/electrical (O/E) transceiver chiplets and high performance SoC like a switch ASIC in Fig. 2.2(a) should be achieved. Eventually it leads to a densely co-packaged solution on a single substrate as shown in Fig. 2.2(b).

In addition to achieving high-bandwidth density, the optical I/Os in the O/E chiplets should also have good energy-efficiency in order to keep the power dissipation of the entire package to manageable level. A possible solution to achieving high-bandwidth density is to ensure the optical I/Os are amenable to dense wavelength division multiplexing (DWDM). While better energy-efficiency can be achieved by realizing photonic blocks like modulator

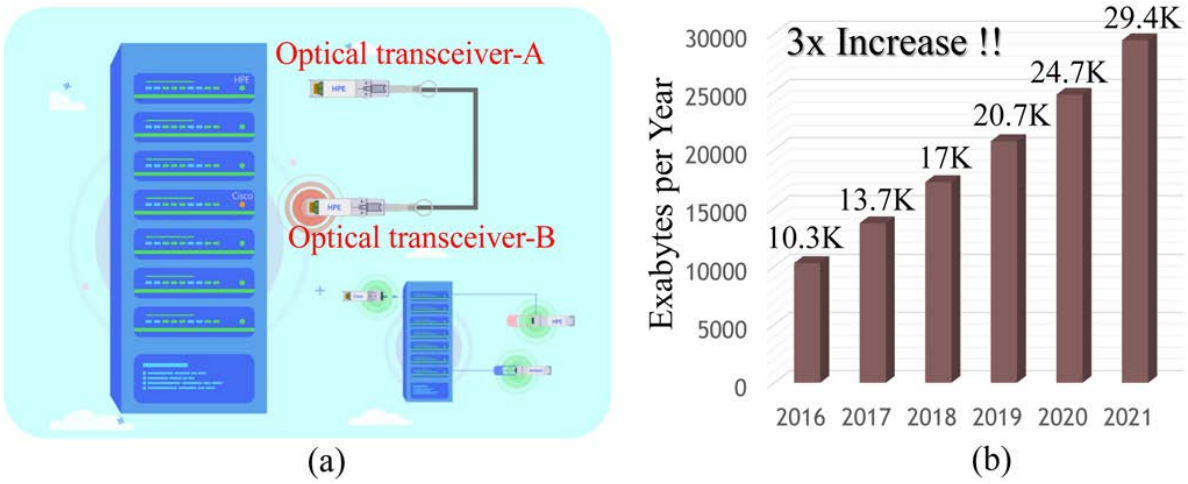


Figure 2.1: (a) Optical transceivers used in a data center racks (b) increase in IP traffic between optical transceivers.

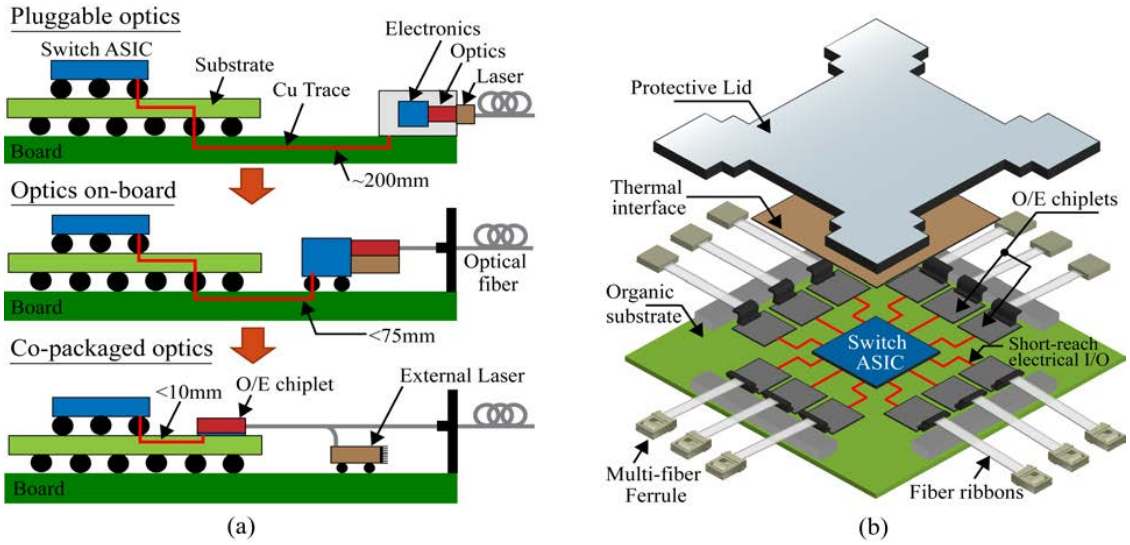


Figure 2.2: (a) Evolution of optical I/O technology in the data centers. (b) Switch ASIC co-packaged with optics using dense short-reach electrical I/Os.

and photodetectors using microring resonators (MRR). As the MRR have small foorprint and thus, have small parasitics they exhibit excellent energy-efficiency [23, 24]. Thus, the (SiPh) optical I/Os using microring resonators (MRR) are well suited for co-packaged optics of Fig. 2.2(b).

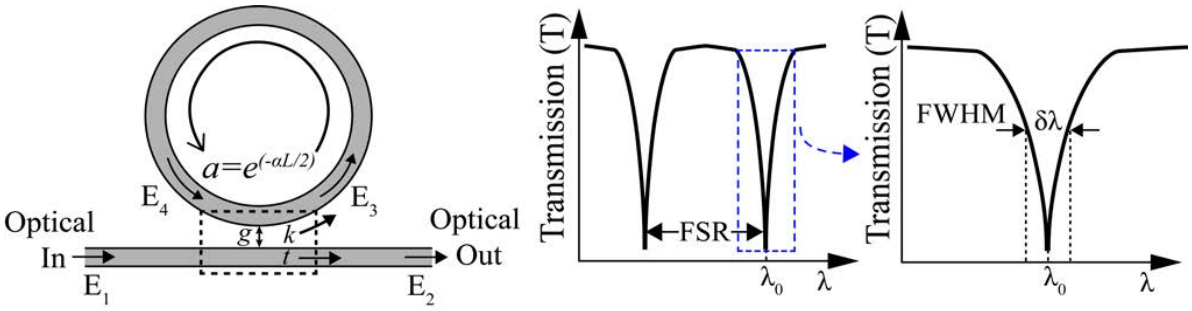


Figure 2.3: Microring resonator (MRR) structure, characteristics, and transfer function.

2.1 Microring resonators (MRR)

To better appreciate the operation of MRR-based SiPh links, first, the structure and characteristics of a microring resonator (MRR) are clarified. A typical MRR consists of a horizontal bus waveguide and circular or a ring waveguide are evanescently coupled with a coupling space g, as illustrated in Fig. 2.3. The coupling (k) and transmission (t) coefficients dictate the amount of optical power coupled into the ring and transmitted into the bus waveguide, respectively. For a lossless coupling, $k^2 + t^2 = 1$.The input (E_1) and output (E_2) optical fields are related to the field in the circular waveguide (MRR cavity) by [25],

$$E_2 = tE_1 + ikE_4 \tag{2.1}$$
$$E_3 = tE_4 + ikE_1 \tag{2.2}$$

Further, the effect of light circulating inside the MRR cavity can be captured by round-trip phase shift θ and round-trip amplitude transmission factor a, and can be represented as,

$$E_2 = ae^{i\theta}E_3 \tag{2.3}$$

By solving (2.1)-(2.3), the ratio of output to input optical fields and the ratio of field in the MRR cavity to input optical field can be obtained by as [26],

$$\frac{E_2}{E_1} = \frac{t - ae^{-i\theta}}{1 - tae^{i\theta}} \cdot e^{i(\pi+\theta)} \text{ and } \frac{E_3}{E_1} = \frac{ak}{1 - tae^{i\theta}} \cdot e^{i(\pi+\theta)} \tag{2.4}$$

where,

a	roundtrip field amplitude transmission, $a = e^{-\alpha L/2}$
θ	roundtrip phase-shift of the ring waveguide (MRR cavity), $\theta=(2\pi/\lambda)\eta_{eff}L$
L	circumference of the MRR cavity
α	propagation loss in the MRR cavity
η_{eff}	effective refractive index of the MRR cavity
η_g	group refractive index, $\eta_g = \eta_{eff} - \lambda\frac{\partial\eta_{eff}}{\partial\lambda}$

The transmission intensity factor T, sketched in Fig. 2.3, and the stored intesity in the MRR cavity are given by the squared modulus of (2.4). They are expressed as,

$$T = \left|\frac{E_2}{E_1}\right|^2 = \frac{t^2 - 2tacos\theta + a^2}{1 - 2tacos\theta + t^2a^2} \text{ and } I = \left|\frac{E_3}{E_1}\right|^2 = \frac{a^2k^2}{1 - 2tacos\theta + t^2a^2} \tag{2.5}$$

Now, the wavelengths for which round-trip phase shift is integer multiple of 2π create constructive interference that resonates the MRR. This creates a notch in the transmission spectrum (Fig. 2.3), at the resonant wavelength, λ_0, which is written as,

$$\lambda_0 = \frac{\eta_{eff}L}{m} \text{ where, } m = 1, 2, 3, ... \tag{2.6}$$

The free spectral range (FSR) of the MRR is given by,

$$FSR = \frac{\lambda^2}{\eta_g L} \tag{2.7}$$

Assuming lossless coupler (α=0 and a=1) and resonance condition ($e^{-i\theta}$=1), the expression in (2.5) can be simplified to,

$$T = \left|\frac{t-a}{1-ta}\right|^2 \text{ and } I = \left|\frac{ak}{1-ta}\right|^2 \tag{2.8}$$

The value of T in (2.8) drops to 0 when t=a. This condition is referred as critical coupling. The Q-factor and the MRRs full-width half-maximum (FWHM) bandwidth ($\delta\lambda$) can be derived by assuming critical coupling and setting $I = I/2$ in (2.8) at resonance. The resulting expression of Q-factor and FWHM is [27],

$$\partial\lambda \approx \frac{\lambda^2\alpha}{\eta_g\pi}, Q = \frac{\lambda}{\partial\lambda} \approx \frac{\eta_g\pi}{\lambda\alpha} \tag{2.9}$$

The smaller value of $\partial\lambda$ in (2.9) indicates the sharpness of the resonance notch in Fig. 2.3. The ratio of the FSR to $\delta\lambda$ is referred as finesse ($\mathcal{F}$) of the MRR, which represents the number of round-trips (within a factor of 2π) made by light in the ring before its energy is reduced to 1/e of its initial value.

The equations derived above, particularly, (2.5)-(2.9) are used while designing MRR-based photonic blocks such as MRR-based detector in Chapter-3 and MRR-based phase modulator in Chapter-4.

2.2 MRR-based monolithic SiPh Optical links

A monolithic SiPh optical link can be realized using MRR as both modulators on the transmitter (Tx) side [28] and photodetector on the receiver (Rx) side [17]. A typical SiPh link

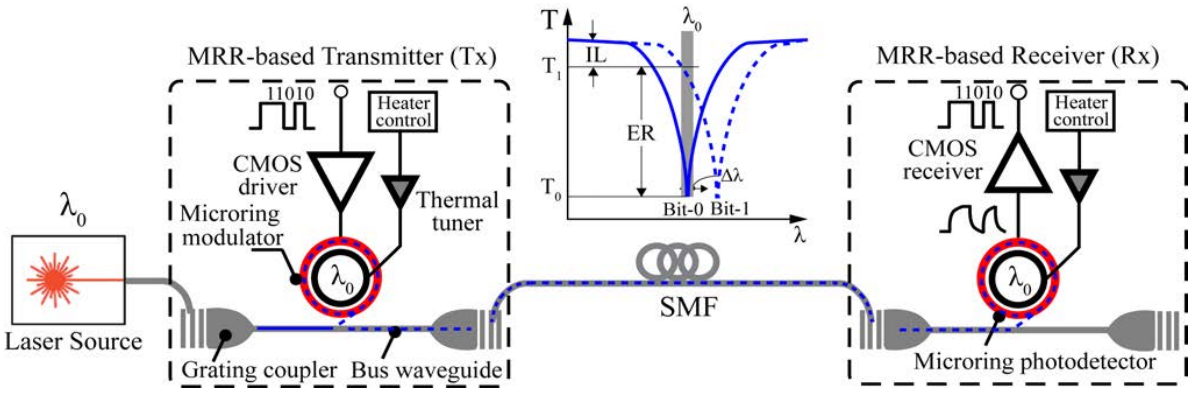


Figure 2.4: Microring resonator (MRR) based single channel SiPh link [30, 28].

is shown in Fig. 2.4. Here, the MRR-based modulator is realized by modulating an MRR's resonance wavelength, while a detector is realized by leveraging MRR's resonance. The construction of such a detector is discussed at length in Chapter-3. The strongest known effect that enables photonics block in silicon is that of carrier plasma dispersion effect induced by the free carrier absorption [29]. By injection or depleting carriers from the MRR cavity, the concentration can be changed which induces a linear change in the index of refraction, and thus, enables modulation of light. The modulator in Fig. 2.4 on Tx-sides switches between two resonances as depicted by the sketch of the transmission spectrum. While transmitting bit-0, the modulator is tuned to resonate at λ_0, whereas to transmit bit-1 it is shifted by $\Delta\lambda$. As a result, the through-port optical intensity modulates between T_0 and T_1. The ratio of the optical intensity between these two levels is defined as the extinction ratio (ER) while the difference is defined as optical modulation amplitude (OMA). The MRR modulator is initially biased at λ_0. At this point, there exists a finite insertion loss (IL), which can be minimized by moving bias point to the left. However, to achieve the same ER, a larger voltage drive is needed for a fixed change in $\Delta\lambda$ per volt. Thus, it is extremely desirable to have a large change in resonant wavelength i.e. large $\Delta\lambda$ for a small drive voltage. Unfortunately, $\Delta\lambda$ is limited by the concentration of the doping and the shape of P-N junction, which is not straight forward to change in a monolithic zero-change process. The IL, ER, MRR's bandwidth, and required drive voltage needed can be estimated from the Q-factor and resonance shift-efficiency $\Delta\lambda$/V (pm/V). Thus, they are the two popular figures-of-merits for the MRR modulators.

In Fig. 2.4, to align the MRR's resonance wavelength on Tx and Rx-side a closed-loop thermal tuning is implemented to lock the MRR to the target laser wavelength. This closed-loop tuning can calibrate for process variations and compensate for environmental and local thermal fluctuations. Thus, it is very critical for the stable operation of MRR-based modulators and detectors. Detailed implementation and measurement results of an Rx-side thermal tuning loop is discussed in Chapter-3, while a Tx-side thermal tuning loop is described in Chapter-4. Once stabilized, the MRR-based devices have less parasitic capacitance due to

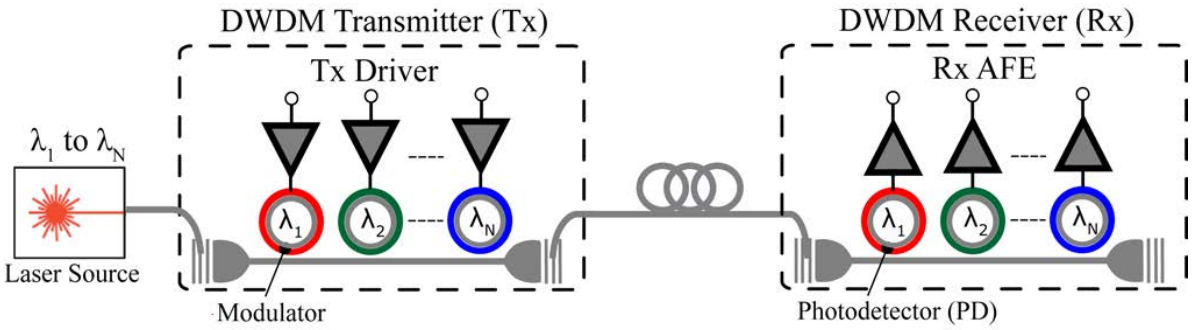


Figure 2.5: N-way DWDM SiPh optical link realized using MRR.

the small footprint. On the other hand, conventional optical Tx using Mach-Zehnder interferometer (MZI)-based modulators (MZM) are often millimeter-sized due to long phase shifters needed to achieve the required π shift. Consequently, such modulators are energy inefficiency, have bandwidth limited by RC, and are costly [24].

As the MRR-based devices are highly wavelength selective, they can readily realize a dense wavelength division multiplexed system simply by cascading them with a slightly different radius on a common bus waveguide. For example, Fig. 2.5 shows a bank of MRR-based modulators coupled to a common bus waveguide at the Tx-side, while at the Rx-side MRR-based detector sample the respective optical spectrum and extract transmitted bits. Similar to a single channel of Fig. 2.4, the MRR modulator, and detector operate in pairs that are responsive to optical power around a single carrier wavelength from λ_1 to λ_N. The number of channels N of a WDM link is determined by Q-factor and channel spacing between the two MRR as the FSR of each MRR is fixed. However, in practice, availability of low-cost stable N-way laser source and power handling capability of bus waveguide often limit the maximum value of N.

A major benefit of realizing a DWDM system with MRRs is that no additional components like an optical multiplexer or a de-multiplexer. This minimizes the insertion loss (IL) and saves the area. Whereas, as the MZI-based modulators are not wavelength selective, they need extra optical multiplexer at the Tx and demultiplexer at the Rx. These Mux/Demux also require thermal tuning, which consumes more power than the thermal tuning needed to stabilize MRRs [31]. Subsequently, the MRR-based DWDM solution is both area and power efficient.

2.3 Problem of high power consumed by the laser source

Owing to their small footprint, MRR-based modulator and detectors often exhibit much lower device parasitics. Consequently, monolithic SiPh links using MRR can provide high

bandwidth and improved energy-efficiency while reducing the overall system cost [30]. Besides, the MRR-based modulators and detectors are readily amenable to DWDM making MRR-based SiPh links a great possible solution for co-packaged optics of Fig. 2.2(b). However, the electrical power consumed by the laser source often dominates the overall link power budget and thus, becomes a bottleneck for further improving overall link energy-efficiency. The laser source must output enough optical power that would overcome the optical link path loss and limited Rx sensitivity while achieving the target BER. As the laser wall-plug efficiency is poor (<10%), the laser source consumes significant electrical power to deliver the minimum optical power required by the link. This problem is exacerbated at higher data-rates, as the Rx sensitivity degrades requiring a further increase in the input optical power.

To exemplify this problem, a conventional intensity modulation and direct detection (IMDD) link comprising of a laser source, a transmitter (Tx), and a direct detection receiver (Rx) are shown in Fig. 2.6. Assuming a perfect ER and the Rx electrical sensitivity of $75\mu A_{pp}$ [32], the minimum input power detectable at the Rx is 150 μW. Considering the link loses of 4 dB for fiber-to-chip coupling loss (α_C) and modulator insertion loss (α_{IL}) of 5 dB, the minimum laser power required by this link is 7.5 mW, which is 50 times higher than the power received at the Rx. A link margin of 2 dB combined with an uncooled laser wall-plug efficiency of 10 % makes the laser alone consume >0.12 W to operate a single optical channel. Besides, a typical laser source requires some form of thermal stabilization, which increases the electrical power consumption by another 3-4x. This is prohibitively high, especially for the co-packaged optics of Fig. 2.2(a)-(b) where an external multiport laser module is envisioned to power as many as 512 optical I/Os needed to meet throughput requirements of the next-generation switch ASICs [33].

As the laser source is off-chip, the optical path loss in Fig. 2.6 comprises at least three fiber-to-chip couplers making the coupling loss a notable factor. This loss is caused by the mode mismatch resulting from a discrepancy in core diameter between the laser carrying fiber (≈10 μm) and the on-chip waveguide (100's of nm). In practice, it is challenging to completely eliminate the coupling loss. It typically ranges from 2-4 dB [34, 35, 7]. In addition, depending on the type of modulator the insertion loss (IL) varies from 2-5 dB for MRR-based [36, 16], 4 dB for electro-absorption [35], and 5 dB for MZM-based [37]. The insertion loss trades-off with bandwidth and required driver voltage to achieve a certain ER. This makes it hard to minimize IL to arbitrarily low value. Also, in DWDM systems, additional non-negligible loss components such as the waveguide loss and the off-resonance ring losses amount to 3-4 dB extra loss in the Tx chip alone. In addition, limited Rx sensitivity also demands higher laser power. The Rx sensitivity can be improved by designing a low noise, and power-supply/common-mode noise-tolerant analog front end (AFE) [38, 39, 18]. However, most of the prior efforts have been for IMDD links that are spectrally inefficient as they use only one degree of freedom, namely, optical intensity. Thus, the IMDD links reported recently require 7-13 dBm of laser power [12, 36, 40].

Besides, compared to IMDD, the coherent links enable complex modulation, such as binary phase-shift keying (BPSK), and thus, are more spectrally efficient. However, due

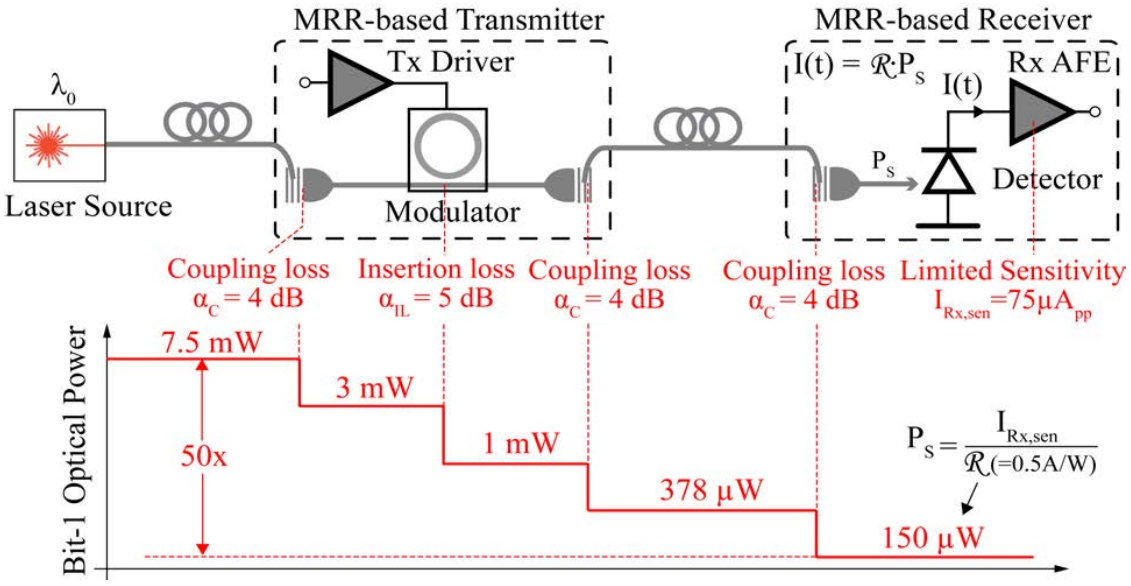


Figure 2.6: Conventional IMDD link with optical path loss.

to cost, complexity, and power-hungry signal processing, they are not suitable for data center applications and are limited to long-haul and metro links. As the short-reach I/Os of data centers have less severe fiber propagation impairments, the signal processing can be dramatically simplified to reduce the power consumption and cost [41]. While this new approach permits the use of coherent links in the data center, it still needs a local laser source. This is not feasible for high-bandwidth density applications, like optical I/O utilizing N-way DWDM, as it would require N independent local laser sources per I/O and many I/O ports.

These challenges are addressed in this thesis. A novel fully differential Rx is described in Chapter-3 which improves the Rx sensitivity while a laser-forwarded coherent link [19] is discussed in Chapter-4 which suppresses the optical link loss by averaging signal path loss with a low-loss laser-forwarded path.

2.4 Monolithic Silicon-Photonics platform in 45nm SOI CMOS

The SiPh links described in this thesis are integrated in a commercial CMOS 1P11M GFUS 45-nm SOI process [42]. All the necessary photonic blocks and transceiver circuits are realized in this platform resulting in a monolithic (single-chip) silicon-photonic solution.

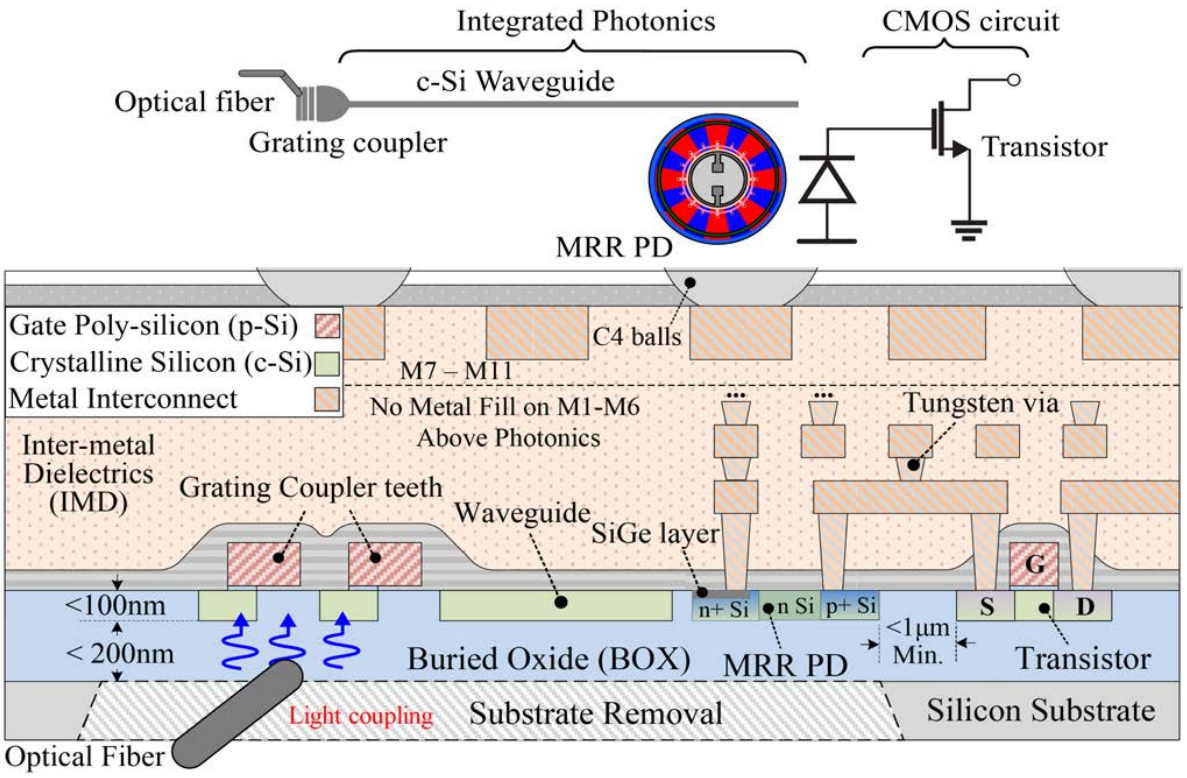


Figure 2.7: Cross section of 45-nm CMOS SOI process for monolithic (single-chip) silicon-photonics integration [28]. Figure is not drawn to scale.

2.4.1 Process cross-section

Fig. 2.7 portrays the cross-section of this platform. All the photonic devices in this platform are designed conforming the design rules and without modifying the native CMOS SOI process. As no extra processing steps or special handling is required by the foundry, the designs in this platform are submitted through standard commercial multi-project wafer services. Thus, high fabrication yield is ensured without incurring any process development costs. Recently, world's first photonic processor-memory link addressing bandwidth and power density issues is demonstrated in this platform [7], [28]. Nearly 70 million transistors and 850 photonic devices were monolithic-integrated demonstrating efficacy of this platform.

A simple SiPh/CMOS circuit where the light is coupled into the chip and guided to the photodetector connected to an NMOS transistor is shown in Fig. 2.7. The equivalent implementation in terms of the process cross-section is also shown, where an optical fiber couples into the chip from the back. The grating couplers divert the light into a waveguide formed using high-quality crystalline silicon (c-Si) layer sandwiched between the buried oxide layer (BOX) and the inter-metal dielectric (IMD). The light is then incident on the photodetector which is connected to the NMOS transistor with <10 μm spacing between them. Tradi-

tionally, the c-Si layer is patterned to form the body of a transistor, which is repurposed as a high-index waveguide core as it is surrounded by lower-index IMD and BOX layers. To confine light within the waveguide sufficient IMD thickness is achieved by blocking metal deposition above photonic blocks. However, the BOX dielectric under the waveguide has a fixed thickness of <200nm, which is insufficient for isolating the waveguide from the silicon substrate. This creates high optical loss due to evanescent leakage. An etching process, as outlined in sub-Section 2.4.3 below, is used to remove the substrate leaving air as the under-clad. As the refractive index of air is lower than that of the BOX, the light is confined in the c-Si waveguide reducing the optical loss to ≈3 dB/cm. Transistor performance is unaffected maintaining accuracy of device models, and existing foundry IP and timing libraries.

A full suite of photonic blocks is developed in this platform. Grating couplers are designed using c-Si and poly-silicon (p-Si) layers where the p-Si layer provides high-directivity and low-loss. The grating couplers used have 78nm bandwidth [43]. Active devices like resonant photodetectors and modulators use $5\mu m$ radius microrings with Q-factor of >10,000 [28]. The P-N spokes use the existing source/drain and well implant doping levels. Using these spokes along the perimeter of MRR, resonant detector with 0.55A/W [44] and a modulator with >20GHz bandwidth [45] are demonstrated. The usability of this platform is common between 1180nm to 1310nm, which recently is expanded till 1610nm to cover all the major telecommunication bands [46].

2.4.2 Advantages of monolithic silicon-photonics integration

Monolithic-integration of photonics and electronics in a conventional CMOS process achieves tighter integration and greatly simplifies packaging, verification, and testing. It specifically benefits the design of optical Rx as it reduces parasitic capacitance by removing the ESD capacitance, package parasitics, and bumps from the signal path. The reduced parasitic capacitance results in higher bandwidth at lower power and cost. For example, as shown in the Fig. 2.8(a), the primary noise contributor in a TIA are the thermal noise of the feedback resistor and the noise from the amplifier. The reduced C_T allows for the use of higher feedback resistance R_F for the same bandwidth. This helps to lower the thermal noise contribution from R_F. As shown in Fig. 2.8(b), for a bandwidth of 7 GHz, a C_T of 100 fF and 20 fF yields $R_{F,max}$ of 1 kΩ and 5 kΩ, respectively. In addition to the reduction in C_T, the 45 nm SOI CMOS process chosen for monolithic integration has one of the highest f_T among CMOS processes [16]. Higher f_T increases transimpedance limit enabling the use of even larger R_F, which reduces thermal noise, and suppresses input-referred contribution of residual offset and comparator minimum voltage. Reducing these noise sources is vital as they limit the sensitivity once the *FD* operation eliminates the data-driven PSN and common-mode noise.

Further, lower C_T and higher f_T also reduce the voltage noise of SF-TIA amplifier that scales with f^2. This voltage noise constitutes the flat part of the integrated noise in Fig. 2.8(c) that reduces from 1.1 μA for C_T of 100fF to 0.28 μA for C_T of 20fF. Lastly, realizing novel architectures of optical Rx, such as fully differential Rx described in Chapter-3, with-

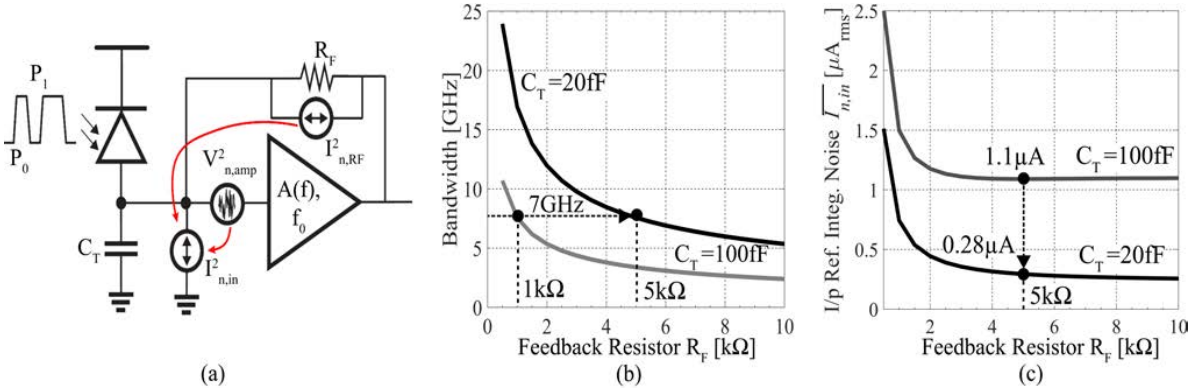


Figure 2.8: SF-TIA (a) noise contributors, (b) Bandwidth, and (c) Input-referred integrated noise

out any performance penalty can only be achieved in a monolithic integration platform. In alternate approaches where the CMOS and photonics are on two discrete chips [32, 47], a differential Rx would double the number of wirebonds or the flip-chip bumps. The resulting additional parasitic greatly reduces bandwidth, adversely affecting the input-referred noise. Besides, splitting the input laser source and coupling it into two discrete PDs further complicates assembly and packaging. Thus, the monolithic integration enables high-sensitivity optical Rx by lowering the input-referred noise and by functionalizing differential operation.

2.4.3 Post-processing Substrate release process

As argued in Section-2.4.1, the thickness of BOX being <200 nm causes light to leak into the substrate. To prevent this, the silicon substrate is removed with XeF2 dry etching. Figure 2.9(a) shows a picture of a test-chip flip-chip attached directly on the FR4 PCB. The total chip thickness is about 254 μm of which the silicon substrate is around 100 μm thick. For substrate thicker than >150 μm, die thining might be required to reduce overall processing time. Once the back substrate is cleaned with isopropyl alcohol and N2 air gun, the chip along with the board (Fig. 2.9(a)) is placed in the Xenon difluoride (XeF_2) gas chamber. The silicon substrate exposed to XeF_2 is isotropically etched, which stops at BOX as the etch process is highly selective between silicon and silicon dioxide (>500:1 Si:SiO_2). A pulsed-etch technique, in which etch steps of 120 secs were interleaved with 60 secs periods during which the by products of the reach like SiF_4 are purged. For a chamber pressure of 3.5 Torr, the substrate removal process takes about 1030 cycles on an average with a yield of around 80%. This method of substrate removal is used for both full and partial release of the silicon substrate.

Note that, the full substrate release through isotropic XeF_2 dry etch is only used to enable the testing of multiple IPs and standalone photonic test-sites. This process can be time-consuming and thus, hard to scale to larger volumes. This issue can be addressed as

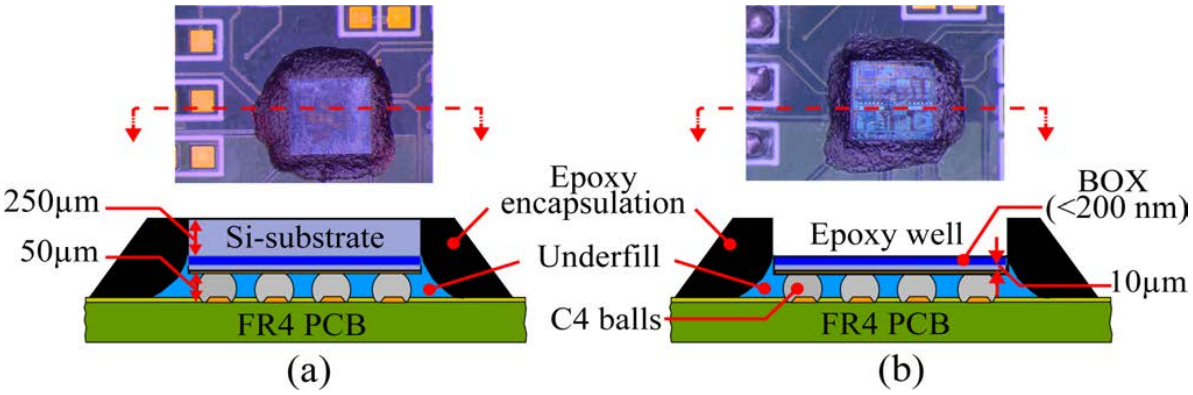


Figure 2.9: Chip-on-board (a) before and (b) after substrate release process.

follows. As only the substrate under the optical devices is required to be removed, a selective or partial substrate removal process can be performed. This is done by exposing only selected substrate to XeF_2 etch while covering the remaining with Kapton tapes or backend hard mask. Depending upon the silicon area, this process requires only 10 etch cycles instead of 30+ cycles required for full substrate release. This reduces the post-processing time by as much as 2/3. Besides, retaining the silicon substrate under CMOS circuits allows for better heat distribution and enables contact to a heat sink. Furthermore, a similar localized substrate removal (utilizing etch through the interconnect stack and localized Si trench) has already been commercially deployed in GlobalFoundries 90WG process, which is widely available and qualified for volume production. Thus, it is viable to apply selective substrate removal process at wafer-level as opposed to individual chip-level.

2.4.4 Substrate release and transfer process

For characterizing an individual photonic block, often a dedicated test-chip carrying test structure variants of a photonic block is taped-out. Such a test-chip provides access to individual photonic blocks using probe pads located at the top metal layer. As the test-chip is not flip-chip packaged before the substrate release, following steps are required to release the substrate, flip the chip, and transfer it onto another substrate to provide access to the top metal probe pads:

1. First the test-chip attached to the first glass substrate using a crystal bond. To do so, the glass substrate is placed on the hot plate set to ∼130°. A dab of crystal bond is applied to this glass substrate. The test-chip is then placed face-down on the crystal bond. It is ensured that the crystal bond at least covers the bottom 10 μm of the chip to prevent the active area (where devices are patterned) from getting etched.

2. Silicon substrate is etched using XeF_2 leaving the chip film in a well formed by hardened crystal bond. The chip at this point is as shown in Fig. 2.10 where the devices

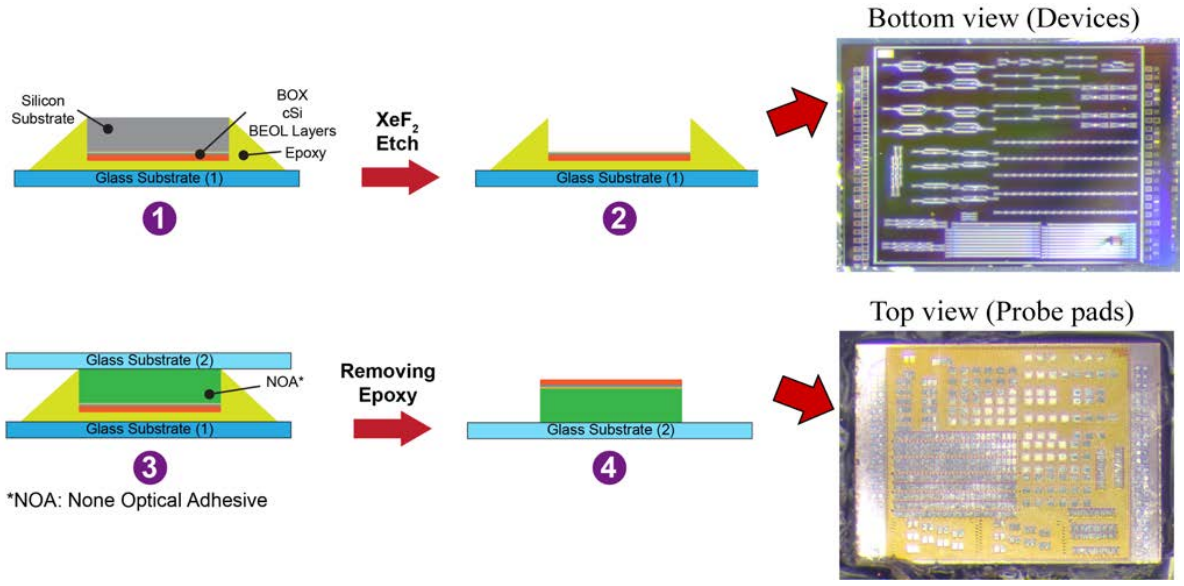


Figure 2.10: Steps to release silicon substrate and transfer the released chip onto another glass substrate.

implemented on the chip are clearly visible through the BOX.

3. A second glass substrate is attached using a nano-optical adhesive (NOA), which is cured by UV exposure.

4. The entire assembly is then flipped, and the first glass substrate is released by dissolving the crystal bond using acetone wash. Lastly, the chip surface is wiped using isopropyl alcohol. At this point, the chip from the top is as shown in Fig. 2.10 where the metal probe pads are now accessible.

These steps were primarily performed on the test-chip used to model and characterize the performance of MRR-based resonant photodetectors. These detectors enable high-sensitivity optical receivers described in Chapter-3 and balanced detector used in laser-forwarded coherent link discussed in Chapter-4.

Chapter 3

High-Sensitivity Differential Optical Receiver

As argued in Section-2.3 in Chapter-2, limited Rx sensitivity forces the laser source to output more optical power and thus, consume increased electrical power. Designing a high-sensitivity optical Rx is crucial of improving overall link energy-efficiency. To this end, a high-sensitivity, fully-differential optical Rx is discussed in this chapter. The optical Rx is targetted for high-density photonic interconnects co-packaged with high-performance SoCs such as that shown in Fig. 2.2 in Chapter-2. Such SoCs have are digital intensive in nature with high switching activity. This creates common-mode and power-supply noise, which degrades the optical Rx sensitivity. To suppress these noise sources and enhance Rx sensitivity, an optical Rx is proposed that realizes fully-differential operation by using implementing a differential photodetector. For this purpose, in the version-1 test-chip, a 3-dB power splitter and two linear SiGe photodetectors are used while in version-2 test-chip a new resonant splitmicroring photodetector is developed. The complete Rx circuits along with the differential detectors are implemented in a 45nm SOI CMOS with no process changes. Details of this process are discussed in Section-2.4 of Chapter-2.

The version-1 test-chips operate at 12 Gb/s with BER $<10^{-12}$ and input current sensitivity of 8.6 μA_{pp} while consuming 4.3mW. To understand the effectiveness of the proposed differential detector, performance of a conventional single-ended (SE) Rx on the same testchip is compared to that of the fully differential (FD) Rx. The measured sensitivity is >2x better than the closest state-of-the art design, achieving same energy per bit at higher data-rate. However, the linear detector had very poor responsivity, which limited the Rx OMA sensitivity of only -4 dBm. Besides, the 3 dB coupler had a big footprint and requires calibration as it was sensitive to wavelength of operation. This issues were addressed in the version-2 test-chip by using an MRR-based split photodetector. When aptly biased, this detector outputs fully differential photocurrent with $< \pm 0.3\%$ splitting error. It has 0.52 A/W responsivity and bandwidth of 5.0 GHz. The Rx circuit is optimized to achieve BER$<10^{-12}$ at 12 Gb/s with optical modulation amplitude (OMA) sensitivity of -18.2 dBm while consuming 7 mW. Compared to a conventional single-ended Rx on the same test-chip, the proposed Rx im-

proves sensitivity from 13 μA_{pp} to 7.9 μA_{pp} without reducing the bandwidth or significantly impacting the Rx energy-efficiency. Theoretical analysis along with various design tradeoffs, performance characterization, and limitations learned from measurement of version-1 and version-2 test-chip are discussed in this chapter.

3.1 Review of high-sensitivity optical Rx

In the applications such as co-packaging optics with high-performance SoCs (Fig. 2.2 in Chapter-2), isolation of optical I/O power-supplies from the noisy digital supplies presents a significant challenge. As a result, the optical Rx sensitivity can be adversely impacted depending on the integration environment. This significantly impacts the laser power requirements and the overall link efficiency and robustness. As the analog front-end (AFE) of a conventional optical Rx receives a single-ended (*SE*) input from the photodetector (PD), its performance is vulnerable to the power-supply and common-mode noise. In practice, these noise sources dominate the Rx sensitivity [39]. Traditionally, a voltage regulator such as an on-chip LDOs with a reasonable sized by-pass capacitor is used to lower the power-line impedance and suppress the power-supply noise. However, such a solution is most effective in low-frequency range to a moderately high-frequency range (<1 GHz). Maintaining a low power line impedance and good regulation at high-frequencies requires a substantial increase in power consumption and an increase in the area due to the larger by-pass capacitor needed [48]. While these power and area penalties may not be severe for a standalone discrete TIAs, they are unaffordable in an optical Rx designed for high-density low-energy optical I/Os co-packaged with SoCs like a switch ASIC as they are strictly area and power-constrained.

Subsequently, prior works have tried to improve the Rx sensitivity by synthesizing differential operation using some form of single-ended to differential conversion circuits. In [39], active sensing and cancellation of supply noise achieve -9.7 dBm sensitivity at 25 Gb/s. However, the overall energy-per-bit degrades due to extra circuits realized for sensing the common-mode and power supply noise, and circuits to apply a necessary correction. Supply noise to some extent can be suppressed by using dummy TIA with suppression limited by the device mismatch [48]. However, in [49] the dummy TIA is used in a feedback loop to make the Rx AFE more tolerant to power-supply noise. To realize a differential operation, in [50, 51], a PD is connected across the Rx input using AC coupling capacitors and large bias resistors. While this clever arrangement results in 2x larger swing at the input of Rx, it limits the use of the receiver to a specific PRBS pattern. For instance, the PRBS31 NRZ test pattern that has the lowest frequency component around 5.6 Hz (12 Gbss/2^{31}) in its spectrum. Using a series coupling capacitor would degrade BER by filtering the low-frequency content. Subsequently, in [50] a PRBS7 bit pattern is used to test the Rx. Besides, the increased area due to the integrated coupling capacitor reduces the bandwidth density of the O/E chiplet.

These issues are addressed by the proposed optical Rx discussed in this chapter. Here, a 12 Gb/s fully-differential (*FD*) optical Rx for DWDM systems with significantly im-

proved sensitivity compared to single-ended solutions is demonstrated in a monolithic silicon-photonic platform. The proposed idea of using a differential detector to suppress common-mode and supply noise is demonstrated through two versions of test-chips. In both of the test-chips, the Rx AFE sub-blocks, like a shunt-feedback TIA (SF-TIA) and a modified StrongARM comparator, are optimized for low input-referred noise. Lastly, the use of a monolithic silicon-photonic platform presents low parasitic capacitance at the Rx input enabling SF-TIA with high-transimpedance gain, which further improves sensitivity. The proposed Rxs in the two test-chips are fully compatible with commonly used equalization schemes [38, 23], which can be incorporated to further improve the sensitivity and data-rate.

3.2 Sensitivity of a conventional single-ended (SE) optical Rx

Figure 3.1 shows a typical single-ended (SE) optical Rx AFE that consists of an SF-TIA, a post-amplifier (G_P), and a comparator. The amplifier realizing SF-TIA has a finite gain of A and single dominant pole at f_a. The total capacitance C_T at the input of the Rx is the sum of the detector's capacitance C_{PD}, wiring parasitic C_p between the detector and SF-TIA, and the SF-TIA input capacitance C_{in}. As depicted in Fig. 3.1, the Rx sensitivity is impaired by (A) total input-referred thermal noise, $\overline{I_{n,in}}$, (B) Power-supply noise (PSN), ΔV_{PSN}, (C) residual offset voltage v_{off}, and (D) Minimum comparator resolution voltage. The total input-referred thermal noise $\overline{I_{n,in}}$ is obtained by integrating the input-referred noise PSD of (A.6) (see Appendix). It comprises of R_F thermal noise, the voltage noise of SF-TIA amplifier, and post amplifier. The PSN is commonly generated in three ways: 1) Noise coupled to Rx AFE analog supply from high-activity digital circuit 2) data-driven PSN due to single-ended PD input current [48, 47] and 3) data-driven transients coupling to the supply through circuit parasitics [52]. The last two means are aggravated in a DWDM system where multiple Rxs switch simultaneously. Furthermore, the input offset voltage can significantly deteriorate Rx sensitivity, mandating some form of offset correction. The limited resolution of offset correction circuit results in residual offset v_{off}. Lastly, the Rx sensitivity is also affected by the comparator minimum resolution voltage, which is mainly dictated by the comparator's minimum overdrive voltage v_{min} and the input-referred noise $\overline{v_{nc}}$. Using a dual-data rate (DDR) Rx topology gives the comparator extra regeneration time, which considerably reduces v_{min}. This causes $\overline{v_{nc}}$ to dominate the minimum resolution voltage.

As shown in Fig. 3.1, a single-ended PD with responsivity $\mathcal{R}$ converts the incident optical power P_{inc} to input peak-to-peak current $I_{in,pp}$ ($= \mathcal{R} \cdot P_{inc}$). The Rx sensitivity in terms of input modulation current, $I_{sen,pp}$, is the minimum $I_{in,pp}$ required to achieve a target BER. In the presence of only the thermal noise, it is given by,

$$I_{sen,pp} = 2\mathcal{Q} \cdot \sqrt{\overline{I_{n,in}^2} + \left(\frac{\overline{v_{nc}}}{Z_T \cdot G_p}\right)^2} \tag{3.1}$$

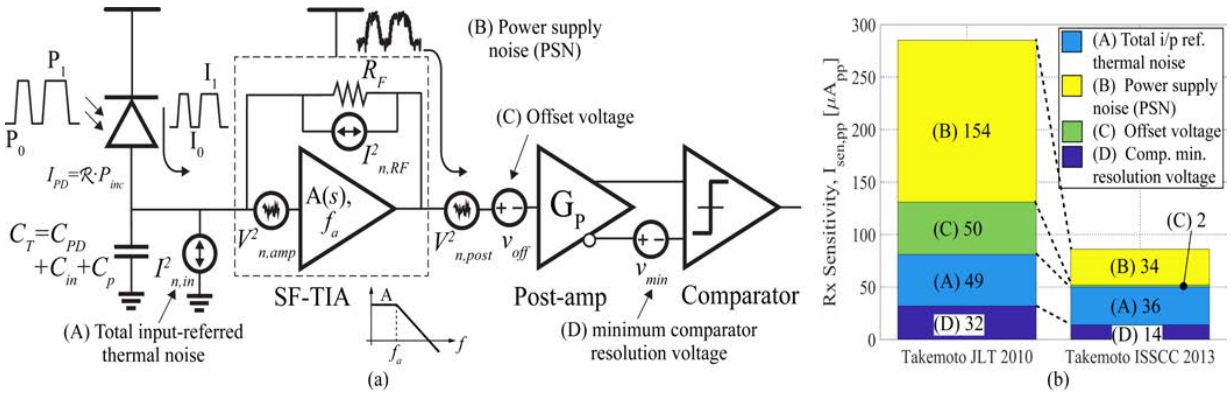


Figure 3.1: (a) Structure of a conventional single-ended *(SE)* optical receiver (Rx). (b) Breakdown of various sensitivity components as reported in [53, 54].

where a $\mathcal{Q}$ of 7 is required for BER $<10^{-12}$ [55]. Considering additional impairment sources the Rx sensitivity from (3.1) increases to [39],

$$I'_{sen,pp} = I_{sen,pp} + I_{PSN} + I_{min} + I_{off} \tag{3.2}$$

$$= 2\mathcal{Q}\sqrt{\overline{I^2_{n,in}} + \left(\frac{v_{nc}}{Z_T \cdot G_p}\right)^2} + 2\left(\underbrace{\frac{\Delta V_{PSN}}{Z_T \cdot G_P}}_{I_{PSN}} + \underbrace{\frac{v_{min}}{Z_T \cdot G_P}}_{I_{min}} + \underbrace{\frac{v_{off}}{Z_T}}_{I_{off}}\right) \tag{3.3}$$

where Z_T is the total transimpedance of the SF-TIA given by (A.1), and ΔV_{PSN} is referred to the output of the post-amplifier. Figure 3.2 intuitively illustrates (3.3). As shown in Fig. 3.2(a), with thermal noise alone, the $I_{in,pp}$ should be greater than or equal to $I_{sen,pp}$ for the Rx to correctly identify received bits. When the Rx decision threshold I_D is between I_0 and I_1 ((I_0 + I_1) /2), an optimum BER is achieved. However, in Fig. 3.2(b), the presence of additional impairments (B+C+D), shift I_D to I'_D (= I_D + I_{PSN} + I_{off}). This significantly degrades the BER. For a given Rx threshold I_D, this incorrect identification of received bits is expressed as,

$$BER = \frac{1}{2} \cdot [P(0/1) + P(1/0)]$$

$$= \frac{1}{4} \cdot \left[erfc\left(\frac{I_1 - I_D}{\sqrt{2}\sigma_n}\right) + erfc\left(\frac{I_D - I_0}{\sqrt{2}\sigma_n}\right)\right] \tag{3.4}$$

Here, it's assumed that 1s and 0s are equally likely i.e. $P(1)$=$P(0)$=0.5, and the variance in current I_1 for bit-1 and I_0 for bit-0 is equal to σ_n. $P(0/1)$ ($P(1/0)$) represent conditional probability of receiving 0 (1) for 1 (0). The *erfc* is the complementary error function. Thus, in the presence of only thermal noise, $I_{sen,pp}$ should be large enough to overcome $2\mathcal{Q} \cdot \overline{i_{n,in}}$.

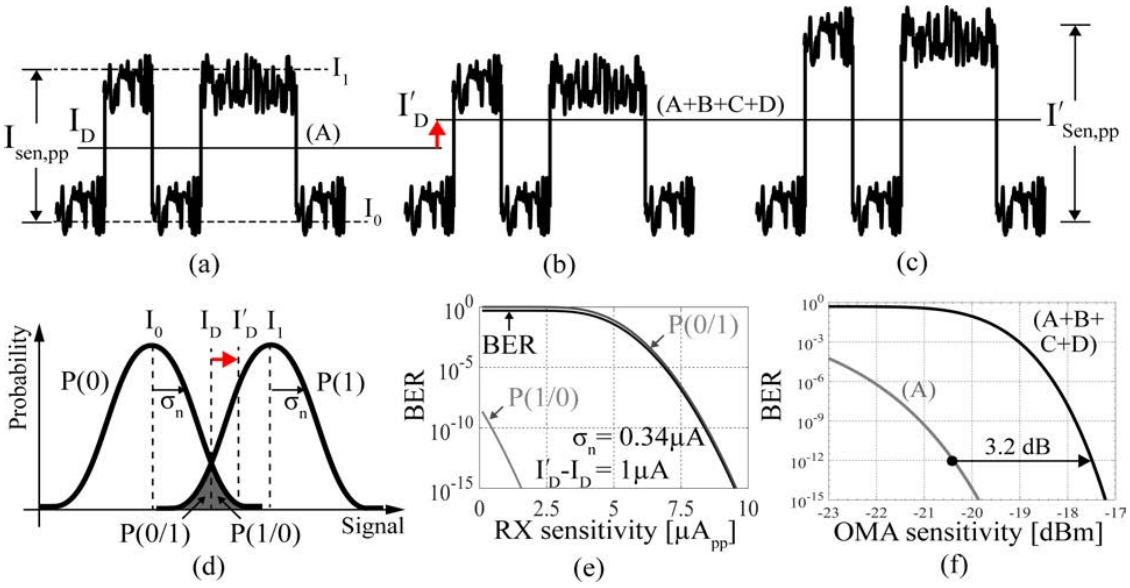


Figure 3.2: NRZ signal (a) with only thermal noise, (b) with all noise sources, and (c) increase sensitivity to recover BER. (d) Gaussian noise statistics. (e) BER and transition error probabilities. (f) Effect of all noise sources on BER. Here, $\overline{i_{n,in}} = 0.325\mu\text{A}_{\text{rms}}$, $i_{PSN} = 2\ \mu$A, $i_{off} = 0.1\ \mu$A, and $i_{min} = 0.1\mu$A.

The BER expression in (3.4) indicate that it has a minimum value of $d(BER)/dI_D = 0$, which yields the optimum value of $I_D = (I_0 + I_1)/2$. For fixed $\mathcal{R}$, the minimum optical power should be atleast $I_D/\mathcal{R}$. The presence of data-driven PSN (B), offset (C), and v_{min} (D) disturbs optimum balance by shifting I_D. As shown in Fig. 3.2(b), say I_D shifts upwards to I'_D. Even a minuscule noise in bit-1 will drop below I'_D causing many bit-1 to be misinterpreted as bit-0. Thus, significantly increasing the BER. To recover the BER, input current signal swing should be increased till I'_D again is the average of bit-1 and bit-0 level. This equivalently means degrading Rx sensitivity to a new increased value of $I'_{sen,pp}$. Also the minimum optical power is now increased to atleast $I'_D/\mathcal{R}$, which degradets the overall link energy-efficiency.

By using (3.2) in (3.4), the BER and I'_D can be related as [47],

$$BER = \frac{1}{4} \cdot \left[erfc\left(\frac{I_{in,pp} - 2 \cdot (I_{PSN} + I_{off} + I_{min})}{2\sqrt{2}\sigma_n} \right) + erfc\left(\frac{I_{in,pp} + 2 \cdot (I_{PSN} + I_{off} + I_{min})}{2\sqrt{2}\sigma_n} \right) \right] \tag{3.5}$$

To recover the BER, as shown in Fig. 3.2(c), the input current signal swing should be increased until I'_D is again set to the average of I_1 and I_0. Equivalently it means increasing Rx current sensitivity to $I'_{sen,pp}$, which is expressed by (3.3).

Alternatively, this effect can be understood by using Gaussian noise statistics sketched in Fig. 3.2(d), and BER and transition probabilities of Fig. 3.2(e)-(f). The probability of

error is equal to the area under the tails of the two Gaussian curves, in Fig. 3.2(d), that extends beyond the receiver's decision threshold I_D. The two key parameters that govern BER are: (1) Bit-1 and Bit-0 noise variance ${\sigma_n}^2$ and (2) difference between I_1 and I_0. As I_D shifts to I'_D due to additional noise sources (B+C+D), $P(0/1)$ great improves while $P(1/0)$ degrades equally, which limits the BER as shown in Fig. 3.2(e). The simulated values of various noise sources over bandwidth of 100 kHz to 10 GHz are:$A = 0.325\ \mu\text{A}_{\text{rms}}$, $B = 2\ \mu$A, $C = 0.1\ \mu$A, $D = 0.1\ \mu$A. Using these values in (3.5), the Rx sensitivity degrades atleast by 3.2 dB as evident from Fig. 3.2(f). 3dB. Consequently, the transmit power should be increased by 3.2 dB, leading to more than 50% increase in laser power consumption.

3.3 Noise Analysis of a Shunt-feedback (SF) TIA

The SF-TIA in Fig. 3.1(a) is realized with amplifier having a finite gain A and single dominant pole f_a. The input pole, $1/(R_F C_T)$ together with the amplifier's dominant pole creates a second order system whose closed-loop transimpedance is given by,

$$Z_T(s) = -\frac{A \cdot R_F}{(A+1)} \cdot \frac{1}{1 + s/(Q\omega_0) + s^2/\omega_0^2} \tag{A.1}$$

where,

$$\omega_0 = \sqrt{\frac{2\pi(A+1)\cdot f_a}{R_F C_T}} \text{ and } Q = \frac{\sqrt{2\pi f_a \cdot (A+1)\cdot R_F C_T}}{2\pi f_a \cdot (R_F C_T + 1)} \tag{A.2}$$

For $Q \leq 1/\sqrt{2}$, undesired peaking in the closed-loop frequency response is avoided and a flat frequency (Butterworth response) is ensured with <4.3% ringing in time-domain [55]. The closed-loop bandwidth for a Butterworth response is,

$$f_{3dB} = \frac{1}{2\pi} \cdot \frac{\sqrt{2A(A+1)}}{R_F C_T} \sim \frac{1}{2\pi} \cdot \frac{\sqrt{2}A}{R_F C_T} \tag{A.3}$$

This bandwidth limits the maximum feedback resistor $R_{F,max}$ that can be used by SF-TIA, which is given by,

$$R_{F,max} \leq A \cdot f_a/(2\pi \cdot C_T \cdot f_{3dB}^2) \approx \beta f_T/(2\pi \cdot C_T \cdot f_{3dB}^2) \tag{A.4}$$

Here, β relates the gain-bandwidth $A{\cdot}f_a$, as a fraction of f_T.

Further, the SF-TIA input-referred noise density in Fig. 3.1 is the sum of noise from R_F, amplifier current noise ${I^2}_{n,amp}$, and the input-referred noise of post-amplifier ${V^2}_{n,post}$,

$$\begin{aligned} I_{n,in}^2 &= I_{n,RF}^2(s) + I_{n,amp}^2(s) + V_{n,post}^2/|Z_T(s)|^2 \\ &= \frac{4kT}{R_F} + \frac{4kT\gamma}{g_m R_F^2} \cdot |1 + sR_F C_T|^2 + \frac{4kT\gamma}{g_{m,post} \cdot |Z_T(s)|^2} \end{aligned} \tag{A.5}$$

where, for Butterworth response (A.1) simplifies to, $|Z_T(s)| \approx |1/(1+s^2/(2\pi f_{3dB})^2)|$.

$$I_{n,in}^2(f) = \frac{4kT}{R_F} + \frac{4kT\gamma}{g_m R_F^2} + \frac{4kT\gamma}{g_m} \cdot (2\pi C_T)^2 f^2 + \frac{4kT\gamma}{g_{m,post} R_F^2} + \frac{4kT\gamma}{g_{m,post} R_F^2} \cdot \left(\frac{f}{f_{3dB}}\right)^4 \tag{A.6}$$

For large R_F, the terms in (A.6) with $R^2{}_F$ in denominator can be ignored. The third term in (A.6) shows amplifier noise, which is minimized when $C_{in} = C_{PD} + C_p$ [55]. This simplifies g_m of TIA as, $g_m = 2\pi f_T C_{in} = \pi f_T (C_T/2)$. Replacing g_m and R_F from (A.4), (A.6) simplifies to,

$$\begin{aligned} I_{n,in}^2(f) &= \frac{8kT \cdot \pi C_T f_{3dB}^2}{\beta f_T} + 16kT\gamma \cdot \pi C_T \cdot \frac{f^2}{f_T} \\ &= 8kT\pi \cdot \left(\frac{C_T}{f_T}\right) \cdot \left(\frac{f_{3dB}^2}{\beta} + 2\gamma f^2\right) \end{aligned} \tag{A.7}$$

3.4 Proposed fully differential (FD) optical Rx

The sensitivity of the proposed *FD* Rx is achieved by reducing all four impairment sources shown in Fig. 3.1. The thermal noise component is reduced by optimizing the designs of the SF-TIA and post-amplifier. A modified StrongARM comparator is used that has longer integration time and thus, lower input-referred noise. The input offset is canceled using conventional current DACs while the differential operation enabled by split-MRR based PDs suppress the PSN and common-mode noise components.

A conventional *SE* Rx is shown in Fig. 3.3(a). The detector is reverse biased by ensuring the bias voltage V_{PD1} is higher than the sum of the diode built-in potential and the main TIA input common-mode V_{CM}. Consequently, it generates a single-ended current in response to an incident optical power. The effect of resulting PSN is reduced using a dummy TIA, which not only consumes additional power but also degrades Rx sensitivity by increasing the noise power. A dummy capacitor, C_{Dummy}, is added to match the parasitic capacitance C_{T1} at the input of the main amplifier. Here, δC is a small mismatch between C_{T1} and C_{Dummy} due to the difference in the type of capacitors. This along with process mismatch makes the Rx AFE asymmetric and mismatches the bandwidth of main and dummy signal path. As a result, the PSN on AV_{DD} appears differently at nodes (1a) and (1b), which is then amplified by the differential gain of the post-amplifier. The main TIA, and the post-amplifier that converts the single-ended input to the differential, pulls a single-ended data-driven current given by,

$$I_{TIA1} = -\frac{R_{F1} \cdot I_{PD}}{r_{o1} || r_{o2}} \text{ and } I_{GP1} = \frac{Z_T \cdot I_{PD}}{2R_{Tail}} \tag{3.6}$$

where r_{o1} and r_{o2} are the output impedance of M_1 and M_2 in Fig. 3.3(b), respectively, and R_{Tail} is the output impedance of the tail current source that biases the input differential

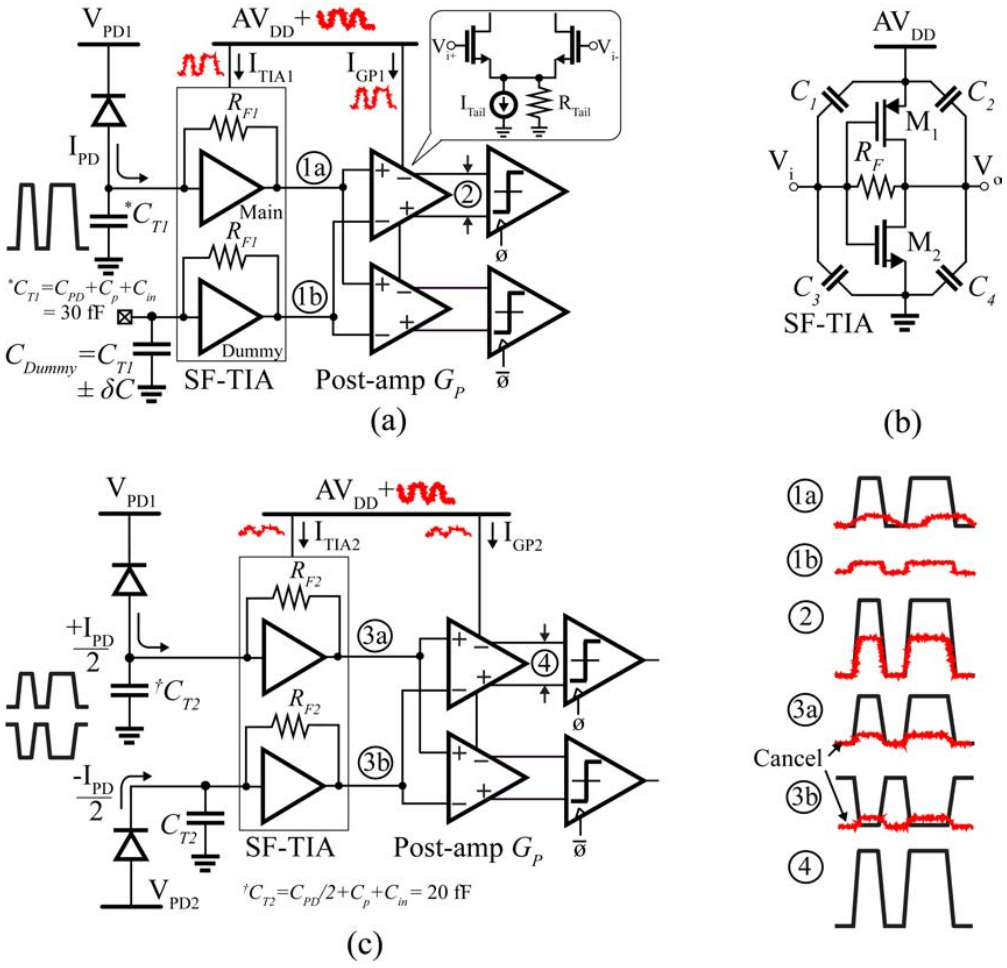


Figure 3.3: (a) Conventional *SE* Rx using a dummy TIA, (b) Capacitance at input/output of SF-TIA (c) Structure of the proposed *FD* DDR Rx.

pair of G_P. The data-driven single-ended current of (3.6), combined with the data-driven transients that couple to the supply-rails through parasitics C_1 - C_4 in Fig. 3.3(b), contributes to supply-variations and thus to the total PSN of ΔV_{PSN} at the output of the post-amplifier. As per (3.3), this affects Rx sensitivity.

Figure 3.3(c) shows the structure of the proposed *FD* DDR Rx where the conventional single-ended PD is split into two and biased with V_{PD1} and V_{PD2} of opposing polarity. By choosing $V_{PD1} = (|V_{PD}| + V_{CM})$ and $V_{PD2} = -(|V_{PD}| - V_{CM})$, the two PD's are biased with an equal reverse bias of V_{PD} while accommodating the TIA's input common-mode. This ensures generation of output signal currents that are equal in magnitude but 180° out of phase and enables a fully balanced Rx AFE with both TIAs driving the post-amplifier differentially. As a result, PSN on AV_{DD} appears identically on ③a and ③b, which is then canceled by the post-amplifier. Due to the differential operation, the current drawn from

Table 3.1: Breakdown of Optical Rx sensitivity at 12 Gb/s (AFE BW of 7 GHz) with BER=10^{-12} for same power consumption

Parameter		**Unit**	***SE* Rx**	***FD* Rx**
Feedback Resistor R_F		kΩ	3.4	5
Input ref. thermal Noise $\overline{I_{n,in}}$ (A)		μA_{rms}	0.39	0.280
Power supply noise I_{PSN} (B)		μA	3.2	0.6
Residual offset v_{off} (C)		mV	0.5	0.5
Comparator minimum	$\overline{v_{nc}}$	mV	1.7	1.2
resolution voltage (D)	v_{min}	mV	0.8	0.8
Input current sensitivity $I_{sen,pp}$		μA_{pp}	12.2	5.5
OMA Sensitivity†		dBm	-16.3	-19.8
Laser power consumption ‡		mW	7.4	3.4

†For PD with $\mathcal{R}$ = 0.52 A/W ‡Chip-to-chip Optical link loss = 15 dB [28]

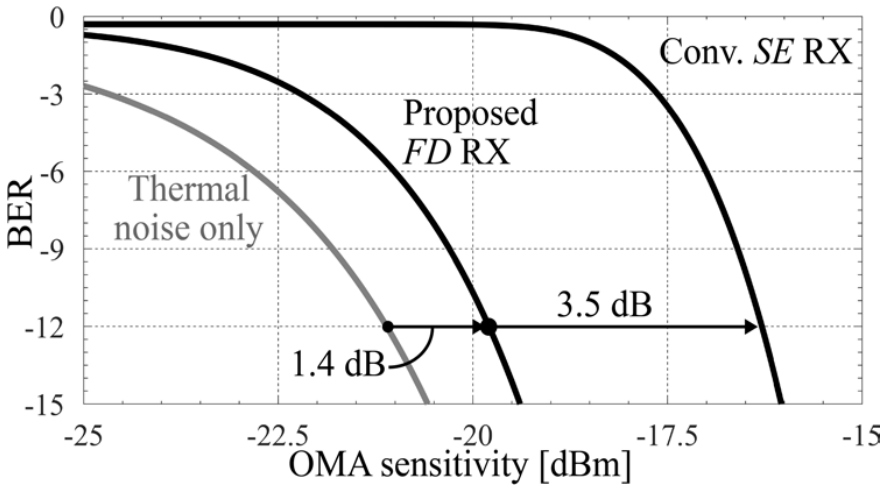


Figure 3.4: Effect of noise sources in Table. 3.1 on BER of *SE* and *FD* Rx.

AV_{DD} by the TIA (I_{TIA2}) and the post-amplifier (I_{GP2}) is fairly constant. This not only eliminates PSN but also eases the voltage regulator design. In addition, the data-driven transients are also canceled if the parasitic capacitance C_1-C_4 match well between the two TIAs. Lastly, the PSN coupling from AV_{DD} can be further rejected by ensuring the condition C_1 / $C_3 = C_2$ / C_4 [52].

Table-3.1 provides a breakdown of the *SE* and *FD* Rx sensitivity for same power consumption over a simulation bandwidth of 100kHz to 10GHz. The *SE* Rx is simulated with a conventional StrongARM comparator while the *FD* Rx uses a modified StrongARM comparator, discussed in Section-3.7, with improved noise performance. The values assumed in the simulation are Z_T = 74 dBΩ, $G_P = 4$, δC = 5fF, PSN on AV_{DD} of 50 mV at 7 GHz,

and AV_{DD} power-grid impedance of 10 Ω. Process variations and device mismatch are introduced using 50 Monte-Carlo simulation runs to get a true estimate of I_{PSN}, which under the ideal condition is fully eliminated by the *FD* Rx. The laser power consumption is calculated assuming a wall-plug efficiency (η) of 10% [56]. To realize the differential operation, splitting MRR to realize two PDs also halves the junction capacitance C_{PD}. Subsequently, the total input capacitance for *FD* Rx, C_{T2}, is smaller than *SE* Rx input capacitance, C_{T1}. In order to keep the AFE bandwidth same, the R_{F1} in *SE* Rx is reduced as outlined in Table-3.1.

Using these values, Fig. 3.2(d) compares the Rx OMA sensitivity of the conventional *SE* Rx of Fig. 3.1 under only thermal noise and a full set of impairments. The OMA sensitivity of *SE* Rx degrades by 3.5 dB due to the presence of additional impairments. This translates into 2.2x increases in the transmit laser power, which substantially degrades the total link energy-efficiency and limits the allowed link insertion loss. As shown in Fig. 3.4, the proposed *FD* Rx greatly suppresses PSN, and reduces $\overline{I_{n,in}}$ and v_{min} to improve sensitivity by 3.5 dB compared to *SE* Rx while having only 1.4 dB hit compared to thermal noise limit. Furthermore, as C_{T2} is smaller than C_{T1}, from (A.6), the input-referred noise greatly improves without consuming additional power. Simulation shows *FD* Rx reduces thermal noise by 28 %.

3.4.1 SNR comparison between the *SE* and *FD* Rx

As the optical power is split into half, it often raises a doubt that the signal swing at the output of *FD* Rx AFE is half that of the *SE* Rx. This is not correct. Instead, if designed aptly, the *FD* Rx can result in higher SNR. To understand this argument, consider a *SE* Rx as shown in Fig. 3.5(a). Here, a PD with responsivity, $\mathcal{R}$, converts the incident optical power, P_{in}, to I_{PD}. The total input-referred current noise is $\overline{I_{n1}}$. The main TIA amplifies both I_{PD} and $\overline{I_{n1}}$ generating V_1. The next amplifier stage takes the difference of V_1 and V_2 to generate V_{Out1}. The dummy TIA generates a reference voltage, V_{CM} that tracks the V_{CM} of the main TIA across PVT. Unfortunately, along with V_{CM} it also generates noise as given by the expression for V_2 in Fig. 3.5(a). Referring the noise component of V_{Out1} to the input reveals that the dummy TIA doubles the noise power and degrades Rx sensitivity by about 3 dB. Nevertheless, it is required to improve the immunity of *SE* TIA to power-supply variations. The resulting noise penalty from the dummy TIA can be reduced by loading it with a capacitor. However, this approach induces bandwidth mismatch between main and dummy paths resulting in severe degradation of high-frequency power-supply rejection [23]. Thus, even though dummy TIA consume extra power and degrades the Rx sensitivity, it is necessary to ensure robust operation of SE TIA.

Further, as shown in Fig. 3.5(b), the *FD* Rx circumvents this inefficient use of dummy TIA. Here, the input optical power is split between the two PDs. The differential biasing of the two PDs generates $+I_{PD}/2$ and $-I_{PD}/2$ current going into Main-1 and Main-2 amplifier, respectively. The differential output V_{Out2} contains only the differential signal component. Comparing V_{Out1} and V_{Out2}, it is clear that the proposed *FD* Rx approach does not lose half signal as the signal swing is exactly the same in both cases. However, it is still possible

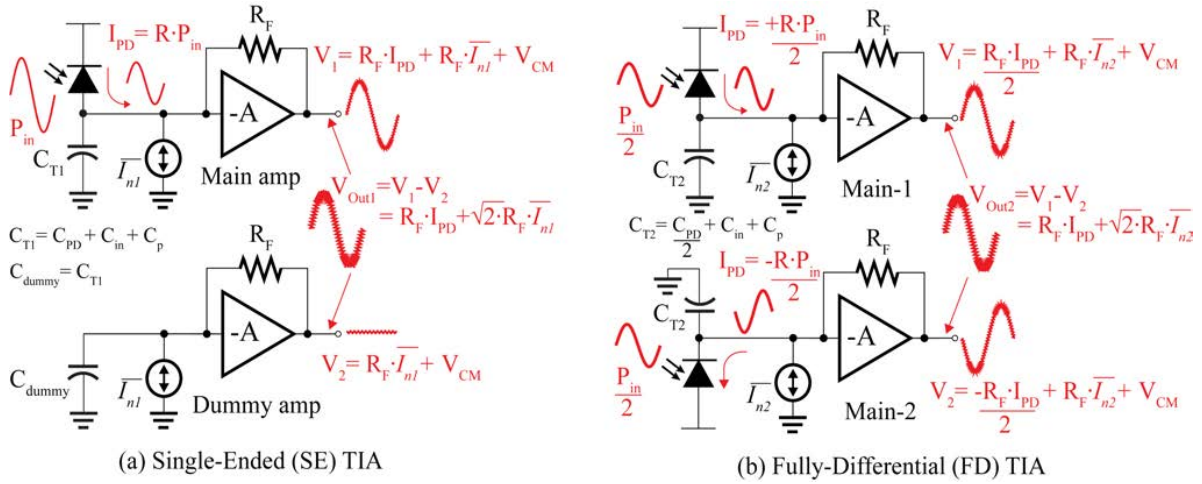


Figure 3.5: Signal swing at the output of: (a) a conventional *SE* TIA and a dummy TIA, and (b) TIA in proposed *FD* configuration.

that the SNR of *FD* Rx is higher than that of the *SE* Rx. Assuming both *SE* and *FD* Rx are realized in a monolithic platform, depending on the realization of differential detector C_{T2} is either equal or less than C_{T1}. As shown in the Section-3.3, if C_{T2} is less than C_{T1}, the amplifier noise contribution to the Rx sensitivity is lower for *FD* Rx. Thus, even though the thermal noise contribution from R_F is the same the overall input-referred noise for *FD* Rx is less. Another way to look at it is that for the same bandwidth, larger R_F can be used with *FD* Rx, decreasing the thermal noise contribution of the R_F resistor to the input-referred noise of the TIA. Consequently, the SNR at the output of *FD* TIA is better than that of *SE* TIA for the same power consumption.

3.4.2 Need for dual-supplies V_{PD1} and V_{PD2}

The differential detector requires two supplies, V_{PD1} and V_{PD2}, in contrast to a single supply used by a *SE* detector. For testing purposes, two discrete off-chip power supplies are used to reverse bias the differential PDs. These supplies are carefully filtered on the PCB. However, in future versions of test-chips, generating these supplies using integrated regulators should be reasonably plausible. The primary purpose of these supplies is to strongly reverse-bias the differential PDs. Under this condition, the PDs have very low dark current, which ensures high reverse impedance. This not only isolates the sensitive TIA input nodes from the V_{PD} supplies but also reduces the loading on the V_{PD} regulators relaxing the regulation requirement. Further, even under illumination, the load provided by the differential PDs is fairly high-impedance. This enables the use of switched capacitor based voltage regulators with a reasonable size of the flying capacitor. Appropriate design and layout choice of the unit cell can ensure V_{PD1} and V_{PD2} are well balanced and have almost identical spectrum.

Note that the need for two power supplies is not a fundamental requirement for biasing

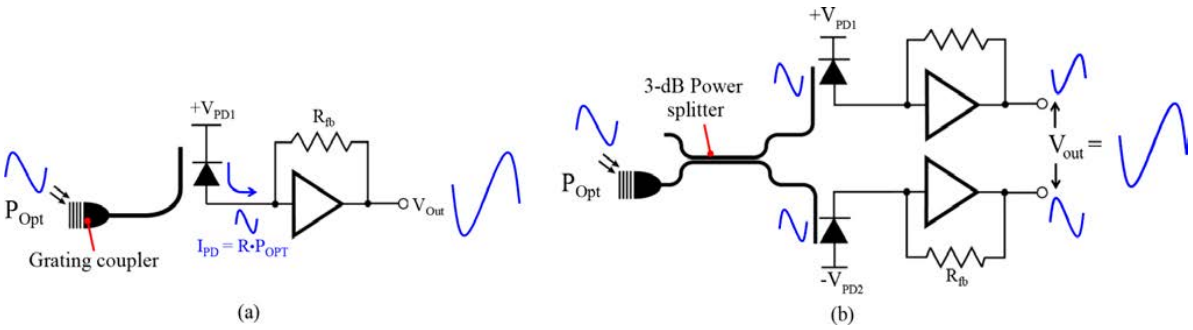


Figure 3.6: Optical and electrical signals in (a) a conventional *SE* Rx, and (b)*FD* Rx with a 3 dB coupler and differential linear detectors.

the differential detectors. This approach is chosen for the ease of testing and exploring the optical Rx performance limits without been bothered by the generation of power supplies. The only critical condition for the sound operation of the differential PDs is that their reverse bias voltage should be equal. As the input and output common-mode of the TIA, powered from AV_{DD} supply, is $AV_{DD}/2$, the extra PD supply can be eliminated by using $V_{PD1} = AV_{DD}$ and $V_{PD2} = 0V$. This generates equal reverse bias voltage of AVDD/2 across the two PDs, which ensures equal parasitic capacitance and responsivity. The diode built-in potential is around ∼0.6V. Hence, this approach requires AV_{DD} >1.2V. Also, a low reverse-bias (<1.0V) degrades the responsivity and increases the depletion junction capacitance which reduces the bandwidth. Nevertheless, the integrated detectors can be optimized to operate under low reverse-bias overcoming these limitations [57]. Hence, in the future, it is quite possible to use only one V_{PD} supply similar to that used in a *SE* Rx.

3.5 Version-1: Differential detector using a 3 dB coupler

A straight forward approach to realize a differential detector is to precede a linear detector with a 3-dB power splitter. In a conventional optical receiver of Fig. 3.6(a), the incident optical light is delivered as is to the photodetector which converts the optical power to the photocurrent. However, in an *FD* Rx the incident optical power is first split equally into the two waveguides that carry it to the linear detectors. This is exemplified in Fig. 3.6(b). The optical power hitting the two photodetectors is still in-phase. However, as the detectors are biased with opposing polarity, the photocurrent generated is equal in amplitude but 180° out of phase. Thus, the voltage swing at the output of the Rx AFE is fully differential. While this approach leads to a fully differential Rx AFE, it relies heavily on the successful implementation of a 3-dB power splitter. Implementing this approach on a discrete platform would double the amount of interconnects between the photonic and electronic chip, which leads to degradation in the input bandwidth. Hence, this approach is more suitable for a

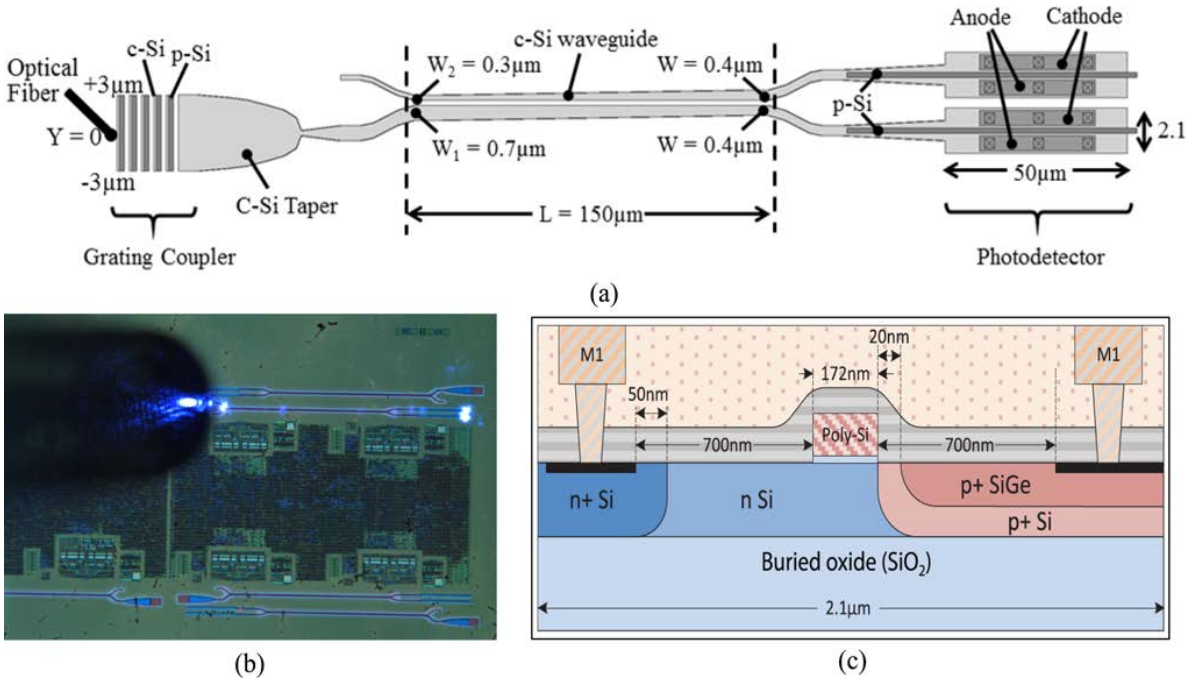


Figure 3.7: (a) Construction of differential detector using a 3 dB coupler and linear SiGe detectors (b) Micrograph of the Rx test-site showing coupling of light into a 3 dB coupler. (c) Structure of linear SiGe detector

monolithic platform where optical functionality, like the splitting of power, can be realized with no additional performance penalty.

The 3 dB coupler in Fig. 3.6(b) can be implemented using directional couplers or adiabatic couplers. These couplers rely on a basic premise that by bringing two optical waveguides close enough, the optical power from one waveguide is coupled into the other. While the directional couplers have a small footprint, it requires a very precise coupling length to achieve a 3 dB power split ratio. Also, the coupling length is very sensitive to wavelength and fabrication imperfections which not only makes it difficult to achieve the desired coupling ratio but also unfit for DWDM applications. This limitation arises because in a typical directional coupler both the fundamental even and odd mode of the structure is excited. These modes then interfere with each other resulting in the characteristic power oscillation between the two waveguides of the coupler. On the other hand, the adiabatic couplers excite only the fundamental mode and adiabatically converts the mode of a single waveguide into either the even or odd mode in the two waveguides that are separated by a small gap. The closer this gap is, the shorter is the length of the coupler over which the adiabatic transition occurs. Once the adiabatic transition is complete, the optical power is naturally split into 3 dB between the two arms. Thus, the adiabatic coupler does not require precise coupling length, as long as it is long enough.

Figure 3.7(a) shows the construction of the 3 dB adiabatic power splitter with a SiGe photodetector. The light is coupled into a grating coupler roughly at the coupling position, Y=0. Couplers are designed with c-Si and poly-silicon (p-Si) layers to achieve low-loss and high directivity. A c-Si taper directs optical modes into an adiabatic directional coupler which splits the optical power equally into two output waveguides. The 3 dB power split is achieved by slowly tapering the widths of the output waveguides, W_1 and W_2, such that the input fundamental mode is maintained until the tapered waveguide widths are equal. At this point, the waveguides are quickly separated resulting in equal optical power split in the two output waveguides. Finally, Fig. 3.7(b) shows a micrograph of one of the Rx test-sites. Here, light is coupled into 3 dB coupler and as shown in Fig. 3.7(b), is well confined within the crystalline silicon (c-Si) waveguide. To release the substrate the process steps as discussed in Section-2.4.3 of Chapter-2 are used. The germanium layer (Ge) used for strain engineer the PMOS transistor in the process is reused to form the p+ SiGe absorption layer (Fig. 3.7(c)) of the photodetector [58]. The silicon nitride layer provides additional tensile stress to boost the detectors quantum efficiency. At 1180nm, the PD has a responsivity of 0.023 A/W. Its device dimensions are a variant of the detector in [58] with slightly shifted geometries. The detector has poor responsivity as it absorption-length-limited. Its responsivity can be increased by increasing the length, but that would also increase the capacitance and reduce the detector's bandwidth [58].

3.6 Version-2: Split-Microring Resonant SiGe Photodetector

Along with improving sensitivity, it is equally desirable for the optical Rx to be amenable to DWDM. This can be enabled by using MRR-based photodetectors (MRR PD). An MRR, as shown in Fig. 2.3 in Chapter-2, is essentially an optical notch filter that passes all the wavelengths except the resonant wavelength λ_0, which can be tuned by the thermal tuner. To extend this single-lane link to an N-way DWDM, N MRRs with slightly offset resonant wavelengths can be coupled to the same waveguide or fiber achieving N times higher aggregate bandwidth per fiber as shown in Fig. 2.5 in Chapter-2.

In this section, design and characterization of MRR-based photodetector is discussed. Later, a differential detector is derived by modifying MRR-based PD. Such a detector is referred in the test as split-MRR PD. The design details and performance characterization of split-MRR PD are also discussed in this section.

3.6.1 Operation of the MRR-based photodetectors (MRR PD)

Although many forms of PD are known, in a monolithic silicon-photonic platform linear p-n or p-i-n PDs are most popular owing to their ease of integration. As the bandgap of silicon is 1.1eV, it is transparent down to wavelengths of around 1275nm (∼0.97eV) making photocurrent generation difficult. To alleviate this issue, the SiGe layer that enhances the

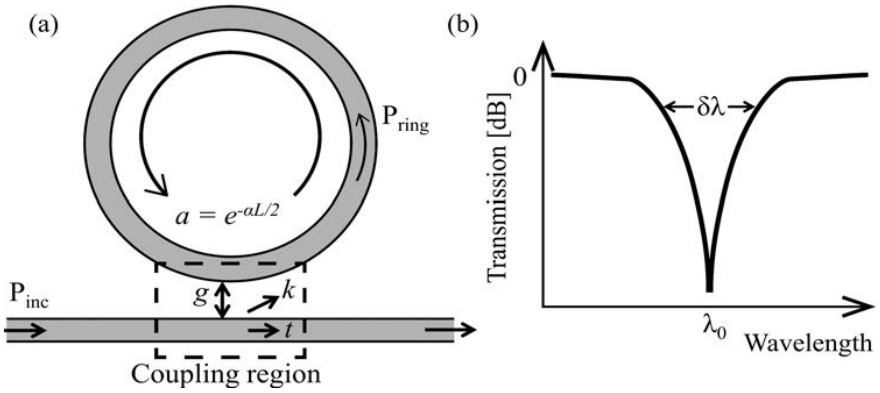


Figure 3.8: Basic MRR (a) topology and (b) transmission spectrum.

mobility of the PFET transistors is grown in drain silicon pockets to shrink the bandgap of silicon [44]. Combining the reduced bandgap with the trap-assisted recombination process through the defect states located in the bandgap, a PD can be realized in a silicon process. Unfortunately, as no change to the underlying CMOS process is made, the optical absorption is limited. For instance, a typical linear PD in the present monolithic platform, described in Section-2.4 of Chapter-2, absorbs <2.5 % of P_{inc} over the detector length L of 100 μm resulting in only 0.023 A/W responsivity at 1180 nm [58, 15]. The responsivity under the long-device limit is 0.2 A/W achieved by increasing the detector length, which increases parasitic capacitance and reduces the bandwidth. To enhance the limited responsivity of the linear PDs, the resonance in an MRR can be used. In Fig. 3.8(a) a basic MRR is evanescently coupled to a straight bus waveguide separated by coupling gap, g. The wavelengths for which round-trip phase shift is integer multiple of 2π create constructive interference that resonates the MRR. This creates a notch in the transmission spectrum (Fig. 3.8(b)), at the resonant wavelength, λ_0. The linewidth of the resonance is characterized by the full width at half maximum (FWHM), $\delta\lambda$, which depends upon round-trip optical loss and coupling strength. The coupling (k) and transmission (t) coefficients dictate the amount of optical power coupled into the ring and transmitted into the bus waveguide, respectively. For a lossless coupling, $k^2 + t^2 = 1$.

Owing to constructive interference with the input optical power at resonance, the power in the MRR is much higher than that in the bus waveguide. This optical power enhancement depends on the Q-factor of the ring. Under critical coupling (i.e. k^2=1-a^2) it is given by,

$$P_{ring} \approx \frac{P_{in}}{(1-a^2)} = \left(\frac{\lambda_0}{\eta_g L}\right)\frac{Q}{\pi} \cdot P_{in} \tag{3.7}$$

where Q=$\lambda_0/(\delta\lambda)$, η_g is the group index, and a is the round-trip amplitude transmission, which relates to propagation loss α by $e^{(-\alpha L/2)}$. The expression in (3.7) can be readily derived using (2.5)-(2.8) from Chapter-2. In the present monolithic platform, the optical power enhancement of (3.7) is between 25x to 35x ignoring the scattering loss. A PD implemented

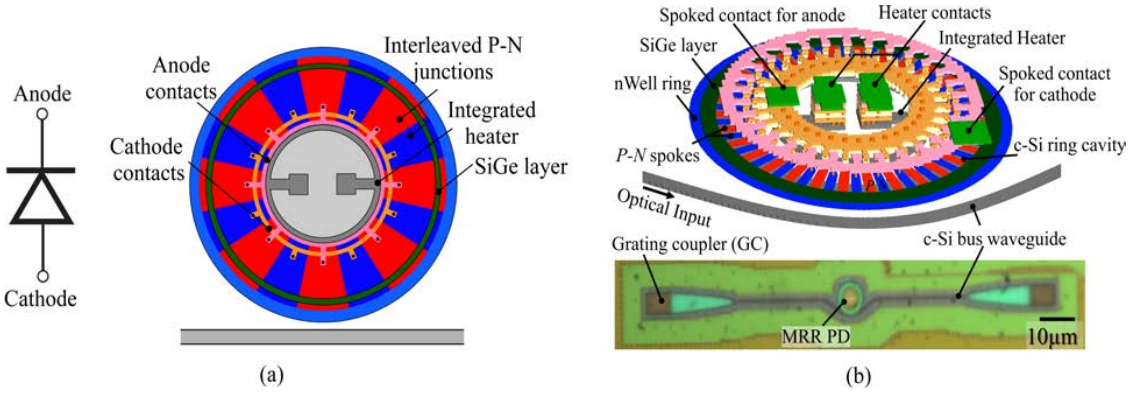


Figure 3.9: (a) Realizing a PD using an MRR (b) 3D layout of an MRR PD.

within such MRR cavity can have significantly higher responsitivity. As shown in Fig. 3.15, this is realized by placing interleaved *P-I-N* SiGe junctions along the MRR cavity yielding a remarkable boost in responsitivity in an extremely compact form factor [59, 44]. A typical MRR based PD has 0.55A/W responsivity with 5 μm radius resonant c-Si cavity [44], while the linear PDs are 50 μm long with only 0.023A/W responsivity [15].

3.6.2 Electrical and Optical Characterization of MRR PDs

To enable the design of an optical receiver a good electrical model of the MRR PD is required. This helps to co-simulation and optimize the Rx AFE for low-noise performance. An MRR PD is essentially a *P-N* diode that is modeled using a series resistance R_S, junction capacitance C_j, reverse resistance R_j, and a current source I_{PD} as shown in Fig. 3.10(a). The physical origin of these lumped components is represented by distributed r_s and c_j in Fig. 3.10(b). The junction capacitance c_j is the useful capacitance as the optical mode is converted to photocurrent in this region. However, the parasitic capacitance c_p between the two *P-N* spokes in Fig. 3.10(b) is not useful and reduces the bandwidth of the MRR PD. To minimize the parasitic capacitance one approach is to reduce the width of *P-N* spokes giving rise to a T-shape junction that is narrower towards the contact and wider at the junction where it matters [44]. Narrowing the spokes increases the series resistance which to some extent is mitigated by using an outer n-well ring shown in Fig. 3.9(b).

To extract the model parameters of Fig. 3.10(a) and characterize the MRR PD performance, a test-chip as shown in Fig. 3.11 is designed. The bottom view shows the chip looking through the BOX after substrate removal. Here, the flip-and-transfer process after substrate removal is used. To gain access to the probe pads on the front side of the chip, it is flipped and transferred to a glass carrier substrate. At this point, the chip appears as shown by the top-view. The processing steps are outlined in Section-2.4.4 of Chapter-2. The chip comprises of a total 104 test-sites with 24 variants of coupling gap, SiGe width, and 80 variants of ring radius forming 5 filter banks. The reported device was chosen as it shows

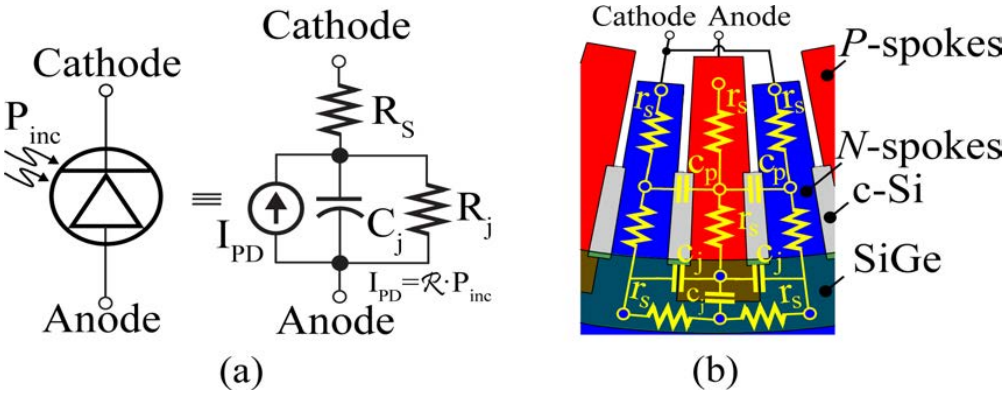


Figure 3.10: (a) Equivalent circuit model for an MRR PD and (b) distributed elements in a *P*-*N* spoke.

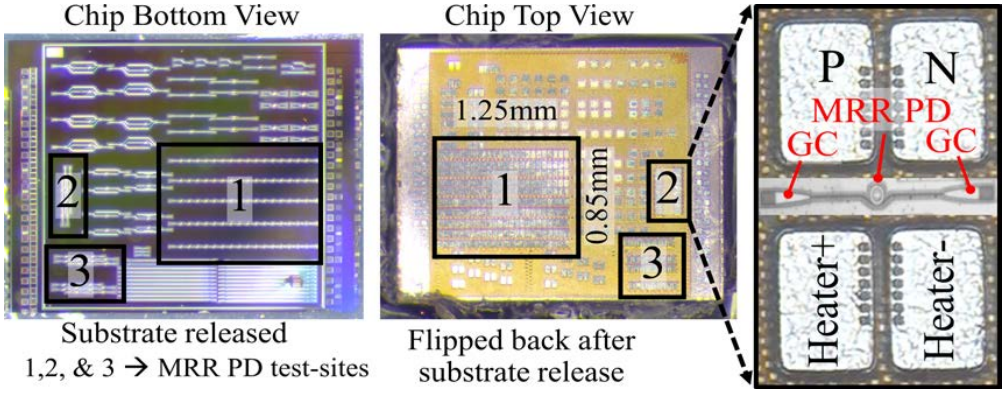


Figure 3.11: Micrograph of a test-chip used to model and characterize MRR PDs.

higher responsivity. A typical test-site consists of four-probe pads as shown in Fig. 3.11. For ease of testing, broadband (1170nm-1560nm) bi-directional couplers are used to couple light in and out of the test-sites.

Figure 3.12(a) shows the PDs I-V curve under dark and illumination conditions. Under the dark condition, the I-V curve is that of a typical diode with a built-in potential of 0.6 V. The reverse saturation current is flat and forward current grows exponential. For reverse bias of 0 to -8 V, the reverse current is in the order of nano-amps and the value of R_j is within 0.1 to 1 GΩ, which is mainly limited by the accuracy of the source meter. In the forward bias region, the series resistance R_S is measured to 150 Ω as in Fig. 3.12(b). At resonance and under illumination, the forward bias behavior of the PD is similar to that under dark condition. However, when reverse biased, the photocurrent does not plateau but rather continues to increase with a reverse bias voltage. At resonance, the light trapped in the MRR cavity generates carriers, which are swept out at a rate based on the strength of the field determined by the reverse bias voltage. This creates an increasing trend in

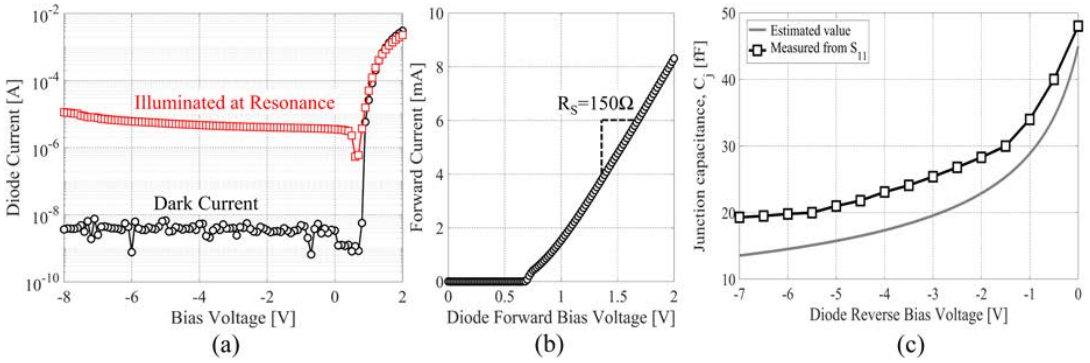


Figure 3.12: I-V plots of photodetector (a) log scale and (b) linear scale. (c) Junction capacitance with reverse bias.

photocurrent.

Further, to determine the junction capacitance C_j, the reflection coefficient S11 using a vector network analyzer (VNA) on a 50 Ω load. In order to accurately measure C_j, the VNA is first calibrated from 0.1 to 10 GHz and its reference plane is moved to the tip of the probes. The capacitance from the probe pad to ground is around 40fF and between the pads is 7 fF. These capacitance values are de-embedded by using on-chip open pad structures. The resulting S11 parameter is that of the MRR PD alone. The junction capacitance is then obtained by converting the S11 parameter to small-signal impedance. Figure 3.12(c) shows the expected decreasing trend in C_j with the reverse bias voltage. Alternately, the n-type and p-type doping concentrations are obtained from dedicated test-structures, which can be used to readily estimate Cj. While the shape of both plots matches, the difference between them can be attributed to the circular spoked anode and cathode routing parasitic (c_p in Fig. 3.10(b)) which are not de-embedded from Cj.

In [60], a strong electric field across P-N junction is created by increasing the reverse bias. This facilitates carrier tunneling which can greatly increase the absorption probability for sub-bandgap photons, and thus the responsivity. A similar experiment is repeated here with the reported MRR PD test-sites. Figure 3.13(a) shows the resulting improvement in responsivity. By increasing the reverse bias voltage to -7.5V the PD responsivity increases to 0.6 A/W. A reverse voltage of more than -8V causes a rapid increase in reverse current that eventually leads to junction breakdown. Hence, in Fig. 3.13(b) the MRR PD is characterized with -7V reverse bias. Figure 3.13(b) shows the optical transmission of the MRR PD with resonant wavelength at 1270nm. It is measured with a reverse bias of -7.0V. The MRR PD has an FWHM of 0.16nm (29.8 GHz) and a free spectral range (FSR) of 17nm (3.2 THz). Thus, the Q-factor is 7.9K.

After extracting the model parameters, another important aspect of MRR PD to characterize is its 3-dB bandwidth. As the test-chip in Fig. 3.11 does not carry test-structure to faithfully characterize S21 of the MRR PD, bandwidth estimated from the statistical eye

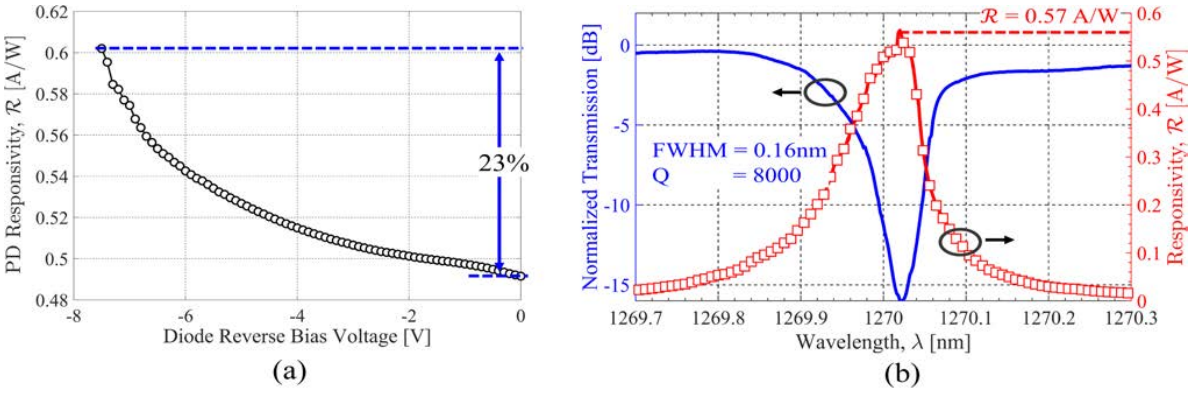


Figure 3.13: (a) Increase in responsivitiy with reverse bias and (b) optical transmission and responsivity with wavelength.

measurement and compared with prior measurement [44]. It was found that the bandwidth of MRR PD is limited to $\sim$ 5 GHz. The bandwidth of the MRR PD is governed by four time constants: 1) Cavity photon lifetime 2) RC time, 3) transit time, and 4) trap-induced carrier emission. The cavity photon lifetime, τ_{ph}, is the time needed for the light intensity to decay by a factor of $1/e$ due to various loss mechanisms. Under critical coupling, the estimated cavity photon lifetime limited bandwidth f_{ph} is around 31.4 GHz. It is given as,

$$f_{ph} = \frac{1}{2\pi\tau_{ph}} = \frac{c}{\lambda \cdot Q} \approx 31.4GHz \tag{3.8}$$

One important point to note from (3.8) is that the signal bandwidth of the MRR PD cannot exceed f_{ph}. For higher bandwidth, lower Q-factor is more desirable. Second, the RC-limited bandwidth for the MRR PD is 40 GHz (R_S=150 Ω, C_j = 20 fF). Third, the transit-time-limited bandwidth for MRR PD is $\sim$45 GHz assuming maximum depletion width of 0.98 μm and saturated carrier velocity of 10^5 m/s. Though the above three time-constants indicate a high-bandwidth response of MRR PD, the measured S21 bandwidth is limited to only 5 GHz [44]. The trap-induced carrier emission is likely the cause. The SiGe layer is believed to cause band discontinuity at the P-N junction interface where the carriers get trapped. These carriers are later slowly emitted creating a long tail in the time domain, and thus, reduces the bandwidth [61]. Applying a strong reverse bias lowers the barrier and alleviates this issue to some extent. The dependence of MRR PD bandwidth on reverse bias voltage is also observed during measurements [44].

Finally, Fig. 3.14(a) shows the design of the integrated heater used to thermally tune the MRR PD. The heater resistance is realized by placing a small c-Si ring within the MRR cavity. This is more preferable as the optical mode in the MRR cavity is more concentrated towards the outer perimeter of the cavity. Thus, the heater can be placed much closer to the MRR cavity improving the heating efficiency as the thermal resistance is greatly reduced. The mean value of the heater resistance (R_{Heat}) measured over 20 test sites from 2-chips is

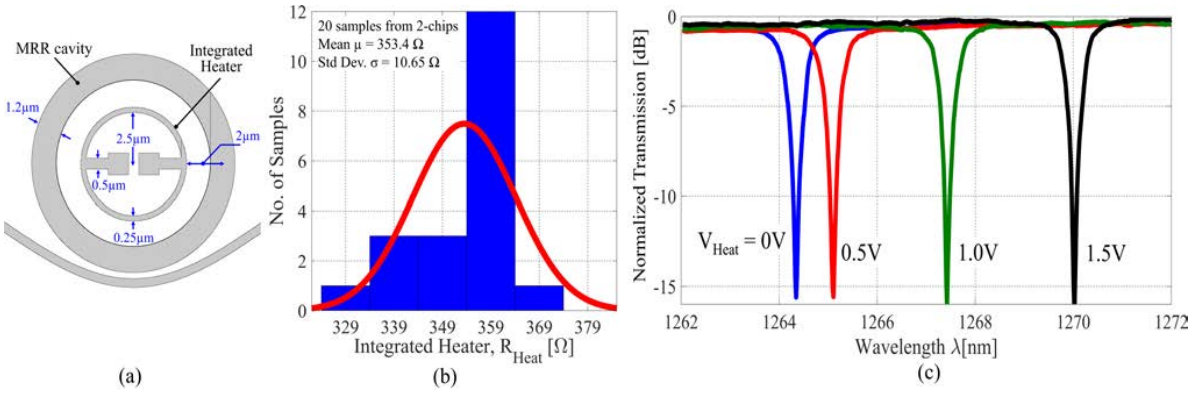


Figure 3.14: (a) MRR cavity with integrated heater (b) distribution of heater resistance (c) shift in optical transmission with V_{Heat}.

353.4 Ω (Fig. 3.14(b)). Considering the CMOS heater driver reliability, if the maximum V_{Heat} applied across R_{Heat} is limited to 1.5 V, then the heater dissipates 6.4 mW raising the MRR PD temperature by ∼110 K. As shown in Fig. 3.14(c), this induces a 5.5 nm (32% of FSR) shift in the resonant wavelength. This amount of tuning is enough to compensate for temperature and process variations in real-life applications.

3.6.3 Structure of Split-Microring Resonant SiGe Photodetector

Figure 3.15 shows the structure of the proposed split-MRR PD. The MRR cavity used in Fig. 3.15 exploits a whispering gallery mode that is concentrated in the outer half of the ring. To effectively separate the optical field, the metal contacts are placed in the center of the ring and connected with metal spokes. A 5 μm microring cavity is etched into the c-Si layer. A SiGe absorption region, responsible for carrier generation, is heteroepitaxially grown within a narrow 0.5 μm wide partially etched trench. This narrow SiGe layer width avoids crystal dislocations [58]. Along the perimeter of the microring 30 lateral P-N junctions are interleaved that use source/drain n-type and p-type implants. These junctions are arranged in the middle of the SiGe layer. Spokes of n-type and p-type are used to connect the P-N junctions with their respective contacts in the center of the ring.

To realize a fully differential PD, in [15], a 150 μm long 3 dB adiabatic splitter was used to equally split the input optical power. Instead, in this work, two PDs are formed on the same c-Si cavity by the selective wiring of P-N junctions. As shown in Fig. 3.16(a), half of P (N) spokes are wired together to form the anode (cathode) node that connects to $+V_{sig}$ (V_{PD1}). The other half are connected to V_{PD2} ($-V_{sig}$). Both of these PDs receive the same incident optical power P_{in}, but due to opposite bias, namely V_{PD1} and V_{PD2}, they output fully-differential photocurrent. The two PDs are isolated by extending the middle two P-spokes in Fig 3.15 and biasing them with V_{PD2}. The adjoining N spokes are biased at V_{PD1} creating a strong depletion region (shaded in Fig. 3.16(a)) that isolates the two PDs sharing

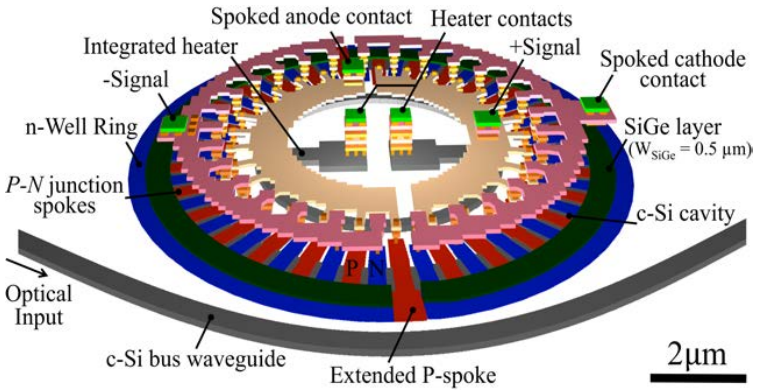


Figure 3.15: 3D layout of the proposed split-MRR resonant photodetector.

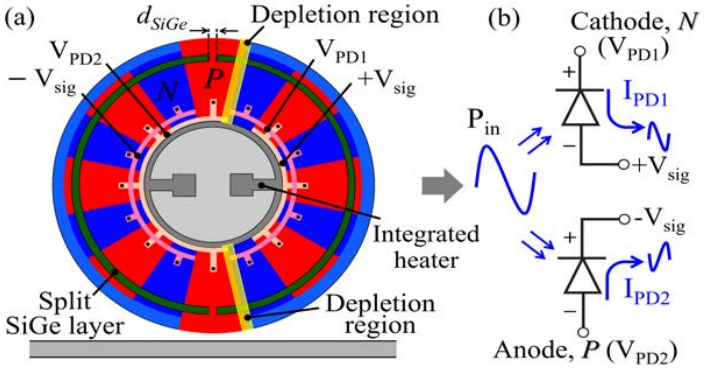


Figure 3.16: (a) Concept of a split photodetector and (b) it's equivalent circuit.

the same optical c-Si cavity. Unlike [59], splitting the SiGe layer minimizes the leakage current between the detectors and further improves the isolation. To minimize reflections created by a discontinuity in the SiGe layer, the separation gap d_{SiGe} of 0.2 μm is chosen. The 3 dB power slitting inherent to the proposed PD is independent of wavelength and temperature. This is a significant advantage compared to [15] as it requires no additional calibration. Furthermore, the split PD has multiple benefits like reduced size, boost in responsitivity, amenability to DWDM realization, and reduced parasitic loss as drop-port and use of p-Si is no longer required.

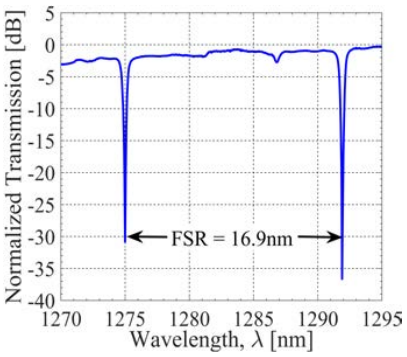
3.6.4 Characterization of Split-Microring Resonant SiGe Photodetector

The free spectral range (FSR) of the split-MRR PD is 16.9nm (3.3THz) as shown in the optical transmission plot in Fig. 3.17(a). The Q-factor of the ring around the resonant wavelength, λ_0 of 1275nm is 7.7K with FWHM bandwidth of 0.165nm (30.5GHz) (Fig.

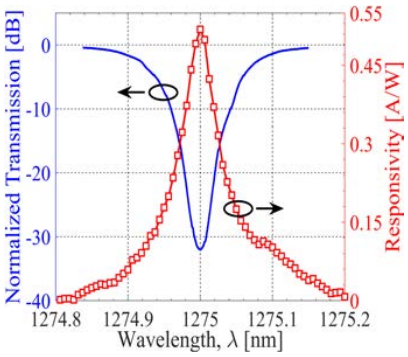
3.17(b)). This value of Q and FSR can comfortably enable a 16-way DWDM receiver with negligible crosstalk. The PD has peak responsivity ($\mathcal{R}$) of 0.52A/W at λ_0 as shown in Fig. 3.17(b). Figure 3.17(c) shows PD's I-V curve with the diode built-in potential of around 0.6V. Under no illumination (dark), the I-V curve is that of a typical diode. The reverse saturation current is flat when reverse biased and forward current grows exponential when forward biased. The dark current is in the order of nano-amps as the measurement is mainly limited by the accuracy of the source meter. At resonance and under illumination, the forward bias behavior of the PD is similar to that under dark condition. However, when reverse biased, the photocurrent does not plateau but rather continues to increase with a reverse bias voltage. At resonance, the light trapped in the MRR cavity generates carriers, which are swiped out based on the strength of the field determined by the reverse bias voltage. This creates an increasing trend in photocurrent. Ideally, a reverse biased split-MRR PD (Fig. 3.16(b)) generates fully differential (180° out of phase) currents. However, due to a mismatch in the input common-mode of the receiver, P-N junction profile, and other process induced variations, some error between I_{PD1} and I_{PD2} exist as shown in Fig. 3.17(d). At P_{in} of -10 dBm this error is less than ±0.3%, which has a negligible impact on total CMRR and hence, can be neglected. Figure 3.17(e) and (f) show the thermal characteristic of the split-MRR PD. At the maximum DAC code, the heaters output 6.5 mW causing ∼110K temperature change, which shifts the resonance wavelength by 5.6nm (1.1THz) i.e. 33% of FSR. This is sufficient to compensate for temperature variations in real-life applications.

3.7 Circuit Implementation

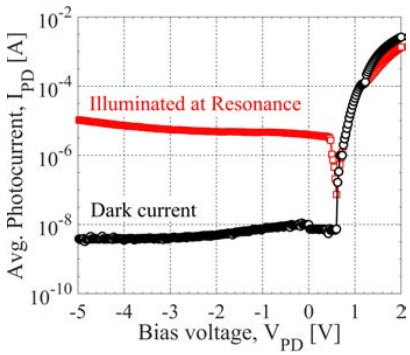
Figure 3.18 shows two *FD* optical Rx with half-rate architecture implemented over two test-chips. A CML clock receiver and distribution network delivers low-jitter off-chip clock to the receiver. The interleaved clocks for the half-rate samplers are generated by the local clock buffers. The threshold of the Rx circuit is set by current DACs at the input of optical Rx. In the version-1 design of Fig. 3.18(a), only pull down DAC was implemented while in version-2 design in Fig. 3.18(b), both pull-up and pull-down current DACs were implemented. The output bits (D_A and D_B) in Fig. 3.18(b) are retimed before being read by the digital backend. The circuit implementation of the Rx AFE is shown in Fig. 3.19(a)-(c). Only body-connected devices are used in the signal path to avoid hysteresis and threshold voltage variation due to floating body effect. Both of the SF-TIAs are realized with a simple NMOS-PMOS inverter based amplifier with 5 kΩ feedback resistor R_F. The NMOS (M_N) and PMOS (M_P) are biased at 1.1 mA drain current with a current density of 0.33 mA/μm and 0.2 mA/μm, respectively. This provides f_T of 250 GHz for NMOS and 180 GHz for PMOS, which is close to the maximum value as shown in Fig. 3.20(a). From (A.4) and (A.7), the high f_T value increases the transimpedance limit and helps reduce the input-referred noise. An 8-bit push-pull current DAC (I_{DAC}), as shown in Fig. 3.19(a), at the input of the SF-TIA, is required to avoid sensitivity degradation due to transmit modulator finite extinction ratio and residual input offset. The total capacitance at the input of the SF-TIA is around 20



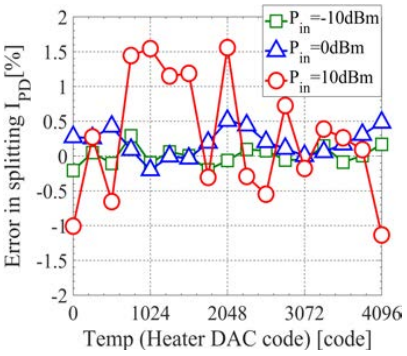
(a) Optical transmission showing free spectral range (FSR) of the detector.



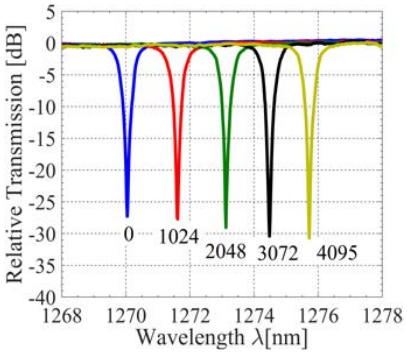
(b) Close-in optical transmission and detector's responsivity with wavelength.



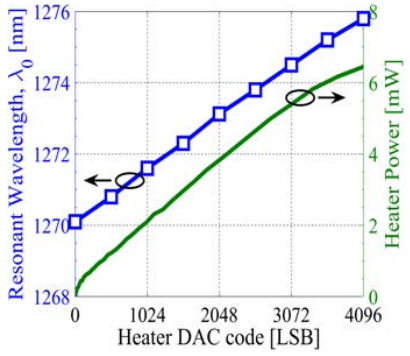
(c) Current-voltage characteristics under dark condition and illumination at resonance.



(d) Error between I_{PD1} and I_{PD2} with temperature at different input optical power.



(e) Optical transmission spectrum for different heater DAC code settings.

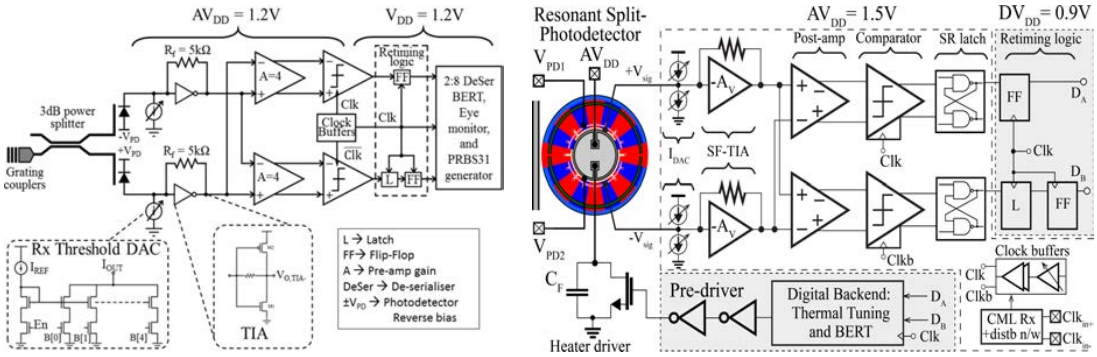


(f) Resonant wavelength (λ_0) and heater-power with heater DAC codes.

Figure 3.17: Measured optical performance and characterization of a split-MRR resonant photodetector.

fF, which is composed of C_{PD} of 10 fF, SF-TIA input capacitance C_{in} of 8 fF, and routing parasitic capacitance of 2 fF. Though the SF-TIA input-referred noise is optimal for C_{in} of 12 fF (C_{PD}+C_p) [55], it is not opted in order to reduce the TIA power consumption [23]. This causes marginal ($< 4\%$) increase in input-referred noise.

The two SF-TIA generate a fully-differential output to drive the post-amplifier G_p. The input pair M_1 and M_2 of G_p are sized to provide an open-loop gain of 4 resulting in a total gain of 86 dBΩ with 3 dB bandwidth of 7 GHz. The load resistors R_L absorb the kickback from the comparator. A matching aware layout of R_L and cascode devices for I_{Tail} are used for achieving a high CMRR to suppress PSN and common-mode noise. The simulation shows a CMRR of 25 dB is achieved at 7 GHz bandwidth. The cascodes M_3 and M_4 reduce the input pair Miller capacitance easing the SF-TIA loading. It also provides a low-impedance node to inject current for correcting the comparator offset. The offset DAC I_{Offset} has 4-



(a) (b)

Figure 3.18: Schematic of proposed *FD* optical Rx: (a) Version-1 design with 3 dB couple and linear SiGe detector and (b) Version-2 design using split-MRR detector.

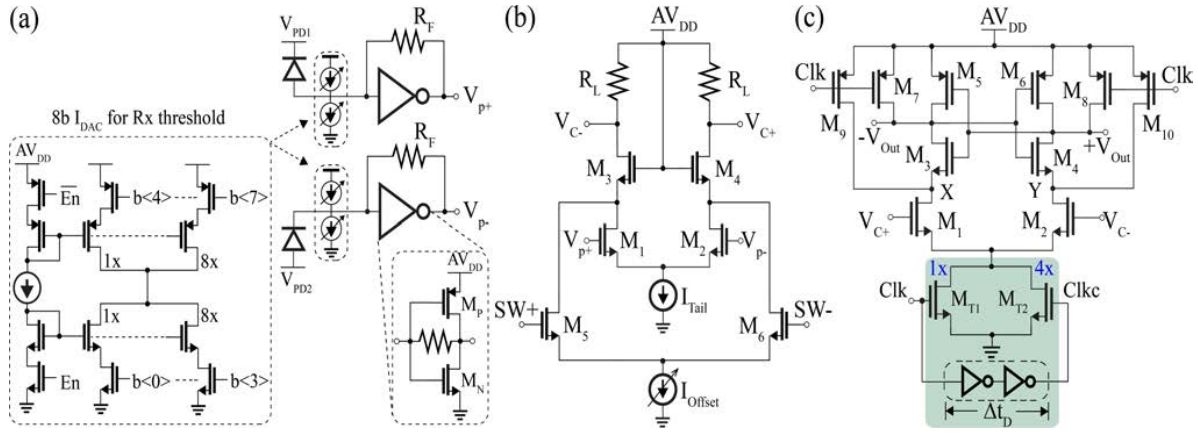


Figure 3.19: Circuit diagram (a) Shunt-feedback TIA (SF-TIA), (b) Post-amp (G_P) with offset cancellation, and (c) modified StrongARM comparator.

bit resolution with a structure similar to I_{DAC}. Figure 3.20(b) shows the total noise PSD referred at the input of the SF-TIA. The integrated noise over 7 GHz is about 280 nA_{rms}. As evident, the thermal noise of R_F and SF-TIA are the dominant noise contributor. The spot thermal noise PSD of R_F is about 2.3 $\text{pA}/\sqrt{Hz}$, which is comparable to other noise sources at mid frequencies. At higher frequencies, the channel noise of SF-TIA, which scales as f^2, dominates. Also, as predicted by (A.6), the post-amplifier noise contribution increases with f^4, which after a point is even higher than that of SF-TIA. The devices of I_{DAC} are sized for minimal noise contribution at all frequencies.

The comparator makes random decision errors (BER=0.5) if the input voltage is below its minimum resolution voltage. This degrades the Rx sensitivity when referred to its input. The comparator's minimum resolution voltage is dominated by its input-referred noise $\overline{v_{nc}}$, which is inversely proportional to g_m/I_D of the input pair [62]. An effective means of increasing

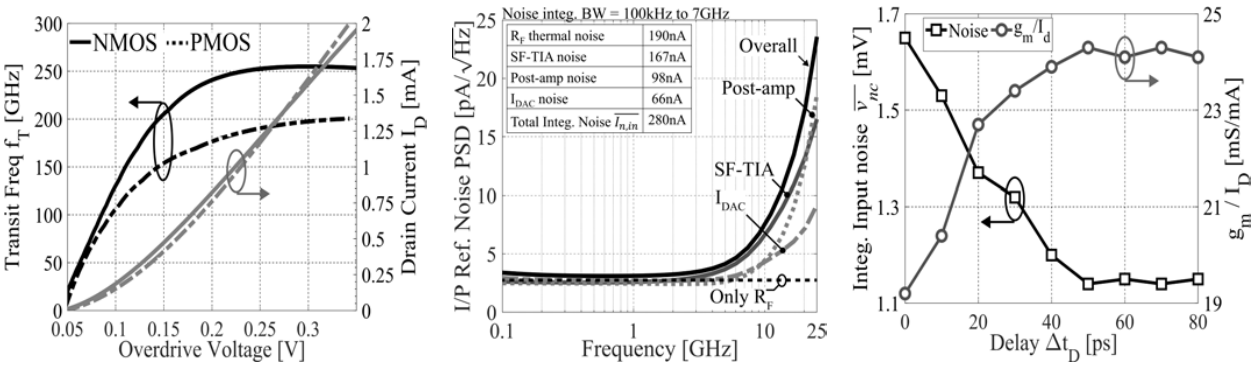


Figure 3.20: Simulation results of the receiver analog front-end. (a) f_T and bias current for NMOS/PMOS, (b) total input-referred noise PSD, and (c) Comparator input-referred noise trade-off.

g_m/I_D is to reduce the tail current but without affecting the regeneration time. To this end, Fig. 3.19(c) shows a modified strongARM comparator, where the tail device is split into two devices M_{T1} and M_{T2} with a 1:4 sizing ratio. The drain current of M_{T1}, I_{T1} controls the integration time t_{INT} during which the input pair effectively integrates the input signal and filters out high-frequency noise. This integration phase is initiated by the rising edge of the clock, which turns M_{T1} *ON* and starts the discharge of the internal nodes X-Y through M_1 and M_2. The delay Δt_D controls t_{INT} as long as $\Delta t_D \leq C_{out} \cdot V_{T,p} / I_{T1}$, where $V_{T,p}$ is the threshold voltage of M_5 and M_6. After the delay of Δt_D M_{T2} turns *ON* initiating the regeneration phase during which the drain current of M_{T2}, I_{T2}, along with I_{T1} determines the regeneration time t_{reg}. The use of two tail devices also helps to reduce kickback noise. To avoid significant speed penalty due to longer t_{INT}, it is chosen such that $t_{INT} + t_{reg} \leq T_{clk}/2$.

As shown in Fig. 3.20(c) increasing Δt_D delays the onset of M_{T2} making the input-pair integrate longer. This increases the g_m/I_D and reduces the $\overline{v_{nc}}$. Thus, for Δt_D between 0 and 50 ps the $\overline{v_{nc}}$ improves by 30% dropping from 1.65 mV to 1.14 mV. When referred to the input the equivalent current noise is 60 nA_{rms}, which is less than the dominant R_F thermal noise illustrated in Fig. 3.20(b). However, increasing Δt_D beyond 50 ps yields no additional noise reduction as g_m/I_D does not increase any further. This is because by then I_{T1} already discharges the output below $V_{T,p}$, which triggers regeneration. During regeneration, both M_{T1} and M_{T2} are *ON* ensuring the total current and, thus the regeneration time constant t_{reg}, is unchanged compared to the conventional comparator. For a brief period between M_{T2} turning *OFF* and precharge switches turning *ON*, crowbar current may exist. To minimize it, M_9 and M_{10} are appropriately sized.

The digital backend of Fig. 3.21 characterizes the performance of the receiver. On the test-chip, it is shared between four receiver sites. A 2:16 deserializer (DeSer), one per receiver, parallelizes incoming serial bits to relax the timing and power consumption of the backend.

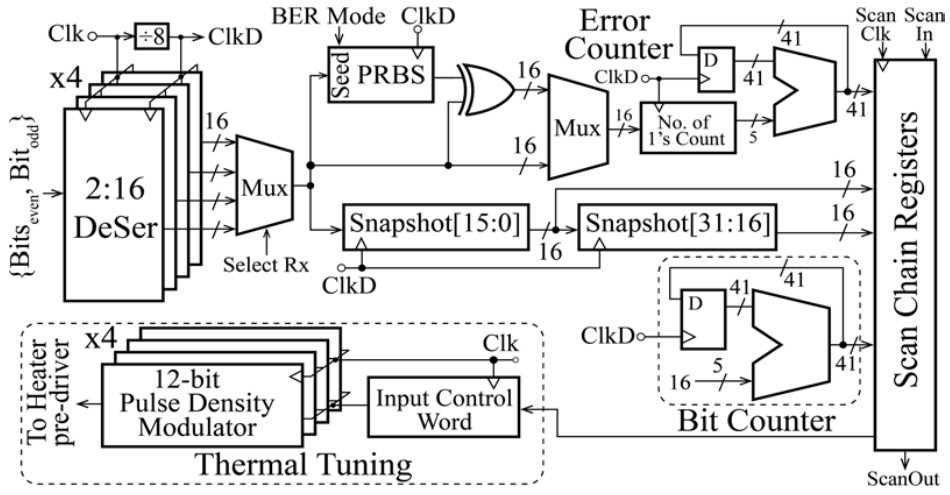


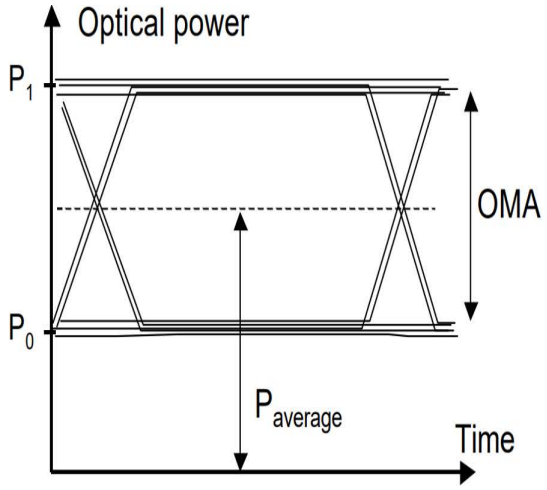
Figure 3.21: Digital backend used to characterize receiver performance.

The PRBS generator can self-seed and generate a 31-bit PRBS pattern, which is compared with the bits received. The error counter increments if this comparison fails, which gives a BER value. Both of the counters are 41-bit wide to enable BER measurement in excess of 10^{-12}. A 32-bit wide snapshot register captures receiver output, which is used for offset correction and noise characterization. Lastly, pulse density modulators (PDM) thermally stabilize the split-MRR detectors by generating pulses whose position is controlled by a 12-bit input control word.

3.8 Realization and Experiments

3.8.1 OMA and finite ER power penalty

Having a low ER (in the range of <6-7 dB) induces severe power penalty on the overall link budget. The resulting offset created due to finite zero power level (P_0 in Fig. 3.22) can be corrected using the current DAC at the input of the Rx (IDAC). However, it comes at the cost of degradation in the Rx sensitivity due to noise contribution from the offset correcting current DAC. Hence, to ensure that the true sensitivity of Rx is measured, it is crucial to ensure an ER of at least 10 dB. As shown in Fig. 3.22, the ER is defined as P_1/P_0, where P_1 and P_0 are the power levels representing binary-1 and 0, respectively. If $P_0 = 0$ then the ER is infinite, while for $P_0 > 0$ ER is finite. When ER is finite, a non-zero optical power is emitted for a binary-0 level that appears as a DC offset. Consequently, to maintain the same BER either the Rx threshold should be increased, which eats into the Rx sensitivity, or the transmit laser optical power should be increased, which degrades overall link energy-efficiency by making laser consume increased electrical power. This degradation in Rx sensitivity and the increase in the transmit laser optical power due to low ER can be quantified as *power*



$$ER = P_1/P_0,\ OMA = P_1 - P_0,\ \text{and}\ P_{average} = \frac{(P_1 + P_0)}{2}$$

$P_{average}$, OMA, and ER are related by,

For high ER,

$$P_1 = P_{peak} = 2 \cdot P_{average} = OMA \quad (1)$$

For low ER,

$$P_1 = P_{peak} = 2 \cdot P_{average} = \left[OMA \cdot \frac{ER+1}{ER-1}\right] - P_0 \quad (2)$$

Figure 3.22: A typical eye at the input of Rx and equations relating OMA, peak optical power, and ER.

penalty. This power penalty is severe, particularly for ER $<$ 7 dB. Further, Rx can handle low ER as long as $P_0 > 0$ does not overload it. However, low ER corrupts the Rx sensitivity measurements impairing it from being a true representation of Rx performance. In addition, as shown in Fig. 3.22, if high ER is achieved then the sensitivity of Rx can be unambiguously quantified by OMA alone. The average sensitivity is then directly related to OMA and is equal to OMA/2. The same does not hold true for low ER. Owing to these reasons, an ER of at least $>$10 dB is ensured during measurements of the two test-chips.

3.8.2 Method to measure sensitivity of the optical Rx

Measuring the electrical peak-to-peak current sensitivity and the optical modulation amplitude (OMA) sensitivity are two of the most critical performance metrics of an optical Rx. Once, OMA is measured the current sensitivity is directly related to it through the responsivity $\mathcal{R}$ of the photodetector. The OMA is defined as the difference between P_1 and P_0, where P_1 and P_0 are the power levels representing bit-1 and 0, respectively. Thus, the OMA sensitivity of an optical Rx is the minimum difference between P_1 and P_0 required of the Rx to detect the received bits with a target BER of $<10^{-12}$. Once OMA sensitivity is obtained, the average Rx sensitivity can be found using expressions shown in Fig. 3.22. Note that as argued earlier, it is necessary to ensure that ER is $>$ 10 dB to accurately measure the Rx sensitivity.

Figure 3.23 shows the test-bench used to measure the Rx OMA sensitivity. The CW laser is modulated with the PRBS31 test pattern to generate an optical test signal. The easiest way to obtain the BER vs. OMA sensitivity plot is to sweep the input laser power and monitor the BER. Unfortunately, the ER at the output of MZM (at node-A) is a function of laser power and the applied DC bias (not shown in Fig. 3.23). This makes it challenging to

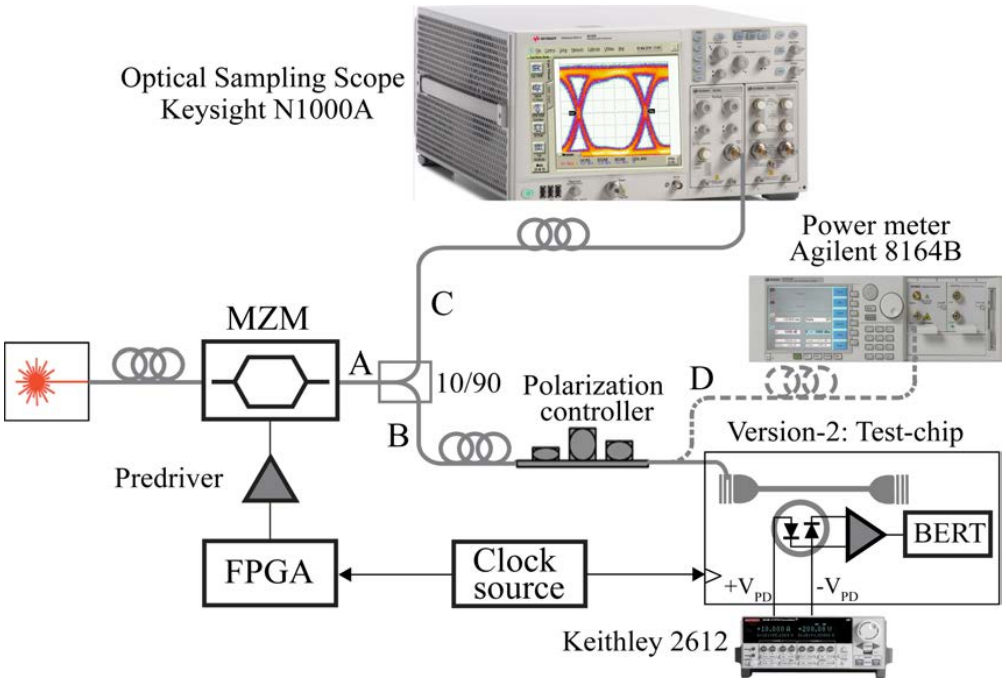


Figure 3.23: Calibration for variation in split ratio with λ and coupling position.

measure OMA by simply sweeping the laser power. Besides, the CW laser source also has a minimum output limit below which it cannot faithfully generate the output. Typically, it is around -15 dBm while for OMA measurement a laser power as small as -25 dBm might be required. To avoid this issue, the laser power is set to a fixed value and MZM is biased at such that the ER at node-A is >10dB. While the laser power is attenuated by tuning the polarization controller. The controller only attenuates the input optical power and retains the ER intact. As the controllers attenuation is unknown, its output is first connected to a power meter to measure the average power. As ER>10 dB, this average value readily translates into the OMA sensitivity of the optical Rx. When the input optical signal is coupled into the Rx chip the differential detector pulls I_{PD1} and I_{PD2} from V_{PD1} and V_{PD2} SMU (Keithley 2612). The input OMA can be cross-verified by converting these average currents to average power and thus, to the input OMA using the PD responsivity. Once the two value of the OMA match, we use the average current values to estimate the input OMA. Lastly, for each OMA point, we perform multiple BER measurements using on-chip BERT and report the best-measured BER value. These steps are repeated for both the data-rates of 6Gbps and 12Gbps. Note that the grating coupler loss is de-embedded from the OMA numbers reported in this thesis. Also note that to measure the OMA, the clock and the threshold of the optical Rx are set to a fixed offset where the best BER performance is expected. This can be obtained by first measuring eye diagrams in statistical and BER mode.

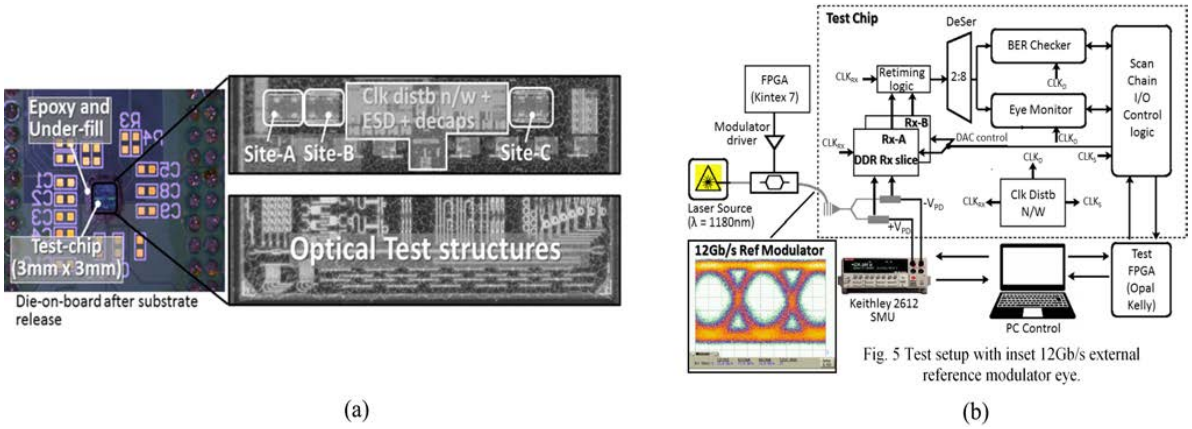


Figure 3.24: (a) Photomicrograph of test-chip. Size is 3 mm X 3 mm with 73 I/O pads. (b) Test setup with inset 12 Gb/s external reference modulator eye.

3.8.3 Version-1 Test-chip: Measurement Results

The optical receivers are fabricated in the GFUS 45-nm SOI CMOS process. Figure 3.24(a) shows the die-photo of the test-chip. It has 3 optical receiver sites, each having 4 analog receiver cores sharing a BERT, eye-monitor, PRBS generator and clock buffers. Site-A has 4 single-ended (*SE*) receivers while sites -B and C each have 4 fully-differential (*FD*) receivers. Optical performance/loss numbers are extracted from the optical test structures designed in a dedicated test-area. The test-chip is bumped with C4 balls, flipped and die-attached directly to an FR4 PCB. The mounted chip is under-filled with electrically insulating adhesive and epoxy is applied on the edges. Underfill holds the chip during die-thinning process and epoxy protects the edges during substrate release.

The test-bench to characterize receiver performance is shown in the Fig. 3.24(b). A JDSU lithium niobate (LiNbO3) Mach Zehnder interferometer (MZI) modulates the 1180 nm laser with 2^{31}-1 PRBS data pattern generated by the Kintex-7 FPGA. MZI has electro-optic bandwidth of 30 GHz while the accompanying modulator driver JDSU H301-1210 has 3 dB RF bandwidth of 11 GHz. Resulting 12 Gb/s modulated PRBS31 output is shown in Fig. 3.24(b) inset. It has 5.5 ps RMS jitter and rise/fall times of 66/62 ps. The MZI is biased to achieve 11.6dB extinction ratio at 12 Gb/s. The PRBS31 modulated data is coupled into the test-chip using lensed fiber with spot diameter of 2.5±0.5 μm. The photodetectors are biased with a reverse voltage of 5 V. The bandwidth and responsivity of the detectors is dependent on V_{PD1} and V_{PD2}. Hence, they are chosen to maximize photodetectors responsivity to 0.023 A/W while achieving 5 GHz bandwidth.

Results for *SE* Rx are measured from Site A in Fig. 3.24(a) whereas the results for *FD* receivers are measured from one of the test-sites of Site B or Site C. Each test site is 300 μm x190 μm while each receiver site has area of 55 μm x 40 μm. Running from analog/digital supplies of 1.2V, the test site consumes 48 mW out of which each receiver consumes 4.7 mW.

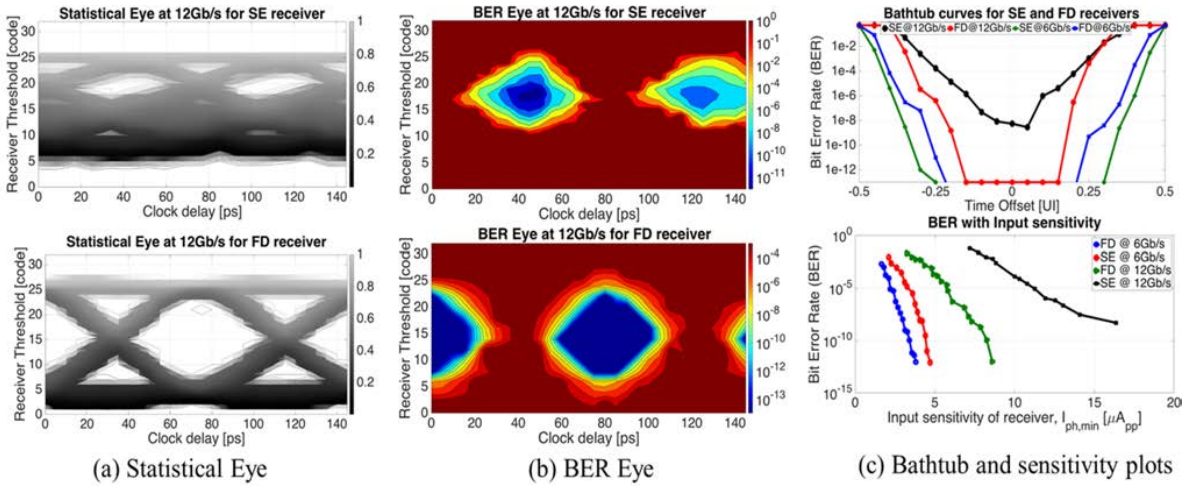


Figure 3.25: Measured statistical eye, BER eye, bathtub curves and sensitivity plots for SE and FD Rxs.

The on-chip BER checker has self-seeded 2^{31}-1 PRBS pattern generator which can lock to the received PRBS31 pattern and compute BER. Both statistical and BER eye are obtained at -0.2dBm input optical power-level (44 μA_{pp}). The receiver threshold is controlled through a 5 bit DAC at the input of the TIA with step size of 1.3 μA_{pp}/code. The input sensitivity is measured by applying 231-1 PRBS test pattern operating at 12 Gb/s. Figure 3.25(a) shows statistical eye for *SE* and *FD* Rxs. It is apparent that *SE* eye is only partially open and shows significant deterioration due to common-mode noise and power supply noise. Figure 3.25(b) shows the BER eye for both *SE* and *FD* Rxs. It can be seen that *FD* Rx can achieve BER $<10^{-12}$ while *SE* Rx barely meets BER $< 10^{-8}$. Figure 3.25(c) shows the bathtub curves and the BER with the Rxs input sensitivity, $I_{ph,min}$ (μA_{pp}). The 12 Gb/s *FD* Rx has 0.3 UI of timing margin at BER $< 10^{-12}$, at 8.6 μA_{pp} input current sensitivity. The *SE* Rx input sensitivity at the same speed is 16.3 μA_{pp} but at higher BER. However, at lower data rate common-mode and supply noise are lowered. For example, at 6 Gb/s the difference between *SE* and *FD* sensitivity is not very significant. Timing margin for *SE* is about 0.4 UI and that for *FD* is about 0.6 UI.

Finally, depending on wavelength, coupling angle and coupling position, multiple optical modes can propagate through power splitter affecting the power-split ratio. To circumvent this issue an off-chip calibration is applied. As shown in Fig. 3.24(b), V_{PD1} and V_{PD2} are tuned until the average current from the detectors are equal. As the tuning efficiency is only 0.33 μA/V, correction range is limited. Figure 3.26 shows the variation in powersplit ratio with λ and Y, and its effect on the BER. After calibration BER of $<10^{-10}$ can be achieved over 40 nm wavelength band ($\Delta\lambda$). For high-density optical interconnect this range is sufficient to fit 36 wavelength multiplexed channels [28].

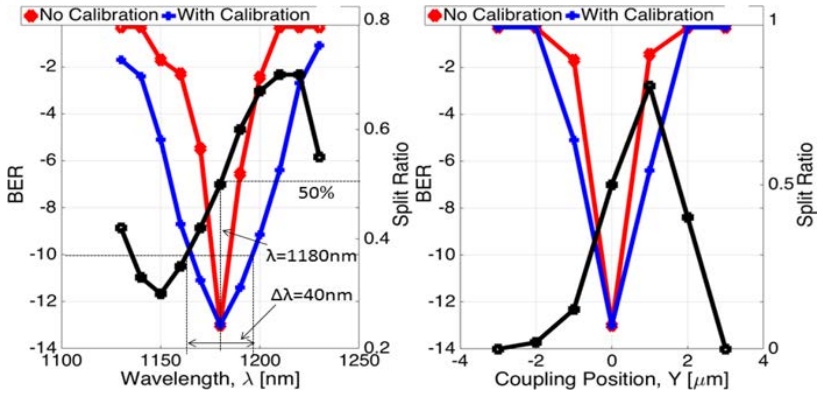


Figure 3.26: Calibration for variation in split ratio with λ and coupling position.

3.8.4 Version-2 Test-chip: Thermal Tuning of Split-MRR Photodetector

The strong thermo-optic coefficient of silicon ($dn_{Si}/dT = 1.8\times10^{-4}K^{-1}$) combined with high Q-factor of MRR changes the optical performance due to thermal effects. For 1 Kelvin temperature change λ_0 drifts by 0.036nm, which is 22% of the FWHM bandwidth. Such thermal dependence is not specific to MRR, but common in real-life applications. For example, the datacenter pluggables use VCSELs that have even higher temperature drift of 0.06nm/K requiring strict regulation of ambient temperature [63] and broad channel spacing.

As the MRR for the Rx experiences lower incident optical power, the self-heating effects are negligible. Thus, the dominant source of thermal drift is the ambient temperature fluctuations. To compensate for it, a thermal tuning loop of Fig. 3.27(a) is used. The off-chip tuning algorithm locks the detector to a target average photocurrent, I_{PD} by reading the current from an external $V_{PD1,2}$ source meter and controlling the PDM through a scan-chain register [64]. The PDM generates pulses with density depending on the input control word over a fixed 0.17 ns period. The thermal impulse response of the detector is low-pass with 67 kHz cutoff [28], which averages the PDM output forming a 12-bit digital-to-analog converter (DAC). A load capacitor, C_F, of 1 pF reduces the slew-rate at the drain of NMOS heater driver, M_1. The resulting output heater power is monotonic and linear with DAC code. The heater resistance, R_{Heater}, measured from 10 detectors is between 250 Ω to 300 Ω. From Fig. 3.17(e)-(f), the tuning efficiency of the loop is 0.86 nm/mW (5.9 μW/GHz) and resolution of 0.27 GHz/LSB.

Figure 3.27(b) depicts the behavior of the tuning loop. For a given target I_{PD} the loop can converge to either to the left (point A) or right (point B) of λ_0. To ensure negative feedback and thus, stable loop operation, left side point A is chosen [28]. If the detector is operating at λ_1 with I_{PD1} greater than the target I_{PD}, the thermal tuning controller will heat the detector until it shifts to point-C. Similarly, if the detector is operating at λ_2 with I_{PD2} less than target I_{PD} then the controller will reduce the heating (cooldown) until the detector

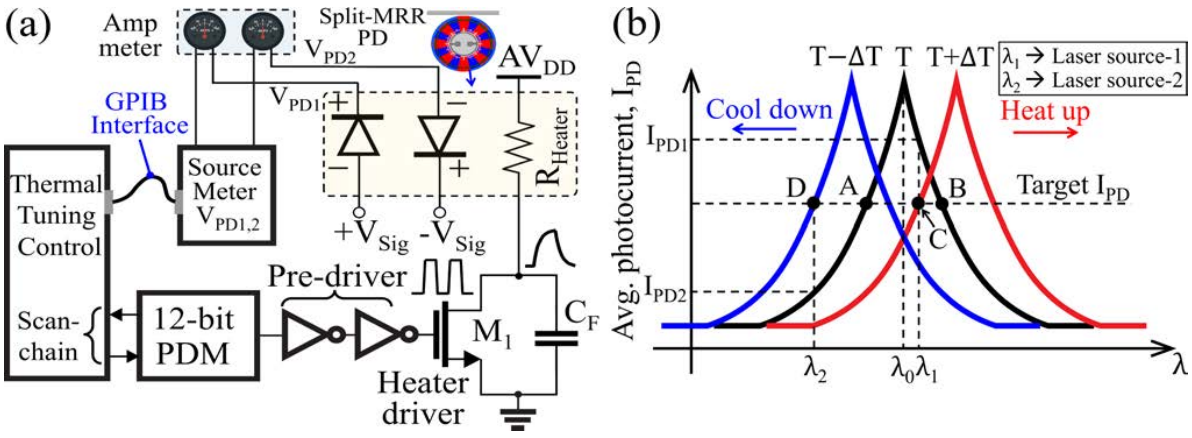
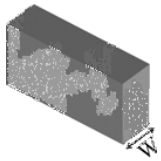
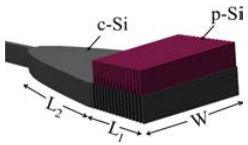
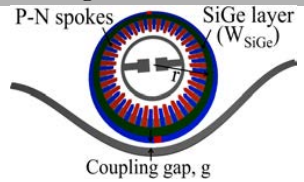


Figure 3.27: (a) Thermal tuning loop and (b) operation of tuning controller used to stabilize resonant split-photodetector.

reaches a point-D. During initialization, converging to a maximum change in temperature of 110 K requires 10 secs. Each step of heating or cooling involves reading I_{PD} and controlling the PDM through a scan-chain, which takes a total time of 8ms. This speed is sufficient to track ambient temperature change and stabilize the split-MRR detector during the BER and statistical eye measurements. Faster tuning in the milliseconds range has been demonstrated previously by fully integrating the control loops [28].

Table 3.2: Specifications of Photonic Blocks used in the Fully Differential Receiver

	c-Si Waveguide	Grating Couplers		Split-microring Resonant Photodetector	
					
	Measured†	Measured†	Best Device* [65]	Measured†	Best Device* [44]
Performance metric	Single-mode	Bandwidth, BW (-1 dB) = 78 nm	Bandwidth, BW (-1dB)=100 nm	$\mathcal{R}$ = 0.52 A/W @λ=1275 nm $BW \sim$ 5 GHz	$\mathcal{R}$ = 0.55 A/W @λ=1176.9 nm $BW \sim$ 5 GHz
Loss	Propagation loss = 3 dB/cm	Coupling loss = 4.5 dB	Coupling loss = 1.2 dB	Propagation loss, α_{ring} = 1.1 dB/cm	α_{ring} = 1.3 dB/cm
Key Dimensions‡	W=0.4 μm	W=6.3 μm, L_1=10 μm, L_2=25 μm		r=5 μm, No. of spokes = 60, g = 0.23 μm d_{SiGe}= 0.2 μm, W_{SiGe} = 0.5μm	

†Measured from the test-chip designed in this work. *Standalone devices reported in the recent literature. ‡Used in this work.

3.8.5 Version-2 Test-chip: Measurement Results

Optical components like c-Si waveguide, vertical grating coupler, and split-MRR PD, are used to realize the *FD* optical Rx. Their performance is measured from the standalone test structures on the same test-chip and summarized in Table. 3.2. The test-bench of Fig. 3.28 characterizes the optical Rx performance from the test sites with co-integrated electronics and photonics. A Lithium Niobate ($LiNbO_3$) Mach-Zehnder modulator (MZM) with 25 GHz electro-optic bandwidth modulates the 1275 nm continuous-wave (CW) input laser with 2^{31}-1 PRBS data pattern generated by the FPGA. The MZM pre-driver amplifies the FPGA output with 30 dB programmable gain and 18 GHz 3 dB RF bandwidth. The MZM is biased to achieve 13.2dB extinction ratio (ER) and 7.3 dB insertion loss at 12 Gb/s. The inset of Fig. 3.28 shows resulting 12 Gb/s modulated PRBS31 test data pattern, which is ISI free with 1.6 ps RMS jitter and rise/fall times of 27/32 ps. It is coupled into the test-chip using a lensed fiber with a spot diameter of 2.5 μm$\pm$0.5 μm. The PD power-supplies $V_{PD1,2}$ are chosen such that the two split-MMR PDs are reverse biased with 5 V. This ensures a maximum responsivity while achieving $\sim$5 GHz bandwidth. Figure 3.29 shows the die-photo of the test-chip. It contains a total of 3 test sites, viz.: A, B, and C, each has 4 Rxs that share a common digital backend. Site-A has 4 *SE* Rxs while site-B and site-C each have 4 *FD* Rxs.

Both *SE* and *FD* Rxs run from an analog supply (AV_{DD}) of 1.5V and a digital supply (DV_{DD}) of 0.9V. At 12 Gb/s the *FD* optical Rx consumes 7 mW (0.58 pJ/bit), of which the TIAs consumes 3 mW while the rest is consumed by the post-amplifier, comparator, and the clock-buffers. Additionally, the digital backend, deserializer, and PDM along with pre-driver consume 18 mW, 0.8 mW, and 0.7 mW respectively. Both statistical and bit-error rate (BER) eye are measured at 0 dBm input optical power generating 0.18 mA average photocurrent and output swing of $1.5V_{pp}$. As all the Rx sites share the same power-supply, turning the neighboring sites ON with continuously toggling input current DACs generates PSN and common-mode noise that couples into the Rx site under test. Consequently, the statistical eye of *SE* Rx in Fig. 3.30(a) significantly deteriorates with a partial vertical opening limited to 50 I_{DAC} codes while the same for *FD* Rx in Fig. 3.30(b) is 130 codes. Further, the rising edge in Fig. 3.30(b) is slightly faster than Fig. 3.30(a) as *FD* Rx has lower PD capacitance (Fig. 3.3(c)). Comparing Fig. 3.30(d) and Fig. 3.30(e), the *FD* Rx achieves BER 10^{-12} while the *SE* Rx barely meets $\sim10^{-8}$. The statistical and BER eye confirm the effectiveness of the *FD* Rx in suppressing PSN and common-mode noise. Bathtub curves and sensitivity plots of Fig. 3.30(c) & (f), further quantify the performance improvement. The OMA sensitivity is defined as a minimum difference between the high and low optical levels that the receiver can detect with BER of $<10^{-12}$ for at least one point on the bathtub curve of Fig. 3.30(c). To measure high OMA sensitivity in Fig. 3.30(f), the input optical power should be reduced to less than -20 dBm while retaining the ER better than 10 dB. For this purpose, the input laser power and polarization controller are tuned. At 12Gb/s the *FD* receiver has 0.25UI timing margin at BER of 10^{-12} with OMA of -18.2 dBm. For BER of 10^{-8}, the *SE* Rx has OMA sensitivity of -16.3 dBm whereas *FD* Rx has -19.1 dBm. The

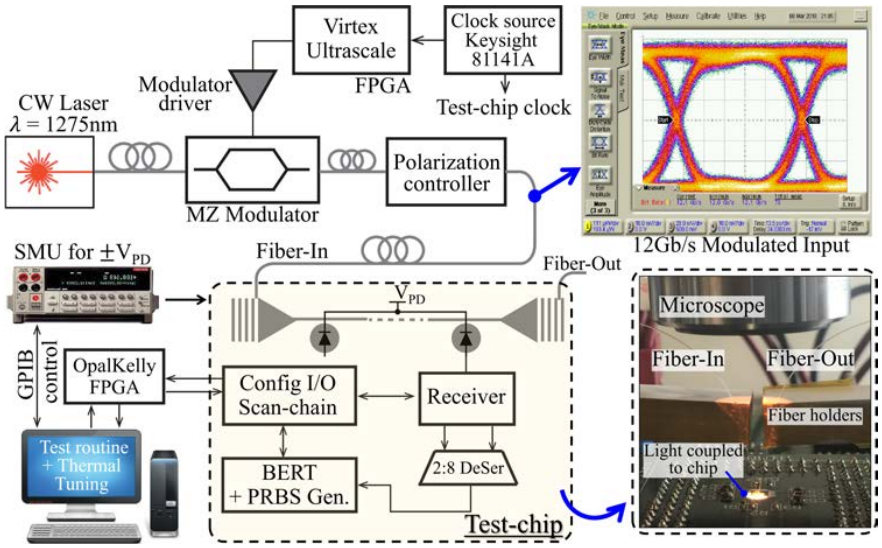


Figure 3.28: Optical test-bench with inset of setup for coupling light into the test-chip and 12 Gb/s modulated input data eye.

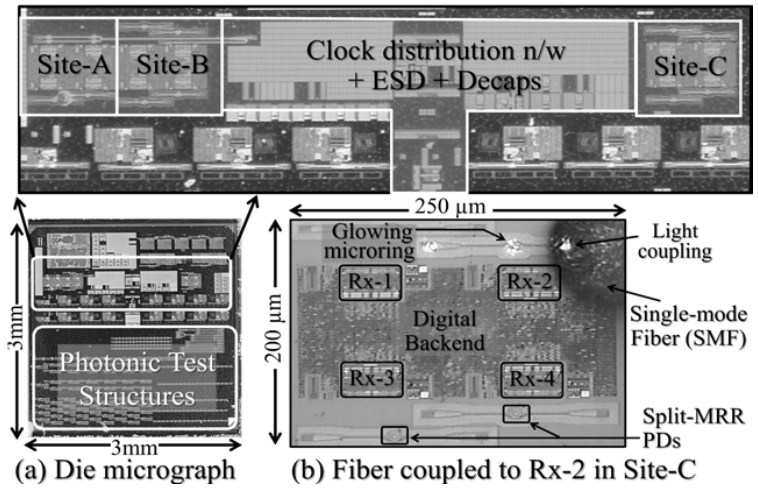
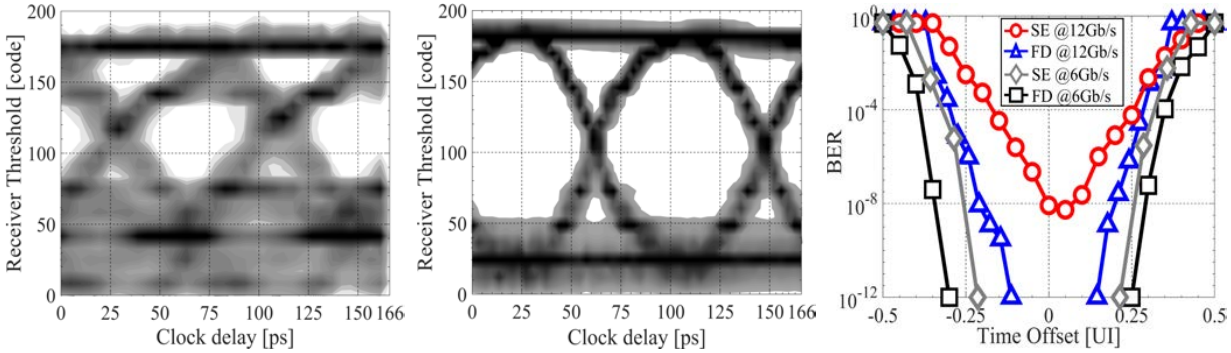


Figure 3.29: Die micrograph and microscope photo of a fiber coupled test-site. At resonance the microring glows due to the light trapped inside.

timing margin for *SE* is about 0.4UI and that for *FD* is about 0.6UI.



(a) Statistical eye of *SE* Rx at 12Gb/s.

(b) Statistical eye of *FD* Rx at 12Gb/s.

(c) Bathtub curves at 0dBm input optical power.

(d) BER eye of *SE* Rx at 12Gb/s.

(e) BER eye of *FD* Rx at 12Gb/s.

(f) Sensitivity plots for *SE* and *FD* Rxs.

Figure 3.30: Measured performance of the optical Rxs for a PRBS31 input pattern. For (a)-(e) input optical power of 0 dBm and ER of 13.2 dB is used.

Table 3.3: Performance Summary and Comparison With State-of-the-Art Moderate to High-Speed Optical Receivers

Reference	[66] **ISSCC 2017**	[47] **JSSC 2018**	[50] **ISSCC 2010**	[67] **ISSCC 2013**	[28] **JSSC 2016**	[15] **ESSCIRC 2016**	[23] **JSSC 2018**	**This Work**
Process	14-nm FinFET	0.18μm SiGe BiCMOS	0.13μm CMOS	90nm CMOS	45-nm SOI CMOS	45-nm SOI CMOS	65-nm CMOS	45-nm SOI CMOS
Integration	Wirebond	Flip-chip	Monolithic	Wirebond	Monolithic	Monolithic	Wirebond	Monolithic
Data Rate [Gb/s]	64 | 32	50	10	9	10	12	12	12
BER/PRBS [bits]	10^{-12}/7	10^{-12}/9	10^{-12}/–	10^{-13}/31	10^{-12}/31	10^{-12}/31	10^{-12}/31	10^{-12}/31
Photodetector cap [fF]	69	60	–	140	15-20	15-20	100	20
PD Responsivity $\mathcal{R}$ [A/W]	0.52	0.8	0.8	0.55	0.023	0.023	0.75	0.52
Area [mm^2]	0.028	3.2$^\diamond$	0.32	0.004	0.0025	0.0022	0.12	0.0021
Efficiency [pJ/bit]	1.4 | 2.8	7.9	1.5	0.93	0.35	0.36	1.9	0.58
$\boldsymbol{I_{sen,pp}}$ [μA$_{\mathbf{pp}}$]†	148‡	96	6	174‡	18	8.6	15‡	7.9
OMA Sensitivity [dBm]	-5.5 | -13	-9.2	–	-5.0	-1.1	-4.3	-16.8	-18.2

†Minimum photodetector current required by the receiver $^\diamond$Full-chip including pads ‡Calculated from OMA and responsivity.

Table 3.3 summarizes the performance of the proposed optical Rx and compares it with the state-of-the-art. The split-MRR PD has a responsivity of 0.52 A/W which is comparable with other designs. However, due to monolithic integration, the capacitance at the input of the receiver is less than 20 fF, which is one third compared to the recently reported flip-chip solution [47]. Among monolithic designs, the proposed optical Rx achieves better sensitivity at 12 Gb/s with similar or better energy-efficiency. Estimating the OMA sensitivity of [50] was not possible as the dark current of the integrated PD is equal to the average current sensitivity of the Rx. The optimized Rx AFE yields better input current sensitivity than previously measured results [15]. Compared to 12 Gb/s Rxs across integration technologies, the proposed Rx achieves current sensitivity comparable to [50] and more than 1.4 dB better OMA sensitivity, which can potentially lower the laser power consumption by 28 %, along with 3x lower energy-per-bit. Lastly, the receiver's footprint area is small enough to enable DWDM systems [7]. The data-rate can be increased further by employing any of the recently reported equalization schemes [38, 23, 66].

3.9 Summary

To address the high power consumption of laser source improving the Rx sensitivity is crucial. In these regards, this chapter presented a high-sensitivity fully differential optical Rx for energy efficient and high bandwidth density optical interconnects. The fully-differential architecture, enabled by the differential detectors, suppresses common-mode and power-supply noise to improve sensitivity without reducing bandwidth or incurring power penalty. The Rx AFE is optimized to reduce the input-referred thermal noise. The comparator noise contribution, which is quite substantial, is reduced by using a modified StrongARM comparator with wider sampling aperture. The high-sensitivity, high-bandwidth density, and low energy are all enabled by the monolithic integration approach of photonic devices with high-performance transistors, which allows photonic-device and circuit co-design and optimization.

The version-1 design carried a fully-differential detector realized using a 3 dB coupler and two linear SiGe detectors achieved electrical sensitivity of 8.6 μA_{pp} at 12 Gb/s with 0.36 pJ/bit energy-efficiency. The linear detectors has a limited responsivity of 0.023 A/W while the 3 dB coupler was bulky and was sensitive to wavelength, which required calibration to avoid BER degradation. These issues addressed in the version-2 test-chip where the differential detector is realized using a split MRR detector. As the Rx AFE and the detectors are monolithic-integrated in 45nm SOI CMOS, the interface parasitic of <20 fF is achieved. This enables SF-TIA to use a large (5 kΩ) feedback resistor without amplifying its voltage noise. The Rx sensitivity is thus greatly improved due to the reduction in input-referred noise. The measurement results from the version-2 test-chip show high OMA sensitivity of -18.2 dBm at 12Gb/s and energy-efficiency of 0.58 pJ/bits while achieving BER $< 10^{-12}$. The energy-efficiency is slightly degraded compared to version-1 test-chip due to additional power spend for thermal tuning of the split detector. However, the footprint area of the receiver

is only 0.0021 mm^2 making it suitable for DWDM systems. From sensitivity viewpoint, the receiver compares favorably with state-of-the-art designs at 12 Gb/s, with significant improvement in energy-efficiency.

Lastly, this chapter also described a procedure to extract parameters and performance characterization of the MRR-based photodetector. These PDs are characterized in terms of responsivity, dark current, RC bandwidth, and thermal tuning range. From the parameter extracted, an equivalent circuit model is built to aid electro-optic co-optimization and design. It was also observed that under sufficient reverse bias the MRR PD achieved a responsivity of 0.6 A/W at -7.5V reverse bias with a negligible dark current. The integrated heater, which is a crucial component for successful operation of MRR PDs, is also characterized. Measured from 20 test-sites over 2 chips, the heater had a mean resistance of 353 Ω and is capable of raising the detector's temperature by $\sim$110 K when the heater driver is powered from 1.5 V supply.

Chapter 4

Demonstration of a Laser-forwarded Coherent Optical Link

For the silicon photonic links to meet the target bit error rate, the laser source must output enough optical power to overcome the optical channel loss and limited receiver sensitivity. Combined with a poor wall-plug efficiency, this optical power requirement makes the electrical power consumed by the laser source a significant portion of the link energy cost. To reduce the laser's electrical power consumption the Rx sensitivity should be improved while the optical path loss should be minimized. In Chapter-3, a high-sensitivity optical Rx is developed, which address a part of this problem. While in chapter laser-forwarded coherent link is demonstrated that greatly reduces the required laser optical power by averaging optical path loss between the main and the forwarded path, and by further improving the Rx sensitivity using a homodyne coherent detection. The link performance analysis reveals that the laser forwarded link improves the laser power budget by ≈6-8 dB compared to a conventional intensity-modulation/direct detection link using typical photonic link components. To demonstrate the laser forwarded link, a microring resonator phase-modulator, a balanced detector, and a 3-dB coupler are integrated with CMOS circuits in a GFUS 45nm SOI process. The transmit driver and the receiver consume 40 fJ/bit and 450 fJ/bit, respectively. Aided by ≈8 dB boost from laser forwarding and the coherent detection gain, the receiver achieves -15.6 dBm optical modulation amplitude sensitivity. The link operates at 10 Gb/s with bit error rate $<10^{-9}$ and electrical energy-efficiency of 2.3 pJ/bit.

4.1 Coherent Link for Short-reach Optical I/O

The IMDD link example discussed in Section-2.3 of Chapter-2, highlights the need for high optical laser power due to limited Rx sensitivity and optical path loss. While some techniques, as briefed in Chapter-3, can be used to improve Rx sensitivity, minimizing optical path loss is not always that straight forward and often involves tight trade-off with other important optical performance metrics like ER and voltage drive for a modulator. Addition-

aly, conventional IMDD links exploit only one degree of freedom, namely, optical intensity. Owing to these reason IMDD links reported in recent literature require 7-13 dBm of laser power [12, 36, 40].

Compared to IMDD, the coherent links enable complex modulation, such as binary phase-shift keying (BPSK), and thus, are more spectrally efficient. However, coherent detection often is costly, complex, and involves power hungry signal processing. Consequently, coherent links are thought to be not suitable for data center applications and are limited to long-haul and metro links. However, the benefits of coherent detection has forced researchers to innovate at architecture level and make deployment of coherent link possible within data center. One such effort is reported in [41]. Here the researchers identify that the short-reach optical I/Os of data centers have less severe fiber propagation impairments. These relaxed requirements can be exploited to dramatically simplify the signal processing and thus, reduce the power consumption and cost associated with coherent detection. While this new approach permits the use of coherent links in the data center, it still needs a local laser source. This is not feasible for high-bandwidth density applications such as optical I/O utilizing N-way DWDM. For instance, a 16-way DWDM shown in Fig. 2.5 of Chapter-2 would require 16 local laser sources per I/O ports. If there are multiple I/O ports, then the number of laser sources would scale further.

To address the limitations imposed by limited Rx sensitivity, optical path loss, and need for multiple local laser sources, this chapter discusses a laser-forwarded (LF) coherent link architecture for short-reach optical I/Os. The basic idea is to forward some portion of the laser power directly to the homodyne coherent Rx [19], bypassing the transmit chip IL. As the forwarded laser (LO at Rx) bypasses the major link losses, the overall photocurrent generated at the Rx is affected only by an average of the signal and LO path loss. Besides, it obviates the need for multiple local laser sources needed to realize DWDM Rx. Also, the homodyne coherent Rx improves the SNR due to a boost from the LO multiplication and a 3-dB SNR gain due to coherent balanced detection. The coherent modulator and demodulator are realized using MRRs as they are inherently wavelength selective and can realize DWDM without using additional components for multiplexing or de-multiplexing. This minimizes the IL, saves area, achieves higher bandwidth density, and improves energy-efficiency [23, 24]. While the use of MRR for coherent communication is well-known [68, 69], the key link components remain off-chip. This chapter presents the first results of an MRR-based LF SiPh BPSK link fully integrated in a zero-change 45-nm SOI CMOS. The Tx generates the 10 Gb/s BPSK data while being stabilized by an on-chip thermal tuning loop and clocked from a low-jitter digital phase-lock loop (DPLL). The Rx achieves an OMA sensitivity of -15.6 dBm enabled by an integrated 3-dB coupler and a balanced MRR-based photodetector (PD). Consequently, the demonstrated link requires less laser power compared to the state-of-the-art IMDD links.

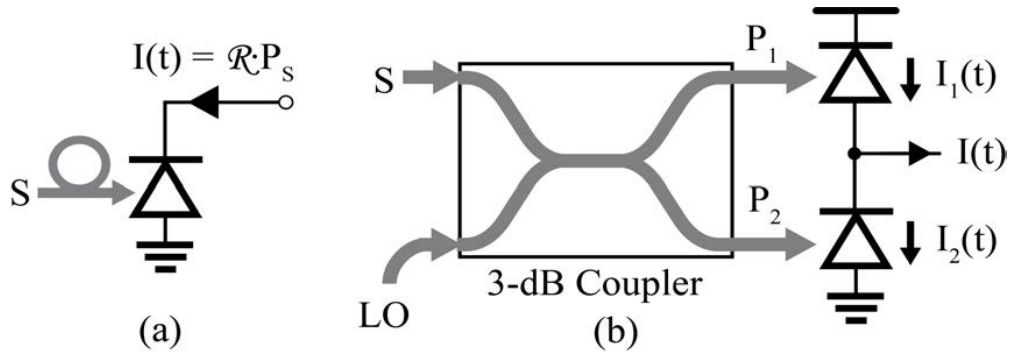


Figure 4.1: (a) Direct detection and (b) Coherent balanced detection.

4.2 Principle of Coherent Balanced Detection

A balanced detector is a key component of coherent homodyne Rx. To understand its operation, first, consider a direct detection as shown in Fig. 4.1(a). Here, a PD with responsivity $\mathcal{R}$ is illuminated with a monochromatic lightwave, $S = \sqrt{P_S}\exp(\mathrm{j}(\omega_\mathrm{L}\mathrm{t}+\phi_{in}(t))$, where ϕ_{in} is the phase of the signal S. The output photocurrent is given by,

$$I(t) = \mathcal{R} \cdot P_S \tag{4.1}$$

As the direct detection measures the average power ($|S|^2$=P_S), the phase information in (4.1) is lost. In contrast, a coherent detector of Fig. 4.1(b) retains the phase information. Here, a 3-dB coupler, also referred as a 180° optical hybrid, mixes the signal S with the LO ($=\sqrt{P_{LO}}\exp(\mathrm{j}\omega_\mathrm{L}\mathrm{t})$). Each of the two input fields splits into the two output ports and an additional phase-shift of 180° is introduced in one of the branches. Mathematically the operation of a 3-dB coupler can be modeled as,

$$\begin{bmatrix}\sqrt{P_1}\\ \sqrt{P_2}\end{bmatrix} = \frac{1}{\sqrt{2}}\begin{bmatrix}1 & 1\\ 1 & -1\end{bmatrix}\cdot\begin{bmatrix}S\\ LO\end{bmatrix} \tag{4.2}$$

Simplifying (4.2) states that the output optical power P_1 and P_2 are proportional to the sum and difference of the inputs S and LO. They are given by,

$$P_1 = (S + LO)^2/2 \text{ and } P_2 = (S - LO)^2/2 \tag{4.3}$$

The resulting photocurrents I_1(t) and I_2(t) are,

$$I_1(t), I_2(t) = \frac{\mathcal{R}}{2}\underbrace{(P_S + P_{LO}}_{\text{Unwanted DC term}} \pm 2\sqrt{P_S P_{LO}}cos(\phi_{in}(t))) \tag{4.4}$$

The DC terms in (4.4) increase the shot noise and can saturate Rx AFE, especially for a strong LO signal. A high-pass filter can eliminate these terms, but it deteriorates bit error rate (BER) as it filters the lower-end of the spectrum. Alternately, a DC cancellation loop

can be used [70]. However, the offset canceling current source requires a careful low-noise design as its thermal noise appears directly at the input degrading the Rx sensitivity. A better approach is to subtract the two photocurrents using a balanced detector formed by stacking two PDs as shown in Fig. 4.1(b). The output current is expressed as,

$$I(t) = I_1(t) - I_2(t) = 2\mathcal{R}\sqrt{P_S P_{LO}} \cdot \cos(\phi_{in}(t)) \tag{4.5}$$

There are no DC terms present in (4.5) and unlike (4.1) it retains the phase information that enables coherent detection. Also, a balanced detector has superior common mode rejection and adjacent channel suppression making it a good fit for co-packaged DWDM optical I/Os which operate next to an SoC with a noisy power-supply environment.

4.3 Laser-forwarded (LF) Coherent Link Architecture

The architecture of the LF coherent link using is shown in Fig. 4.2. A laser source outputs a continuous lightwave laser with wavelength λ_{L}, which is split between the signal path and the forward laser path. On the signal path, the Tx uses an MRR-based O-DAC to modulate the phase of incoming lightwave such that ϕ_{in} in (4.5) changes between 0 and π. At Rx, this results in a peak-to-peak signal current of $4\mathcal{R}\sqrt{P_S P_{LO}}$. In an LF coherent link, both the signal and LO are derived from the same laser source by splitting it with a factor k ($0< k <1$). Assuming the link loses of Fig. 2.4 in Chapter-2, the signal current is,

$$I(t)_{in}^{LF} = 4\mathcal{R} \cdot \sqrt{\alpha_T \alpha_C \cdot k(1-k)} P_L \tag{4.6}$$

where P_L is the laser power and α_{T} ($=\alpha_C^3 \alpha_{IL}$) is the signal path loss. The current in (4.6) is maximized for $k = 0.5$, suggesting an even split of laser power between the signal and the LO. A multi-port laser source with equal output power per wavelength per port would be an ideal fit for this purpose. Subsequently, for the same laser power the peak-to-peak signal current for LF and IMDD link is,

$$I(t)_{in}^{LF} = 2\mathcal{R} \cdot \sqrt{\alpha_T \alpha_C} P_L \text{ and } I(t)_{in}^{IMDD} = \mathcal{R} \cdot \alpha_T P_L \tag{4.7}$$

Comparing the two expressions in (4.7), the strength of LF architecture is evident. The signal current in an IMDD link is directly affected by the link loss, whereas in an LF link the signal current is affected by the geometric mean of the loss in the signal path and the LO path. Consequently, the gain of an LF coherent link over an IMDD link, can be expressed as,

$$A_{LF} = \frac{I_{in}^{LF}(t)}{I_{in}^{IMDD}(t)} = 2\sqrt{\frac{\alpha_C}{\alpha_T}} \approx 9 \tag{4.8}$$

For the same link components, the gain A_{LF} in (4.8) improves the SNR and thus, the Rx sensitivity or for the same Rx sensitivity reduces the laser power, . The three main reasons behind the gain A_{LF} are: 1) the 3 dB SNR gain due to coherent balanced detection as indicated by (4.5), 2) mixing with LO provides an optical gain of $2\sqrt{P_{LO}/P_S}$, and 3) averaging of the signal and the LO path link loss. Furthermore, a portion of the coupled LO laser power can be used for the return transmit link, avoiding the need for extra fiber to route the LO.

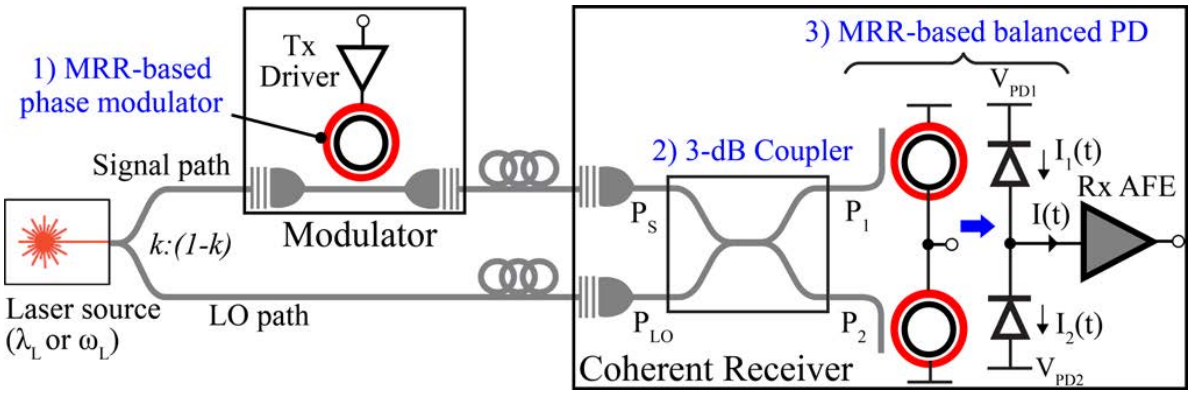


Figure 4.2: An MRR-based LF coherent link concept [19].

4.3.1 Coherent Rx sensitivity and Noise sources

A high sensitivity Rx AFE is necessary to support and preserve the SNR gains due to coherent balanced detection. Assuming balanced PDs have negligible dark current, the sensitivity of the Rx AFE is dominated by the PD shot noise and thermal noise from the AFE. The rms values of the shot noise ($\overline{i_{nS}}$) and the thermal noise ($\overline{i_{nT}}$) are given as,

$$\overline{i_{nS}} = \sqrt{2q\mathcal{R}P_i \cdot \Delta f} \text{ and } \overline{i_{nT}} = \sqrt{i_{n,TIA}^2 \cdot \Delta f} \tag{4.9}$$

where P_i is the total power hitting a PD, Δf is the AFE bandwidth, and $i_{n,TIA}$ is the one-sided total input-referred noise current density of the AFE expressed in pA/$\sqrt{Hz}$[71]. To achieve a target BER, the input signal currents of (4.7) should be much higher than the total rms noise. The relation between the two is given as,

$$BER = \frac{1}{4}\left[erfc\left(\frac{I_{in,pp} - 2I_{th}}{\sqrt{2}\sigma_{n1}}\right) + erfc\left(\frac{I_{in,pp} + 2I_{th}}{\sqrt{2}\sigma_{n0}}\right)\right] \tag{4.10}$$

assuming the ideal ER for the IMDD link. In practice additional shot and thermal noise are present at the Rx input due to ER (6-10 dB) and additional offset correction circuitry. Here, σ_{n1} and σ_{n0} represent total noise current for bit-1 and bit-0, respectively, while I_{th} models minimum receivable signal.

The values of σ_{n1} and σ_{n0} in (4.10) are given by,

$$\begin{aligned} \text{IMDD link: } \sigma_{n1} &= \sqrt{2q\mathcal{R}\alpha_T P_L \Delta f + \overline{i_{nT}^2}};\ \sigma_{n0} = \overline{i_{nT}} \\ \text{LF link: } \sigma_{n1} &= \sigma_{n0} = \sqrt{q\mathcal{R}(\alpha_T + \alpha_C) P_L \Delta f + \overline{i_{nT}^2}} \end{aligned} \tag{4.11}$$

The shot noise in an LF link is generated from two different PDs. Thus, their variance adds up as they are independent. Using the signal current of (4.7) and noise of (4.11) in (4.10), the BER plots for IMDD and LF link are obtained as shown in Fig. 4.3(a). Here, $\overline{i_{nT}}$=2.5

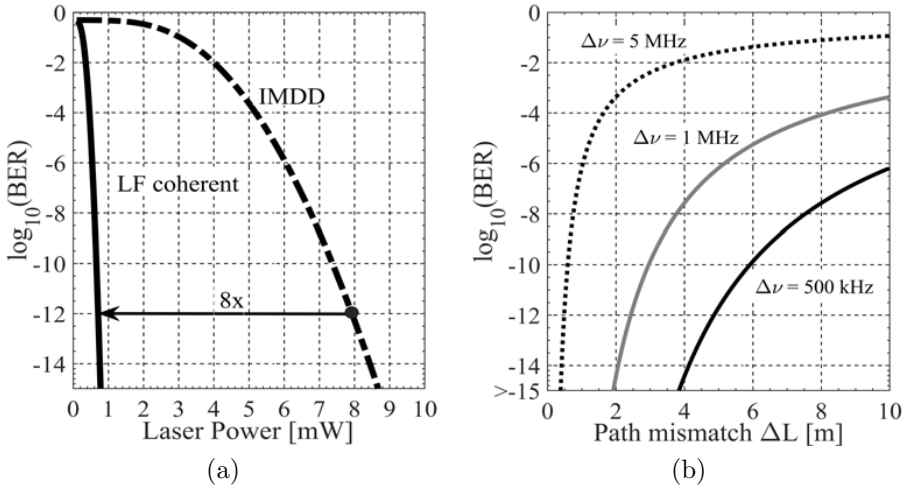


Figure 4.3: (a) BER vs. laser power. and (b) Impact of path length mismatch.

μA over 20 GHz bandwidth and I_{th}=7.5 μA are assumed [39]. The losses are the same as for a typical IMDD link (Fig. 2.4 in Chapter-2). As evident from Fig. 4.3(a), the LF coherent link meets the target BER at much reduced laser power. As the shot noise is included in Fig. 4.3(a), the reduction in laser power is slightly lower than that predicted by (4.8).

Further, instead of forwarding the LO, a conventional BPSK link derives LO using a local laser source. In this case, the peak-to-peak signal current is $4\mathcal{R}\sqrt{P_S P_{LO}}$, while the noise current $\sigma_{n1}(=\sigma_{n0})$ is $\sqrt{2q\mathcal{R}(\alpha_T P_S + P_{LO})\Delta f + \overline{i_{nT}^2}}$. Here, the LO power can only be increased to a point beyond which the generated shot noise will dominate the total noise. Any further increase in the LO power does not improve the SNR as it gets limited by the shot noise [72]. In contrast, SNR of an LF coherent link is proportional to P_L. Thus, increasing P_L will improve the SNR as long as the increase in the signal power stays within the MRR's power handling capability. After this point, it gets harder to phase-modulate and thermally stabilize the MRR. Lastly, the relative intensity noise (RIN) of the laser due to intensity fluctuations from spontaneous emission also affects the Rx sensitivity. However, as the noise variance of RIN is correlated between two output ports of the 3-dB coupler, the balanced detector rejects it and makes its contribution negligible [72].

4.3.2 Impact of Laser Phase noise

Laser phase noise, an inevitable aspect of a free running laser, is caused by random spontaneous emissions. In a practical LF link, the phase noise manifests itself through the path length mismatch ΔL between the signal and the LO path. When there is no path length mismatch, the LO is synchronous to the signal and the phase noise is canceled as it is perfectly correlated between the two paths. However, for finite path length mismatch the amount of phase noise influencing the link BER depends on ΔL and 3-dB linewidth $\Delta\nu$ of

the laser source. To estimate the effect of the phase noise on BER, the signal current under no modulation ($\phi_{in} = 0$) can be written using (4.5) and (4.6) as,

$$I(t)_{in}^{LF} = \mathcal{R} \cdot \sqrt{\alpha_T \alpha_C} P_L cos(\phi_n(\Delta t_p)) \tag{4.12}$$

Here, $\phi_n(\Delta t_p)$ is the net phase noise process related to the laser phase noise as $\phi_{nl}(t)$-$\phi_{nl}(t\text{-}\Delta t_p)$. Here, the propagation time difference $\Delta t_p = \Delta L/c'$, where c' is the velocity of light in an optical fiber (2.1×10^8 m/s).

The laser phase noise is a Weiner process defined as,

$$\phi_{nl}(t) = \int_0^t \dot{\phi}_{nl}(\tau)\,\mathrm{d}\tau \implies \phi_n(\Delta t_p) \sim \mathcal{N}\Bigg(0, \underbrace{\frac{4\pi}{3}\Delta\nu\Delta t_p}_{\sigma_n^2}\Bigg) \tag{4.13}$$

As $\phi_{nl}(t)$ is an integral of a zero-mean Gaussian process $\dot{\phi}_{nl}(t)$, its difference $\phi_n(\Delta t_p)$ is also a zero-mean Gaussian random variable with variance σ_n^2 as shown in (4.13) [72]. Consequently, $\phi_n(\Delta t_p)$ varies randomly and can potentially result in no signal current at all if it lingers close to $\pi/2$.

Since the exact method of determining BER for the LF link in the presence of phase noise is rather complex, a simpler upper bound on BER can be obtained by noting that a ONE is detected for a ZERO being transmitted if the phase noise $\phi_n(\Delta t_p) > \pi/2$. Thus, the BER is given by [72],

$$\begin{aligned} BER &= Pr\left[\phi_n(\Delta t_p) > \frac{\pi}{2}\right] \\ &= erfc\left(\frac{\pi}{\sqrt{8}\sigma_n}\right) = erfc\left(\sqrt{\frac{3\pi c'}{32\Delta\nu\Delta L}}\right) \end{aligned} \tag{4.14}$$

Fig. 4.3(b) plots the upper bound on BER as given by (4.14). As expected, the BER deteriorates as laser linewidth and path length mismatch increases. For a typical distributed feedback (DFB) laser used in data-com applications with a linewidth of 1 MHz, a maximum of 2.5 m of path-length mismatch can be tolerated while maintaining a BER of 10^{-12}. Simulations suggest this causes the gain of LF link over IMDD link to reduce from 7.6x in Fig. (4.3)(a) to 3.8x (∼6 dB). The BER bound of (4.14) can be improved by compensating for the path-length mismatch using a phase tracking closed-loop at the Rx [19]. In practice, the typical path length mismatch should be less than this since the laser module can be co-located either on the same shelf or the same rack as the Tx chip.

4.4 Optical Blocks in Monolithic Si-Ph platform

The LF link uses crystalline silicon (c-Si) waveguide, grating couplers (GC), optical-DAC based MRR phase modulator, 3-dB coupler, and balanced MRR PDs. These devices along

with the transceiver circuits are fully integrated in a monolithic SiPh platform based on a 1P11M GFUS 45-nm SOI CMOS process. Realization and the salient features of this platform are detailed in [28, 16]. Its key aspect is the ability to integrate photonic devices microns away from CMOS circuits. This improves overall system performance by minimizing routing parasitic and enabling dense functional integration. Additional chip assembly steps for packaging and fiber coupling are outlined in [7, 18] while the substrate release process used is as described in Section-2.4.3 in Chapter-2.

4.4.1 MRR-based Optical-DAC (O-DAC) phase modulator

An MRR-based modulator is essentially a PN diode formed by interleaved P-N junction phase shifters along the circular MRR cavity [73]. Using this modulator an O-DAC is realized by segmenting the phase shifters and driving each of the segments independently [45]. The carrier density in the cavity can be controlled by the number of segments being depleted, which linearly varies the effective refractive index (η_{eff}). Consequently, the resonant wavelength shifts which change the phase of the optical output. To quantify the effect of change in η_{eff} on the amplitude and phase the ratio of transmitted (E_2) and the incident (E_1) optical field in Fig. 4.4(a) can be used. Depending on the transmission (t) and coupling (k) coefficients, a part of E_1 is transmitted as E_2 while the other is coupled into the MRR cavity. This relationship is derived in Chapter-2 and repeated below for clarity,

$$\frac{E_2}{E_1} = \frac{t \cdot e^{-i\theta} - a}{1 - ta \cdot e^{i\theta}} \cdot e^{i\theta}, \text{ where } \theta = \frac{2\pi\eta_{eff}L}{\lambda_L} \tag{4.15}$$

Here, L is the round trip length of the MRR cavity, a is the round-trip amplitude transmission that relates to the propagation loss α [cm^{-1}] by $e^{-\alpha L/2}$, and t is the transmission coefficient. Any change in η_{eff} changes the imaginary part of (4.15) strongly impacting the phase of E_2. It can be written as,

$$\phi = \pi + \theta + atan\left(\frac{tsin\theta}{a - tcos\theta}\right) + atan\left(\frac{tasin\theta}{1 - tacos\theta}\right) \tag{4.16}$$

The shape of phase response in (4.16) depends upon the relation between t and a. For $t = a$ (critical coupling) the phase response of E_2 abruptly shifts by π near resonance, while for $t > a$ (under-coupled) the phase response is not monotonic and turns negative near resonance. However, a continuous and positive phase shift is necessary for phase modulation, which only over-coupled ($t < a$) MRRs can exhibit [74]. This condition is met for the O-DAC by appropriately designing the gap between the MRR cavity and the bus waveguide [45].

In [45], it is proven that O-DAC has better linearity and lesser complexity than its electrical counterpart. As shown in Fig. 4.4(a), O-DAC segments are created by simple wiring of the interleaved P-N junction phase shifters. All the anode contacts are tied to V_{Mod}, while the cathodes are driven individually. Controlled by bits *En0* to *En15*, the inverter-based modulator driver either depletes the P-N junction segment by connecting it to the ground or removes it by connecting it to AV_{DD}. Thus, as shown in Fig. 4.4(b),

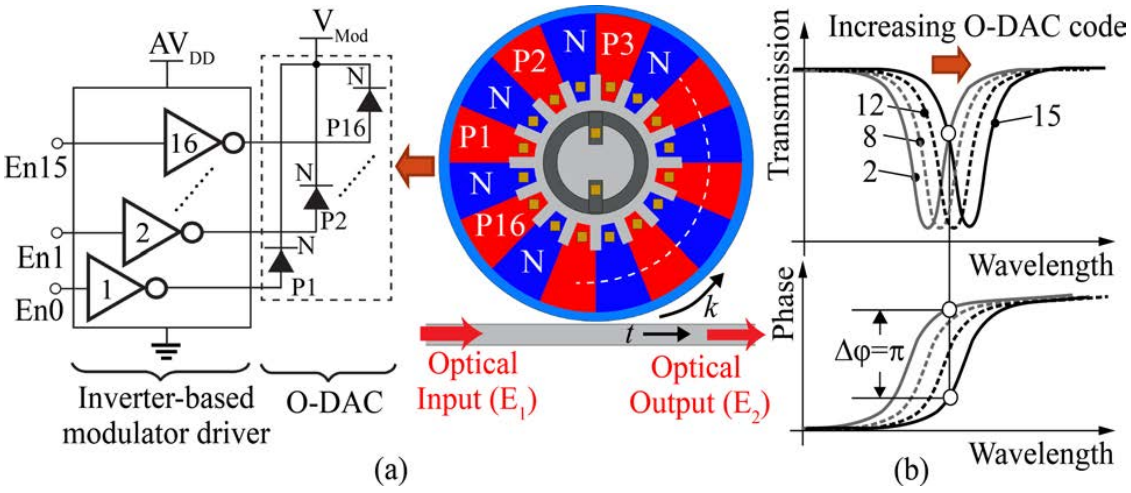


Figure 4.4: (a) MRR based O-DAC (b) Phase shift with O-DAC code.

increasing the O-DAC code from 2 to 15 changes the carrier concentration in the MRR cavity, which induces a change in η_{eff} due to carrier plasma dispersion effect. This results in shifting the transmission to the right and thus, changing the phase response as given by (4.16). Since the carrier injection modulators are slow, the O-DAC is operated in depletion mode by ensuring strong reverse biasing i.e. $V_{Mod} > AV_{DD}$. A 32 segment (32 anodes and 32 cathodes) O-DAC is used, while the upper limit set by the design rules for minimum allowed doping regions width is 64.

Lastly, an important consideration while driving the O-DAC is to operate it in depletion mode. As in the carrier injection mode, electron/hole carriers are injected into the intrinsic region of the O-DAC, its speed limited by the minority carrier lifetime. Subsequently, the require pre-emphasis drive for high data rate operation. Besides, they consume static power and show lower energy-efficiency due to forward-bias operation. In contrast, operating O-DAC in carrier-depletion mode avoids these issues as it only depletes the carriers from the O-DAC cavity.

4.4.2 Coherent Balanced Detector

The key blocks required to realize a coherent balanced detector are a 3-dB coupler and MRR-based balanced PDs. Figure 4.5(a) shows the structure of the adiabatic 3-dB coupler [15]. The light is coupled into a grating coupler (GC) with teeth designed using c-Si and poly-silicon layers to achieve low-loss and high-directivity. The GCs at port-1 & 2 have a bandwidth of 78 nm and a coupling loss of 4 dB [43]. A c-Si taper directs the optical modes into the adiabatic coupler. The adiabatic coupling is achieved by placing the two waveguides close enough as permitted by the process rules, which is 120 nm for this work. The initial widths W_1 and W_2 gradually tapered over a length of 400 μm such that the fundamental mode is maintained until the tapered waveguide widths are equal to 0.4 μm. At this point,

the optical power is evenly divided in the two output waveguides which are then quickly separated resulting in the optical power at the port-3 (P_1) & 4 (P_2) as given by (4.3). The parameters W_1, W_2, and L are determined using mode solver simulations.

Figure 4.5(b) shows the structure of an MRR-based PD. The c-Si cavity of the MRR is evanescently coupled to the bus waveguide. At resonance, the optical power in the MRR cavity constructively interferes with the input causing the power in the MRR cavity to be much higher than in the input bus waveguide. This optical power is converted to photocurrent by placing interleaved p-i-n junctions along the perimeter of the MRR cavity. The resulting detector has much higher responsivity in an extremely compact form factor. A typical MRR PD using 5 μm radius cavity has a responsivity of >0.5 A/W with >5 GHz bandwidth, and <20 fF capacitance [44, 18]. To effectively separate the optical field concentrated in the outer half of the ring, the metal contacts are placed in the center and connected with metal spokes. The structure of MRR PD is similar to an O-DAC except for an SiGe absorption region that is responsible for carrier generation. To avoid crystal dislocations, the SiGe layer is heteroepitaxially grown within a 0.5 μm wide partially etched trench [58]. The 30 lateral P-N junctions use the same n-type and p-type implants as source/drain. Spokes of n-type and p-type are used to connect the P-N junctions with their respective contacts in the center of the ring. An MRR PD designed in this manner is used to realize a balanced PD in Fig. 4.5(c) by stacking two PDs and appropriately wiring them. The process-induced mismatch in the resonance of the two PDs is tuned out by an integrated heater shown in Fig. 4.5(c). The mean value of the heater resistance measured over 20 test sites is 353.4 Ω with 10.65 Ω deviation [20].

4.5 Transceiver Implementation

4.5.1 BPSK Transmitter Circuits

The architecture of the BPSK Tx consists of a data-path, clock-path, and a thermal tuning loop as shown in Fig. 4.6(a). In this work, a previously reported design is re-used [45]. The two PRBS-31 blocks generate the transmit bits, which later are received and checked by the Rx digital backend to compute the link BER. An inverter-based modulator driver, chosen for its energy efficiency, drives the 16 individual anode segments in a thermometric manner leading to a 4-bit binary O-DAC. These 16 codes are mapped such that the driver depletes zero to all P-N junctions. Out of these 16, the two specific codes yield phase shift keying while keeping intensity nearly constant. These two codes are stored in the LUT through scan registers. All the cathode segments are shared and connected to 2 V DC.

The transmission spectrum of an MRR drifts as much as 0.036 nm (or 7 GHz/K) for 1 Kelvin temperature change. This drift in intensity induces equivalent phase drift $\Delta\phi_{\text{drift}}$ as shown in Fig. 4.7(a). An optical transceiver co-packaged with a switch ASIC experiences even higher thermal drifts resulting in higher $\Delta\phi_{\text{drift}}$. Hence, a closed-loop thermal tuning to stabilize the MRR modulator is realized in Fig. 4.6(a) using a weakly coupled drop-port

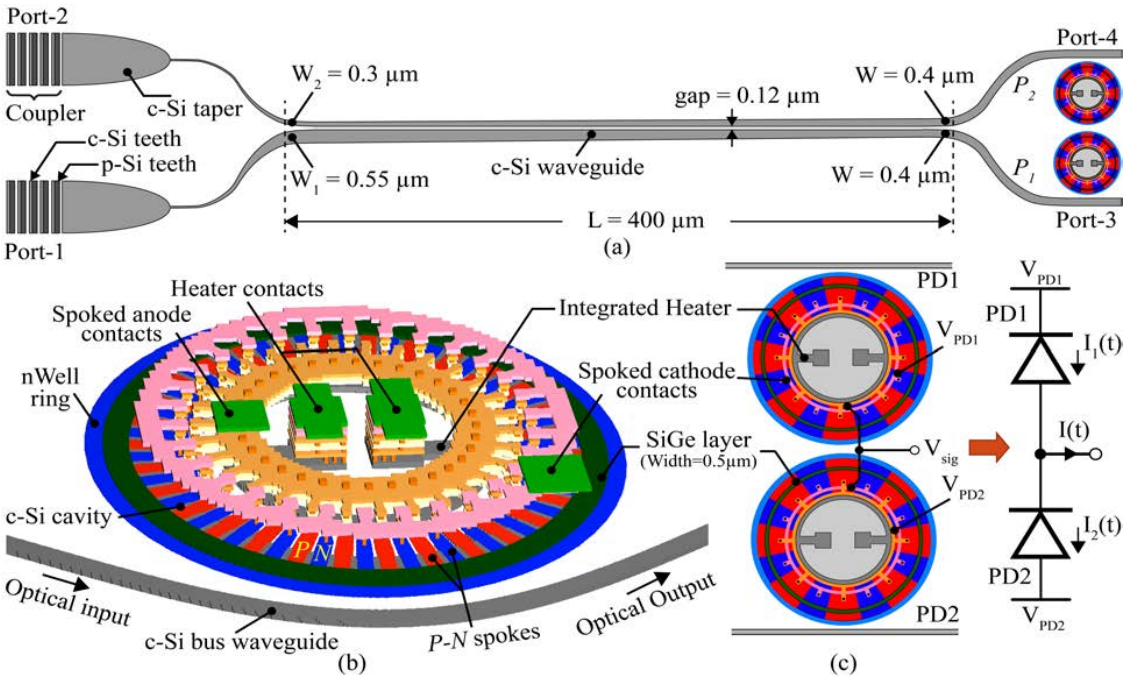


Figure 4.5: (a) Integrated 3-dB adiabatic directional coupler (b) 3D layout of an MRR PD (c) Balanced PD realized using a stack of two MRR PDs.

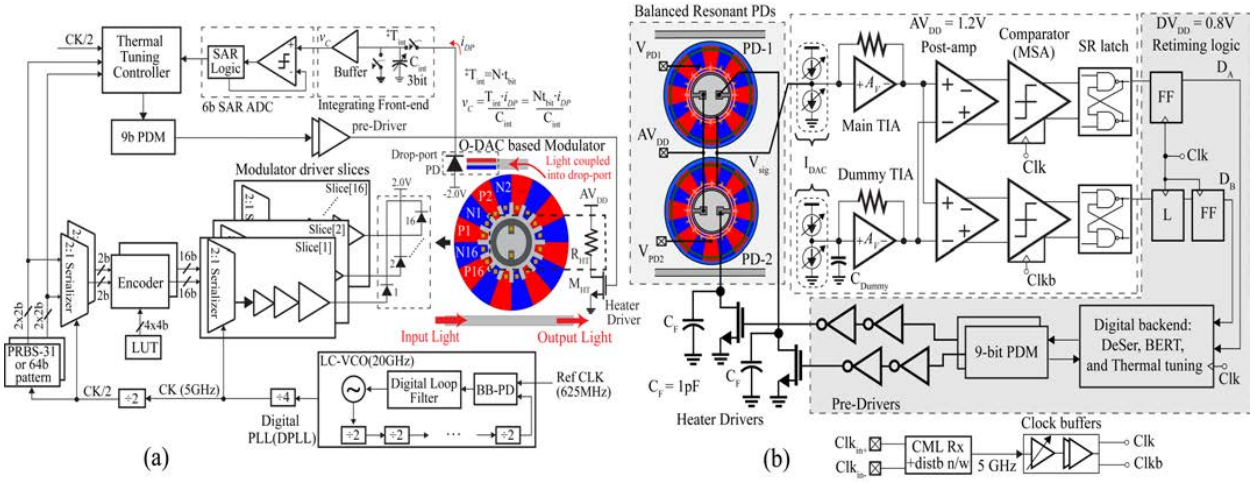


Figure 4.6: Architecture of (a) BPSK transmitter (Tx) and (b) coherent receiver (Rx).

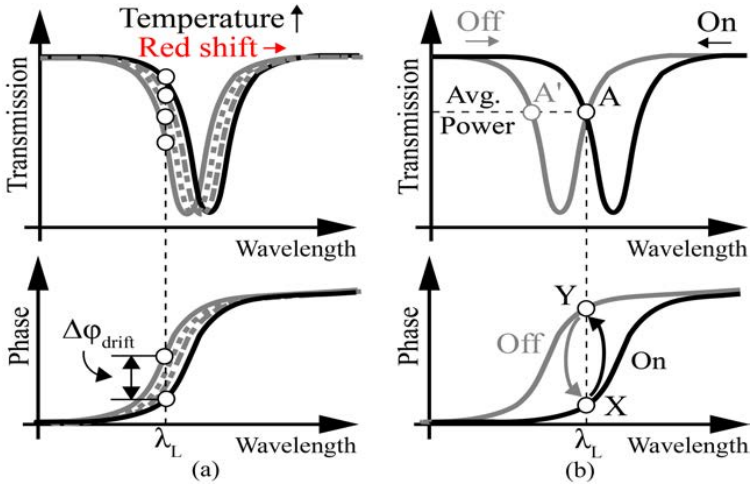


Figure 4.7: (a) Phase drift due to thermal variations (b) operation of the thermal tuning controller

with a linear PD and an integrated c-Si heater. The drop-port senses a small fraction (≈1%) of the cavity optical power, and the linear PD converts it to the photocurrent i_{DP}. It is then integrated on a capacitor C_{int} over an interval of N symbols. A 6-b SAR ADC quantizes the voltage across C_{int}, v_C ($=Nt_{bit}.i_{DP}/C_{int}$), and generates the input for the thermal tuning feedback loop. The voltage v_C is measured at two time instances t_1 and t_2. The goal of the loop is to make $v_C(t_1)=v_C(t_2)$. At this point, the loop has reached a steady-state and the cavity is locked to average optical power. Intuitively, as shown in Fig. 4.7(b), the laser wavelength λ_L is parked on the left of the resonance where the MRR is thermally stable. While transmitting a bit the transmission spectrum slides downwards moving point A to A'. Equivalently, the phase of the MRR transitions from point X to Y. In steady-state, the loop locks the MRR at point A.

The clock path of the Tx in Fig. 4.8 is based on a DPLL that generates 5 GHz clock using a digitally controlled LC oscillator (LC-VCO). The DPLL uses a bang-bang phase detector (BB-PD) and a digital loop-filter with delta-sigma modulation, both designed using automated Berkeley Analog Generator [75]. The measured tuning range of the DPLL is 16-22GHz while the random-jitter is $<2\text{ps}_{\text{rms}}$. The phase-noise measured is <-141 dBc/Hz at 1 MHz offset.

4.5.2 Coherent Receiver AFE Circuits

Figure 4.6(b) shows a pseudo-differential half-rate architecture of the coherent Rx. The clock path comprising CML receiver and clock distribution circuit provides a 5 GHz low-jitter off-chip clock. The Rx AFE output bits D_A and D_B are retimed and processed by the digital backend. The Rx AFE circuits and the digital backend is similar to that described in Section-3.7 of Chapter-3. The single-ended output of the balanced PD is amplified by the

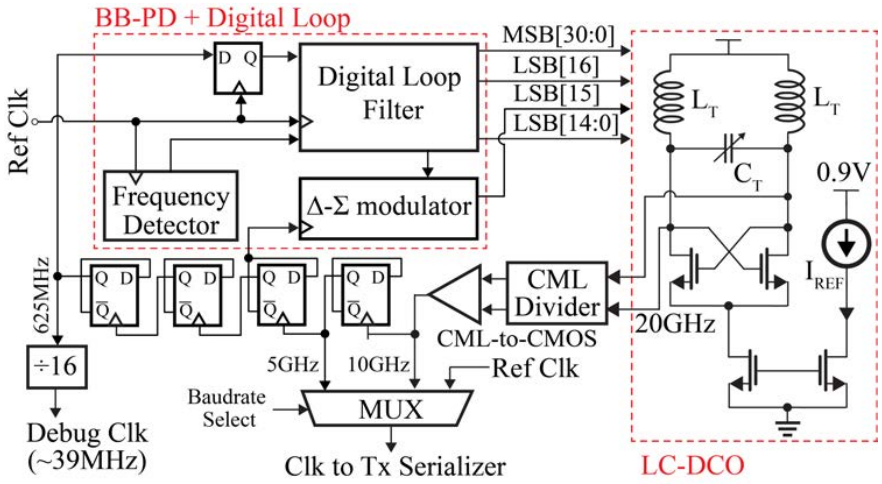


Figure 4.8: Block diagram of Tx clock path and bang-bang DPLL.

main TIA and converted to the differential by the post-amplifier. A dummy TIA is used to ensure equal input common-mode on both terminals of the post-amplifier. This combined with a dummy capacitor C_{Dummy}, that matches the PD junction capacitance, improves the supply noise immunity at the cost of degraded Rx sensitivity due to increased noise power. The two identical and independent thermal tuners tune the resonance of the balanced PDs. A 9-bit pulse density modulator generates pulses depending on the input control word over a fixed 0.17 ns period. These pulses are averaged by the 67 kHz cutoff low-pass thermal impulse response. Similar to [18], the on-chip thermal tuning circuit is driven by an off-chip tuning algorithm that locks the two PDs to a target wavelength. The heater drivers are capacitively loaded to reduce the output slew-rate.

4.6 Realization and Experiment Results

Figure. 4.9 shows the die-photo of the test chip and highlights key sub-blocks. It contains multiple Tx and Rx test sites, and standalone photonic test structures. As evident from Fig. 4.9, the photonic blocks and CMOS circuits are closely integrated with a reasonable footprint. The test-chip is flip-chip attached to the FR4 board using 50 μm C4 bumps [18]. The Tx circuits are powered from 1.0 V/1.5 V while the Rx circuits are powered from 0.8V/1.2V power supply.

4.6.1 Measurement of Standalone Rx and Tx chips

The balanced PDs are biased such that both have an equal reverse bias of 2 V. This ensures the two PDs are well matched and avoids Rx sensitivity degradation due to offset from PD mismatch. As shown in Fig. 4.10(a), the on-chip 3-dB coupler operates with a 50:50 coupling

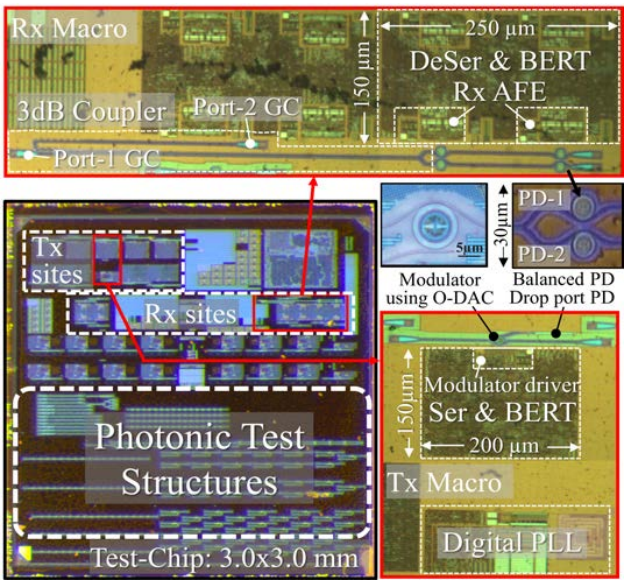


Figure 4.9: Structure of a conventional single-ended *(SE)* optical receiver (RX).

ratio only over a limited range of wavelengths. At 1272.5 nm it is exactly 50:50 with ∼0.6 dB excess loss and ≤3.2 dB IL. Hence, the resonance of balance PDs and the O-DAC are thermally locked to 1272.5 nm. Figure 4.10(b) shows the BER plots of a standalone RX at 10 Gb/s and 6 Gb/s. It is characterized using a reference $LiNbO_3$ phase-modulator. The bathtub curves are wider for higher LO power as it improves the eye-opening at the Rx input. The OMA sensitivity measured at 10 Gb/s was -15.6 dBm OMA. Figure 4.11(a) shows the Tx eye de-modulated using an off-chip 3-dB coupler at 10 Gb/s before being thermally stabilized. The O-DAC operates in the depletion mode with 2.0 V reverse bias. It has a Q-factor of ∼6K and is driven by 1.5 V swing. The BPSK eye is maximized when the difference between P_1 and P_2 (Fig. 4.2) is maximum while their sum is minimum. This is achieved by switching O-DAC between code 2 and 15 at an IL of 7 dB. The resulting Tx optical eye is shown in Fig. 4.11(b) after being thermally stabilized using an on-chip thermal tuning loop. The measured jitter is ∼2 ps_{rms} when Tx is clocked from the DPLL .

4.6.2 Laser Forwarded Coherent Link Demonstration

Figure 4.12 shows an LF coherent link set up between a Tx and an Rx chip. The laser source with a linewidth of 500 kHz is used. Its output power is split using an off-chip fiber-coupler (FC) between the signal (P_S) and the LO path (P_{LO}). Polarization controllers (PC) adjust the polarization to match the input polarization of the grating couplers. Lensed fibers are used to couple light in and out of the Tx/Rx chips and are secured using fiber trays to avoid mechanical disturbance. Figure 4.12 also shows optical power at key nodes due to various link losses. Comparing the signal power at node (6) and (7) a signal boost of 8.7 dB is

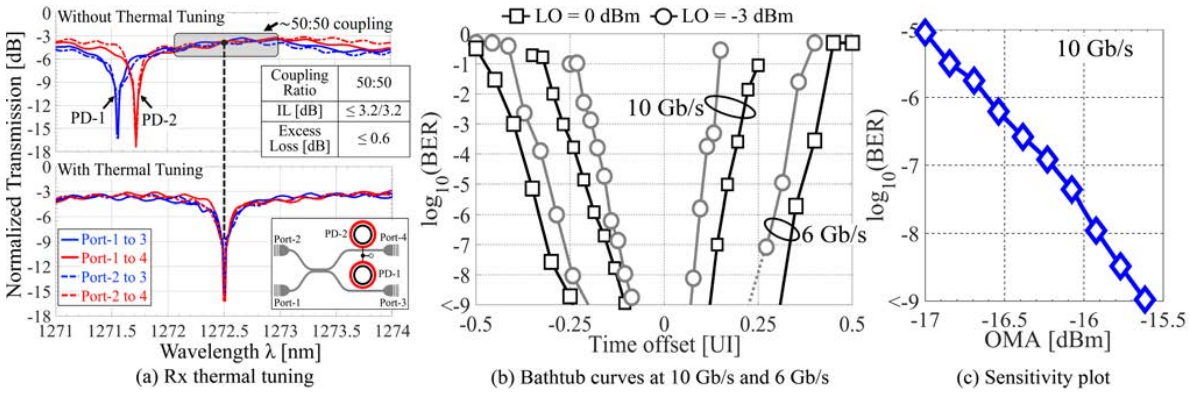


Figure 4.10: Characterization of standalone coherent Rx using an external $LiNbO_3$ phase modulator.

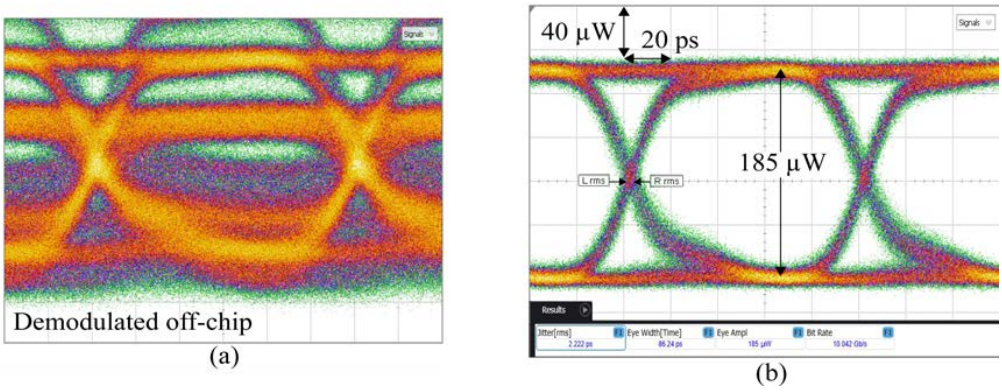
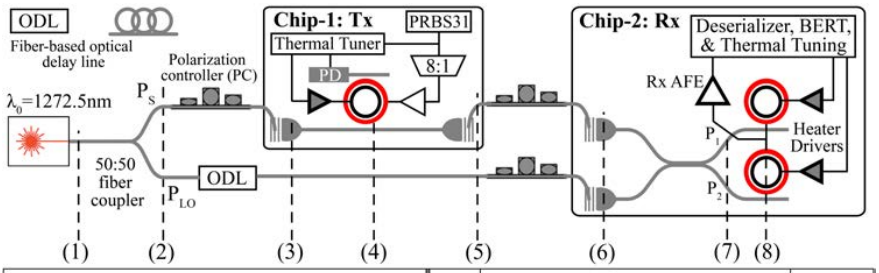


Figure 4.11: Measured 10 Gb/s Tx eye (a) before and (b) after thermal stabilization

evident due to mixing with LO. To improve link margin the O-DAC is biased at 3 dB IL.

Compared to the *LO* path, the signal path has two extra lensed fibers to couple light in and out of the Tx chip. The resulting path-length mismatch is compensated using a simple single-mode fiber (SMF) based delay line instead of the manual free-space optical delay line in [17]. Besides, the BER at an attenuated *LO* power of -3 dBm is measured by replacing the 50:50 coupler with 75:25 coupler and reducing the laser power instead of using an optical attenuator. Owing to these two simplifications, the fluctuations in the received eye are greatly subdued which improves the BER performance from 10^{-7} [17] to 10^{-9} in this work.

Figure 4.13(a) shows a setup that compares photocurrent generated in an IMDD and an LF coherent link for a fixed 4 dBm laser input with no modulation applied. As shown in Fig. 4.13(b), a peak current of 17.5 μA is generated in an IMDD link while a peak current of ± 45 μA is generated in the LF link. In the LF link, the residual path-length mismatch is a source of two nonidealities. First, as explained in Section-4.3.2 and evident from Fig. 4.13(b), the



Optical Loss Budget (Values in dBm)			Node	Parameters	P_S/P_{LO}
Node	Parameters	P_S/P_{LO}	(5, 6)	GC coupling loss of 4 dB	-15/-4
(1)	Laser power P_L = 4 dBm	–	Output of the 3-dB Adiabatic coupler		P_1/P_2
(2)	FC excess loss of 1 dB	0/0	(7)	3-dB coupler excess loss of 0.6 dB	-6.3/-9.3
(3)	GC coupling loss of 4 dB and VOA of 0.5 dB	-4/0	Responsivity of PD-1 & 2 = 0.35 A/W		
(4)	Modulator IL of 3dB	-7/0	(8)	Balanced PD photocurrent	45 μA

Figure 4.12: Optical setup to demonstrate LF coherent Tx-to-Rx link loop-back.

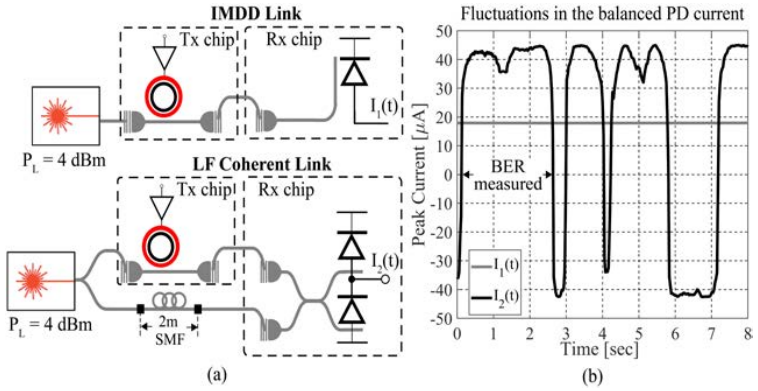


Figure 4.13: (a) Test setup to compare IMDD and LF links (b) Comparison of generated photocurrent under no modulation.

laser's accumulated phase noise and slow frequency drift manifests through the path-length mismatch. This cuases peak-to-peak fluctuations in the balanced PD photocurrent. Second, the path-length mismatch induces a static phase-shift $\Delta\phi$ that limits the amount of peak current to $I_{max} \cdot cos(\Delta\phi)$, where I_{max} is the peak current as estimated by (4.6) (for k=0.5). Consequently, the LF gain A_{LF} reduces from 9×, as estimated by (4.8), to 5.2× in Fig. 4.13(b). The addition of a low-speed phase tracking loop can fix the static phase offset, frequency fluctuations and in part filter-out some of the accumulated phase-noise due to the path length mismatch [19].

Figure 4.14 shows the BER of the LF coherent link measured at 10 Gb/s. The photocurrent in Figure 4.13(b) is only stable during a window of time-interval. Measuring BER during these intervals can give a good idea about the link's BER performance. This can be achieved by continuously measuring BER in real-time with the clock and the Rx threshold

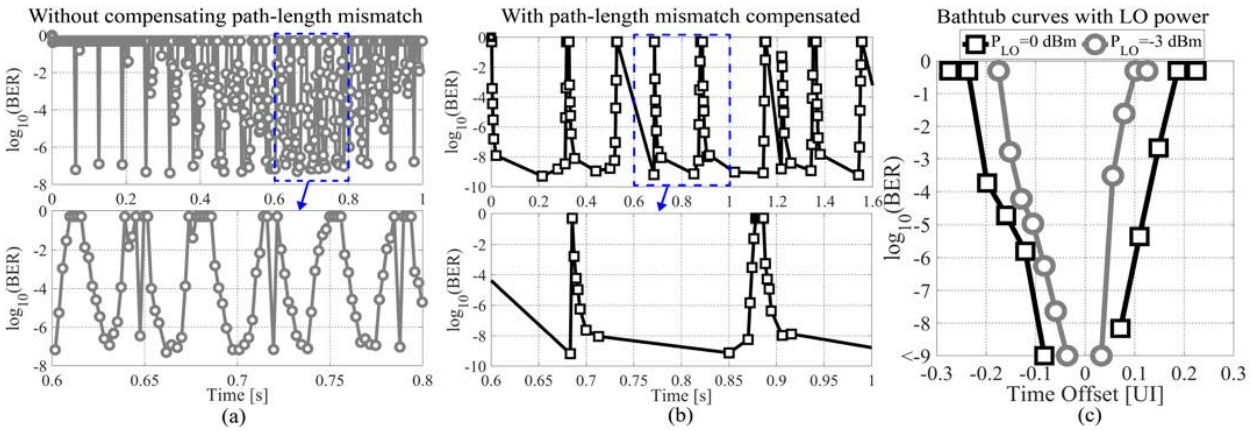


Figure 4.14: Measured at 10 Gb/s: BER at fixed offset (a) without and (b) with path-length mismatch compensation, (c) LF coherent link bathtub curves with *LO* power. The *LO* power is attenuated from 0 dBm to -3 dBm while keeping the signal power constant. The simplest means to achieve this without adding additional components to the optical bench is to replace 50:50 coupler with 75:25 and scale down the laser power to keep signal power the same.

fixed at an offset where the lowest BER is expected. Figure 4.14(a) and (b) shows BER measurement results with such an approach. Each BER point has 2 ms readout overhead. When the path-length mismatch is not compensated (SMF is removed), the fluctuations are more rapid which limits the BER measurement to 10^{-7}. When the path-length mismatch is compensated the fluctuations are a bit more stable allowing a 10^{-9} BER measurement. As the BER is measured in real-time, it is inversely proportional to the time difference between the two points. For example, in the zoomed plot of Fig. 4.14(b), the between time point 0.72 s and 0.85 s, the BER is being continuously measured. For measuring a further lower BER of 10^{-12} at 10 Gb/s, the photocurrent in Fig. 4.13(b) should be stable for more than 100 secs, which can be only achieved by adding a phase tracking loop. Figure 4.14(c) shows the LF link bathtub curves at the Rx chip for the data received from the Tx chip. Due to improved test-setup, the timing margin of these curves is wider than in [17].

Lastly, Fig. 4.15 breaks down the energy consumed by each LF link sub-blocks. Among the Tx circuits, the DPLL consumes the most power as it is designed to support data rates up to 40 Gb/s, while at the Rx end the Rx AFE consumes the most power amounting to 450 fJ/bit. The Tx modulator driver consumes only 40 fJ/bit. With 1.2 mW/nm tuning efficiency, the Tx thermal tuner shifts the O-DAC resonance by 0.5nm while the Rx tuner shifts the PDs resonance by 1 nm consuming a total of 290 fJ/bit. A thermal cross-talk of 20% is also observed between the two PDs which helps to reduce the power required by the tuners. The total energy efficiency of the LF coherent link including Tx, Rx, thermal tuners, and clocking, is 2.3 pJ/bit. Table-4.1 summarizes the performance of the LF coherent link and compares it with other state-of-the-art optical links. As apparent, this work is

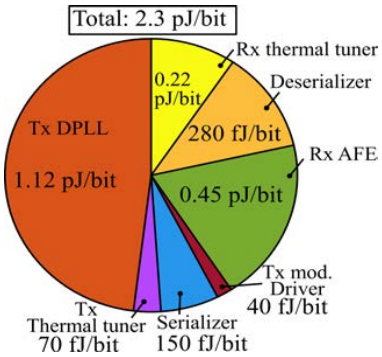


Figure 4.15: Electrical energy-efficiency breakdown at 10 Gb/s.

the only BPSK transceiver reported in recent literature that is fully integrated in a SiPh platform. Unlike [68] and [28], this work does not require any external off-chip components like an optical amplifier. The link achieves a comparable BER of 10^{-9} while operating at 10 Gb/s. Owing to >8 dB LO boost and coherent SNR gain, the Rx achieves -15.6 dBm OMA sensitivity, which is significantly higher compared to prior works. As a result, the link operates with 4 dBm laser power, which is 3 dB [12, 40] and 9 dB [36] lower. Optimization of SiPh devices particularly coupling loss of GC and implementation of a closed-loop phase tracking in future designs are expected to improve the link BER performance while further lowering the required laser power. In addition, the architecture of the LF link is compatible with commonly used Tx/Rx-side equalization schemes, which can be employed for faster data-rate operation and further improving Rx sensitivity.

4.6.3 Comment on closed-loop phase-tracking

In general, coherent demodulation requires local generation or some form of extraction of the carrier phase. Any noise or error in tracking the carrier phase leads to the degradation of SNR. The results are shown in Fig. 4.13(b) and Fig. 4.14(a)-(b) are indicative of this effect. Here, the fluctuations in the Rx eye caused by laser phase-noise degrades the BER. However, owing to laser-forwarding architecture these drifts are slow as shown in Fig. 4.13(b). A simple phase tracking loop realized on the Rx-side can fix for these drifts and stabilize the Rx eye. As the fluctuations in Fig. 4.13(b) are slow, a simple thermal tuning based phase-shifter can correct the phase errors. Besides, the thermal tuning based phase-shifter can have a much wider tuning range. A conceptual diagram of one such loop is shown in Fig. 4.16, where the phase shifter is realized in the LO path. It appears similar to a traditional clock recovery loop but operates at much lower bandwidth.

Figure 4.17(a)-(b) shows the drift in the output photocurrent of a balanced detector when an independent laser source is used as LO and when it is laser-forwarded. The use of a local laser source is commonly employed in conventional BPSK links. Here, as evident from Fig. 4.17(a), the current flips within <1 μs, while the same in LF coherent link takes about 5

Table 4.1: Comparison with recently reported monolithic SiPh optical links that do not need an external optical amplifier.

Reference		**This Work**	**[12] HOTI'17**	**[36] VLSI'18**	**[40] VLSI'19**
Integration		Monolithic	Monolithic	Hybrid	Hybrid
Tech-nology	**CMOS**	45nm SOI	45nm SOI	14nm FinFET	16nm FinFET
	SiPh	CMOS	CMOS	28nm SOI	GeSi SOI
Modulation		BPSK	NRZ	NRZ	NRZ
Data Rate		10 Gb/s	8 Gb/s	32 Gb/s	50 Gb/s
BER/ PRBS [bits]		10^{-9}/31	10^{-10}/31	$<10^{-9\dagger}$/7	10^{-12}/7
Wavelength		1272 nm	1270 nm	1330 nm	1570 nm
Modulator ER		5 dB	5 dB	4.2 dB	>3 dB
PD capacitance		20 fF	20 fF	30 fF	90 fF*
PD Responsivity		0.35A/W	0.5 A/W	0.9 A/W	1 A/W
Rx OMA sensivity [dBm]		-15.6	-11.7†	-10.3	-10.9
Efficiency [pJ/bit]		2.3	2.6	0.23‡	3.16
Min. Link Laser power		4 dBm	7 dBm	13 dBm	7.5 dBm†

†Estimated from plots or data given. ‡TIA+Tx driver only.
*Includes ESD and bump capacitance.

μs. This is a crucial differentiator, as the bandwidth of phase tracking loop required for conventional BPSK link is in the order of few GHz [76], while that with LF coherent link will be in the order of few kHz [19].

4.7 Summary

In the pursuit to lower the electrical power consumed by the laser source, this chapter described a laser forwarded coherent link for short-reach optical I/Os. Its effectiveness is analyzed and proven experimentally. The phase-modulators and coherent homodyne detectors are realized using microring resonators. The LF link reduces the required laser power by improving Rx sensitivity and averaging the optical link losses. The photonic devices and transceiver circuits are fully integrated in a 45-nm SOI monolithic SiPh platform making the LF link suitable for dense co-packaged optical I/Os. A 10 Gb/s BPSK link between a Tx and

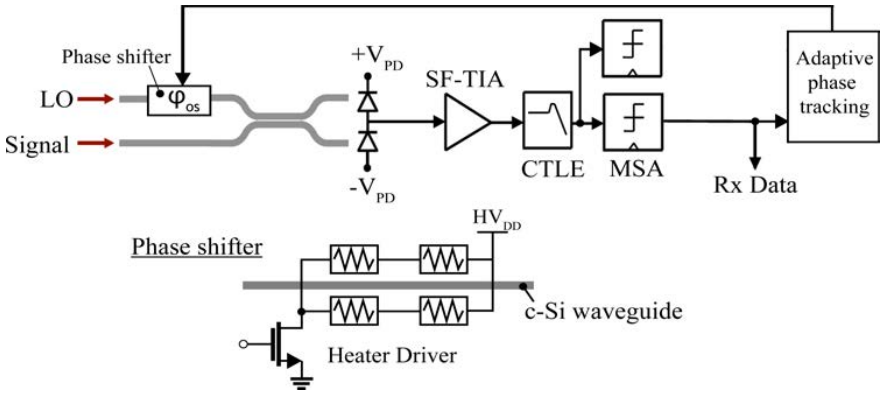


Figure 4.16: Block diagram of a phase tracking loop.

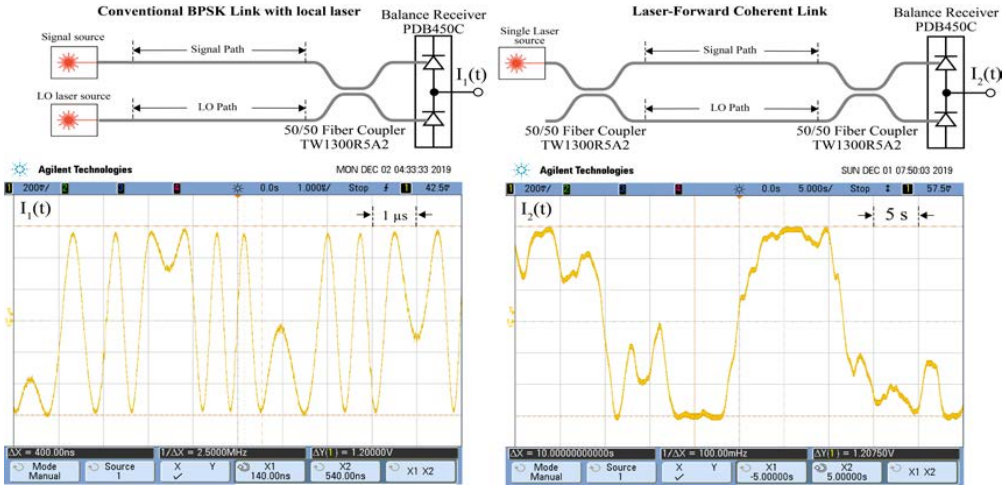


Figure 4.17: Drift in the output of a balanced detector when the LO is (a) derived from an independent local laser source, and (b) when the laser is forwarded.

an Rx chip is demonstrated. The overall link BER performance was limited by slow fluctuations in the received eye due to phase-drifts. This can be addressed by a closed-loop phase tracking loop. The LF link architecture can be readily scaled to support higher-order modulation that relaxes the energy bottle-neck imposed by laser sources and further improving the link energy-efficiency.

Chapter 5

Optically Sampled ADC: Architecture and Circuit Implementation

Consistent with the primary goal of this thesis, another system benefiting from the close integration of CMOS circuits with SiPh is the optically-sampled analog-to-digital converter (O-ADC). This chapter discusses the architecture and circuit implementation of O-ADC. The sampling clock jitter is one of the many limitations with conventional CMOS high-bandwidth ADCs. By moving the sampling function into the optical domain O-ADC addresses this problem. The optical clock sources such as a mode-locked laser (MLL) can generate very narrow optical pulses with jitter <10 fs_{rms} [77, 78]. The architecture of O-ADC is such that it not only enables optical sampling and electronic quantization, it is also integration friendly. The architecture tradeoffs, benefits, and performance limitations of O-ADC are discussed in this chapter. The circuit implementation of CMOS AFE and 8b asynchronous SAR quantizer are also discussed.

Owing to the performance benefits of the O-ADC architecture, this thesis reports the first optically sampled ADC that achieves >5b ENOB with CMOS and silicon photonics 3D integrated on a single chip. The implementation and measurement of O-ADC test-chip are detailed in Chapter-6.

5.1 Performance Limitation of Conventional CMOS ADCs

Analog-to-digital converters (ADC) perform the task of converting analog signals to digital values that can be stored or further processed by digital signal processors. Applications such as data communications (e.g. 400 Gb/s ITU-OTUs, fiber to home, etc), instrumentation (high-speed oscilloscopes), broadband capture (Cable TV, software-defined radio, etc), etc demand ADCs to have effective number of bits resolution of >5b and input sampling bandwidth of >20 GHz. So far the conventional CMOS ADCs have successfully met this demand. However, the jitter in the sampling clock, limited input sampling bandwidth, and

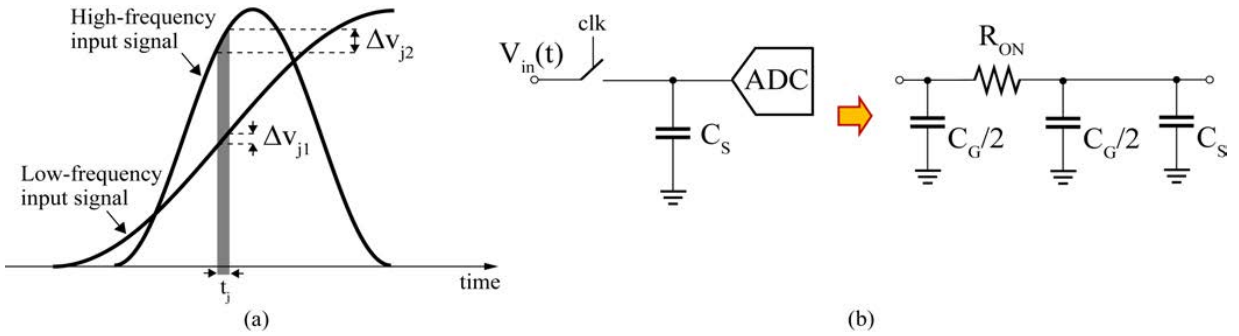


Figure 5.1: (a) Error in sampling input signal due to jitter in sampling clock and (b) Simplified input signal sampling circuit.

sampling clock and input signal distribution network is making it increasingly difficult to achieve higher ENOB at high input frequencies. These issues are further elaborated below.

5.1.1 Sampling clock jitter

An ADC performs two basic operations on the incoming continuous-time signal: samples in time-domain and quantization in the amplitude domain. The time sampling is realized by referencing the input signal to a repetitive and stable reference signal often referred to as the sampling clock. At the precise time instances defined by the sampling clock, the quantizer then quantizes the sampled signal resulting in the discretization of the input analog signal.

Any error or uncertainty in the ideal sampling instances of the sampling clock translates to inaccurate discretization reducing the effective resolution of the ADC. These deviations of sampling instances are often referred to as sampling clock jitter t_j, whose RMS value is often a figure-of-merit for the quality of the clock source. Further, the impact of clock jitter is even more severe for the high-frequency input signal. For instance, consider a clock with jitter t_j in Fig. 5.1(a) sampling a low-frequency and a high-frequency signal. As evident the resulting error voltage Δv_j is higher for the high-frequency signal as its rate of change (V/s) is higher. Due to this reason, the clock jitter is harmless when sampling a DC signal, and its effect increases for higher input frequency.

The impact of sampling clock jitter t_j can be predicted by quantifying the impact of Δv_j in Fig. 5.1(a) on the SNR of the ADCs. To do so, assume an input signal as given by,

$$V_{in}(t) = A \cdot sin(2\pi f_{in} t) \tag{5.1}$$

The RMS value of the slope of the signal in Fig. 5.1(a) can be obtained by taking a derivative of (5.1). This results in,

$$\left.\frac{dV_{in}}{dt}\right|_{rms} = \frac{\Delta v_{j,rms}}{t_j} = \frac{2\pi f_{in} A}{\sqrt{2}} \tag{5.2}$$

Thus the RMS error voltage $\Delta v_{j,rms}$ due to the clock jitter t_j can be easily found by re-arranging (5.2) as shown below,

$$\Delta v_{j,rms} = \frac{2\pi f_{in} A t_j}{\sqrt{2}} \tag{5.3}$$

The last step is to convert the effect of RMS error voltage $\Delta v_{j,rms}$ of (5.3) into SNR. This can be simply done by taking the ratio of RMS input signal to $\Delta v_{j,rms}$ as given by,

$$SNR = 20log_{10}\left[\frac{V_o/\sqrt{2}}{\Delta v_{j,rms}}\right] = 20log_{10}\left[\frac{1}{2\pi f_{in} t_j}\right] \tag{5.4}$$

Note that the expression in (5.4) assumes that the SNR of ADC is only limited by the clock jitter, and the ADC has infinite resolution and, thus, no quantization noise. A similar expression to quantify the impact of clock-skew on SNR can also be derived [79].

Using the SNR expression of (5.4), Table-5.1 outlines the maximum allowable clock jitter for achieving a target ENOB for an input frequency of 10 GHz and 45 GHz. This reveals the severe impact of sampling clock jitter on ADC's SNR. For instance, to achieve an ENOB of 6b at 10 GHz the clock jitter must be less than 203 fs, which is achievable by CMOS on-chip clock sources. However, when the input frequency is increased to 45 GHz, the clock jitter should be less than 45 fs. This can be quite challenging for CMOS clock sources to meet. Note that the expression in (5.4) includes only the impact of jitter on SNR and excludes the other ADC non-idealities. In [80], the overall signal-to-noise-plus-distortion ratio (SNDR) is shown that includes all of these effects. It is given as,

$$SNDR = 10log_{10}\left[\frac{\frac{1}{2}A^2}{(A^2/2^{2(N-1)})(1/12 + 1/4\sigma_{DNL}^2 + \sigma_{INL}^2) + \underbrace{(\sqrt{2}\pi f_{in} A t_j)^2}_{Jitter} + \sigma_n^2}\right] \tag{5.5}$$

Here, the SNDR is affected by ADC non-idealities such as quantization noise (factor of 1/12 in (5.5)), DNL, INL, noise (σ_n in 5.5), and jitter. One of the important points highlighted in (5.5) is that out of all the sources of non-idealities, only sampling clock jitter is signal-dependent. It also points to the fact that sampling clock jitter has the strongest impact for a full-scale input signal. Note that assuming a single-tone full-scale input is too pessimistic. The jitter specification can be relaxed by assuming a spectrum that resembles actual input [81, 82]. For instance, assuming a two-tone input would reduce the amplitude A in (5.3) by 6 dB, which reduces the RMS error $\Delta v_{j,rms}$ and thus, t_j by almost ∼2x. Also increasing the input signal swing to full-scale increases the non-linearity of the ADC. It is captured by using worst-case INL in (5.5).

5.1.2 Finite input sampling bandwidth

In addition to clock jitter, limited analog bandwidth of the input sampling circuit throws another challenge for high-ENOB high-sampling bandwidth ADC design. Figure 5.1(b)

Table 5.1: Estimated upper bound on sampling clock jitter for a target ENOB and input frequency

ENOB	Sampling Clock Jitter	
N [bits]	f_{in}=10 GHz	f_{in}=45 GHz
14	0.8 fs	0.2 fs
12	3.2 fs	0.7 fs
10	12.7 fs	2.8 fs
8	50.8 fs	11.3 fs
6	203.2 fs	45 fs

shows a simplified model of a typical ADC's sampling circuit. A series switch samples the input analog signal on the sampling capacitor C_S. Its value is determined based on noise requirement (kT/C) or matching limitations. The sampling switch can be modeled by an RC π-network comprising the ON resistance R_{ON} of the switch and parasitic capacitance C_G. For a typical switch, C_G=C_{GS} + C_{GD} + C_{GB}.

The analog sampling bandwidth of the ADC is determined by R_{ON}, C_G, and C_S. There are several techniques in literature that aim to reduce R_{ON}. For example, boot-strapping can be used to lower R_{ON}. However, it trades-off with device life-time. The dimensions of sampling switch can be increased, but after a point the resulting device parasitics also increase C_G. Another common approach is to lower C_S to improve the analog bandwidth. Unfortunately, this approach increases noise which requires increase in the input signal swing to keep SNR the same. With increased signal swing the distortion of ADC and the input buffer worsens, which lowers the overall SNDR as per (5.5). Lastly, from Fig. 5.1(b), it might appear that using high transit frequency (f_T) can help lower R_{ON}. While it is true that increasing f_T helps to realize a switch with lower R_{ON} and lower C_G, to achieve high sampling rate time-interleaving is often employed which connects many sampling switches in parallel. The resulting routing and presence of additional devices increase the parasitic capacitance making the sampling bandwidth less dependent on f_T. Thus, even employing DSM CMOS nodes with high f_T is also not useful in improving sampling bandwidth [80]. Consequently, the analog bandwidth of CMOS ADCs is still ∼20 GHz [80].

5.1.3 Routing of sampling clock and input signal

A common architecture for realizing high-speed CMOS ADCs is time-interleaving. Here, multiple identical ADCs are time multiplexed forming a parallel array of say M identical ADCs. Each ADC operates at a sampling rate of F_s, while all M ADCs combined achieve a higher net sample rate of MF_s. In such situation, routing of input signal and sampling clock to each to the sub-ADCs further complicates design of high-performance high-speed ADCs. Both the clock and input should be routed such that skew between the sub-ADCs is the same. Else as argued in [79] the resulting skew can degrade the SNR of overall ADC.

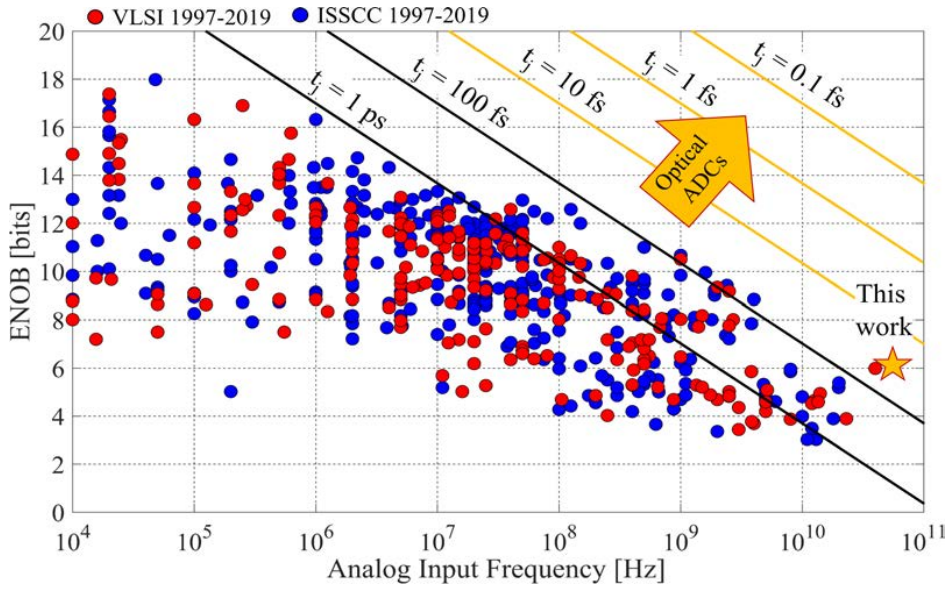


Figure 5.2: ENOB of conventional as a function of input frequency for CMOS ADCs reported in literature [83].

Besides, coupling of input to clock or clock to input creates harmonic distortion. For instance, coupling of input signal to the clock branch creates second-order harmonic distortion.

5.1.4 Survey of CMOS ADCs: ENOB vs f_{in}

Figure 5.2 plots the ENOB with the input signal frequency for the CMOS ADCs published in the literature. The impact of the limitations discussed above is visible here. The plot also shows jitter lines from 1 ps to 0.1 fs. While CMOS clock source can provide clocks with jitter around 100 fs, optical clock sources might be needed when ADCs require jitter performance better than 10 fs and beyond [84].

As indicated by (5.5), the clock jitter reduces the ENOB with increasing input signal frequency. This trend is visible in Fig. 5.2. It is very challenging to achieve high ENOB and high input frequencies. To realize design points in this region, optically sampled ADCs offer a viable alternative. However, the challenge then is to realize sampling in the optical domain, quantization in the electrical domain, and the architecture of the optical ADC should integration friendly to achieve a single-chip solution. These challenges are addressed by the O-ADC demonstrated in this thesis. As discussed in Chapter-6, the O-ADC test-chip achieves 6b ENOB with analog sampling bandwidth of >45 GHz and sampling jitter of <36 fs_{rms}. This design performance point is marked by ★ in Fig. 5.2.

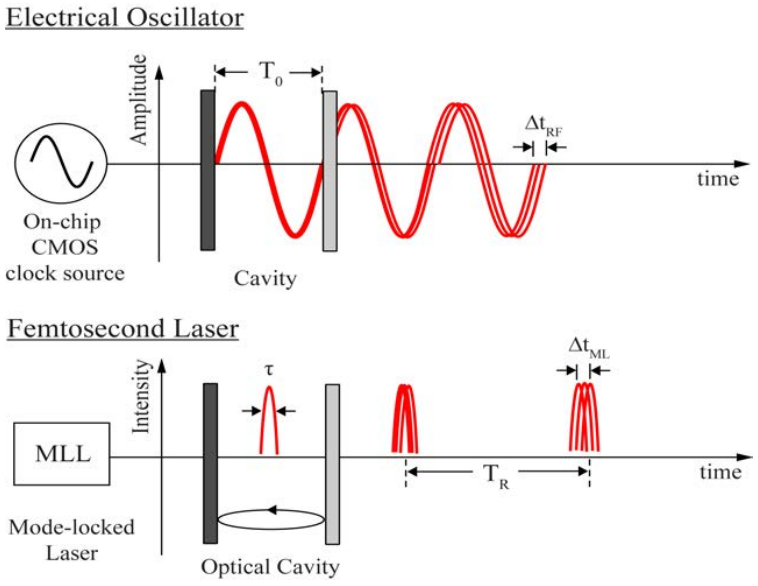


Figure 5.3: Illustration of timing jitter in (a) conventional electrical oscillators, and (b) optical pulse train generated from a mode-locked lasers [87, 88, 89]

5.2 Sampling an Electrical Signal using Optical Pulses

The ability of optical sources such as mode-locked laser (MLL) to produce ultra-low jitter optical pulses was predicted back in 1993 [85]. Since the MLL has evolved with recently reported timing jitter to be <1 fs [86, 78]. This level of jitter performance is tempting for ADC designers as the accuracy is greatly influenced by a stable and precise clock source.

To clarify the jitter benefits of MLL over conventional electrical oscillators, consider a simple time-domain illustration as shown in Fig. 5.3. In an electrical oscillator of Fig. 5.3(a), the zero crossings of the signal undergo a random walk due to fundamental noise sources affiliated with the generation of oscillations. The standard deviation of these zero crossings is equivalent to the integrated phase noise. This is also applicable to the optical pulse train source of Fig. 5.3(b). The losses in the resonator cavity of Fig. 5.3(a) are compensated by an amplifier to sustain the oscillations. Both the amplifier and loss mechanism contributes towards additive noise, which is determined using the fluctuation-dissipation theorem [87]. This white noise leads to jitter in the zero crossings of the oscillation signal whose variance increases linearly over time. The rate of increase of the jitter variance can be given by [87],

$$\sigma^2(\Delta t_{RF}) = \frac{1}{(2\pi)^2} \cdot T_0^2 \cdot \frac{1}{W_{mode}} \cdot \frac{kT}{\tau_{c,RF}} \tag{5.6}$$

where, T_0 is the period of the oscillation, W_{mode} is the intra-cavity energy stored in the resonator mode, kT is the thermal energy, and $\tau_{c,RF}$ is the cavity delay time for the energy stored in the resonator. A similar expression can be derived for the optical pulse trains

generated from an MLL source shown in Fig. 5.3(b). It is given as,

$$\sigma^2(\Delta t_{ML}) = \frac{\pi^2}{6} \cdot \tau^2 \cdot \frac{1}{W_{pulse}} \cdot \frac{\hbar\omega_c}{\tau_{c,ML}} \tag{5.7}$$

where, τ is the pulse width, W_{pulse} is the intra-cavity pulse energy, $\hbar\omega_c$ is the photon energy with pulse center frequency of ω_c, and $\tau_{c,ML}$ is the cavity decay time. Comparing (5.6) and (5.7) assuming 1550 center wavelength and temperature of 300 K, it can appear that MLL sources have poor noise performance as $\hbar\omega_c \approx 30 \cdot kT$. However, the differentiating factor is the ultra-narrow pulse duration of optical pulses in the MLL source e.g. <200 fs [77]. As most of the photons are concentrated in short pulse duration, the pulse position is fairly stable against perturbations caused by the noise source. Consequently, the MLL can have timing jitter almost two orders of magnitude lower than that of the electrical oscillators [87].

5.2.1 Types of optical ADCs

Optical ADCs is an active research topic today. Either sampling and/or quantization functions of conventional electronic ADCs are being replaced by equivalent optical counterparts. A good survey of published optical ADCs is outlined in [90]. The concept of optical ADCs was first reported back in the early 1970s [91, 92]. Since optical ADCs are actively researched with remarkable progress been reported in recent literature. In [93] an optical quantizer based ADC is shown that uses spatial interferometry with 3.6 bits for a 1.25-GHz input signal sampled at 40 GSa/s, while in [94] an integrated optical spatial quantizer based ADC achieved 3b ENOB for an 18-GHz signal. Researchers in [95] demonstrated the first optical quantizer and encoder based on time-interleaved ADC that uses nonlinear Sagnac loop mirrors and achieves 3.75n ENOB at 160 GS/s. While notable advances have been made, ADCs realized using optical quantizer has resolution limited to 3-4 bits. Currently, research efforts are in progress to further improve the accuracy.

On the other hand, an optically-assisted time-stretched ADCs is reported in [96, 97], where modulated optical pulses are significantly dispersed and temporally stretched so that a slow discrete electronic ADC can digitize the signal. Using this approach an optical ADC is demonstrated that digitizes 95.3 GHz tone at 10 TS/s with 4.5b ENOB [98]. While this ADC achieved astonishing results, it requires dispersion compensated fiber which is not straight forward to integrate on a SiPh chip. However, a slightly different approach of optical sampling employing a wavelength-demultiplexing scheme reported in [99] and thoroughly analyzed in [100] lends itself readily to single-chip SiPh and CMOS integration. The performance of such ADCs along with necessary calibration techniques and algorithms are well studied in the literature. In [101], demonstrates a 9.8b ENOB for a 733 MHz input signal sampled at 505 MS/s. A similar architecture is adopted for the O-ADC test-chip demonstrated in this thesis.

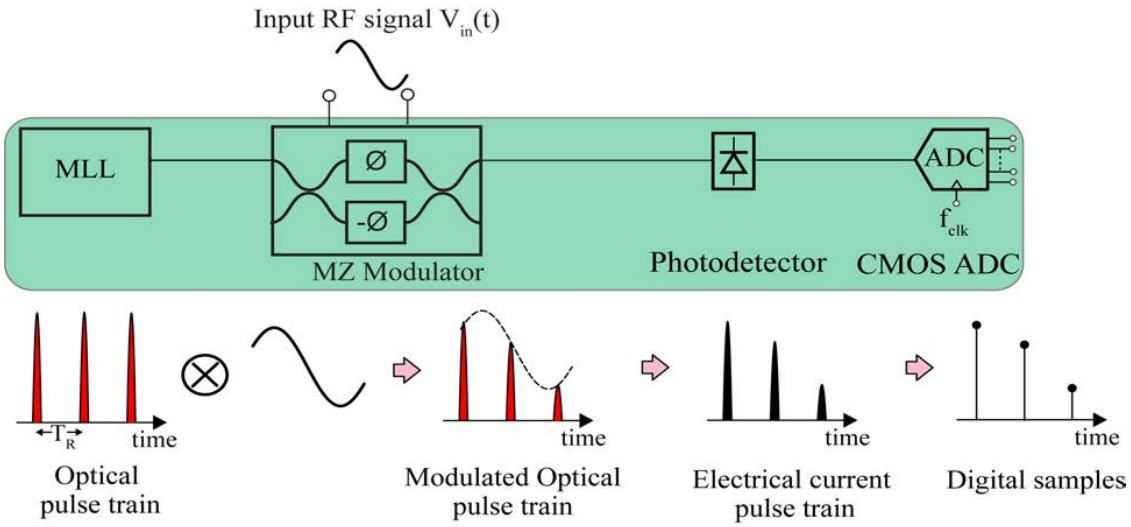


Figure 5.4: Concept of optical sampling in optically sampled ADC (O-ADC).

5.2.2 Basic concept of time-interleaved optical sampling

To leverage the low-jitter performance of MLL source, a simple single-channel optically sampled ADC can be realized as shown in Fig. 5.4. Here, an electro-optic modulator such as Mach Zehnder (MZ) interferometer-based modulator intensity modulates the incoming optical pulses from the MLL source with the input RF signal. The sampling process occurs during this electro-optic modulation of optical pulses. The modulated pulses at the output of the modulator carry the RF signal values at the time instances defined by the temporal position of the optical pulses. Lastly, the optical pulses are converted into electrical current pulses using photodetectors and digitized by electronic ADCs. The operations illustrated in Fig. 5.4 shows optical sampling and electronic quantization functions of an optically sampled ADC (O-ADC).

The simple scheme of Fig. 5.4 ensures low-jitter sampling, but the sample rate is limited by the spacing between the optical pulses, which is defined by the repetition rate of the MLL T_R. This makes it difficult to achieve accurate sampling at high sample rate as increasing the MLL repetition rate would require re-engineering of the MLL cavity, which can be very challenging. Even if the problem of MLL repetition rate is resolved, the architecture of Fig. 5.4 has another issue that it requires CMOS ADC to operate a full-rate. For instance, if a sampling rate f_S of 10 GS/s is desired then the CMOS ADCs should be also clocked at 10 GHz (f_{clk}). Both of these limitations can be addressed by employing wavelength and time-interleaving as shown in Fig. 5.5. Here, the center wavelengths of the pulses at the input of the modulator change periodically in time. Thus, for a system with N channel requires N distinct wavelengths that are created by splitting the spectrum of MLL. As this approach requires passive filters that can be readily integrated in a SiPh chip, this approach is later adopted in this thesis. Thus, as shown in Fig. 5.5, an optical demultiplexer (optical

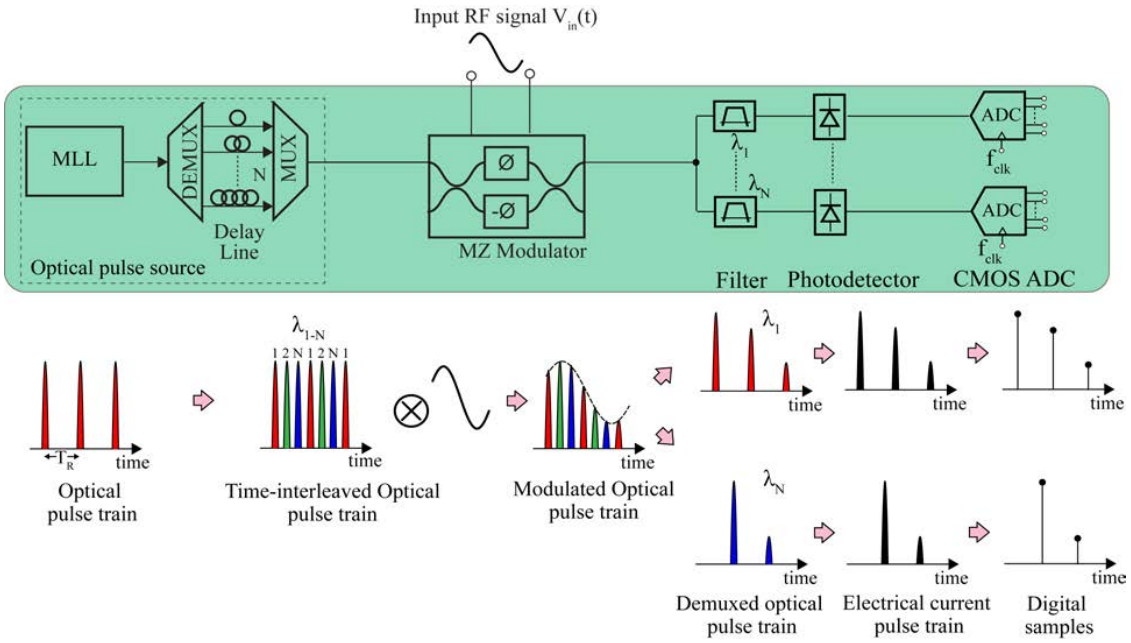


Figure 5.5: Concept of time-interleaved optical sampling.

filter) splits the optical pulses at the output of MLL into sub-pulses centered at a different wavelength. Note that the operation of optical demux is quite different from a time-demux popularly used as a logic gate. These pulses are then delayed with respect to each other using passive delay lines and combined into a single path using a N-to-1 multiplexer. The result is a pulse train with a repetition rate increased by N. These pulses are separated both in time and in wavelength and are modulated by an input RF signal. These modulated pulses are first separated and then converted to electrical current pulses, which are later digitized by CMOS ADCs. Thus, the overall O-ADC achieves $N \cdot f_S$ higher sample rate, while each sub-ADCs operate at f_S sample rate.

In summary, the major benefits provided by the architecture of Fig. 5.5 are: jitter of O-ADC is governed by the extremely low jitter of the optical pulses, due to use of passive optical components it is amenable to integration in any emerging CMOS and SiPh platforms, and the sampling bandwidth is determined by electro-optical interaction in the modulator, which can be very fast. Thus, the O-ADC has the potential to enable ADCs with high-resolution and high input sampling bandwidth.

5.3 Architecture of O-ADC

Using the topology discussed in Fig. 5.5, an O-ADC architecture as shown in Fig. 5.6 is implemented in this work. The optical pulse train with repetition period T_R is split into N trains, each centered at a different wavelength, with a 1-to-N wavelength demultiplexer

(optical filter). These trains pass through optical delay lines, which introduce incremental delays and are then recombined with a multiplexer to produce a pulse train with a repetition period of T_R/N. All of this setup is combined and represented as a simple optical pulse source in Fig. 5.6. The modulation of the optical pulse train with the RF signal, or in other words the optical sampling, is performed using an off-chip electro-optic MZM. The modulated pulse train is then coupled into the test-chip, which is realized on a single-chip implemented in a 3D integrated platform. These pulses are then taken apart into N channels using double-ring filters matched to the one used to realize optical pulse source. These pulses in all N channels are individually converted to the current pulses by the integrated photodetectors. The double-ring filters and detectors are realized on SiPh chip. The current pulses are amplified and digitized with CMOS ADCs realized in 65nm. The SiPh chip and the 65nm CMOS chip are integrated at the wafer-scale using through-oxide-vias (TOVs).

The CMOS ADCs are synchronized with the MLL pulses using the electrical clock output. The digitized samples stored in the on-chip memory back are read and post-processed to compensate for distortions and interleaved errors before obtaining the final digital representation of the RF signal. As mentioned earlier, the jitter of the overall O-ADC is governed by the jitter of the optical pulses. It will be shown later that the jitter in the CMOS clock does not influence the ADC performance. In addition, the interleaving scheme of Fig. 5.5 not only increases the sample rate by a factor of N but also reduces the required analog bandwidth from the detectors and CMOS ADCs by N. Thus, O-ADCs with high sample rate and high sampling bandwidth can be realized by interleaving relatively low-speed components. This is another important advantage offered by the O-ADC architecture of Fig. 5.6.

5.3.1 Sampling bandwidth of O-ADC

In addition to improving the sampling jitter, the O-ADC architecture of Fig. 5.6 also is capable of increasing the input signal sampling bandwidth. Here, we evaluate and identify limits on sampling bandwidth, and potential sources that are the bottleneck to achieving wider bandwidth. For this purpose, it is assumed that an MLL source is available as reported in [77]. It outputs pulses with <0.2 ps pulse width at 1 GHz repetition rate with a full-width half max (FWHM) of 17.5 nm (2.2 THz) and jitter with 22 fs. For simplicity, a rectangular optical pulse of width 0.2 ps is used in the simulation as shown in Fig. 5.7. Note that the optical pulse source in Fig. 5.6 represents an MLL source combined with demux-delay line-mux interleaver.

The optical demux slices the spectrum of MLL into N with each slice centered around a different wavelength. In Fig. 5.7, for example purpose, N of 4 is chosen. The FWHM bandwidth of the spectrum at the output of the optical demux (optical filter) is 0.65 nm. Consequently, the optical pulse expands from 0.2 ps to 5.5 ps. These optical pulses are then delayed and combined. Both of these operations do not alter the optical pulse width. The time and wavelength spaced 4 optical pulses with color black, red, blue, and green, at the output of the multiplexer, are as shown in Fig. 5.7. Further, these pulses are modulated by

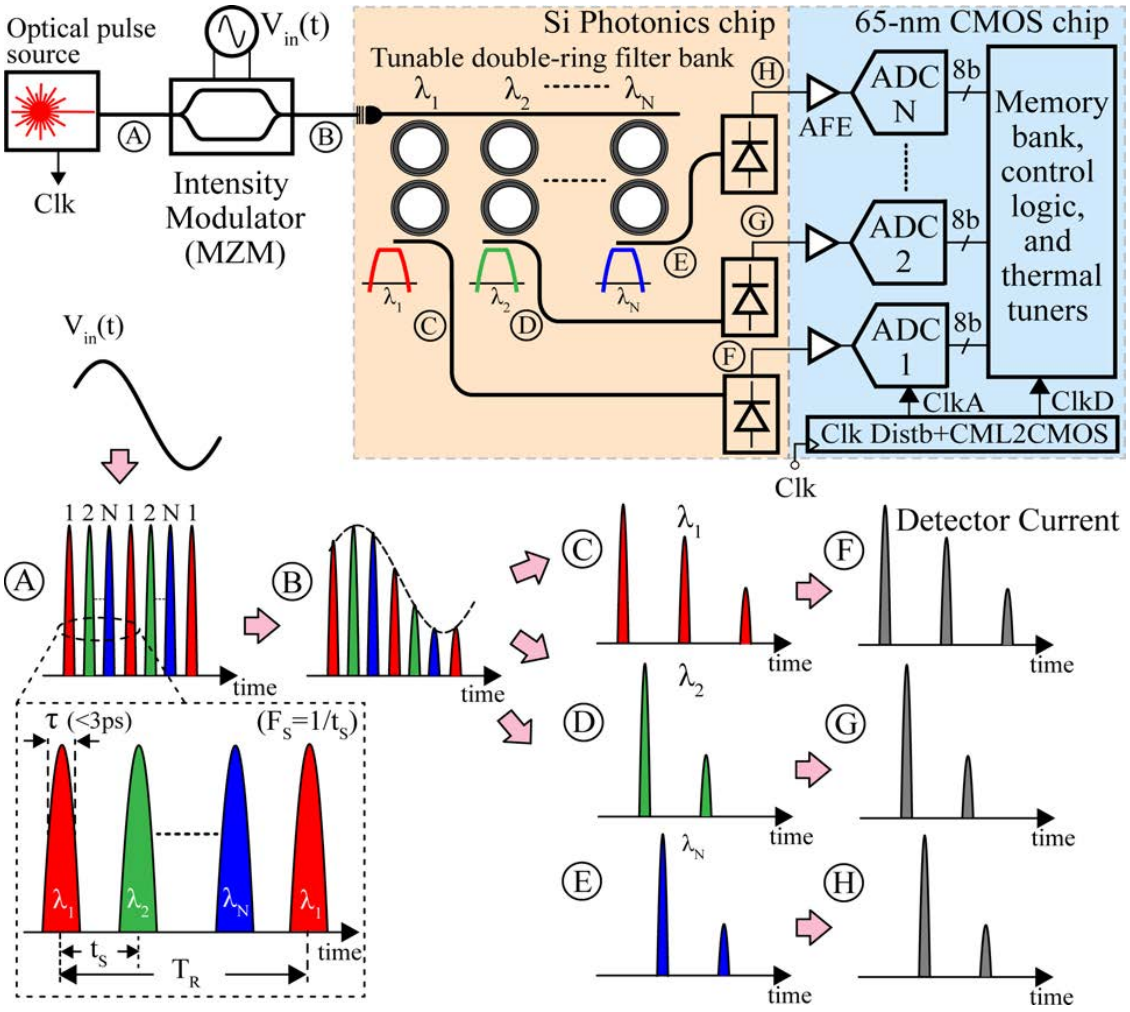


Figure 5.6: Architecture of optically sampled ADC (O-ADC) that uses low-jitter optical pulses to sample the input signal.

an MZM with a 10 GHz RF input signal. The modulated pulses are shown in the bottom-left plot in Fig. 5.8.

At this point, there are two bandwidth limitations. First, the limit is imposed by the finite pulse width of the optical pulses BW_1 and the second limit is due to the electro-optic bandwidth of the modulator BW_2. The bandwidth limit due to finite optical pulse width can be estimated simply by,

$$BW_1 = \frac{1}{2\pi\tau_a} \approx 29GHz \tag{5.8}$$

where, τ_a is the optical pulse width after the demultiplexer. If the $BW_2 < BW_1$ then the electro-optic bandwidth of the modulator becomes a bottleneck. The modulator later used

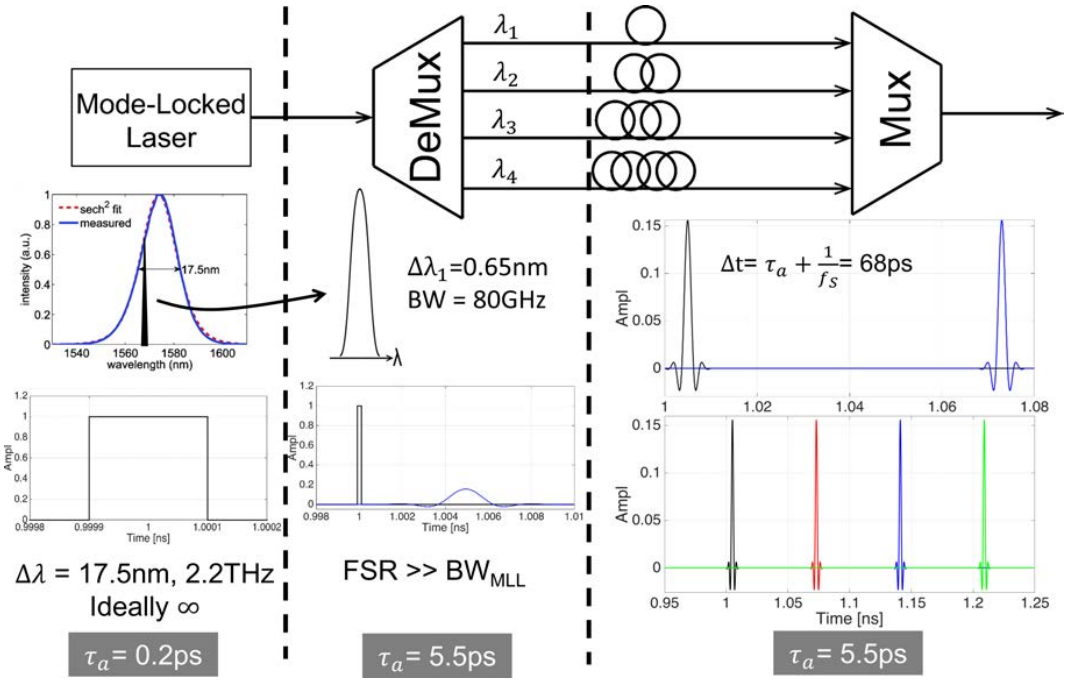


Figure 5.7: Optical pulse width at various nodes in pulse interleaver. The MLL parameters are obtained from [77].

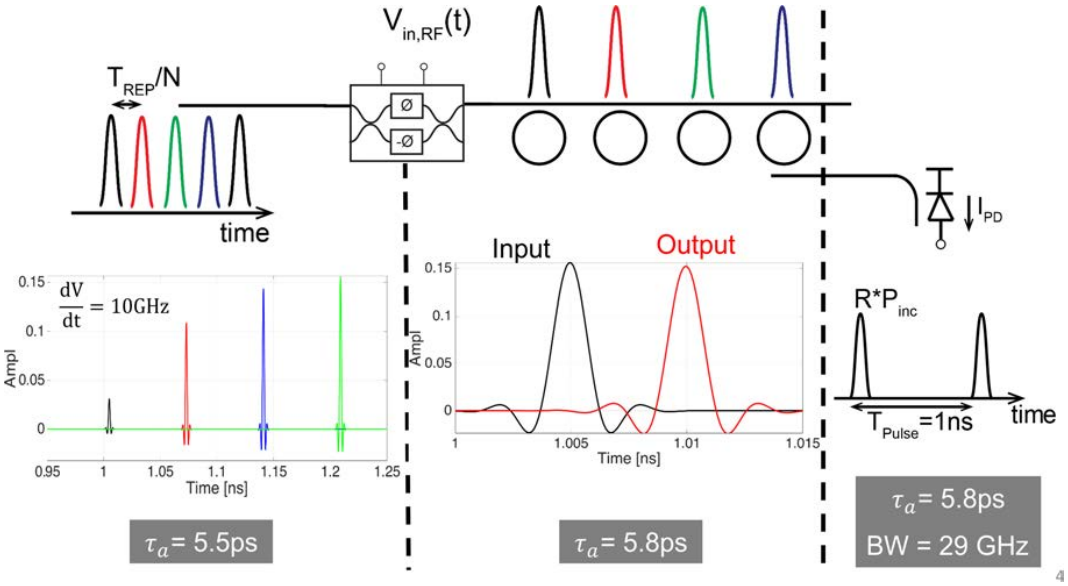


Figure 5.8: Optical pulse width at the input and output of MZM, double-ring filter banks, and photodetectors.

in Chapter-6 to measure O-ADC test-chip has 40 GHz bandwidth, while there are integrated modulator demonstrated in the literature that have similar or higher bandwidth. Thus, to achieve high sampling bandwidth, the optical demux should have as wider bandwidth as possible. However, due to limited FSR of the demux, realizing wider bandwidth often puts a limitation on the amount of channel that can be interleaved forcing the sample rate of the CMOS ADCs to increase to meet target overall sampling rate.

After modulation, the optical pulses are filtered, converted to current, and digitized. As the signal is already sampled, none of these steps affect the sampling bandwidth of the O-ADC.

5.3.2 Performance tradeoffs of O-ADC

For a fixed average optical power delivered from the MLL, the presence of optical losses and additive thermal noise limits the resolution (ENOB) that can be achieved by the O-ADC. Assuming an ideal CMOS ADC, the ENOB of the O-ADC is primarily determined by the SNR at the output of the photodetector in Fig. 5.8. It is given as,

$$SNR = 10log_{10}\left[\frac{P_S}{P_n}\right] \text{ and } ENOB = \frac{SNR - 1.76}{6.02} \tag{5.9}$$

where, P_S is the signal power while P_n is the integrated noise power over the noise equivalent bandwidth BW_n. Assuming the dark current of the photodetector contributes negligible shot noise, the noise power can be expressed as,

$$P_n = 2q \cdot \frac{I_{max} + I_{min}}{2} \cdot BW_n = 2q \cdot \frac{I_{max}}{2}(2 - m) \cdot BW_n \tag{5.10}$$

where, I_{max} and I_{min} is the maximum and minimum current generated by the photodetector for a modulation depth m applied by the modulator. Thus, $I_{min} = (1-m)I_{max}$. Further, the signal power P_S can be expressed as,

$$P_S = \left(\frac{I_{max} - I_{min}}{2}\right)^2 = \frac{m^2 I_{max}^2}{4} = \left(\frac{m\mathcal{R}}{2}\right)^2 \cdot \alpha_{DL}^2 P_{inc}^2 \tag{5.11}$$

where, $\mathcal{R}$ is the detector responsivity, α_{DL}^2 is the drop-port loss of the double-ring filters in Fig. 5.6, and P_{inc} is the incident optical power per channel in the bus-waveguide in Fig. 5.6. The total optical power in the bus-waveguide is NP_{inc}. Using (5.9) and (5.11) the SNR can be expressed as,

$$SNR = \left(\frac{m}{\sqrt{2-m}}\right)^2 \cdot \frac{\mathcal{R}^2}{4} \cdot \frac{\alpha_{DL} P_{inc}}{2qBW_n} \tag{5.12}$$

The expression of (5.12) reveals an important requirement of O-ADC. The SNR can be improved by 1 bit by increasing modulation depth m by ∼2x. However, as will see in the section later increasing modulation depth too much induces distortion in the modulator.

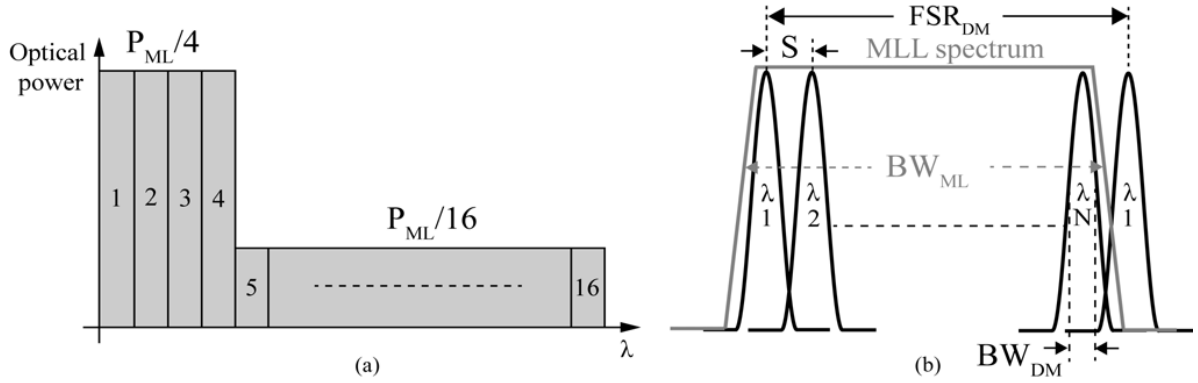


Figure 5.9: (a) Peak power and bandwidth of MLL to support N=4 and N=16. (b) FSR, channel spacing, and bandwidth of demux.Typical values of FSR is 2.2 THz, S is 120 GHz and BW_{DM} is 20 GHz [100].

While this distortion can be calibrated, there is a limit to which the calibration can be effectively applied. For instance, making the modulation depth of 1 would induce strong clipping distortion which cannot be calibrated. Thus, the linearity performance of the O-ADC degrades greatly.

Further, the incident optical power P_{inc} in (5.11) can be further expressed as,

$$P_{inc} = \underbrace{\left(\frac{BW_{DM}}{BW_{ML}}\right)}_{Spectral fill} \cdot \underbrace{\alpha_{IL}^{I}\alpha_{IL}^{MZ}\alpha_{c}}_{Optical Loss} \cdot \frac{P_{ML}}{N} \tag{5.13}$$

where,

BW_{DM}	Spectral bandwidth of the optical demultiplexer. Typical value is 1.1 nm.
BW_{ML}	Spectral bandwidth of MLL source. Typical value is 17 nm.
α_{IL}^{I}	Insertion loss of the interleaver (demux-delay line-mux). Typical value is 7 dB.
α_{IL}^{MZ}	Insertion loss of the MZ modulator. Typical value is 4 dB.
α_c	Fiber-to-chip coupling loss. Typical value for Fig. 5.6 is 3.5 dB.
P_{ML}	Peak MLL output optical power per channel. Typical value is 0.1 W.

To maximize SNR, from (5.12), it is evident that P_{inc} should be maximized. On the other hand, to increase the sampling rate the number of interleaved wavelengths should be increased as the sampling rate of the O-ADC is related to N and repetition rate F_R of the MLL as given by,

$$F_S = N \cdot F_R \text{ where, } F_R = 1/T_R \tag{5.14}$$

However for fixed MLL output power, from (5.13), increasing N would reduce P_{inc} as the MLL power is now split between more number of channels. This is clarified in Fig. 5.9(a)

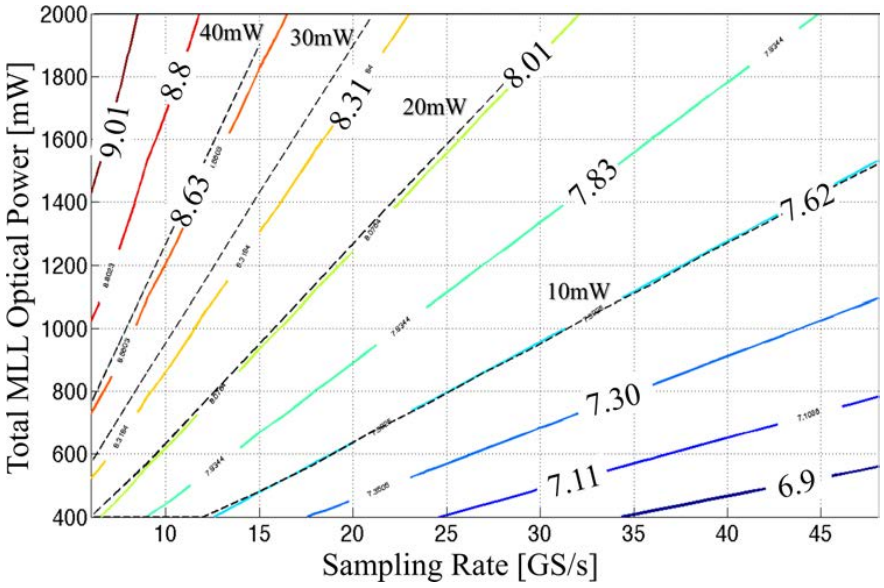


Figure 5.10: Simulated achievable ENOB lines for given input MLL power and O-ADC sampling rate contour. The numbers on each line highlight the achievable ENOB while the dotted lines show the effective power in the double-ring filter bank, which can induce additional distortion depending on the ring's design.

where an MLL spectrum with a peak output power of P_{ML} per channel is been divided into 4 channels. Keeping the same average optical power, if the number of channels is increased from 4 to 16, the P_{ML} should be reduced as it is distributed among more channels as shown in Fig. 5.9(a). A more practical scenario is described in Fig. 5.9(b) where an MLL with fixed output power and spectral bandwidth BW_{ML} is available. The bandwidth of demux BW_{DM} and channel spacing S is chosen such that it spans the MLL spectrum. Note that the FSR of the demux must be bigger than the BW_{ML}. To accommodate larger number of channels, the bandwidth of the demux and the channel spacing can be squeezed. However, as the bandwidth of the demux is lowered the spectral fill term in (5.13) also reduces which in turn reduces P_{inc} and degrades SNR as per (5.12). In o

$$FSR_{DM} \geq BW_{ML} \approx N_{max} \cdot (BW_{DM} + S) \tag{5.15}$$

where, N_{max} is maximum number of interleaving channels possible for a given BW_{ML}, S, and BW_{DM}.

The arguments made and analysis done for expressions (5.9)-(5.14) are put in perspective by Fig. 5.10. Here, the achievable ENOB is calculated from (5.9) for varying MLL optical power and the sampling rate of O-ADC defined by (5.14). As evident from Fig. 5.10, for fixed MLL optical power, increasing the sampling rate by increasing N will reduce ENOB. To keep ENOB constant, the MLL optical power should also be increased. This gives rise to the ENOB lines in Fig. 5.10. As the MLL optical power increases so will the power in the

double-ring filters, which is indicated by the dotted lines in Fig. 5.10. This leads to ENOB being further degraded due to distortion from the double-rings, which is covered later. A preferred way to increase the sampling rate of O-ADC is to keep P_{ML} constant and increase the repetition rate F_R. However, as the analog bandwidth of the photodetector and the sampling rate of the CMOS ADC depend on F_R, both of them should also be increased.

Thus, on one hand, the value of N_{max} is limited by the FSR of demux while on the other F_R is limited by maximum achievable analog bandwidth of the detector and CMOS ADC. In such a scenario, responsivity $\mathcal{R}$ of the detector in (5.12) is the only knob that does not have any tradeoffs attached. Increasing $\mathcal{R}$ not only linearly increases SNR but also reduces the optical power needed in the double-ring and thereby lowering their distortion. In summary, the purpose of this analysis is to give a rough idea about the required input optical power, achievable resolution, and the importance of the number of interleaved channels. The key take away is that for a given ENOB,

- the optical power must change in proportion to the number of interleaved channels.
- the power must change in proportion to the repetition rate.
- any change in the loss of the optical components must be compensated by adjusting the optical power.

5.3.3 Impact of distortion from double-ring fitlers

In Fig. 5.10, it might be tempting to observe that high ENOB at a faster sampling rate can be achieved by simply increasing the MLL output optical power. While this intuition is correct, the distortion induced by the double-ring filters at high optical power puts a practical limit on maximum achievable ENOB. Any optical block designed using silicon waveguides will experience two-photon absorption (TPA) because when two photons combine to overcome the bandgap of silicon additional electron-hole pairs are generated. These TPA generated free electrons and holes act as absorption centers. This phenomenon is referred to in the literature as free carrier absorption (FCA). The presence of these free carriers (electrons and holes) also changes the refractive index of the silicon (as discussed in Chapter-3) inducing the phenomenon called free-carrier dispersion (FCD) effect. All of these nonlinear phenomena generate nonlinear distortion, which eventually deteriorates linearity or the SFDR of the O-ADC. The impact of these nonlinearities is escalated at higher optical power. Thus, if the optical power is increased to achieve higher ENOB, the resulting increase in nonlinearity would adversely affect the ENOB.

The combined effect of these three sources of distortion can be quantified by measuring the traditional distortion coefficients. For this purpose, distortion coefficients till 5^{th} order is measured from the drop-port spectrum of the double-ring filters whose design and implementation are discussed in Chapter-6. These distortion coefficients are then used along with the simulated SNR values to get an estimate of the overall SNDR as shown in Fig. 5.11(a). The ENOB in Fig. 5.11(b) is then calculated from the simulated SNDR. As shown in Fig.

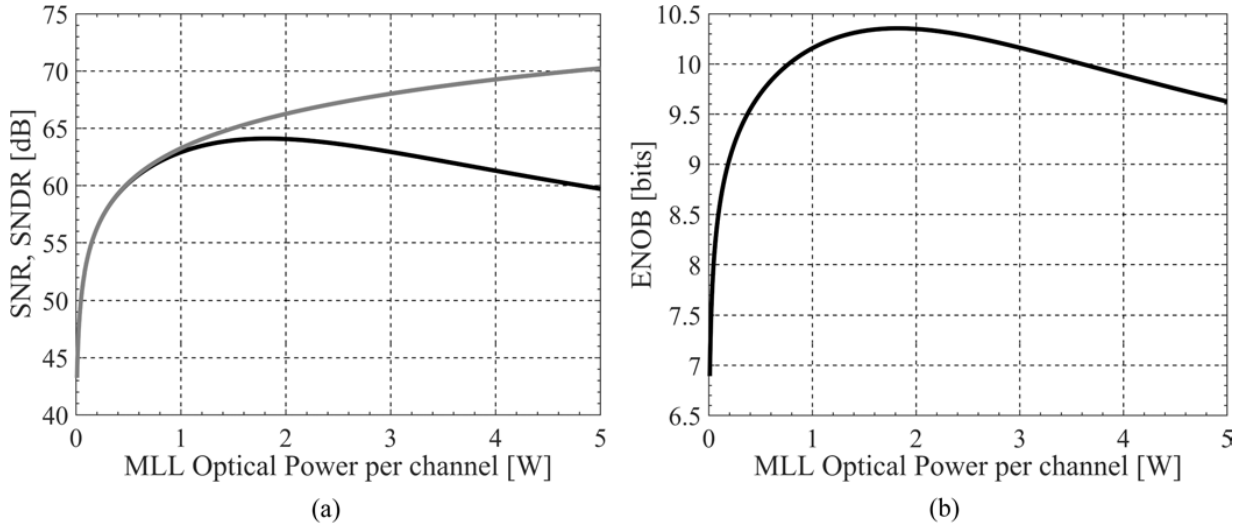


Figure 5.11: Simulated: (a) SNR and SNDR, and (b) resulting ENOB. The distortion coefficients uptill 5^{th} harmonics are used whose values are obtained from measurement of double-ring filters designed in 3D integration platform discussed in Chapter-6.

5.11(a), the SNR continual increases with the increasing MLL optical power. This behavior is also predicted by (5.12). However, the distortion is not modeled in the ENOB lines of Fig. 5.13 always increases with MLL power. In the presence of distortion, the SNDR and ENOB plots are shown in Fig. 5.11(a) and (b), respectively. The SNDR degrades at high enough MLL optical power due to the distortion arising in the double-ring filters. The distortion contribution of the filters can be controlled by design to some extent [100]. Alternatively, digital calibration techniques can also be adopted at the cost of increased overall power consumption of O-ADC.

Note that during the development of test-bench to evaluate O-ADC test-chip performance in Chapter-6, the losses were significantly higher due to the use of discrete components. Thus, the MLL optical power was not sufficient, which was compensated using an off-chip Er-doped Fiber Amplifier (EDFA).

5.3.4 Impact of cross-talk due to double-ring filters

Like every other traditional optical or RF filter, the double-ring filters used in Fig. 5.6, have finite rejection. Consequently, the optical power on the neighboring channel wavelength is rejection partially. This unrejected optical power drops onto the detector and creates cross-talk current pulses as shown in Fig. 5.12(a). Similar to any traditional filter design, the rejection can be improved by implementing a higher-order filter or increasing the spacing between the two channels. However, achieving wider bandwidth and higher-order simultaneously is challenging. Figure 5.12(b) illustrates this tradeoff. Here, the signal to interference ratio is plotted against channel spacing for varying bandwidth. For lower bandwidth filters,

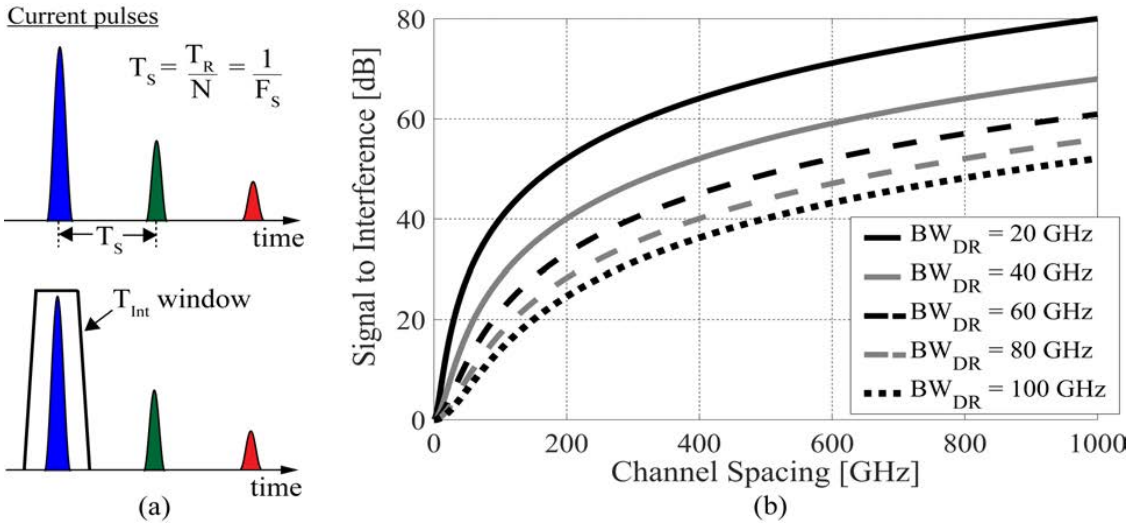


Figure 5.12: (a) Interfering current pulses from adjacent channels. (b) Impact of cross-talk with channel spacing for varying BW_{DR}.

it is better to achieve higher rejection at the same channel spacing.

An important aspect to notice in Fig. 5.12(a) is that the cross-talk current pulses are separated in time due to the time-interleaving nature of the optical pulse source. This feature is later used to advantage in Section-5.5 where a switch-capacitor-based current integrating front end with integration window designed such that it integrates current pulses from the present channel. Thus, it rejects the cross-talk current pulses to a great extent.

5.4 Comments on modulator and modulator driver

In Fig. 5.6, a Mach Zehnder interferometer-based modulator (MZM) is used that preferrably requires a material with strong eletro-optic effects. For demonstration purpose, a $LiNbO_3$ MZM is used as they are easily available, wide-bandwidth, and compact. In future, these MZM will be integrated on the O-ADC chips using other III-V semiconductor materials like GaAs and InP that have equally strong electro-optic effects.

As shown in Fig. 5.13(a), the MZM comprises an input waveguide that is split into two paths that are later recombined into an output waveguide. The two paths make up the two arms of the interferometer. The driver in Fig. 5.13(a) applies an RF input and also provides the necessary bias for the MZM. The applied voltage creates an electric field across each arm of MZM that induces change in the refractive index and thus, the optical path length modulating the phase of the optical signal in each arm. When the two paths are combined, the different phase modulation in each arm translates into intensity modulation in the output waveguide. To achieve a chirp free intensity modulation, meaning only intensity is modulated without occassional phase or frequency modulation, the phase modulation in

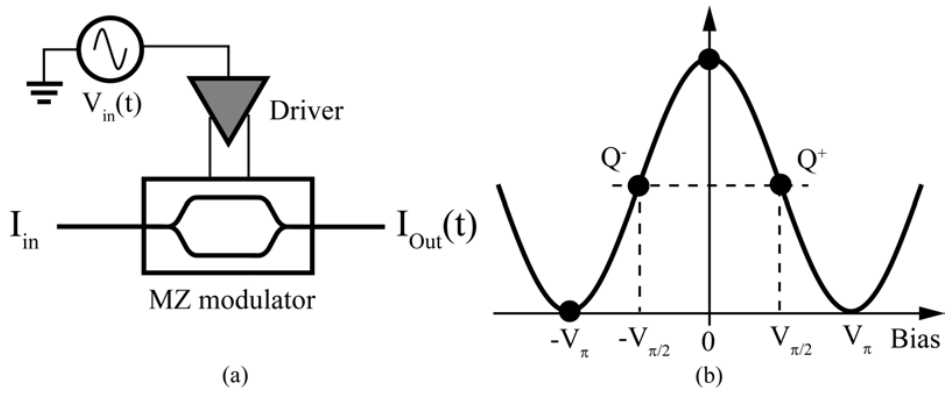


Figure 5.13: (a) An MZM driven by a driver, and (b) transfer function of an MZM.

each arm should be exactly equal and opposite in sign.

The RF input and the DC bias are applied to the MZM using two separate pairs of electrodes. They are often referred as modulation and bias electrodes, respectively. In Fig. 5.13(a), the MZM driver superimposes the modulation signal onto the bias voltage. Thus, for an RF input signal V_{in}(t) in Fig. 5.13(a), the transfer function of an intensity modulator is given by,

$$I_{out}(t) = T_{mz}\frac{I_{in}}{2}\left[1 + sin\left(\pi\frac{V_{in}(t)}{V_\pi} + \theta\right)\right] \tag{5.16}$$

where,

V_π	Voltage required to achieve a phase-shift of π
θ	Deviation from the quadrature bias point
T_{mz}	Transmission of the modulator
I_{in}	Input optical intensity
I_{out}	Output optical intensity that varies as a function of V_{in}(t)

Depending upon the application, the MZM is biased at an appropriate bias point. Fig. 5.13(a) shows various bias points in the transfer function of an MZM. A voltage of V_π shifts the transfer function from minimum to maximum or maximum to minimum. The MZM is biased at this point for non-linear applications like NRZ transmission. If the input NRZ data has an amplitude of V_π then the output data is NRZ as well with improved signal quality as overshoot and patterning are clipped by the non-linear transfer of the MZM.

However, for applications requiring high-linearity such as O-ADC, the MZM is biased at the quadrature point (Q^- or Q^+ in Fig. 5.13(b)). When biased at the quadrature point the phase term θ in (5.16) is zero and the input signal utilizes the linear part of the transfer as shown in Fig. 5.14. Note that higher linearity is achieved by making sure that the input modulating signal has an amplitude much smaller than the V_π of the modulator. However, improving linearity by reducing the modulation depth results into SNR degradation which

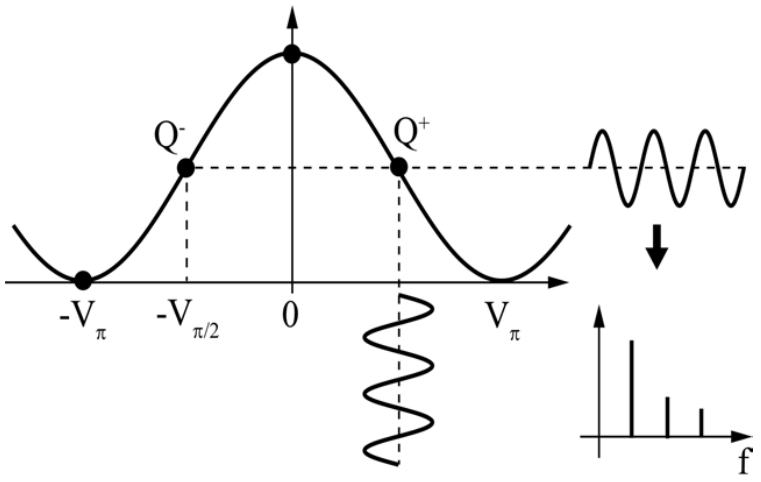


Figure 5.14: Analog modulation of MZM when biased at quadrature.

would be explained in later section. Lastly, it should be mentioned that the value of V_π is also dependent on application. For application requiring high-linearity, it is desirable to have low V_π and thus, more gradual and linear transfer curve. However, for communication applications that use phase-shift keying like BPSK or DPSK, the value of V_π should be as small as possible to reduce the demand of high drive voltage swing and high sampling rates.

5.4.1 Modulator Linearization

As given by (5.16), the transfer characteristic of MZM is cos^2-shaped. The resulting nonlinearity can be much worse than that contributed by the double-ring filters in Fig. 5.11(a). This makes the MZM the dominant source of nonlinearity and limits the dynamic range or the SNDR of the O-ADC. Thus, it is crucial to linearize the MZM transfer characteristic. A simpler means to linearize is to use small modulation depth. However, choosing too small of a modulation depth can be expensive from SNR perspective as given by (5.12). A better approach is to use moderate modulation depth (between 0.5 to 0.8), and calibrate for the resulting non-linearity. Note that maximum modulation depth (i.e. m=1 when output of the driver swings full V_π) would induce hard distortion which cannot be calibrated [100].

The calibration of MZM transfer characteristic or linearization can be performed by observing that the expression (5.16) is fairly static in nature, and thus, can be readily inverted in the digital domain to fully recover the original input tone. Thus, if the output of the ADC is V_{ADCout} for an input of V_{in}(t), then the calibration to be applied can be obtained by re-arranging (5.16) as shown below,

$$V_{in,calib}(t) = \frac{V_\pi}{\pi}\left[\frac{1}{2}\cdot sin^{-1}\left(\frac{2V_{ADCout}}{K1} - 1\right)\right] \tag{5.17}$$

Here, $V_{in,calib}$(t) is the calibrated value for V_{in}(t) from sampled and quantized ADC output V_{ADCout}, while K_1 is a constant proportional to the energy of the input optical pulses. Any error due to drift from the quadrature point (i.e. $\theta \neq 0$) will result in an offset which is calibrated using foreground calibration approach described in Chapter-6.

Using this approach researchers in [101] showed improvement in linearity of >80 dB and demonstrated a discrete implementation of an optically sampled ADC with ∼10 b ENOB. However, this linearization method is not perfect and has some limitations. It can only linearize non-linearity resulting from interferometer transfer function given by (5.16). Depending on the quality crystal used to implement MZM, the phase modulation in each of the arms of MZM can be different, and can exhibit nonlinear behavior. This added non-linearity cannot be calibrated by the approach described above. In addition, any non-linearity added by the MZM driver (shown in Fig. 5.13(a)) will also be not calibrated. While developing the test-bench for the O-ADC test-chips, these two aspects are actively kept in mind. To avoid distrotion from phase modulator, a high quality $LiNbO_3$ based MZM is used and the distortion from driver is avoided by filter its output before it drives the MZM.

5.5 Limitations and Tradeoffs of O-ADC building blocks

The architecture of O-ADC is Fig. 5.6 enables sampling of high-speed RF signal with low-jitter optical pulses. In the process, it requires a few additional components that influence the overall ADC performance and offer certain design choices to make. The previous Section-5.3 covered them in detail. However, it also helps to outline these limitations and tradeoffs on per block basis, which is shown in this section below. Here, the impact of each sub-blocks of Fig. 5.6 on overall O-ADC performance is summarized.

5.5.1 MLL optical pulse source

The low-jitter optical pulses for O-ADC are provided by the MLL source. The key metrics of MLL that influence O-ADC performance are optical pulse width, jitter, output power, and repetition rate. While the optical pulse width is determined by the bandwidth of the demux, the MLL is still required to have wide enough spectral bandwidth to accommodate the target number of interleaving channels. The jitter of the MLL source directly translates into the sampling jitter of the O-ADC. Hence, having a low-jitter MLL is desirable. However, the full advantage of low-jitter of the MLL can only be taken if a high enough sampling bandwidth of the O-ADC is achievable.

Furthermore, the optical power of the MLL is another influential parameter that directly impacts O-ADC performance. The ENOB of the O-ADC improves with optical power until it gets limited by the distortion from the double-ring filter bank. Lastly, the repetition rate of the MLL helps to achieve higher sampling rate O-ADC without requiring a large number of interleaving channels which adversely impacts the ENOB. While the MLL designers focus

on performance like achieving extremely narrow pulse-width or ultra-low jitter, an MLL dedicated for O-ADC would have slightly different design specifications owing to the reasons listed above.

5.5.2 Demux-delay line-mux interleaver

The interleaver block comprising of the demultiplexer, delay lines, and a multiplexer is an important element of O-ADC. Particularly, demux is the most crucial component as the spectral bandwidth of the demux controls the optical pulse width and thus, the sampling aperture of the O-ADC. Further, the FSR of the demux should also be larger than the spectral bandwidth of the MLL. To increase the number of interleaved channels while keeping the optical pulse width wide enough, the demux should be designed with wide spectral bandwidth and sharp roll-off. Further, the smaller spectral bandwidth of the demux adversely impacts SNR as it degrades the spectral fill, represented in (5.13). Besides, controlling the delay realized by the delay lines is crucial to avoid spurs in the O-ADC output spectrum due to timing mismatch. These spurs will degrade the SNDR and thus, the ENOB of O-ADC. In chapter-6, the delay line is realized using optical fiber where the delay is implemented by tuning fiber length. This way of implementing the delay line ensures timing mismatch is minimized. However, it is hard to integrate. In [100], the delay line is implemented using silicon waveguides. While the precise delay cannot be ensured due to process variations, integrated heaters are used to tune out any timing mismatch. This approach does cost increased power consumption. Lastly, for the design of the multiplexer, it is important to minimize the insertion. This helps to increase the incident optical power and thus, the SNR for the same MLL optical power.

5.5.3 Electro-optic modulator

The modulator is on the most important blocks of the O-ADC as it enables the sampling process. From the O-ADC system perspective, the bandwidth, linearity, and modulation depth are the most critical parameters of the modulator. A high electro-optic (S_{21}) bandwidth is crucial as it governs the maximum input RF signal rate at which the modulator can intensity modulate the optical pulse. This modulation should occur with good linearity in order to realize high ENOB at maximum input bandwidth. Lastly, the modulator should also maintain good linearity while achieving good modulation depth. Researchers in [99] show that for an MZ modulator a modulation depth of 0.6 is optimal. A good modulation depth further enables higher ENOB by maximizing the SNR. Additionally, to realize a truly single-chip solution, the driver in Fig 5.13(a) should also be integrated. In this case, the input capacitance and V_π of the modulator are also equally important as they require the driver to produce high swing output at high frequencies while driving a large capacitive load. For instance, the MZM with 40 GHz bandwidth used in Chapter-6 to test the O-ADC test-chips requires 4.5 V_{pp} swings at 40 GHz, which can be challenging for a CMOS integrated driver.

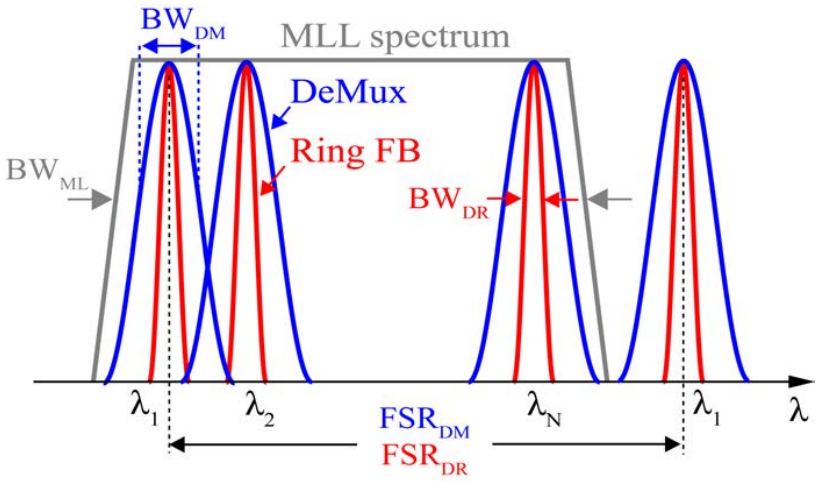


Figure 5.15: Wavelength spectrum matching between MLL, demux, and double-ring filter bank.

5.5.4 Double-ring filter bank

As the double-ring filter bank receives sampled data, it does not influence the sampling bandwidth of the O-ADC. However, its spectral bandwidth, linearity, and roll-off do impact SNDR, and thus, the ENOB of the O-ADC. Firstly, due to power enhancement in the double-rings, it can generate distortion due mechanisms such as TPA, FCA, and FCD. The coefficients that control these distortions are a strong function of the device geometry. Thus, the design of double-ring filters should be done accounting for the distortion. [100]. The spectral bandwidth is another crucial factor. The double-ring filter should be designed in conjunction with the spectral response of the MLL and the demux as shown in Fig. 5.15. The FSR of the double-ring FSR_{DR} should be greater than or equal to the FSR of the demux FSR_{DM}, which in turn should be greater than the spectral bandwidth of the MLL. Lastly, the roll-off of the filter also matters as it controls the amount of cross-talk. A combination of filter design along with circuit trick like switch-capacitor based integrator can address this issue.

5.5.5 Photodetector and CMOS AFE

The photodetectors convert the sampled and filter optical pulses to current while the CMOS AFE quantizes the samples resulting in the digitization of the RF input signal. The responsivity $\mathcal{R}$ of the photodetector is one of the most critical knobs in improving the O-ADC performance as increasing it incurs no other O-ADC system tradeoffs and linearly improves the ENOB. Also, the analog bandwidth of the detector and AFE is crucial especially when it is not possible to increase the number of interleaving channels and still improvement in a sampling rate of the O-ADC is desired. In such a situation, the repetition rate of the MLL

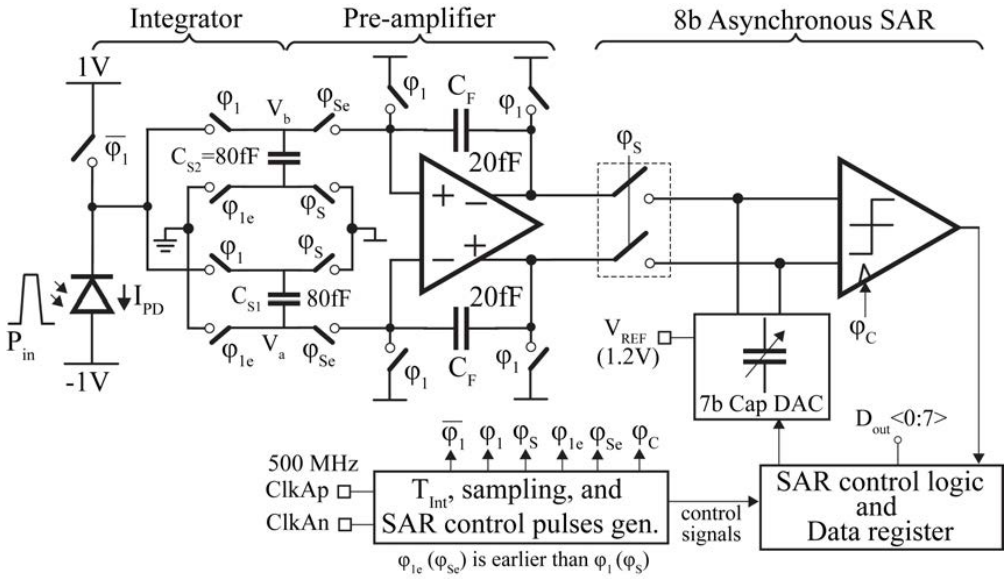


Figure 5.16: Analog-front end and 8b asynchronous SAR ADC.

should be increased which would require an increase in the analog bandwidth of the detector and the AFE. Lastly, the input-referred noise of the AFE is crucial as it can marginally reduce the overall ENOB.

5.6 Circuit Implementation

The optical pulses that are filtered by the double-ring filter are incident on the photodetector, which generates current pulses in response. An analog frontend (AFE), comprising an integrator and a pre-amplifier, and an 8b asynchronous SAR quantizes these current pulses. Figure 5.16 shows the overall circuit implementation of the AFE along with the SAR ADC. This circuit is primarily a switched capacitor-based whose timing diagram is shown in Fig. 5.17. During ϕ_1, the detector current is integrated on the sampling capacitors C_{S1} and C_{S2} for T_{Int} duration. As the optical pulses have a fixed width, the integrator rather acts as an amplifier with gain $\tau/2C_S$ and generates a single-ended voltage across $C_{S1,2}$. To decrease sensitivity to supply and common-mode noise, the ADC is often implemented differentially. As the voltage across $C_{S1,2}$ is single-ended, it needs to be converted to the differential. For this purpose, before transferring charge to C_F in Fig. 5.16, the capacitor C_{S1} is flipped while C_{S2} is connected as is. This is achieved by switching the bottom plate of C_{S1} and the top plate of C_{S2} during phase ϕ_2. Note that while this operation achieves the desired single-ended to differential conversion, the charge transfer from C_{S2} is sensitive to the parasitics, which is mitigated by careful layout and proper sizing.

During ϕ_2, in addition to the charge transfer, the SAR ADC samples the voltage on the

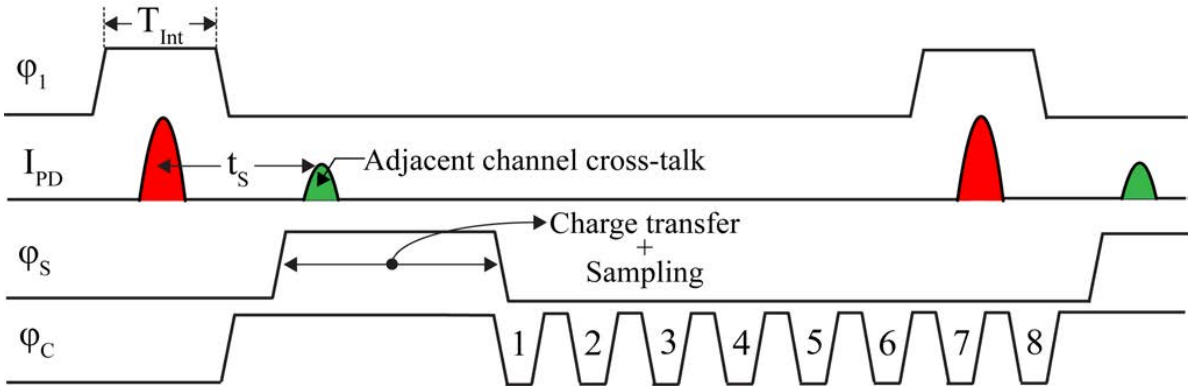


Figure 5.17: O-ADC AFE timing diagram.

top plate of the 7b capacitive DAC. This improves the conversion speed by resolving the first bit without charge redistribution. Once the input is sampled, the asynchronous SAR control logic generates the necessary control signals and comparator clock loop ϕ_C until all 8 bits are resolved. Later in Chapter-6, it is shown that the designed ADC achieves DNL and INL within ±1 LSB when measured at 500 MS/s.

5.6.1 Analog front-end (AFE) and its specifications

The purpose of the analog front-end (AFE) circuits is to convert the photodetector's output current to a voltage such that it can be quantized by the succeeding CMOS ADC. As the output of the photodetector is single-ended the AFE, which is based on switch-capacitor, converts it to the differential. The AFE should perform these operations while maintaining the noise and linearity so as to not degrade the O-ADC SNDR. The peak current expected from the photodetector is around 1.6 mA. To achieve an ENOB of 8b the AFE is designed with a total input-referred current noise of $< 6\mu A_{rms}$ and is clocked at 500 MHz. The anticipated width of the detector current pulses is around 10-20 ps.

The benefits of using a switch-capacitor based integrator as shown in Fig. 5.18 are threefolds. First, by appropriately align the integration window around the current pulses from the present channel the cross-talk current pulses can be completely eliminated. The benefit of this approach is experimentally proven in Chapter-6 where the integration window is deliberately made wider to encompass even the cross-talk pulses. This results in additional spurs in the output spectrum, which degrades the SNDR. Second, by integrating only over the duration of T_{Int} the signal current is adversely affected by the shot noise only in that limited duration. Thus, integrating the current pulses over a narrower integration window helps to minimize the impact of the shot noise. Third, by making the integration duration wide enough the jitter in the CMOS clock that affects the rising and the falling edges of the integration pulse, as shown in Fig. 5.18, does not influence the overall O-ADC performance. However, in order to minimize shot noise if the integration window is significantly made

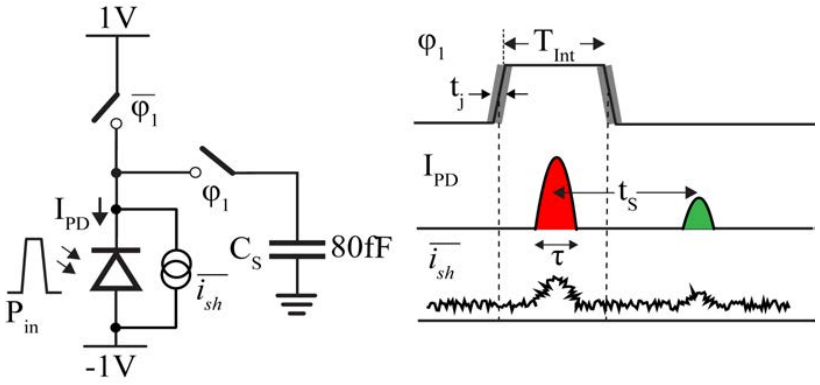


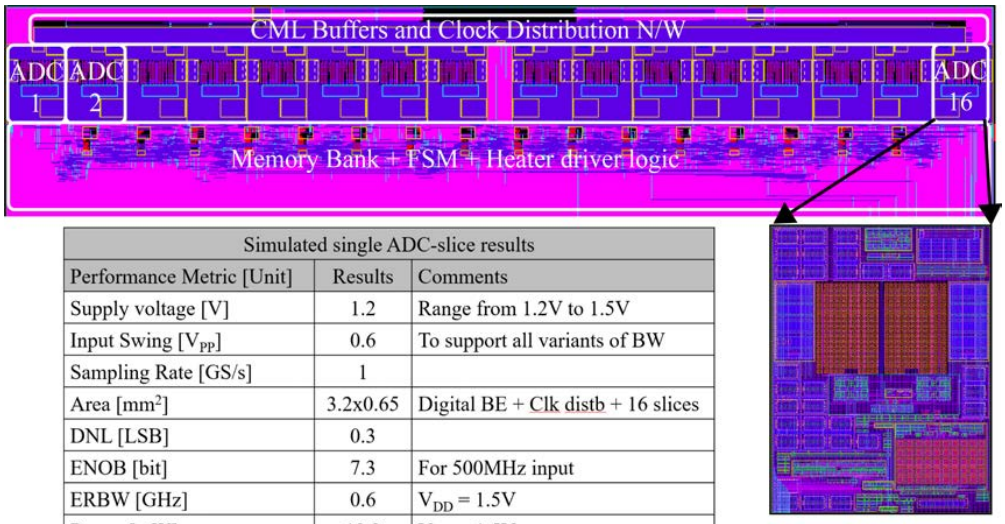
Figure 5.18: Equivalent circuit for the switch-capacitor integrator.

narrower then the CMOS clock jitter can affect the O-ADC performance.

5.6.2 Asynchronous SAR ADC

As shown in Fig. 5.16, during ϕ_2 the charge from $C_{S1,2}$ is transferred to C_F and the 7-bit binary-weighted capacitive DAC that samples the output of the pre-amplifier by top plate sampling. This helps to improve the settling speed and be energy efficient as the first MSB bit can be resolved without redistributing any charge. Thus, for an N-bit ADC, the number of unit capacitors required in the capacitor DAC is half that of the conventional SAR ADC. As will be argued in chapter-6, to limit the distortion from the double-ring filters the maximum incident optical power is restricted. This translates into a maximum peak-to-peak differential swing of 0.7 V at the output of the pre-amplifier helping both the pre-amplifier and the ADC sampling circuit to maintain good linearity. The reference voltage (V_{REF}) is supplied from an off-chip source and is filtered by a total of 640 pF on-chip decoupling capacitor. On the falling edge of the charge transfer pulse in Fig. 5.17 the sample is acquired. After this, the SAR loop runs asynchronously until all bits are resolved. The main benefit of the asynchronous operation is that it removes the need for a high-speed external clock and its distribution network. Besides, it significantly improves the metastability performance of the comparator.

To achieve 8-bit accuracy a fully differential SAR ADC architecture with a monotonic downward switching scheme is used [102]. Here, only one capacitor is switched for every bit cycle reducing the number of transitions and thus, improving total energy efficiency per conversion (pJ/bit). As a result, the common-mode voltage on the capacitor DAC slowly collapses from half V_{REF} to 0V. The SAR ADC conversion rate is limited by the DAC settling, comparator decision delay, and SAR logic delay. As the switching sequence used does not require an upward transition, the DAC settling is improved by optimizing the NMOS pull-down switches [103]. This is necessary as the impact of logic delay gets multiplied by the number of SAR conversion cycles. Further, the comparator used in Fig. 5.16 is similar to that



Simulated single ADC-slice results		
Performance Metric [Unit]	Results	Comments
Supply voltage [V]	1.2	Range from 1.2V to 1.5V
Input Swing [V_{PP}]	0.6	To support all variants of BW
Sampling Rate [GS/s]	1	
Area [mm^2]	3.2x0.65	Digital BE + Clk distb + 16 slices
DNL [LSB]	0.3	
ENOB [bit]	7.3	For 500MHz input
ERBW [GHz]	0.6	V_{DD} = 1.5V
Power [mW]	13.2	V_{DD} = 1.5V
FoM [pJ/bit]	82.3	$P_{Total}/2^{ENOB}\times\min\{2\cdot ERBW, f_S\}$

Figure 5.19: Layout of 16 slices of ADC implemented in 65nm CMOS with summary of simulation results.

implemented in [103] except the input pair of the pre-amplifier is PMOS based to support the input common-mode as low as 0V. The comparator was preceded with a pre-amplifier that absorbed the kickback noise. The capacitor array is realized using metal-oxide-metal (MoM) consisting of only 3 metal layers. This resulted in small capacitance density (pF/μm^2) making the capacitor DAC occupy most of the area. As a small unit capacitor of 1 fF unit capacitor is used to build the binary-weighted DAC, a parasitic aware routing scheme was used.

5.6.3 Digital backend

The output of the ADC is stored in an on-chip memory bank. The size of the memory bank depends upon the sample points needed to be stored, which further depends upon how low the noise floor in the ADC output spectrum should be. The spectrum of the ADC output is obtained simply by computing its FFT, which comprises a series of $M/2$ points in the frequency domain where M is the number of samples stored in the memory. These points are spaced apart by F_S/M and each of these points is often referred to as frequency bins that determine the resolution of the FFT. The noise floor of the FFT is equal to the sum of the SNR of the N-bit ADC and the processing gain, which is given as,

$$\text{FFT Floor} = 6.02N + 1.76 \text{ dB } + \underbrace{10log(M/2)}_{Processinggain} \approx 77dB \tag{5.18}$$

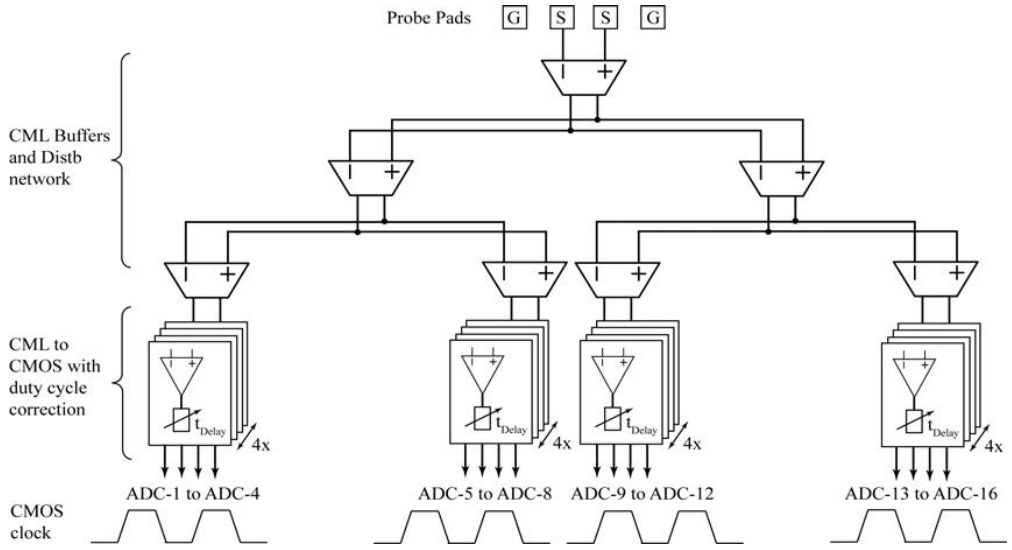


Figure 5.20: On-chip CML clock distribution network and CML-to-CMOS converter at the leaf nodes.

Note that the ADC's quantization noise spans only over the Nyquist bandwidth (i.e. dc to $F_S/2$), while the FFT is a spectrum analyzer with a bandwidth of F_S/M, which pushes the noise down by an amount equal to the processing gain of the FFT as defined by (5.18). Thus, to study and observe all the distortion tones of O-ADC sufficient processing gain is necessary.

The memory bank and the controller FSM are laid out as shown in Fig. 5.19. The main purpose of the FSM is to control the read and write access to the memory bank, and when the memory bank is full the FSM signals an over-flow to the off-chip FPGA, which then reads out the memory data. Lastly, the heater driver logic in Fig. 5.19 essentially implements a PDM based driver as discussed in Chapter-3. It is used to thermally tune the double-ring filters.

5.6.4 CMOS clock distribution

The optical pulse source in Fig. 5.6 also outputs an electrical clock. To preserve the time instances of the optical pulses, the AFE and the SAR ADC operates by using this clock as a reference. The test-bench in chapter-6 gives more information on the locking the ADC clock to the electrical clock at the output of the MLL. As shown in Fig. 5.20, this electrical clock is coupled to the chip using GSSG probe pads. Alternatively, in the test-chip, this clock can also be fed into the chip through wirebonded I/O pads. An H-tree formed using CML buffers distributes the clock to four nodes that generate the CMOS clock for the 16 ADC slices. Each of these nodes has CML-to-CMOS converter with duty cycle correction and coarse and fine delay line for adjusting clock distribution skew. The circuit of Fig. 5.20

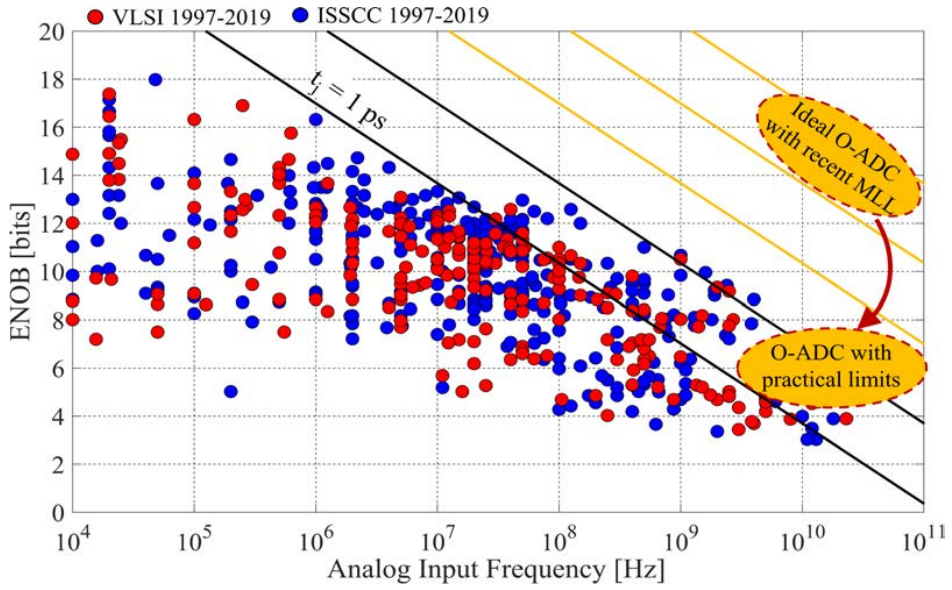


Figure 5.21: ENOB with input frequency for projected performance of ideal O-ADC with state-of-the-art MLL and of O-ADC with practical limitations discussed in this chapter.

is designed to distribute a maximum of 8 GHz clock and it is laid out as shown in Fig. 5.19.

5.7 Summary and Discussion

This part of the thesis demonstrates another system that benefits from the close integration of SiPh with CMOS circuits and resolves the performance bottleneck by offloading certain tasks to the optical domain. In this view, an optically sampled ADC (O-ADC) is demonstrated where the sampling clock jitter and input sampling bandwidth problems are addressed by moving the sampling function to the optical domain. An architecture of O-ADC is shown that is amenable to integration on a single chip implemented in a 3D integration platform. It was identified that the operation of sampling in an O-ADC occurs when the optical pulses are multiplied with the electrical RF input signal using an electro-optic modulator. The bandwidth limitation involved during this process determines the overall sampling bandwidth of the O-ADC. Thus, the limited spectral bandwidth of the demux expands the pulses and limits the bandwidth of the O-ADC, while the electro-optic bandwidth of the MZM (electro-optic modulator) limits the ability to modulate the intensity of the optical pulses. Additionally, a detailed analysis of SNR and linearity of O-ADC is presented that helps to identify and quantify the impact of the number of interleaving channels, modulation depth, and MLL optical power on the ENOB of O-ADC. This impact is highlighted in the performance plot of Fig. 5.21 where the performance of the ideal O-ADC using state-of-the-art MLL source and a practical O-ADC with limitations discussed in this chapter is

predicted.

The limited rejection from double-ring filters introduces interference from the adjacent channels. The magnitude of interference is a strong function of the bandwidth and channel spacing of the double-ring filters. Later, a switch-capacitor-based integrating front-end was shown to completely eliminate the cross-talk by appropriately choosing the integration window. Further, as the modulator's nonlinearity directly translates into spurious harmonics and performance degradation, a linearization approach is shown to minimize the modulator's distortion and enable the use of higher modulation depths. Note that it was shown earlier in this chapter that achieving high modulation depth is crucial for achieving high SNR. Lastly, the limitations of each sub-blocks of O-ADC and their impact on overall performance are outlined.

The implementation of the analog front end (AFE) is also discussed in this chapter. The AFE comprises switch-capacitor based integrator, amplifier, and an 8b asynchronous SAR ADC. A brief description of how these blocks meet the target specifications is outlined along with details of critical sub-blocks like clock distribution and memory bank that stores acquired samples.

Chapter 6

Realization and Measurement of O-ADC chip

To demonstrate the ability of O-ADC architecture, described in Fig. 5.6 in Chapter-5, to sample a high-frequency RF signal with low-jitter optical pulses a test-chip is designed in a wafer-scale heterogeneous 3D integrated SiPh/65-nm CMOS process. This test-chip is intended to be a proof of concept. To simplify the implementation, the optical pulse source and MZM are not integrated on the chip for the time being. However, as the SiPh wafer is independently optimized, new materials are constantly made available which can enable the integration of all or some part of the optical source in the future test-chips. For example, in [104] a monolithically integrated erbium (Er)-doped tunable laser is already demonstrated in this process, while the efforts to integrate other direct emission materials, such as Inp, GaN, and GaAs, on a manufacturable SiPh platform are already on their way [105]. This chapter covers the details of the 3D integration process and its challenges, design of filter-banks and detector, packaging, O-ADC test-bench, and measurement results.

6.1 Heterogeneous 3D Integration of CMOS and Silicon-Photonics at wafer-scale

The O-ADC test-chip is implemented in a fully functional SiPh and 65-nm CMOS heterogeneous 3D integration platform with through-oxide vias (TOVs) interconnects [13]. This process is fully compatible with 300 mm CMOS production that allows a direct transition to volume manufacturing. The key integration process steps are shown in Fig. 6.1. It starts with two 300 mm wafers that are independently optimized for optical and electronics performance. The circuits are designed in 65 nm bulk CMOS LP-process, while the optical devices are fabricated on a 300 mm SiPh SOI wafer with 220 nm Si thickness and 2 μm buried oxide (BOX). Both wafers are fabricated using a precision of 193 nm immersion lithography.

Next, the two wafers are face-to-face direct oxide bonded. The bonding tool aligns the reference alignment marks that are formed on the wafer during wafer processing. The oxide-

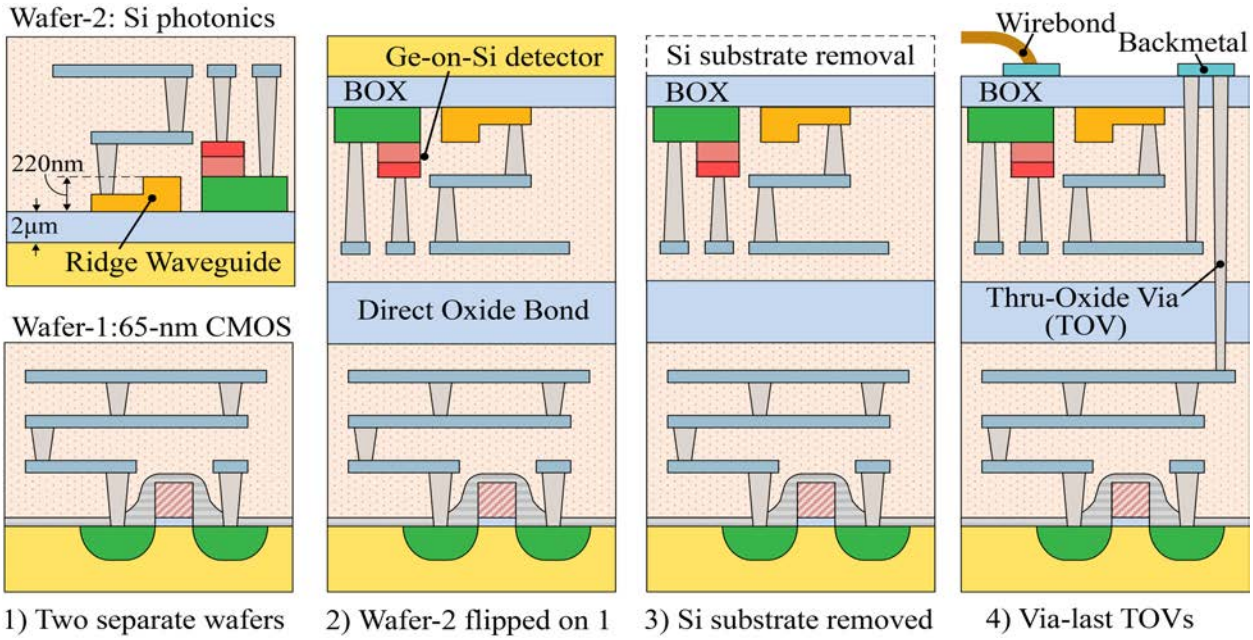


Figure 6.1: An overview of the wafer-scale heterogeneous platform with 3D integrated SiPh and 65-CMOS wafers.

oxide direct wafer bonding relies on hydrogen bond formation resulting from water absorption at the oxide surface. The two wafers, thus, are held together by a network of hydrogen bonds formed over the hydrated surface yielding higher effective bonding energy. While direct oxide bonding enables CMOS process compatible heterogeneous wafer stacking, it requires a clean and atomically smooth surface to ensure a void-free high-bonding strength interface. Surface variations like long-range wafer-scale nonuniformity or pattern-induces topography, particles, or hydrophobic spots prevent hydrogen bond formation that creates a surface defect. These defects are the sites for void nucleation that decrease the bond strength and compromise the process reliability. Figure 6.2(a) shows an image of a reticle with microvoids that appear as white dots all over the reticle. In [13], a specific surface cleaning recipe is used to bring the RMS surface roughness down to 0.1-0.5 nm. Consequently, as shown by the SAM image in Fig. 6.2(b), no white dots are visible indicating virtually zero microvoids over the entire wafer.

Further, once the two wafers are bonded the silicon handle of SiPh wafer is etched selectively stopping at the BOX. This process is done in multiple steps to reduce mechanical stress on the bonded wafers. Lastly, the Cu TOVs are patterned and etched through the entire photonics stack with an aspect ratio of around ∼4:1. These TOVs are ultra-dense with a minimum of 7 μm pitch and have a parasitic capacitance of <3 fF. The dual TOV approach in Fig. 6.1 improves yield by increasing TOV/M2 contact area and manufacturability by avoiding exposure to Cu contamination. Once the TOVs are formed, a backmetal (BM) layer, as shown in Fig. 6.1, connects the photonics and electronics TOVs together,

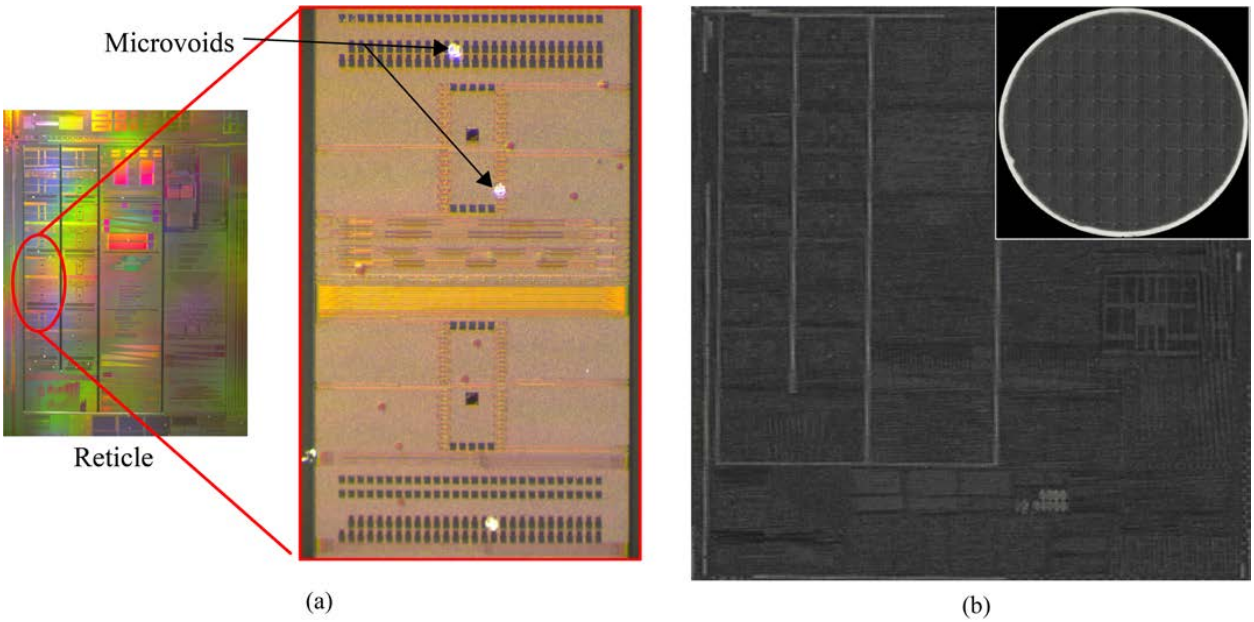


Figure 6.2: (a) A reticle from initial wafer runs that were affected by microvoids (b) SAM of a reticle and a wafer (W130) with zero microvoids.

while also forming wirebond pads. The BM layer is formed just like the other damascene metal levels by etching trenches into the BM IMD, metalized, and polished.

6.2 Optical Blocks

The key optical components used to realize O-ADC are Si waveguide, the edge coupler, tunable double-ring filter bank, and the linear Ge-on-Si detector. The optical performance of these blocks is measured from dedicated test sites and summarized in Table. 6.1 along with salient features of the 3D integration platform.

6.2.1 Tunable Double-Ring Filters

A double-ring filter bank demultiplexes and diverts the optical power at a resonant wavelength from bus waveguide to the photodetector connected to its drop-port. This demultiplexing requires good alignment of the ring's resonant wavelength to the incoming wavelengths, which is challenging to maintain in presence of process mismatch and thermal drifts. An active thermo-optic control loop can address this issue. However, to enable such a loop the tunable double-ring filters with integrated heaters are required. For realizing O-ADC, the tunable interior-ridge double-ring filters with integrated silicon heaters are used [106].

Figure 6.3 shows the structure, cross-section, and scanning electron microscope (SEM) image of a double-ring filter with a 3 μm radius. The bending loss common among rings

Table 6.1: Performance and loss summary of optical blocks in 3D integrated SiPh platform

Parameters	**Value**	**Parameters**	**Value**
Waveguide loss(1500-1600 nm)	3 dB/cm	Filter bank: Ring radius	3 μm
Waveguide width	400 nm	Filter bank: Channel spacing	200 GHz
Process lithography	193 nm immersion	TOV pitch	7 μm
Fiber-to-chip edge coupling loss	3 dB†	Detector: Responsivity	0.9 A/W
Edge coupler bandwidth	100 nm	Detector: Bandwidth	>30 GHz
Filter bank: FSR measured	34 nm (4.3 THz)	Detector: Saturation Power	15 mW
Filter bank: Q-factor	2600$^{\diamond}$	Thermal tuner:R_{Heat}	1.5 kΩ
Filter bank: Drop-port BW	75 GHz	Thermal tuner: Tuning eff.	0.88 nm/mW

†Best measured standalone device $^{\diamond}$With variation of $< \pm 200$ ‡Mean from 32 test-sites

with such a small radius is overcome by using ridge waveguide and fine line edge roughness available in the SiPh platform. To create a ridge waveguide, the outer part of a wider MRR is formed with a 220 nm Si layer on 2 μm BOX while the internal part is etched down by 110 nm. The TE optical mode is strongly confined in this outer ridge waveguide allowing to plant lossless contacts on the inner periphery of the ring without inducing optical losses. Doping offset of 800 nm (see cross-section in Fig. 6.3) reduces the resistance of the integrated Si heater, which is necessary for a wider tuning range as the CMOS heater drivers are often supply limited. The SEM image clearly shows the structure of the ridge waveguide and heater tethers with metal contacts.

For improving the SNR, the bandwidth of the double-ring filters should be wide enough to capture most of the optical power around the resonant wavelength, while having a steep roll-off to avoid adjacent channel cross-talk. The drop-port response shown in Fig. 6.4(a) suggests a 3 dB FWHM bandwidth of around 75 GHz (0.6 nm) and better than 40 dB adjacent channel rejection, both of which are achieved by sizing the bus-to-ring and ring-to-drop gap of 127 nm while keeping 346 nm gap between the two rings. An uncorrupted FSR of 34 nm ($\sim$4 THz) is measured from the drop-port, as shown in Fig. 6.4(b), suggesting a single-mode operation. The resonance of the double-ring filter can shift due to process mismatch or thermal variations. To compensate, the integrated heaters are driven individually by the NMOS drivers, which are controlled using a 10b PDM as shown in Fig. 6.5(a). With a maximum tuning range of 2.5 nm and an efficiency of 0.27 GHz/code (9 μW/GHz), the thermal tuning circuit can move the filter's response to the target wavelengths of λ_1 (=1548.5 nm) and λ_2 (=1550.12 nm), as shown in Fig. 6.5(b).

Figure 6.6 shows the measurement and characterization of the resistance (R_{Heat}) of the integrated heater. A low value of R_{Heat} helps dissipate more electrical power that eventual heats the ring and shifts the resonant wavelength. Thus, achieving lower R_{Heat} increases the thermal tuning range. For this purpose, the integrated heaters are implanted with a p-type doping concentration of 1×10^{18} cm^{-3}. The 8 heater tethers connect the integrated heater to the metal vias. These tethers are p+ type doped with concentration of 1×10^{20}

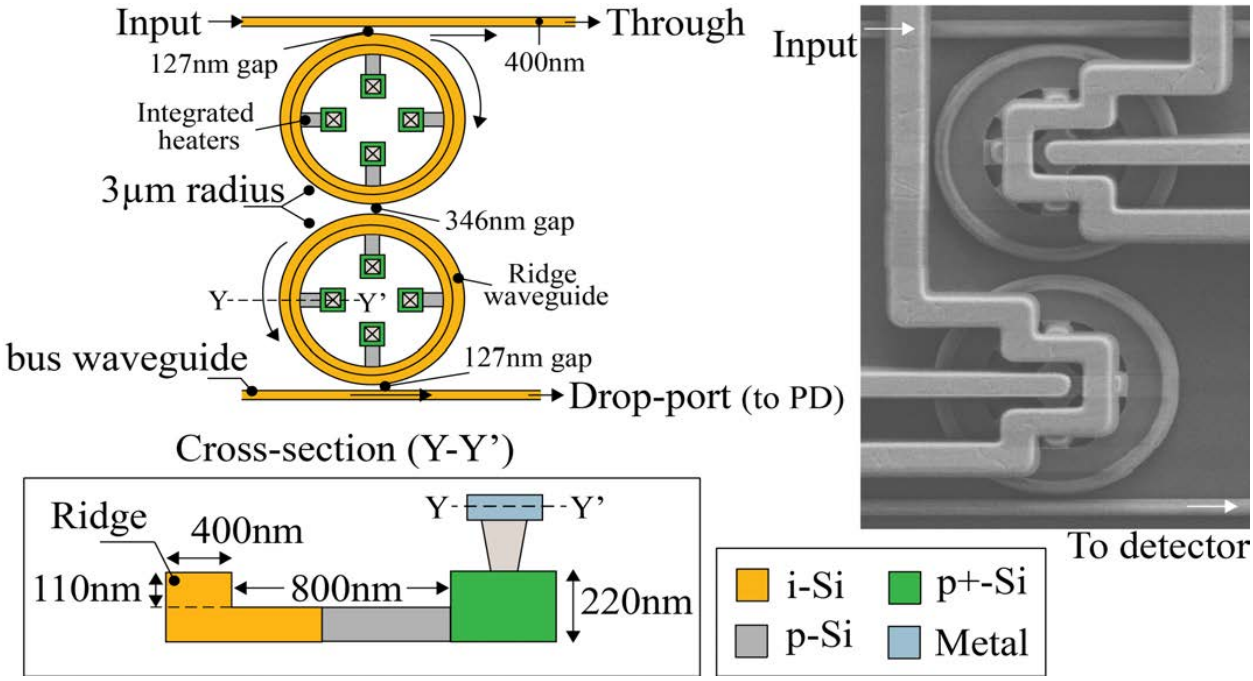


Figure 6.3: A double-ring filter bank, it's cross-section, and SEM image.

cm^{-3}. Subsequently, the R_{Heat} with a mean of 1.5 KΩ is achieved.

6.2.2 Vertical *p-i-n* junction Ge-on-Si Photodetector

Another important optical block of O-ADC is the linear photodetector. The structure of the Ge-on-Si detector is shown in Fig. 6.7. Its structure is described in detail in [107]. The germanium layer is heteroepitaxially grown on top of heavily p-doped silicon formed on the silicon. A vertical *p-i-n* junction is formed by doping the top of the germanium layer by n-type dopant. The metal contacts to the n-doped germanium and the p-doped silicon are routed to the TOVs BM pad, which is further connected to the CMOS O-ADC AFE by TOVs. The width of the germanium layer is 4 μm and the detector's length is 12 μm. The detector is connected at the drop-port of the double-ring filter through a taper that is coupled with 100 nm spacing. The measured dark current of the Ge-on-Si detectors was <10 nA with -1 V reverse bias, while its responsivity is 0.9 A/W at 1550nm with 30 GHz bandwidth. The measured saturation power of the detector is >10 mW, which is in line with that reported in [107].

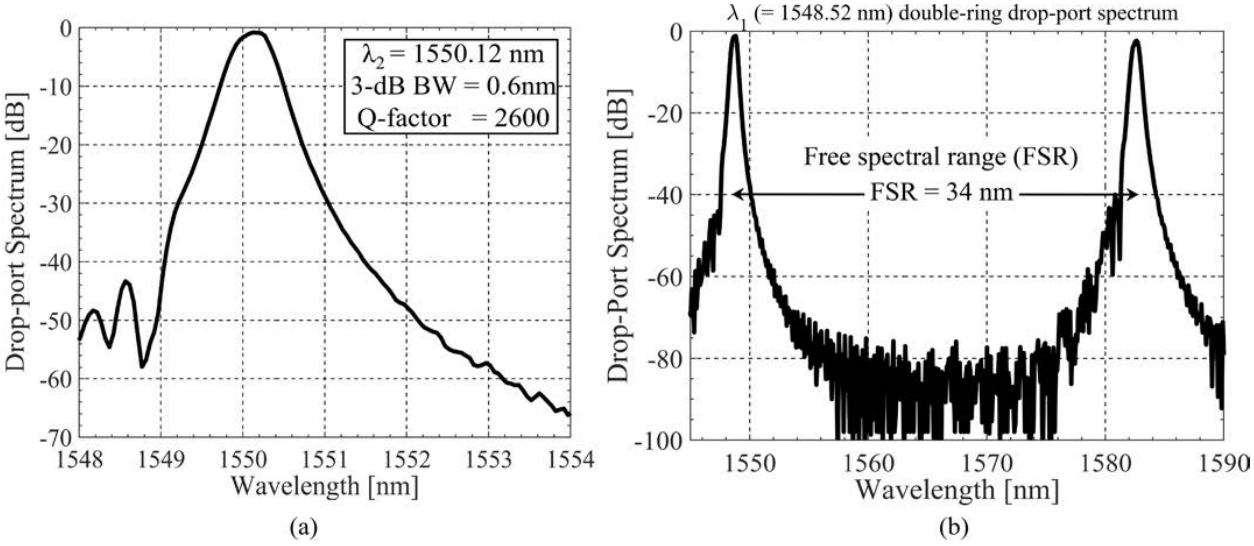


Figure 6.4: Drop-port response of a double-ring (a) around λ_2 and (b) over a span of an FSR.

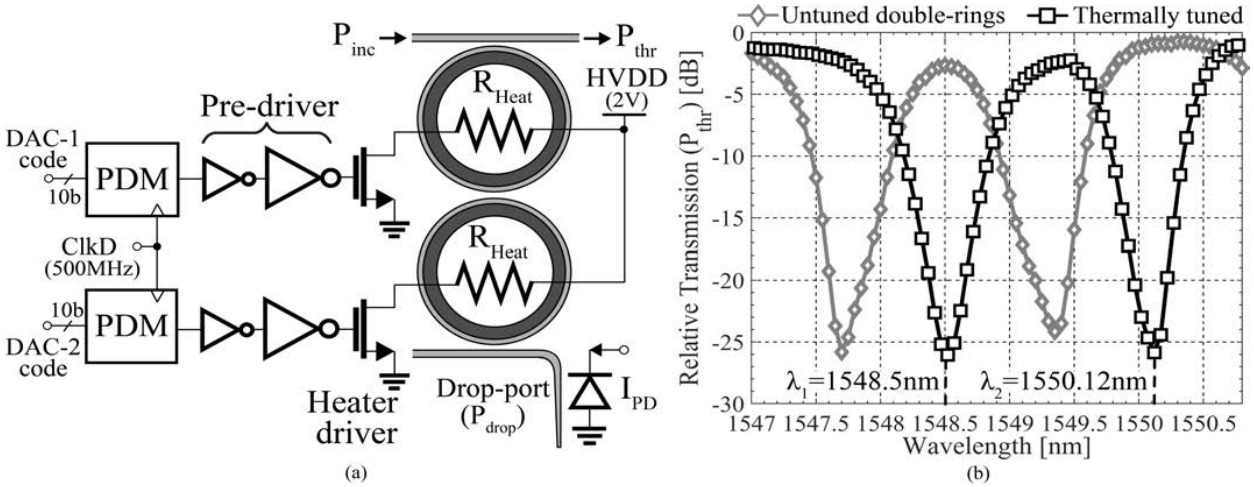


Figure 6.5: (a) Heater driver circuit and (b) double-ring transmission before and after thermal tuning.

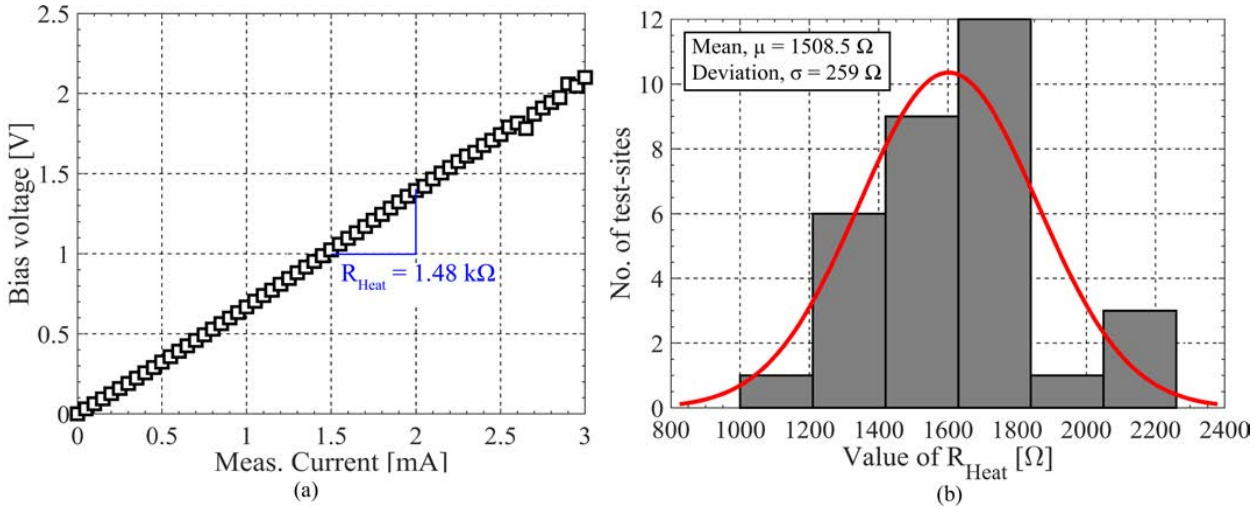


Figure 6.6: (a) Measured I-V plot and (b) distribution of R_{Heat} measured over 32 test-sites.

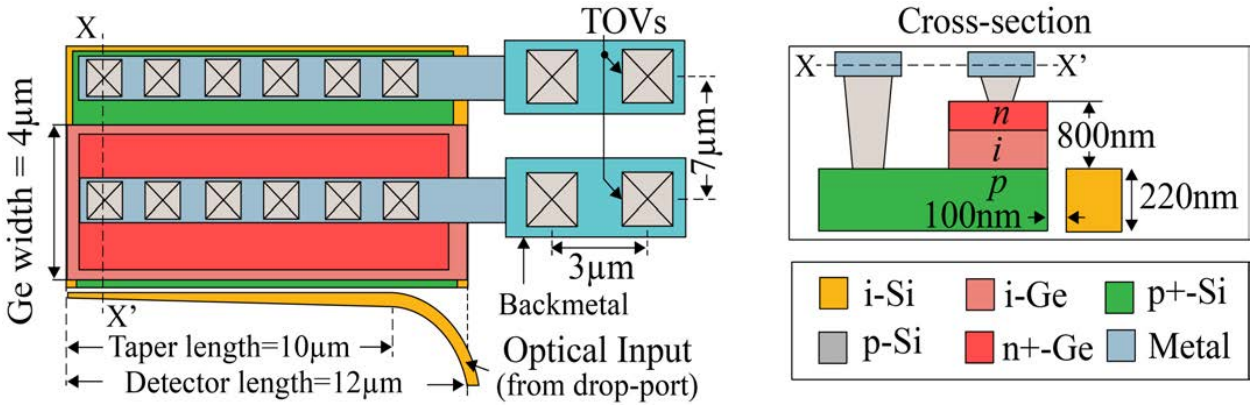


Figure 6.7: Linear Ge-on-Si photodetector and it's cross-section.

6.3 Test-chip packaging and fiber coupling

The test-chip is fabricated at the wafer-level. Figure 6.8 shows the photo of the finished 3D integrated SiPh and 65 nm CMOS wafers. Each reticle carries 8 O-ADC chips with variants of double-ring filter banks. An array of 16 SAR ADCs is implemented in each O-ADC chip. However, to keep the complexity in the generation of 16 interleaved pulses manageable, only two adjacent SAR ADC slices in Fig. 6.8 are functionalized. The zoomed inset micrograph of the photonic chip shows the structure of double-ring filters, a detector, and the connection made to the TOV BM pads. The IR image of the chip shows the glowing rings that suggest the optical power is captured in the rings. The 3.3 mm × 5 mm test-chip is packaged in a standard PGA208 ceramic package.

To enable edge coupling, as shown in Fig. 6.9, the vertical edges of the chip are diced

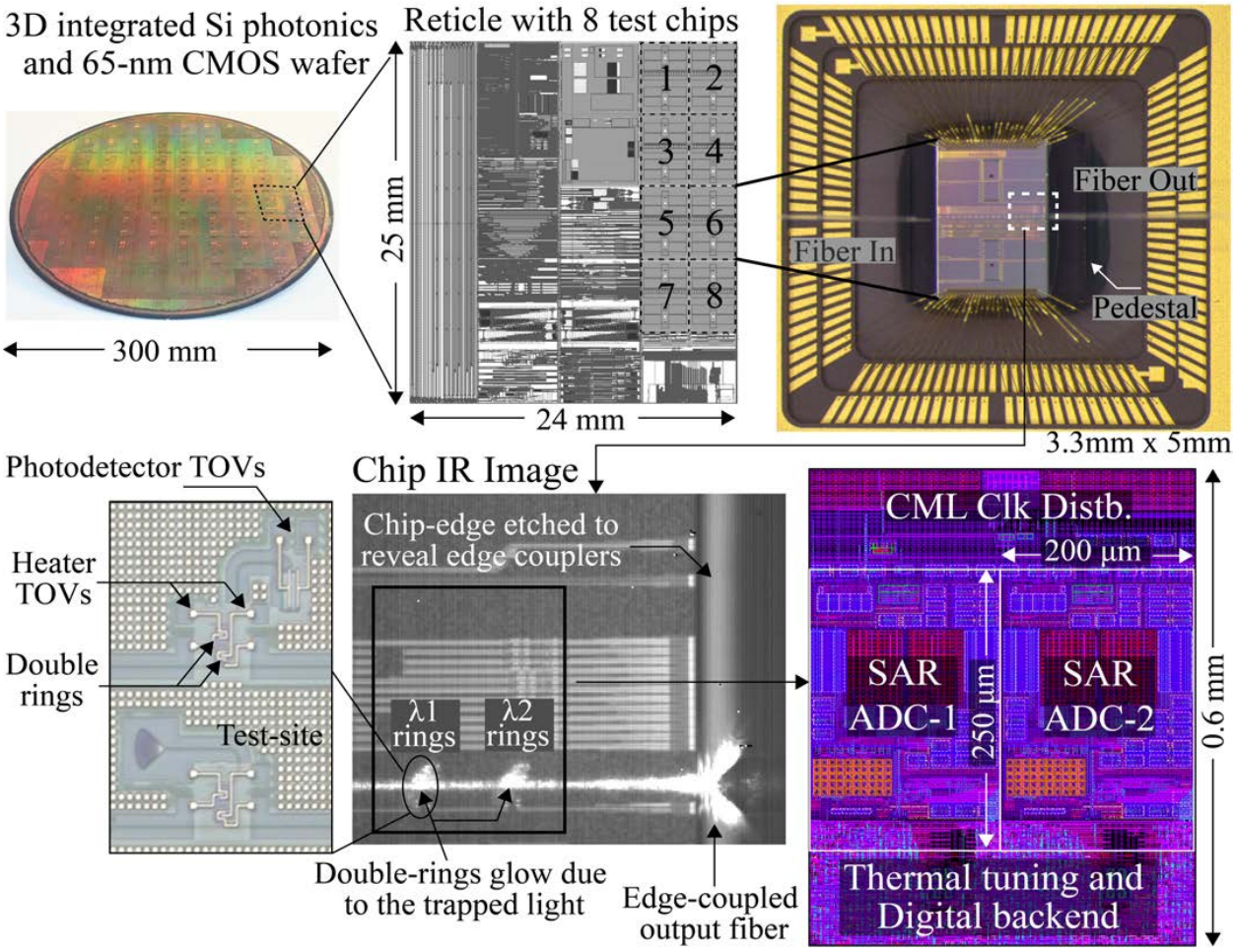


Figure 6.8: Wafer photo, packaged test-chip, and die photo with SAR ADC layout.

and wirebonds placement is limited only to the top and bottom edges of the chip. The chip is placed on a borosilicate glass pedestal to raise the chip above the PGA package cavity allowing fibers to couple into the chip edge. To achieve good coupling efficiency, lens fibers are used with 2.5 μm spot diameter.

6.4 Test bench

The O-ADC chips are characterized using the test-bench shown in Fig. 6.10. The key components of the test-bench are a high-power ELMO MLL source (marked (1) in Fig. 6.10) [108] and a $LiNbO_3$ MZM from EOSpace Inc with 40 GHz of 3-dB bandwidth (marked (7) in Fig. 6.10). The MLL outputs optical pulses with width 0.15 ps and a 100 MHz repetition rate. The output of the MLL is first demultiplexed using a DWDM optical demultiplexer with 200GHz spacing. This operation chops the spectral bandwidth of the MLL into two

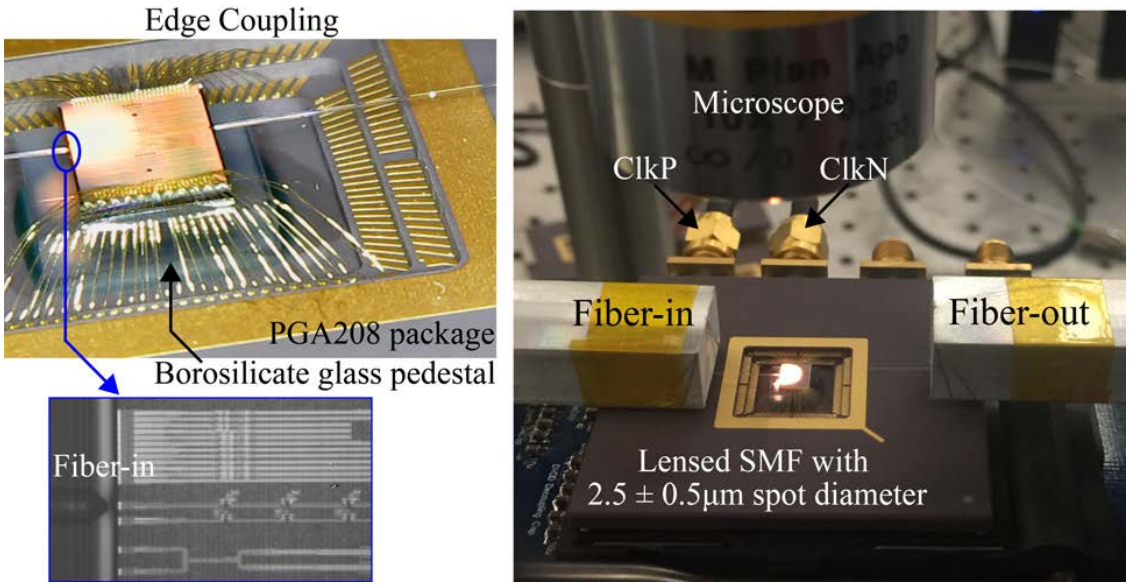


Figure 6.9: Fiber-to-chip edge coupling on a packaged test-chip.

smaller bandwidths around λ_1 and λ_2, which expands the pulses from 0.15 ps to 3 ps while reducing the pulse amplitude equivalently. One of the output branches of the demultiplexer is delayed by 250 ps using an SMF fiber delay. The polarization of the two paths is then adjusted and multiplexed again creating 250 ps spaced optical pulses. Due to attenuation from the demux-delay line-mux interleaver, the optical power at the output of the multiplexer is substantially small. An EDFA is used to restore the optical power before it is coupled into the O-ADC test-chip.

While two interleaved optical pulses are enough to demonstrate, interleaving more pulses would require additional fiber delays and polarization controllers that complicates the optical test-bench. However, the interleaver can be integrated into a future SiPh chip test-chips [109].

The measured phase noise of the optical pulses was better than 25.1 fs_{rms} limited by equipment precision. The noise floor in Fig. 6.11(b) was determined by photodetector's shot noise. The pulse-width estimated using a femtosecond autocorrelator reveals a pulse-width of <3 ps, which is limited by the bandwidth of the optical demultiplexer. For further reduction in pulse-width, an optical demultiplexer with wider bandwidth is required.

6.5 Measurement Results

The static performance of the detector can be characterized by a $\log I_D$-V plot as shown in Fig. 6.12(a). It is apparent that under the dark condition at -1 V reverse bias the dark current of the detector is <10 nA. As a result, the dark-current component of the shot-noise is negligible. Increasing the input optical power (P_{inc} in Fig. 6.5(a)) increases the

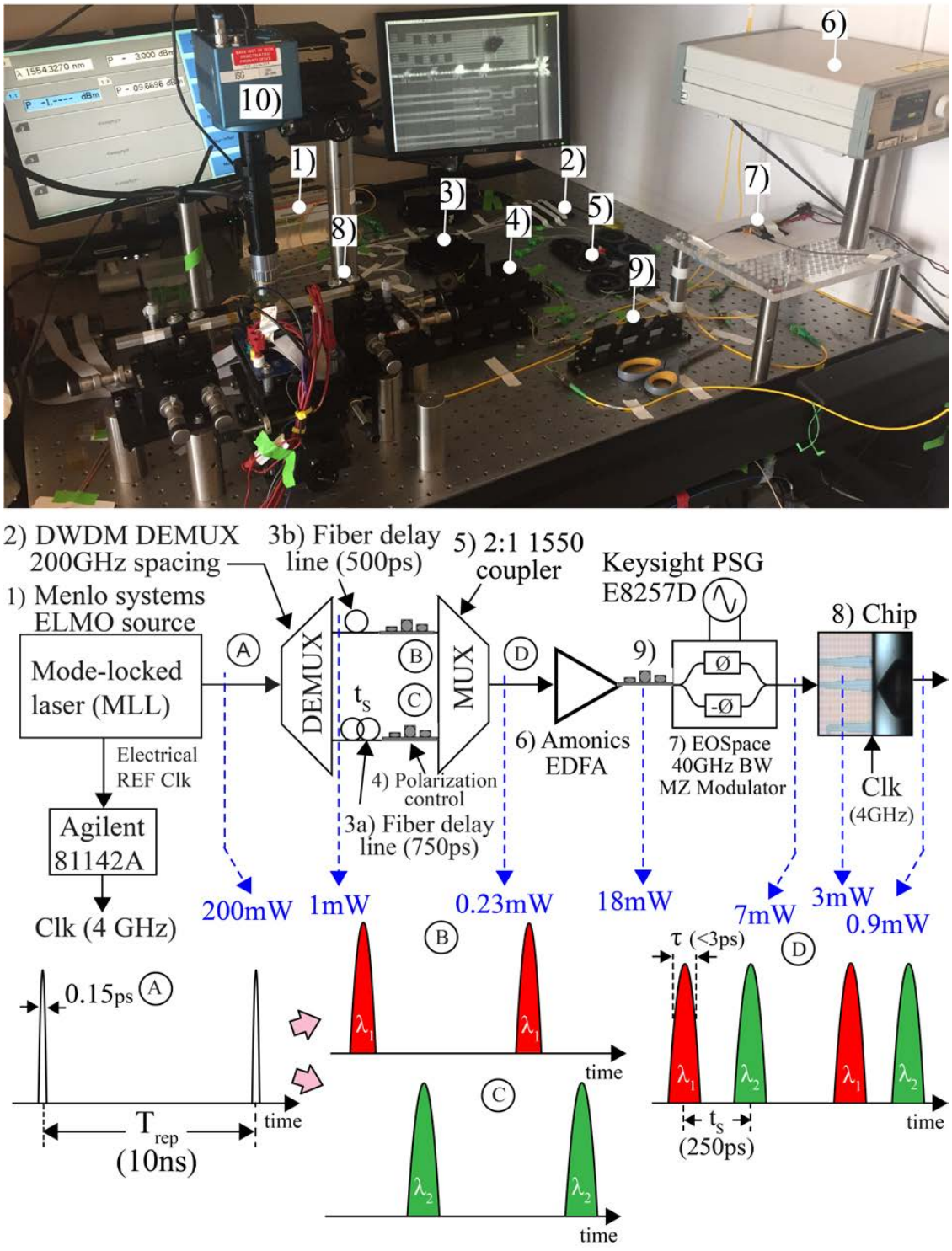


Figure 6.10: Test-bench used to characterize O-ADC performance.

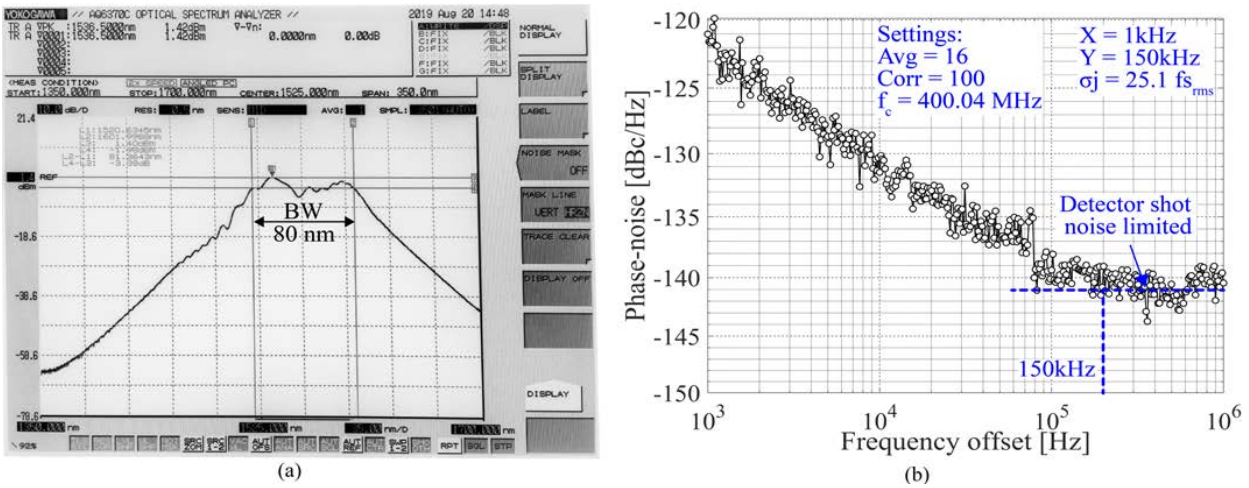


Figure 6.11: (a) Bandwidth and (b) phase noise measurement of ELMO MLL-based optical pulse source.

SNR. However, the double-ring filters often tend to distort for high incident optical power. This maximum incident optical power is depicted in Fig. 6.12(b) where the photocurrent in response to the optical power in the bus waveguide of the double-ring filter is shown. As evident, the double-ring filters operate linearly for optical power below 8 mW. However, for higher optical power it exhibits a compressive distortion, which can degrade the overall SNDR of the O-ADC. Thus, the input power to the test-chip is limited such that <8 mW power hits the double-rings. Fig. 6.12(c) shows the measured DNL and INL at the output of the SAR. While both DNL and INL are $< \pm 1$ LSB, the cubic form of INL indicates odd-order distortion from the push-pull amplifier in the AFE being the dominant source.

Further, the performance of the O-ADC is evaluated using a single tone RF input applied as a test signal driving the MZM. The output of the O-ADC is recorded on the on-chip memory bank and readout using scan registers. To obtain an optimal ADC performance following the calibration procedure is applied to the raw data before the plotting the spectrum. The primary purpose of O-ADC is to demonstrate optical sampling. Subsequently, to simplify post-processing foreground calibration is performed.

1. The mismatch between the two channels is first compensated. The offset is measured in the foreground with no input applied and subtracted from the raw data.

2. The difference in gain of the AFE, the mismatch in the double-rings, and the mismatch in detector's responsivity induces a gain error. To compensate for it, a known input is applied and the raw data is scaled in the backend.

3. Lastly, the harmonic distortion of the MZM is canceled as shown in [110, 99]. Say the

output of the two channels is y_1 and y_2, which is expressed as,

$$y_1 = K_{1a} \cdot arcsin(K_{2a} \cdot V_{in}/K_{3a} + K_{4a}) \quad (6.1)$$
$$y_2 = K_{1b} \cdot arcsin(K_{2b} \cdot V_{in}/K_{3b} + K_{4b}) \quad (6.2)$$

The overall the overall output of the O-ADC is y_{out} is simply y_1+y_2. By appropriately scaling the coefficients K_{1a} to K_{4b} in (6.1) and (6.2) the nonlinearity of the MZM can be completely eliminated as long as the AFE of the O-ADC is perfectly linear and has high-enough bandwidth. In practice, as the AFE has finite nonlinearity, the MZM nonlinearity cannot be completely canceled.

4. As the sampling instance is set by the fiber delay, it is precise and stable. During the measurements, significant timing error was not observed and hence, no calibration for timing mismatch is performed.

After performing the calibration as outlined above, the O-ADC output spectrum is as shown in Fig. 6.13(a). As the pulses are 250 ps apart, the effective sampling rate achieved is 4 GHz. The spectrum in Fig. 6.13(a) with gray lines is the one before calibration. Additionally, to study the impact of cross-talk the integration window is deliberately widened, by setting T_{Int}=2t_S, so that the current pulses from neighboring channels also get integrated on the sampling capacitors. This induces spurs that are identified by the × marker. When T_{Int}(=t_S) is correctly chosen and proper calibration is applied the SNDR improves from 34 dB to 39.5 dB as shown in Fig. 6.13(b). Figure 6.13(b) shows a spectrum for 44.73 GHz input tone at an equivalent sampling rate of 4 GS/s. While this sampling is below the Nyquist rate, the input tone and all of its harmonics are aliased down to the Nyquist band, while preserving signal, distortion, and noise power. The estimated upper bound on the sampling jitter computed from the measured SNR of 40 dB is 36 fs_{rms}. This done by using the following expression,

$$t_a = \frac{1}{2\pi f_{in}} \sqrt{(10^{-SNRH/20})^2 - (10^{-SNRL/20})^2} \quad (6.3)$$

Here, t_a is the sampling jitter, SNRH is the SNR at f_{in} of 44.73 GHz, while SNRL is the SNR at low input frequency. The expression in (6.3) provides an estimate on sampling jitter. Getting an accurate measurement of t_a is quite challenging as the jitter from the input signal or the jitter induced from the layout, signal routing, grounding, etc, cannot be isolated.

As illustrated in Fig. 6.13(b), the linearity at high frequency is limited by the residue HD3 from the MZM. This is also evident in Fig. 6.14(a)-(b), where the SFDR and thus, SNDR increases for higher input frequencies. Measurements beyond 45 GHz were limited by the combination of the 3-dB bandwidth of the MZM and limited optical pulse width. Table 6.2 summarizes the performance of the O-ADC and compares it with the recent state-of-the-art optically sampled ADCs and electronic ADCs. This design is the first demonstration of an optically sampled ADC with 6b ENOB and being fabricated in a CMOS foundry. The work in [111] requires the growth of GaAs to realize an optical switch, which may not be

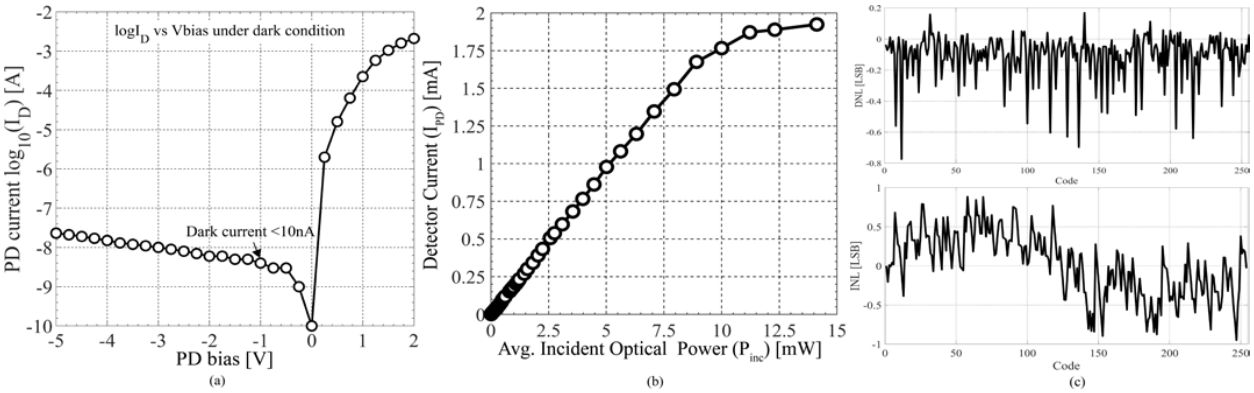


Figure 6.12: Measured plots of (a) $\log I_D$ with detector bias current (b) Detector's current with incident optical power and (c) DNL/INL of the 8b asynchronous SAR.

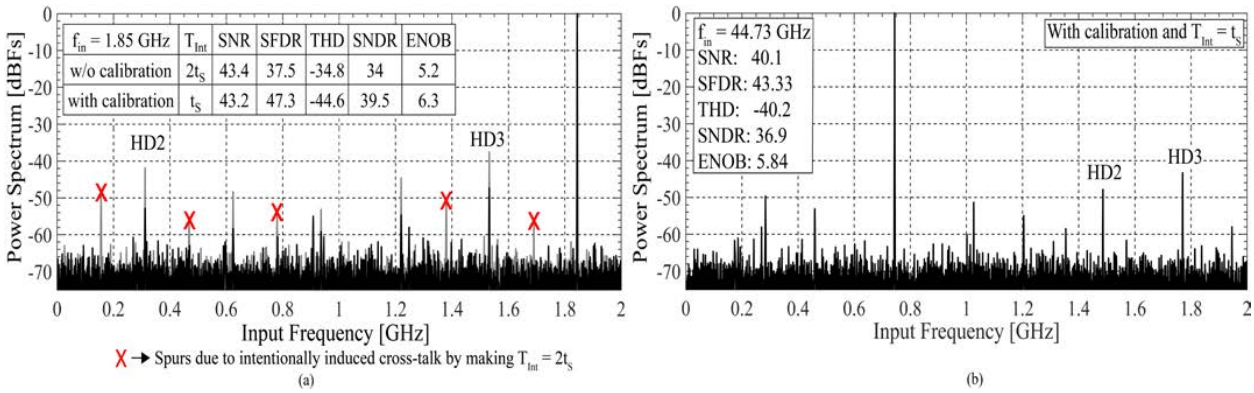


Figure 6.13: Spectrum of equivalent time sampled signal with input tone at (a) 1.85 GHz and (b) 44.73 GHz.

fully compatible with CMOS manufacturing. Besides the large feedthrough capacitance in the hold phase limits the performance of the ADC to only 4 bits. Further, the present design achieves the highest SNDR for >40 GHz input [83] and the first design to report SNDR measurement beyond 40 GHz. Table 6.3 shows the power breakdown of the test-chip and the power consumed by the optical pulse generator. The optical pulse source consumes the power of 4 W, a drawback common among systems that attempt to use optical pulses as a time reference. However, this pulse source can be relatively remote eliminating the need to draw this much power on the same chip as the O-ADC itself.

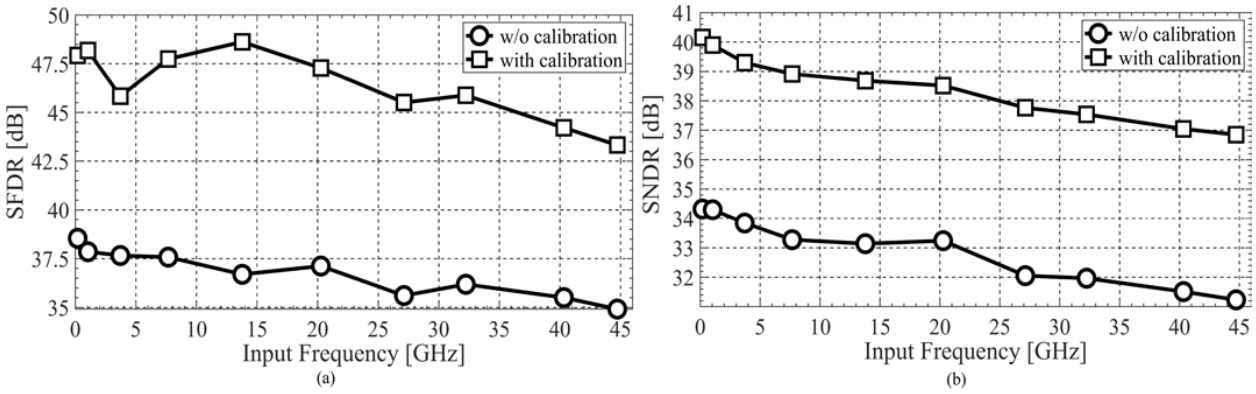


Figure 6.14: Measured (a) SFDR and (b) SNDR with input frequency.

Table 6.2: Performance summary and comparison with state-of-the-art high sampling bandwidth ADCs

Parameters	**This Work**	**[111] JSSC'03**	**[112] CLEO'11**	**[113] VLSI'18**	**[114] ISSCC'10**
Sampling Architecture	Optical pulse based			Electrical (Direct sampling)	
Technology	3D Integrated SiPh w/ 65nm	250nm CMOS w/ LT GaAs	Discrete off the shelf	14nm FinFET CMOS	65nm CMOS
Supply Voltage [V]	1.2/1.5/2	2.5	2/5†	0.8/0.95*	1/1.2/2.5
Resolution [bits]	8	4	9	10	6
Conversion Rate [GS/s]	4	0.16	2	32	40
SNDR at low input frequency [dB]	40.2	24†	-	47.3	34.9
High input frequency ($f_{in,high}$) [GHz]	44.73	40	40**	39.8	18
SNDR at $f_{in,high}$ [dB]	36.9	23.4	43.8	37.8	25.2
Power [mW]	88$^{\#}$	140$^{\#}$	-	199	1500
SNDR at $f_{in,high}$ [dB]	36.9	23.4	43.8	37.8	25.2

*SAR ADCs/Interleaver+Sampler †Estimated from available data

**Signal source limited ‡Includes optical blocks $^{\#}$Electrical power only

Table 6.3: Electrical and optical power breakdown of O-ADC

Sub-blocks	**Supply [V]**	**Power [mW]**	**Sub-blocks**	**Supply [V]**	**Power [mW]**
AFE (Integrator + Amplifier) (x2)	1.5	42.2	CML Clk distb + delay lines	1.5	5.8
Async SAR @500 MS/s (x2)	1.5	24	Heater Driver (x4)	2.0	3
Thermal tuning logic @500 MHz (x4)	1.2	3.2	Memory bank + control logic	1.2	9.8
Optical power required by O-ADC		7	Optical pulse source power consumption		4000

6.6 Summary

A realization and implementation details are covered in this chapter. A test-chip of O-ADC is implemented in a wafer-scale heterogeneous platform with 3D integrated CMOS 65nm and SiPh wafers. The two wafers are connected using high-density TOVs. The problem of microvoid formation at the oxide interface was addressed by ensuring an atomically smooth wafer surface. The double-ring filter and linear Ge-on-Si detectors are designed in the 3D CMOS/SiPh platform. The O-ADC chip is packaged and wirebonded in a standard ceramic PGA208 package. A glass pedestal is used to elevate the chip and facilitate edge coupling. The performance of O-ADC is measured using an MLL-based optical test-bench that generates optical pulses with 26fs jitter and 250ps spacing to sample the input signal. The incident optical power is limited to <8 mW to avoid distortion from double-ring filters. After applying proper calibration, the performance of O-ADC is measured. It achieves 6b ENOB over an input range of 2MHz to 45GHz and 37dB SNDR at 45GHz input with <36 fs estimated sampling jitter.

Chapter 7

Conclusion

While CMOS scaling is likely to continue, the development of recent technology nodes, such as 14 nm and 10 nm, has taken longer than usual. Increased process complexity is in part responsible for this slow down of CMOS scaling. Silicon photonics (SiPh) has emerged as a viable technology capable of extending and continuing Moore's law. Just like integrating the inductor revolutionized the CMOS RF design, integration of active and passive photonic devices with CMOS is greatly positioned to revolutionize a number of analog and mixed-signal applications. This thesis is an attempt in that direction. Here, two systems are described that benefit from close integration for photonics with CMOS. The performance benefits derived are outlined below:

I. Optical links that requirer less laser power

The SiPh links are well suited for co-packaging with SoCs that demand high-throughput, like switch ASIC. However, due to high link losses, these SiPh links end up requiring substantial laser power. This limits the amount of improvement in energy-efficiency that SiPh links can achieve. To address this problem, in this thesis, it was identified that limited sensitivity of the optical receiver (Rx) and higher link losses are mainly responsible for the high laser power requirement of SiPh links. Both, Rx sensitivity and link losses can be improved by leveraging the availability of photonics next to CMOS.

- The breakdown of various sources affecting sensitivity reveals power-supply and common-mode noise being one of the dominant factors. To suppress it, a fully differential photodetector using an adiabatic 3-dB coupler was implemented in version-1 of high sensitivity optical Rx test-chip. While the chip performed as expected, the coupling ratio of the coupler was sensitive to the wavelength of operation. This requires additional calibration steps, which can limit the practicality of the Rx. Besides, the coupler was sizeable and nonconformal to DWDM realization.

- The drawbacks of version-1 test-chip were overcome in the version-2 chip, where a differential detector is realized using microring resonators (MRR). Due to the availability

of a photonic design kit in a CMOS process, the functionality of differential operation was realized simply by appropriately wiring of *P-N* junctions. The MRR PD had 0.55 A/W responsivity at 1275 nm and a current splitting error of $< \pm 0.3\%$. The low parasitic capacitance of MRR PD increased the transimpedance limit and enabled the use of high feedback resistance to minimize the thermal noise. Consequently, the optical Rx achieves an OMA sensitivity of -18.2 dBm at 12 Gb/s, which is among one of the best reported for mid-data rate receivers.

- Apart from sensitivity, reducing optical link loss is equally critical. For this purpose, using the improved sensitivity optical Rx a laser-forwarded (LF) link is demonstrated that forwards a part of the laser directly to the Rx. Thus, the photocurrent at the Rx is only affected by a geometric mean of the lossy signal path and low-loss forwarded path. All the necessary optical blocks like MRR phase-modulator, 3-dB coupler, and MRR balanced PD are integrated with CMOS circuits in a GFUS 45nm SOI monolithic SiPh platform. The link operates at 10 Gb/s with 2.3 pJ/bit energy-efficiency and BER $<10^{-7}$, which was limited by phase-drift induced due to laser phase noise.

The design of SiPh links offers interesting and exciting challenges that can be explored in the future. In the near term, the data-rates of the optical Rx and LF link demonstrated in this thesis can be extended beyond moderate data rates ($\sim$10 Gb/s) by employing equalization schemes. To increase overall throughput, a dense wavelength division multiplexed Rx system can be readily realized using the Rx reported in this thesis. In the longer term, solving the packaging problem for the SiPh links is another exciting research topic. Packaging SiPh links in a multi-chip module (MCM) along with SoCs such as FPGAs, graphical processing units (GPUs), central processing units (CPUs), and switch ASICs. Such a hybrid package solution can enable rapid movement of data in and out of the SoCs that would be important in applications like AI accelerators, handling machine learning workloads, etc. To encourage research in this direction DARPA recently launched a new program named, Photonics in the Package for Extreme Scalability (PIPES) [115] aims to embed integrated SiPh links into cutting-edge MCMs and create advanced optical packaging to address the data movement demands of highly parallel systems.

II. Optically sampled Analog-to-digital converters (O-ADC)

Another system that takes advantage of the integration of SiPh with CMOS transistors is the O-ADC. Here, the performance limitations imposed by finite input sampling bandwidth, sampling clock jitter, and challenging routing of input/ clock path, are resolved by using optical pulses. Thus, the task of sampling an input RF signal is moved to the optical domain where low-jitter optical pulses can readily realize precise sampling. To this end, a two-channel O-ADC is implemented in a wafer-scale heterogeneous platform with 3D integrated 65-nm CMOS and SiPh using high-density TOVs. An optical test-bench based on ELMO MLL generates optical pulses with 26 fs_{rms} jitter pulses and 250 ps spacing. The measurement of

the O-ADC chip demonstrates an ENOB of 6b over an input range of 2 MHz to 45 GHz and 37 dB SNDR at 45 GHz input with <36 fs estimated sampling jitter.

The O-ADC system described in this thesis was mainly intended to serve as a demonstration with many further improvements possible. First, the T_{Int} generator should be able to generate an arbitrary pulse width and not defined by the clock-edges. This would allow for finer and closely spaced integration pulses. To realize a highly integrated O-ADC, the interleaved should be integrated on the SiPh chip [109]. This would enable higher interleaved channels increasing the throughput of the O-ADC. Further, the MZM should also be integrated on the SiPh chip with the MZM pre-driver being implemented on the CMOS chip. This would enable an O-ADC system at a multi-chip scale. Lastly, for achieving 100 GS/s O-ADC, increasing the repetition rate of the MLL is necessary. For instance, in [116], a 100 GS/s O-ADC is described that uses 10 GHz repetition rate MLL with 1.5 ps pulse width [117]. In the future, it might be possible to even integrate MLL source on the SiPh chip. Recently, DARPA announced a new program named, Lasers for Universal Microscale Optical Systems (LUMOS) with a goal to co-integrate direct-emission materials, such as InP, GaN, and GaAs, with low-loss dielectric materials such as silicon and silicon nitride to create accessible, manufacturable optical microsystems [105].

Finally, the systems discussed in this thesis are just two examples of many exciting possibilities enabled by integrating silicon photonics with CMOS. Recently, many other novel applications have started to emerge. Recently researchers in [118], have shown an optical neural network that can handle inference tasks with significantly higher computational speed, while in [119] a highly sensitive MRR-based electrochemical biosensor is shown for multiparameter biomarker profiling that can open new modalities for molecular-level sensing. Besides, the high interconnect density between integrated transistor and photonics enables new applications like integrated LiDAR [120] and integrated CPU-memory links [28].

The main premise at the start of this thesis was that integrating CMOS and photonics not only reduces routing parasitics but also can enhance overall system performance by offloading certain operations to the optical domain. Thereby the performance bottlenecks are resolved, which neither CMOS nor photonics can achieve on their own. As this thesis concludes it is encouraging to witness emerging efforts that would package photonics with cutting-edge multi-chip modules [115, 121] or extend the usability of the SiPh platform by integrating novel materials [105]. It is also encouraging to observe SiPh going beyond the shadows of being the technology of the future, and delivering real products that are rapidly replacing electrical I/Os in data centers. For instance, Luxtera shipped near 2 million SiPh transceivers in 2018 before its acquisition by Cisco. Intel is already shipping 100G PSM4 SiPh transceivers and in early 2019 demonstrated their SiPh transceiver product for the next generation 400 GbE standard. Today, almost all major foundries have the SiPh platform as one of their process offerings. Combined this with the availability of photonic CAD tools, design kits, and developed understanding of SiPh technology, the designers can now realize the full potential of integrating SiPh with CMOS. Consequently, like the integration of inductors revolutionize CMOS radios, SiPh is also likely to revolutionize data movement and compute applications. It's only a matter of time.

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