NEGATIVE RESISTANCE CURVE TRACER

by

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NEGATIVE RESISTANCE CURVE TRACER†

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Abstract

Tracing the negative resistance characteristics of 2-terminal and 3-terminal devices often ended in failure due to jump phenomenon, hysteresis, and oscillation resulting from the tracing circuit. All of these problems are overcome in the curve tracer described in this paper. A detailed nonlinear dynamic circuit analysis is used to develop a simple method for quenching oscillations and other exotic phenomena.

Our curve tracer is designed to trace either voltage-controlled or current-controlled negative resistance characteristics of both 2-terminal and 3-terminal devices. All six representations which completely characterized a 3-terminal or 2-port nonlinear resistor are allowed. In particular, using a novel approach for implementing a nullator and norator, transmission (chain) characteristics of 3-terminal and 2-port devices have been successfully traced for the first time.

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1. INTRODUCTION

A 2-terminal negative resistance device (Fig. 1(a)) is one whose voltage versus current (v-i) characteristics exhibits a negative slope over some region of the device's operating range. Since the v-i characteristic of any physical device must eventually lie in the first and third quadrant (i.e., they must be eventually passive) even if the device is biased by batteries, a 2-terminal negative-resistance device characteristic is either voltage-controlled (type N) as shown by the hypothetical curve in Fig. 1(b), or current-controlled (type S) as shown by the hypothetical curve in Fig. 1(c).

A 3-terminal negative resistance device (Fig. 2(a)) is one whose family of characteristics has at least one curve in the $v_1-i_1$ plane or $v_2-i_2$ plane exhibiting a negative slope region. A hypothetical example of a family of 3-terminal negative-resistance device characteristics is shown in Fig. 2(b) for the voltage-controlled type, and in Fig. 2(c) for the current-controlled type.

Numerous 2-terminal negative resistance devices have been reported in the literature, the most well known being the tunnel diode, which is a type N device, and a glow tube, which is a type S device. An extensive catalog of such devices is listed in [1]. Indeed, with the systematic method for designing negative resistance devices using existing solid state devices developed in [1-2], there is now available virtually thousands of such 2-terminal negative resistance devices.

Examples of 3-terminal negative resistance devices are also frequently reported, specially in the recent literature. For example, a 2-μm gate length GaAs MESFET with $N_D = 6 \times 10^{16}$ cm$^{-3}$ has been observed to exhibit a voltage-controlled negative resistance characteristic [3]. An older example is the unijunction transistor which has a current-controlled negative resistance characteristic [4]. Indeed, with the recent advances in material technology on GaAs and other materials having a negative differential drift velocity versus electric field characteristic [4], many more 3-terminal negative resistance devices are emerging over the horizon. In addition, a systematic circuit approach for generating new 3-terminal negative resistance devices having a "tailored" characteristic has just been reported [5].

In spite of the existence of a wide variety of negative resistance devices, very few scope tracings of such characteristics have appeared in the literature.†

†This is because physical batteries have an internal resistance and are themselves eventually passive.
The reason is that the "negative resistance" often caused jump phenomenon, hysteresis, and oscillation in the tracing circuitry. Indeed, all commercially available curve tracers are based on the concept of applying a "sweeping" voltage source over the device's dynamic range and then monitoring the device current [6]. This technique will never work for current controlled devices because the load line representing the voltage source and its internal resistance will intersect their v-i characteristics (Figs. 1(c) and 2(c)) at several points during part of the tracing cycle, resulting at best in a jump phenomenon. This problem can be easily overcome by using a current source sweep instead.

A much more serious problem is the perennial oscillation and instability that occur in many negative resistance devices.

Our objective in this paper is to design a curve tracer which is capable of tracing the voltage-controlled or current-controlled characteristics of both 2- and 3-terminal negative resistance devices. In the case of a 3-terminal device, our design will allow the device to be traced in any one of the following six standard representations listed in Table 1.

### Table 1. Equations for the six representations of a 3-terminal or 2-port device

<table>
<thead>
<tr>
<th>Current-controlled representation</th>
<th>Voltage-controlled representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>( v_1 = \hat{v}_1(i_1,i_2) )</td>
<td>( i_1 = \hat{i}_1(v_1,v_2) )</td>
</tr>
<tr>
<td>( v_2 = \hat{v}_2(i_1,i_2) )</td>
<td>( i_2 = \hat{i}_2(v_1,v_2) )</td>
</tr>
<tr>
<td><strong>Hybrid-1 representation</strong></td>
<td><strong>Hybrid-2 representation</strong></td>
</tr>
<tr>
<td>( v_1 = \hat{v}_1(i_1,v_2) )</td>
<td>( i_1 = \hat{i}_1(v_1,i_2) )</td>
</tr>
<tr>
<td>( i_2 = \hat{i}_2(i_1,v_2) )</td>
<td>( v_2 = \hat{v}_2(v_1,i_2) )</td>
</tr>
<tr>
<td><strong>Transmission-1 representation</strong></td>
<td><strong>Transmission-2 representation</strong></td>
</tr>
<tr>
<td>( v_1 = \hat{v}_1(v_2,-i_2) )</td>
<td>( v_2 = \hat{v}_2(v_1,i_1) )</td>
</tr>
</tbody>
</table>
| \( i_1 = \hat{i}_1(v_2,-i_2) \) | \( -i_2 = \hat{i}_2(v_1,i_1) \) }
Whereas the methods for tracing the first 4 representations are a simple extension of the 2-terminal case, tracing the two transmission (chain) representations require some special techniques so that a voltage source and a current source can be simultaneously applied across the same pair of terminals! Indeed, to the best of our knowledge, no one has been able to trace the transmission characteristics of any 3-terminal or 2-port device before, let alone its negative resistance.

In order not to distract those readers interested only in using our tracer to trace negative resistance devices, the complete schematic diagram is first given in Section 2 along with numerous examples illustrating its use. The theory for quenching the oscillation and instability is developed in Section 3. This theory is crucial to the successful design of our tracer. The special technique developed for tracing the transmission representation is described in Section 4. Details on the design of the various components of the complete curve tracer circuit in Section 2 are described in Section 5 and in the Appendix.

2. THE CURVE TRACER: A USER'S GUIDE

A. External Description

In its simplest form, the circuit for tracing a 2-terminal negative resistor is shown in Fig. 3(a) for the voltage-controlled case, and in Fig. 3(b) for the current-controlled case. The series resistance $R$ in Fig. 3(a) can be interpreted as the internal resistance of the voltage source $v_\text{s}(t)$ and should ideally be kept as small as possible. The shunt conductance $G$ in Fig. 3(b) can be interpreted as the internal conductance of the current source $i_\text{s}(t)$ and should ideally be kept as small as possible.

The capacitance $C$ in Fig. 3(a) and the inductance $L$ in Fig. 3(b) are needed to quench any oscillation and other more complicated forms of instability. It will be shown in Section 3 that by choosing a large enough value of $C$ and $L$, no instability will occur provided the tracing signal frequency is sufficiently small: The larger the value of $C$ and $L$, the smaller the allowable frequency. Since too low a frequency would result in flicker in the oscilloscope tracing, a minimum frequency of 60 Hz is recommended. This implies that the value of $C$ and $L$ should be chosen as small as possible.

It will also be shown in Section 3 that there is a trade off between the values of $R$ and $C$, and between $G$ and $L$: increasing $R$ over a limited range allows
us to decrease C and increasing G over a limited range allows us to decrease L. Since the trade off depends on the device characteristic itself, it is essential to allow both R and C in Fig. 3(a), and G and L in Fig. 3(b) to be adjustable externally.

The same basic circuits in Fig. 3 can be used to trace the negative resistance characteristics of a 3-terminal device (for the first 4 representations in Table 1) by simply applying a staircase voltage or current waveform to the other terminal. The increment in each step in the staircase signal determines the "spacing" between the curves in the family of characteristics. Since this choice depends on the nature of the device, the incremental step must also be externally adjustable.

Finally, since different devices have different dynamic ranges, the amplitude of the tracing signal $v_s(t)$ and $i_s(t)$ should also be adjustable.

To summarize, any general purpose curve tracer must have external switches and knobs for adjusting, at the very least, the following parameters:

<table>
<thead>
<tr>
<th>Voltage-controlled device</th>
<th>Current-controlled device</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. R</td>
<td>1. G</td>
</tr>
<tr>
<td>2. C</td>
<td>2. L</td>
</tr>
<tr>
<td>3. incremental step $\Delta i$ or $\Delta v$</td>
<td>3. incremental step $\Delta v$ or $\Delta i$</td>
</tr>
<tr>
<td>4. amplitude of $v_s(t)$</td>
<td>4. amplitude of $i_s(t)$</td>
</tr>
</tbody>
</table>

In addition, the following external terminals are needed:

1. Device terminals: for connecting 2-terminal or 3-terminal device being traced.
2. Input signal terminals: to be connected to a periodic signal generator, usually a sinusoidal signal.
3. Output terminals: for connecting the device voltage signal to the horizontal plate and the device current signal to the vertical plate of the oscilloscope. A symbolic diagram illustrating how these terminals are connected in an actual measurement setup is shown in Fig. 4(a). A photograph of the curve tracer designed with the above features is shown in Fig. 4(b).
B. Complete Circuit Schematic Diagram

For users interested in building this curve tracer, a complete schematic diagram is shown in Figs. 5(a), (b), (c) and (d). For clarity purpose, this diagram is broken up into 3 parts and labelled as Figs. 5(b), (c) and (d), respectively. All components are clearly labelled for easy duplication. The complete list of components and their specifications are given in Appendix A.

The switches mounted on a common shaft are connected by dotted broken lines. For example, switch SW in Fig. 5(a) is a 2-pole 4-position switch mounted on a common shaft.

Fig. 5(a) is the block diagram of the curve tracer. It consists basically of three parts such as tracing signal generator, staircase signal generator and vertical and horizontal channel measurement circuit. There is a 2-pole 4-position switch SW which is used to switch the tracing signal and staircase signal to different terminals of the device being traced. Inductor \( L_s \) is used to adjust the inductance in series with current-controlled 2-terminal device. Potentiometer \( R_p \) is used to adjust the shunt resistance. Potentiometer \( R_s \) and capacitor \( C_p \) are used to adjust the resistance in series and capacitance in parallel with the voltage-controlled 2-terminal device being traced, respectively. The input signal for driving the tracer signal generator and the staircase signal generator are supplied by an external signal generator which is usually a sinusoidal signal generator. The output signals of the vertical and horizontal channel measurement circuit are applied to the vertical and horizontal terminals of the oscilloscope, respectively.

Figures 5(b), (c) and (d) form the complete circuitry of the curve tracer. Figure 5(b) shows the tracer signal generator circuit which transforms the input signal into a voltage source or current source having several optional waveforms (e.g., positive half sine wave, negative half sine wave, etc.) useful on various occasions.

Figure 5(c) shows the staircase signal generator circuit which is used to generate the voltage or current increment signals so that the family of characteristics describing a 3-terminal or 2-port device can be traced in a single measurement set up.

Figure 5(d) shows the vertical and horizontal channel measurement circuit which measures the current and the voltage associated with the device under test. Switch \( SW_2 \) switches the different tracer and staircase signals to the associated terminals of the 3-terminal device so that the families of
characteristics associated with any one of the 6 representations of the device may be traced in a single set up. Position 1 (present position of the arrow in Fig. 5(d)), 2, 3 or 4 corresponds to selecting the voltage-controlled, current-controlled, hybrid-2 or hybrid-1 (as shown in Table 1) representation of the device. Position 5 or 6 corresponds to selecting the transmission-1 or transmission-2 representation of the device.

When tracing a 2-terminal voltage-controlled (type N) device, SW₂ should be switched to position 1, and when tracing a 2-terminal current-controlled (type S) device, SW₂ should be switched to position 2.

The position of switch SW₁₁ and SW₁₂ depends on whether voltage or current is measured, respectively, i.e., to measure the voltage across the associated terminals of the device, we set SW₁₁ to position v, and to measure the current through the associated terminals of the device, we set SW₁₁ to position i.

The banks of capacitors and inductors in Fig. 5(d) correspond to C and L in Figs. 3(a) and (b), respectively. An extra position (ext.) in each switch allows the user to connect a capacitor or inductor (whose value is not available internally) across an external terminal pair.

C. Sample Tracings of 2-Terminal Negative Resistance Devices

Hundreds of negative resistance device characteristics have been successfully traced with our curve tracer. The following is a sample of some of these devices with interesting v-i characteristics. Most of these tracings require a "stabilizing" capacitance or inductance and could not have been traced by existing commercial curve tracers.

1. Voltage-controlled (type N) devices:

Figure 6(a) shows the scope tracing of a commercial 1N3717 tunnel diode (made by General Electric Co.) taken without the shunt capacitor in Fig. 3(a). Note that the negative resistance region looks like a mess although superficially its outline seems to suggest a smooth typical tunnel diode characteristic with a single peak and a single valley point [4]. Applying our theory from Section 3, we know the instability phenomenon in Fig. 6(a) can be quenched by connecting a sufficiently large capacitance C in parallel with the tunnel diode provided the frequency is low enough. The characteristic in Fig. 6(b) was successfully traced with a 40 Hz sinusoidal tracing signal and a 1 μF shunt capacitance. This v-i curve came as a big surprise as it differs drastically
from the expected conventional tunnel diode characteristic.

To ensure that this v-i curve is indeed the true device characteristic, we have made a point-by-point dc measurement and used multiple exposure to capture the points on film, as shown in Fig. 6(c). They coincide exactly with the "ac" tracing in Fig. 6(b). To ensure that the tracing circuit is not oscillating at a frequency beyond the bandwidth of our oscilloscope, we have checked the waveforms using a high frequency (200 MHz bandwidth) scope and found no discernible oscillation.

We have repeated our experiment with several other tunnel diodes (e.g., 1N3720) and found all of them to be characterized by a double-peak double-valley characteristic. We conclude therefore that at least for the batch of tunnel diodes we have traced, they are characterized by a v-i curve somewhat different from those published in textbooks. While this characteristic is more interesting and potentially more useful as a harmonic generator, any circuit design based on the conventional characteristic would clearly be in serious error!

Consider next the voltage-controlled negative resistance one-port shown in Fig. 7(a). The v-i curve in Fig. 7(b) is traced without a shunt capacitance. Note the instability near the negative resistance region. By adding a 0.1 μF shunt capacitance, we obtained the "clean" v-i curve in Fig. 7(c).

The preceding v-i characteristics lie in the first and third quadrants, as expected, since the devices are passive and unbiased.

Consider next the 2-transistor one-port shown in Fig. 8(a) which is biased by a 10 V battery. The v-i curve in Fig. 8(b) is again all messed up. The clean characteristic in Fig. 8(c) is traced with a 0.1 μF shunt capacitance. Note that unlike the previous characteristics, this device is not passive because there are points in the second and fourth quadrants. However, it is eventually passive, as expected.

To show that the parameters of some negative resistance devices, especially those made of op amps, are such that a stable v-i characteristic can be traced without the shunt capacitance, three different op amp one-ports are shown in Fig. 9, 10 and 11, along with their respective voltage-controlled negative resistance characteristics.

2. Current-controlled (type S) devices:

Consider the one-port shown in Fig. 12(a). Its v-i characteristic traced without a series inductance is shown in Fig. 12(b). Note the oscillation due to the tracing circuit wiped out the most interesting portion of the v-i
characteristic. The same one-port traced with a 2 mH series inductance and 
\( G = 8.8 \times 10^{-6} \) mho is shown in Fig. 12(c).

Consider next the two-transistor one-port shown in Fig. 13(a). Its \( v-i \) characteristic traced in Fig. 13(b) without a series inductance leads to oscillation within the negative resistance region. By connecting a 3 mH inductance in series, we obtain the sharp \( v-i \) characteristic in Fig. 13(c).

Figures 14 through 17 show 4 different current-controlled negative resistance one-ports which were successfully traced without a series inductance. Observe that none of the current-controlled characteristics in Figs. 12-17 could be obtained by commercial curve tracers based on a voltage sweep.

D. Sample Tracings of 3-Terminal or 2-Port Negative Resistance Devices.

Numerous 3-terminal and 2-port negative resistance devices have been successfully traced using our curve tracer. The following is a sample of some of these devices.

Consider the 2-port shown in Fig. 18(a). Tracing the \( v-i \) characteristics with \( i_2 \) as a parameter (see hybrid-1 representation from Table 1) without a shunt capacitance, we obtain the messy characteristics in Fig. 18(b). Since each \( v-i \) curve in Fig. 18(b) is voltage-controlled, we can quench the oscillation by adding a shunt capacitance across port 1. The resulting family of characteristics \( i_1 = \hat{i}_1(v_1,i_2) \) is shown in Fig. 18(c).

Consider next the 2-port shown in Fig. 19(a). Tracing the \( i_1-v_1 \) characteristic with \( i_2 \) as a parameter (see hybrid-1 representation from Table 1) without a series inductance, we obtained the messed up characteristics in Fig. 19(b). Since each \( v-i \) curve in Fig. 19(b) is current-controlled, we can quench the oscillation by adding an inductance in series with port 1. The resulting family of characteristics is shown in Fig. 19(c).

To demonstrate that our curve tracer can indeed trace the characteristics of a 3-terminal or 2-port device in any of the 6 representations, consider the two-transistor 2-port shown in Fig. 20(a). The 2 families of characteristics corresponding to each of the 6 distinct representations in Table 1 are shown in Figs. 20(b), (c), (d), (e), (f) and (g), respectively. These characteristics are all traced without any shunt capacitance or series inductance. The two transmission (chain) representations shown in Figs. 29(f) and (g) are as clear as the others, thereby demonstrating the possibility of tracing these two families of characteristics. To the best of our knowledge, this measurement had never been made before.
Just as the chain matrix is extremely useful in analyzing and designing two or more linear 2-ports connected in cascades, the possibility of measuring the nonlinear transmission characteristics could be equally useful in analyzing and designing nonlinear 2-ports connected in cascades. The resulting transmission characteristics in this case will be just the composition of the respective transmission characteristics.

3. **QUENCHING THE OSCILLATION**

No physical device is purely resistive. The oscillation or other unstable behavior that often plagued the tracing circuitry is strictly a dynamic phenomenon and can only be quenched by carrying out a detailed analysis using a realistic dynamic circuit model for the device. Using a device physics approach [4] or a circuit-theoretic approach [7], we can derive the following basic result:

**Positive Resistance Device Modeling Principle**

1. Every voltage-controlled (type N) negative resistance device must be modeled with a capacitor in parallel with a type N negative resistor, as shown in Fig. 21(a), and possibly additional dynamic elements at higher frequencies.

2. Every current-controlled (type S) negative resistance device must modeled with an inductor in series with a type S negative resistor Fig. 21(b), and possibly additional dynamic elements at higher frequencies.

We have found the models given in Fig. 21 are adequate for our purpose in this paper.

In order to analyze and develop a method to quench oscillations and other instability phenomena frequently encountered in conventional curve tracers, we have found that it is necessary to include at least a series parasitic inductance $L_p$ to the type N device model in Fig. 21(a), and a shunt parasitic capacitance $C_p$ to the type S device model in Fig. 21(b), in order to account for the small but non-zero line inductance and stray capacitance of the connecting wires. Hence, the simplest realistic circuit model of our negative-resistance curve tracer is as shown in Fig. 22(a) for a type N curve tracer, and Fig. 22(b) for a type S curve tracer. Since these 2 circuits are dual of each other [8], we will analyze only the type N circuit.

The state equation for the type N curve tracer circuit model in Fig. 22(a) is given by
In order to uncover the source of the oscillation, it suffices to replace the voltage source \( v_s(t) \) by a battery \( E \) so that we can analyze the stability of each equilibrium point. For the circuit in Fig. 22(a), the equilibrium points are identical to the dc operating points obtained by the load line method, as illustrated in Fig. 23 using a typical tunnel diode \( v-i \) characteristic. Observe that there are 3 equilibrium points in Fig. 23(a) but only one in Fig. 23(b). The bifurcation parameter is given by

\[
R = \frac{1}{G_{\text{max}}} \tag{2}
\]

where

\[
G_{\text{max}} \triangleq \text{magnitude of maximum negative slope of the } v_R-i_R \text{ characteristic} \tag{3}
\]

In order for the curve tracer to work properly, it is necessary that each equilibrium point be locally asymptotically stable [8-9] for all values of \( E \) within the dynamic range of interest. To derive the conditions for satisfying this requirement, consider the Jacobian matrix associated with (1) about an equilibrium point \( Q \):

\[
J_Q = \begin{bmatrix}
-\frac{1}{C} \hat{i}_R'(V_Q) & \frac{1}{C} \\
-\frac{1}{L} & -\frac{R}{C}
\end{bmatrix} \tag{4}
\]

where \( \hat{i}_R'(V_Q) \) denotes the slope at \( v_R = V_Q \). The necessary and sufficient conditions for the equilibrium point \( Q \) to be locally asymptotically stable are given by [8-9]:

\[
T_Q \triangleq -\frac{R}{L} - \frac{1}{C} \hat{i}_R'(V_Q) < 0 \tag{5}
\]

\[
\Delta_Q \triangleq \frac{R}{LC} \hat{i}_R'(V_Q) + \frac{1}{LC} > 0 \tag{6}
\]

Since \( R > 0 \), \( L > 0 \), and \( C > 0 \), conditions (5) and (6) are always satisfied if \( \hat{i}_R'(V_Q) \geq 0 \). Hence all equilibrium points falling on the non-negative
slope region of the \( v_R - i_R \) characteristic are always locally asymptotically stable. This explains why it is easy to trace monotone-increasing \( v-i \) characteristics.

However, both (5), and (6) are easily violated in negative resistance characteristics especially when the negative slope is steep, i.e., when \( i_R'(V_Q) \ll 0 \). Since (5) and (6) must be satisfied at all operating points in the negative resistance region, the most critical situation occurs at the "steepest" point where the slope

\[
i_R'(V_Q) = -G_{\text{max}}
\]

is most negative, where \( G_{\text{max}} \) as defined in (3) is a positive number. Using this notation, conditions (6) and (5) can be recast into (8) and (9), respectively, and restated in words as follows:

**Stability Theorem**

The necessary and sufficient conditions for all operating points of the type N curve tracer model in Fig. 22(a) to be locally asymptotically stable are:

\[
R < \frac{1}{G_{\text{max}}}
\]

(8)

\[
R > (LG_{\text{max}})^{-\frac{1}{C}}
\]

(9)

Since \( G_{\text{max}} \) is fixed for a given device and \( L \), being the parasitic inductance, can not be reduced below some minimum value, the conflicting demands of (8) and (9) often can not be satisfied by adjusting only the parameter \( R \) alone, especially when the negative slope is steep, as in the examples in Figs. 6-8. Observe, however, that so long as \( G_{\text{max}} < \infty \), conditions (8) and (9) can always be satisfied by choosing a sufficiently large value for \( C \). This is easily met by connecting an adjustable capacitance \( C_1 \) in parallel with the device so that \( C = C_0 + C_1 \), as shown in Fig. 3(a).†

In the R-C parameter plane, conditions (8) and (9) define the stable region shown in Fig. 24(a) for a typical value of \( L \). The minimum capacitance \( C_{\text{min}} \) needed to quench the oscillation occurs at the intersection between the

†Since \( C_0 \) is very small in a typical device, \( C = C_0 + C_1 \approx C_1 \). Hence we will neglect \( C_0 \) from our subsequent discussion for simplicity.
two bifurcation curves \( \Delta = 0 \) and \( T = 0 \). Note that the shaded region shifts to the right as \( L \) increases, as shown in Fig. 24(b) for a somewhat larger value of \( L \). Hence \( C_{\text{min}} \) increases with \( L \).

To minimize \( C_{\text{min}} \), therefore, we must keep the connecting wires as short as possible.

Choosing the parameters \( R \) and \( C \) within the shaded region in Fig. 24 guarantees that the equilibrium point will be either a stable node or a stable focus [8] for each dc input voltage \( E \).

For each equilibrium point \( V_C = V_Q \) and each initial condition \( V_C(0) \), the transient decay rate is determined by the real part \( \sigma \) of the eigenvalues

\[
s_{1,2} = -\frac{1}{2} \left( \frac{R}{L} + \frac{\hat{i}_R(V_Q)}{C} \right) \pm \frac{1}{2} \sqrt{\left( \frac{R}{L} + \frac{\hat{i}_R(V_Q)}{C} \right)^2 - 4 \frac{R}{L C} \left( R \hat{i}_R(V_Q) + 1 \right)}
\]

(10)

if \( V_C = V_Q \) is a focus, or by the smaller real natural frequency \( \sigma \) (corresponding to choosing the negative sign in (10)) if \( V_C = V_Q \) is a node. A typical relationship between \( \sigma \) and \( C \) as calculated from (10) using a fixed value for \( R \), \( L \), and \( \hat{i}_R(V_Q) \) is shown in Fig. 25. Note that \( |\sigma| \) is largest at \( C = C_{\text{opt}} \).

Now the transient will for all practical purposes be negligible after 5 time constants \( \tau \), where \( \tau = \frac{1}{|\sigma|} \). Hence, it is possible to trace the \( v-i \) characteristic using a periodic ac voltage source \( v_s(t) \) provided its frequency \( \omega \) is chosen so that

\[
\omega < \frac{1}{5} |\sigma| \quad (11)
\]

Since \( \sigma = 0 \) when \( C = C_{\text{min}} \) in Fig. 25, where \( C_{\text{min}} \) corresponds to the intersection between the two bifurcation curves \( T = 0 \) and \( \Delta = 0 \) in Fig. 24(a), it follows from (11) that we must choose \( C \) greater than \( C_{\text{min}} \). The maximum allowable frequency occurs when we choose \( C = C_{\text{opt}} \). Any larger value of \( C \) must be accompanied by a decrease in \( \omega \). We can now summarize our preceding analysis as follows:

**Oscillation Quenching Guidelines for Type N Device (Fig. 3(a))**

1. Choose \( R < \frac{1}{G_{\text{max}}} \).
2. Choose \( C > C_{\text{min}} \).
3. Decreasing $R$ must be accompanied by an increase in $C$.
4. Increasing $C$ beyond $C_{\text{opt}}$ must be accompanied by a decrease in the tracing frequency $\omega$.

By duality, we can state:

<table>
<thead>
<tr>
<th>Oscillation Quenching Guidelines for Type S Device (Fig. 3(b))</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Choose $G &lt; \frac{1}{R_{\text{max}}}$, where $R_{\text{max}}$ is the magnitude of the slope of $v_R(i_R)$ at its steepest point.</td>
</tr>
<tr>
<td>2. Choose $L &gt; L_{\text{min}}$, where $L_{\text{min}}$ corresponds to $C_{\text{min}}$ in Fig. 24(a).</td>
</tr>
<tr>
<td>3. Decreasing $G$ must be accompanied by an increase in $L$.</td>
</tr>
<tr>
<td>4. Increasing $L$ beyond $L_{\text{opt}}$ must be accompanied by a decrease in the tracing frequency $\omega$, where $L_{\text{opt}}$ corresponds to $C_{\text{opt}}$ defined above.</td>
</tr>
</tbody>
</table>

4. TRACING THE TRANSMISSION REPRESENTATION

The two transmission representations listed in Table 1 are the nonlinear generalization of the well-known chain matrix representations for linear time-invariant 2-ports, namely,

<table>
<thead>
<tr>
<th>linear 2-port</th>
<th>transmission-1</th>
<th>transmission-2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$v_1$</td>
<td>$v_2$</td>
</tr>
<tr>
<td></td>
<td>$i_1$</td>
<td>$-i_2$</td>
</tr>
<tr>
<td>transistor</td>
<td>$t_{11}t_{21}$</td>
<td>$t_{12}t_{22}$</td>
</tr>
</tbody>
</table>

| nonlinear 2-port | $v_1 = \hat{v}_1(v_2,-i_2)$ | $v_2 = \hat{v}_2(v_1,i_1)$ |
|                 | $i_1 = \hat{i}_1(v_2,-i_2)$ | $-i_2 = \hat{i}_2(v_1,i_1)$ |

The two matrices in Eqs. (12a) and (12b) are called chain matrices. The transmission representation is most conveniently used when two or more linear 2-ports are connected in cascade. In this case the transmission matrix of the composite 2-port is just the product of the respective chain matrices. Likewise, when two or more resistive 2-ports are connected in cascade, the transmission representation of the composite 2-port is just the composition of the respective transmission functions. This remarkable property is of immense help in both

The chain matrix in Eq. (12a) is usually denoted by $\begin{bmatrix} A & B \\ C & D \end{bmatrix}$ in the literature.
Unfortunately, manufacturers never specify a nonlinear 3-terminal device by its transmission representation. The reason is simple: no measurement technique, let alone a dedicated instrument, is available.

One obstacle here is due to the fact that both independent variables ($v_2$ and $-i_2$ in the transmission 1 representation; $v_1$ and $i_1$ in the transmission 2 representation) in Eqs. (13a) and (13b) pertain to the same port.

For example, to measure the transmission 2 representation, it is necessary to apply an independent voltage source $v_s(t)$ and an independent current source $i_s(t)$ to port 1 of the 3-terminal device so that $v_1 = v_s(t)$ and $i_1 = i_s(t)$. The only two ways for connecting these two sources directly, as shown in Fig. 26, are not feasible because whereas $v_1 = v_s(t)$ in Fig. 26(a), $i_1 \neq i_s(t)$ unless $i_{in} = 0$; and whereas $i_1 = i_s(t)$ in Fig. 26(b), $v_1 \neq v_s(t)$ unless $v_{in} = 0$.

Another serious obstacle is encountered at port 2; namely, the load $N$ in Fig. 26 must not present any constraint between the two dependent port variables $v_2$ and $i_2$ because both $v_2$ and $i_2$ are defined uniquely by the transmission functions via Eq. (13b). Note that open circuiting port 2 is not allowed because $i_2$ would then be constrained to zero. Likewise, short circuiting port 2 is not allowed because $v_2$ would then be constrained to zero. In fact, $N$ can not be any ordinary one-port because such a one-port would be described by a relationship between $v_2$ and $i_2$, thereby creating an implicit constraint between these two dependent variables.

The first obstacle can be overcome by inserting a nullator in series with the voltage source $v_s(t)$ as shown in Fig. 27(a), thereby clamping $i_{in} = 0$. Moreover, since the voltage across the nullator is zero, we still have $v_1 = v_s(t)$.

The second obstacle can be overcome by choosing the load $N$ to be a norator, as shown in Fig. 27(b). Since this element imposes no constraint in either $v_2$ or $i_2$, the port current $i_2$ and port voltage $v_2$ depend only on $v_1$ and $i_1$. Hence, the norator is functioning like a "slack" variable in linear programming.

Although individually, nullators and norators can not be realized by any physical circuit, together they can be simulated by an op amp operating in its linear region, as shown by the ideal op amp model in Fig. 27(b). Hence,

---

$^\dagger$The nullator is a singular circuit element defined by a single point at the origin, namely, $v = 0$, $i = 0$ [10-11].

$^{++}$A norator is a singular circuit element defined by all points in the $v$-$i$ plane [10-11].
replacing the nullator and norator in Fig. 27(b) by an op amp, we obtain the practical circuit in Fig. 27(c) for tracing the transmission 2 characteristics of a 3-terminal device $D$.

To trace the transmission 2 characteristics of a 3-terminal device $D$ using the circuit in Fig. 27(c), we first apply the signal $v_s(t)$ to the horizontal channel and the signal $v_2$ to the vertical channel of the oscilloscope. A staircase signal $i_s(t)$ is then applied to obtain the first family of characteristics; namely, $v_2 = v_2(v_1, i_1)$. To obtain the second family of transmission characteristics, we repeat the above measurement but with $i_2(t)$ applied to the vertical channel through a small current sensing resistor.

To obtain the transmission 1 characteristics, we simply use the same circuit in Fig. 27(c) but with terminal 1 and 2 of the 3-terminal device $D$ interchanged. The transmission characteristics shown in Figs. 19 and 20 are all measured using this simple tracing circuit. Our experience has shown that this circuit is rather robust and stable, in spite of the fact that the nullator and norator are highly pathological. This circuit is also interesting because it illustrates how a purely abstract concept can become indispensable in the design of a practical circuit. Indeed, we do not know of any other way for measuring the transmission characteristics.

5. DESIGN DETAILS

As mentioned above in Section 2, the complete circuit of the curve tracer consists basically of three parts: the tracer signal generator, the staircase signal generator and the vertical and horizontal channel measurement circuit. The tracer signal generator shown in Fig. 5(b) includes a full-wave rectifier, an amplifier, a voltage source, and a current source. Push-pull transformer $T_1$ is used to apply the signal from the external signal generator to the full-wave rectifier consisting of four diodes $D_1, D_2, D_3$ and $D_4$. Capacitors $C_1$ and $C_2$ are used to avoid potential parasitic oscillations. The load of the full-wave rectifier is a voltage amplifier $IC_1$ which has different gain for different waveforms so that the amplitudes of its output voltages will be basically the same when the input voltage of the push-pull transformer $T_1$ is constant. The output stage $IC_2$ is a buffer.

The operational amplifier $IC_3$ amplifies the input signal from switch $SW_2$. The output voltage of $IC_3$ is applied to transistors $Q_1$ and $Q_2$. Transistor $Q_1$ will conduct when the input voltage of $IC_3$ is negative, and $Q_2$ will conduct...
when the input voltage of IC$_3$ is positive, respectively. The feedback of IC$_3$

The high-voltage op amp IC$_4$ amplifies the input signal from potentiometer
R$_6$. Meanwhile, SW$_2$ will ground the input terminal of IC$_3$ so that the current
source will not interfere with other circuits. Transistors Q$_3$ and Q$_5$ are the
driver stages of the tracer voltage source, and transistors Q$_4$ and Q$_6$ are the
power output stages of the tracer voltage source. Transistors Q$_3$ and Q$_4$ will
conduct when the input signal of IC$_4$ is negative, and Q$_5$ and Q$_6$ will conduct
when the input signal of IC$_4$ is positive, respectively. Diodes D$_{3g}$, D$_{6g}$, D$_{9g}$ and
D$_{10g}$ provide biasing for the output stages, and D$_7$, D$_8$, D$_{11g}$ and D$_{12g}$ are used for
overload protection. Resistors R$_{24}$ and R$_{25}$ connected to the emitters of Q$_4$ and
Q$_6$, respectively, are current-limiting resistors.

Figure 5(c) shows the circuit diagram of the staircase signal generator
which consists of three parts: the staircase voltage generator, the staircase
voltage source, and the staircase current source. IC$_6$, IC$_7$, IC$_8$, and IC$_9$ form
the staircase voltage generator. The op amp IC$_6$ is used as a zero-crossing
detector. The input signal of IC$_6$ is the same as that of transformer T$_1$ in the
tracer signal generator so that the staircase signal is synchronized to the
tracing signal.

The output pulses of the zero-crossing detector are used as triggers for
the monostable multivibrators IC$_7$ and IC$_8$. The negative output pulses of IC$_6$
will be clipped by diode D$_{13}$. IC$_5$ is a +5 volt regulator that is used as a DC
power supply for the monostable multivibrators IC$_7$ and IC$_8$. The output (posi-
tive) pulses of IC$_7$ charge capacitor C$_{10}$ of the integrator (formed by IC$_9$, 
resistor R$_{34}$ and capacitor C$_{10}$) to generate a staircase voltage between the
output terminals of IC$_9$. The output (positive) pulses of IC$_8$ will discharge
the integrator so that a periodic staircase voltage will be obtained. By
adjusting the width of output pulses of IC$_7$ (by adjusting potentiometer R$_{27}$),
we can change the "increment" in the steps. The "number" of steps can be
changed by adjusting the width of the output pulses of IC$_8$ (by adjusting
potentiometer R$_{29}$).

Diode D$_{14}$ is used to avoid a premature discharge of the capacitor C$_{10}$
while generating the step voltages. The network formed by resistor R$_{35}$ and
potentiometer R$_{36}$ is used to adjust the zero step of the output staircase
voltage of the integrator. Op amp IC$_{10}$ and IC$_{11}$ form a voltage source with
positive and negative voltage output. In fact, IC$_{10}$ is used as a phase
inverter and IC₁₁ is a voltage follower. There is a voltage divider between IC₁₀ and IC₁₁ to change the step increment. The positive step voltage from the integrator is fed to the inverting input or non-inverting input of IC₁₀ by switch SW₁ so that positive and negative step voltages can be obtained. Op amp IC₁₂ and transistor Q₇ with the associated resistors form a positive staircase current source to which the positive staircase voltage from IC₁₁ is applied through SW₁. Potentiometer R₅₆ is used to adjust the zero step of the positive staircase current signal. Op amp IC₁₃ and transistor Q₈ with the associated resistors form a negative staircase current source to which the negative staircase voltage from IC₁₁ is applied through SW₁. Diode D₁₅ and potentiometer R₆₆ are used to adjust the zero step of the negative staircase current signal.

Figure 15(d) is the circuit diagram of the vertical and horizontal channel measurement circuit. In fact, the vertical and horizontal channels are basically the same. To improve the precision of the measurement circuit, we use JFET input quad op amp followers IC₁₄, IC₁₅, IC₁₉ and IC₂₀ as the input stages of these two channels so that the current through the device being traced will be almost equal to that through the current sensing resistor. There are four voltage dividers formed by resistors R₇₅-R₇₈, R₇₉-R₈₂, R₉₆-R₉₉ and R₁₀₀-R₁₀₃, respectively, so that the op amp followers IC₁₄, IC₁₅, IC₁₉ and IC₂₀ would not saturate within the dynamic range of the device being traced. The division factors are 1, 2, 5 and 10, respectively. Hence, the input voltages of these followers will be reduced by 1, 2, 5 or 10 times so that the voltage amplitude displayed on the scope is equal to 1, 2, 5, or 10 of the actual amplitude of the output voltage, depending on the positions of the switches SW₉ and SW₁₀. When measuring current through the device being traced, the voltage across the current sensing resistor R₉₂-R₉₅ (or R₇₁-R₇₄) is applied to the differential amplifier IC₂₁ (or IC₁₆ for the horizontal channel). Current sensing resistors R₇₁-R₇₄ and R₉₂-R₉₅ are both chosen equal to 1 k, 500, 100 and 10 ohm, respectively. Hence, there is 1, 2, 10 and 100 mA of current through the device being traced for a 1 volt voltage across the resistors, respectively, depending on the positions of the switches SW₇ and SW₈. Op amp IC₂₂ (or IC₁₇, for the horizontal channel), is a phase inverter. Op amp IC₂₃ (or IC₁₈ for the horizontal channel) is a voltage follower serving as the output stage of the curve tracer. The polarities of the output signals of the vertical and horizontal channel can be changed by switches SW₁₄ and SW₁₃, respectively. While measuring voltage, switch SW₁₂ (or SW₁₁ for the horizontal
channel) will ground the inverting input of the differential amplifier IC_{21} (or IC_{16}, in horizontal channel).

Op amp IC_{24} is playing the role of both nullator and norator when tracing the transmission characteristics of a 3-terminal device.

Potentiometer R_{68} is used as the shunt resistance in the tracing current source, and inductors L_{1} through L_{6} are connected in series with the device being traced, respectively. Both the shunt resistance and inductance are used to quench the oscillation when tracing a current-controlled 2-terminal device. Similarly, the potentiometer R_{112} connected in series and capacitors C_{11} through C_{16} connected in parallel with the device, respectively, are used to quench the oscillation when tracing a voltage-controlled 2-terminal device, as already described in Section 3.
REFERENCES


### APPENDIX A: THE CATALOG OF COMPONENTS

<table>
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<td>1/4 LM2900n quad amp</td>
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FIGURE CAPTIONS

Fig. 1. (a) A 2-terminal device with associated reference directions for $v$ and $i$.
    (b) A hypothetical voltage-controlled negative resistance device.
    (c) A hypothetical current-controlled negative resistance device.

Fig. 2. (a) A 3-terminal device with associated reference directions for $v_1$, $v_2$, $i_1$ and $i_2$.
    (b) A hypothetical family of voltage-controlled negative resistance characteristics.
    (c) A hypothetical family of current-controlled negative resistance characteristics.

Fig. 3. (a) Basic circuit for tracing a voltage-controlled negative resistance device.
    (b) Basic circuit for tracing a current-controlled negative resistance device.

Fig. 4. (a) Set up for actual measurement.
    (b) Photograph of curve tracer.

Fig. 5. (a) Block diagram of curve tracer.
    (b) Tracer signal generator circuit.
    (c) Staircase signal generator circuit.
    (d) Vertical and horizontal measurement circuit.

Fig. 6. (a) Unstable tracing of a 1N3717 tunnel diode without shunt capacitor.
    (b) $v$-$i$ characteristic traced by a 40 Hz sinusoidal signal with a 1 $\mu$F shunt capacitance.
    (c) $v$-$i$ characteristic traced by a point-by-point dc measurement with a 1 $\mu$F shunt capacitance. All curves are traced with the same series resistance $R = 6 \Omega$.
    Horizontal scale: 0.2 volts per division,
    Vertical scale: 3.3 mA per division.

Fig. 7. (a) One-port made of a pnp transistor and an n-channel JFET.
    (b) Unstable tracing without shunt capacitor.
    (c) Stable tracing with 0.1 $\mu$F shunt capacitance. All curves are traced with the same series resistance $R = 5 \Omega$.
    Horizontal scale: 2 volts per division,
    Vertical scale: 20 mA per division.

Fig. 8. (a) One-port made of 2 npn transistors and a battery.
    (b) Unstable tracing without shunt capacitor.
    (c) Stable tracing with 0.1 $\mu$F shunt capacitance. All curves are traced with the same series resistance $R = 5 \Omega$.
    Horizontal scale: 0.4 volts per division,
    Vertical scale: 4 mA per division.

Fig. 9. (a) One-op-amp negative-resistance one-port.
    (b) $v$-$i$ characteristic traced without shunt capacitance; $R = 100 \Omega$.
    Horizontal scale: 4 volts per division,
    Vertical scale: 0.5 mA per division.

Fig. 10. (a) Two-op-amp negative resistance one-port.
    (b) $v$-$i$ characteristic traced without shunt capacitor; $R = 100 \Omega$.
    Horizontal scale: 4 volts per division.
    Vertical Scale: 2.5 mA per division.

Fig. 11. (a) Three-op-amp negative resistance one-port.
    (b) $v$-$i$ characteristic traced without shunt capacitor; $R = 100 \Omega$. 
Horizontal scale: 4 volts per division.
Vertical scale: 0.5 mA per division.

Fig. 12. (a) A current-controlled negative resistance one-port made of an npn transistor and an n-channel JFET.
(b) v-i characteristic traced without series inductance.
(c) v-i characteristic traced with 2 mH series inductance.
All curves are traced with $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 2 volts per division.
Vertical scale: 10 mA per division.

Fig. 13. (a) A current-controlled negative resistance one-port made of 2 npn transistors.
(b) v-i characteristic traced without series inductor.
(c) v-i characteristic traced with 3 mH series inductance.
All curves are traced with $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 1 volt per division.
Vertical scale: 0.5 mA per division.

Fig. 14. (a) A current-controlled negative resistance one-port made of 2 pnp transistors.
(b) v-i characteristic traced without series inductance; $G = 8.8 \times 10^{-7}$ mho.
Horizontal scale: 0.4 volt per division.
Vertical scale: 2 mA per division.

Fig. 15. (a) A current-controlled negative resistance one-port made of an npn transistor and a pnp transistor.
(b) v-i characteristic traced without series inductor; $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 2 volts per division.
Vertical scale: 0.5 mA per division.

Fig. 16. (a) A current-controlled negative resistance one-port made of an npn and a pnp transistor.
(b) v-i characteristic traced without series inductor; $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 0.4 volts per division.
Vertical scale: 2 mA per division.

Fig. 17. (a) A current-controlled negative resistance one-port made of five op-amps.
(b) v-i characteristic traced without series inductor; $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 1 volt per division.
Vertical scale: 5 mA per division.

Fig. 18. (a) A voltage-controlled negative resistance 2-port.
(b) $v_i$-i$_i$ characteristics (with i$_2$ as parameter) traced without shunt capacitor.
(c) $v_i$-i$_i$ characteristics (with i$_2$ as parameter) traced with 0.1 $\mu$F capacitor; $R = 10 \Omega$.
Horizontal scale: 2 volts per division.
Vertical scale: 20 mA per division.
Current step: -0.2 mA per step.

Fig. 19. (a) A current-controlled negative resistance 2-port.
(b) $v_i$-i$_i$ characteristics (with i$_2$ as parameter) traced without series inductance.
(c) $v_i$-i$_i$ characteristics (with i$_2$ as parameter) traced with 6.7 mH series inductance; $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 1 volt per division.
Vertical scale: 2 mA per division.
Fig. 20. (a) A 2-port made of a pnp transistor and an npn transistor.  
(b) Current-controlled representation.  
   Horizontal scale: 1 mA per division.  
   Vertical scale: 5 volts per division.  
(c) Voltage-controlled representation.  
   Horizontal scale: 1 volt per division.  
   Vertical scale: $i_1$: 2 mA per division, $i_2$: 5 mA per division.  
(d) Hybrid-1 representation.  
   Horizontal scale: $v_1$: 5 volts per division, $i_2$: 4 mA per division.  
   Vertical scale: $i_1$: 2 mA per division, $v_2$: 2.5 volts per division.  
(e) Hybrid-2 representation.  
   Horizontal scale: $i_1$: 4 mA per division, $v_2$: 2 volts per division.  
   Vertical scale: $v_1$: 2.5 volts per division, $i_2$: 1 mA per division.  
(f) Transmission-1 representation.  
   Horizontal scale: $v_2$: 0.5 volt per division, $i_2$: 1 mA per division.  
   Vertical scale: $v_1$: 1 volt per division, $i_1$: 1 mA per division.  
(g) Transmission-2 representation.  
   Horizontal scale: $v_1$: 0.5 volt per division, $i_1$: 1 mA per division.  
   Vertical scale: $v_2$: 1 volt per division, $i_2$: 1 mA per division.  
Fig. 21. (a) Circuit model for a type N device.  
(b) Circuit model for a type S device.  
Fig. 22. (a) Curve tracer circuit model for type N device.  
(b) Curve tracer circuit model for type S device.  
Fig. 23. (a) When $R > \frac{1}{G_{\text{max}}}$, load line intersects the $v_R$-$i_R$ characteristic at 3 points.  
   (b) When $R < \frac{1}{G_{\text{max}}}$, load line intersects the $v_R$-$i_R$ characteristic at only one point.  
Fig. 24. (a) Shaded region shows allowed parameter range for $R$ and $C$ for small $L$.  
   (b) Shaded region shows allowed parameter range for $R$ and $C$ for large $L$.  
Fig. 25. Real part of $s$ plotted as a function of $C$ with all other parameters held constant.  
Fig. 26. (a) Connecting a voltage source $v_S(t)$ and a current source $i_S(t)$ in parallel with port 1 is equivalent to just connecting the voltage source $v_S(t)$ alone.  
   (b) Connecting a current source $i_S(t)$ and a voltage source $v_S(t)$ in series with port 1 is equivalent to just connecting the current source $i_S(t)$ alone.  
Fig. 27. (a) Connecting a nullator in series with the voltage source and a norator across port 2.  
   (b) Ideal op amp model in the linear region with infinite gain.  
   (c) Practical op amp circuit for tracing the transmission representation 2.
Fig. 4
Fig. 5(a)
From FB in Fig 5(d) to $i_s(t)$ in Fig. 5(d) to $v_s(t)$ in Fig. 5(d)
Fig. 5(c)
Fig. 5(d)
Fig. 9

(a) Circuit diagram: 100 KΩ, 9.7 KΩ, LM741C, 100 KΩ

(b) Graph: i, mA v, volt

Fig. 10

(a) Circuit diagram: 3.37 KΩ, 3.16 KΩ, 235 Ω, 6.23 KΩ, 391 Ω, 11.23 KΩ

(b) Graph: i, mA v, volt

Fig. 11

(a) Circuit diagram: 340 Ω, 26.8 KΩ, 41.3 KΩ, 3.98 KΩ, 5.1 KΩ, 4.7 KΩ

(b) Graph: i, mA v, volt
Fig. 20

(a)

(b)

(c)
Fig. 20
Fig. 23

slope = $-G_{\text{max}}$

slope = $\frac{1}{R}$
$V_s(t) \uparrow i_s(t) \downarrow V_1 \downarrow V_2$  

(a)  

Fig. 26  

$V_s(t) \uparrow i_s(t) \downarrow V_1 \downarrow V_2$  

(b)  

Nullator $i_{in}$  

(i)  

Norator  

(b)  

$V_s(t) \uparrow i_s(t) \downarrow V_1 \downarrow V_2$  

(c)  

Fig. 27