THE SIMULATION OF MOS INTEGRATED CIRCUITS

USING SPICE2

by

Andrei Vladimirescu and Sally Liu

Memorandum No. UCB/ERL M80/7

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ELECTRONICS RESEARCH LABORATORY

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Many people contributed to develop the new input and model equations for MOSFET's. The continuing encouragement and support of our research advisor, Professor D. O. Pederson, is greatly appreciated. Steady discussions with E. Cohen and other members of the UC Berkeley Integrated Circuits Computer-Aided Design Group are acknowledged. Discussions with Professors W. G. Oldham, P. R. Gray, D. A. Hodges, and R. A. Newton helped in many decisions that had to be taken.

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1. INTRODUCTION

This report is addressed to all SPICE2 users involved in the design of MOS (Metal Oxide Semiconductor) IC's (Integrated circuits). The material contained herein serves as an addition to the SPICE2.G User's Guide [1].

The device and model parameters documented refer to the SPICE2.G release versions from the University of California, Berkeley and obsolete the information contained in the "SPICE2 MOS Modeling Handbook" [2] which is valid for the SPICE2.D release versions.

The impact of MOS IC's in both analog and digital applications as well as the decreasing dimensions of the single transistors enabled by advances in processing have made it necessary to refine the models and to provide more information about each device as it appears on the circuit layout. Associated with each MOSFET is a drain and source-junction sidewall capacitance (which has a different voltage dependence than the bottom of the diffusion) and a parasitic series resistance. These are unique to a certain geometry. At the model level there are effects which become important as the channel length and width go below 10μm. A thorough description of all parameters appearing on the element (device) card and model card is contained in Sec. 2.

In SPICE2.G there are three different MOS models available to the user. The Level 1 model is the simple Shichman-Hodges model implemented according to [3]. This first order model has been found necessary for checking out the correctness of hand calculations when understanding or developing new circuits. The Level 2 model is an analytical one-dimensional model which incorporates most of the second-order effects of small-size devices. The Level 3 model is a semi-empirical model described by a set of parameters which are defined by curve-fitting rather than physical background. It is necessary for the circuit designer to know what are the equations governing the behaviour of the MOSFET's and what is the influence of the various model parameters even if hand calculations are almost impossible at this complexity. This insight of the MOS2 and MOS3 model equations is found in Sec. 3 and 4.

The accuracy of the model depends heavily on the values of the input parameters. These input parameters should be related to the particular process used at each manufacturing site. The large number of parameters which describe the model require the existence of a parameter extraction system. Sec. 5 provides some detail on how to use some simple preprocessor programs for the evaluation of the SPICE2 input parameters from the measurements taken on test devices.

Sec. 6 gives an example of a sample SPICE2 MOS IC input deck stressing the correlation among different model parameters and the importance of modelling various second-order effects for a good agreement with measured performance.
2. DESCRIPTION OF MOSFET PARAMETERS

2.1. Device Parameters

According to the new format of the MOSFET device line [1] there are up to 8 parameters describing each geometry. With the exception of \( W \) and \( L \) (which are defaulted to \( 1 \) m), all other parameters default to zero if not specified.

\( W \) and \( L \) are the channel width and length in meters as measured on the layout;

\( AD \) and \( AS \) are the drain and source area, respectively; they scale the parameters \( JS \) and \( CJ \) of the model line. If not specified they are assumed zero. When absolute values for the junction reverse current \( (IS) \) or the junction capacitances \( (CBD, CBS) \) are input on the model line the areas can be omitted. \( AD \) and \( AS \) are measured as if on a layout and thus model the bottom of the junction.

\( PD \) and \( PS \) are the perimeters of the drain and source respectively; they multiply the junction sidewall capacitance \( CJSW \) specified in \( \text{F/m} \) on the model line.

\( NRD \) and \( NRS \) are the number of squares of the parasitic series resistance of the drain and source diffusions as estimated from the layout. \( NRD \) and \( NRS \) multiply the sheet resistance \( RSH \) given on the model card. An alternate way to specify series resistances for the drain and source is to enter the total values \( RD \) and \( RS \) on the model card; these values will then be added to all devices which invoke that particular model. When \( RD \) and \( RS \) appear in the definition of a model then those devices referencing this model need no \( NRD \) or \( NRS \).

As is seen from the above there is a close correlation between the parameters which appear on the device card and the parameters input on the model card. Since a hierarchical order of the model parameters is given in the following paragraph, only a single example is mentioned. The presence of \( NSUB \) on the model line automatically calls for the calculation of \( CJ \). A way to strip the model of any bottom junction capacitance is to delete \( AD \) and/or \( AS \) from the device card.

2.2. Model Parameters

This section rather than reproducing the information contained in the User's Guide groups the 37 parameters describing the MOSFET model in a logical manner.

\( LEVEL \) indicates the program which model is desired;
\( LEVEL=1 \) invokes the Shichman-Hodges model (default);
\( LEVEL=2 \) invokes the "MOS2" model to be described in the following section;
\( LEVEL=3 \) invokes the semi-empirical model described in Sec. 4.

A first classification is to divide the input data into "Electrical" (derived) and "Processing" (primary) parameters. According to this viewpoint, \( VTO \) and \( GAMMA \) are
The following 5 data are the Electrical (derived) parameters:

VTO is the Extrapolated Zero-Bias Threshold Voltage of a long and wide channel device. This voltage is derived at the onset of strong inversion and marks the point where the device starts conducting if the weak inversion current is neglected (see the description of the parameter NFS).

If VTO is not an input parameter and NSUB and TOX are specified, SPICE2 will evaluate the threshold from the equation

\[ V_{TO} = V_{FB} + 2\varphi_F + \frac{2\sqrt{\varepsilon_S SI_{NSUB}}\varphi_F}{C_{OX}} \]  

where

\[ V_{FB} = \varphi_{MS} - \frac{qN_{SS}}{C_{OX}} \]  

is the flatband voltage \[4\], \[5\] and \(\varphi_{MS}\) is the metal (poly-silicon) semiconductor work function difference. VTO will be printed out in the summary of the model parameters at the beginning of the SPICE2 output. The value VTH which is printed in the operating point information represents the threshold for given terminal voltages and for the particular device including size dependence, (see Sec. 3.1.).

KP is the Intrinsec Transconductance Parameter. If it is not specified and UO (surface mobility) and TOX are entered, it is computed by the program according to the equation

\[ KP = UO \times C_{OX} \]  

GAMMA is the Bulk Threshold Parameter and represents the proportionality factor relating the change in threshold voltage to backgate bias. It is encountered in the expression of VTO, the drain-source current \(I_{DS}\), and saturation voltage. When it is not input and if the necessary processing parameters are given, it is derived from

\[ GAMMA = \frac{\sqrt{2q\varepsilon_S I_{NSUB}}}{C_{OX}} \]  

if the necessary processing parameters are given.
PHI is the Surface Potential at strong inversion \(2\Phi_p\). When not input it is computed from

\[
PHI = 2 \frac{kT}{q} \ln \frac{NSUB}{ni}
\]  

(2.5)

LAMBDA is the Channel-Length Modulation Parameter and is equivalent to the inverse of the Early voltage for the bipolar transistor and is a measure of the output conductance in saturation. By specifying this parameter the MOSFET will have a finite but constant output conductance in saturation.

If LAMBDA is not input the LEVEL=1 model will assume a zero output conductance while the LEVEL=2 model will compute a finite and voltage-dependent output conductance defined by

\[
LAMBDA = \frac{\Delta L}{L \times V_{DS}}
\]  

(2.6)

where \(L\) is the channel length input on the device line less the lateral diffusions of the drain and source, \(L_d\), and \(\Delta L\) is a function of \(V_{DS}\) and \(V_{DSAT}\) as is shown later.

The above set of electrical parameters is adequate for the LEVEL=1 model.

In the following the parameters which characterize the gate and channel of the MOSFET are summarized. These parameters are further classified as oxide characteristics, charge concentrations and mobility parameters.

The characteristics of the thin oxide are listed below.

TOX is the Oxide Thickness and comes into the calculation of the conduction factor, backgate bias effect and gate-channel voltage-dependent capacitances.

If not specified, in the LEVEL=1 model TOX will be assumed infinite, i.e., \(V_{TOX}\), \(K_P\), or GAMMA will be defaulted rather than computed if these last quantities are not entered directly. The gate capacitances, \(C_{GS}\), \(C_{GD}\) and \(C_{GB}\) are assumed to be the overlap capacitances, i.e., they are constant with voltage. In the LEVEL=2 and =3 model, TOX defaults to 1000A implying that the gate capacitances are always voltage-dependent.

CGSO is the Gate-Source Overlap Capacitance per meter channel width and represents the capacitance due to the lateral diffusion of the source in a silicon gate MOSFET; the input value is multiplied by the channel width. This is the constant part of the total \(C_{GS}\) capacitance which has also a contribution due to the thin oxide capacitance (the voltage-dependent charges associated with the gate and channel).

CGDO is the Gate-Drain Overlap Capacitance per meter channel width. The same considerations as above apply.

CGBO is the Gate-Bulk Overlap Capacitance per meter channel length and is, as opposed to the above capacitances, a field oxide capacitance. It is the result of the
requirement that the gate has to extend beyond the channel by a certain amount
according to the specific design rules. The total $C_{QP}$ overlap capacitance results by
multiplying the above value by the channel length.

There are five parameters which describe or relate to charge concentrations.

NSUB is the Substrate Doping and is used in the derivation of most of the electric-
ical parameters. The effect of implants can be added by specifying different VTO's and
maintaining the same NSUB in the different models for the calculations, say of the
junction capacitances. NSUB can be specified for a LEVEL=1 model as well and it
assumes the same role.

NSS is the Effective Surface Charge Density and is used for the evaluation of VTO.
In most cases it is more accurate to specify VTO as obtained from a parameter extrac-
 tion system rather than NSS.

NFS is the Effective Fast Surface State Density and serves both as a flag for the
evaluation of subthreshold currents and as a quantity controlling the amount of
subthreshold current flowing in the device. If not specified, the MOSFET conducts only
in strong inversion. This parameter is meaningless for a LEVEL=1 model.

NEFF is the Total Channel Charge (Fixed and Mobile) Coefficient. It is used as a
multiplicative factor of NSUB in order to get the proper value of the output conduc-
tance in saturation. Physically it accounts for the fact that in the channel there is
both mobile and fixed charge and the total amount has to be considered for computing
the output conductance. NEFF has meaning only when the velocity saturation model is
used (VMAX is specified) in the LEVEL=2 model.

TPG is the Type of Gate indicates whether the simulated device has a metal or
polysilicon gate (and which polarity type relative to the substrate). The NGATE param-
eter of the older SPICE2 (D and E) versions has been deleted since the poly gate is usu-
ally heavily doped and the Fermi level is located very close to one of the band edges.

A last group of parameters characterizing the gate and channel refer to the pro-
PERTIES of carriers in the conductive channel. The first four describe the surface mobil-
ity and its variation with the electric field.

UO is the Surface Mobility at low gate voltages. It is the only mobility parameter
which has meaning for a LEVEL=1 or =3 model.

UCRIT is the Critical Field for Mobility Degradation and is the limit at which the
surface mobility UO starts decreasing according to the empirical relation given below.

UEXP is the Critical Field Exponent for the empirical formula which characterizes
the degradation of the surface mobility.

UTRA is the Transverse Field Coefficient for the empirical mobility degradation for-
mula.
The above four parameters enter in the following equation of the surface mobility degradation [6]

\[ \mu_s = UO \times \left( \frac{UCRIT \times S_I}{C_{ox}(V_{GS} - V_{TH} - UTRA \times V_{DS})} \right)^{UEXP} \]  

(2.7)

The above parameters are determined best by curve fitting as is shown in Sec. 5. In most cases UTRA can be chosen between 0.0 and 0.5.

VMAX is the Maximum Drift Velocity of Carriers and affects the drain-source saturation voltage of the MOSFET. It has been proven that for devices with channel lengths shorter than 10\( \mu \) the drain current saturates before the channel pinches off because the electrons (holes) reach the scattering limited velocity in the channel. The model proposed by Baum and Beneking [7] and first used in the SHOMOS model [8] is applied in order to get \( V_{DSAT} \) from the following equation

\[ V_{MAX} = \frac{I_{DSAT}}{W \times Q_{CHAN}} \]  

(2.8)

where \( I_{DSAT} \) and \( Q_{CHAN} \) are functions of \( V_{DSAT} \). More details about this are given in the following section.

VMAX also acts as a flag in the LEVEL=2 model. When specified the scattering limited velocity of carriers determines \( V_{DSAT} \); otherwise the pinch-off approach gives \( V_{DSAT} \). This parameter is meaningless for the LEVEL=1 model. When specified in LEVEL=2, the channel shortening effect uses the NEFF parameter as introduced above (see also Sec. 3).

A last category of parameters characterize the drain and source junctions of the MOSFET. There is some overlap among some of these parameters, e.g., the reverse current of the junction can be input either as IS (in A) or as JS (in A/m^2). Whereas the first is an absolute value, the second is multiplied by AD and AS to give the reverse current of the drain and source junctions respectively. This methodology has been chosen since AD and AS default to zero. The same procedure applies also to the zero-bias junction capacitances CBD and CBS on one hand, and CJ on the other as is seen in the following description.

RD and RS are the Drain and Source Ohmic Resistances and are values which apply to all devices invoking the model in which they are specified. (This was the only way for the SPICE2.D and .E versions to include series resistances).

RSH is the Sheet Resistance of the Drain and Source Diffusions and is multiplied by the number of squares NRD and NRS which are entered on each device card to give the total drain and source ohmic resistance respectively, for each device.
When both the total value (RD or RS) and the RSH are input the total value overrides.

CBD and CBS are Zero-Bias B-D and B-S junction capacitances and are total values for all devices which reference the model where they are specified.

CJ is the Zero-Bias B-D and B-S junction capacitance per m² of junction area and is multiplied by the areas AD and AS entered on the device card to give total values for the B-D and B-S junction capacitances, respectively, specific to each single device. CJ is computed automatically by the program if NSUB is specified and a step junction is assumed.

When both the total value (CBD or CBS) and CJ (or NSUB) are input, the total value overrides.

MJ is the Grading Coefficient of the B-D and B-S junctions and applies to both CBD and CBS, or CJ.

The above capacitances are well suited for modeling the bottom of the junctions. It has been found experimentally that an important part of the junction capacitance is contributed by the sidewall of the diffusion which extrapolates to a different zero-bias value and grading coefficient than those pertaining to the bottom of the diffusion. The following two parameters account for this capacitance.

CJSW is the Zero-Bias Junction Sidewall Capacitance per meter of Drain and Source Perimeter. It is multiplied by PD and PS entered on the device line to give the drain and source junction sidewall capacitances, respectively.

MJSW is the Grading Coefficient of the Junction Sidewall.

All the above capacitances and grading coefficients are determined best from curve fitting of measurements taken on specially designed test chips as is outlined in Sec. 5.

The total junction capacitance can be expressed as follows:

For reverse bias, $V_{BS} < FC \times PB$ (see below for explanation of FC and PB)

$$CBS_{tor} = CJ \left[ \frac{AS}{1 - \frac{V_{BS}}{PB}} \right] + CJSW \left[ \frac{PS}{1 - \frac{V_{BS}}{PB}} \right] \quad (2.9)$$

For forward bias, $V_{BS} > FC \times PB$

$$CBS_{tor} = CJ \left[ \frac{AS}{(1 - FC)(1 + MJ)} \right] \left[ 1 - FC(1 + MJ) + \frac{V_{BS}}{PB} \times MJ \right] \quad (2.10)$$
The above equations insure a smooth transition from the reverse bias region to the forward bias region and prevent the capacitance from increasing to infinity.

IS is the Reverse Current of the Drain or Source Junctions and is a total value, the same for all the drain and source junctions of the devices which reference the model containing IS.

JS is the Reverse Current Density of the Drain or Source Junction per \( m^2 \) of junction area. The total value IS results from a multiplication by \( AD \) and \( AS \) and is specific to each junction of each transistor.

If neither of the above currents are specified, the program will default IS to \( 1.0E^{-14} \) A. If both IS and JS are specified, IS overrides JS.

PB is the Bulk Junction Potential is used in the junction capacitance formulation.

FC is the Forward Bias Nonideal Junction Capacitance Coefficient and is used as shown above in matching the transition point and voltage characteristic of the junction capacitance when bias changes from reverse to forward. The default value of 0.5 proves satisfactory most of the time.

XJ is the Metallurgical Junction Depth.

LD is the Lateral Diffusion Coefficient in meters. The effective channel length is

\[
L = L_M - 2 \times LD
\]

where \( L_M \) is the length on the circuit mask input on the device line. In all subsequent equations \( L \) represents the effective channel length.

LD is used for the computation of \( L \) only, whereas XJ is both a flag and parameter used in the evaluation of the short-channel effect.

The only parameters not mentioned so far are

KF is the Flicker Noise Coefficient

AF is the Flicker Noise Exponent. These two parameters are used in the small-signal AC noise analysis to determine the equivalent noise current generator connected between drain and source, the value of which is

\[
I_N = \sqrt{\frac{8kTg_m}{3} + \frac{KAF}{fC_{ox}WL}}
\]

In the future an improved noise model for the MOSFET is needed.
Listed below are four model parameters which are specific to the LEVEL=3 model only. For this model, the parameters LAMBDA, UCRIT, UEXP, UTRA, and NEFF are meaningless.

ETA is the Static Feedback Effect Parameter. It is the proportionality factor which multiplies the value of \( V_{DS} \) in the \( V_{TH} \) equation implemented in MOS3 to model the static drain to gate feedback effect.

DELTA is the Channel Width Factor. This is an empirical factor which adjusts the depleted bulk charge underneath the gate to be in agreement with the observed threshold voltage increase in narrow-channel devices.

THETA is the Empirical Mobility Modulation Parameter and is used to compute mobility degradation as a function of \( V_{DS} \).

KAPPA is the Field Correlation Factor. It is used to adjust the electric field across the surface depletion region of the device in saturation.
3. IMPLEMENTATION OF SMALL-SIZE DEVICE SECOND-ORDER EFFECTS IN THE
MOS2 MODEL

This section presents the main features of the LEVEL=2 (MOS2) model and the
equations which describe the various first- and second-order effects.

The following effects are modeled in MOS2:
- Backgate bias and small-size (short- and narrow-channel) effect on threshold voltage
  considering also the static feedback from drain to gate;
- Saturation due to the scattering limited drift velocity of carriers and finite voltage-
dependent output conductance;
- Surface field dependent mobility;
- Weak inversion conduction;
- Charge controlled model of regenerative effects;
- Variation of all quantities with temperature.

In the rest of this section the pertinent equations are listed with emphasis on the
influence of the different input parameters.

3.1. Threshold Voltage

From the zero-bias threshold voltage $V_{TO}$ given in Sec. 2, which applies for a MOS-
FET with large dimensions ($W, L > 20 \mu m$) and with the source and bulk connected
together, SPICE2.G readjusts this value to $V_{TH}$ at each operating point and for each
transistor according to its size.

Physically the following effects take place:
- An increase of the bulk-to-source voltage increases the depletion charge which causes
  $V_{TH}$ to go up.
- In a short-channel device part of the depletion charge in the bulk terminates the elec-
tric field of the drain and source junctions. The electric field from gate to bulk
depletes less charge and thus $V_{TH}$ is lowered. This can be viewed by the trapezoid
approach introduced by Yau [9] and which is used by SPICE2 (see Fig. 3.1.).
- The edge effects in a narrow channel cause the depletion charge to extend beyond the
  width of the channel. The gate-to-bulk field has to be increased to balance this charge;
  thus, $V_{TH}$ increases (see Fig. 3.2.).
- The amount of charge underneath the gate depleted by the drain junction field rather
  than the gate-to-bulk field increases with $V_{DS}$ thus lowering $V_{TH}$. This effect is approxi-
mated geometrically in MOS2 as shown in Fig. 3.3. and is referred to as the static
drain-to-gate feedback on threshold.

An equation for $V_{TH}$ which sums up the above features, can be expressed as
\[(x + x_J)^2 = (x_J + w_0)^2 - w_0^2\]

\[x = x_J \left( \sqrt{1 + \frac{2w_0}{x_J}} - 1 \right)\]

\[Q_B = w_0 \times L\]

\[Q_B' = w_0 \left[ L - x_J \left( \sqrt{1 + \frac{2w_0}{x_J}} \right) \right]\]

\[\frac{Q_B'}{Q_B} = \left[ 1 - \frac{x_J}{L} \left( \sqrt{1 + \frac{2w_0}{x_J}} - 1 \right) \right]\]

FIG. 3.1.
FIG. 3.2.
\[ V_{TH} = V_{BIN} + \gamma_s \sqrt{2 \phi_F - V_{BS}} \]  

(3.1)

where

\[ V_{BIN} = V_{BI} + \text{DELT}A \frac{\pi \varepsilon_s l}{4 C_{ox} W} (2 \phi_F - V_{BS}) \]  

(3.2)

is the corrected built-in voltage for narrow channel, and

\[ V_{BI} = V_{FB} + 2 \phi_F \]  

(3.3)

\( \gamma_s \) is the corrected \( \gamma \) for short-channel with static drain-to-gate feedback (see Fig. 3.3.)

\[ \gamma_s = \text{GAMMA} (1 - \alpha_s - \alpha_D) \]  

(3.4)

where \( \alpha_D \) and \( \alpha_s \) are the correction factors for the depletion charge at the drain and source, respectively,

\[ \alpha_s = \frac{1}{2} \frac{X_D}{L} \left[ \sqrt{1 + 2 \frac{W_s}{X_D}} - 1 \right] \]  

(3.5)

\[ \alpha_D = \frac{1}{2} \frac{X_D}{L} \left[ \sqrt{1 + 2 \frac{W_D}{X_D}} - 1 \right] \]  

(3.6)

The depletion widths \( W_s \) and \( W_D \) are

\[ W_s = X_D \sqrt{2 \phi_F - V_{BS}} \]  

(3.7)

\[ W_D = X_D \sqrt{2 \phi_F - V_{BS} + V_{DS}} \]  

(3.8)

where

\[ X_D = \sqrt{\frac{2 \varepsilon_s l}{q NSUB}} \]  

(3.9)

The implementation of the geometry in Fig. 3.3. represents an idealization of the actual depletion layer shape. Preliminary results show that it offers a good approximation at a minimum computational effort.

It should be noticed that the absence of \( X_J \) from the input file bypasses the correction for short channel effect.
DASHED ZONE - BULK CHARGE DEPLETED BY GATE FIELD

FIG. 3.3
3.2. Drain-Source Current

In order to correct for small dimensions, the implemented drain-source current equation is slightly modified relative to previous formulations [4], [5] which include the effect of the bulk charge.

The current in strong inversion \((V_{GS} > V_{TH})\) is given by

\[
I_{DS} = \beta \left( V_{GS} - V_{BIN} - \frac{\eta V_{DS}}{2} \right) V_{DS} - \frac{2}{3} \gamma_{S} \left( 2 \varphi_{F} + V_{DS} - V_{BS} \right)^{3/2} - \left( 2 \varphi_{F} - V_{BS} \right)^{3/2} \]

where

\[
\eta = 1 + \Delta \gamma \frac{\pi \epsilon_{Si}}{4 \epsilon_{ox} W}
\]

\[
\beta = \frac{W}{L} \mu_{S} C_{ox}
\]

It can be seen that the narrow channel effect is included through \(V_{BIN}\) given in Eq. (3.2) and \(\eta\). The short channel uses the corrected \(\gamma_{S}\). \(\mu_{S}\) represents the degraded surface mobility. For large \(W\) and \(L\) the above equations revert to the well known forms [4], [5].

3.3. Operation in the Saturation Region

3.3.1. Saturation due to Pinch-off, Channel Length Modulation

As mentioned earlier, if \(V_{MAX}\) is not input the program computes the saturation voltage \(V_{DSAT}\) assuming the channel pinches off at the drain limit. With the corrections for small-size effects, \(V_{DSAT}\) is

\[
V_{DSAT} = \frac{V_{GS} - V_{BIN}}{\eta} + \frac{1}{2} \left( \frac{\gamma_{S}}{\eta} \right)^{2} \left[ 1 - \left( 1 + 4 \left( \frac{\eta}{\gamma_{S}} \right)^{2} \frac{V_{GS} - V_{BIN} + 2 \varphi_{F} - V_{BS}}{\eta} \right)^{1/2} \right]
\]

The finite output conductance observed in saturation is due to the spread of the pinch-off region into the channel thus reducing the effective channel length, \(L_{eff} = L - \Delta L\), and increasing the geometrical ratio of the conduction factor.

\[
\frac{W}{L - \Delta L} = \frac{W}{L(1 - \Lambda \delta X V_{DS})}
\]
LAMBDA = \frac{\Delta L}{L \times V_{DS}}

If LAMBDA is not an input parameter, its value is computed according to Eq. (3.12) where

\[ \Delta L = X_D \left[ \frac{V_{DS} - V_{DSAT}}{4} + \sqrt{1 + \frac{1}{4} \left( \frac{V_{DS} - V_{DSAT}}{4} \right)^2} \right]^{1/2} \] (3.13)

This formulation does not include the effect of the field between gate and drain and gate and pinch-off point respectively [10], but insures the continuity of the current and its first derivative at the transition from the triode- into the saturation region (important in an iterative solution algorithm of nonlinear simultaneous equations). Another drawback of the above formulation of the channel modulation is that it overestimates the output conductance in saturation.

One problem with short channel devices is that at high \( V_{BS} \) punch-through occurs. This effect is not modeled in SPICE2. In order to prevent the channel length from going negative, Eq. (3.12) is used only when the effective channel length \( L_{eff} \) is larger than the zero-bias depletion layer width \( W_B \), \( (W_B = X_D \sqrt{P_B}) \). When \( L_{eff} \) gets smaller than \( W_B \), Eq. (3.12) is replaced by

\[ L_{eff} = \frac{W_B}{1 + \frac{\Delta L - L_{max}}{W_B}} \] (3.14)

where

\[ L_{max} = L - W_B \] (3.15)

Although this equation does not model punch-through it prevents numerical non-convergence problems that have been observed.

3.3.2. Saturation due to Scattering Limited Velocity; Channel Length Modulation

In short-channel MOSFETs the saturation of the current occurs because the charge carriers reach their maximum scattering limited velocity before pinch-off. In other words, a lower current is expected from a short channel device as compared to a long channel device of identical geometric ratios, processing and biasing conditions.

\( V_{DSAT} \) is obtained as the solution of Eq. (2.8) after substituting the expressions for \( I_{DSAT} \) and \( Q_{CHAN} \). This leads to
A problem arises because $Q_{CHAN}$ is defined at the point where the carriers reach their maximum velocity. This point moves towards the source as $V_{BS}$ increases. The shortening of the channel is implemented in MOS2 as proposed by Baum [7],

$$L_{eff} = L - X_D \sqrt{\frac{X_D \ VMAX^2}{2 \mu_S}} + \frac{X_D VMAX}{2 \mu_S} \ (3.17)$$

In this theory on a $V_{GS}$=constant curve, the saturation voltage varies (decreases) as $V_{BS}$ increases. From a numerical point of view this requires the simultaneous solution of two nonlinear equations, i.e., iterative computation which increases the computer analysis time. There is a proposal [11] which limits the solution to two iterations. However the method adopted in SPICE2.G precludes any nested iterative process based on the following assumptions:

First, define $V_{KA}$ according to Eq. (3.16) with $L_{eff} = L$ and use this value for any $V_{BS}$ on a $V_{GS}$=constant characteristic. This is based on the fact that Eq. (3.17) does not provide an accurate description of the output conductance in saturation and $NEFF$ has to be used as an empirical factor. In the expression of $X_D$, Eq. (3.9), NSUB is replaced by $NEFF*NSUB$.

Second, good agreement of the simulated and measured I-V characteristics can be obtained by adjusting NEFF.

A closed-form solution can be obtained as follows. Eq. (3.16) can be simplified to obtain

$$v = \frac{(V_1 - \frac{x^2}{2}) (x^2 - V_2) - \frac{2}{3} \gamma_S (x^3 - V_2^\frac{3}{2})}{V_1 - \gamma_S x - x^2} \ (3.18)$$

where

$$x = \sqrt{V_{DSAT} + 2\varphi_F - V_{BS}}$$

$$V_1 = \frac{V_{GS} - V_{BIN}}{\eta} + 2\varphi_F - V_{BS}$$

$$V_2 = 2\varphi_F - V_{BS}$$
Eq. (3.16) can be written as a quartic equation

\[ x^4 + ax^3 + bx^2 + cx + d = 0 \quad (3.19) \]

with

\[ a = \frac{4}{3} \gamma_s \]

\[ b = -2(V_1 + \nu) \]

\[ c = -2\gamma_s \nu \]

\[ d = -V_2^2 - \frac{4}{3} \gamma_s V_2^2 + 2V_1V_2 + 2\nu V_1 \]

This equation can be solved by Ferrari's method. Among the 2 or 4 real roots, the smallest positive one is the valid solution; the choice is based on the fact that the equation represents the difference

\[ I_{DSAT} - V_{MAX} \times W \times Q_{CHAN}(L) \quad (3.20) \]

which decreases as \( V_{DSAT} \) increases.

In some cases the equation might not have a real solution. In this case the program computes \( V_{DSAT} \) based on the pinch-off approximation and prints out a message.

### 3.4 Weak Inversion Conduction

A MOSFET is not an ideal switch which starts conduction abruptly; there is current flowing in the device below the threshold voltage which marks only the onset of strong inversion. This current is known as the weak inversion or subthreshold current. The simulation of this behaviour is important for present day MOS circuits which are often designed to operate in the weak inversion region. The model implemented in SPICE2.G uses as a starting point the analysis performed by Swanson and Meindl for CMOS devices [12].

As shown in Fig. 3.4, a new threshold voltage \( V_{GN} \) is defined, above \( V_{TH} \), which marks the transition from the weak inversion to the strong inversion characteristic.
\[ V_{ON} = V_{TH} + \frac{n kT}{q} \]  

(3.21)

where

\[ n = 1 + \frac{C_{FS}}{C_{OX}} \frac{C_D}{C_{OX}} \]  

(3.22)

\[ C_{FS} = q \times NFS \]  

(3.23)

\[ C_D = \frac{\partial Q_B}{\partial V_{BS}} = \left\{ -\gamma_S \frac{d \sqrt{2 \Phi_F - V_{BS}}}{dV_{BS}} - \frac{\partial \gamma_S}{\partial V_{BS}} \sqrt{2 \Phi_F - V_{BS}} + \Delta \frac{\pi e_S}{4 C_{OX}} \right\} C_{OX} \]  

(3.24)

NFS is introduced as a parameter in the evaluation of \( V_{ON} \). Its presence is necessary to invoke the weak inversion feature. NFS is not related to the physical nature of the subthreshold conduction, which is not determined by the fast surface state density. It is a curve-fitting parameter which can be extracted from measurements.

In the above equation it is important to notice that the quantity \( \sqrt{2 \Phi_F - V_{BS}} \) which is a multiplicative factor of the depletion-charge formulation assumes that \( V_{BS} \) is negative. A more exact way to express Eq. (3.24) is to replace the square root by a \( F(V_{BS}) \).

In the new MOS2 model, this function is made to decay asymptotically towards zero when \( V_{BS} \) becomes positive rather than clamp it to zero as was the case in the SPICE2.D and .E versions;

\[ F(V_{BS}) = \frac{\sqrt{2 \Phi_F}}{1 + V_{BS} / 4 \Phi_F} \]  

(3.25)

The weak inversion current equation for \( V_G < V_{ON} \) is

\[ I_D = \beta \left( \frac{V_{ON} - V_{BIN} - \frac{\eta V_{BS}}{2}}{2} \right) V_{DS} - \frac{2}{3} \gamma_S \left( (2 \Phi_F - V_{BS} + V_{DS})^{\frac{3}{2}} - (2 \Phi_F - V_{BS})^{\frac{3}{2}} \right) \times e^{\frac{2}{kT}(V_{GS} - V_{ON})} \]  

(3.26)

This equation insures the continuity of the current at \( V_{ON} \) but not the continuity of the first derivative in contrast to the previous formulation [2]. This alternative has been chosen since the earlier expression suffered from introducing a negative resistance in the \( I_D - V_{DS}, V_{GS} = \text{constant characteristics} \).
FIG. 3.4.
In order to obtain the usual aspect of the characteristics in the $I_{DS}-V_{DS}$ plane a saturation voltage is defined at $V_{GS}=V_{ON}$ which replaces $V_{DS}$ in Eq. (3.26) when the latter becomes larger than the former. The role of the exponential factor is then to scale this characteristic.

### 3.5. Temperature Dependence

The MOS2 model readjusts all temperature-dependent variables in the drain-source current equation. These include:
- proportionality with $T$ of the Fermi potential $\varphi_F$;
- variation with temperature of the energy gap;
- temperature dependence of the built-in voltage $V_B$ of the drain and source junctions;
- mobility variation as $T^{-3/2}$;
- temperature variation of the reverse current of the diffused junctions.

### 3.6. Charge-Oriented Model for MOSFET Capacitances

Meyer's capacitance model [13] which has been used in earlier versions of SPICE2 suffers from a fundamental weakness: it does not conserve charge. An improved formulation of the charge-oriented model proposed by Ward and Dutton [14] is used in SPICE2.G. The new model is based on the actual distribution of charge in the MOS structure and its conservation:

$$ Q_{CHAN} = Q_D + Q_S = -(Q_G + Q_B) $$

The current flowing at any terminal of a region can be related to the charge contained in that region, i.e.,

$$ i_C = \frac{dQ_C}{dt} $$

$$ i_B = \frac{dQ_B}{dt} $$

$$ i_S + i_D = \frac{d(Q_S + Q_D)}{dt} $$

The equivalent terms of the modified nodal admittance matrix are found by using the numerical implicit integration algorithm already built into the circuit simulator for the transient analysis [15].
\[ \int_{t_0}^{t_1} idt = Q(t_1) - Q(t_0) \] (3.29)

The charges at any time point are assumed a function of only the terminal voltages at that same time point. Due to the complexity involved in finding the derivatives, a simple formulation is used for the charges [16] which is adjusted for continuity at the transitions between regions of operation. The exact formulations are the subject of a future write-up. If the trapezoidal integration formula is used, Eq. (3.29) can be rewritten as follows

\[ \frac{h}{2}(t_{y1}^1 + t_{y0}) = (Q_{y1}^0 - Q_{y0}) + \sum_x \frac{\partial Q_y}{\partial V_x} V_x^{2_1} (V_{x1}^{2_1} - V_{x1}^{0_1}) \] (3.30)

where x stands for GB, DB and SB, and y for G, B, D and S. The subscripts indicate the time point and superscripts the iteration. Thus quantities at time point "0" are known (previous time point), quantities at time point "1" iteration "0" are also known from the solution of the last iteration at the present time point. Time "1", iteration "1" is the current iteration which, by substituting the above equation into the modified nodal system, has \( V_{x1}^{0_1} \) as a solution.

Defining capacitances for the small-signal analysis

\[ C_{yz} = \frac{\partial Q_y}{\partial V_x} \] (3.31)

one notes that between each pair of nodes there are two capacitances, which in general are different.

Fig. 3.5. plots the voltage dependence of the various terminal capacitances associated with the \( Q_G \) and \( Q_B \) charges. Only six capacitances out of a total of twelve defined by Eq. (3.31) are independent due to the charge-conservation principle expressed by Eq. (3.27). \( Q_S \) and \( Q_D \) share equal parts of the channel charge \( Q_{CHAN} \) in the linear region. In saturation \( Q_D \) gets only \( XQC \times Q_{CHAN} \) where \( XQC \) is a model input parameter which defaults to zero; \( Q_S \) results from Eq. (3.27).
4. THE MOS3 MODEL: A SEMI-EMPirical MODEL FOR SMALL GEOMETRY MOSFET'S

A small-geometry MOSFET, defined as a transistor with \( L \leq 2 \mu m \) and \( W \leq 2 \mu m \) is characterized by the following features:

- threshold-voltage sensitivity to the length and the width of the device due to the two-dimensional nature of potential distribution;
- threshold-voltage sensitivity to the drain voltage due to the drain induced barrier lowering;
- relaxed transition between linear and saturation regions, and lowered saturation voltage and saturation current due to the velocity saturation of hot electrons.

The MOS3 model has been developed to address the above features and the computational efficiency. The companion capacitance model, which conserves charge [14], is also derived and implemented.

Instead of repeating the physical explanations already presented in the previous section, the MOS3 model is described in simple terms with emphasis on the different approaches between the MOS2 and MOS3 models, followed by the parameter extraction methodology of those newly introduced parameters and the performance comparison between MOS2 and MOS3.

All the parasitic resistances, overlap and junction capacitances are described by the same parameters as in MOS2. The model parameters relating to the intrinsic MOSFET are designed to be compatible with those of MOS2. The rule of "Electrical" and "Processing" parameters also holds for MOS3. The four new parameters which are specific to MOS3 are described in Sec. 2. ETA, DELTA and KAPPA are dimensionless "Electrical" parameters, of typical values close to 1. THETA is an "Electrical" parameter of unit 1/Volt. Its typical value is approximately 0.1.

4.1. Threshold Voltage

The relationship between \( V_{TH} \), the threshold voltage, and the substrate bias deviates from the first-order square root dependence as the device dimensions are scaled down. This is mainly because the built-in potential depends logarithmically on the substrate doping which is scaled up proportionally with the dimensions. This feature is modeled by decoupling the effects of channel length, channel width and static feedback from drain to gate. Each of these features is enabled by specifying the parameters XI, DELTA and ETA, respectively.

The short-channel effect, the decrease of \( V_{TH} \) as the channel length is scaled down, is modeled with Dang's [17] modified trapezoidal approach, reckoning with the influence of cylindrical field distribution (see Fig. 4.1).
$$\Phi - V_{BS} = \frac{XJ^2}{X_D} \left( 1 + \frac{W_C}{XJ} \right) \left[ \ln \left( 1 + \frac{W_C}{XJ} \right) - \frac{1}{2} + \frac{1}{2(1 + \frac{W_C}{XJ})} \right] = \left( \frac{W_P}{X_D} \right)^2$$

$$\frac{W_C}{XJ} = d_0 + d_1 \frac{W_P}{XJ} + d_2 \left( \frac{W_P}{XJ} \right)^2$$

$$\left( \frac{W_S + LD}{W_P + XJ} \right)^2 + \left( \frac{W_S + LD}{W_C + LD} \right)^2 = 1$$

$$W_S = (W_C+\delta) \left[ 1 - \frac{W_0^2}{(W_P+XJ)^2} \right] - LD$$

**FIG. 4.1.**
The narrow channel effect, the increase of $V_{TH}$ as the channel width is scaled down, is modelled by taking into account the extra bulk charge at the edge of the channel as described in the previous section. To include other edge effects such as the existence of field implant and non-planarity due to the LOCOS process, the empirical parameter DELTA is introduced.

The static feedback effect can be explained as a consequence of the drain induced barrier lowering [18]. A term, linearly proportional to $V_{DS}$, is included in the $V_{TH}$ expression. The constant of this term is inversely proportional to the oxide capacitance and the cube of the channel length [19]. The parameter ETA is introduced to allow more flexibility.

An expression for $V_{TH}$ which sums up the above features is formulated as:

$$V_{TH} = V_{FB} + 2\phi_F - \sigma V_{DS} + \gamma F_S \sqrt{2\phi_F - V_{BS}} + F_n (2\phi_F - V_{BS})$$  \hspace{1cm} (4.1)

where

$$\sigma = \text{coefficient of static feedback}$$  \hspace{1cm} (4.2)

$$\eta = \frac{\text{ETA} \Omega}{C_{ox} L^6}$$

$$\Omega = \text{empirical constant}$$  \hspace{1cm} (4.3)

$$= 8.15 \times 10^{-22} \; (F \times m)$$

$$F_S = \text{correction factor of short channel effect}$$  \hspace{1cm} (4.4)

$$= 1 - \frac{XJ}{L} \left[ \frac{LD + W_C}{XJ} \sqrt{1 - \frac{W_P/XJ}{1 + W_P/XJ}} - \frac{LD}{XJ} \right]$$

$LD$ is the lateral diffusion length, $W_P$ is the depletion layer width of a plane junction, $W_C$ is the depletion layer width of a cylindrical junction and

$$\frac{W_C}{XJ} = d_0 + d_1 \frac{W_P}{XJ} + d_2 \left( \frac{W_P}{XJ} \right)^2$$  \hspace{1cm} (4.5)

d_0, d_1 and d_2 are empirical constants of values:

$$d_0 = 0.0831353$$

$$d_1 = 0.8013292$$
$d_2 = -0.01110777$

and

$$F_N = \text{correction factor of narrow channel effect} \quad (4.6)$$

$$= DE\Delta \frac{\pi \varepsilon_{\text{SI}}}{2C_{\text{OX}} W}$$

$$X_D = \text{coefficient of depletion layer width} \quad (4.7)$$

$$= \sqrt{\frac{2\varepsilon_{\text{SI}}}{qN_{\text{SUB}}}}$$

4.2. Basic Drain Current Equation

The drain current can be expressed as:

$$I_{DS} = \beta \int_0^{V_{DS}} [V_{GS} - V_{TH}(y)] dV_y \quad (4.8)$$

$$= \beta \int_0^{V_{DS}} [V_{GS} - V_{TH} - (1 + F_B)V_y] dV_y$$

where

$$\beta = \frac{W}{L} \mu_{\text{EFF}} C_{\text{OX}} \quad (4.9)$$

$$F_B = \text{Taylor series expansion coefficient of bulk charge} \quad (4.10)$$

$$= \frac{\gamma F_S}{4\sqrt{2\phi_F - V_{BS}}} + F_N$$

After the integration, the following equation is obtained [20]:

$$I_{DS} = \beta \left[ V_{GS} - V_{TH} - \frac{1 + F_B}{2}V_{DS} \right] V_{DS} \quad (4.11)$$

With such simplicity, an explicit saturation voltage expression is guaranteed. Based on the assumption that the $V_{DS}$ dependent term in $V_{TH}$ represents the average drain voltage influence on the channel potential, it is treated as a constant throughout the integration.
4.3. Surface Mobility Modulation by Gate Voltage

The simplest empirical equation is used to enhance the computational speed:

\[ \mu_s = \frac{U_0}{1 + \Theta(V_{GS} - V_{TH})} \]  

(4.12)

4.4. Velocity Saturation of Hot Electrons

The saturation of hot electron velocity lowers the conduction current in the linear region. Thus relaxes the transition between the linear and the saturation regions. In the linear region this effect is modelled by the conventional hyperbolic equation [21]:

\[ \mu_{EFF} = \frac{\mu_s}{1 + \frac{\mu_s}{V_{MAX} \times L} V_{DS}} \]  

(4.13)

If the parameter VMAX is not specified by the user, \( \mu_{EFF} \) is set to \( \mu_s \) and this effect is not modelled.

4.5. Saturation Voltage

The saturation voltage of a short-channel device is the drain voltage at which the carriers asymptotically reach the maximum velocity at the drain limit (see Fig. 4.2):

\[ I_{DS}^{\infty} = Q_H(drain) V_{MAX} \]  

(4.14)

After the substitution of the expressions of \( Q_H \) and \( I_{DS}^{\infty} \), the above equation becomes:

\[ \frac{W}{L} \mu_s C_{OX} \left[ V_{GS} - V_{TH} - \frac{1 + F_B}{2} V_{DSAT} \right] \]  

\[ V_{DSAT} = \frac{W \times C_{OX} \left[ V_{GS} - V_{TH} - (1 + F_B) V_{DSAT} \right]}{V_{MAX}} \]  

(4.15)

From the above equation \( V_{DSAT} \) is solved,

\[ V_{DSAT} = \frac{V_{GS} - V_{TH}}{1 + F_B} + \frac{V_{MAX} \times L}{\mu_s} \sqrt{\frac{V_{GS} - V_{TH}^2}{1 + F_B}} + \frac{V_{MAX} \times L^2}{\mu_s} \]  

(4.16)

\( V_{DSAT} \) will depend on \( V_{DS} \) if the parameter ETA is not zero. If parameter VMAX is absent from the input, the saturation voltage will be determined by the maximum of the drain current equation, corresponding to the situation of channel pinch-off:
\[ V_{\text{DSAT}} = \frac{V_{\text{GS}} - V_{\text{TH}}}{1 + F_B} \] (4.17)

4.6. Channel Length Modulation

As \( V_D \) becomes greater than \( V_{\text{DSAT}} \), the point where the carrier velocity begins to saturate moves towards the source. The channel length reduction, \( \Delta L \), is formulated based on Baum's theory \[7\] :

\[
\Delta L = \sqrt{\frac{E_P X_G^2}{2}} + \kappa \times X_G^2 (V_D - V_{\text{DSAT}}) - \frac{X_G^2 E_P}{2}
\] (4.18)

where

\[ E_P = \text{lateral field at channel pinch-off point} \] (4.19)

\( I_{\text{DSAT}} \) and \( G_{\text{DSAT}} \) are the drain current and the drain conductance at saturation respectively.

It should be noted that the point where the velocity begins to saturate differs from the point where the inversion charge goes to zero, i.e., the channel pinch-off point. \( V_{\text{DSAT}} \) is the voltage at velocity saturation, while \( E_P \) is the lateral field at channel pinch-off. Thus the voltage across the depleted surface, of length \( \Delta L \), should be less than \( (V_D - V_{\text{DSAT}}) \). The parameter \( \kappa \) is introduced to account for this effect. As \( \Delta L \) approaches \( L \), the same scheme as described in Sec. 3.3.1 is used to prevent a negative effective channel length.

4.7. Weak Inversion Conduction

The equations in the weak inversion region are the same as those used in MOS2, which provide both the continuity of the drain current, the proper bias dependence and sufficient computational efficiency. The same parameter NFS is used to turn on the weak inversion feature. For details see Sec. 3.4.
FIG. 4.2.
4.8. Temperature Dependence

All the quantities referred to in the model equations have the same temperature dependence as in MOS2. The four newly introduced parameters are all empirical. No temperature dependence has been developed for them as yet.

4.9. Capacitance Model with Charge Conservation

The total amount of charge residing on the gate, \( Q_G \), can be evaluated as:

\[
Q_G = W \int_0^L q_g(y) \, dy
\]

where

\[
q_g = \text{gate charge per unit area}
\]

\[
= \frac{\mu_s W^2 V_{DS}}{L_{DS}} \int_0^L q_g(y) q_c(V_y) \, dV_y
\]

\[
q_c = \text{channel charge per unit area}
\]

\[
= -C_{ox} \left[ V_{GS} - V_{TH} - (1 + F_B) V_y \right]
\]

After carrying out the integration,

\[
Q_G = W \times L \times C_{ox} \left[ V_{GS} - (V_{FB} + 2\varphi_P - \sigma V_{DS}) - \frac{V_{DS}}{2} + \frac{1 + F_B}{12 F_I} V_{DS}^2 \right]
\]

where

\[
F_I = V_{GS} - V_{TH} - \frac{1 + F_B}{2} V_{DS}
\]

Similarly, one can get the total bulk charge \( Q_B \) as

\[
Q_B = -W \times L \times C_{ox} \left[ \frac{F_S \sqrt{2\varphi_P - V_{BS}} + F_N (2\varphi_P - V_{BS}) + \frac{F_B}{2} V_{DS} - \frac{F_B (1 + F_B)}{12 F_I} V_{BS}^2}{12 F_I} \right]
\]

The total channel charge \( Q_{CHAN} \) results from the charge conservation principle,

\[
Q_{CHAN} = -(Q_G + Q_B)
\]

It is equally divided into the source and the drain charges in the linear region of
operation. In saturation \( Q_d \) gets a share \( XQC \) of \( Q_{CHAN} \).

Each of these charges has three associated derivatives which are the capacitive elements in the circuit model. It should be noted that only six of these twelve capacitive components are independent.

4.10. Parameter Extraction for MOS3

The characteristics of small geometry MOSFETs are sensitive to the device dimensions. The systematic parameter extraction requires measurements of several devices with different combinations of length and width, and the manipulation of the collected data. The fundamental parameters \( VTO, NSUB, UO \) and/or \( GAMMA \) and \( KP \), which are common to both MOS2 and MOS3, should be extracted from a long and wide device, as described in next section. Only the extraction methodology of parameters relating to the second-order effects is described in the following:

4.10.1. THETA, Mobility Modulation Parameter

The effective surface mobility is the slope of the \( [(L \times I_{DS})/(W \times C_{OX} V_{DS})] \) versus \( V_{GS} \) plot in the linear region, at constant \( V_{DS} \) and \( V_{BS} \), as indicated by the current equation, (4.11). Rearrange Eq. (4.12) as:

\[
\frac{UO}{\mu_S} = 1 + \text{THETA}(V_{GS} - V_{TH})
\]  

(4.27)

Clearly, parameter THETA is the slope of the \( (UO/\mu_S) \) versus \( V_{GS} \) plot. In order to isolate the gate voltage influence from the hot electron effect, the measurements of \( I_{DS} \) versus \( V_{CS} \) must be carried out at low \( V_{DS} \), say 0.2 volts.

4.10.2. ETA, Static Feedback Parameter

The coefficient \( \sigma \), the slope of the \( V_{TH} \) versus \( V_{DS} \) plot at constant \( V_{BS} \) as defined in Eq. (4.2), represents the magnitude of the static feedback effect. The determination of \( \sigma \) involves the measurement of the threshold voltage of small geometry MOSFET's at intermediate \( V_{DS} \) level. The \( V_{TH} \)'s should be determined from the \( I_{DS} \) versus \( V_{GS} \) curves at different \( V_{DS} \), at low current levels (see Fig. 4.3).
FIG. 4.3.

\textit{voltage offset = delta VTH}
Other threshold voltage determination algorithms, based on either the simple saturation current equation which is proportional to the square of \((V_{GS} - V_{TH})\) or the approximately linear current equation which is proportional to \((V_{GS} - V_{TH} - V_{DS}/2)V_{DS}\), does not hold because of the hot electron effect. Parameter ETA is related to \(\sigma\) by

\[
ETA = \sigma \frac{C_{ox} L^3}{\Omega} \tag{4.28}
\]

The value of the empirical constant \(\Omega\), see Eq. (4.3), has been adjusted such that, for most practical devices, ETA assumes a value close to one.

4.10.3. DELTA, Width Effect on Threshold Voltage

The coefficient of the width effect on \(V_{TH}\) at constant \(V_{DS}\), relates inversely to the channel width as indicated by Eq. (4.6). DELTA relates to \(F_N(2\varphi_F - V_{BS})W\), the slope of \(V_{TH}\) versus \(1/W\) plots, as:

\[
DELTA = \text{slope} \frac{2C_{ox}}{\pi \varepsilon_S} \frac{1}{(2\varphi_F - V_{BS})} \tag{4.29}
\]

Its value varies from process to process.

4.10.4. VMAX, Limited Velocity of Hot Electrons

The effective mobility at intermediate \(V_{DS}\) level deviates from the value at low \(V_{DS}\), \(\mu_S\). The parameter VMAX can be estimated as follows: measure \(I_{DS}\) versus \(V_{GS}\) at different fixed \(V_{DS}\)'s, extract the effective mobility, \(\mu_{EFF}\), from the collected data, and finally plot \((1/\mu_{EFF} - 1/\mu_S)\) versus \(V_{DS}/L\). The slope of this plot is the inverse of VMAX as indicated by the rearrangement of Eq. (4.13):

\[
\frac{1}{\mu_{EFF}} - \frac{1}{\mu_S} = \frac{V_{DS}}{\text{VMAX} \times L} \tag{4.30}
\]

4.10.5. KAPPA, Correlation Coefficient of the Drain Field in Saturation

The extraction of parameter KAPPA from measurement is not as straightforward as for the other parameters. First, one has to estimate the approximate saturation voltage and saturation current using the VMAX obtained, as above. Then the channel length reduction can be estimated as:

\[
\Delta L = L (1 - \frac{I_{DS}}{I_{DSAT}}) \tag{4.31}
\]

The slope of \(\Delta L^2\) versus \(V_{DS}\) plot is approximately \(KAPPA \times X_F\).
4.11. Performance Comparison between MOS2 and MOS3

Though MOS2 and MOS3 share most of the model parameters, different values for the same parameter must be used to produce approximately the same characteristics. For example, the parameter VMAX has no effect on the linear region characteristics of MOS2, while it lowers the effective mobility of MOS3. In order to get a match, a lower value for UO in MOS2 is required.

The $V_{BS}$ dependence of the basic drain current equation in MOS3 is an approximation of that in MOS2. With all other parameters being properly adjusted for a specific device, say $L=5\mu m$, $NSUB=4 \times 10^{16} \text{ cm}^{-3}$ and $TOX=0.1 \mu m$, this approximation only introduces about 2% deviation in the case of $V_{GS}$ well above $V_{TH}$. The deviation increases to 20% when the gate voltage is only 0.5 volts above $V_{TH}$. However, in the latter case, the device is already approaching subthreshold conduction and the basic strong inversion theory begins to fail.

The benchmark runs with SPICE2.G indicate that, with compatible input parameters, the MOS3 model is up to 40% faster in the model computation time as compared with MOS2, depending upon the nature of the circuit and its operation.
5. MODEL PARAMETER EXTRACTION

Naturally the accuracy of the results of a MOS IC simulation depends heavily on the values of the model input parameters. The I-V characteristics predicted by the equations of the model must match very closely the measured characteristics. The complexity of the equations in Sec. 3 is such that some computer aids are required to obtain the program value of the device parameters. The best results are obtained if a characterization system is set up [22] which has as core a desk-top or a mini computer which controls the measuring instruments and does the necessary computations for finding the model parameters. The equations implemented in the parameter extraction program must be identical to those used in the circuit simulator. A data acquisition software designed for a certain model provides accurate input parameters only for that particular model. When the model is changed, the parameter extraction software has to be changed as well.

Another tool necessary for parameter extraction is a test chip which should have the following features:
- a short- and a long channel MOSFET;
- a narrow- and a wide channel device;
- diffused resistances;
- poly-silicon resistances;
- a rectangular and a meander form junction capacitor;
- a thin and a field oxide capacitor.

A desired feature of the parameter extraction software is to find the spread of the parameters for a number of wafer runs and to group the parameters according to a certain criterion, e.g., speed or power consumption, into a worst, best and nominal case input file [23].

It is the purpose of this section to illustrate the methodology and the minimum hardware software to extract the main input parameters for the MOS2 model. The reported work has been performed using a Tektronix 4051 desktop calculator, Tektronix 576 curve tracer, a C-V measuring instrument and a multimeter.

5.1. VTO and NSUB Measurement

The measurement is taken on a saturated transistor connected to a curve tracer. Since at this starting point few parameters are known, the saturated characteristic is approximated by a parabola rather than using the exact current equation given in Sec. 3.
where $C_{j_1}$ is the ordinate at the origin of the C-V plot and $A_1$ is the area (known) of the rectangular capacitor. The measured results indicate that $M_J$ is very close to 0.5.

$C_{JSW}$ and $M_{JSW}$ can be found using a linear regression through the $(V_R, C_{j_2})$ data points of the meander-form diffusion. Eq. (5.4) can be rewritten as

$$\log C_K = \log (P \times C_{JSW}) - M_{JSW} \times \log \left(1 + \frac{V_R}{P_B}\right)$$ \hspace{1cm} (5.5)

where

$$C_K = C_{j_2} - A_2 \left[ \frac{C_{j_1}}{V_R} V_R^2 \right]^{1 + \frac{1}{P_B}}$$ \hspace{1cm} (5.6)

The data processing is performed by PROGRAM1 (see Appendix 1) which, in response to the point pairs $(V_R, C_{j_2})$ and other constants, displays the result of the interpolation, i.e., $C_{JSW}$ and $M_{JSW}$.

If $M_J = 0.5$ is not adequate, PROGRAM1 can be easily modified to perform the same linear regression as Eq. (5.5) for the large rectangular capacitor only to find $M_J$.

5.3. Mobility Parameter Extraction

Finding the parameters which describe the mobility variation with the surface field is very important for an accurate simulation of the I-V characteristic. $U_O$, $U_{CRIT}$, and $U_{EXP}$ which appear in the mobility degradation formula of MOS2 (see Eq. (2.7)), must be found.

The experimental setup allows independent variation of $V_{DS}$ and $V_{GS}$ on the curve tracer and to extract data points from the linear- (very low $V_{DS}$) and triode region up to $V_{DSAT}$.

A straight line can be interpolated through these data points by rearranging Eq. (2.7)

$$\log \left( \frac{\mu_S}{U_O} \right) = U_{EXP} \log \left( \frac{\varepsilon_S}{C_{ox}} U_{CRIT} \right) - \log \left( V_{GS} - V_{TH - UTRA} \times V_{DS} \right)$$ \hspace{1cm} (5.7)

where
\[
\sqrt{\frac{I_{DS}}{K_P}} = V_{GS} - V_{TH}
\]  

(5.1)

The threshold \( V_{TH} \) is taken as the intercept on the abscissa of the above linear regression through the coordinate pair \( (\sqrt{I_{DS}}, V_{GS}) \). Several \( V_{TH} \) are calculated; one for each \( V_{BS} \).

\[
V_{TH} = V_{TO} + \text{GAMMA}(\sqrt{V_{SB} + PHI} - \sqrt{PHI})
\]  

(5.2)

where \( PHI = 2\phi_F \). From another straight line interpolated in the plane \( (\sqrt{V_{SB} + PHI}, V_{TH}) \), the slope gives GAMMA and

\[
NSUB = \frac{\text{GAMMA}^2}{2q \varepsilon_{SI}} \left( \frac{\varepsilon_{OX}}{TOX} \right)^2
\]  

(5.3)

All the above extrapolations are performed by PROGRAM1 written in BASIC for the Tek 4051 the listing and operating instructions of which are contained in Appendix 1. The user has mainly to input only the \( (I_{DS}, V_{GS}) \) point pairs and the \( V_{BS} \) stepping and the program will display \( V_{TO}, \text{GAMMA} \) and \( \text{NSUB} \).

These measurements should be performed on a long and wide channel MOSFET since the above values will then be corrected by the program for small-size effects. For more accuracy the extraction program could perform one more iteration once the first estimate has been found for \( V_{TO} \) and \( \text{NSUB} \) and use the exact current equation as implemented in MOS2.

5.2. Capacitance Measurements

As has been already mentioned in Sec. 2 the junction capacitance is separated into a bottom and a sidewall capacitance

\[
C_{TOT} = A \left( \frac{C_J}{V_R} \right)_{\text{MOS}} \cdot P \left( \frac{C_{JSW}}{1 + \frac{V_R}{P_B}} \right)_{\text{MOS}}
\]  

(5.4)

where \( A \) represents the plane area (on layout), \( P \) the perimeter and \( V_R \) the reverse bias applied to the junction.

\( CJ \) can be found first by assuming that the sidewall capacitance of the large rectangular capacitor is negligible. From a C-V plot, one gets
\[
\frac{\mu_s}{U_0} = \frac{K_P_i}{K_P_0}
\]

(5.8)

with

- \(K_P_i\) - conduction factor for different \(V_{GS}\)
- \(K_P_0\) - maximum value of conduction factor

\(U_{EXP}\) and \(U_{CRIT}\) are obtained from the above linear regression as the slope and y intercept respectively by plotting \(\log(K_P_i/K_P_0)\) on the y- and \(\log(V_{GS} - V_{TH} - UTRA \times V_{DS})\) on the x axis.

The data processing is performed again by PROGRAM1 by specifying \((V_{DS}, V_{GS}, I_{DS})\) points where for different \(V_{GS}\) curves different maximum \(V_{DS}\) values are entered in order to cover each characteristic up to \(V_{DSAT}\). PROGRAM1 computes \(U_0\), \(U_{CRIT}\) and \(U_{EXP}\) for each \(V_{DS}\) range and at the end displays an average for each of the three values over the whole interval.

5.4. Approximation of \(V_{MAX}\)

A second program written in BASIC for the Tek 4051, PROGRAM2 (see Appendix 2) helps with its two options to evaluate \(V_{MAX}\). The first alternative is to plot \(V_{DSAT}\) as a function of the effective channel length \(L\) with \(V_{GS}\) as a parameter. For each \(V_{MAX}\), one gets a different set of curves. Fig. 5.1. shows such a sample plot.

The second option plots \(I_{DSAT}\) as a function of \(V_{MAX}\) with \(V_{GS}\) as a parameter. A different set of curves results for each \(L\). A sample plot for this option is shown in Fig. 5.2.

Starting from the measured characteristics one defines \(V_{DSAT}\) as the voltage starting from which the I-V curve can be approximated by a straight line and the current corresponding to this point is \(I_{DSAT}\). With these values one can get a good guess for \(V_{MAX}\) from plots similar to those in Fig. 5.1. and 5.2. It is emphasized that PROGRAM2 uses the same equations as those implemented in SPICE2.G for \(V_{DSAT}(V_{MAX})\).
FIG. 5.1.

FIG. 5.2.
6. SIMULATION EXAMPLE

It is the purpose of this example to show the ease with which a section of a CMOS LSI circuit is accurately simulated starting from the layout and using the new device card format and model input parameter. The circuit of Fig. 6.1 represents a short path of a MOS/LSI circuit. The output signal CS generated from CLK can be measured at an output pad and compared with the simulated waveform. The input deck for SPICE2.G is given in Appendix 3.

The measured circuit chips were located on the same wafer with the test patterns from which the parameter extraction has been performed. For an accurate simulation all the parasitics of the layout must be included; \( R_1 \) represents the series resistance of the input pad protection while \( R_2 \) and \( R_3 \) represent crossunder diffusions. Each C includes all the capacitive effects associated with that node, e.g., \( C_1 \) is contributed by Al-to-Field oxide, Poly to-field, N+ and P+ junctions and thin oxide, where for each the accurate overlap area must be evaluated. Each of the gates has been modeled as a subcircuit. A load capacitance of 100pF has been used; the rest is attributed to the probe and parasitics. Fig. 6.2 shows a sample simulated output of the waveforms.

An interesting result has been obtained by performing the simulation with and without sidewall capacitance and with and without scattering-limited drift-velocity effects (VMAX). The input file given in Appendix 3 is complete in the sense that it includes series resistance, sidewall capacitance and drift velocity saturation. The devices which have no perimeter specified had a negligible sidewall compared to the area.

The results of the different simulations and the measured values are summarized in Table I. It can be noticed that the above two effects contribute a 15 to 20% accuracy improvement and the simulated results of this circuit containing 22 MOSFETs is within 5 to 10% of the results for the actual circuit.
FIG. 6.2.

TU SYNC LSI IC CS CIRCUITRY

Temp = 27.0°C
<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MEASURED</th>
<th>SIMULATED</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>W/O Sidewall</td>
</tr>
<tr>
<td></td>
<td></td>
<td>W/O VMAX</td>
</tr>
<tr>
<td>Delay</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CL = 20pF</td>
<td>64 - 75</td>
<td>49</td>
</tr>
<tr>
<td>TD (NS)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CL = 120pF</td>
<td>90 - 105</td>
<td>70</td>
</tr>
<tr>
<td>Fall Time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CL = 20pF</td>
<td>32 - 36</td>
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</tr>
<tr>
<td>TF (NS)</td>
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<td></td>
</tr>
<tr>
<td>CL = 120pF</td>
<td>85 - 120</td>
<td>90</td>
</tr>
</tbody>
</table>
Appendix 1
User Instructions and Listing of PROGRAM1

Load the program from the tape cartridge (Tektronix 4051) by typing:

FILE n  CR
OLD  CR

VTO, GAMMA, and NSUB Interpolation

Calculator prompts:
TYPE OF LIN REGRESSION, DEVICE TYPE,
NO. OF POINT PAIRS, NO. OF CURVES

Answer

GAMMA  CR
N (or P)  CR
no. of \( (I_{DS},V_{GS}) \) pairs for each \( V_{TH} \).  CR
no. of different VSB values

Prompt:

PHI, TOX, VSB STEP

Enter appropriate signed values; although NSUB is not yet known specify guess for PHI \((2\phi_F)\).

Prompt:

\[ n, \text{ VSB} = \text{ value}, V_{GS} = , I_{DS}(UA) = \]

where \( n \) specifies the coordinate pair number, value the \( V_{SB} \) value and the user enters:

VGS value, IDS value in \( \mu A \)  CR

This is repeated as many times as necessary for entering all data as specified at the beginning; VGS must have the appropriate sign.

At conclusion the program will print:

VTO = value, GAMMA = value, NSUB = value
Capacitance Interpolation

Answer in response to the starting prompt (TYPE OF LIN REGRESSION, etc):

- CAPACITANCE
- N (or P) CR
- no. of \((V_R, C_R)\) point pairs, CR
- 1 CR

Prompt:

PB, CJ (PF/U~2), AREA (U~2), PERIMETER

where PB and CJ have the same meaning as in SPICE2 and AREA and PERIMETER refer to the meander form capacitor.

Enter the corresponding values separated by commas and CR after the last one.

At the conclusion the calculator will display:

- \(CJSW = \text{value}\), \(MJSW = \text{value}\)

The program assumes CJ known and interpolates for \(MJ=0.5\); it can be easily modified for a two step interpolation, first for CJ and MJ with the area of the rectangular capacitor, and then for CJSW and MJSW.

Mobility Interpolation

Answer in response to the starting prompt (TYPE OF LIN REGRESSION, etc):

- MOBILITY CR
- N (or P) CR
- no. of \((V_{GS}, J_{DS})\) point pairs, CR
- no. of different VDS ranges CR

The range of \(V_{GS}\) has the meaning that different \(V_{DS}\) values can be specified for each \(V_{GS} = \text{constant characteristic in order to cover each } V_{GS} \text{ curve up to the saturation point } V_{DSAT}. For the sample data shown in Table A.1 enter:

- MOBILITY CR
- P CR
- 4.4 CR

Prompt:

VTO, NSUB, TOX, UTRA, W, LEFF, VSB

The respective values are entered separated by commas and a CR after the last one.
LEFF is the layout channel length less the under-diffusions.

Prompt:

\[ n, \ VDS = , \ VGS = , \ IDS(UA) = \]

where \( n \) is the current number of data point set; at each such prompt one line from Table A.1 has to be input. After all data for one \( V_{DS} \) range have been input the corresponding \( UO, \ UCRIT, \) and \( UEXP \) are displayed:

\[ VDS = \ \text{value}, \ UO = \ \text{value}, \ UCRIT = \ \text{value}, \ UEXP = \ \text{value} \]

This operation is repeated until all the different \( V_{DS} \) ranges are entered. At the end the program will print an average value for the three mobility factors over all the data points. An example is shown in Fig. A1.
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<th>VGS</th>
<th>IDS (uA)</th>
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</thead>
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</tr>
<tr>
<td></td>
<td>-3.0</td>
<td>22.5</td>
</tr>
<tr>
<td></td>
<td>-3.5</td>
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<tr>
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</tr>
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</table>

**FIG. A.1.**
PROGRAM 1

10 INIT
20 LET G* = "GAMMA"
30 LET U* = "MOBILITY"
40 LET C$ = "CAPACITANCE"
50 PRINT "TYPE OF LINE REGRESSION, DEVIATION, Type of Curves"
60 PRINT "NO. OF POINT PAIRS, NO. OF CURVES"
70 LET U* = "MOBILITY"
80 LET C$ = "CAPACITANCE"
90 LET U* = "MOBILITY"
100 LET C$ = "GAMMA"
110 STOP
PROGRAM 1 (continued)

430 A0=T*(F2+V5)
440 PRINT N,"VDS=","VGS=","IDS(UA)="
450 INPUT V4(N),V6(N),Y0
460 A1=A0+T*V4(N)
470 A2=SQR(A0)+3
480 A3=SQR(A1)+3
490 B0=2/31*G5*(A3-A2)
500 I0=(V0+F2+V4(N)/2)*V4(N)
510 V2=V1+U3*V4(N)
520 I1=Y0*1.0E-6
530 D0=V6(N)*V4(N)-I0-B0
540 K1(N)=I1/D0
550 IF N=1 THEN 570
560 IF N>1 AND K1(N)<=K0 THEN 580
570 K0=K1(N)
580 IF N<N THEN 250
590 S1=0
600 S2=0
610 S3=0
620 S4=0
630 FOR J=1 TO M
640 K1(J)=LGT(K1(J)/K0)
650 V6(J)=LGT(T*(V6(J)-V1-U3*V4(N)))
660 S1=S1+V6(J)
670 S2=S2+V6(J)+12
680 S3=S3+K1(J)
690 S4=S4+V6(J)*K1(J)
700 NEXT J
710 U0(N1)=K0*T0/E0*L/W
720 N0=(S3*S2-S1*S4)/(N*S2-S1+2)
730 S0=(N*S4-S1*S3)/(N*S2-S1+2)
740 U2(N1)=-50
750 U1(N1)=10*(N0/S0)*3.9/T0*11.7
760 PRINT "VDS=";V4(N);" U0=";U0(N1);" UCRIT=";U1(N1);" UEXP=";U2(N1)
770 IF N1<N1 THEN 230
780 U6=0
790 U7=0
800 U8=0
810 FOR K=1 TO M1
820 U6=U6+U6(K)
830 U7=U7+U1(K)
840 U8=U8+U2(K)
850 NEXT K
860 U6=U6/M1
870 U7=U7/M1
880 U8=U8/M1
890 PRINT "*** AVERAGE OVER SPECIFIED INTERVAL ***"
900 PRINT "*** U0"=";U6,"UCRIT"=";U7,"UEXP=";U8
910 GO TO 1570
920 IF N>1 THEN 1060
930 IF H=1 AND N1>1 THEN 1000
940 PRINT "PHI<TOX(U),USB STEP"
950 INPUT F2,T0,D1
960 T0=T0*1.0E-4
980 U5=0
990 GO TO 1010
1000 U5=U5+D1
1010 S1=0
1020 S2=0
1030 S3=0
1040 S4=0
1050 B2<N1>=SQR<T*(U5+F2)
1060 PRINT N,"USB=";U5,"VGS=";U5,"IDS(UA)="
1070 INPUT X0,Y0
1080 Y2=SQR<Y0*1.0E-6>
1090 S1=S1+T*X0
1100 S2=S2+X0
1110 S3=S3+Y2
1120 S4=S4+T*X0*Y2
1130 IF N>M THEN 250
PROGRAM 1 (continued)

1140  D2=N*S2-S1^2
1150  NO=(S3*S2-S1*S4)/D2
1160  S0=(N*S4-S1*S3)/D2
1170  V9(N1)=-T*N0/S0
1180  IF N1<M1 THEN 230
1190  S1=0
1200  S2=0
1210  S3=0
1220  S4=0
1230  FOR J=1 TO M1
1240  S1=S1+B2(J)
1250  S2=S2+B2(J)^2
1260  S3=S3+T*U9(J)
1270  S4=S4+T*U9(J)*B2(J)
1280  NEXT J
1290  D2=N*S2-S1^2
1300  NO=(S3*S2-S1*S4)/D2
1310  G2=(N*S4-S1*S3)/D2
1320  N5=(3.9*G2/T0)^2*8.854E-14/3.744E-18
1330  PRINT "UT0=";U9(1),"GAMMA=";G2,"HSUB=";N5
1340  G0 TO 1570
1350  IF N>1 THEN 1420
1360  PRINT "PB,CA0<PF/UT2>,AREA(UT2),PERIMETER(U)"
1370  INPUT F3,C0,A0,P0
1380  S1=0
1390  S2=0
1400  S3=0
1410  S4=0
1420  PRINT N,"UR,CJ<PF>"
1430  INPUT U1,C1
1440  K=C1-A0*C0/SQR(1+U1/F3)
1450  X0=LGT(1+U1/F3)
1460  Y0=LGT(K)
1470  S1=S1+X0
1480  S2=S2+X0^2
1490  S3 = S3 + Y0
1500  S4 = S4 + X0 * Y0
1510  IF N < M THEN 240
1520  NO = (S3 * S2 - S1 * S4) / (N * S2 - S1^2)
1530  S0 = (N * S4 - S1 * S3) / (N * S2 - S1^2)
1540  C2 = 10 * (N0 - 6) / P0
1550  M0 = -S0
1560  PRINT "CPO(F/M) = \"; C2, "M = \"; M0
1570  END
Appendix 2
User Instructions and Listing of PROGRAM2

Use the same procedure as in Appendix 1 to load the program from the tape cartridge.
Prompt:

SELECT TYPE OF PLOT: ENTER 1 FOR VDSAT = F(L)
2 FOR IDSAT = F(VMAX)

Enter:
1 (or 2) CR

A first set of parameters is required next:

TYPE, VTO, NSUB, TOX(U), W(U), LEFF(U), VSB

Enter the required data as follows:

N (or P) CR
values CR

The values are input separated by commas and a CR at the end of the line.
Additional parameters are required next:

UO, UCRIT, UEXP, UTRA, VMAX (M/S)

These are input in the same dimensions as used in SPICE2.G.
The limits and step size of the variable (L or VMAX depending on which type of plot has been selected, 1 or 2 respectively) are requested next:

LOWER LEFF OR VMAX, UPPER LEFF OR VMAX, STEP,
LOWER [VGS], UPPER [VGS], [STEP]

After entering these last values plots of the type shown in Figs. 5.1. and 5.2. will be displayed on the screen.
initial
100 DIM Y0(3), Y1(24), A4(4), B4(4), P9(24)
110 PRINT "SELECT TYPE OF PLOT: ENTER 1 FOR UDSSAT=F(L)"
120 PRINT 
130 INPUT T6
140 PRINT "TYPE, VTO, HSUB, TOX(U), W(U), LEFF(U), USB"
150 INPUT T$, V8, N0, T0, W, L0, U5
160 T=1
170 IF T$="H" THEN 190
180 T=-1
190 L0=L0*1.0E-4
200 T0=T0*1.0E-4
210 W=W*1.0E-4
220 PRINT "U0, UCRIT, UEXP, UTRA, UMAX(M/S)"
230 INPUT U0, U1, U2, U3, U
240 PRINT "LOWER, LEFF OR UMAX, UPPER, LEFF OR UMAX, STEP"
250 INPUT W1, W2, W3
260 IF T6=1 THEN 290
270 W1=W1*1.0E-4
280 W2=W2*1.0E-4
285 W3=W3*1.0E-4
290 V=V*100
300 N=INT((W2-W1)/W3)+1
310 DIM X(N), Y(10, N)
320 PRINT "LOWER /VGS/, UPPER /VGS/, STEP"
330 INPUT W4, W5, W6
340 H1=1.45E+10
350 E0=3.45E-13
360 E2=1.04E-12
370 V0=0.926
380 Q=1.6E-19
390 F2=T*2*V0*LOG(N0/H1)
400 C0=E0/T0
410 Q0=SQR(2*Q*E2*N0*F2*T)
420 \( G0 = Q0 / (C0 \cdot SQR(T2 \cdot T)) \)
430 \( F0 = V8 - F2 - T \cdot G0 \cdot SQR(T \cdot F2) \)
440 \( G1 = Q0 / C0 \)
450 \( U7 = V8 + G0 \cdot (SQR(T \cdot (V5 + F2)) - SQR(T \cdot F2)) \)
460 \( I1 = 1 \)
470 FOR I = W4 TO W5 STEP W6
480 \( V6 = T \cdot I \)
490 \( U1 = T \cdot (V6 - F0 + U5) \)
500 \( U2 = T \cdot (V5 + F2) \)
510 \( A1 = 4 / 3 \cdot G0 \)
520 \( B0 = -2 \cdot U1 \)
530 \( D0 = -U2 + 2 - 4 / 3 \cdot G0 \cdot SQR(U2 \cdot 3) + 2 \cdot U1 \cdot U2 \)
540 \( U3 = V6 - F0 - F2 + T \cdot G0 \cdot T / 2 \cdot (1 - SQR(1 + T \cdot 4 / G0 \cdot T (V6 - F0))) \)
550 \( U = U2 \cdot LOG(U1 \cdot E2 / C0 / (T \cdot (V6 - V7 - U3 \cdot U3))) \)
560 \( U = U0 \cdot EXP(U) \)
570 IF U <= U0 THEN 590
580 \( U = U0 \)
590 \( J1 = 1 \)
600 FOR J = W1 TO W2 STEP W3
610 IF T6 = 2 THEN 660
620 \( L0 = J \cdot 1.0E-4 \)
630 IF I1 > 1 THEN 690
640 \( X(J1) = L0 \cdot 10000 \)
650 G0 TO 690
660 \( U = J \cdot 1000000 \)
670 IF I1 > 1 THEN 690
680 \( X(J1) = U \cdot 1.0E-6 \)
690 \( U9 = U \cdot L0 / U \)
700 \( C1 = -2 \cdot G0 \cdot U9 \)
710 \( B1 = B0 - 2 \cdot U9 \)
720 \( D1 = D0 + 2 \cdot U9 \cdot U1 \)
730 \( A = -B1 \)
740 \( B = A1 \cdot C1 - 4 \cdot D1 \)
750 \( C = -D1 \cdot (A1 \cdot T2 - 4 \cdot B1) - C1 \cdot T2 \)
760 \( R = -(A1 \cdot T2) / 3 + B \)
PROGRAM 2  (continued)

770  S=2*(A/3)^3-A*B/3+C
780  R3=R*R*R
790  S2=S*S
800  P=S2/4+R3/27
810  IF P>=0 THEN 900
820  P0=ABS(P)
830  R0=SQR(S2/4+P0)
840  P2=-SQR(P0)
850  F=ATN(2*P2/S)
860  R0=EXP(LOG(R0)/3)
870  Y0(1)=2*R0*COS(F/3)-A/3
880  N=3
890  GO TO 990
900  N=1
910  P2=SQR(P)
920  P3=-S/2+P2
930  P4=-S/2-P2
940  P5=SGN(P3)
950  P6=SGN(P4)
960  P3=P5*EXP(LOG(ABS(P3))/3)
970  P4=P6*EXP(LOG(ABS(P4))/3)
980  Y0(1)=P3+P4-A/3
990  M1=0
1000  K=1
1010  A3=A1^2/4-B1+Y0(K)
1020  B3=Y0(K)^2/4-D1
1030  A3=SQR(A3)
1040  B3=SQR(B3)
1050  FOR M=1 TO 4
1060  S1=INT((M-1)/2)
1070  A4(M)=A1/2+-1^M-1*A3
1080  B4(M)=Y0(K)/2+-1^S1*B3
1090  D4=A4(M)*A4(M)/4-B4(M)
1100  IF D4<0 THEN 1170
1110  M1=M1+1
1120 \text{Y1(M1)} = -A4(M)/2 + \text{SQR}(D4)
1130 \text{P9(M1)} = Y1(M1) + 4 + A1 \times Y1(M1) \times 3 + B1 \times Y1(M1) \times 2 + C1 \times Y1(M1) + D1
1140 \text{M1} = \text{M1} + 1
1150 \text{Y1(M1)} = -A4(M)/2 - \text{SQR}(D4)
1160 \text{P9(M1)} = Y1(M1) + 4 + A1 \times Y1(M1) \times 3 + B1 \times Y1(M1) \times 2 + C1 \times Y1(M1) + D1
1170 \text{NEXT M}
1180 \text{M2} = 0
1190 \text{FOR K = 1 TO M1}
1200 \text{IF ABS(P9(K) > 1.0E-5 THEN 1270}
1210 \text{IF Y1(K) < 0 THEN 1270}
1220 \text{M2 = M2 + 1}
1230 \text{IF M2 > 1 THEN 1250}
1240 \text{Y2 = Y1(K)}
1250 \text{IF Y2 < Y1(K) THEN 1270}
1260 \text{Y2 = Y1(K)}
1270 \text{NEXT K}
1280 \text{U4 = T \times Y2 \times Y2 - U5 - F2}
1290 \text{IF T6 = 2 THEN 1320}
1300 \text{Y(I1, J1) = T \times U4}
1310 \text{GO TO 1330}
1320 \text{Y(I1, J1) = W/L0 \times U \times C0 \times ((V6 - F0 - F2 - V4/2) \times V4 - 2/3 \times G0 \times (Y2 \times 3 - \text{SQR}(V2) \times 3))}
1330 \text{J1 = J1 + 1}
1340 \text{NEXT J}
1350 \text{I1 = I1 + 1}
1360 \text{NEXT I}
1370 \text{I1 = I1 - 1}
1380 \text{J1 = J1 - 1}
1390 \text{S3 = 5}
1400 \text{S0 = LGT(Y(I1, J1))}
1410 \text{S1 = INT(S0)}
1420 \text{IF S0 - S1 = LGT(7.5) THEN 1510}
1430 \text{IF S0 - S1 > LGT(5) THEN 1490}
1440 \text{IF S0 - S1 > LGT(2.5) THEN 1470}
1450 \text{S2 = 2.5}
1460 \text{GO TO 1530}
1470 S2=5
1480 GO TO 1530
1490 S2=7.5
1500 GO TO 1530
1510 S2=10
1520 S3=10
1530 S0=S2*10^S1
1540 DIM Y7(J1)
1550 PAGE
1560 GOSUB 1650
1570 FOR I=1 TO J1
1580 FOR J=1 TO J1
1590 Y7(J)=Y(I,J)
1600 NEXT J
1610 MOVE X(1),Y7(1)
1620 DRAW X,Y7
1630 NEXT I
1640 GO TO 2040
1650 REM *** DRAW AND LABEL AXES ***
1660 VIEWPORT 25,120,20,90
1670 A=X(1)
1680 B=X(J1)
1690 C=0
1700 D=S0
1710 T8=S2/4*10^S1
1720 T9=0.02*(B-A)
1730 WINDOW A-T9,B,C-T8,D
1740 T=T8
1750 MOVE A,0
1760 FOR I=1 TO J1
1770 DRAW A+(I-1)*(B-A)/(J1-1),0
1780 PRINT "HJJ";X(I)
1790 MOVE A+(I-1)*(B-A)/(J1-1),C-T
1800 DRAW A+(I-1)*(B-A)/(J1-1),C+T
1810 MOVE A+(I-1)*(B-A)/(J1-1),C
PROGRAM 2 (continued)

1820 NEXT I
1830 T=T9
1840 MOVE A,0
1850 FOR I=1 TO S3+1
1860 DRAW A,(I-1)*(D-C)/S3
1870 PRINT "HHHHH";S2/S3*(I-1)
1880 MOVE A+T,(I-1)*(D-C)/S3
1890 DRAW A+T,(I-1)*(D-C)/S3
1900 MOVE A,(I-1)*(D-C)/S3
1910 NEXT I
1920 MOVE A,C+2/3*S0
1930 IF T6=2 THEN 1960
1940 PRINT "HHHHHHHHHHHHHHHHHHHJJJJJJJJJJJJJJJJ"
1950 GO TO 1970
1960 PRINT "HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH"
1970 PRINT "JJ *101";S1
1980 MOVE A+1/3*(B-A),C
1990 IF T6=2 THEN 2020
2000 PRINT "JJJJJJ LEFF (U)"
2010 GO TO 2030
2020 PRINT "JJJJJJ VMAX *10^4 (M/S)"
2030 RETURN
2040 END
Appendix 3

Example circuit SPICE2.G Input

SECTION OF CMOS LSI CIRCUIT FOR SPICE2.G

.OPTIONS ABSTOL=1U ACCT VNTOL=100N NODE
• 2 IN NAND DEFINITION
.SUBCKT NAND 1 2 3 4 5
M1 3 1 6 5 N1 W=40U L=8U AD=800P AS=480P NRD=2 NRS=1
M2 6 2 5 5 N1 W=40U L=8U AD=280P AS=2080P NRD=1 NRS=6
M3 3 1 4 4 P1 W=20U L=8U AD=338P AS=1164P NRD=1 NRS=3
M4 3 2 4 4 P1 W=20U L=8U AD=338P AS=1164P NRD=2 NRS=8
.ENDS NAND
• INVERTERS 210 AND 211
.SUBCKT INV210 1 2 3 4
M5 2 1 4 4 N1 W=24U L=8U AD=828P AS=1024P NRD=40 NRS=17
M6 2 1 3 3 P1 W=24U L=8U AD=1432P AS=4040P NRD=5 NRS=18
.ENDS INV210
.SUBCKT INV211 1 2 3 4
M7 2 1 4 4 N1 W=8U L=8U AD=200P AS=5120P NRD=7 NRS=65
M8 2 1 3 3 P1 W=8U L=8U AD=160P AS=4040P NRD=3 NRS=8
.ENDS INV211
• 3 IN NOR GATE
.SUBCKT NOR 1 2 3 4 5 6
M10 4 1 6 6 N1 W=20U L=8U AD=1150P AS=5120P NRD=22 NRS=65
+ PD=125U PS=230U
M11 4 2 6 6 N1 W=20U L=8U AD=1150P AS=5120P NRD=22 NRS=65
+ PD=125U PS=230U
M12 4 3 6 6 N1 W=20U L=8U AD=1150P AS=5120P NRD=75 NRS=65
+ PD=125U PS=230U
M13 7 3 5 5 P1 W=60U L=8U AD=420P AS=980P NRD=.5 NRS=.1
M14 8 2 7 5 P1 W=60U L=8U AD=1020P AS=420P NRD=1 NRS=.5
M15 4 1 8 5 P1 W=60U L=8U AD=960P AS=1020P NRD=1 NRS=1
.ENDS NOR
• OUTPUT BUFFER
.SUBCKT OUTBUF 1 2 3 4 5 6 7 8
M20 4 8 6 6 N1 W=384U L=8U AD=4148P AS=8048P NRD=.5 NRS=.5
+ PD=445U PS=1510U OFF
M21 4 8 5 5 P1 W=824U L=8U AD=11560P AS=9360P NRD=.5 NRS=.5
+ PD=1190U PS=1650U
M22 8 7 6 6 N1 W=128U L=8U AD=1900P AS=8048P NRD=2 NRS=5
+ RSH=14 LEVEL=2
.MODEL N1 NMOS(TOX=0.125U NSUB=10E15 VTO=0.924 XJ=1.9U LD=1.5U
+ JS=1.24E-4 PB=0.89 UO=622 UCRIT=3.97E4 UEXP=0.08 UTRA=0.25
+ CGB=3E-10 CGD=4.35E-10 CGS=4.35E-10 CJSW=2F VMAX=5E4 NEFF=3
+ RSH=3 LEVEL=2)
.MODEL P2 PMOS(TOX=0.125U NSUB=3.2E15 VTO=-0.65 XJ=1.5U LD=1.125U
+ JS=7.75E-5 PB=0.86 UO=222 UCRIT=5.83E4 UEXP=0.15 UTRA=0.25
+ CGB=3E-10 CGD=3.26E-10 CGS=3.26E-10 CJSW=1F VMAX=5E4 NEFF=3
+ RSH=14 LEVEL=2)
.MODEL N2 NMOS(TOX=0.125U NSUB=10E15 VTO=0.924 XJ=1.9U LD=1.5U
+ JS=1.24E-4 PB=0.89 UO=814 UCRIT=6.2E4 UEXP=0.13 UTRA=0.25
+ CGB=3E-11 CGD=4.35E-10 CGS=4.35E-10 CJSW=2F VMAX=5E4 NEFF=3
+ RSH=3 LEVEL=2)
.END
REFERENCES


1979


