SPICE2 MESFET MODEL DESCRIPTION

by

C. D. Hartgring

Memorandum No. UCB/ERL M79/1

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ABSTRACT

A model for Schottky Barrier Field Effect Transistors with micrometer and submicrometer dimensions has been implemented in the integrated circuit simulation program SPICE2. This report gives a description of the model.

ACKNOWLEDGEMENTS

The help of A. Vladimirescu, E. Cohen, and L. Jensen in implementing the model in SPICE2 is gratefully acknowledged. The discussions with my research adviser, Professor W. G. Oldham and with my colleagues, T. Chiu and M. Furukawa, have facilitated the progress of my research.

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TABLE OF CONTENTS

1. INTRODUCTION

The characteristics of Schottky Barrier Field Effect Transistors (MESFET) with micrometer and submicrometer dimensions are extensively discussed by Lyon-Caen et al. [1]. In this reference a model for the MESFET for integrated circuit simulation is presented. This model has been slightly modified and has been implemented in the integrated circuit simulation program SPICE2 (see Refs.[2] and [3]).

This report gives a description of the model topology (Section 2), the model parameters (Section 3), the physical basis for the mathematical formulation (Section 4), and examples clarifying model use (Section 5).

A summary of the equations used in the model is given in Appendix A, and a listing of the modifying deck that has been used to implement the model in SPICE2, version 2E2, is given in Appendix B.

2. MODEL TOPOLOGY

The MESFET model has not been implemented as a separate device model and must be defined as a subcircuit in SPICE2. In the subcircuit a modified MOSFET model is used to calculate the drain-to-source current and several capacitances according to the equations given in this report.

The MOSFET model has been modified by adding two extra levels (LEVEL=-1, and -2). The use of the different levels is explained in Section 3. The "negative level" MOSFET models have the same topology as the "positive level" MOSFET models (Fig.2.1), but different equations are used to calculate IDS, CGS, CGD, CSB, and CDB. The meaning of the input parameters also differs in both models, e.g. NFS is the "fast surface state density" in the "positive level" MOSFET model as opposed to being the "effective channel doping" in the "negative level" MOSFET model. Differences in meanings of the input parameters are discussed in Section 3.

The "negative level" MOSFET model can be used in a subcircuit that also contains resistances (representing the series-resistances) and two Schottky diodes (representing the gate-channel diode). This subcircuit then describes the behavior of the MESFET completely.

The topology of the subcircuit is given in Fig.2.2.

No series-resistances should be specified in the "negative level" MOSFET model and the DIODE model as these resistances are added in the subcircuit. Neither should a capacitance be specified in the DIODE model as it is already included in the "negative level" MOSFET model.

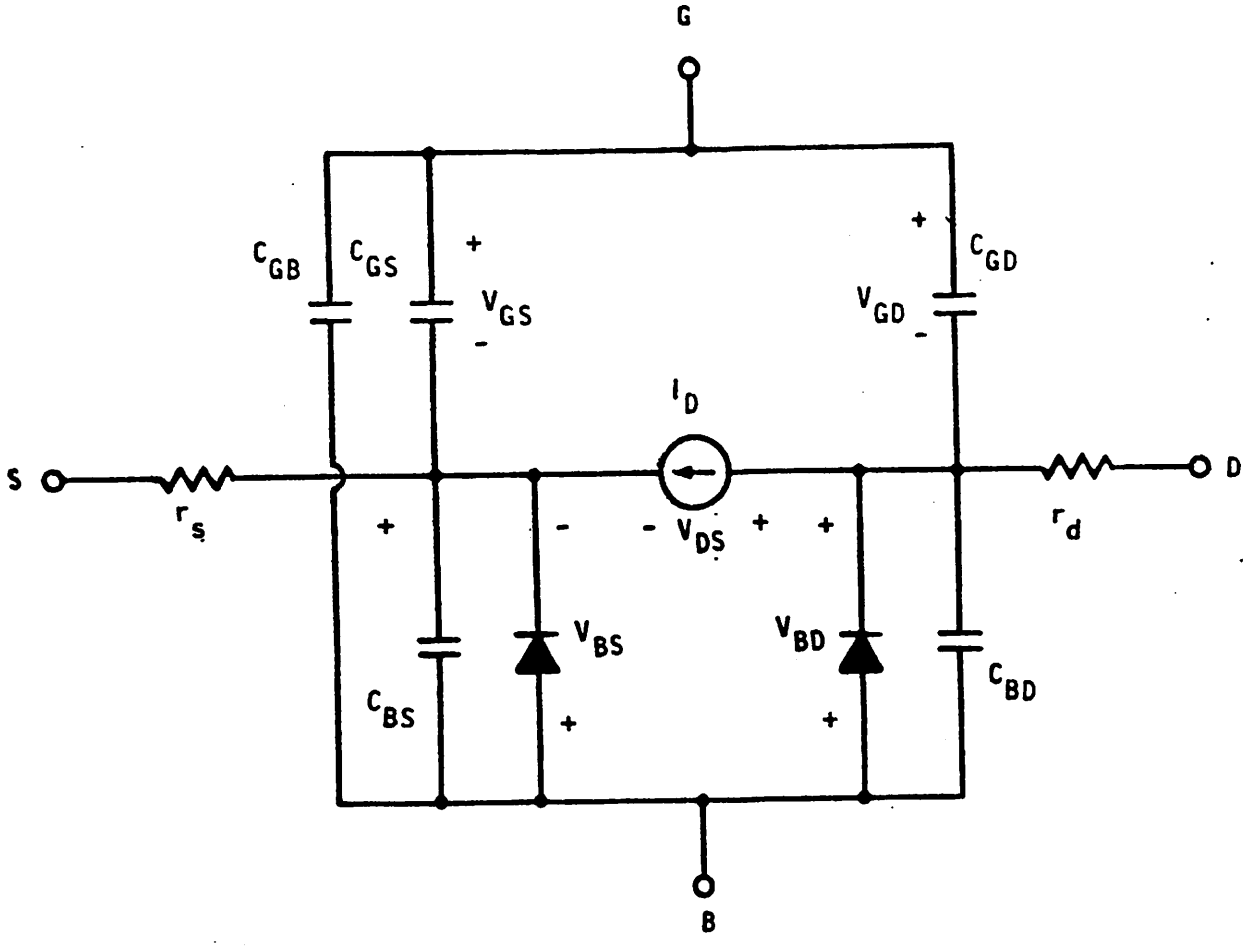

Figure 2.1: SPICE2 MOSFET model.

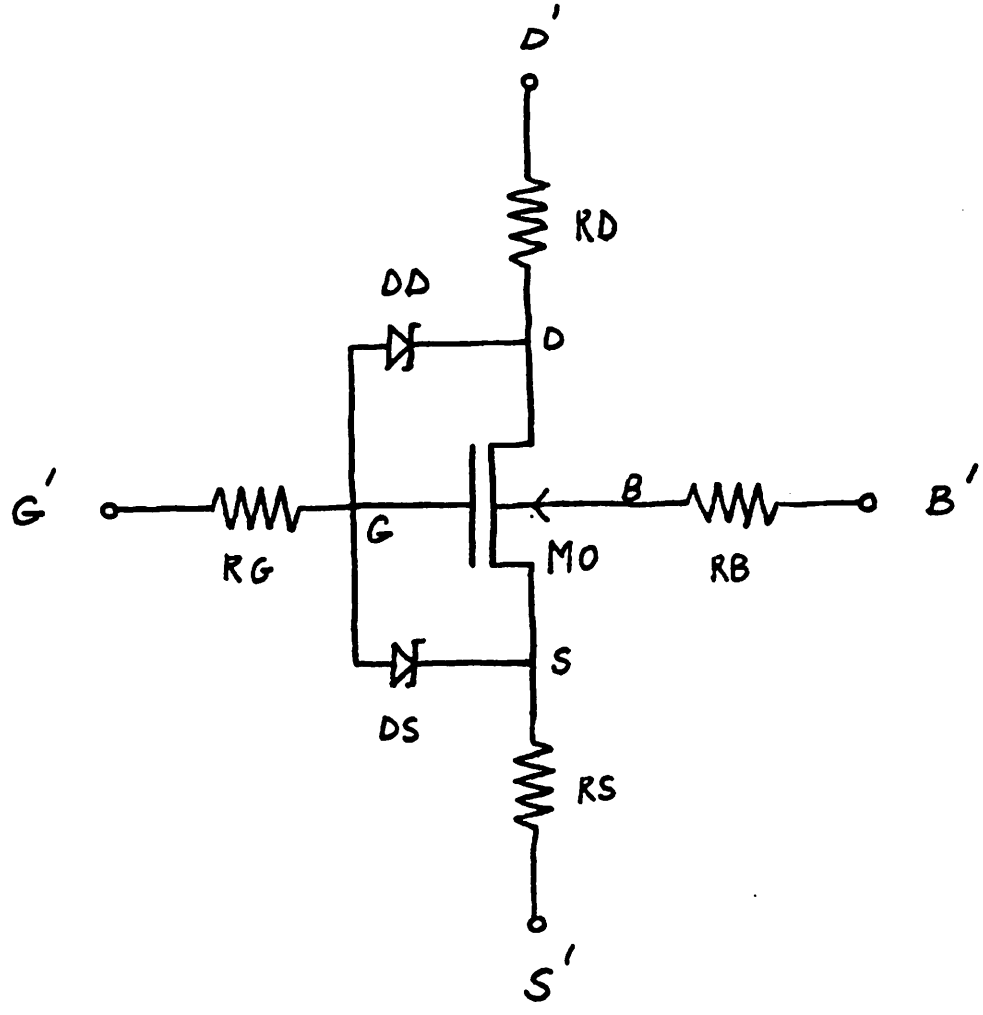

Figure 2.2: Topology of the subcircuit used to simulate a MESFET.

MO is the modified MOSFET model.
RG is the gate series-resistance.
RD is the drain series-resistance.
RB is the bulk series-resistance.
RS is the source series-resistance.
DD and DS are Schottky diodes representing the gate-channel diode.

3. MODEL PARAMETER DEFINITIONS

In the derivation of several equations a constant impurity concentration was assumed. However, as the channel is formed by ion implantation and diffusion, this is not a correct assumption. Therefore effective values for TOX, NFS, and UO have to be used as model parameters in order to match the experimental characteristics to the simulated ones.

A total of 24 parameters can be specified in the "negative level" MOSFET model. If a parameter is not specified the default value will be used. Table 3.1 provides a listing of the parameters of the "negative level" MOSFET model, a description of them, and their default values.

As previously noted, some parameters in this model have a meaning different to that in the "positive level" MOSFET model. In order to avoid confusion these parameters are marked with an asterix (*) in table 3.1. The following paragraphs briefly discuss each line entry in the table and refer to the appropriate section of Chapter 4 where further information is given on the impact of the parameters on model characteristics.

TABLE 2.1: "NEGATIVE LEVEL" MOSFET PARAMETER'S

PARAMETER		DESCRIPTION	UNITS	DEFAULT VALUE
LEVEL		Determines which MOSFET model is to be used by SPICE.		-1
TOX	*	Effective channel thickness	m	1.4E-7
NFS	*	Effective impurity concentration in the channel	cm^{-3}	4.0E16
UO		Effective mobility in the channel	cm^2/Vs	650
PHI	*	Built-in voltage of the Schottky gate-channel diode.	V	0.6
KP	*	Parameter used to model capacitive feedback from the drain in the channel	A/V^2m	4
NSS	*		V	-0.05
UCRIT	*	Parameters used to model the space-charge limited currents in the substrate	A/Vm	0.2
XJ	*		A/V^2m	0.0
LD	*		-	13.0
UEXP	*	Threshold voltages for the space-charge limited currents in the substrate	V	0.35
UTRA	*		V	-0.05
LAMBDA	*	Parameter used in the models for the gate-source and gate-drain capacitances	-	0.54
VTO	*	Parameter used in the empirical model for the gate-source and gate-drain capacitances	-	1.8
GAMMA	*	Parameter used to model the substrate-bias effect	$V^{-\frac{1}{2}}$	0.07

TABLE 2.1: "NEGATIVE LEVEL" MOSFET PARAMETERS (CONTINUED)

PARAMETER	DESCRIPTION	UNITS	DEFAULT VALUE
KF *	Temperature coefficient of PHI	V/°C	-1.6E-3
PB	Bulk junction potential	V	0.6
CGS	Gate-source overlap capacitance per unit gate width	F/m	1.5E-10
CGD	Gate-drain overlap capacitance per unit gate width	F/m	1.5E-10
CGB	Gate-bulk overlap capacitance per unit gate length	F/m	1.5E-10
CBS *	Zero-bias substrate-channel junction capacitance per unit area	F/m^2	3.0E-5
CBD	Zero-bias substrate-drain and substrate-source junction capacitance per unit area	F/m^2	3.0E-5
JS	Bulk junction reverse saturation current per unit junction area	A/m^2	1.0E-4
FC	Forward-bias non-ideal junction capacitance coefficient	-	0.5

* These parameters are defined differently in the "negative level" and the "positive level" MOSFET model.

A. LEVEL- Determines which MOSFET Model is to be used by SPICE2.

A LEVEL=-1, and -2 should be specified to gain access to the "negative level" MOSFET model. The different levels determine which equations for the gate-source and gate-drain capacitances will be used by SPICE2. Level=-1 should be specified if the empirical model (Eqs.(4.13-4.14)) is to be used and level=-2, should be specified if the theoretical model (Eqs.(4.12-4.13)) is to be used.
The gate-source and gate-drain capacitances are extensively discussed in Section 4E.

B. TOX- Effective Channel Thickness.

The effective channel thickness, TOX, determines the gate-source gate-drain capacitances (see Section 4E), the pinch-off voltage, Vp, given by Eq.(3.1), and the Shockley component, IDSS, of the source-to-drain current given by Eq.(3.2).

$$Vp = \frac{q*NFS*TOX^2}{2*eps} \tag{3.1}$$

where q is the elementary charge and eps is the dielectric constant of silicon.

$$IDSS = 2*\frac{eps}{TOX}*UO*Vp^2*\frac{W}{L}*\left\{Fd-Fs-\frac{2}{3}*(Fd^{3/2}-Fs^{3/2})\right\} \tag{3.2}$$

where W is the channel width, L is the channel length, and Fs and Fd are given by

$$Fs = \begin{cases} 0 & \text{for } Vp < VGS \\ \dfrac{PHI-VGS}{Vp} & \text{for } Vt < VGS < Vp \\ 1 & \text{for } VGS < Vt \end{cases} \qquad (3.3)$$

and

$$Fd = \begin{cases} 0 & \text{for } Vp < VGD \\ \dfrac{PHI-VGD}{Vp} & \text{for } Vt < VGD < Vp \\ 1 & \text{for } VGD < Vt \end{cases} \qquad (3.4)$$

where Vt is the threshold voltage. For VGS < Vt the device is in the cut-off region and IDSS=0. The threshold voltage is given by

$$Vt = PHI-Vp \qquad (3.5)$$

TOX can be determined by a measurement of the gate-source capacitance as a function of VDS. The reader is referred to Section 4E. The dependence of TOX on the substrate bias is discussed in Section 4C.

C. NFS- Effective Impurity Concentration in the Channel.

The effective impurity concentration in the channel, NFS, should be determined from the pinch-off voltage, Vp (Eq.(3.1)), which in turn can be obtained from the threshold voltage Vt (Eq.(3.5)).

D. UO- Effective Mobility in the Channel.

The effective mobility, UO, influences the Shockley component, IDSS, of the drain-to-source current. This parameter should be determined from IDSS as described below.

If the device is in the saturation region (VGD < Vt), IDSS can be approximated by

$$IDSS = .5*\frac{eps}{TOX}*UO*\frac{W}{L}*(VGS-Vt)^2 \qquad (3.6)$$

Plotting of IDSS versus $(VGS-Vt)^2$ will give UO. In order to find IDSS from the IV characteristics the IDS-VDS curves in the saturation region should be extrapolated to VDS=0. This is illustrated by Fig. 3.1.

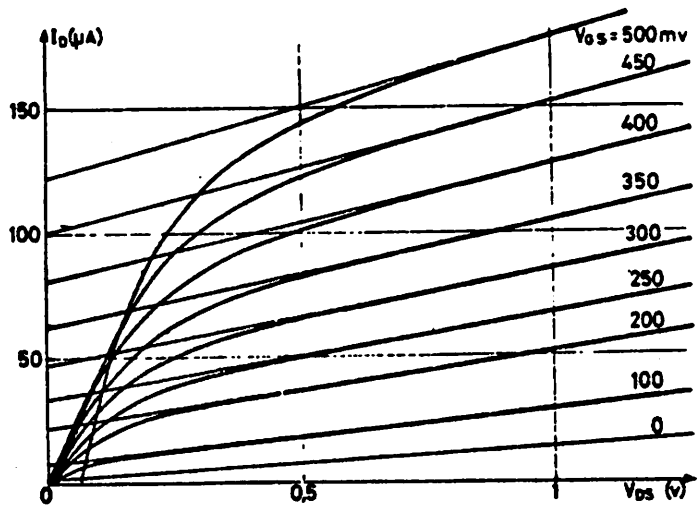

Figure 3.1: The value of IDSS in the saturation region is found by extrapolation of the IV characteristics.

E. PHI- Built-in Voltage of the Schottky Gate-channel diode.

PHI is the built-in voltage of the gate-channel diode and is given by

$$PHI = EG - \frac{kT}{q} \ln\left(\frac{NFS}{ni}\right) \tag{3.7}$$

where EG is the barrier-height in volts, kT/q is the thermal voltage, and ni is the intrinsic carrier concentration.

F. KP and NSS- Parameters Used to Model Capacitive Feedback from Source to Drain.

KP influences the drain-to-source current, IDS, and is used to model the capacitive feedback from the drain to the channel. This capacitive feedback is discussed in Section 4C and therefore only the equations that are used in the model to describe this effect are given here. The component of IDS that is due to the feedback is called IDSC.

$$IDSC = \begin{cases} W*KP*(VGS-Vt-NSS)*VDS & \text{for } 2NSS < VGS-Vt \text{ and } 0 < NSS \\ W*KP*(VGS-Vt)*VDS & \text{for } 0 < VGS-Vt \text{ and } NSS < 0 \end{cases} \tag{3.8}$$

G. UCRIT,XJ, and LD- Parameters Used to Model the Space-charge Limited Currents in the Substrate.

These parameters are used to model the space-charge limited currents in the substrate. These currents are discussed in Section 4B, and therefore only the equations used in the model to simulate this effect are given here. IDSR and IDSL are the components of IDS that are due to the space-charge limited currents in the substrate.

$$IDSR = W*UCRIT*VDS \quad \text{for } 0 < VGS-Vt \tag{3.9}$$

$$IDSL = W*XJ*\left(VDS+LD*(VGS-Vt-UTRA)\right)^2 \quad \text{for } VGS-Vt < UTRA \tag{3.10}$$

H. UEXP, and UTRA- Threshold Voltages for the Space-charge Limited Currents in the Substrate.

The physical meaning of UEXP and UTRA is as follows:
for VGS-Vt > UEXP, IDS is proportional to VDS for constant VGS;
for VGS-Vt < UTRA, IDS is proportional to VDS^2 for constant VGS.

I. LAMBDA and VTO- Parameters Used to Model the Gate-source and Gate-drain Capacitance.

LAMBDA influences both the theoretical and the empirical equations for the capacitances. Both the gate-source and gate-drain capacitances are proportional to LAMBDA.

VTO influences only the empirical equation for these capacitances. A detailed description of the modeling of the gate-drain and gate-source capacitances is given in Section 4E.

J. GAMMA- Parameter Used to Model the Substrate-Bias Effect.

Part of the depletion layer of the channel-substrate junction extends into the channel and reduces the effective channel-thickness TOX. The width of the depletion layer depends on the applied voltage and this makes TOX dependent on the channel-substrate voltage. The substrate-bias effect is modeled by

$$TOX(VBS) = TOX*(1-GAMMA*\sqrt{PB-VBS}) \qquad (3.11)$$

where VBS is the substrate-source voltage, and TOX(VBS) is the effective channel thickness. In order not to encumber the notation TOX is written for TOX(VBS) throughout this report.
A detailed description of the substrate-bias effect is to be found in Section 4C.

K. KF- Temperature Coefficient of PHI.

The temperature dependence of PHI is modeled as follows.

$$PHI(T) = PHI + KF*(T-300) \qquad (3.13)$$

where PHI(T) is the value of PHI at temperature T.
In order not to encumber the notation PHI is written for PHI(T) throughout this report.

L. PB- Bulk Junction Potential

This parameter represents the PN junction built-in voltage of the source-substrate and drain-substrate junctions. It is used in the equations for the total drain-substrate and source-substrate capacitances and in the equation that is used to model the substrate-bias effect.

M. CGS and CGD- Source and Drain Overlap Capacitances.

CGS and CGD represent the overlap capacitance per unit gate width. SPICE2 multiplies these values by the gate width and adds to them a variable percentage of the gate-channel capacitance. This percentage depends on the operating region of the transistor. A more complete explanation of the capacitance calculation procedure is contained in Section 4D.

N. CGB- Gate-substrate Overlap Capacitance

CGB represents the overlap capacitance per unit gate length. SPICE2 multiplies this capacitance by the gate length to obtain the total gate-substrate capacitance. The small voltage-dependent term that appears if the transistor enters the cut-off region has been neglected.

O. CBS- Zero-bias Substrate-channel Junction Capacitance.

CBS represents the zero-bias substrate-channel junction capacitance per unit gate area. SPICE2 multiplies this value by the gate area. A variable part of the zero-bias substrate-channel capacitance is added to the zero-bias source-substrate and drain-substrate capacitances (Eq.(3.14)), and is used in the junction capacitance equations (Eq.(3.13)).
A detailed description of this component is given in Section 4D.

P. CBD- Zero-Bias Substrate-Source and Substrate-Drain Junction Capacitance.

CBD represents the zero-bias substrate-source and substrate-drain junction capacitances per unit junction area. SPICE2 multiplies these values by the source or drain area as appropriate. CBD is used with the parameters PB and FC in the voltage variable junction capacitance equations indicated below.

$$CSBj = \frac{CSB0}{\sqrt{1-VBS/PB}} \qquad \text{for } VBS < FC*PB$$

$$CSBj = \frac{CSB0*}{(1-FC)^{1.5}}\left\{(1-1.5*FC)+0.5*VBS/PB\right\} \qquad \text{for } VBS < FC*PB \tag{3.13}$$

where CSB0 is given by

$$CSB0 = alpha*CBS*AG + CBD*AS \tag{3.14}$$

where CBSj is the junction capacitance, AS is the source junction area, AC is the gate area, CBS is the zero-bias substrate-channel capacitance and alpha is a variable which depends on the operating region of the transistor (see section 4E). Similar equations apply to the drain-substrate junction.

Q. JS- Bulk Junction Reverse Saturation Current.

This parameter represents the coefficient of the diode equation which simulates the IV characteristics of the drain-substrate and source-substrate diodes. SPICE2 multiplies JS by the appropriate drain or source junction area. The diode equation used in the model is given below.

$$IBS = JS*\left\{\exp(VBS/VT)-1\right\} \qquad (3.16)$$

where VT=kT/q is the thermal voltage, and IBS is the current through the source-substrate junction.

R. FC- Forward Bias Non-Ideal Junction Capacitance Coefficient.

This parameter, along with PB, determines the transition between the use of the reverse bias junction capacitance equation and the forward bias diffusion capacitance. The appropriate equations are given in Section N of this chapter.

4. IMPLEMENTATION OF FIRST AND SECOND ORDER EFFECTS IN THE MESFET MODEL

This chapter describes the implementation of the first and second order effects in the model and provides a physical basis for the mathematical formulation of these effects. The description is divided into discussions of (A) space-charge limited currents, (B) capacitive feedback from drain to the channel, (C) substrate bias effects, (D) variable capacitance effects, and (E) temperature effects.

A. Space-charge Limited Currents in the Substrate

Reiser [4] has shown, by means of a two-dimensional computer simulation of the MESFET, that the space-charge limited currents in a MESFET operating in the saturation region are proportional to VDS. In the MESFET model implemented in SPICE2 the distinction between saturation region and triode region has not been made for this case. The component IDSR of IDS, due to the effect described above, is modelled by (after Ref.[1])

$$IDSR = \begin{cases} UCRIT*VDS & \text{for} \quad 0 < VGS-Vt \\ UCRIT*\left(\frac{VGS-Vt-NSS}{-NSS}\right)*VDS & \text{for} \quad NSS < VGS-Vt < 0 \\ 0 & \text{for} \quad VGS-Vt < NSS \end{cases} \tag{4.1}$$

In the range VGS-Vt < 0, the equation serves to assure continuity of IDSR. The component IDSR is neglected if NSS > 0.

For small values of VGS, there are also space-charge limited currents in the substrate and they show a VDS^2 dependence, as stated by the Mott and Gurney law [5] which is given by

$$J = \frac{9}{8}\, mu*eps*VDS\ /L \tag{4.2}$$

where eps is the dielectric constant of silicon and mu is the mobility in the substrate. This equation is valid for an intrinsic substrate and is derived for a one-dimensional structure. De Chambost [6] has investigated the space-charge limited currents in two-dimensional structures as well as those with extrinsic substrates. Substrate doping and bias appeared to be important parameters in suppressing the currents. The space-charge limited currents also depend on VGS, as is shown by Lyon-Caen et al. [1]. In this reference an equation is given for modeling these currents. The equation is used in the model that is implemented in SPICE2 and is given below. IDSL is the component of IDS due to this effect.

$$IDSL = \begin{cases} W*XJ*\left\{VDS-LD*(UTRA-(VGS-Vt))\right\}^2 & \text{for} \quad VGS-Vt < UTRA \\ 3*W*XJ*VDS^2*\left\{\left(\frac{UEXP-(VGS-Vt)}{UEXP-UTRA}\right) - \frac{2}{3}\left(\frac{UEXP-(VGS-Vt)}{UEXP-UTRA}\right)^{3/2}\right\} & \text{for} \\ & UTRA < VGS-Vt < UEXP \\ 0 & \text{for} \quad UEXP < VGS-Vt \end{cases} \tag{4.3}$$

The parameters UCRIT, XJ, LD, NSS, UTRA, and UEXP are weak functions of VBS. These are not implemented in the model.

B. Capacitive Feedback from Drain to Channel

The output conductance, g, of a MESFET operating in the saturation region due to the capacitive coupling of the drain with the channel is given by (see Ref.[7])

$$g = KP*(VGS-Vt) \tag{4.4}$$

KP is proportional to UO and to the inverse of L^2. In the model no distinction is made between the saturation region and the triode region for this case, and the equation that is used to model this effect is given below. IDSC is the component of IDS that is due to the capacitive coupling.

$$IDSC = \begin{cases} W*KP*(VGS-Vt)*VDS & \text{for} \quad Vt < VGS \\ 0 & \text{for} \quad VGS < Vt \end{cases} \tag{4.5}$$

It was found that for low values of VDS the output conductance of some devices could be better modeled by the following empirical equation :

$$g = KP*(VGS-Vt-NSS) \tag{4.6}$$

where NSS > 0. A constant output conductance due to space-charge limited currents, as described in Section 4A, is not found in these devices (in fact a negative constant output conductance, UCRIT, are found if Eq.(4.1) and Eq.(4.5) is used in the calculation).

Specifying a value of NSS that is not negative will result in the use of the empirical equation which is implemented by

$$IDSR = \begin{cases} W*KP*(VGS-Vt-NSS)*VDS & \text{for} \quad 2NSS < VGS-Vt \\ 0.25*W*KP*(VGS-Vt)^2*VDS/NSS & \text{for} \quad 0 < VGS-Vt < 2NSS \\ 0 & \text{for} \quad VGS-Vt < 0 \end{cases} \tag{4.7}$$

where IDSR is the component of IDS that arises from the output conductance for low values of VDS (IDSCR=IDSC+IDSR).

C. Substrate Bias Effects

Part of the channel-substrate depletion layer extends into the channel and decreases the effective channel thickness. This part is proportional to the square root of PB-VBS. Therefore the substrate bias effect is modeled by the following equation.

$$TOX = TOX*(1- GAMMA* \sqrt{PB-VBS}\ ) \tag{4.8}$$

SPICE2 changes TOX according to the above equation and therefore the value of TOX that is used as an input parameter for the model may not already include this effect.
The substrate bias also influences the parameters UCRIT, XJ, LD, NSS, and UEXP, but this effect is not implemented in the model.

D. Variable Capacitance Effects

The gate-source, gate-drain, substrate-source, and substrate-drain capacitances are dependent on the operating region of the transistor. The variable part, CGS', of the gate-source capacitance and the variable part, CGD', of the gate-drain capacitance, will be discussed first. Subsequently, the variable part, CSB', of the substrate-source capacitance and the variable part, CDB', of the substrate-drain capacitance are discussed.

1. Gate-source and gate-drain capacitances

Assuming a constant impurity concentration in the channel and by using the abrupt depletion approximation and the gradual channel approximation, equations for CGS' and CGD' can be derived.

$$CGS' = 3*\frac{eps}{TOX}*\left[\frac{(1-Fs^{1/2})*(-3*Fd-Fs+4*Fd^{1/2}+2*Fs^{1/2}-2*Fd^{1/2}*Fs^{1/2})}{\{3*(Fs^{1/2}+Fd^{1/2})-2*(Fs+Fd+Fs^{1/2}*Fd^{1/2})\}^2}\right] \quad (4.9)$$

$$CGD' = 3*\frac{eps}{TOX}*\left[\frac{(1-Fd^{1/2})*(-3*Fs-Fd+4*Fs^{1/2}+2*Fd^{1/2}-2*Fs^{1/2}*Fd^{1/2})}{\{3*(Fd^{1/2}+Fs^{1/2})-2*(Fd+Fs+Fd^{1/2}*Fs^{1/2})\}^2}\right] \quad (4.10)$$

where Fs and Fd are given by Eqs.(3.3-3.4).
Reasonable approximations of these complicated equations are as follows:

i. CGS' is independent of VDS. (This is completely true for VGD < Vt.)

ii. CGD' is a linear function of Fd that is given by

$$CGD' = \begin{cases} CGS' & \text{for } Fd = Fs \\ 0 & \text{for } Fd = 0 \end{cases} \qquad (4.11)$$

Equations(4.9-4.10) then take the forms

$$CGS' = 3*\frac{eps}{TOX}* \frac{(1+Fs^{1/2})}{(1+2*Fs^{1/2})^2} \qquad (4.12)$$

$$CGD' = CGS'* \left(\frac{1-Fd}{1-Fs}\right) \qquad (4.13)$$

Equation(4.12) is plotted in Fig.4.1 (curve 1). A measured curve is also shown in this figure (curve 2, from Ref.[1]).

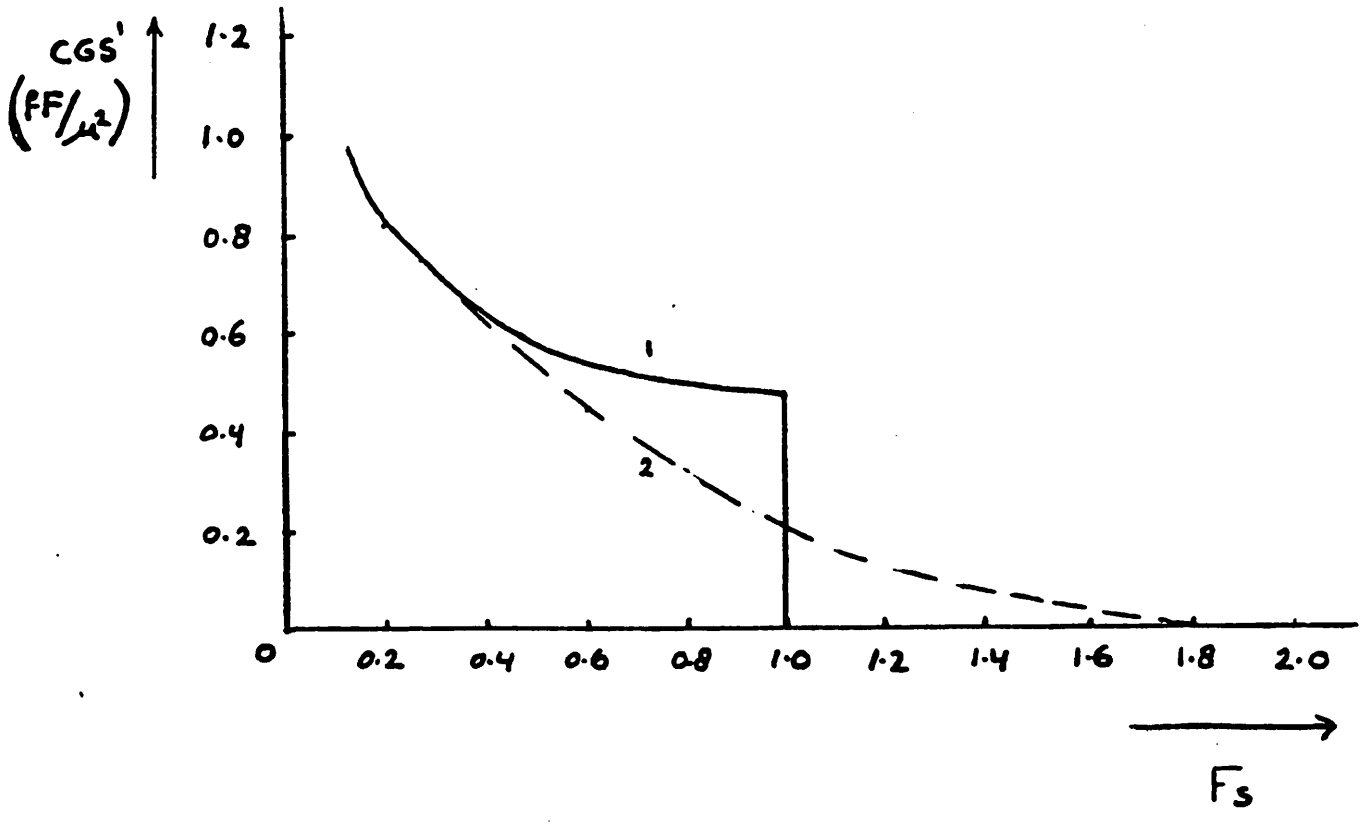

Figure 4.1: CGS' as a function of Fs. 1: Calculated. 2: Measured. (After Ref.[1])

From this figure it can be concluded that the capacitance does not abruptly change to zero at Fs=0. The depletion approximation does not seem to be valid in this case.
The measured curve can be suitable matched by an equation of the form

$$CGS' = LAMBDA*\frac{eps}{TOX}*(VTO-Fs)^2 \qquad (4.14)$$

where LAMBDA=0.54 and VTO=1.8. In this case Fs is permitted to have a value larger than one.
The empirical model for the gate-source capacitance uses Eq.(4.14), while the theoretical model uses Eq.(4.12) in which LAMBDA is substituted for the factor 3. The total gate-source and gate-drain capacitances are given by the sum of the overlap capacitance and the variable part.

2. Substrate-source and substrate-drain capacitances

The channel-substrate junction capacitance, CBC, can be written as

$$CBC = \frac{0.7*CBS*W*L}{\sqrt{1-VBS/PB}} \qquad (4.15)$$

If the device is in the saturation region, this capacitance can be modeled by a gate-source capacitance of $\frac{2}{3}$ CBC.
In the model no distinction between saturation and triode regions has been made. The equation for CSB' due to this effect is then as follows.

Empirical model:

$$CSB' = \frac{2}{3}\ CBC \qquad \text{for all VGS} \qquad (4.16)$$

Theoretical model:

$$CSB' = \begin{cases} \frac{2}{3}\ CBC & \text{for } Vt < VGS \\ 0 & \text{for } VGS < Vt \end{cases} \qquad (4.17)$$

In both models, CBD' is modeled in the same way as CGD', and is given by

$$CDB' = \frac{2}{3}\ CSB' * \left(\frac{1-Fd}{1-Fs}\right) \qquad (4.18)$$

The total substrate-source or substrate-drain capacitance is the sum of the substrate-source or substrate-drain junction capacitance and part of the substrate-channel capacitance.

E. Temperature Effects

1. DIODE model

No changes have been made. The temperature dependence can be simulated in the usual manner by specifying PT and EG (see Ref.[8]).

2. Negative level MOSFET model

The temperature dependence of the parameters is as follows.

$$PHI(T) = PHI + KF*(T-300) \qquad (4.19)$$

$$UO(T) = UO * 300/T$$

In order not to encumber the notation, PHI and UO are written for PHI(T) and UO(T) throughout this report.

JS PB CBD CBS	No changes have been made in the temperature dependence of these parameters. For their temperature dependence the reader is referred to Ref.[8].

5. EXAMPLES

As an example of the use of the model, the circuit shown in Fig.5.1 has been simulated.

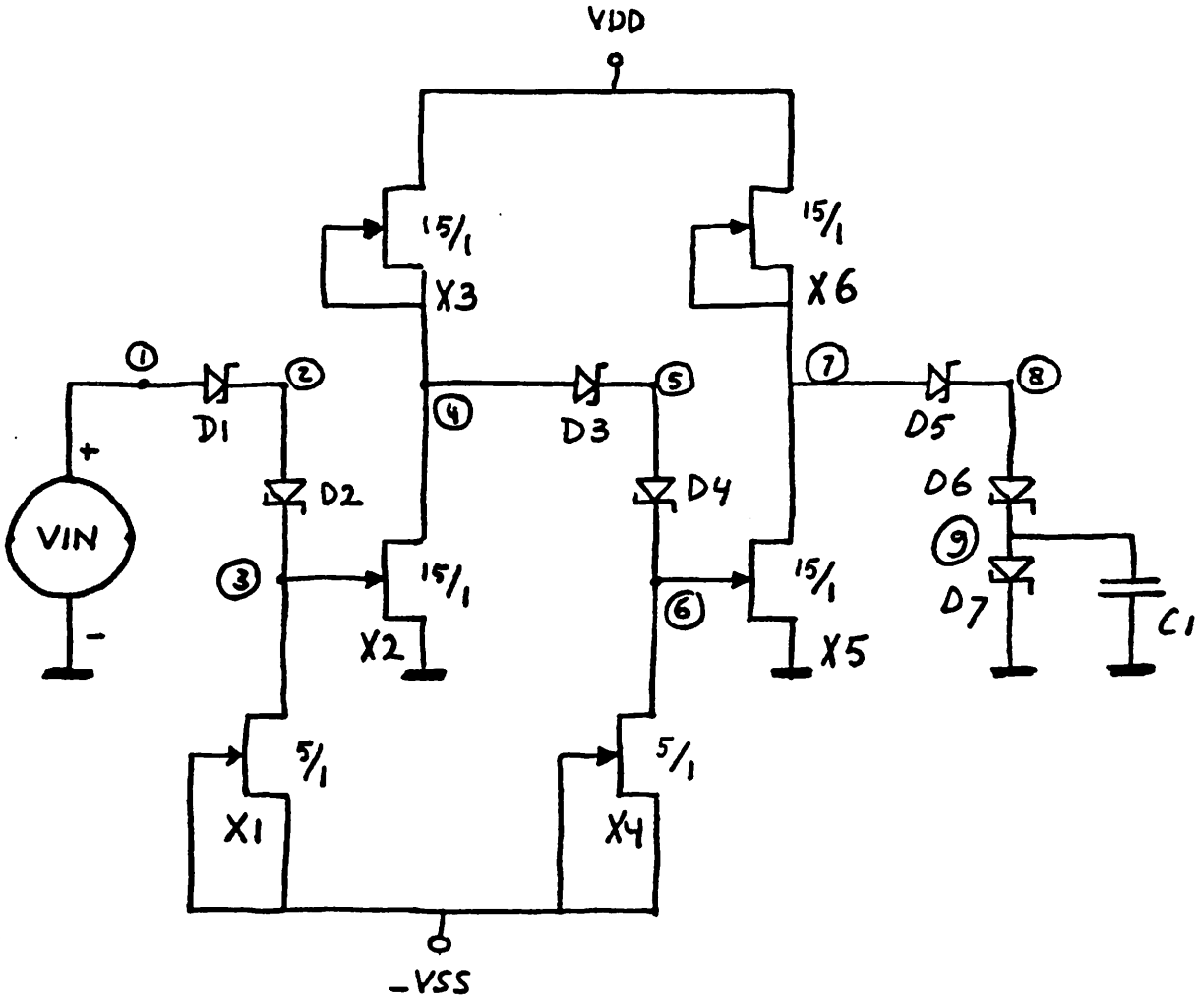

Figure 5.1: Circuit used in the simulation.

The IV characteristics of the device used in the simulation are shown on page 27 and page 28. A simulation of the DC transfer function is given in Section 5B, and a simulation of the transient response is given in Section 5C. The job control

********** 15 NOV 78 ********** SPICE 2E.2 (26SEP78) ********** 19:25:08 **********

DC OPERATING TEST

DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

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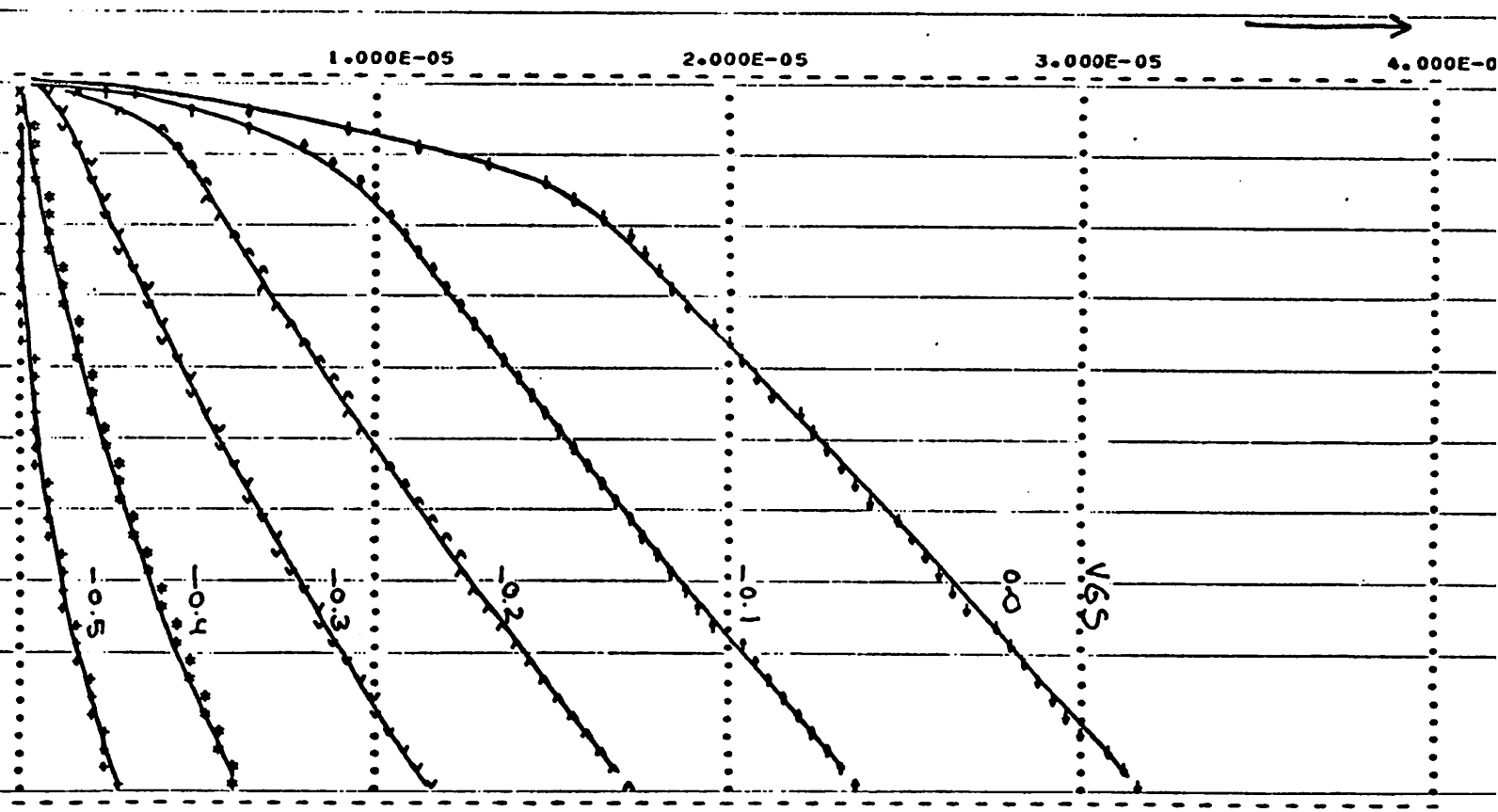
LEGEND:

+: I(VN5)
*: I(VN4)
v: I(VN3)
^: I(VN2)
↑: I(VN1)
↓: I(VO)

VDD (+*v^↑↓)	I(VN5)
5.000E-02	1.940E-11
1.000E-01	2.123E-11
1.500E-01	2.305E-11
2.000E-01	2.488E-11
2.500E-01	2.671E-11
3.000E-01	2.853E-11
3.500E-01	7.375E-10
4.000E-01	5.892E-09
4.500E-01	1.603E-08
5.000E-01	3.113E-08
5.500E-01	5.120E-08
6.000E-01	7.620E-08
6.500E-01	1.061E-07
7.000E-01	1.409E-07
7.500E-01	1.807E-07
8.000E-01	2.254E-07
8.500E-01	2.749E-07
9.000E-01	3.292E-07
9.500E-01	3.884E-07
1.000E+00	4.526E-07
1.050E+00	5.216E-07
1.100E+00	5.952E-07
1.150E+00	6.737E-07
1.200E+00	7.572E-07
1.250E+00	8.454E-07
1.300E+00	9.380E-07
1.350E+00	1.036E-06
1.400E+00	1.138E-06
1.450E+00	1.245E-06
1.500E+00	1.357E-06
1.550E+00	1.474E-06
1.600E+00	1.595E-06
1.650E+00	1.721E-06
1.700E+00	1.851E-06
1.750E+00	1.987E-06
1.800E+00	2.127E-06
1.850E+00	2.272E-06
1.900E+00	2.420E-06
1.950E+00	2.574E-06
2.000E+00	2.733E-06



25:08 **********

C

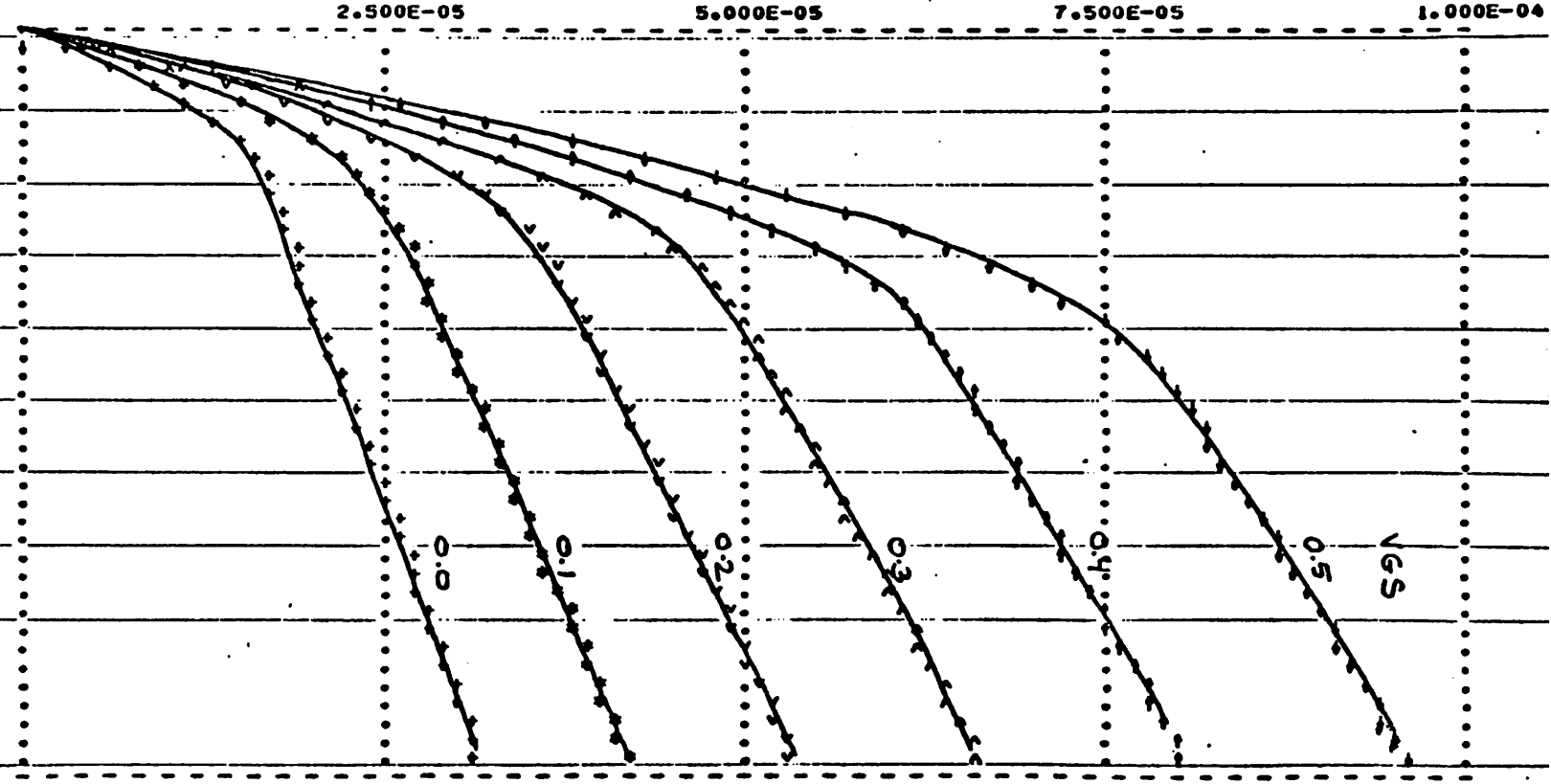
****

DIODE	
IS	1.00E-12
N	1.100
EG	.720
PT	2.000

MESF	
TYPE	NMOS
LEVEL	-1.000
VTO	1.800
KP	5.00E+00
GAMMA	.065
PHI	.560
LAMBDA	.540
CGS	1.50E-10
CGD	1.50E-10
CGB	1.50E-10
CBD	3.00E-05
CBS	3.00E-05
TOX	2.14E-07
PB	.600
JS	1.00E-04
NSS	-.030
NFS	3.00E+16
XJ	2.00E-01
LD	4.500
UO	650.000
UCRIT	3.30E-01
UEXP	.320
UTRA	-.030
KF	-1.60E-03
AF	1.000
FC	.500
W	5E-06
L	1E-06

IDS (A)

VDD	I(VO)
(+*VA+++)----------	0.
5.000E-02	3.349E-06
1.000E-01	6.368E-06
1.500E-01	9.057E-06
2.000E-01	1.126E-05
2.500E-01	1.313E-05
3.000E-01	1.464E-05
3.500E-01	1.578E-05
4.000E-01	1.656E-05
4.500E-01	1.706E-05
5.000E-01	1.754E-05
5.500E-01	1.803E-05
6.000E-01	1.851E-05
6.500E-01	1.899E-05
7.000E-01	1.947E-05
7.500E-01	1.995E-05
8.000E-01	2.043E-05
8.500E-01	2.090E-05
9.000E-01	2.138E-05
9.500E-01	2.185E-05
1.000E+00	2.233E-05
1.050E+00	2.280E-05
1.100E+00	2.327E-05
1.150E+00	2.372E-05
1.200E+00	2.417E-05
1.250E+00	2.467E-05
1.300E+00	2.514E-05
1.350E+00	2.558E-05
1.400E+00	2.603E-05
1.450E+00	2.651E-05
1.500E+00	2.698E-05
1.550E+00	2.742E-05
1.600E+00	2.787E-05
1.650E+00	2.832E-05
1.700E+00	2.880E-05
1.750E+00	2.926E-05
1.800E+00	2.969E-05
1.850E+00	3.013E-05
1.900E+00	3.061E-05
1.950E+00	3.106E-05
2.000E+00	3.149E-05



JOB CONCLUDED

cards naturally depend on the computer system used, but for clarity an example is given in Section 5A.

A. Job Control Cards

An example of the job control cards is given below.

```
D7621,0,40,60000,50.CEES HARTGRING
%rPW=MESFET
ROUTE,USERB
ATTACH,SPICE,ID=2307
RFL,40000
FLGO,SPICE
```

B. DC Transfer Function

The input deck is shown below. The output is shown on page 30.

```
dc transfer function
.op
.dc vin 0 2 .05
.plot dc v(4)
vin 1 0
vdd 10 0 2
vss 0 11 1
d1 1 2 diod1
d2 2 3 diod1
d3 4 5 diod1
d4 5 6 diod1
d5 7 8 diod1
d6 8 9 diod1
d7 9 0 diod1
x1 3 11 11 11 mesf1
x2 4 3 0 11 mesf3
x3 10 4 4 11 mesf3
x4 6 11 11 11 mesf1
x5 7 6 0 11 mesf3
x6 10 7 7 11 mesf3
.subckt mesf3 6 5 7 8
rs 3 7 400
rg 2 5 3
rd 1 6 400
```

********** 15 NOV 78 ********** SPICE 2E.2 (26SEP78) ********** 19:40:23

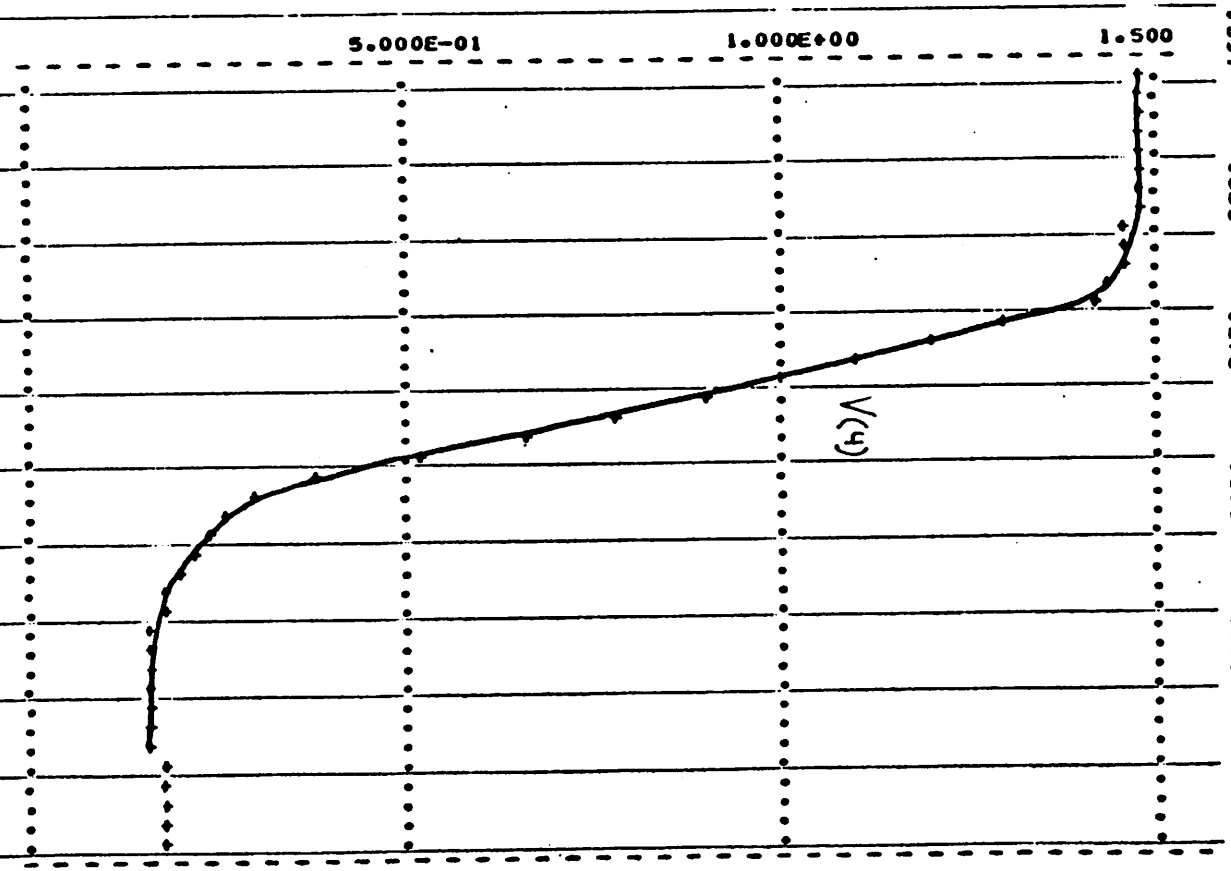
DC TRANSFER FUNCTION

DC TRANSFER CURVES

TEMPERATURE = 27.000 DEG C

****

VIN	V(4)
0.	1.478E+00
5.000E-02	1.478E+00
1.000E-01	1.478E+00
1.500E-01	1.478E+00
2.000E-01	1.478E+00
2.500E-01	1.478E+00
3.000E-01	1.477E+00
3.500E-01	1.474E+00
4.000E-01	1.469E+00
4.500E-01	1.462E+00
5.000E-01	1.452E+00
5.500E-01	1.439E+00
6.000E-01	1.421E+00
6.500E-01	1.295E+00
7.000E-01	1.205E+00
7.500E-01	1.109E+00
8.000E-01	1.005E+00
8.500E-01	8.950E-01
9.000E-01	7.775E-01
9.500E-01	6.520E-01
1.000E+00	5.212E-01
1.050E+00	3.849E-01
1.100E+00	3.052E-01
1.150E+00	2.691E-01
1.200E+00	2.403E-01
1.250E+00	2.173E-01
1.300E+00	2.004E-01
1.350E+00	1.870E-01
1.400E+00	1.755E-01
1.450E+00	1.677E-01
1.500E+00	1.640E-01
1.550E+00	1.625E-01
1.600E+00	1.627E-01
1.650E+00	1.642E-01
1.700E+00	1.670E-01
1.750E+00	1.657E-01
1.800E+00	1.722E-01
1.850E+00	1.757E-01
1.900E+00	1.795E-01
1.950E+00	1.839E-01
2.000E+00	1.884E-01



MODEL	X1.MI	X2.MI	X3.MI	X4.MI	X5.MI	X6.MI
ID	7.29E-06	1.92E-12	3.15E-05	2.65E-05	7.25E-05	7.27E-05
VGS	-.009	-.882	-.013	-.033	.409	-.029
VDS	.096	1.478	.497	1.374	.136	1.743
VBS	-.009	-1.000	-2.491	-.033	-1.031	-1.228
VTH	-.397	-.335	-.273	-.365	-.333	-.324

```
rb 4 8 5k
dd 2 1 diode 3
ds 2 3 diode 3
ml 1 2 3 4 mesf w=15u l=1u as=200p ad=200p
.ends mesf3
.subckt mesfl 6 5 7 8
rs 3 7 1250
rg 2 5 1
rd 1 6 1250
rb 4 8 10k
dd 2 1 diode
ds 2 3 diode
ml 1 2 3 4 mesf w=5u l=1u as=100p ad=100p
.ends mesfl
.model diode d(is=1p n=1.1 eg=.72 pt=2 )
.model diodl d(is=2p n=1.1 eg=.72 pt=2 rs=1500 )
.model mesf nmos (phi=.56 kp=5 tox=2.14e-7 nfs=3e16 ld=4.5 uo=650
+      ucrit=.33 uexp=.32 nss=-.03 utra=-.03 xj=.2 gamma=.65 )
.options acct reltol=.01 abstol=50n vntol=100u
.end
%r
```

C. Transient Response

Two runs have been made.

In the first run LEVEL=-1 and LAMBDA=0.54 is used (empirical model). The input deck for this run is shown below and the output is shown on page 32.

In the second run LEVEL=-2 and LAMBDA=3 is used (theoretical model). The input deck is the same as in the first run, except for the parameters LEVEL and LAMBDA. The output is shown on page 33.

```
transient response
.op
.tran .1n 4n
.plot tran v(4) v(1) v(7)
.plot tran v(3)
vin 1 0 pulse( .164 1.48 0 .1n .1n 1.5n 5n)
vdd 10 0 2
vss 0 11 1
cl 9 0 50f
```

********** 15 NOV 78 ********** SPICE 2E.2 (26SEP78) ********** 20:01:37 **********

TRANSIENT RESPONSE

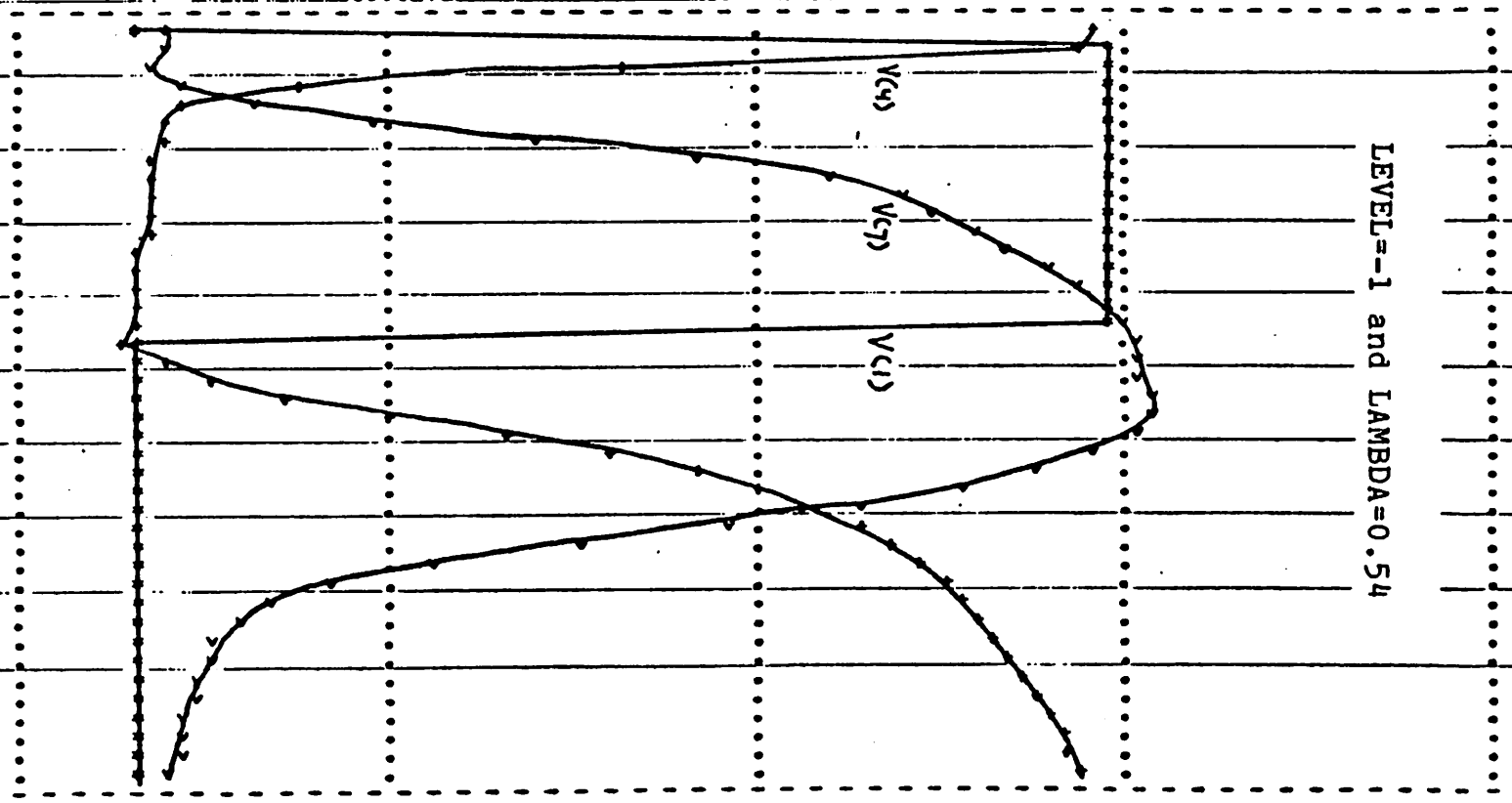
TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

****

LEGEND:

+: V(4)
*: V(1)
V: V(7)

TIME (+V)	V(4)
0.	1.459E+00
1.000E-10	1.449E+00
2.000E-10	8.169E-01
3.000E-10	3.719E-01
4.000E-10	2.274E-01
5.000E-10	2.084E-01
6.000E-10	1.963E-01
7.000E-10	1.872E-01
8.000E-10	1.835E-01
9.000E-10	1.835E-01
1.000E-09	1.775E-01
1.100E-09	1.707E-01
1.200E-09	1.654E-01
1.300E-09	1.624E-01
1.400E-09	1.623E-01
1.500E-09	1.616E-01
1.600E-09	1.610E-01
1.700E-09	1.383E-01
1.800E-09	2.031E-01
1.900E-09	2.610E-01
2.000E-09	3.587E-01
2.100E-09	5.027E-01
2.200E-09	6.638E-01
2.300E-09	8.059E-01
2.400E-09	9.125E-01
2.500E-09	9.940E-01
2.600E-09	1.067E+00
2.700E-09	1.131E+00
2.800E-09	1.184E+00
2.900E-09	1.221E+00
3.000E-09	1.251E+00
3.100E-09	1.272E+00
3.200E-09	1.296E+00
3.300E-09	1.321E+00
3.400E-09	1.345E+00
3.500E-09	1.366E+00
3.600E-09	1.385E+00
3.700E-09	1.401E+00
3.800E-09	1.415E+00
3.900E-09	1.426E+00
4.000E-09	1.435E+00



********** 15 NOV 78 ********** SPICE 2E.2 (26SEP78) ********** 20:03:12 **********

TRANSIENT RESPONSE

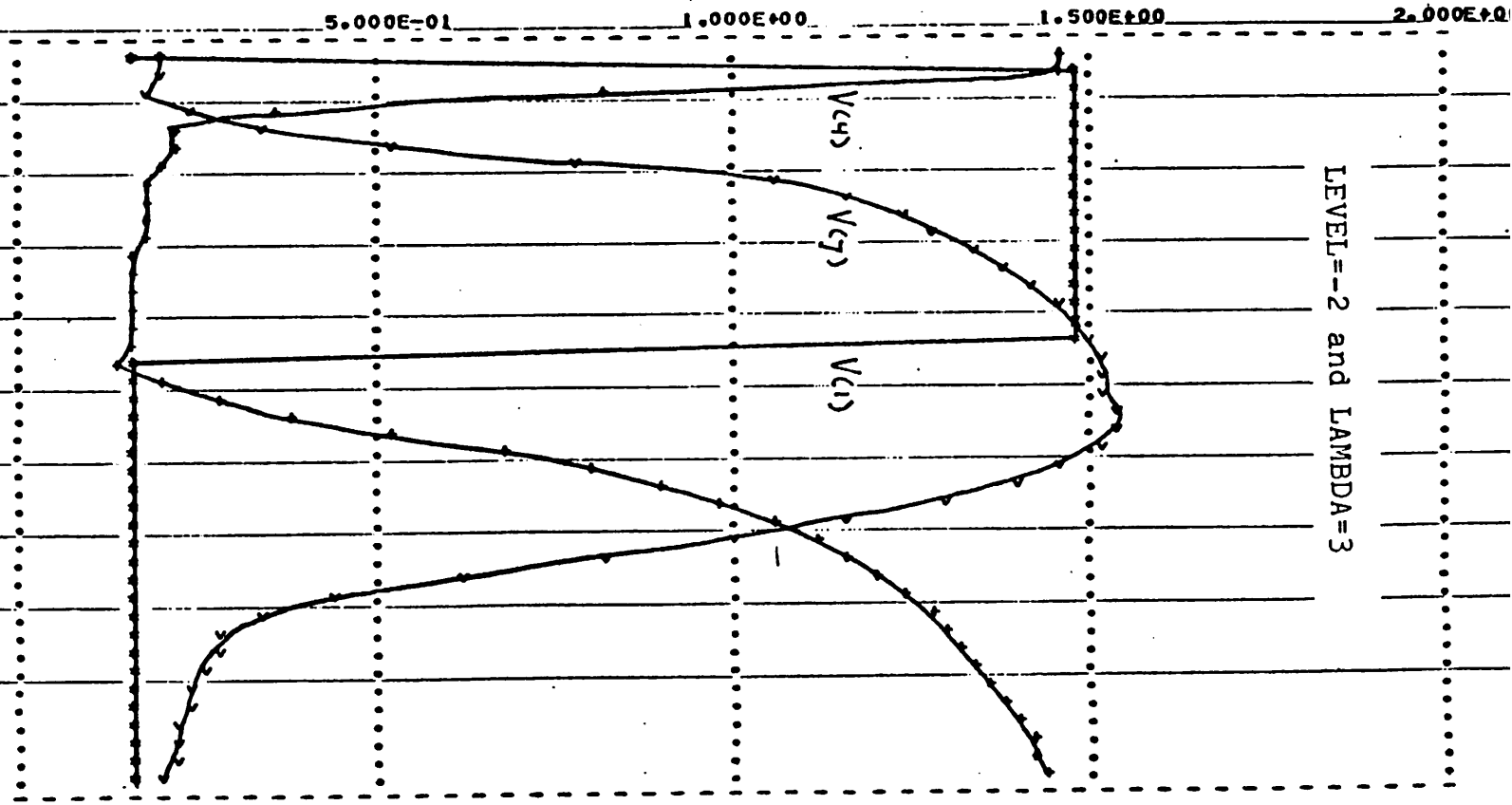
TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

****

LEGEND:

+: V(4)
*: V(1)
v: V(7)

TIME	V(4)
0.	1.459E+00
1.000E-10	1.462E+00
2.000E-10	8.154E-01
3.000E-10	3.541E-01
4.000E-10	2.263E-01
5.000E-10	2.166E-01
6.000E-10	1.913E-01
7.000E-10	1.848E-01
8.000E-10	1.852E-01
9.000E-10	1.823E-01
1.000E-09	1.763E-01
1.100E-09	1.687E-01
1.200E-09	1.592E-01
1.300E-09	1.608E-01
1.400E-09	1.615E-01
1.500E-09	1.612E-01
1.600E-09	1.601E-01
1.700E-09	1.446E-01
1.800E-09	2.076E-01
1.900E-09	2.712E-01
2.000E-09	3.818E-01
2.100E-09	5.253E-01
2.200E-09	6.739E-01
2.300E-09	8.011E-01
2.400E-09	9.027E-01
2.500E-09	9.808E-01
2.600E-09	1.059E+00
2.700E-09	1.116E+00
2.800E-09	1.161E+00
2.900E-09	1.207E+00
3.000E-09	1.247E+00
3.100E-09	1.272E+00
3.200E-09	1.297E+00
3.300E-09	1.322E+00
3.400E-09	1.344E+00
3.500E-09	1.366E+00
3.600E-09	1.386E+00
3.700E-09	1.400E+00
3.800E-09	1.413E+00
3.900E-09	1.428E+00
4.000E-09	1.438E+00



```
d1 1 2 diod1
d2 2 3 diod1
d3 4 5 diod1
d4 5 6 diod1
d5 7 8 diod1
d6 8 9 diod1
d7 9 0 diod1
x1 3 11 11 11 mesf1
x2 4 3 0 11 mesf3
x3 10 4 4 11 mesf3
x4 6 11 11 11 mesf1
x5 7 6 0 11 mesf3
x6 10 7 7 11 mesf3
.subckt mesf3 6 5 7 8
rs 3 7 400
rg 2 5 3
rd 1 6 400
rb 4 8 5k
dd 2 1 diode 3
ds 2 3 diode 3
m1 1 2 3 4 mesf w=15u l=1u as=200p ad=200p
.ends mesf3
.subckt mesf1 6 5 7 8
rs 3 7 1250
rg 2 5 1
rd 1 6 1250
rb 4 8 10k
dd 2 1 diode
ds 2 3 diode
m1 1 2 3 4 mesf w=5u l=1u as=100p ad=100p
.ends mesf1
.model diode d(is=1p n=1.1 eg=.72 pt=2 )
.model diod1 d(is=2p n=1.1 eg=.72 pt=2 cjo=3.5f pb=.6 rs=1500 )
.model mesf nmos (phi=.56 kp=5 tox=2.14e-7 nfs=3e16 ld=4.5 uo=650
+       ucrit=.33 uexp=.32 utra=-.03 nss=-.03 xj=.2 level=-1
+       lambda=.54 )
.options acct reltol=.01 abstol=50n vntol=100u
.end
%r
```

APPENDIX A. SUMMARY OF EQUATIONS

This summary of equations containes all the equations that have been added to the MOSFET model. It is divided into (A1) temperature dependence, (A2) Substrate bias effect, (A3) the drain-to-source current IDS, and (A4) capacitances.

A1. Temperature Dependence

$$PHI(T) = PHI + KF*(T-300)$$

$$UO(T) = UO*300/T$$

A2. Substrate Bias Effect

$$TOX(VBS) = TOX*(1-GAMMA*\sqrt{PB-VBS})$$

A3. Drain-to-source Current IDS

$$IDS = IDSS + IDS1 + IDS2$$

where

$$IDSS = 2*\frac{eps}{TOX}*UO*Vp^2*\frac{W}{L}*\left[Fd-Fs-\frac{2}{3}(Fd^{3/2}-Fs^{3/2})\right]$$

$$Fs = \begin{cases} 0 & \text{for} \quad PHI < VGS \\ \frac{PHI-VGS}{Vp} & \text{for} \quad Vt < VGS < PHI \\ 1 & \text{for} \quad VGS < Vt \end{cases}$$

$$Fd = \begin{cases} 0 & \text{for} \quad PHI < VGD \\ \dfrac{PHI-VGD}{Vp} & \text{for} \quad Vt < VGD < PHI \\ 1 & \text{for} \quad VGD < Vt \end{cases}$$

$$IDS1 = \begin{cases} W*XJ*\left[VDS-LD*(UTRA-VGS)\right]^2 & \text{for} \quad VGS-Vt < UTRA \\ 3*W*XJ*VDS^2*\left[\left(\dfrac{UEXP-(VGS-Vt)}{UEXP-UTRA}\right) - \dfrac{2}{3}\left(\dfrac{UEXP-(VGS-Vt)}{UEXP-UTRA}\right)^{3/2}\right] & \text{for} \\ & UTRA < VGS-Vt < UEXP \\ 0 & \text{for} \quad UEXP < VGS-Vt \end{cases}$$

If NSS < 0

$$IDS2 = \begin{cases} 0 & \text{for} \quad VGS-Vt < NSS \\ UCRIT*W*\left(\dfrac{VGS-Vt-NSS}{-NSS}\right)*VDS & \text{for} \quad NSS < VGS-Vt < 0 \\ W*\left[UCRIT+KP*(VGS-Vt)\right]*VDS & \text{for} \quad 0 < VGS-Vt \end{cases}$$

If NSS > 0

$$IDS2 = \begin{cases} 0 & \text{for} \quad VGS-Vt < 0 \\ 0.25*KP*W*(VGS-Vt)^2*VDS/NSS & \text{for} \quad 0 < VGS-Vt < 2NSS \\ KP*W*(VGS-Vt-NSS)*VDS & \text{for} \quad 2NSS < VGS-Vt \end{cases}$$

A4. Capacitances

$$CGS.tot = CGS*W + CGS'$$

$$CGD.tot = CGD*W + CGD'$$

$$CGB.tot = CGB*L$$

$$CDB.tot = \frac{CBD*AD}{\sqrt{1-VBS/PB}} + CDB'$$

$$CSB.tot = \frac{CBD*AS}{\sqrt{1-VBS/PB}} + CSB'$$

$$CGD' = CGS'*\left(\frac{1-Fd}{1-Fs}\right)$$

$$CDB' = CSB'*\left(\frac{1-Fd}{1-Fs}\right)$$

Theoretical model:

$$CGS' = LAMBDA*\frac{eps*}{TOX}\ \frac{(1+Fs^{1/2})}{(1+2*Fs^{1/2})^2}$$

$$CSB' = \begin{cases} \dfrac{0.7*CBS*W*L}{\sqrt{1-VBS/PB}} & \text{for } Vt < VGS \\ 0 & \text{for } VGS < Vt \end{cases}$$

Empirical model:

$$CGS' = LAMBDA*\frac{eps*}{TOX}*(VTO-Fs)^2$$ Fs can have a value larger than one.

$$CSB' = \frac{0.7*CBS*W*L}{\sqrt{1-VBS/PB}}$$

APPENDIX B. MODIFYING DECK

The listing of the program that is used to modify SPICE, version 2E2, is printed below.

```
D7621,0,77,10000,400.CEES
%rPW=MESFET
SET,R1=1,R2=2
COMMON,OPL$1,SC,FA
IFNERR,THEN,GOTO,GOTOPL
COMMON,OPL$1,WR,FA
ATTACH,OLDPL,SPICEPL,ID=4275,CY=1,PW=READ
COPY,I=OLDPL(R,UNLOAD),O=OPL$1(R,UNLOAD),LVL=EOI,END=EOF,B,DETAIL
COMMON,OPL$1,SC,FA
GOTOPL:.:GOTOPL:
COMMON,OPL$2,WR,FA
IFERR,THEN,STOP
REQUEST,MODLST,PR
REQUEST,FTNLST,PR
REQUEST,LIBLST,PR
REQUEST,LDRLST,PR
COMMON,MODNPL,WR,FA
RFL,40000
COPY,I=INPUT,O=NEWDK(RA),LVL=EOF
X,MODIFY,SP=0,P=OPL$1,L=MODLST,C=FTNTXT,N=MODNPL
COMMON,FTNBIN,WR,FA
RFL,54000
RUNW,,,,FTNTXT,FTNLST,FTNBIN
RFL,21000
X,LIBEDIT(P=OPL$1,N=OPL$2,L=LIBLST,B=0)
REWIND,OPL$2
X,GTR,OPL$2,SPBIN,Q,NR,Z=ANY/OVERLAY-FOURAN
COMMON,SPICE,WR,FA
RFL,64000
CLDR,I=SPBIN,L=LDRLST,NOGO
%r
MESFET
      SUBROUTINE MESFET(VDS,VBS,VGS)
C
C THIS SUBROUTINE CALCULATES THE DC DRAIN CURRENT AND ITS DERIVIATES
C
*CALL MOSARG
      IF (VBS.GT.0.0) GO TO 5
C
C  TAHPLA=PB
C  SCATT=VP_0
C  RAT= TOX_NEW / TOX_0
C  BETA2= PROPORTIONALITY CONSTANT SHOCKLEY EQUATION
C  BION= VP_NEW
```

```
C  VON= VT_NEW
C  UTHSUB= NSS
C  ALPHAF= KP
C  VBP= UCRIT
C  AHPLA=LD
C
      HELP=SQRT(TAHPLA-VBS)
      GO TO 10
    5 HELP=SQRT(TAHPLA)
      HELP=HELP-VBS/(HELP+HELP)
      HELP=AMAX1(0.0,HELP)
   10 RAT=1.0-GAMMA*HELP
      COX=RAT
      BETA2=BETA1*RAT**3
      BION=SCATT*RAT*RAT
      VON=PHI-BION
      UTRAN=UTRA+VON
      UEXPN=UEXP+VON
      UTHN=UTHSUB+VON
      ETAS=(PHI-VGS)/BION
      ETAD=(PHI-VGS+VDS)/BION
      IF (ETAS.LE.0.0) ETAS=0.0
      IF (ETAD.LE.0.0) ETAD=0.0
      IF (ETAD.GE.1.0) ETAD=1.0
      VGST=VGS-VON
      VDSAT=VGST
      IF (VDSAT.LE.0.0) VDSAT=0.0
      GDS=0.0
      GM=0.0
      GMBS=0.0
      CDRAIN=0.0
C
C   OUTPUT CONDUCTANCE COMPONENT FOR LOW VDS (IDS2)
C
      IF (UTHN.GE.VON) GO TO 20
      IF (VGS.LE.UTHN) GO TO 30
      IF (VGST.GE.0.0) GO TO 18
      VGSQ=VGS-UTHN
      VTQ=VON-UTHN
      GDS2=VBP/VTQ
      GM=GDS2*VDS
      GDS=GDS2*VGSQ
      CDRAIN=GDS*VDS
      GMBS=BION*GAMMA*GDS*VDS/(VTQ*HELP*RAT)
      GO TO 30
   18 GM=ALPHAF*VDS
      GDS=VBP+ALPHAF*VGST
      CDRAIN=GDS*VDS
      GMBS=GM*BION*GAMMA/(HELP*RAT)
      GO TO 30
C
   20 IF (VGST.LE.0.0) GO TO 30
      XUS=2.*UTHN-VON
      IF (VGS.LT.XUS) GO TO 25
      GM=ALPHAF*VDS
```

```
      GDS=ALPHAF*(VGS-UTHN)
      CDRAIN=GDS*VDS
      GO TO 30
   25 UTHQ=UTHN-VON
      UTHV=VGST/UTHQ
      GM=.5*ALPHAF*UTHV*VDS
      GDS=.25*ALPHAF*UTHV*VGST
      GBS=ALPHAF*VDS*UTHV*(.5-.25*UTHV)*GAMMA*BION/(HELP*RAT)
     CDRAIN=GDS*VDS
C
C   SUBSTRATE LEAKAGE COMPONENT (IDS1)
C
  30  IF (XJ.LE.0.0.OR.VGS.GE.UEXPN) GO TO 60
      IF (VGS.GT.UTRAN) GO TO 40
      GREET=VDS+AHPLA2*(VGS-UTRAN)
      IF (GREET.LE.0.0) GREET=0.0
      GDS1=2.0*XJ*GREET
      GDS=GDS+GDS1
      GM=GM+GDS1*AHPLA2
      CDRAIN=CDRAIN+XJ*GREET*GREET
      GO TO 60
  40  VLG=UEXPN-VGS
      VLQ=UEXPN-UTRAN
      IF (UEXP.LE.UTRA) WRITE(6,42)
   42 FORMAT(5X,'ERROR :  UEXP IS LESS THAN UTRA')
      GRA1=VLG/VLQ
      GRA2=GRA1-2.0*GRA1*SQRT(GRA1)/3.0
      GRA3=3.0*XJ*VDS*VDS
      GDS=GDS+6.0*XJ*VDS*GRA2
      GM=GM+GRA3*(SQRT(GRA1)-1.0)/VLQ
      CDRAIN=CDRAIN+GRA2*GRA3
C
C   CALCULATE THE SHOCKLEY COMPONENT
C
  60  IF (VGST.LE.0.0) GO TO 100
      CDRAIN1=BETA2*(ETAD-ETAS-2.0*
     1        (ETAD*SQRT(ETAD)-ETAS*SQRT(ETAS))/3.0)
     CDRAIN=CDRAIN+CDRAIN1
      GM=GM+2.0*BETA2*(SQRT(ETAS)-ETAS)
      GMBS=GMBS+1.5*CDRAIN1*GAMMA/(HELP*RAT)
      GDS=GDS+2.0*BETA2*(SQRT(ETAD)-ETAD)
  100 RETURN
      END
%r
MESCAP
      SUBROUTINE MESCAP(VGS0,VGD0,VGB0,VGS1,VGD1,VGB1,COVLGS,COVLGD,
     1                  COVLGB,CGS0,CGD0,CGB0,CGS1,CGD1,CGB1)
C
C  THIS SUBROUTINE CALCULATES THE CAPACITANCES CGD AND CGS
C
*CALL MOSARG
C
C  BETA0= EPSILON/ TOX_0
C  COX= TOX_NEW / TOX_0
C  SCATT= VP_0
```

```
C   XLAMDA= LAMBDA
C   TAHPLA= PB
C   UFB= (1-Fd)/(1-Fs)
C
      CGB1=COVLGB
      CGB0=COVLGB
      TRUT=XLAMDA*BETA0
      TRUTN=TRUT/COX
      IF (LEV.LT.-1) GO TO 110
C
C    EMPIRICAL MODEL (LEVEL=-1)
C
      XSUG=BETA-ETAS
      IF (XSUG.GT.0.0) GO TO 10
      CGS1=COVLGS
      CGD1=COVLGD
      GO TO 20
   10 CGS=TRUTN*XSUG*XSUG
      CGS1=CGS+COVLGS
      CGD1=UFB*CGS+COVLGD
   20 VBS=VGS0-VGB0
      IF (VBS.GT.0.0) GO TO 70
      HELP0=SQRT(TAHPLA-VBS)
      GO TO 80
   70 HELP0=SQRT(TAHPLA)
      HELP0=HELP0-VBS/(HELP0+HELP0)
      HELP0=AMAX1(0.0,HELP0)
   80 FLUT0=1.0-GAMMA*HELP0
      BION1=SCATT*FLUT0*FLUT0
      TRUTN=TRUT/FLUT0
      VON1=PHI-BION1
      ETAS1=(PHI-VGS0)/BION1
      ETAD1=(PHI-VGD0)/BION1
      IF (ETAS1.LE.0.0) ETAS1=0.0
      IF (ETAD1.LE.0.0) ETAD1=0.0
      IF (ETAD1.GE.1.0) ETAD1=1.0
      XSUG1=BETA-ETAS1
      IF (XSUG1.GT.0.0) GO TO 30
      CGS0=COVLGS
      CGD0=COVLGD
      GO TO 100
   30 IF (ETAS1.LT.1.0) GO TO 35
      UFB1=0.0
      GO TO 40
   35 UFB1=(1.0-ETAD1)/(1.0-ETAS1+1.0E-7)
   40 CGS=TRUTN*XSUG1*XSUG1
      CGD0=CGS*UFB1+COVLGD
      CGS0=CGS+COVLGS
      GO TO 100
C
C    THEORETICAL MODEL (LEVEL=-2)
C
  110 INDEX=1
      UFB3=UFB
      ETAS3=ETAS
```

```
 120 IF (ETAS3.LE.1.0) GO TO 130
     CGS=COVLGS
     CGD=COVLGD
     GO TO 180
 130 SQETAS3=SQRT(ETAS3)
     XTEL=1.0+2.*SQETAS3
     CGS=TRUTN*(1.0+SQETAS3)/(XTEL*XTEL)
    CGD=UFB3*CGS+COVLGD
     CGS=CGS+COVLGS
 180 GO TO (200,250),INDEX
 200 INDEX=2
     CGS1=CGS
     CGD1=CGD
     VBS=VGS0-VGB0
     IF (VBS.GT.0.0) GO TO 220
     HELP0=SQRT(TAHPLA-VBS)
     GO TO 230
 220 HELP0=SQRT(TAHPLA)
     HELP0=HELP0-VBS/(HELP0+HELP0)
     HELP0=AMAX1(0.0,HELP0)
 230 FLUT0=1.0-GAMMA*HELP0
     TRUTN=TRUT/FLUT0
     BION1=SCATT*FLUT0*FLUT0
     ETAS3=(PHI-VGS0)/BION1
     ETAD3=(PHI-VGD0)/BION1
     IF (ETAD3.LE.0.0) ETAD3=0.0
     IF (ETAS3.LE.0.0) ETAS3=0.0
     IF (ETAD3.GE.1.0) ETAD3=1.0
     IF (ETAS3.LT.1.0) GO TO 240
     ETAS3=1.0
     UFB3=0.0
     GO TO 120
 240 UFB3=(1.0-ETAD3)/(1.0-ETAS3+1.0E-7)
    GO TO 120
 250 CGS0=CGS
     CGD0=CGD
 100 RETURN
     END
%r17
*CREATE NEWDK
*IDENT 06MES01
*EDIT MESFET
*EDIT MESCAP
*EDIT MOSFET
*DECK MOSFET
*I MOSFET.45
      LEV=VALUE(LOCM+36)
      IF (LEV.LT.1) GO TO 16
*I EBMOS.29
      GO TO 18
C
C   MESFET MODEL PARAMETERS
C
  16  TOX=VALUE(LOCM+13)
      XW=VALUE(LOCV+2)
```

```
      XL=VALUE(LOCV+1)
      DEVMOD=VALUE(LOCV+8)
      VINIT=VALUE(LOCM+33)
      CSAT=VALUE(LOCM+15)
      AD=VALUE(LOCV+3)
      AS=VALUE(LOCV+4)
      CDSAT=CSAT*AD
      CSSAT=CSAT*AS
      GDPR=VALUE(LOCM+6)
      GSPR=VALUE(LOCM+7)
      COVLGS=VALUE(LOCM+8)*XW
      COVLGD=VALUE(LOCM+9)*XW
      COVLGB=VALUE(LOCM+10)*XL
      BETA=VALUE(LOCM+1)
      ALPHAF=VALUE(LOCM+2)*XW
      GAMMA=VALUE(LOCM+3)
      PHI=VALUE(LOCM+4)
      XLAMDA=VALUE(LOCM+5)
      TAHPLA=VALUE(LOCM+14)
      XNFS=VALUE(LOCM+18)
      AHPLA2=VALUE(LOCM+20)
      VALPHA=VALUE(LOCM+23)
      VBP=VALUE(LOCM+24)*XW
      UTHSUB=VALUE(LOCM+17)
      UEXP=VALUE(LOCM+25)
      UTRA=VALUE(LOCM+26)
      XJ=VALUE(LOCM+19)*XW
      BETA0=VALUE(LOCM+39)*XW*XL
      SCATT=VALUE(LOCM+38)
      BETA1=VALUE(LOCM+40)*XW/XL
      VTO=PHI-0.3*SCATT
      AION=VALUE(LOCM+12)*XW*XL
      COX=1.0
      CD1=ALPHAF*XL*XL/VALPHA
*D MOSFET.245
      CZBS=VALUE(LOCM+11)*AS
      IF (LEV.GT.0) GO TO 507
      IF (LEV.GT.-2) GO TO 503
      IF (ETAS.GE.1.0) AION=0.0
  503 IF (ETAS.LT.1.0) GO TO 505
      UFB=0.0
      GO TO 506
  505 UFB=0.7*(1.0-ETAD)/(1.0-ETAS+1.0E-7)
  506 CZBS=CZBS+0.7*AION
      CZBD=CZBD+AION*UFB
  507 CONTINUE
*D 03JAN78.6
      MOP=LEV+1
      IF (MOP.LE.1) MOP=1
      GO TO (448,405,410,445), MOP
*I EBMOS.37
  448 CALL MESFET(VDS,VBS,VGS)
      GO TO 460
*D 03JAN78.12
      MOP=LEV+1
```

```
      IF (MOP.LE.1) MOP=1
      GO TO (458,452,453,455), MOP
*I 03JAN78.17
      GO TO 460
  458 CALL MESFET(-VDS,VBD,VGD)
*I AUG0576.14
      IF (LEV.LT.1) GO TO 812
*D MOSFET.330
  810 CONTINUE
*I MOSFET.335
  812 CALL MESCAP(VGS1,VGD1,VGB1,VGS,VGD,VGB,COVLGS,COVLGD,COVLGB,
     1       CGS1,CGD1,CGB1,CGS,CGD,CGB)
      GO TO 816
*D EBMOS.47
  813 IF (LEV.LT.1) GO TO 814
      CALL MOSCAP(VGD1,VGS1,VGB1,VGD,VGS,VGB,COVLGD,COVLGS,COVLGB,
*I EBMOS.48
      GO TO 816
  814 CALL MESCAP(VGD1,VGS1,VGB1,VGD,VGS,VGB,COVLGD,COVLGS,COVLGB,
     1      CGD1,CGS1,CGB1,CGD,CGS,CGB)
*EDIT MODCHK
*DECK MODCHK
*D METERS.1,03JAN78.16
     1 1.8, 4.0, 0.07, 0.6, 0.54, 2*0.0, 3*1.5E-10, 2*3.0E-5, 1.4E-7,
    1  0.6, 1.0E-4, 0.0, -0.05, 4.0E16, 0.0, 13.0, 0.0, 1.0, 650.0,
    2  0.2, 0.35, -0.05, -1.6E-3, 1.0, 0.5, -1.0,
*I 03JAN78.26
      IF (LEV.LT.1) GO TO 25
*I MODCHK.133
      IF (ID.LT.4) GO TO 54
      LEV=VALUE(LOCV+30)
      IF (LEV.GT.0) GO TO 54
      DO 53 I=1,NOPAR
      IF (VALUE(LOCV+I).EQ.0.0) GO TO 52
      IF (IMF(I).LT.0.0) GO TO 53
      IF (VALUE(LOCV+I).LT.0.0) GO TO 52
      GO TO 53
   52 VALUE(LOCV+I)=DEFVAL(LOCM+I)
   53 CONTINUE
      GO TO 72
   54 CONTINUE
*I MODCHK.143
   72 CONTINUE
*I 10APR78.1
      DIMENSION IMF(30), IK(30)
*I 03JAN78.19
      DATA IMF /
     1 1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,-1,1,-1,1,1,1,1,1,-1,-1,-1,1,1,
    2 -1 /
      DATA IK /
     1 1,2,1,1,1,0,0,2,2,2,2,2,2,1,2,0,1,2,2,1,0,0,1,2,1,1,2,1,1,1 /
*D 12APR78.5,23JAN77.3
*D MODCHK.39
     2  6HCGS    ,6HCGD    ,6HCGB    ,6HCBD    ,6HCBS    ,6HTOX    ,6HPB
*I 16APR78.12
```

```
   98  CONTINUE
*I MODCHK.342
      LEV=VALUE(LOCV+36)
      IF (LEV.GT.0) GO TO 474
C
C    PROCESS MESFET MODEL PARAMETERS
C
      TOX=VALUE(LOCV+13)
      VPINCH=5.E5*CHARGE*VALUE(LOCV+18)*TOX*TOX/EPSSIL
      TOX=EPSSIL/TOX
      VALUE(LOCV+39)=TOX
      VALUE(LOCV+40)=2.0E-4*TOX*VPINCH*VPINCH*VALUE(LOCV+23)
      VALUE(LOCV+38)=VPINCH
      GO TO 477
  474 CONTINUE
*D METERS.10,METERS.12
*D METERS.14,METERS.16
*D MODCHK.344
  477 PB=VALUE(LOCV+14)
*I 03JAN78.66
      IF (LEV.LT.1) GO TO 480
*I MODCHK.214
      IF (ID.LT.4) GO TO 248
      LOC=LOCS
      LOCV=NODPLC(LOC+1)
      IF (VALUE(LOCV+36).GT.0.3) GO TO 248
      DO 246 ILL=1,30
      ITAB(ILL)=IK(ILL)
  246 CONTINUE
  248 LOC=0
*EDIT TMPUPD
*DECK TMPUPD
*I TMPUPD.144
      LEV=VALUE(LOCV+30)
      IF (LEV.GT.0) GO TO 415
      VALUE(LOCV+23)=VALUE(LOCV+23)/RATIO
      VALUE(LOCV+4)=VALUE(LOCV+4)+DTEMP*VALUE(LOCV+27)
      GO TO 440
  415 CONTINUE
*I TMPUPD.153
  440 CONTINUE
%r
*FILE MODNPL
*INSERT OPL/ELMNSY,OPL/MESFET
*INSERT OPL/ELMNSY,OPL/MESCAP
*FILE FTNBIN
*INSERT REL/ELMNSY,REL/MESFET
*INSERT REL/ELMNSY,REL/MESCAP
%r
```

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