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# NONLINEAR CONVERTERS

# FOR PULSE-CODE-MODULATION SYSTEMS

by

G. Smarandoiu

Memorandum No. UCB/ERL M78/27

24 May 1978

(cover)

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College of Engineering
University of California, Berkeley
94720

# NONLINEAR CONVERTERS
# FOR PULSE-CODE-MODULATION SYSTEMS

D.Eng. Gheorghe Smărăndoiu

Dept. of Electrical
Engineering and
Computer Sciences

David A. Hodges
Chairman of Committee

ABSTRACT

The work presented in this report was directed towards the practical implementation of charge-redistribution techniques in nonuniform converters used in Pulse-Code-Modulation (PCM) telephone transmission.

An encoder-decoder converter pair implementing the μ255 companding law was comercially manufactured using standard CMOS technology.

The codec (coder-decoder) meets standard telephone transmission specifications.

## DEDICATIE

Această lucrare este dedicată soţiei mele Lili. Sacrificiile ei au făcut-o posibilă.

## DEDICATION

This manuscript is dedicated to my wife Lili. Her sacrifices made it possible.

## ACKNOWLEDGEMENTS

I am greatly indebted to Professor David A. Hodges whose guidance and encouragement throughout my years of graduate study led to the successful completion of the work presented in this report. This work does also draw from the ideas of Professor Paul R. Gray and I would like to thank him for so generously offering them.

I was fortunate to study at U.C.B. with Dr. James L. McCreary and Dr. Yannis P. Tsividis and I do sincerely appreciate the many fruitful discussions that we had, as well as their work from which the present one is amply inspired.

At Siliconix I had an excellent working relationship with George F. Landsburg who actually took over the "reconstruction" work after I had left the company. The many useful suggestions of Lorimer Hill and Walter Broedner are also appreciated. For so generously supporting the internship idea and for helping me through some of the most difficult moments I am deeply indebted to John Hulme, Vice President of Engineering at Siliconix Inc.

The completion of the manuscript was made possible by the kindness of my ex-Berkeleyan Director Dr. Constantin D. Bulucea and I would like to thank him once again for his support during the doctoral program.

No words would be sufficient to express my gratitude towards my family who had faith and patience during these last years of continuous sacrifice. I hope they will forgive me.

The work described in this report was performed mainly during the internship that I spent at Siliconix Inc. in Santa Clara, California.

I would also like to acknowledge the support that I received as a Fulbright-Hays fellow and the support from the National Science Foundation received under Grant ENG73-04184-A01.

The whole program was made possible by the generous leave of absence that I was granted from my company Institutul de Cercetări pentru Componente Electronice, Bucureşti, Romania.

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# CHAPTER 1

# 1. INTRODUCTION.

The potential of and need for a totally digital communications network are well understood and its practical implementation is under way. Such a digital hierarchy requires at the first level terminals which convert analog signals into digital form suitable for transmission and then reconstruct the digital information into analog form. At the present time the most common terminal is the so called digital channel bank ( 1 ). Pulse-Code-Modulation (PCM) and Time-Division-Multiplex (TDM) techniques are used to convert several voice channels into binary form and vice-versa. The analog-to-digital (ADC) and digital-to-analog (DAC) converters are shared over a number of 24 to 32 voice channels. This type of digital channel bank configuration is presented in Figure 1.1.

A channel bank operating with per channel dedicated ADC's and DAC's would eliminate the relatively complicated analog multi- and demultiplexing and would also greatly simplify maintenance. Such a system is presented in Figure 1.2.

The main factor determining the choice between these two possible architectures is cost. The version containing dedicated channel converters becomes economically feasable only if the converters can be produced at a competitive cost.

Whereas relatively inexpensive linear converters have been available for some time, this has not been the case with the specialized converters used in the digital channel banks.

Such converters known as codec's (coder-decoder) have

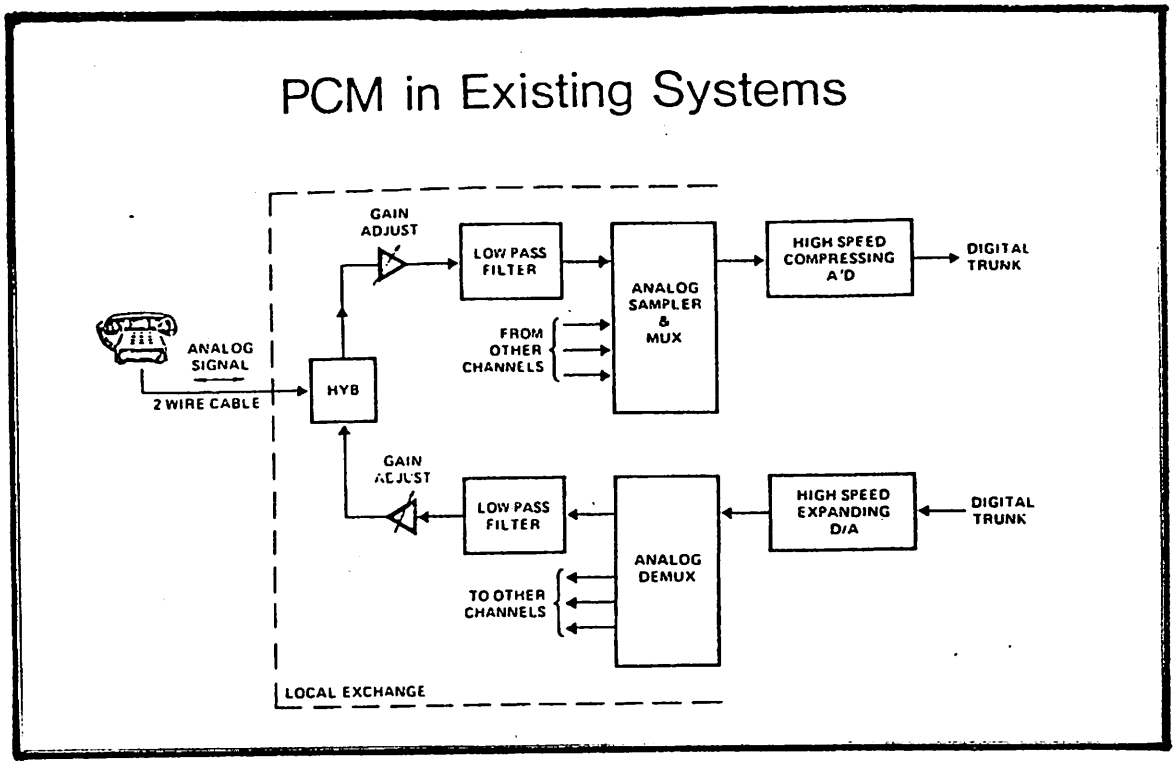

PCM in Existing Systems
GAIN ADJUST
LOW PASS FILTER
ANALOG SAMPLER & MUX
HIGH SPEED COMPRESSING A'D
DIGITAL TRUNK
FROM OTHER CHANNELS
ANALOG SIGNAL
2 WIRE CABLE
HYB
GAIN ADJUST
LOW PASS FILTER
ANALOG DEMUX
HIGH SPEED EXPANDING D/A
DIGITAL TRUNK
TO OTHER CHANNELS
LOCAL EXCHANGE

Figure 1.1

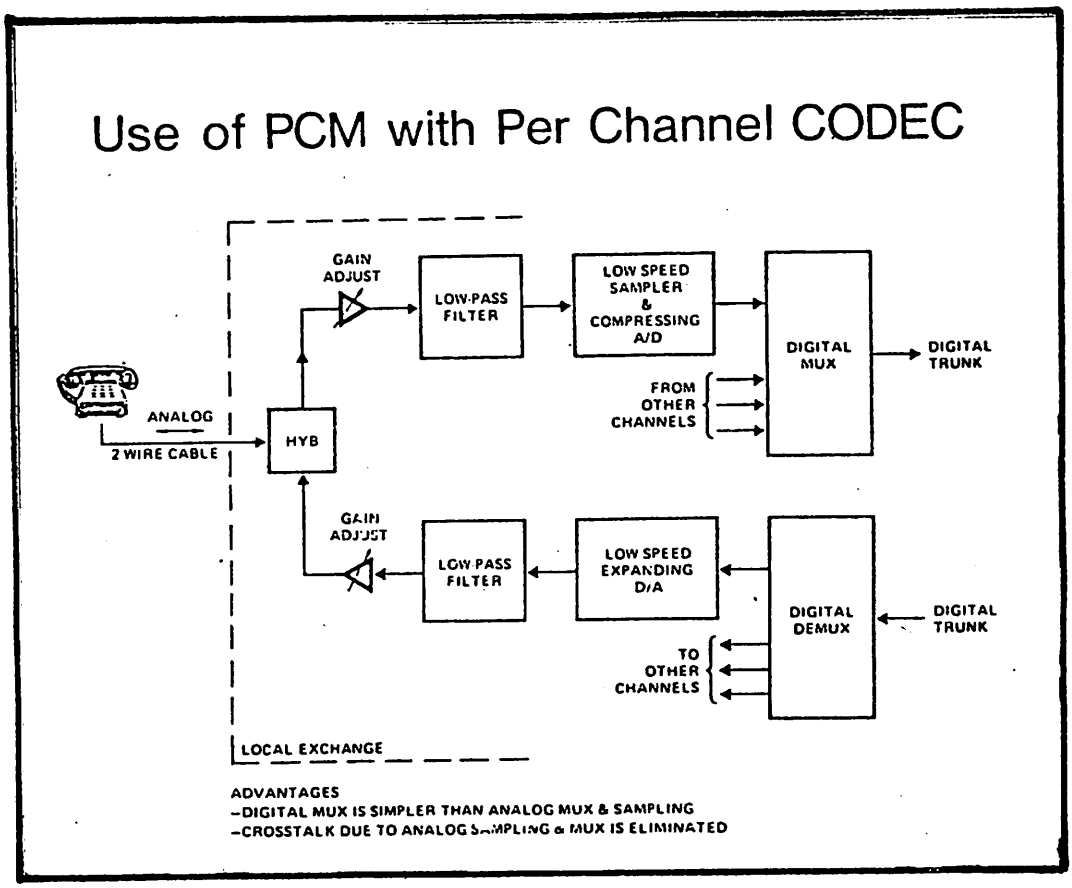

Use of PCM with Per Channel CODEC
GAIN ADJUST
LOW-PASS FILTER
LOW SPEED SAMPLER & COMPRESSING A/D
DIGITAL MUX
DIGITAL TRUNK
FROM OTHER CHANNELS
ANALOG
2 WIRE CABLE
HYB
GAIN ADJUST
LOW-PASS FILTER
LOW SPEED EXPANDING D/A
DIGITAL DEMUX
DIGITAL TRUNK
TO OTHER CHANNELS
LOCAL EXCHANGE
ADVANTAGES
–DIGITAL MUX IS SIMPLER THAN ANALOG MUX & SAMPLING
–CROSSTALK DUE TO ANALOG SAMPLING & MUX IS ELIMINATED

Figure 1.2

to implement nonlinear transfer curves, illustrated in Figure 1.3 and respectively 1.4. Such transfer curves represent piece-wise linear approximations of ideally logarithmic transfer curves. The reasons for such transfer curves have been explained in great detail elsewhere (2,3).

The coder implements a compressing conversion while the decoder will reconstruct the original signal based on an expanding transfer characteristic. The overall effect is coarser resolution at large analog inputs than at smaller ones. This corresponds to adequate conversion of voice signals yielding acceptable signal-to-noise ratios (SNR) over a wide dynamic range. The SNR is defined as the power ratio between the reconstructed fundamental signal and the rest of the harmonics, these harmonics being mainly the result of quantization errors. The limits for acceptable SNR performance are illustrated in Figure 1.5a. The +3dB signal corresponds to a maximum amplitude equal to the full scale of the converters (approximately). An other parameter characterizing the codec is the gain-tracking (GTRCK) defined as the power ratio between the reconstructed signal and the original one. The acceptable limits are illustrated in Figure 1.5b. Both tests, SNR and GTRCK, are performed with 1kHz sinusoidal signals scanning the dynamic range. The sampling frequency is of 8kHz corresponding to a maximum input signal bandwidth of 4kHz, i.e. typical for voice.

The piecewise linear approximation of the ideal logarithmic transfer curves is implemented with 8 positive and 8 negative

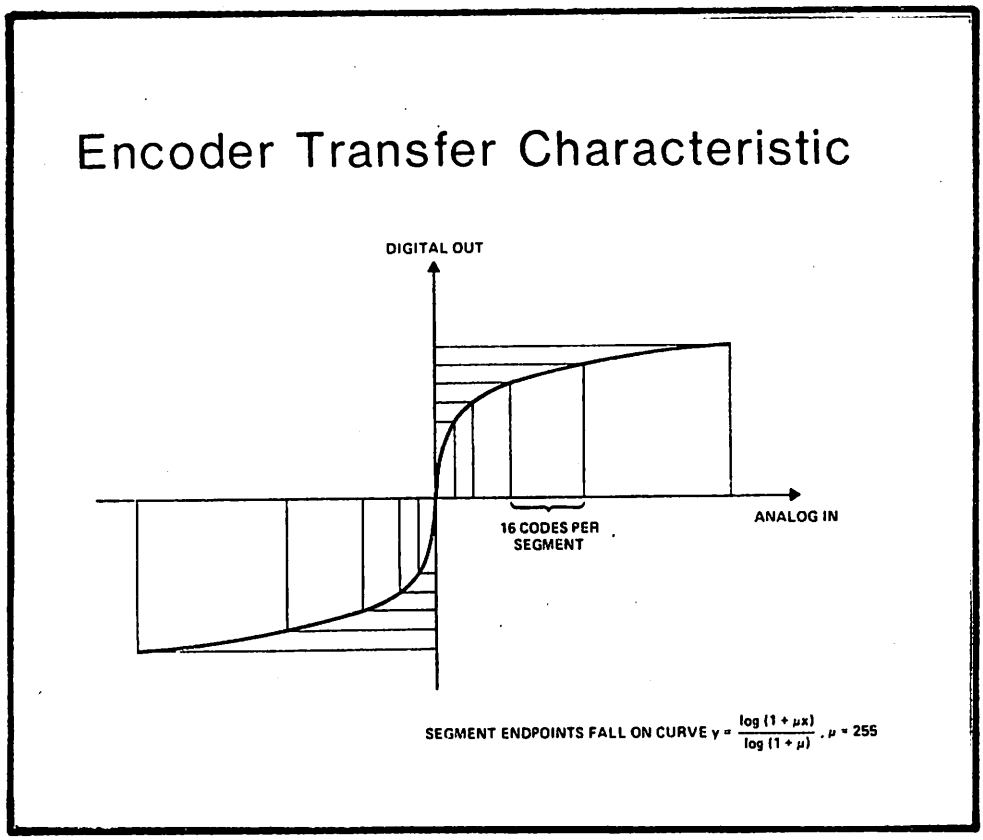

Encoder Transfer Characteristic
DIGITAL OUT
ANALOG IN
16 CODES PER SEGMENT
SEGMENT ENDPOINTS FALL ON CURVE $y = \frac{\log(1+\mu x)}{\log(1+\mu)}$, $\mu = 255$

Figure 1.3

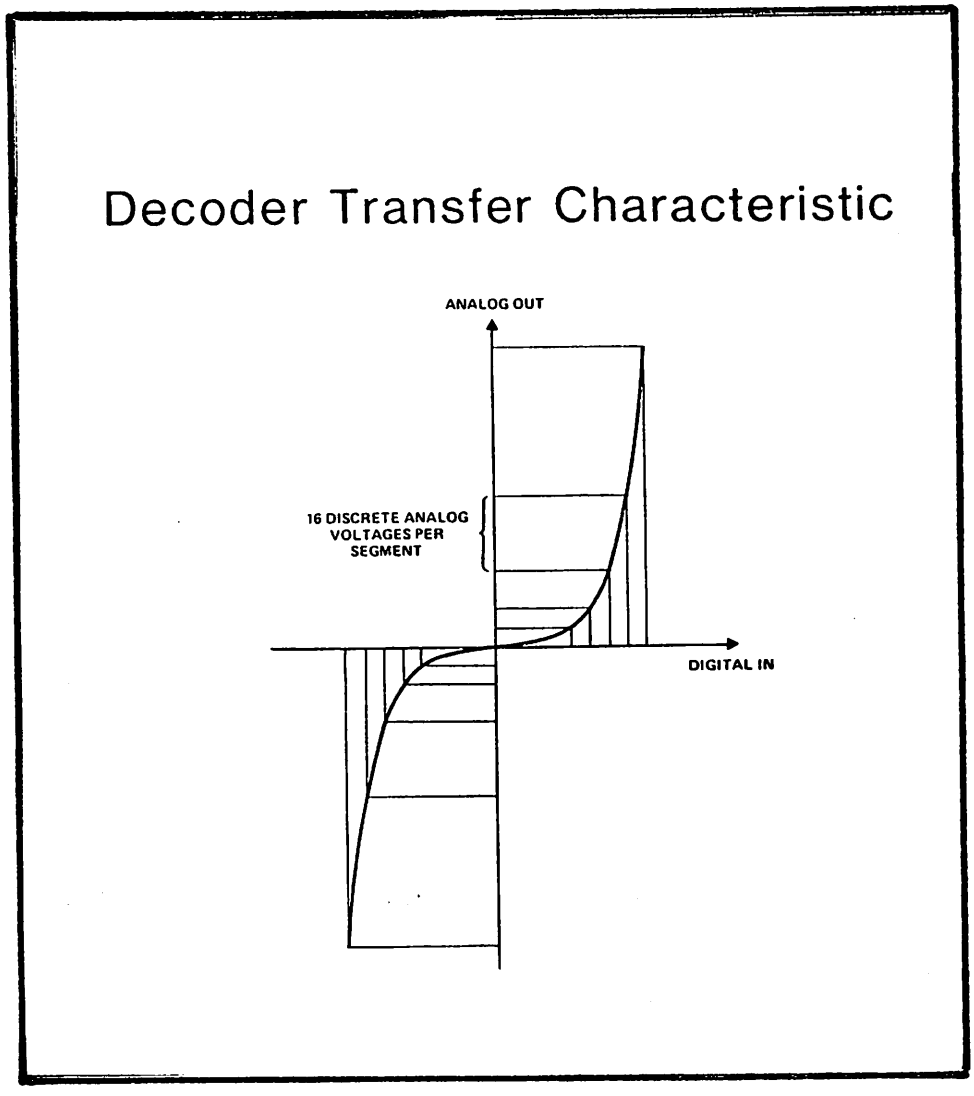
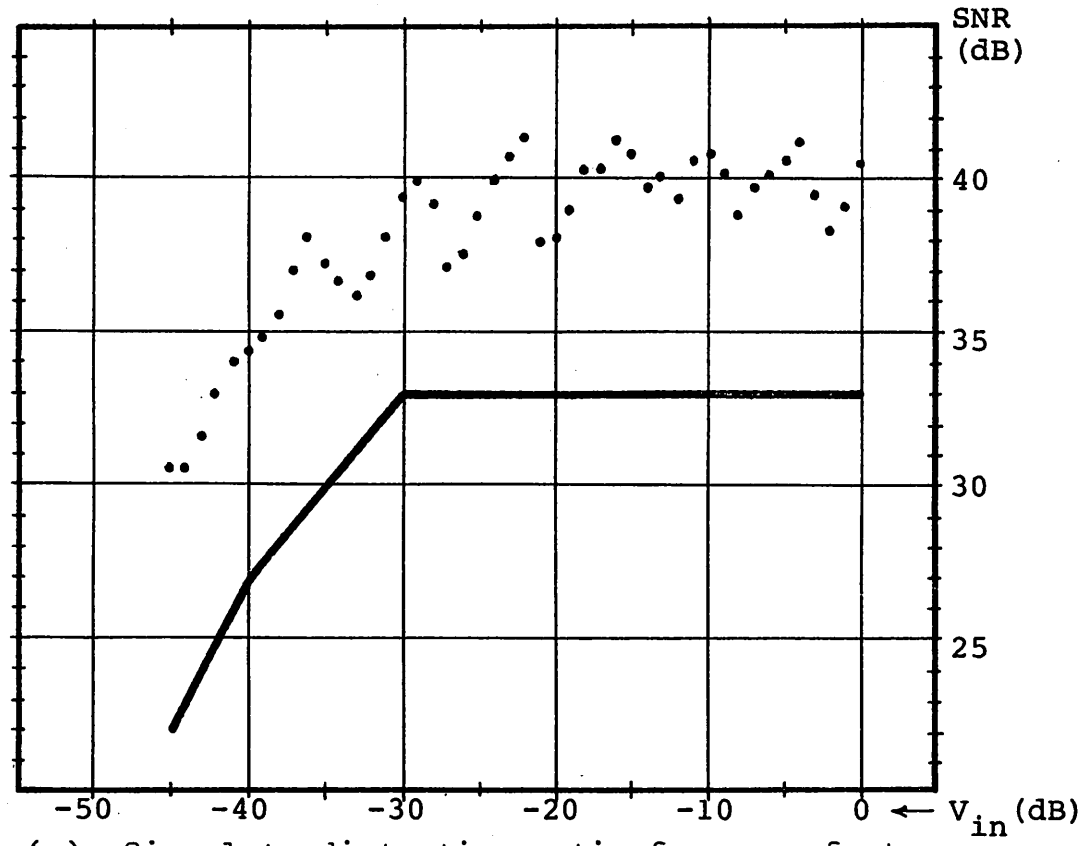
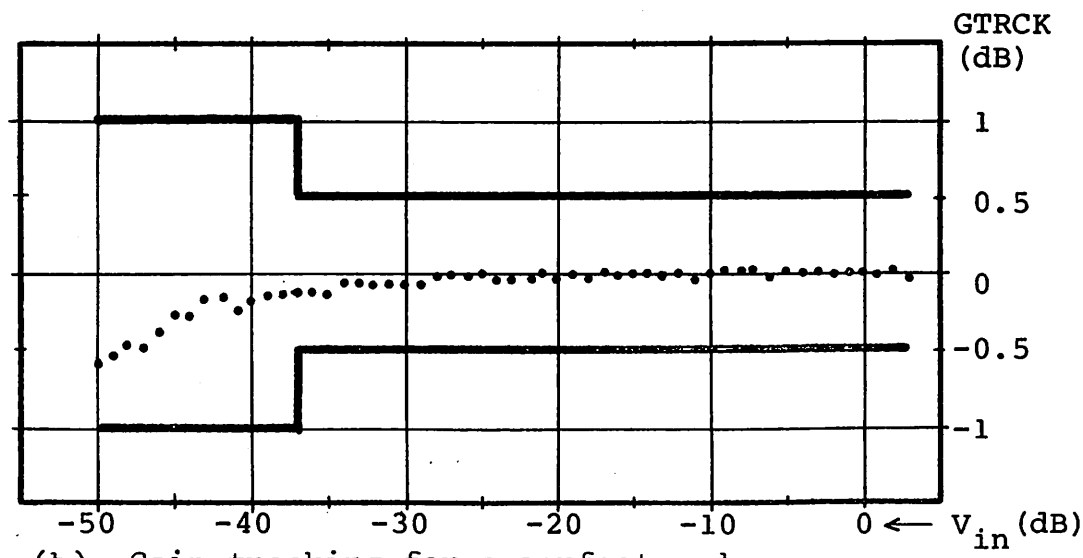

Decoder Transfer Characteristic
ANALOG OUT
16 DISCRETE ANALOG VOLTAGES PER SEGMENT
DIGITAL IN

Figure 1.4




(a) Signal-to-distortion ratio for a perfect codec.



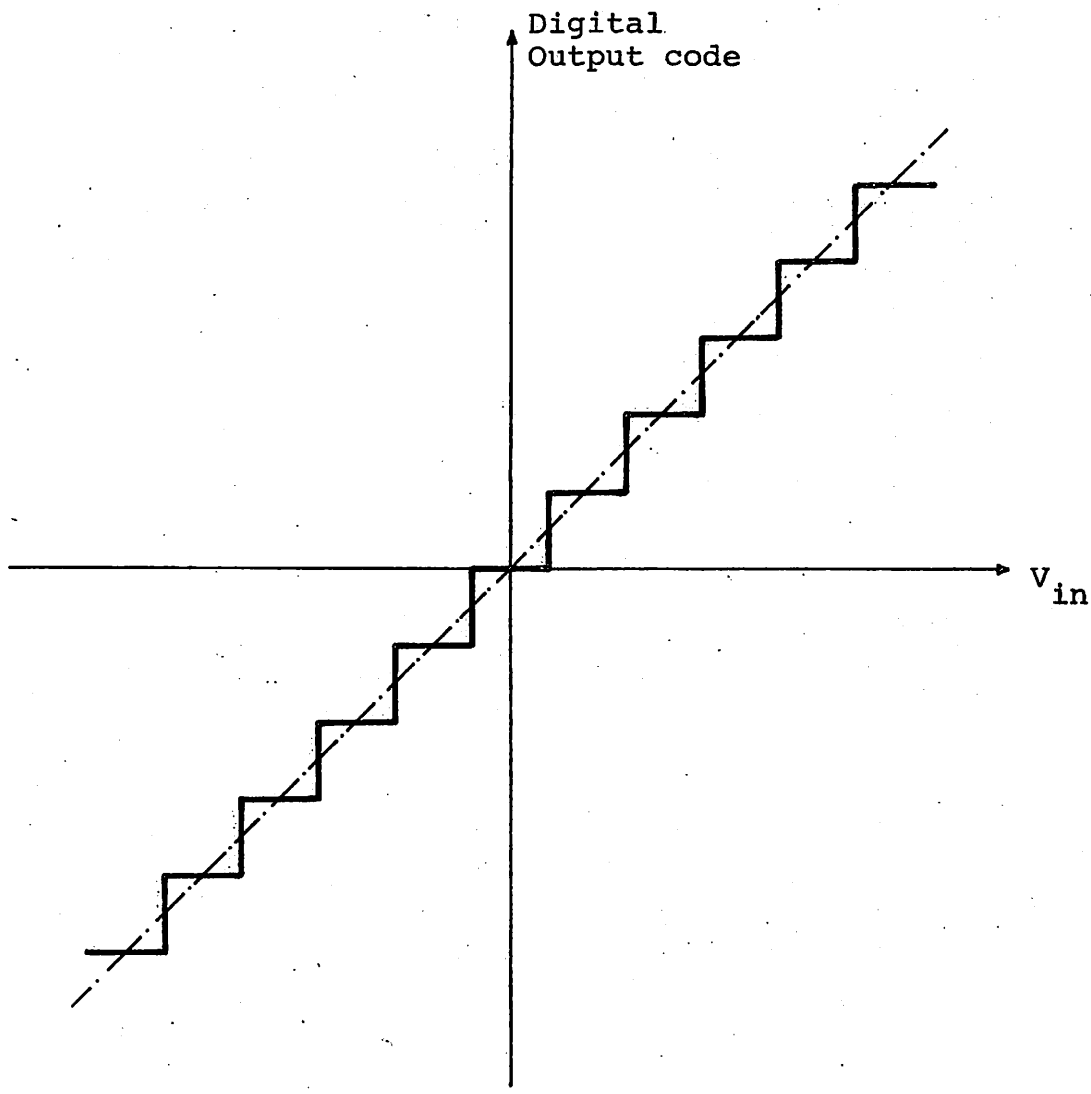

(b) Gain tracking for a perfect codec.

Figure 1.5

binary weighted segments, each of them being divided into 16 steps. The segments are such that the length of a segment is double to that of the previous one. The only exception to this rule is the first segment which contains 15 and 1/2 steps yielding a smooth transition through 0. This is illustrated in Figure 1.6. The rest of the coder segments contain 16 equal steps. The last step in the decoder segments is 1.5 times longer than the previous ones. This is illustrated in Figure 1.7 and is also done for smoothness. Such an arrangement yields 255 discrete decision levels, whence the name of the conversion law, $\mu$255.

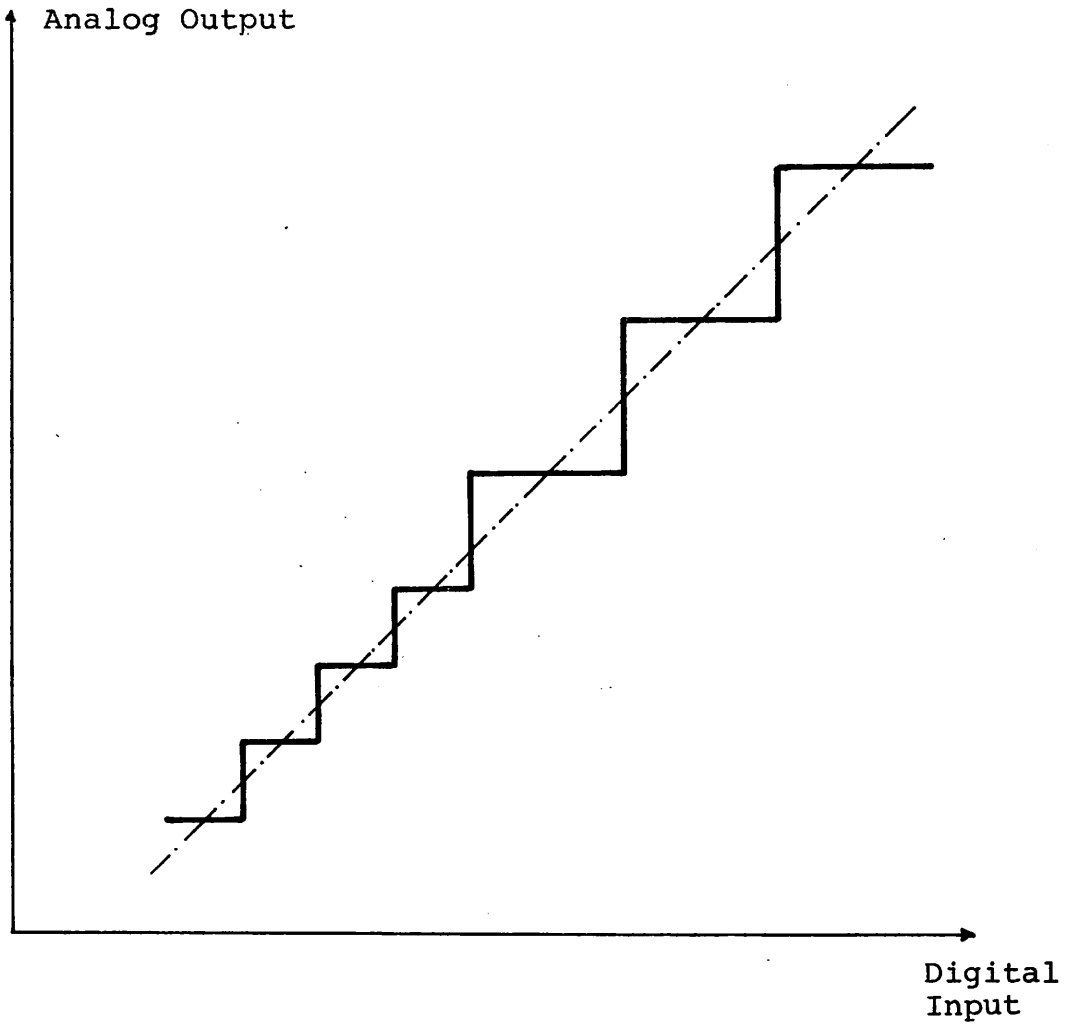
The SNR and GTRCK curves presented in Figure 1.5 correspond to the case of a perfect codec which implements the piecewise linear approximation of the ideal logarithmic conversion law. These piecewise linearized transfer curves could in principle be implemented in any number of ways, with one of the first attempts ( 4 ) using resistive ladders.

With the introduction of charge-redistribution techniques ( 5, 6 ) the realization of economical single chip codecs has become for the first time realistically feasable. The suitability of this technique to nonuniform conversion such as the one required in PCM communication will be analized shortly in Chapter 2. An extensive analysis can be found in ( 3 ). Chapter 3 is devoted to the practical circuit design aspects of the capacitor arrays and the amplifiers used in the converters. Some of the experimental results not covered in Chapter 3 are included in Chapter 4.




Encoder transfer characteristic around $V_{in}=0$

Figure 1.6




Decoder transfer characteristic around the boundary between two segments.

Figure 1.7

The conclusions of this work are presented in Chapter 5.

Since the design was extensively based on computer simulations using XCODEC ( 7 ) the modified version used for the present work has been reproduced in the Appendix. This is done with the kind permission of Y. P. Tsividis, the author of XCODEC.

It should be mentioned that the present work is a natural extension of the work done by J. L. McCreary and Y. P. Tsividis; therefore a complete understanding of the topics being discussed in this report is possible only after the understanding of their original effort presented in ( 8 ) and ( 3 ). With this in mind some of the topics have been described very briefly with no pretense for completness.

# CHAPTER 2

## 2.1 CHARGE REDISTRIBUTION CONVERSION TECHNIQUES.

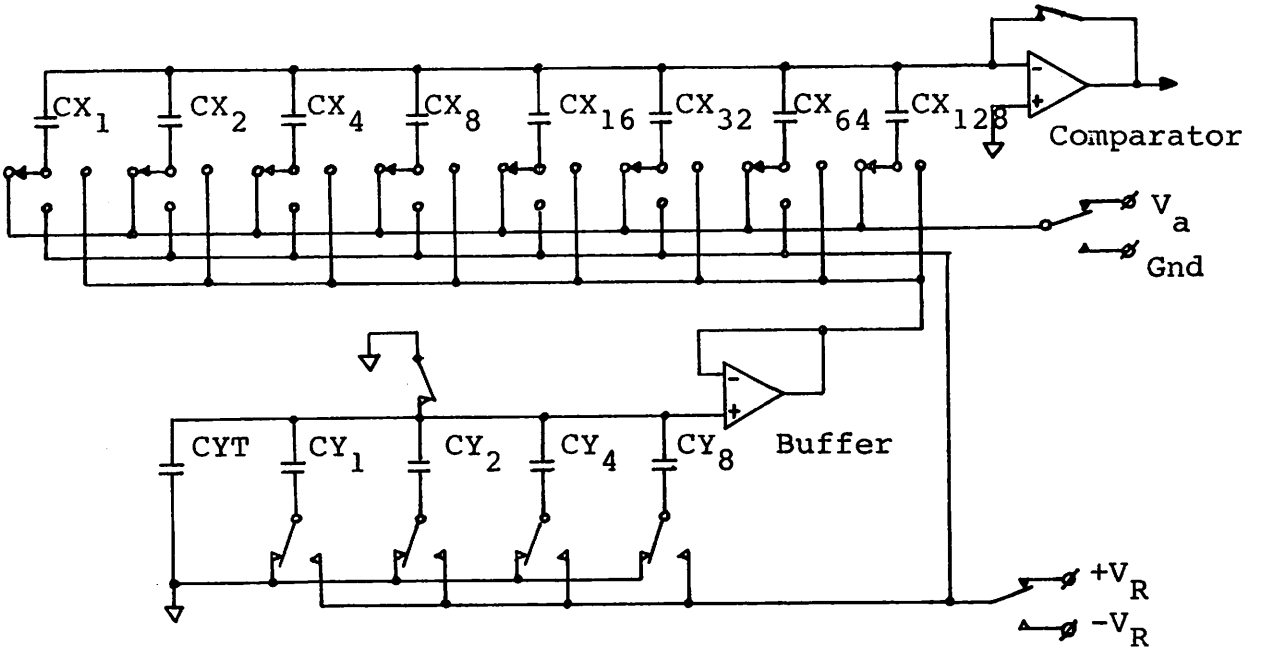
The feasability of analog-to-digital converters based on the use of capacitors instead of resistive ladders and on charge redistribution techniques has been demonstrated by the realization of 8 and 10 bit linear converters (6,5).

One of the major benefits of this technique lies in the fact that the MOS capacitors are compatible with a high yield technology capable of integrating on the same chip digital as well as analog circuitry. Whereas the application of MOS/LSI techniques to digital circuitry has become common practice, its suitability for analog functions has only been demonstrated more recently (9,10,11).

The charge-redistribution technique based on ratioed capacitors (8) appears to be particularly well suited for the implementation of single-channel PCM codecs. The conversion technique used in this case is very similar to the one implemented in the original linear converter (12) and its applicability to nonuniform conversion has been demonstrated in a multichip implementation (13).

## 2.2 ENCODING ALGORITHM.

The encoding algorithm can be described on the basis of Figure 2.1. The conversion is based on the use of two binary weighted capacitor arrays. The segment array, containing capacitors CX1 to CX128, is used to determine the segments of the coder transfer curve, whereas the step array, CY1 to CY8 and CYT, is used for the generation of the steps within a segment.




Simplified encoder block diagram.

Figure 2.1

A conversion proceeds as follows:

First the top plates of the segment array are grounded and the bottom plates are connected to the analog input. In this way the segement capacitors are charged up with $V_a$, the analog input voltage, the polarity being such that the top plates are at $-V_a$ with respect to the bottom plates. The sign (polarity) of the input sample is determined by opening the grounding switch at the top of the segment capacitors, and by grounding the bottom plates. By doing so the voltage at the top plates goes to:

$$V^1_{top} = -V_a$$

and the comparator will switch accordingly. The placement of the analog sample within the segments of the transfer curve is determined by using successive approximation. By throwing the bottom plates of capacitors CX1 to CX8 to the appropriate $V_R$ (reference voltage), the voltage at the top plates becomes:

$$V^2_{top} = -V_a + \frac{CX1+CX2+CX4+CX8}{CXTOT} V_R = -V_a + \frac{15}{255} V_R$$

If $V^2_{top} > 0$, then:

$$V_a < \frac{15}{255} V_R$$

which implies that the input sample falls within the lower 4 segments of the transfer curve (with $V_a$ and $V_R$ assumed to be positive for simplicity). During the following step CX4 and CX8 are thrown back to ground so that:

$$V^3_{top} = V^2_{top} - \frac{CX4+CX8}{CXTOT} V_R = -V_a + \frac{3}{255} V_R$$

and if $V^3_{top}$ is again positive then $V_a$ falls within the first two segments of the transfer curve, etc.

At the end of the fourth charge redistribution the placement within one of the 8 segments of the transfer curve is known (sign bit + 3 "segment bits"). The position of the sample within a segment is determined using the step capacitors.

Thus at the end of the "segment conversion" the capacitors are thrown such that the polarity of:

$$V^4_{top} = -V_a + \frac{CX1+...CXj}{CXTOT} V_R$$

can be changed by either adding to $V^4_{top}$ the value $\frac{CX(j+1)}{CXTOT} V_R$ or by subtracting $\frac{CXj}{CXTOT} V_R$. If $V^4_{top}$ is negative then the placement of the analog sample within the respective segment is found by adding to $V^4_{top}$ multiples of $\frac{CX(j+1)}{CXTOT} x \frac{V_R}{16}$. These multiples are generated with the step capacitor array and fed through the buffer and the segment capacitor CX(j+1) to the top of the segment array. The algorithm is once again successive approximation. Four charge redistributions are needed for the placement of the analog sample within the 16 possible levels in the segment (yielding 4 "step bits").

It is more or less obvious that the matching of the segment capacitors has nothing to do with the matching of the step capacitors. This is probably the most important advantage of the conversion scheme as far as practical implementation is concerned. One can also observe that the encoder will be strictly monotonic.

## 2.3 PRACTICAL CIRCUIT CONFIGURATIONS.

The block diagrams of a practical encoder and respectively decoder circuit based on charge redistribution in capacitive ladders are shown in Figures 2.2 and 2.3.

The analog-to-digital conversion is performed during 12 time slots within a frame of 125μs corresponding to a sampling frequency of 8kHz. The resulting length of a time slot is therefore about 10.4μs. 3 time slots are used for the acquisition of the analog sample, 8 for the charge redistributions yielding the digital output code and 1 for loading the output shift register. The time slots are obtained by internally dividing the incoming 1.544MHz clock.

The digital output word is shifted out at a rate of 1.544Mbit/s corresponding to the use of the circuit as a single-channel encoder used in a 24 channel digital channel bank. The operations that have to be performed during one time slot are: digital control, actual charge redistribution after switch closure, buffer settling, correct comparator response and logic interpretation of the response. The time available in a time slot should be divided accordingly; how this is done will be described in the next chapter.

The operation of the decoder is much simpler being of the " one shot" type. The digital word is first loaded into a buffer register. This operation is performed during a SYNC pulse having a duration of about 5.18μs (in the encoder the digital word is shifted out during a similar SYNC pulse).

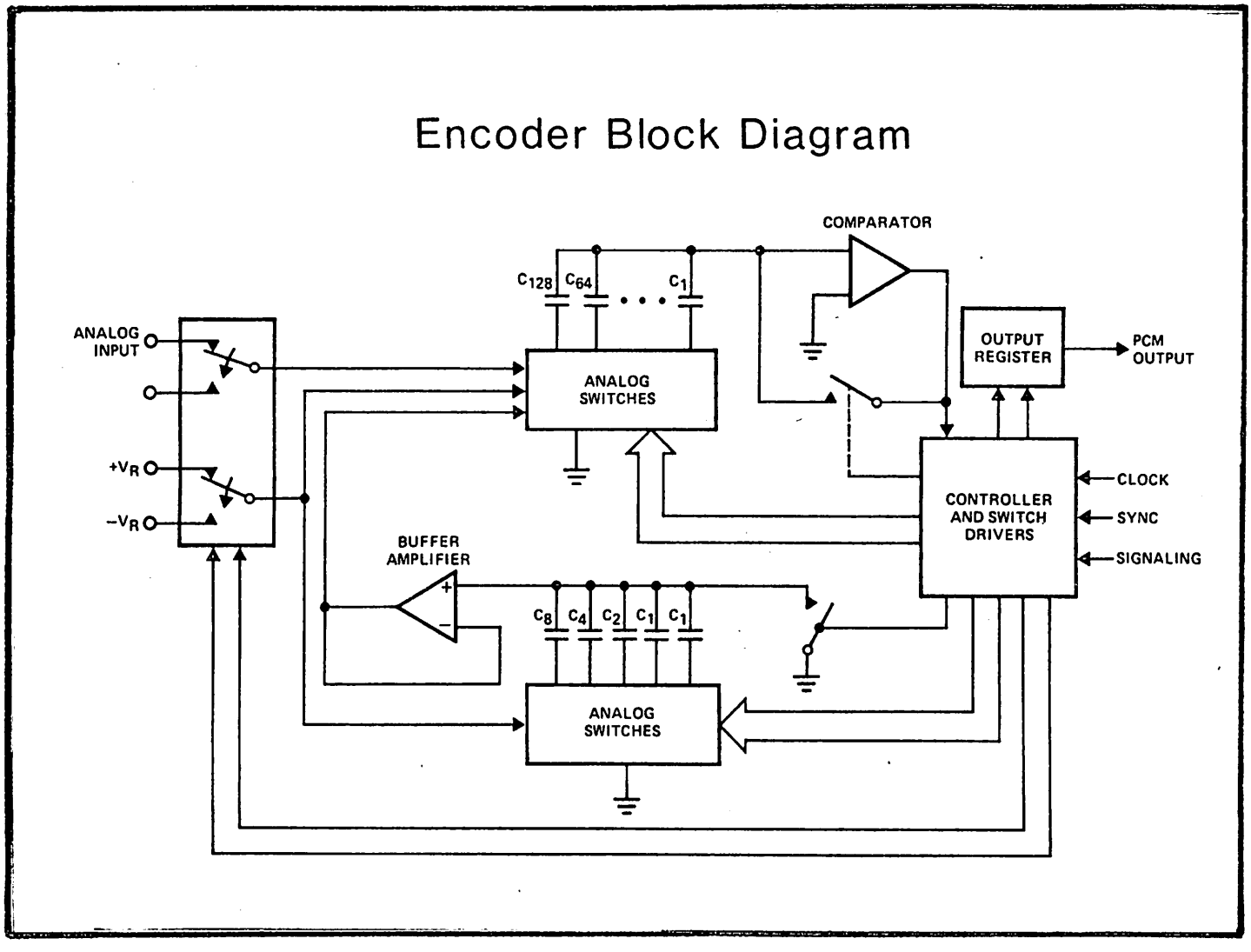

Encoder Block Diagram
COMPARATOR
C128
C64
C1
ANALOG INPUT
+VR
-VR
ANALOG SWITCHES
OUTPUT REGISTER
PCM OUTPUT
CONTROLLER AND SWITCH DRIVERS
CLOCK
SYNC
SIGNALING
BUFFER AMPLIFIER
C8
C4
C2
C1
C1
ANALOG SWITCHES

Figure 2.2

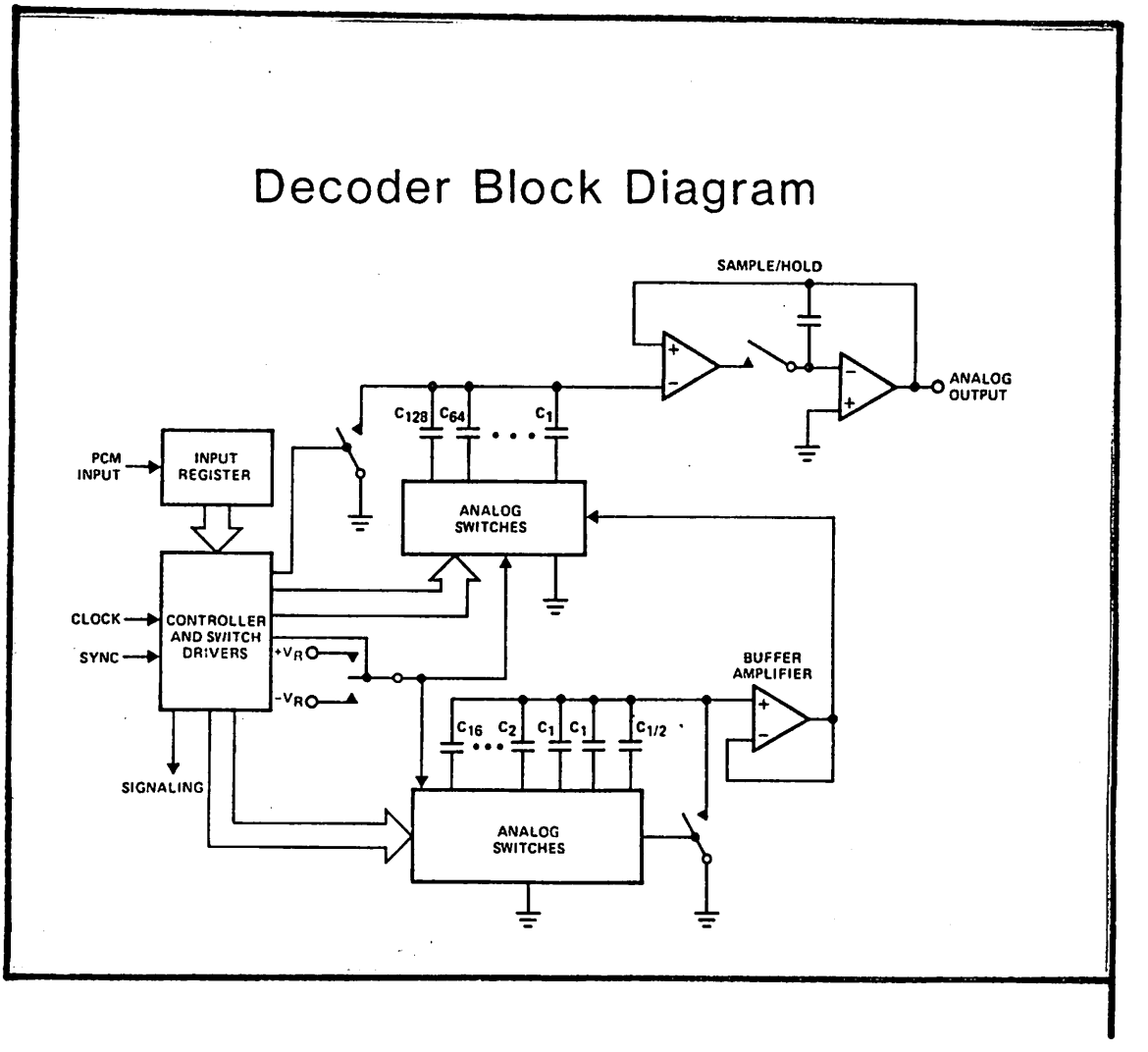

Decoder Block Diagram
SAMPLE/HOLD
ANALOG OUTPUT
PCM INPUT
INPUT REGISTER
C128
C64
C1
ANALOG SWITCHES
CLOCK
SYNC
CONTROLLER AND SWITCH DRIVERS
+VR
-VR
BUFFER AMPLIFIER
C16
C2
C1
C1
C1/2
SIGNALING
ANALOG SWITCHES

Figure 2.3

The corresponding analog voltage is then set up by closing the appropriate switches. This voltage is initially set up at the top plates of the segment capacitors while the internal switch of the sample and hold amplifier is still open. The switch is closed after a short time necessary for charge redistribution and the analog voltage is presented at the S/H amplifier output. The sampling switch is kept closed for about 12.95μs but the amplifier will settle much faster. The amplifier is then put into hold until the occurence of an other SYNC pulse. With the timing circuitry that was built in, the decoder can handle up to 4 channels if "synched" 4 times during a frame; this corresponds also to a sampling rate of 32kHz.

The critical circuit elements of the codec pair will be analized in the next chapter.

# CHAPTER 3

## 3.1 THE CAPACITOR ARRAYS.

It has been mentioned earlier that the performance of a PCM codec is evaluated mainly in terms of signal-to-noise ratio (SNR) and gain tracking (GTRCK).

Assuming that electrical and dynamic conditions are satisfied, the only element that will influence the SNR and GTRCK values is the shape of the transfer curve implemented by the codec. This shape in turn is determined by capacitor ratios, the offset voltages and gains of the buffers used in both the coder and the decoder.

This section is concerned with the requirements imposed on capacitor matching - one of the most important ingredients to the success of the conversion scheme.

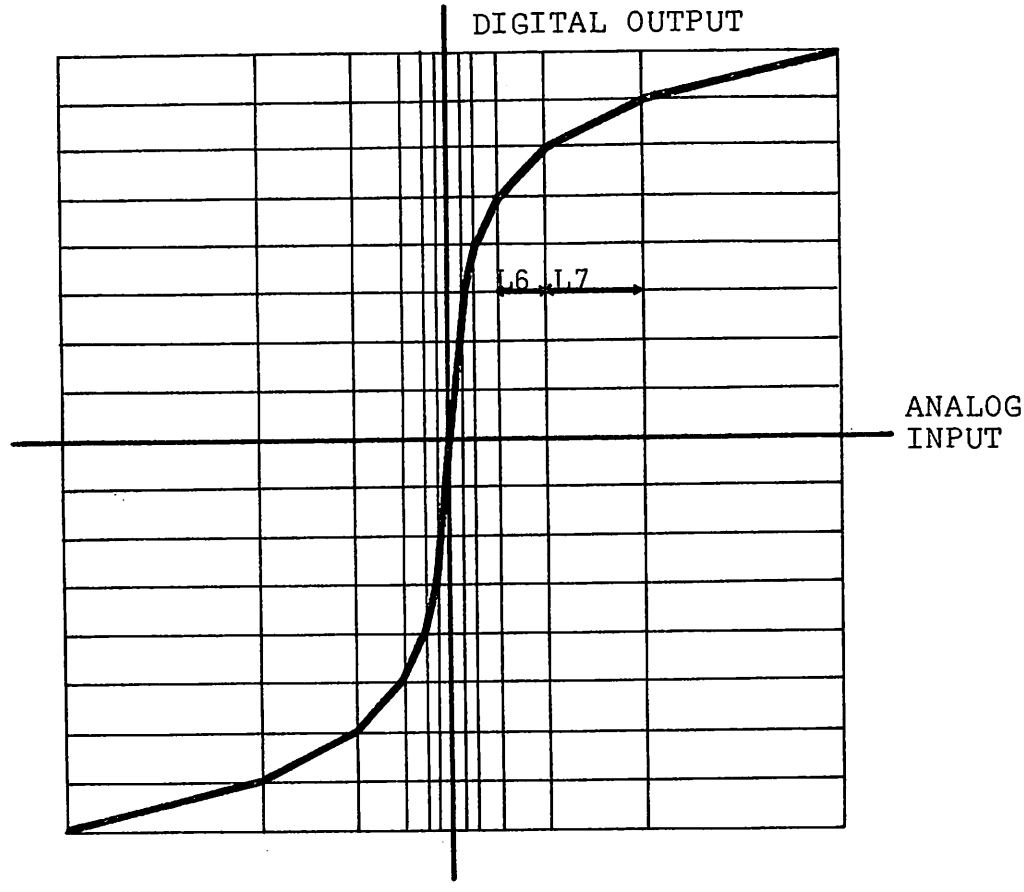
### 3.1.1 The relation between the shape of the transfer curves and capacitor matching.

An important ( and decisive for practicality ) feature of the conversion scheme is the fact that the capacitors in the segmentarrays do not have to be matched with the capacitors in the step arrays; the reason for the validity of this statement is that the end points of the segments are determined solely by the capacitors in the segment array and the step length ratios within a segment are determined solely by the step array capacitors. Exceptions to this rule are caused by some nonideal parameters such as buffer offset voltage and buffer gain. These imperfections will alter the ratio of either the first or last step to any other step within a segment and

they will also affect the segment ratio in the decoder. It may be noted though that these exceptions do not conflict with the statement about matching, they merely qualify the interpretation of the segment or step ratios. The relation between capacitor ratios and the shape of the transfer curves is illustrated in Figures 3.1 to 3.3 by means of examples; the L´s refer to the length of the segments or respectively steps.

For the implementation of the μ255 companding law the ideal length ratio between consecutive segments is 2. In the coder the 16 steps within a segment should be equal and in the decoder the last step in every segment should be 1.5 times longer than any one of the other 15 steps. Deviations from these ideal values will result in SNR and GTRCK values that are worse than the theoretical limits attainable with a perfect codec. A practical codec yielding SNR and GTRCK values that lie within some range of the ideal values will be acceptable as long as this range does not exceed the margins specified by the telecommunication industry.

The question then is: how much deviation from the ideal capacitor ratios is tollerable before the codec fails to pass SNR and GTRCK specifications? This question has to be answered before any attempt is made towards practical implementation; as a consequence the effect of nonideal capacitor ratios (as well as that of other nonidealities) on the SNR and GTRCK performance has to be evaluated via simulation.

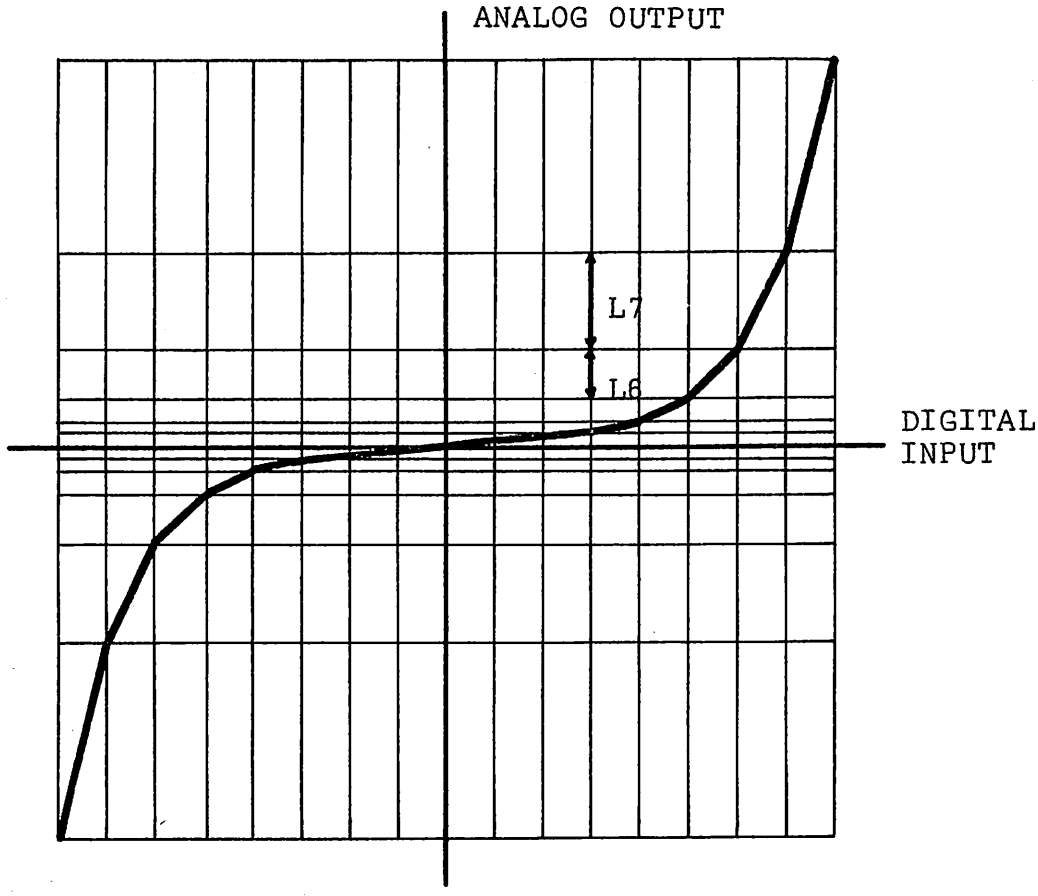



$$\frac{L7}{L6} = \frac{CX64}{CX32}$$

L6 is measured in voltage units from the beginning of the sixth segment to the beginning of the seventh segment. The beginning of the sixth segment is the voltage at which the code 10101111 starts to occur when the transfer curve is scanned from left to right or the code 10110000 starts to occur when the transfer curve is scanned from right to left. The beginning of the seventh segment is defined in a similar manner (10011111, left to right, 10100000, right to left); etc.

Segment capacitor matching in the coder.

Figure 3.1



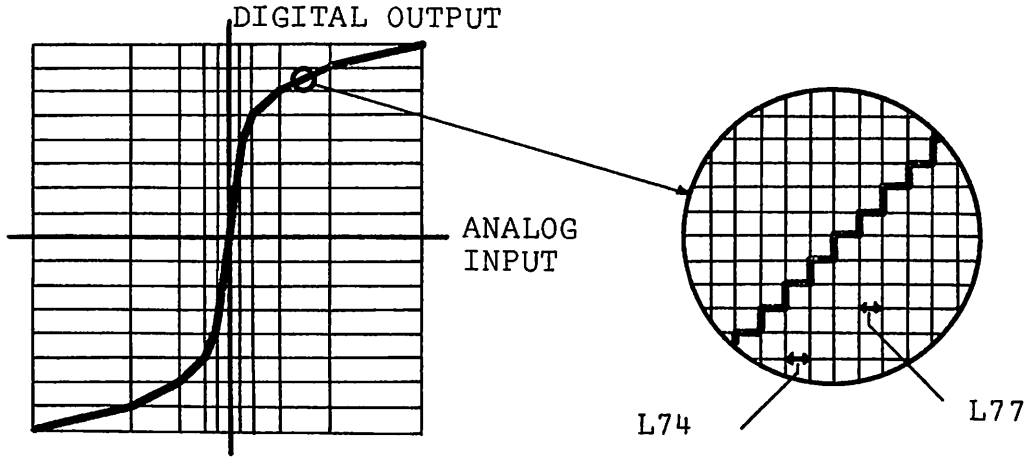

$$\frac{L7}{L6} = \frac{CX64}{CX32} * \frac{1 + \frac{CX128}{CX64} * \frac{VOSAY}{VREF-VOSAY}}{1 + \frac{CX64}{CX32} * \frac{VOSAY}{VREF-VOSAY}}$$

L6 is measured in voltage units and is the difference between the output voltage corresponding to the code 10011111 and the output voltage corresponding to the code 10101111; etc.

VOSAY is the offset voltage of the step array buffer.

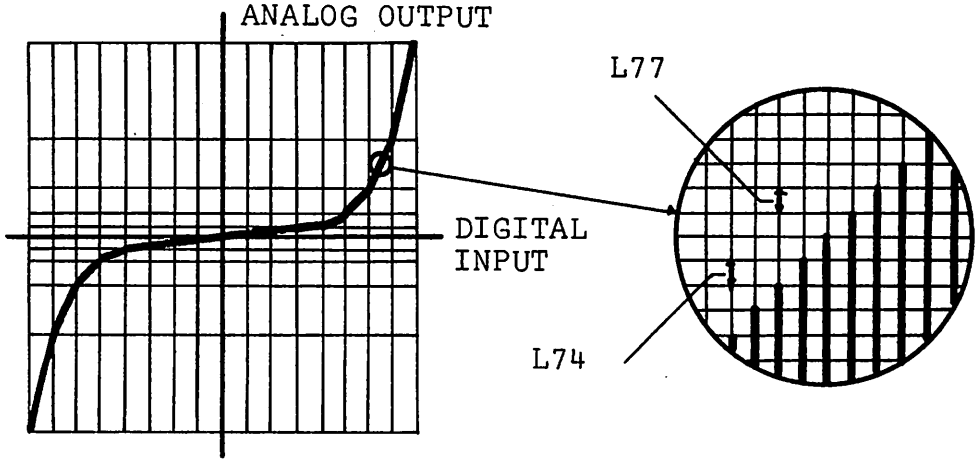
Segment capacitor matching in the decoder.

Figure 3.2




$$\frac{L77}{L74} = \frac{CY1}{CY4-CY2-CY1}$$

L74 is measured in voltage units from the beginning of the fourth step in the seventh segment to the beginning of the next step. The beginning of the fourth step is the voltage at which the code 10011011 starts to occur for left to right scanning or the code 10011100 starts to occur for right to left scanning; etc.




$$\frac{L77}{L74} = \frac{CY1}{CY4-CY2-CY1}$$

L74 is measured in voltage units and is the difference between the output voltage corresponding to code 10011011 and the output voltage corresponding to code 10011100; etc.

Step capacitor matching in the coder (top) and in the decoder (bottom).

Figure 3.3

The tool for such a simulation has been created by Y. P. Tsividis (7); it is XCODEC - a computer program for the evaluation of companded PCM codecs and it is based on a statistical approach to the coding process.

The analysis is static in the sense that a codec is characterized solely through the dc transfer curves of the compressing ADC and the expanding DAC. This is in agreement with the earlier statement that the shape of the transfer curve alone will determine the SNR and GTRCK performance.

This shape in turn should depend only on static parameters such as capacitor ratios and amplifier imperfections.

The influence of dynamic and electrical factors on the shape of the transfer curve can be eliminated, or at least minimized, through proper circuit design and will be treated later.

The transfer curves used by XCODEC have to be supplied by the user via appropriate subroutines. XCODEC will then use these transfer curves to simulate SNR and GTRCK testing procedures and provide outputs similar to the ones that would be obtained in an actual practical evaluation of a codec. The SNR and GTRCK values are compared against the spec limits and any failure is signaled through an appropriate message.

Sample outputs obtained from XCODEC are shown in the Appendix.

Since the relation between the static parameters (capacitor ratios, offset voltages, etc. ) and the shape of the transfer curve is straightforward it turns out that

XCODEC can be used to evaluate the influence of any one imperfection on the performance of the codec. Due to the complexity of the relation between the transfer curve and the SNR and GTRCK performance it is difficult to determine combinations of acceptable maximal imperfections. On the other hand it is easy to keep all but one of the parameters ideal and then find the maximum acceptable deviation for that single parameter. The collection of these individual parameter deviations can then be used as a guide for the construction of a set of possible multiple parameter deviations; in this way one can evaluate the sensitivity of the codec to more than one imperfection.

The iteration process used to find the maximum acceptable single parameter deviation can be incorporated into XCODEC as a semiautomated search routine. Such a routine is described in the appendix containing the XCODEC users manual.

### 3.1.2 Maximal individual capacitor deviations from ideal values.

Since the absolute magnitude of the capacitance is irrelevant from a matching point of view (not in practice) one can describe the capacitor arrays by means of normalized capacitors. In this context the ideal values of the capacitors would be:

- in the coder and decoder segment arrays:

CX1=1/255; CX2=2/255; CX4=4/255; CX8=8/255; CX16=16/255; CX32=32/255; CX64=64/255; CX128=128/255;

CXTOT=CX1+CX2+...+CX128=1

CXP (parasitic) = 0% of CXTOT = 0%

- in the coder step array

CY1=1/16; CY2=2/16; CY4=4/16; CY8=8/16;

CYTM (terminal) =1/16

CYTOT=CY1+CY2+...+CYTM=1

CYP=0% of CYTOT = 0%

- in the decoder step array

CYHS (halfstep) = 1/33; CY1=2/33; CY2=4/33; CY4=8/33;

CY8=16/33;

CYTOT=CYHS+CY1+...+CYTM=1

CYP=0% of CYTOT = 0%

Deviations of the capacitors from their ideal values will alter the individual capacitors but will not affect the total normalized capacitance of an array. This definition reflects the fact that an array acts as a divider in which the only relevant thing is the ratio between the capacitance of the individual components and the total capacitance of the array. Therefore no matter how distorted the individual members of the array are in absolute value, their sum can still be considered as equal to 1; the distortions merely act on the redistribution of the individual ratios.

Mathematically these statements are expressed as follows:

- in the coder and decoder segment arrays

CX1(1+dCX1)+CX2(1+dCX2)+...+CX128(1+dCX128)=1

where CX1, CX2, etc. are the ideal values of the components

and dCX1, dCX2, etc. are the deviations of those components from their ideal values. It follows that:

$$CX1 \times dCX1 + CX2 \times dCX2 + \ldots + CX128 \times dCX128 = 0$$

or: $dCX1 + 2dCX2 + \ldots + 128dCX128 = 0$

- in the coder step array:

$$CY1(1+dCY1) + CY2(1+dCY2) + \ldots + CYTM(1+dCYTM) = 1$$

or: $CY1 \times dCY1 + CY2 \times dCY2 + \ldots + CYTM \times dCYTM = 0$

or: $dCY1 + 2dCY2 + \ldots + dCYTM = 0$

- in the decoder step array:

$$CYHS(1+dCYHS) + CY1(1+dCY1) + \ldots + CYTM(1+dCYTM) = 1$$

or: $CYHS \times dCYHS + CY1 \times dCY1 + \ldots + CYTM \times dCYTM = 0$

or: $dCYHS + 2dCY1 + \ldots + 2dCYTM = 0$

As a result of these bounding relations if one capacitor deviates from its ideal value then at least one other capacitor will deviate in the opposite sens in order to maintain the balance. In the case of individual parameter deviations only one of the capacitors will be "deliberately" altered.

Thus for example if dCX1 = 1% then:

$$dCX2 = dCX4 = \ldots = dCX128 = -(1\%)/254 = -0.004\%$$

In other words CX2, CX4, etc. up to CX128 are matched among themselves but are not matched with CX1. Therefore the individual parameter deviation analysis will show how far one single capacitor can be out of line before the codec fails to pass SNR and GTRCK specs. The results of such tests performed for all the capacitors in all the arrays are shown in TABLES 3.1 to 3.4. The other factors influencing the shape of the transfer curve have been considered ideal.

Maximal individual positive deviations of coder capacitors using a perfect decoder (%).

| dCX1 | dCX2 | dCX4 | dCX8 | dCX16 | dCX32 | dCX64 | dCX128 |
|---|---|---|---|---|---|---|---|
| 3.38 | - 0.01 | - 0.01 | - 0.01 | - 0.01 | - 0.01 | - 0.01 | - 0.01 |
| - 0.06 | 7.99 | - 0.06 | - 0.06 | - 0.06 | - 0.06 | - 0.06 | - 0.06 |
| - 0.19 | - 0.19 | 11.63 | - 0.19 | - 0.19 | - 0.19 | - 0.19 | - 0.19 |
| - 0.43 | - 0.43 | - 0.43 | 13.36 | - 0.43 | - 0.43 | - 0.43 | - 0.43 |
| - 1.19 | - 1.19 | - 1.19 | - 1.19 | 17.81 | - 1.19 | - 1.19 | - 1.19 |
| - 2.65 | - 2.65 | - 2.65 | - 2.65 | - 2.65 | 18.44 | - 2.65 | - 2.65 |
| - 3.71 | - 3.71 | - 3.71 | - 3.71 | - 3.71 | - 3.71 | 11.06 | - 3.71 |
| -11.15 | -11.15 | -11.15 | -11.15 | -11.15 | -11.15 | -11.15 | 11.06 |

| dCY1 | dCY2 | dCY4 | dCY8 | dCYTM | CYP |
|---|---|---|---|---|---|
| 65.6 | - 4.4 | - 4.4 | - 4.4 | - 4.4 | 0 |
| - 4.7 | 33.1 | - 4.7 | - 4.7 | - 4.7 | 0 |
| - 5.7 | - 5.7 | 17.2 | - 5.7 | - 5.7 | 0 |
| - 7.7 | - 7.7 | - 7.7 | 7.7 | - 7.7 | 0 |
| -12.9 | -12.9 | -12.9 | -12.9 | 206.3 | 0 |
| 0 | 0 | 0 | 0 | 0 | 15.9 |

TABLE 3.1

Maximal individual negative deviations of coder capacitors using a perfect decoder (%).

| dCX1 | dCX2 | dCX4 | dCX8 | dCX16 | dCX32 | dCX64 | dCX128 |
|---|---|---|---|---|---|---|---|
| -13.28 | 0.05 | 0.05 | 0.05 | 0.05 | 0.05 | 0.05 | 0.05 |
| 0.08 | -10.63 | 0.08 | 0.08 | 0.08 | 0.08 | 0.08 | 0.08 |
| 0.19 | 0.19 | -12.19 | 0.19 | 0.19 | 0.19 | 0.19 | 0.19 |
| 0.44 | 0.44 | 0.44 | -13.59 | 0.44 | 0.44 | 0.44 | 0.44 |
| 1.07 | 1.07 | 1.07 | 1.07 | -15.94 | 1.07 | 1.07 | 1.07 |
| 1.70 | 1.70 | 1.70 | 1.70 | 1.70 | -11.88 | 1.70 | 1.70 |
| 2.07 | 2.07 | 2.07 | 2.07 | 2.07 | 2.07 | - 6.19 | 2.07 |
| 13.04 | 13.04 | 13.04 | 13.04 | 13.04 | 13.04 | 13.04 | -12.94 |

| dCY1 | dCY2 | dCY4 | dCY8 | dCYTM |
|---|---|---|---|---|
| -66.0 | 4.4 | 4.4 | 4.4 | 4.4 |
| 5.4 | -37.5 | 5.4 | 5.4 | 5.4 |
| 5.1 | 5.1 | -15.3 | 5.1 | 5.1 |
| 9.4 | 9.4 | 9.4 | - 9.4 | 9.4 |
| 4.5 | 4.5 | 4.5 | 4.5 | -71.9 |

TABLE 3.2

Maximal individual positive deviations of decoder capacitors using a perfect coder (%).

| dCX1 | dCX2 | dCX4 | dCX8 | dCX16 | dCX32 | dCX64 | dCX128 |
|---|---|---|---|---|---|---|---|
| 14.69 | - 0.06 | - 0.06 | - 0.06 | - 0.06 | - 0.06 | - 0.06 | - 0.06 |
| - 0.09 | 11.72 | - 0.09 | - 0.09 | - 0.09 | - 0.09 | - 0.09 | - 0.09 |
| - 0.21 | - 0.21 | 13.31 | - 0.21 | - 0.21 | - 0.21 | - 0.21 | - 0.21 |
| - 0.49 | - 0.49 | - 0.49 | 15.23 | - 0.49 | - 0.49 | - 0.49 | - 0.49 |
| - 1.17 | - 1.17 | - 1.17 | - 1.17 | 17.50 | - 1.17 | - 1.17 | - 1.17 |
| - 2.24 | - 2.24 | - 2.24 | - 2.24 | - 2.24 | 15.63 | - 2.24 | - 2.24 |
| - 2.64 | - 2.64 | - 2.64 | - 2.64 | - 2.64 | - 2.64 | 7.88 | - 2.64 |
| -11.34 | -11.34 | -11.34 | -11.34 | -11.34 | -11.34 | -11.34 | 11.25 |

| dCYHS | dCY1 | dCY2 | dCY4 | dCY8 | dCYTM | CYP |
|---|---|---|---|---|---|---|
| 187.5 | - 5.9 | - 5.9 | - 5.9 | - 5.9 | - 5.9 | 0 |
| - 4.4 | 67.8 | - 4.4 | - 4.4 | - 4.4 | - 4.4 | 0 |
| - 4.1 | - 4.1 | 30.0 | - 4.1 | - 4.1 | - 4.1 | 0 |
| - 5.7 | - 5.7 | - 5.7 | 17.8 | - 5.7 | - 5.7 | 0 |
| - 7.4 | - 7.4 | - 7.4 | - 7.4 | 7.9 | - 7.4 | 0 |
| - 5.7 | - 5.7 | - 5.7 | - 5.7 | - 5.7 | 89.1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 6.1 |

TABLE 3.3

Maximal individual negative deviations of decoder capacitors using a perfect coder (%).

| dCX1 | dCX2 | dCX4 | dCX8 | dCX16 | dCX32 | dCX64 | dCX128 |
|---|---|---|---|---|---|---|---|
| - 4.53 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 |
| 0.06 | - 7.03 | 0.06 | 0.06 | 0.06 | 0.06 | 0.06 | 0.06 |
| 0.18 | 0.18 | -11.44 | 0.18 | 0.18 | 0.18 | 0.18 | 0.18 |
| 0.44 | 0.44 | 0.44 | -13.59 | 0.44 | 0.44 | 0.44 | 0.44 |
| 1.13 | 1.13 | 1.13 | 1.13 | -16.88 | 1.13 | 1.13 | 1.13 |
| 2.51 | 2.51 | 2.51 | 2.51 | 2.51 | -17.50 | 2.51 | 2.51 |
| 3.46 | 3.46 | 3.46 | 3.46 | 3.46 | 3.46 | -10.31 | 3.46 |
| 14.17 | 14.17 | 14.17 | 14.17 | 14.17 | 14.17 | 14.17 | -14.06 |

| dCYHS | dCY1 | dCY2 | dCY4 | dCY8 | dCYTM |
|---|---|---|---|---|---|
| -100.0 | 3.1 | 3.1 | 3.1 | 3.1 | 3.1 |
| 3.7 | -57.0 | 3.7 | 3.7 | 3.7 | 3.7 |
| 4.2 | 4.2 | -30.6 | 4.2 | 4.2 | 4.2 |
| 5.4 | 5.4 | 5.4 | -16.9 | 5.4 | 5.4 |
| 9.4 | 9.4 | 9.4 | 9.4 | - 9.9 | 9.4 |
| 6.5 | 6.5 | 6.5 | 6.5 | 6.5 | -100.0 |

TABLE 3.4

### 3.1.3 Combinations of capacitor nonidealities.

Once the maximal individual capacitor deviations are known one can use these as a guide and check the performance of the codec in the presence of more than one nonideality. The results of such tests are shown in Figures 3.4 to 3.6; they correspond to the codec descriptions given in TABLE 3.5. The amplifier nonidealities used for these evaluations are comparable to practically realizable values.

Parameters that have no influence on the SNR and GTRCK performance of the codec have been kept ideal.Such parameters are the parasitic capacitance in the segment arrays of both the coder and decoder, the offset and gain of the output buffer in the decoder and the gain of the amplifiers associated with the step arrays. This last parameter can in fact influence the performance of the codec but the practical gain of such a buffer is sufficiently close to unity and therefore it can be considered perfect for the purpose of the present analysis.

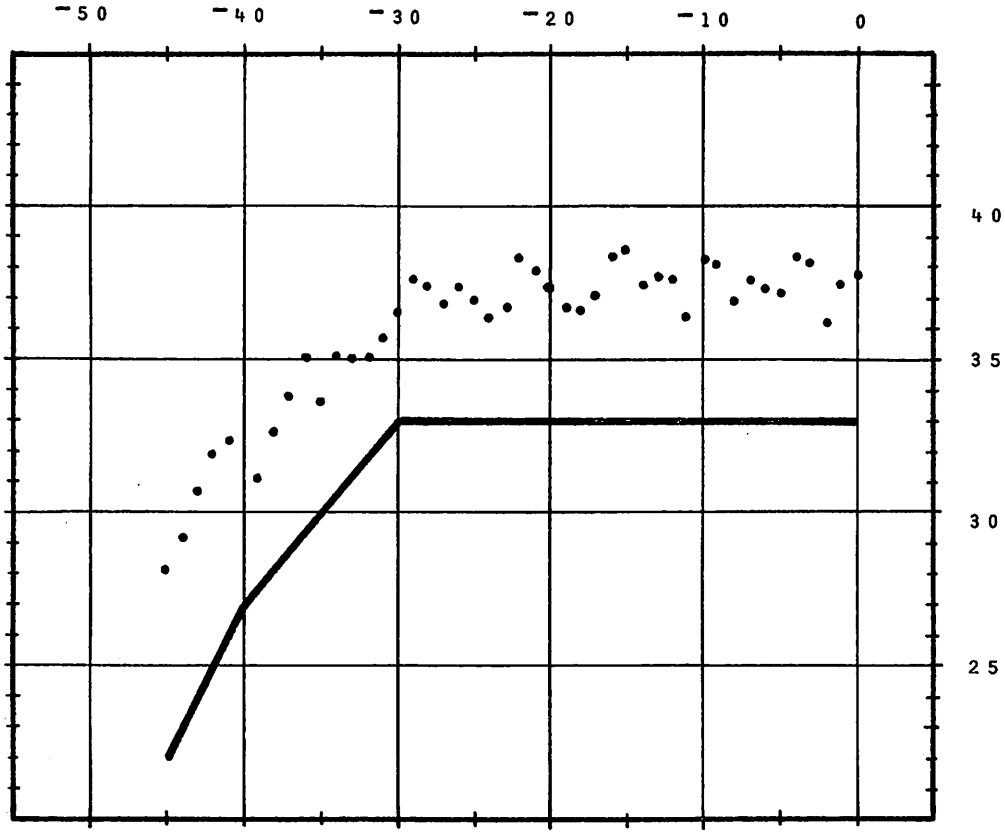
The capacitor deviations listed in TABLE 3.5 were chosen in a manner that yields a "wavy" overall codec transfer curve such that the decoder nonidealities acentuate the coder imperfections.

The results of this multiple deviation analysis are somewhat puzzling in as far as the mismatch between CX1 and at least half of the capacitors in each segment array is larger in TABLE 3.5 than in TABLE 3.1 and respectively 3.4.

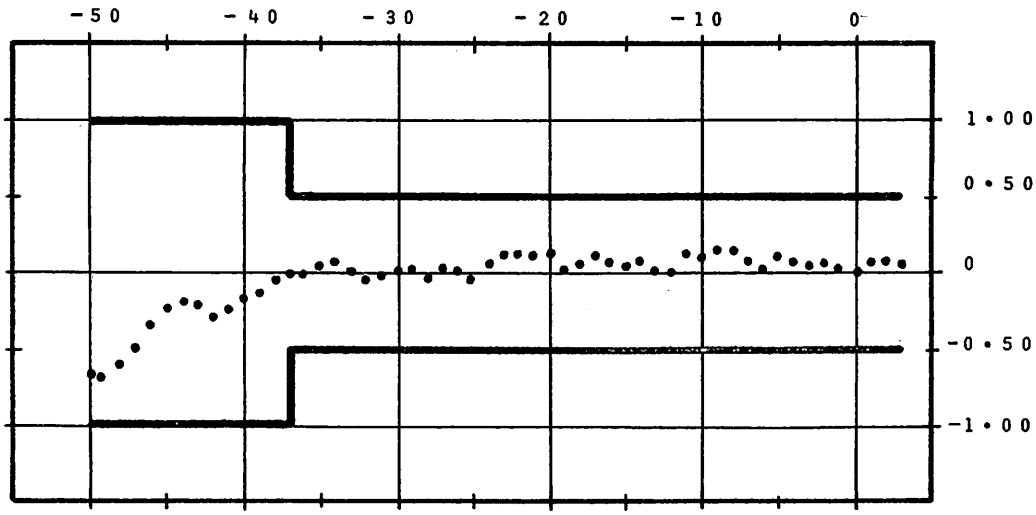
| Coder nonidealities | (a) | (b) | (c) |
|---|---|---|---|
| dCX1 | 1.00% | 2.00% | 3.00% |
| dCX2 | -1.00% | -2.00% | -3.00% |
| dCX4 | 1.00% | 2.00% | 3.00% |
| dCX8 | -1.00% | -2.00% | -3.00% |
| dCX16 | 1.00% | 2.00% | 3.00% |
| dCX32 | -1.00% | -2.00% | -3.00% |
| dCX64 | 1.00% | 2.00% | 3.00% |
| dCX128 | -0.34% | -0.67% | -1.01% |
| dCY1 | 5.00% | 5.00% | 5.00% |
| dCY2 | -5.00% | -5.00% | -5.00% |
| dCY4 | 5.00% | 5.00% | 5.00% |
| dCY8 | -1.25% | -1.25% | -1.25% |
| dCYTM | -5.00% | -5.00% | -5.00% |
| CYP | 2.00% | 2.00% | 2.00% |
| VOSC (% of VR) | -0.10% | -0.10% | -0.10% |
| VOSA (% Of VR) | 1.00% | 1.00% | 1.00% |
| **Decoder nonidealities** | | | |
| dCX1 | -1.00% | -2.00% | -3.00% |
| dCX2 | 1.00% | 2.00% | 3.00% |
| dCX4 | -1.00% | -2.00% | -3.00% |
| dCX8 | 1.00% | 2.00% | 3.00% |
| dCX16 | -1.00% | -2.00% | -3.00% |
| dCX32 | 1.00% | 2.00% | 3.00% |
| dCX64 | -1.00% | -2.00% | -3.00% |
| dCX128 | 0.34% | 0.67% | 1.01% |
| dCY1 | -5.00% | -5.00% | -5.00% |
| dCY2 | 5.00% | 5.00% | 5.00% |
| dCY4 | -5.00% | -5.00% | -5.00% |
| dCYHS | -5.00% | -5.00% | -5.00% |
| dCYTM | 5.00% | 5.00% | 5.00% |
| dCY8 | 1.56% | 1.56% | 1.56% |
| CYP | 1.00% | 1.00% | 1.00% |
| VOSAY (% of VR) | -1.00% | -1.00% | -1.00% |

Codec nonidealities corresponding to SNR and GTRCK curves shown in Figures 3.4 to 3.6.

TABLE 3.5

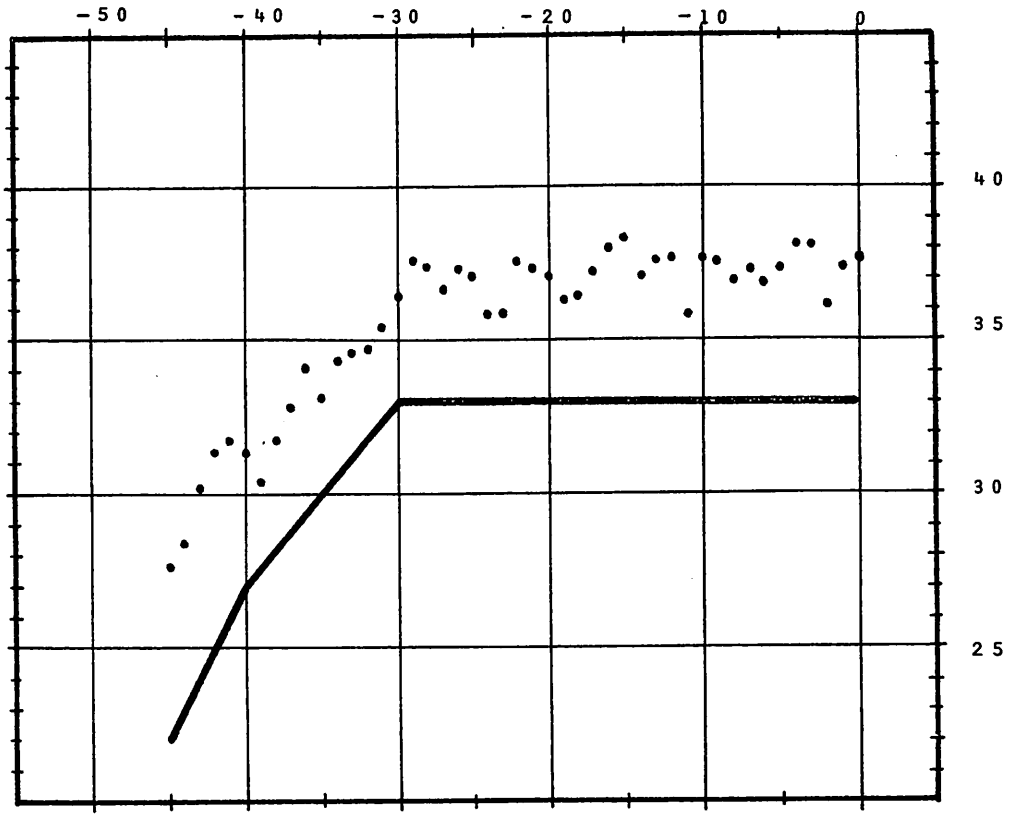



(a) Signal-to-distortion ratio for the codec described in TABLE 3.5a.
Input level (horizontal axis) and SNR (vertical axis) are expressed in dB's.

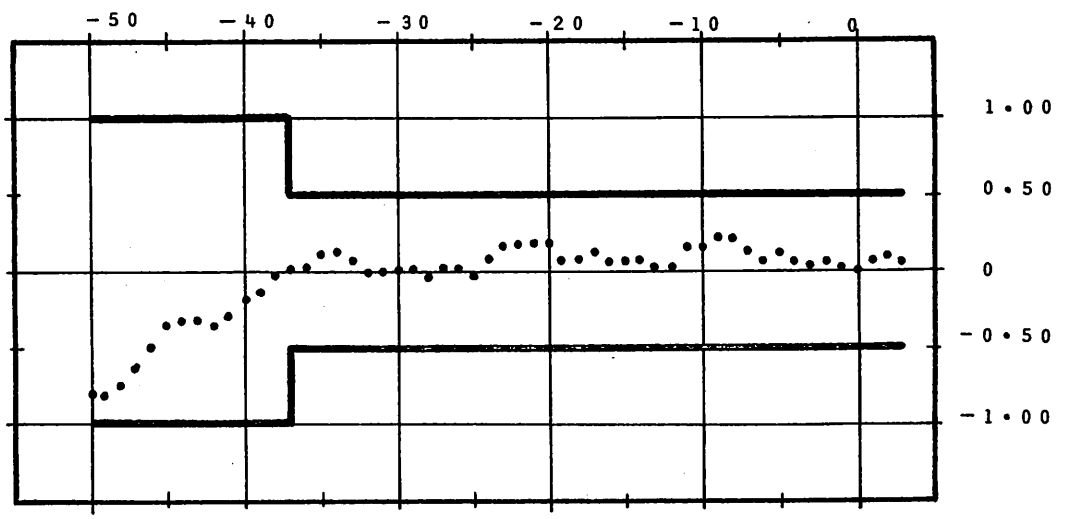



(b) Gain tracking for the codec described in TABLE 3.5a
Input level (horizontal axis) and GTRCK (vertical axis) are expressed in dB's.

Figure 3.4

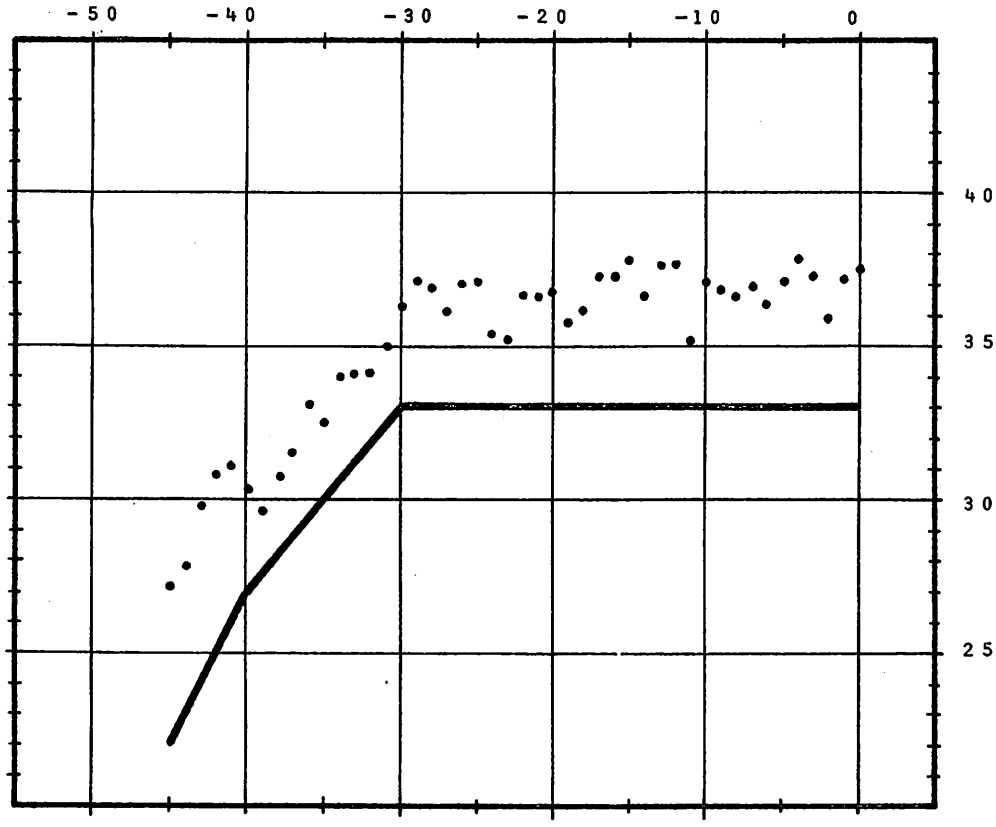



(a) Signal-to-distortion ratio for the codec described in TABLE 3.5b.
Input level (horizontal axis) and SNR (vertical axis) are expressed in dB's.

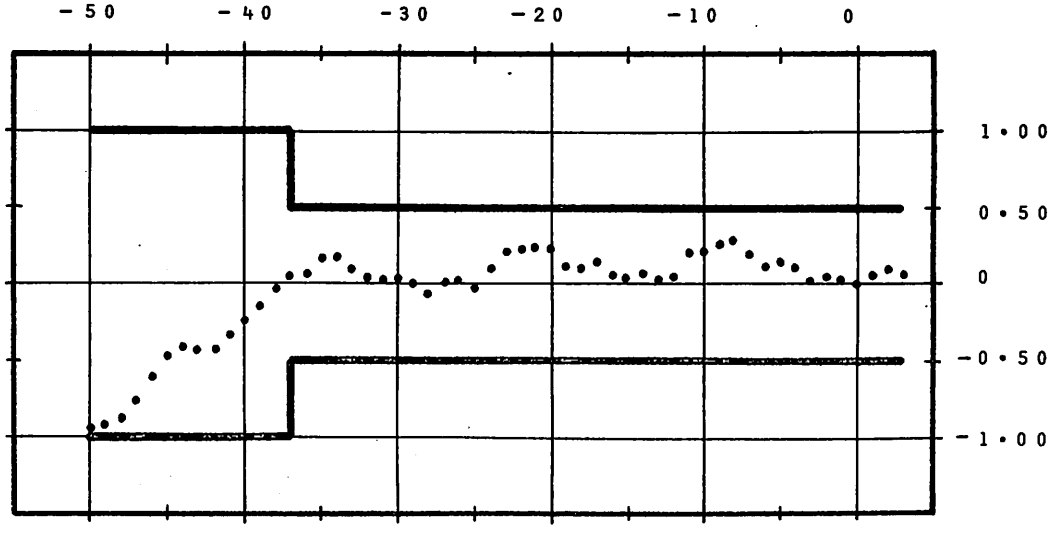



(b) Gain tracking for the codec described in TABLE 3.5b. Input level (horizontal axis) and GTRCK (vertical axis) are expressed in dB's.

Figure 3.5




(a) Signal-to-distortion ratio for the codec described in TABLE 3.5c.
Input level (horizontal axis) and SNR (vertical axis) are expressed in dB's.




(b) Gain tracking for the codec described in TABLE 3.5c. Input level (horizontal axis) and GTRCK (vertical axis) are expressed in dB's.

Figure 3.6

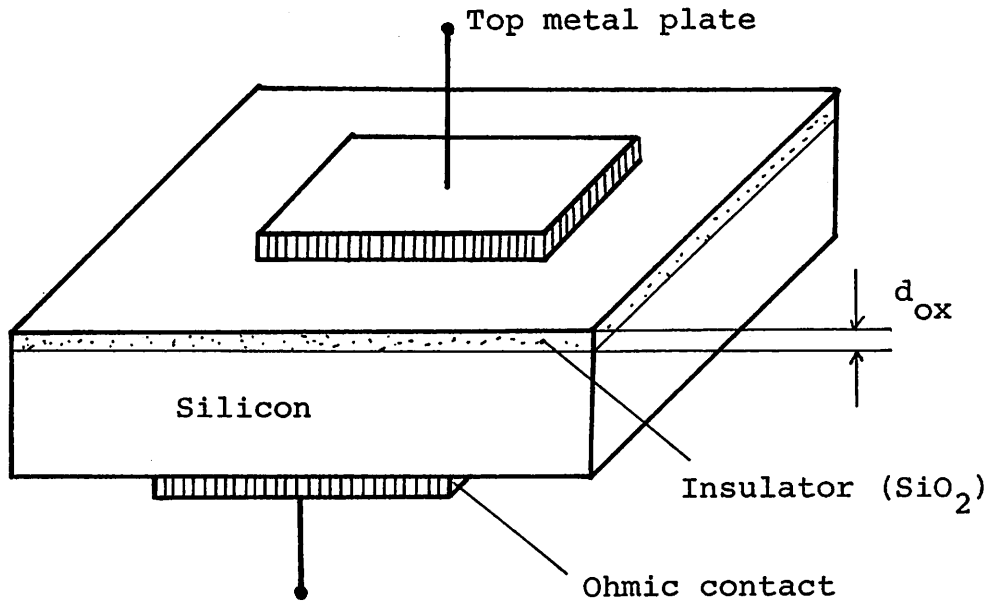
### 3.1.4 Practical methods for the implementation of matched MOS capacitors.

The methods for building matched MOS capacitors in integrated circuits have been described by J. L. McCreary (8). They will be repeated here for the sake of completeness.

The classical MOS capacitor structure is illustrated in its crudest form in Figure 3.7a and the electrical behavior of this device is described in Figures 3.7b and 3.8. The MOS structure has been the object of innumerable investigations reported in a comparable number of papers; therefore it is believed that the two figures mentioned before do suffice for the purpose of the present discussion without further elaboration. References (14) and (15) can be used for a more complete description.

From Figure 3.7b it is apparent that for a given process the ratio of two capacitors is equal to the ratio of the areas defining those two capacitors. The qualifier "for a given process" implies that the permittivity of the insulator, $\varepsilon_{ox}$, and the insulator thickness, $d_{ox}$, are constant across the capacitor array. Therefore the only parameter under the control of the circuit designer is the area of the capacitors. The following matching rules (8) apply for the case of capacitor matching through area ratioing.

1. If the capacitance ratio of two capacitors is m/n, where m and n are integers, then the two capacitors should




MOS capacitor structure

(a)


$C_{ox} = \frac{\varepsilon_{ox} \times A}{d_{ox}}$ ( Oxide capacitance)

$C_D = f(V)$ (Silicon space charge capacitance)

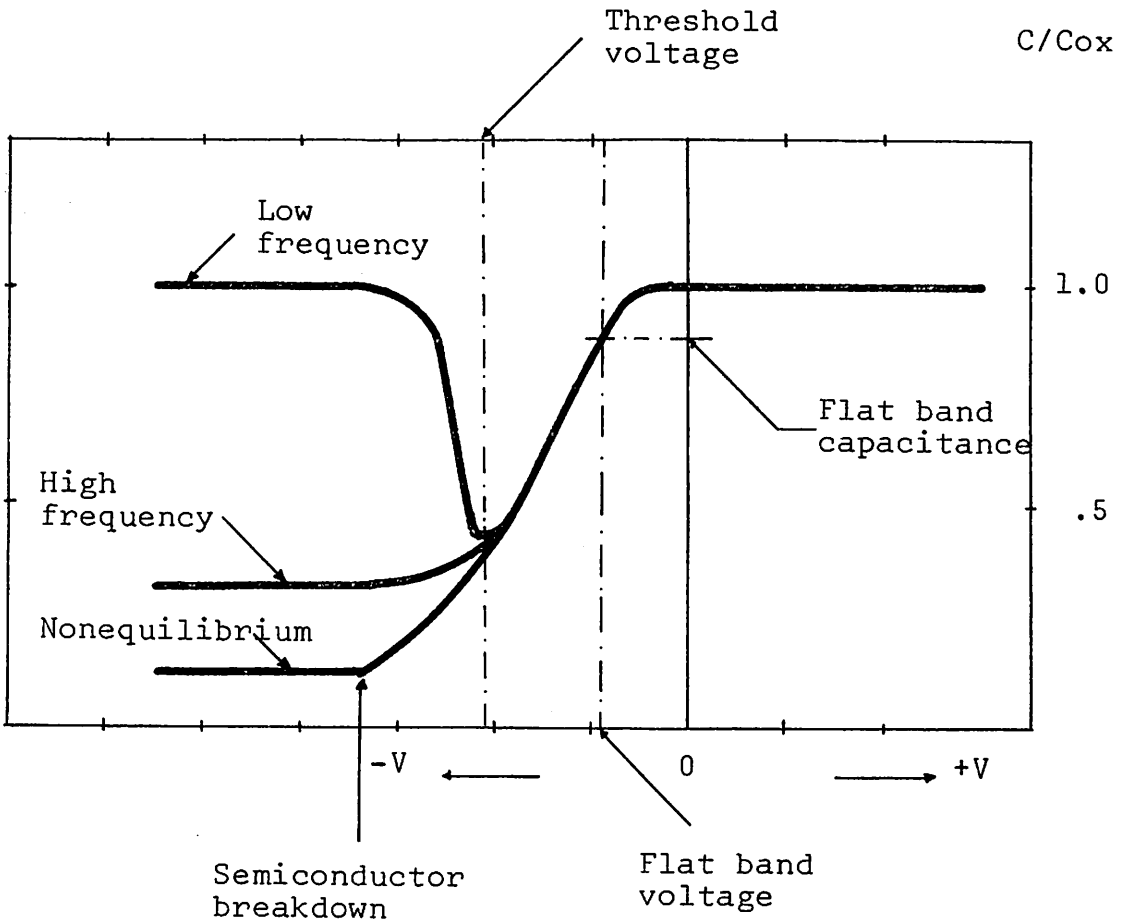
$C$ (MOS capacitance) $= \frac{C_{ox}\, C_D}{C_{ox} + C_D}$

$\frac{C}{C_{ox}} = \phi(V)$ is shown in Figure 3.8

MOS capacitance definition

(b)

Figure 3.7




MOS capacitance-voltage curves (qualitative).

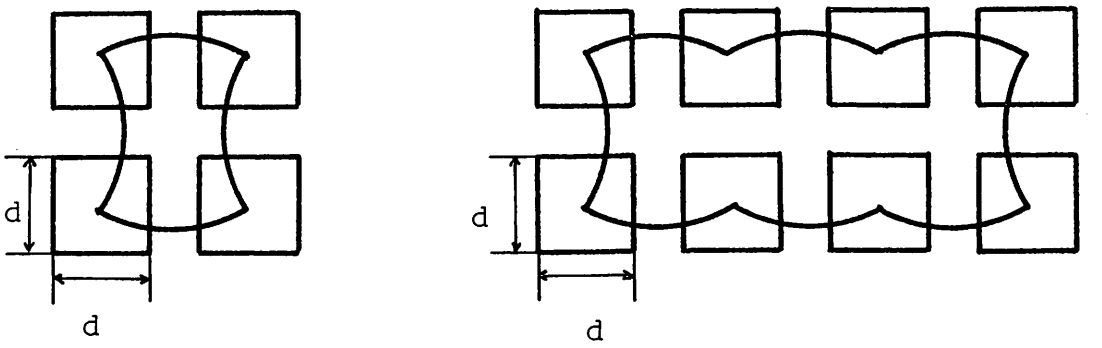
Figure 3.8

be built out of units such that the ratio between the number of units will be equal to m/n. This idea is illustrated in Figure 3.9a. Such an implementation will yield area ratios insensitive to the absolute value of the unit dimensions. This is in contrast to the case illustrated in Figure 3.9b; here the linear dimensions of the two capacitors are modified by the same amount in absolute value. The net result of this effect is the fact that the area ratio is a function of u, the "edge uncertainty".

In practice the different sized patterns defining the two areas may exhibit different "u"'s due to different etching conditions. Therefore it would be difficult and certainly impractical to base a design on the approach illustrated in Figure 3.9b.

2. The layout of the capacitors should be such that every single pattern defining the area will "see" the same surroundings. This is illustrated in Figure 3.10 for the case when the area is defined by the metal plate ( 8 ). In such a layout every capacitor will present the same etching front and the resulting linear dimensions are likely to be indeed the same for all the units.

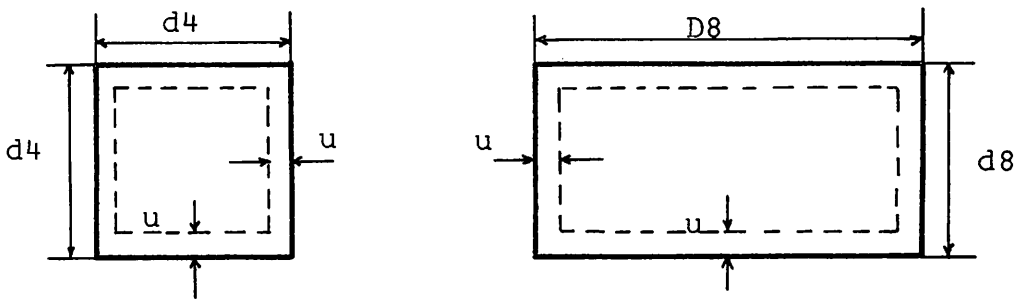
3. The capacitor layout should be insensitive to reasonable mask misalignment. The solution proposed in ( 8 ) is illustrated in the same Figure 3.10. In this implementation the top metal plate is allowed to shift on top of the thin oxide area. The capacitance will remain constant as long as the metal plate remains inside the thin oxide area.It can




$A4=4*d^2$ $A8=8*d^2$

A8/A4 = 2 (independent of d)

(a)



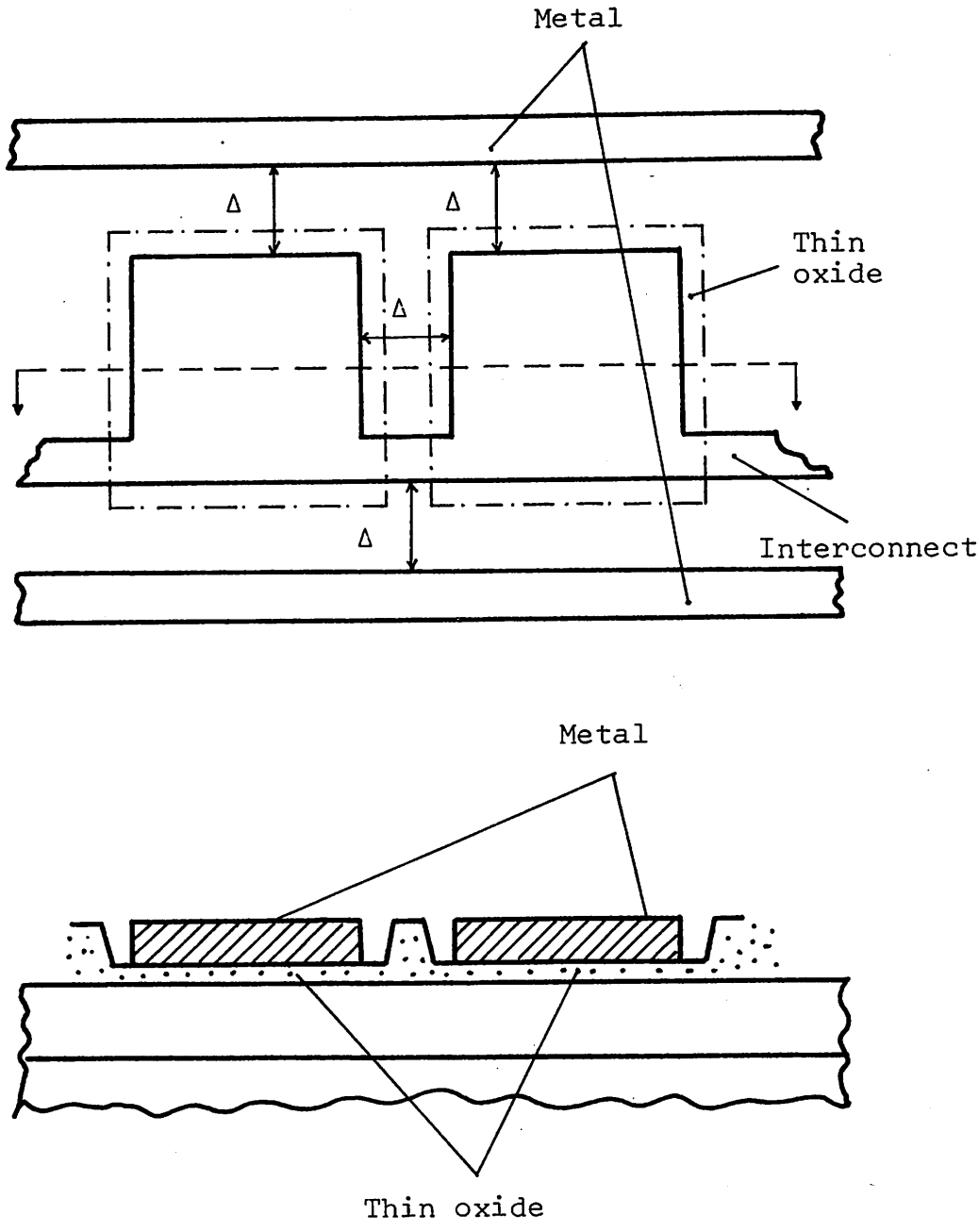

$A4=(d4-u)^2$ $A8=(D8-u)*(d8-u)$

d4=d8 A8/A4 = (D8-u)/(d4-u) = f(u)

(b)

Capacitor ratioing methods.

Figure 3.9




MOS capacitor.
(defined mainly by metal plate)

Figure 3.10

be seen that the contribution to the capacitance resulting from the interconnecting metal "stubs" is also constant as a consequence of the symmetrical layout.

4. If the matching of the capacitors is extremely critical then in order to eliminate the effect of long range oxide gradients the capacitors should be laid out in a centroid pattern. This idea is illustrated in ( 8 ).

3.1.5 Capacitor structure and layout for the PCM codec.

All the rules mentioned before, with the exception of rule No. 4, have been used in the course of the work being described here. Since the ultimate goal was to build a commercial product some of the detail choices made in ( 8 ) have been modified to suit the present case.

Rule No. 1 has been used to the fullest extent by building all the capacitors as multiples of the smallest capacitor in the particular array. Such a decision is justified from a yield point of view since it completely eliminates the influence of run to run variations in etching rates. This is particularly important in the PCM application since the allowable tolerance for the smallest capacitor in the segment arrays is much tighter than in the case of a linear converter - about 4% (PCM) compared to 50% (linear).

Application of rule No. 2 is a natural fallout from the extensive use of rule No. 1 since the capacitors can be arranged in a very regular array. As opposed to ( 8 ) it was

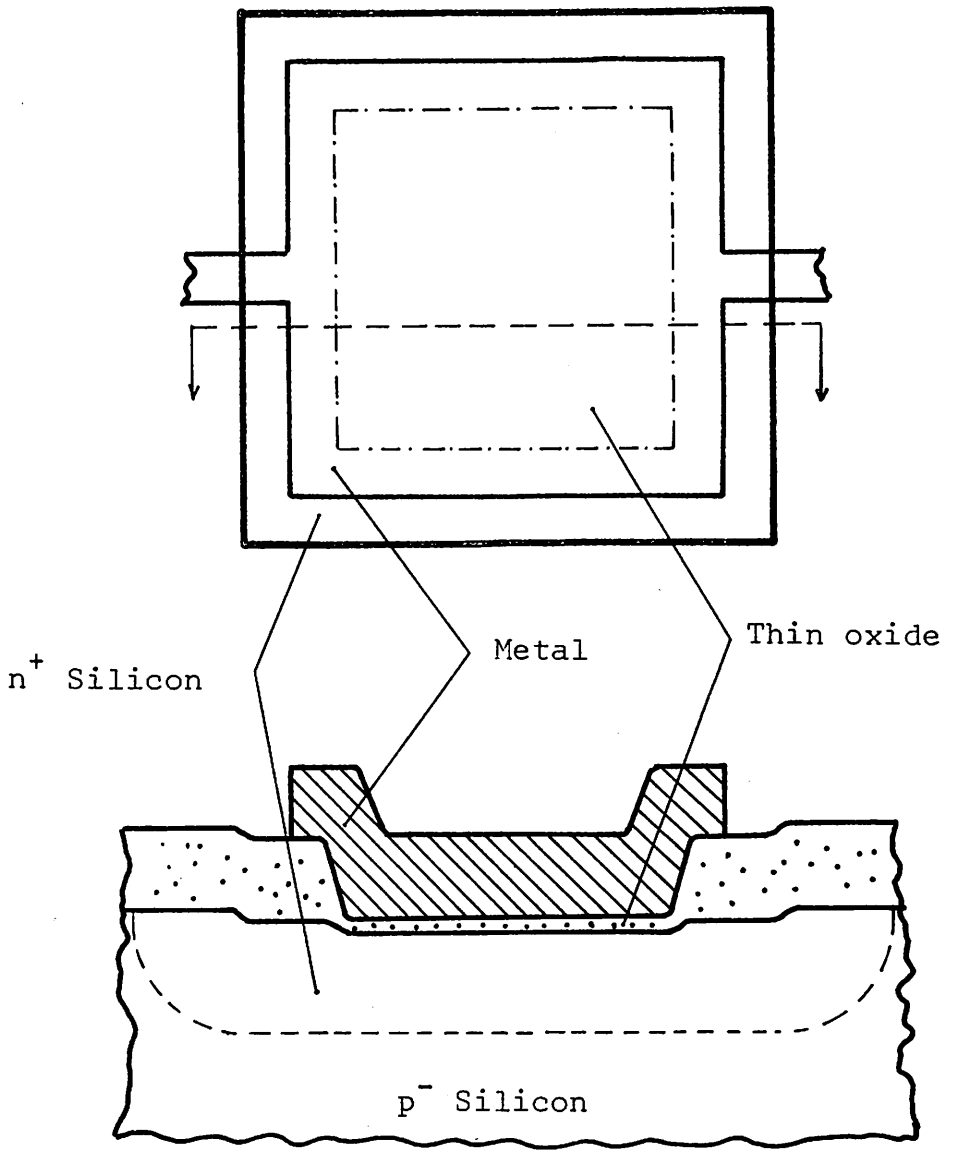
decided to determine the value of the capacitance mainly through the area of the insulator, i.e. the thin oxide.

The resulting capacitor structure is illustrated in Figure 3.11. There are several reasons for making this choice and they will be examined in the following lines.

The value of a capacitor defined mainly by the metal plate, as the one shown in Figure 3.10, is more sensitive to irregularities in the metal edge than the value of a capacitor defined mainly by the thin oxide area, Figure 3.11.

This is so because the thin oxide amplifies the effect of irregularities in the "metal capacitor" whereas this effect is attenuated by the thick oxide in the "oxide capacitor". The edge that is important for the"oxide capacitor" is the edge of the thin oxide region; this edge is the result of an etching process of much longer duration than the one used for metal and therefore less likely to be "jagged".

A comparison between the masking steps used to define the metal edge in both the "metal" and the "oxide" versions, Figure 3.12 and respectively 3.13, illustrates the fact that in the second version the adherence between mask and wafer is better so that the definition of the pattern image is likely to be superior in the "oxide capacitor" case. The critical edge in this implementation, the thin oxide edge, is defined by a similar "nongap" masking step. An other argument in favor of the thin oxide defined capacitor is the fact that in the metal-defined capacitor the critical




MOS capacitor.

(defined mainly by thin oxide)

Figure 3.11

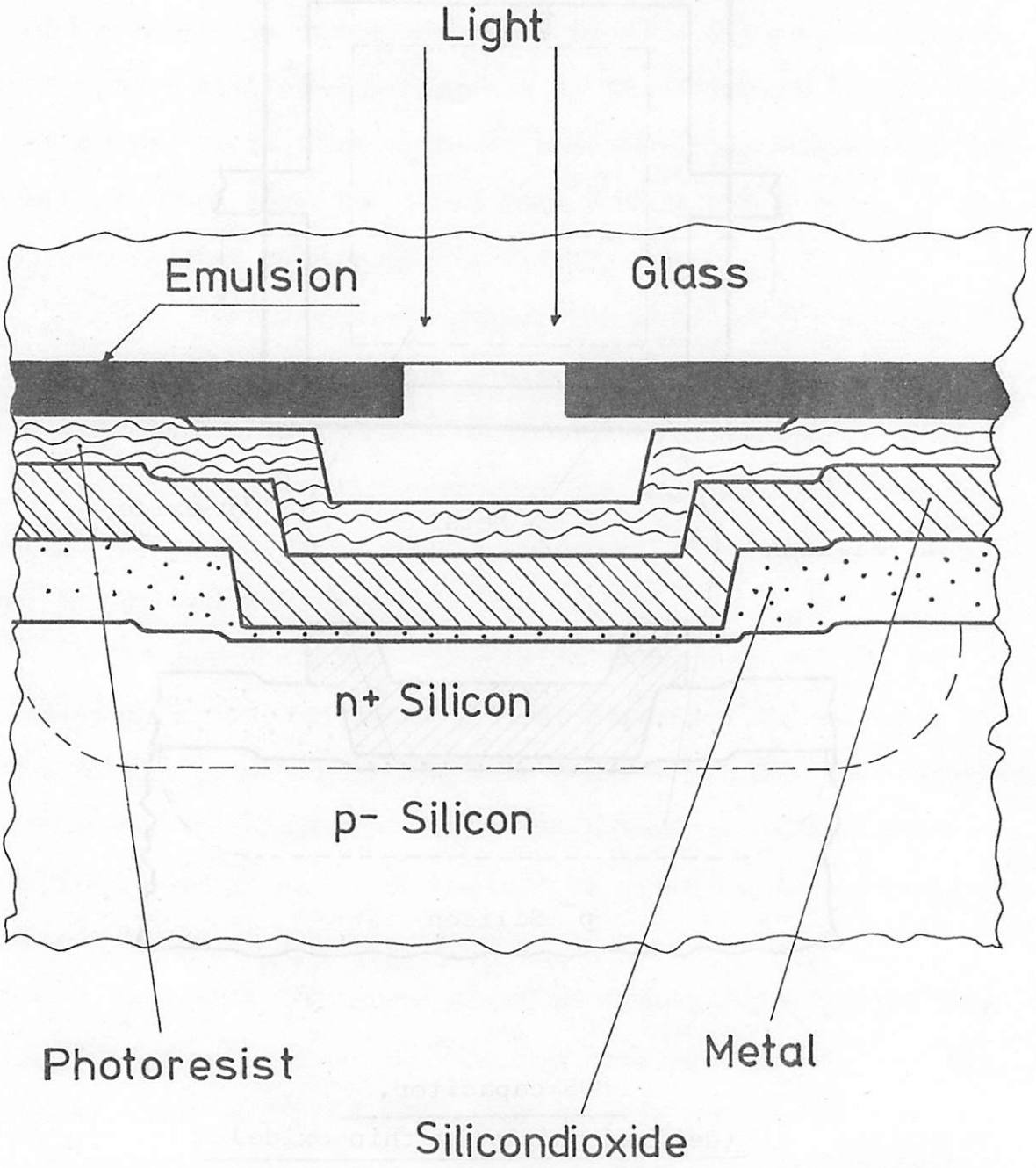

Light
Emulsion
Glass
n+ Silicon
p- Silicon
Photoresist
Metal
Silicondioxide

Figure 3.12

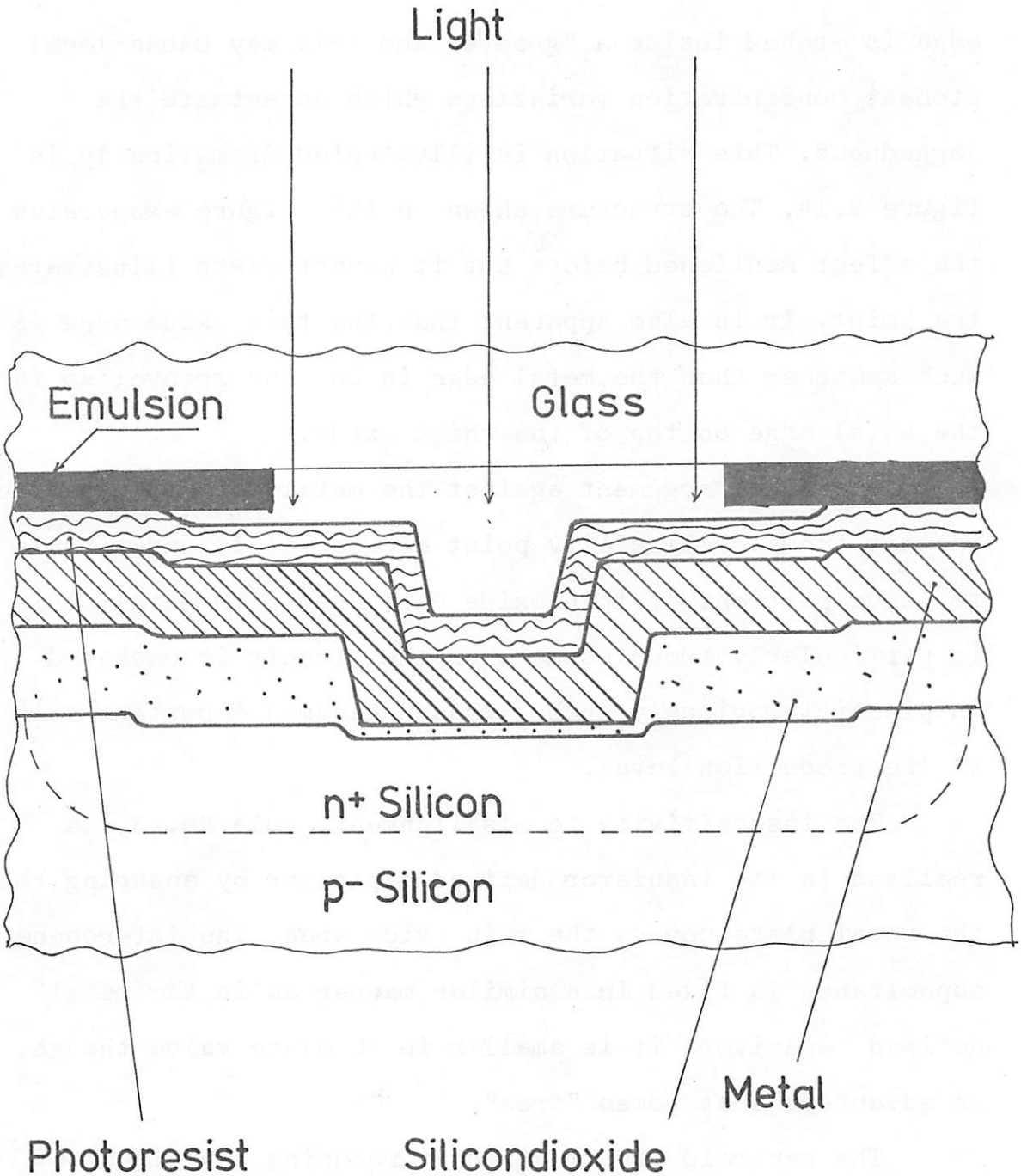

Light
Emulsion
Glass
n+ Silicon
p- Silicon
Metal
Photoresist
Silicondioxide

Figure 3.13

edge is etched inside a "groove" and this may cause local etchant concentration variations which accentuate the jaggedness. This situation is illustrated dramatically in Figure 3.14. The structure shown in this figure exagerates the effect mentioned before but it nevertheless illustrates the point. It is also apparent that the thin oxide edge is much smoother than the metal edge inside the groove; so is the metal edge on top of the thick oxide.

One final argument against the metal defined capacitor is that from a reliability point of view it is undesirable to leave portions of thin oxide uncovered with metal. This is particularly troublesome when the circuit is packaged in plastic. Obviously such a reason becomes important only at the production level.

The insensitivity to misalignment, rule No. 3, is realized in the insulator defined capacitor by ensuring that the metal plate covers the thin oxide area. The interconnect capacitance is fixed in a similar manner as in the metal defined capacitor; it is smaller in absolute value though, an advantage that comes "free".

The centroid layout aimed at reducing the effect of long range oxide gradients is not very attractive from an interconnect point of view. Fortunately the mismatches traceable to long range oxide gradients are negligible in the case of the PCM codec, as will be shown later.As a result the layout was not done in a centroid manner.

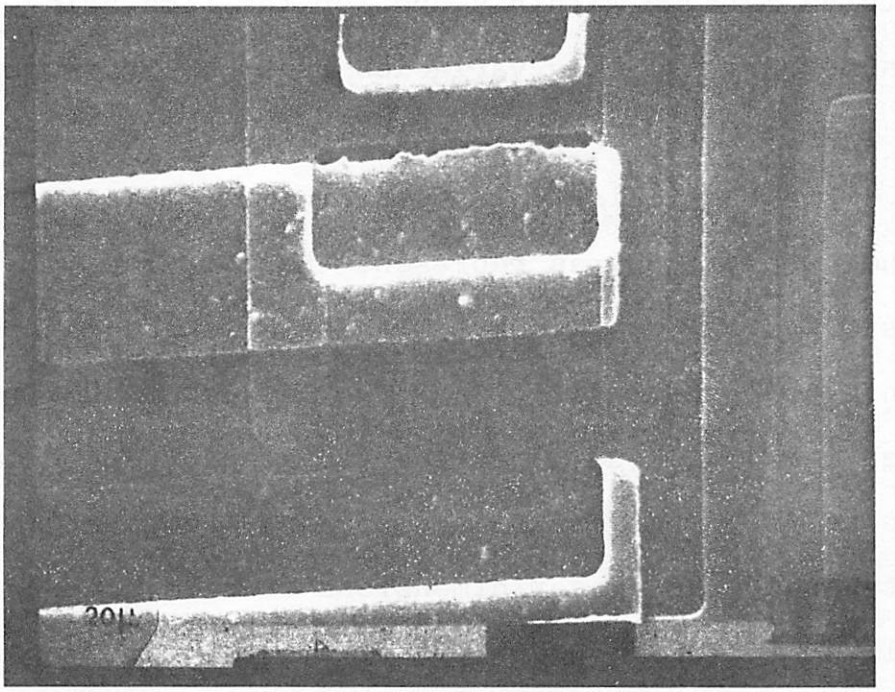



Illustration of the "in groove" etching of aluminum.

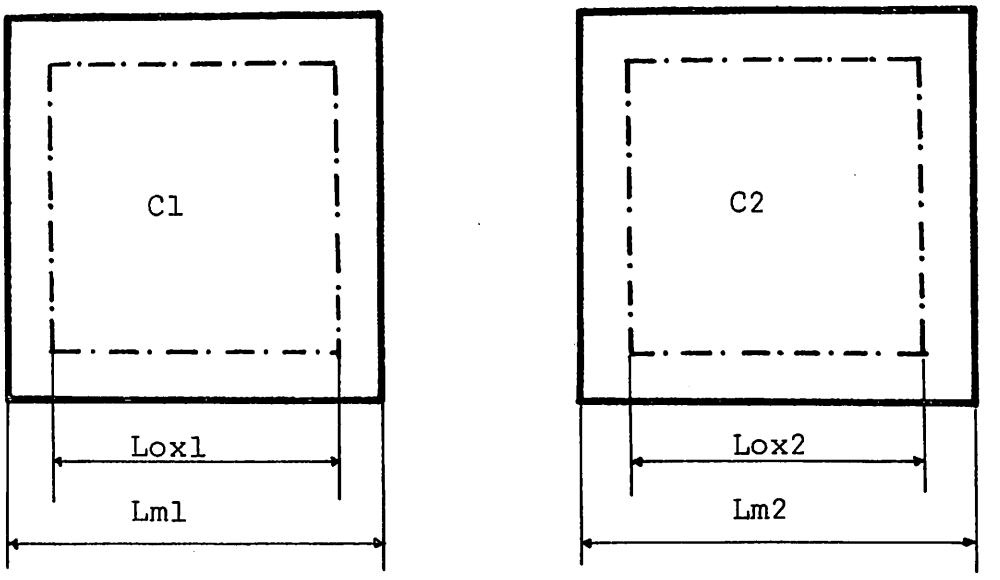
Figure 3.14

### 3.1.6 The absolute dimensions of the unit capacitors.

After deciding on the type of structure to be used for the capacitors one has to choose the absolute dimensions of the unit.

Consider two capacitors of "identical" size that have to be matched within $\varepsilon$ and for the time being let us assume that the only variables are the linear dimensions.

The vehicle for this analysis is defined in Figure 3.15, where the inside squares define the thin oxide areas and the outside squares represent the top metal plates. If the matching of any two distinct units can be maintained within $\varepsilon$ then the ratio of any two capacitors built out of such units will deviate from its ideal value by at most $\varepsilon$. The relation between this error and the relative mismatches of the linear dimensions is straightforward and is illustrated in Figures 3.16 to 3.19. It was assumed that the oxide is ten times thicker under the metal lip than in the center of the structure. In order to obtain numerical results one has to assign a value to r, the ratio between the nominal lateral dimensions of the two squares. In the course of the design this would be done in an iterative manner but for the purpose of illustration we can use $r = 1.3$ which corresponds to the final choices made for the lateral dimensions. The sensitivity of the matching error to y, the relative deviation in the metal edge dimension decreases as r approaches 1. In spite of the




$Lox1 - Lox2 = \Delta ox;\ (Lox1 + Lox2)/2 = Lox;\ \left|\frac{\Delta ox}{Lox}\right| = x$

$Lm1 - Lm2 = \Delta m;\ (Lm1 + Lm2)/2 = Lm;\ \left|\frac{\Delta m}{Lm}\right| = y$

$Lm/Lox = r$

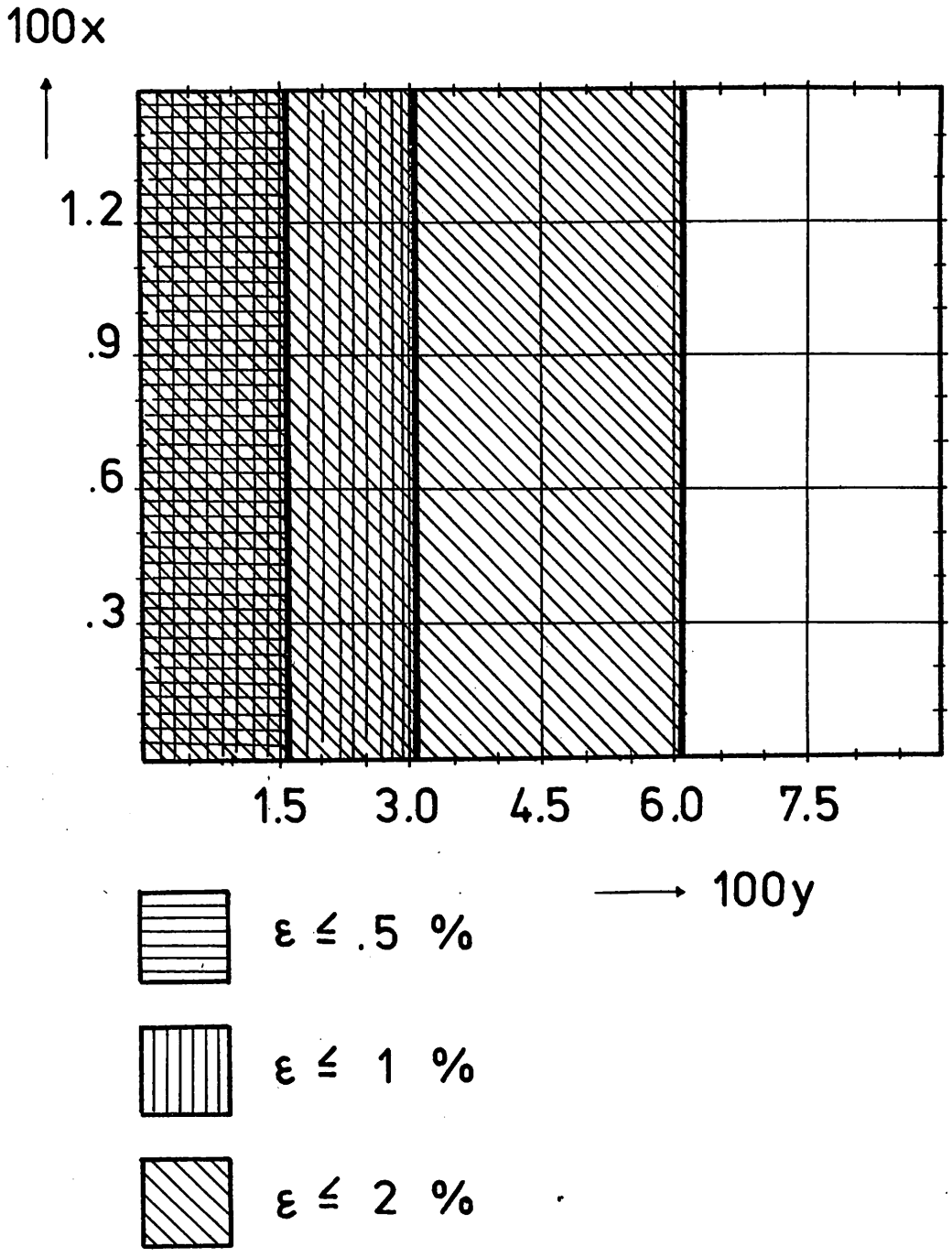
$C1 \sim (Lox1)^2 + .1[(Lm1)^2 - (Lox1)^2]$

$C2 \sim (Lox2)^2 + .1[(Lm2)^2 - (Lox2)^2]$

$C1/C2 = 1 \pm \varepsilon;\quad \varepsilon = f(x,y,r)$

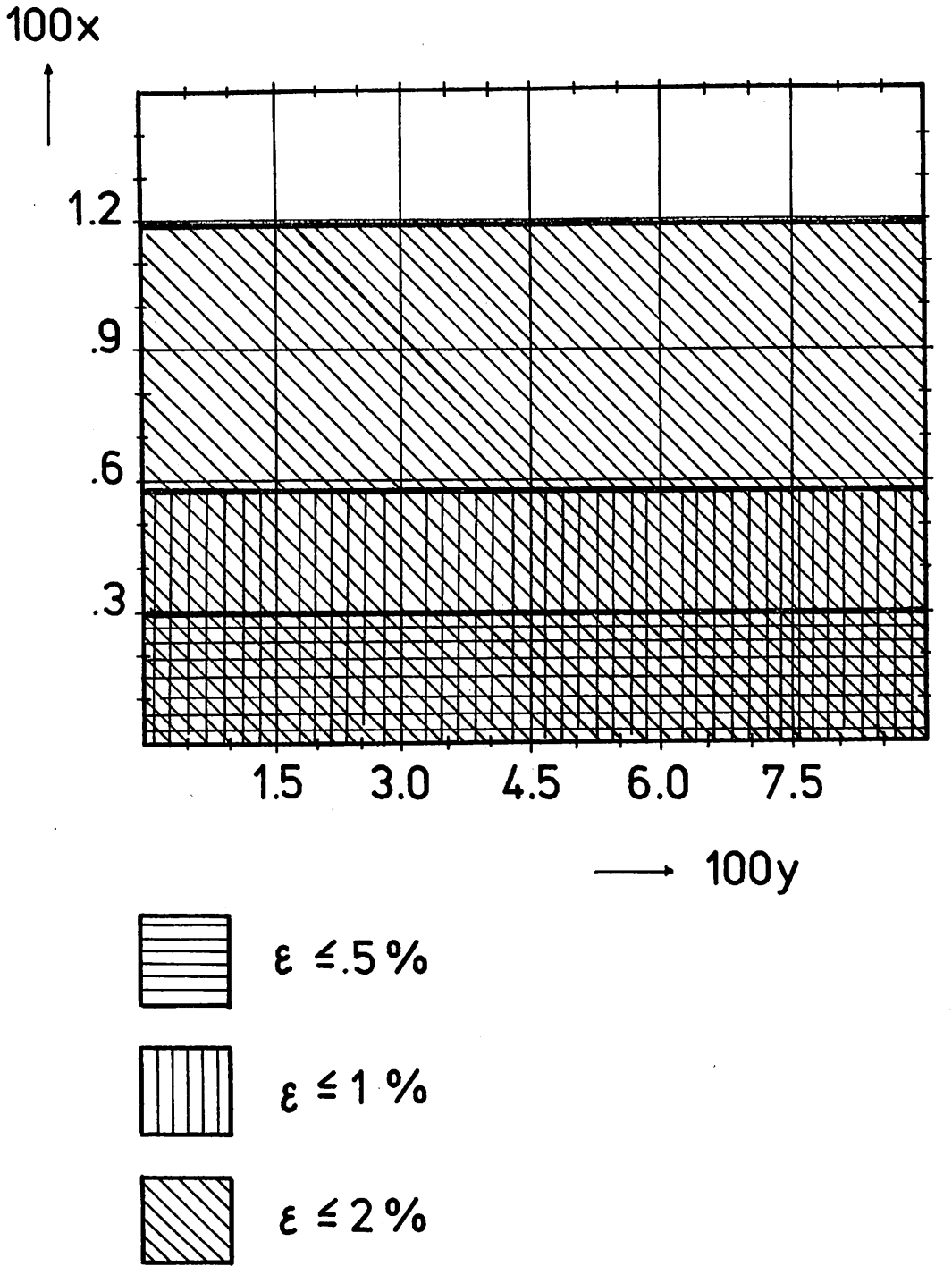
Matching of "identical" capacitors.

Figure 3.15



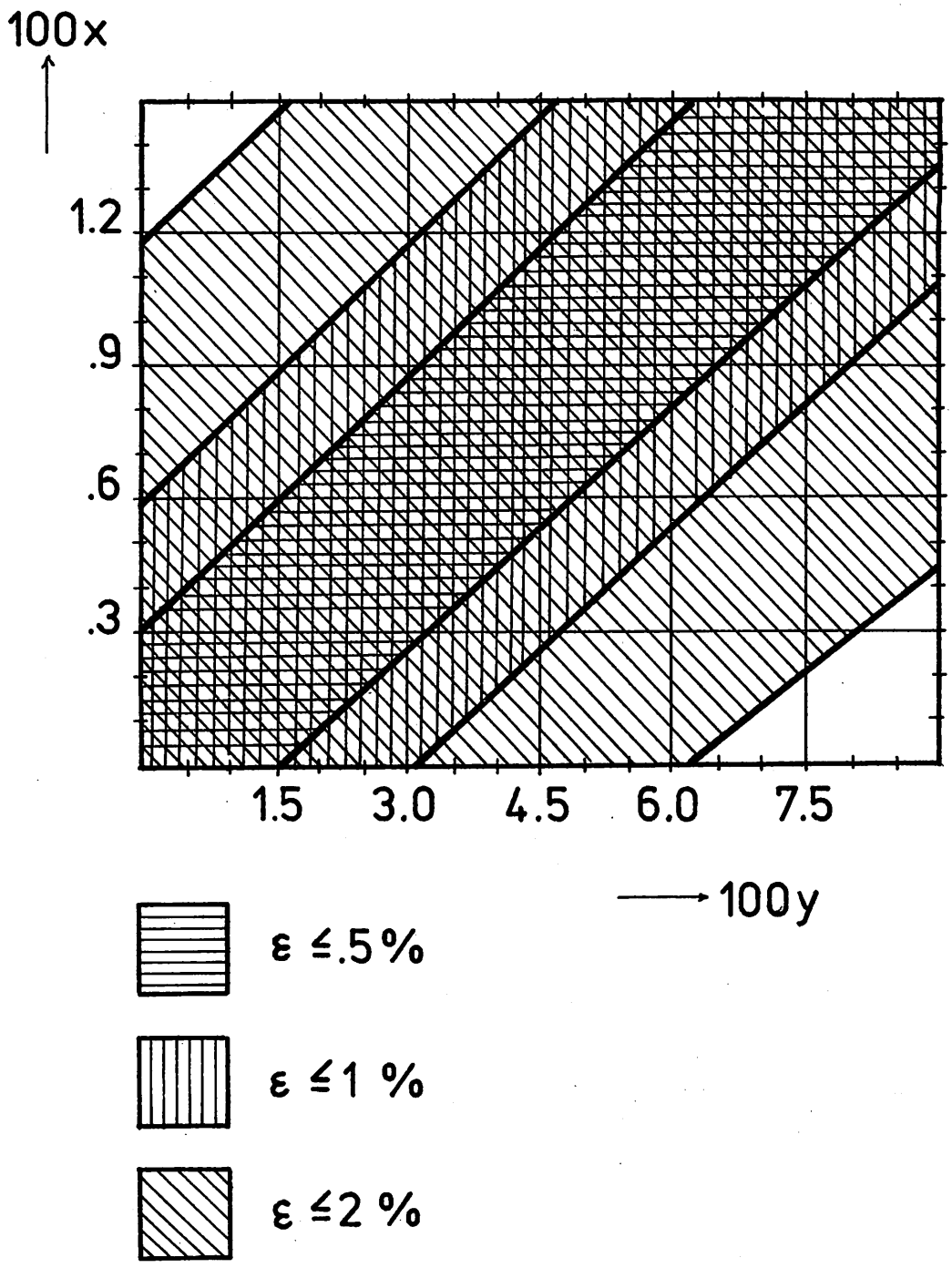

Matching error ε in the case Δox = 0

Figure 3.16



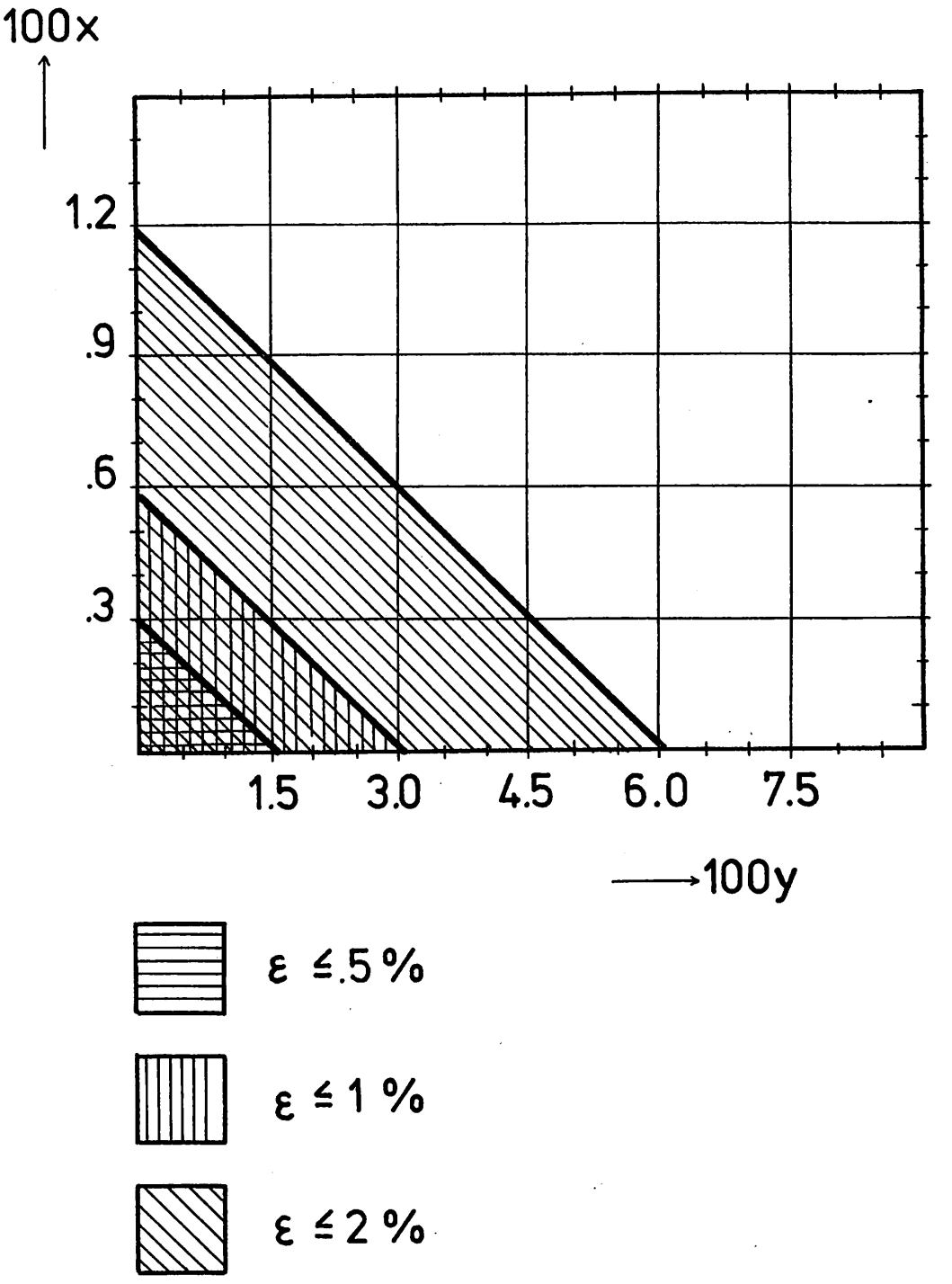

Matching error ε in the case Δm = 0

Figure 3.17




Matching error in the case (Δox)*(Δm)< 0

Figure 3.18




Matching error ε in the case (Δox)*(Δm) > 0

Figure 3.19

relatively large value chosen for r one can see that y has much less influence on the matching error than x.

The finite Δ's are the result of several imperfections.

From measurements made on working plate patterns it was found that Δox (or at least the contribution to it) can be of about .1μm, this being the difference between the lateral dimensions of otherwise "straightedged" squares.

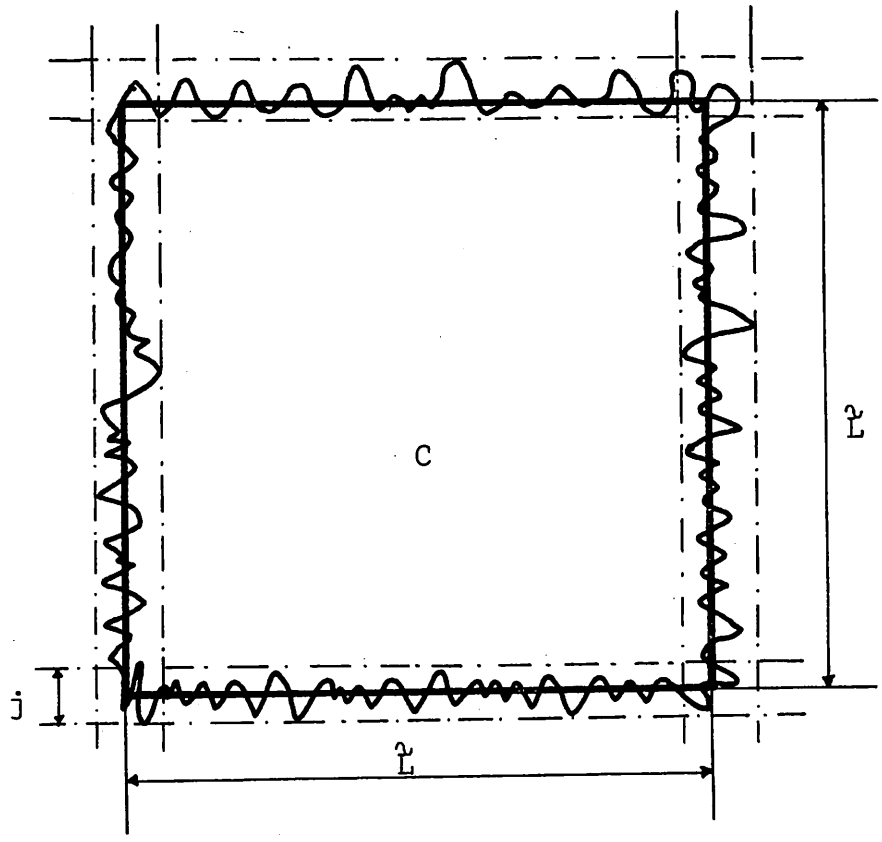
A similar value of Δm is obviously much less troublesome. The main contribution to Δm results from the jaggedness of the etched edge. This is illustrated in an exagerated manner in Figure 3.20. Such jaggedness could probably be described by a more or less complicated random function but eventually some of the parameters entering this description would have to be measured experimentally.

One parameter of the "jaggedness" that can be easily measured without having to resort to special test structures is the maximum difference between the "peaks" and "valleys" occuring along the edge. This has been denoted as j in Figure 3.20. It is reasonable to expect that j is much larger than the Δ of the same figure; therefore an estimate like Δ = j/2 appears to be safely conservative. From measurements made on reasonably well behaved metal edges it was found that j is of about .6μm. It has been argued earlier that the quality of the thin oxide edge is likely to be superior to the quality of the metal edge (see also Figure 3.14). Therefore if we estimate Δox as being of the same magnitude with the "metal Δ", i.e. about .3μm, we

run a good chance of obtaining a superconservative Δox.

The sum of the Δ contributions from mask differences and from jaggedness would then be about .4μm. From Figure 3.21 it follows that in order to meet the 1% matching condition of Figure 3.19 one would have to choose Lox >65μm, which yields x < .6%. In view of all the conservative assumptions made so far one may expect that a value of Lox = 50μm will be adequate. Such reasoning as the one just presented is likely to lead to oversized capacitors but as long as the final array size is within practical limits one may argue that it is worth building in the additional safety margin. This safety margin will then allow other parameters to deviate more than in the case of a critically dimensioned capacitor array. The final choice of capacitor dimensions is shown in Figure 3.22; these dimensions yield a unit of about .85pF. A sufficiently wide metal lip ensures insensitivity to misalignment; this overlap was in fact exagerated so that the sizes of the squares would permit an easy conversion to the oxide defined capacitor if there were a desire for doing so.

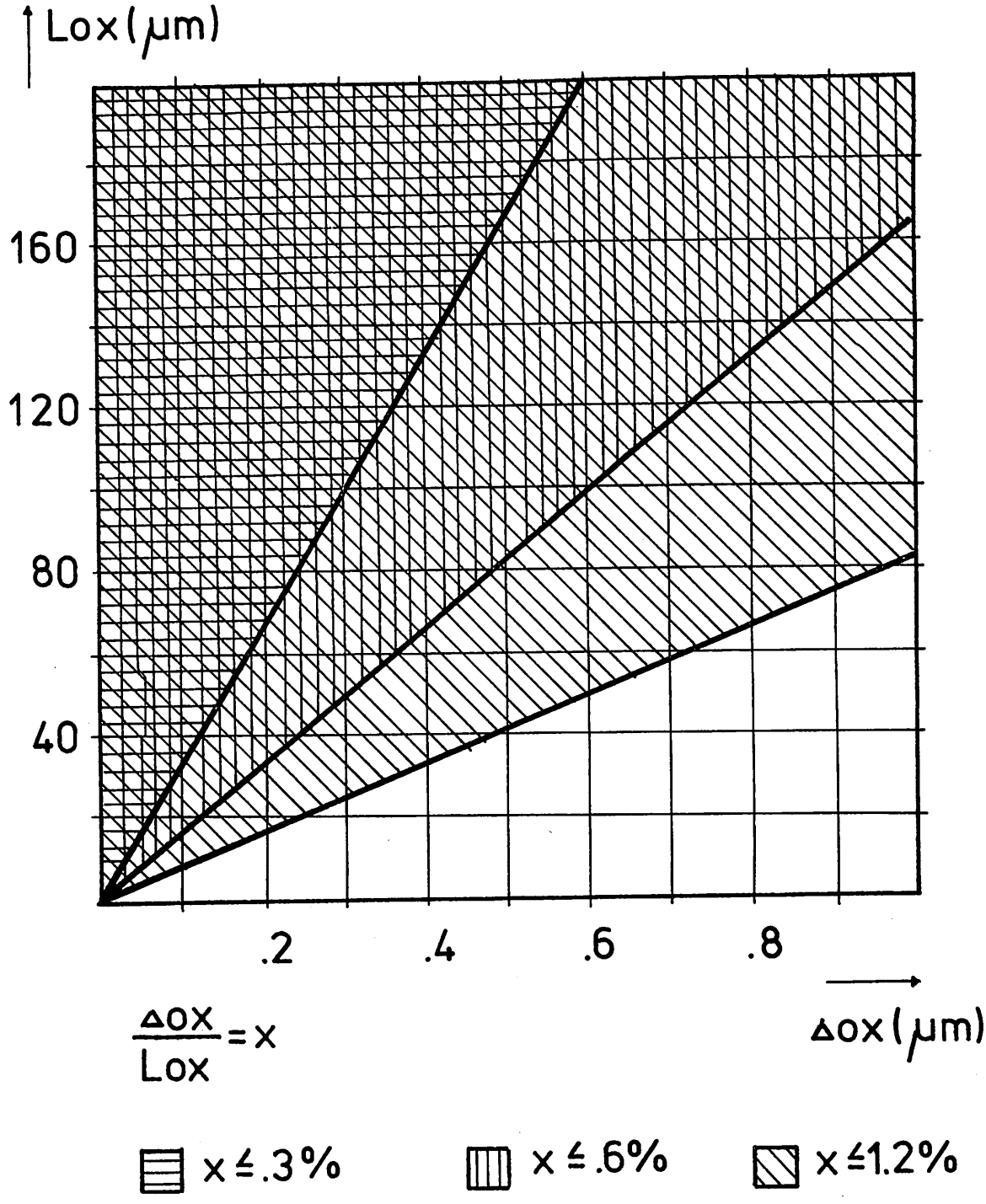
The final layout for the segment array is shown in Figure 3.23. One may notice the "gaps" in the bottom diffusion plates of the capacitors; these gaps ensure the matching of the interconnect contributions. As a result one may safely claim that the capacitors are matched within fringing field effects.




$$C \sim (\tilde{L})^2 = (Lnom \pm \Delta)^2$$

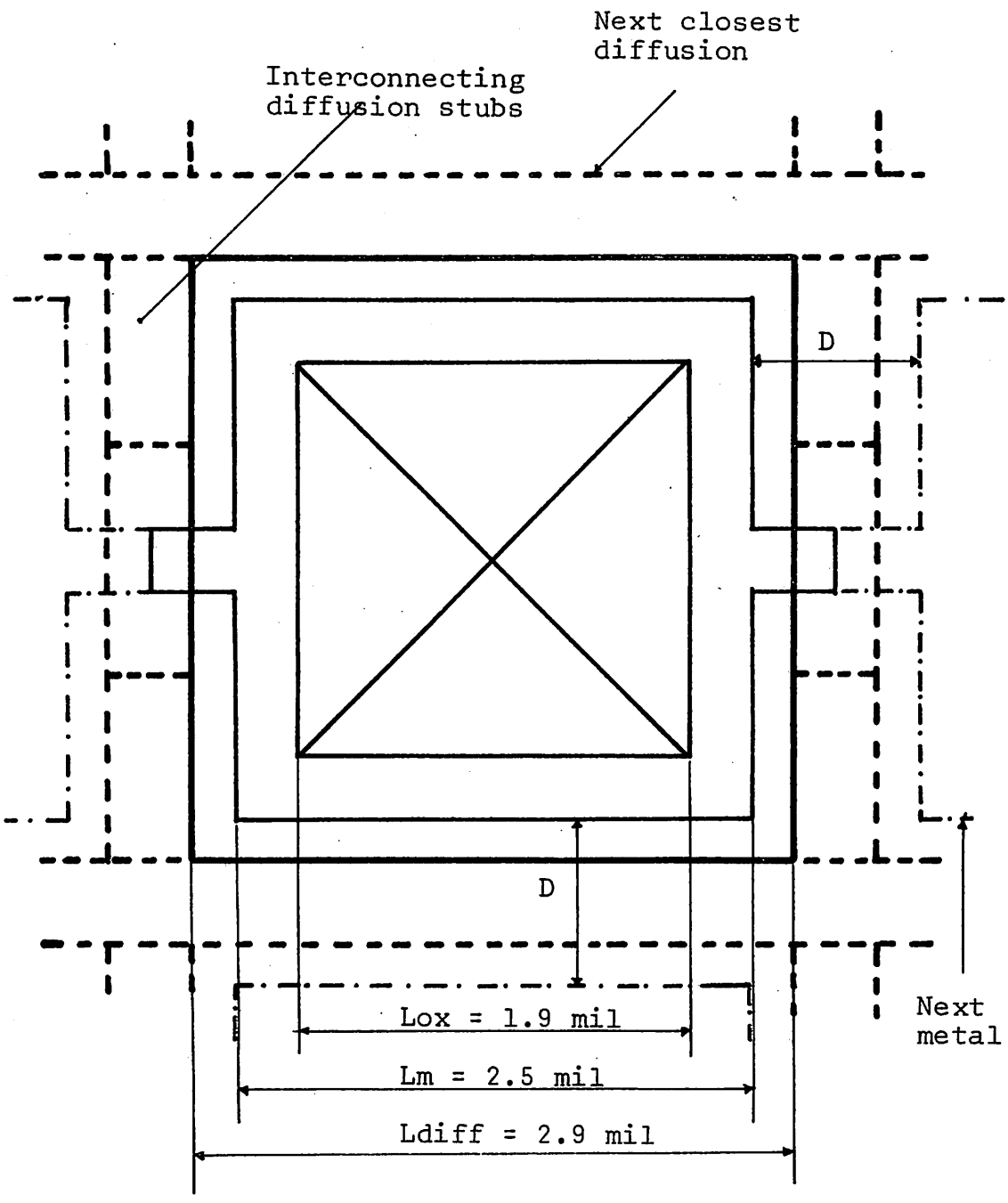
Capacitor with jagged edge.

Figure 3.20



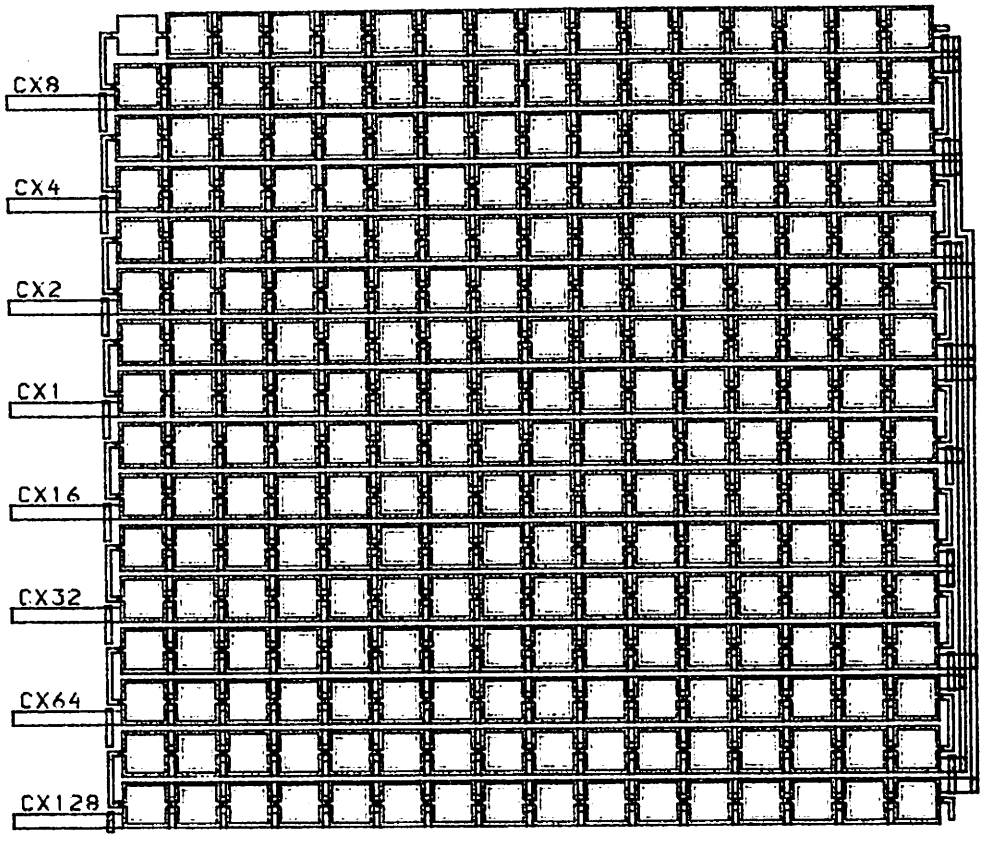

Relation between absolute lateral dimension absolute deviation .

Figure 3.21




Absolute dimensions of unit capacitor.

Figure 3.22




METAL - BLACK

INSULATOR - GREEN

SEMICONDUCTOR - RED

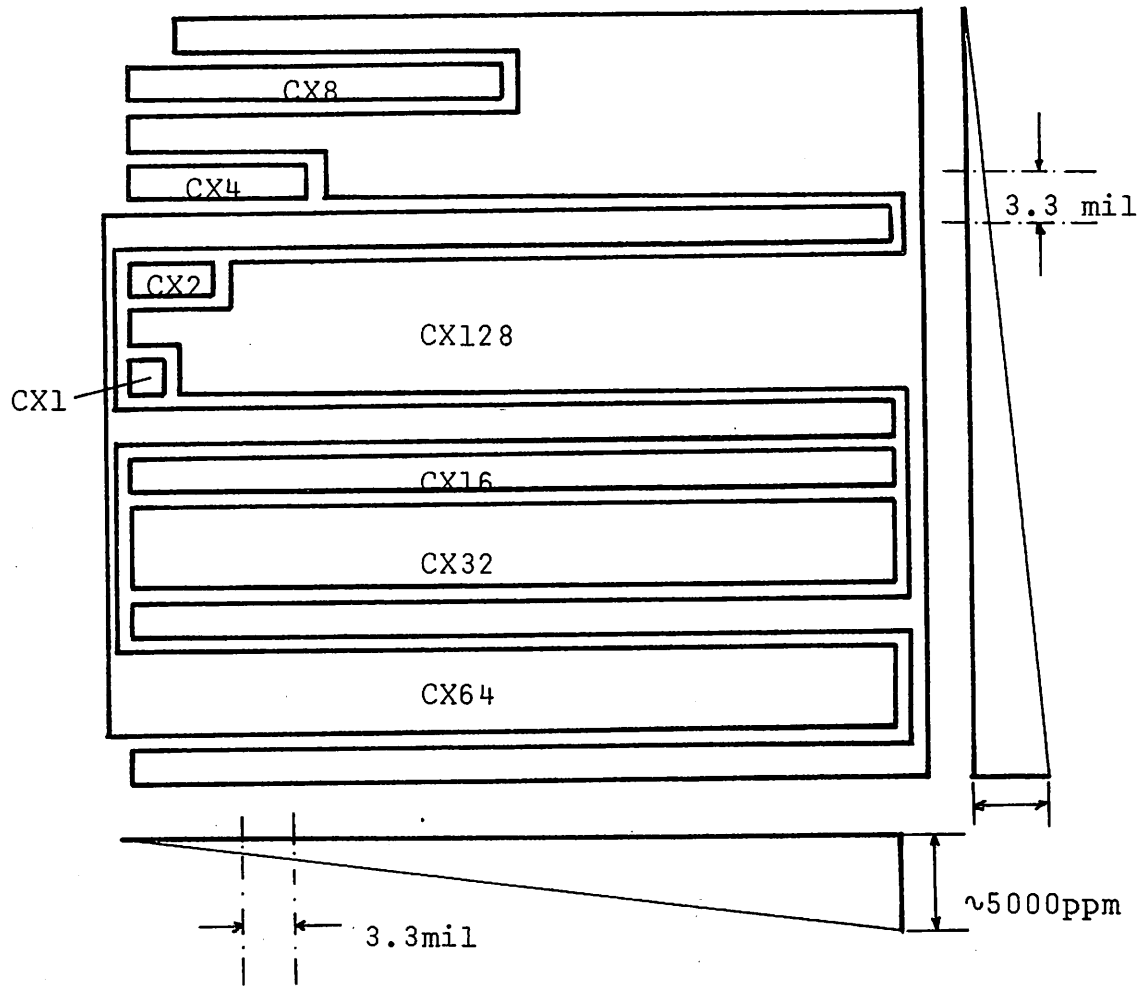
FIGURE 3.23

### 3.1.7 The influence of long range oxide gradients on capacitor matching.

After the absolute value of the unit capacitor and the layout of these units in the array are known one can evaluate the sensitivity of the noncentroid layout to long range oxide gradients. The two most likely cases are illustrated in Figure 3.24. The center to center spacing between two adjacent capacitors is 3.3 mils; assuming a gradient of 100ppm/mil one can easily compute the resulting mismatches. These results are listed in TABLE 3.6. By comparing these deviations with the results obtained from XCODEC simulations one must conclude that long range oxide gradients have no effect on the capacitor matching. Therefore the penalty for not using a centroid layout appears to be negligible.

### 3.1.8 Electrical properties of the MOS capacitors.

In a CMOS process there are three choices of bottom plates for an MOS capacitor , $n^+$, $p^+$, or $p^-$. A fourth choice the $n^-$ substrate is in general impractical because of its permanent connection to the positive supply. The fact that the capacitance of the MOS structure is voltage dependent has been already mentioned by means of Figures 3.7 and 3.8. Since it was decided to try to maintain the matching of the capacitors within 1% it turns out that the type of bottom plate to be used has to be capable of such a performance. This means that the capacitance variation traceable to voltage dependence has to be small enough.




Long range oxide gradient superimposed on segment array.

Figure 3.24

| | Horizontal gradient | Vertical gradient |
|---|---|---|
| dCX1 | ±0.25% | ±0.02% |
| dCX2 | ±0.23% | ±0.08% |
| dCX4 | ±0.20% | ±0.15% |
| dCX8 | ±0.13% | ±0.21% |
| dCX16 | ±0 | ±0.05% |
| dCX32 | ±0 | ±0.10% |
| dCX64 | ±0 | ±0.07% |
| dCX128 | ∓0.02% | ∓0.05% |

Capacitance deviations in the segment array as a result of long range oxide gradient.

TABLE 3.6

A good indicator of the voltage dependance of an MOS capacitor is the capacitance at the flat-band voltage.

$$C_{FB} = \frac{\varepsilon_{ox}}{d_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_s}\sqrt{\frac{kT\,\varepsilon_s}{C_B\,q^2}}}$$

where: $\varepsilon_{ox}$ is the permittivity of the insulator

$\varepsilon_s$ is the permitivitty of silicon

$C_B$ is the doping concentration of the bottom plate diffusion

$d_{ox}$ is the insulator thickness

$\frac{kT}{q}$ = 25.9 mV at 300°K

The MOS capacitance reaches the maximum value when there is an accumulation of carriers in the bottom plate. This maximum value is:

$$C_{max} = \frac{\varepsilon_{ox}}{d_{ox}}$$

The relative deviation of the MOS capacitance from the maximum value is:

$$\Delta C = \frac{C_{max} - C}{C_{max}}$$

The dependence of $\Delta C_{FB}$ on bottom plate doping is

listed in TABLE 3.7 for an oxide thickness of 1000Å.

TABLE 3.7 describes the small signal behavior of the capacitors whereas in the charge redistribution scheme the relevant description is the large signal capacitance. Since the latter is an integral of the former it turns out that the large signal capacitance will exhibit less voltage dependence due to the averaging process. Still the order of magnitude of the percentage deviations from the maximum value will be comparable so that the numbers listed in TABLE 3.7 can be used as an indication of the "quality" of a given bottom plate.

In the standard process used for the implementation of the PCM converters the three possible bottom plates yield the following values:

| | |
|---|---|
| $p^-$ with $C_B = (3\text{-}4)\times10^{16}\ cm^{-3}$ | $\Delta C_{FB} > 4.14\%$ |
| $p^+$ with $C_B = (5\text{-}9)\times10^{17}\ cm^{-3}$ | $\Delta C_{FB} > 1.35\%$ |
| $n^+$ with $C_B \cong 10^{20}\ cm^{-3}$ | $\Delta C_{FB} < .43\%$ |

From a matching point of view it appears that the only acceptable choice is the $n^+$ diffusion as long as one tries to maintain the matching within the 1% limit mentioned earlier. The $n^+$ bottom plates do also present reduced resistance thus simplifying the interconnection of the unit capacitors and hence the layout.

| $C_B$ ($cm^{-3}$) | $\Delta C_{FB}$ (%) | $V_{th}-V_{FB}$ (V) |
|---|---|---|
| $10^{14}$ | 57.72 | .522 |
| $10^{15}$ | 30.16 | .803 |
| $10^{16}$ | 12.01 | 1.481 |
| $10^{17}$ | 4.14 | 3.503 |
| $10^{18}$ | 1.35 | 10.033 |
| $10^{19}$ | .43′ | 31.600′ |
| $10^{20}$ | .14′ | 103.076′ |

Values marked with ′ have been "forced" by an extension of Fermi-Dirac statistics; at such doping levels the semiconductor is degenerate and the statistics governing the behavior of the carriers are different.

TABLE 3.7

3.1.9 Experimental results.

The capacitors were built according to the design decisions presented up to this point.

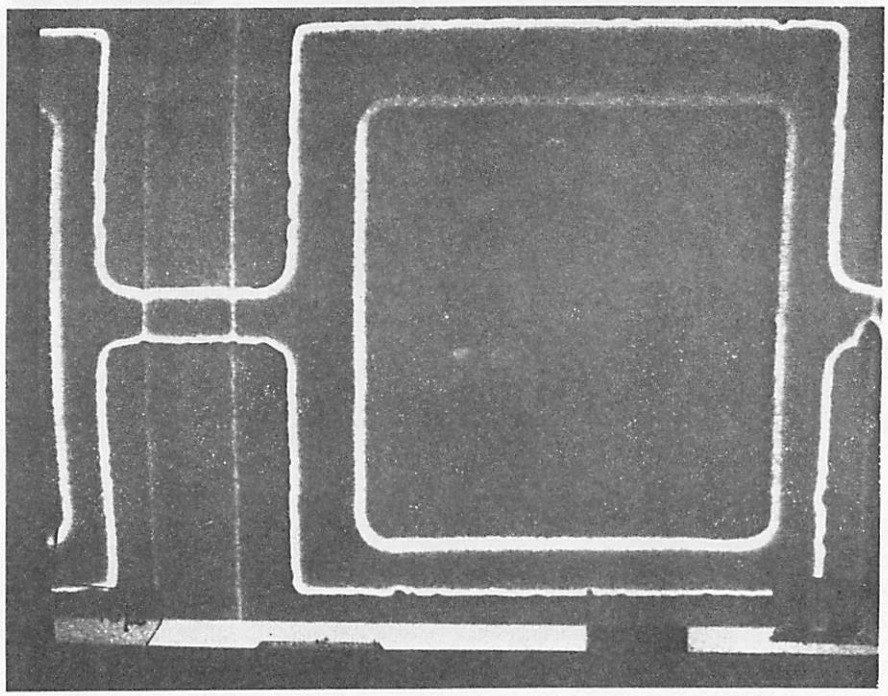
The Scanning Electron Microscope (SEM) pictures of the unit capacitor are presented in Figures 3.E1 to 3;E5.

Figure 3.E1 represents a top view of the unit capacitor and one can see that the "inside edge", defined by the thin oxide, is indeed smoother than the "outside edge", defined by the metal. This feature can be observed at a magnified scale in Figure 3.E2 which represents a view of the capacitor corner. The straightness of the oxide edge is illustrated in Figure 3.E3 and in Figure 3.E4, both representing close up views of the "inside edge". In contrast to this smooth edge, the "outside edge", presented in Figure 3.E5, is more "jagged".

Figure 3,E6 represents a top view of a few capacitors in the segment array.

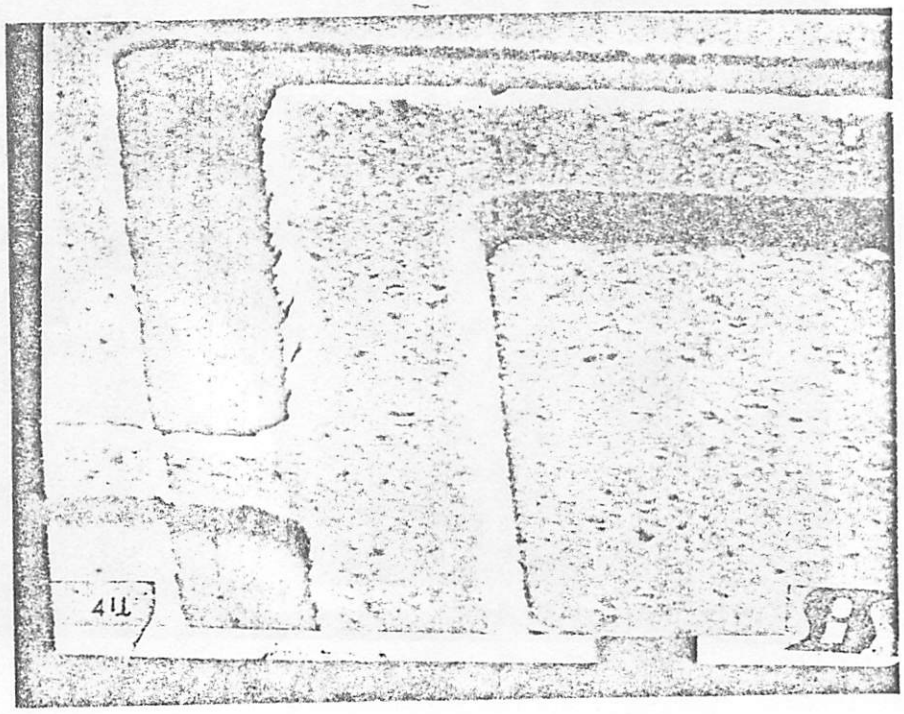
Due to the small absolute value of the capacitances it is not practical to directly measure the capacitance for the purpose of matching evaluation. Matching can nevertheless be measured indirectly by measuring the "voltage length" of the segments or steps in the transfer curve. Results obtained from such measurements are presented in TABLE 3.E1. The segment start is defined as the voltage at which the output code (at the output of the coder) changes by 1 bit. This measurement does also yield the comparator offset voltage, which in this particular case was of about 6mV. Thus it appears that the capacitor matching is within the desired

limits. Since the segment capacitor matching is close to perfect one can assume that the same holds for the step array capacitors. Based on this observation one can estimate the buffer offset voltage and the parasitic capacitance in the step array by measuring the steps. The results of such an experiment are presented in TABLE 3.E2. By repeating this type of measurement on a statistical basis, one can reduce the parasitic capacitance in the step array by trimming the terminator and thus improve the performance even more.



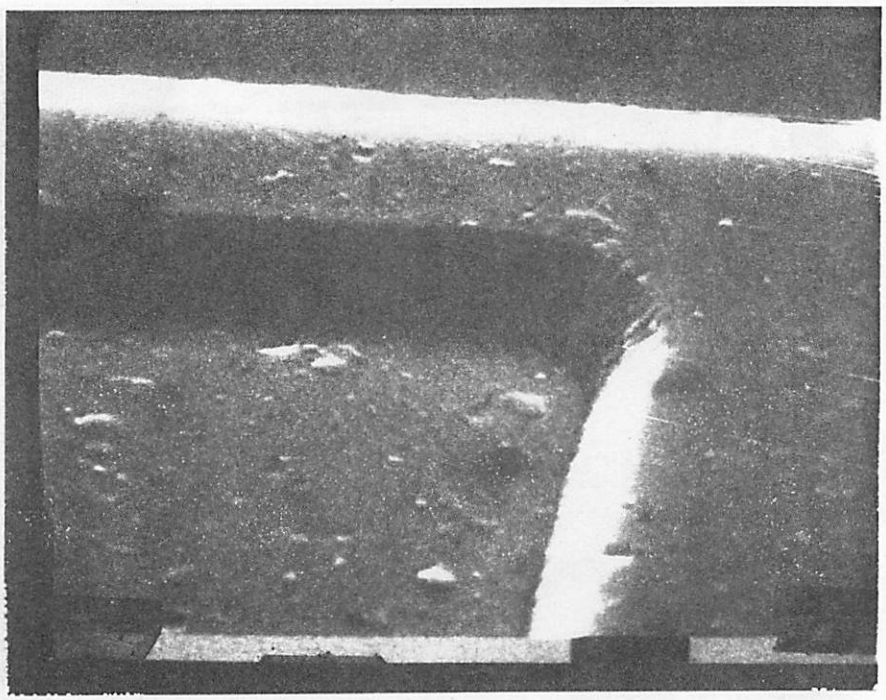
Top SEM view of the unit capacitor.

Figure 3.E1



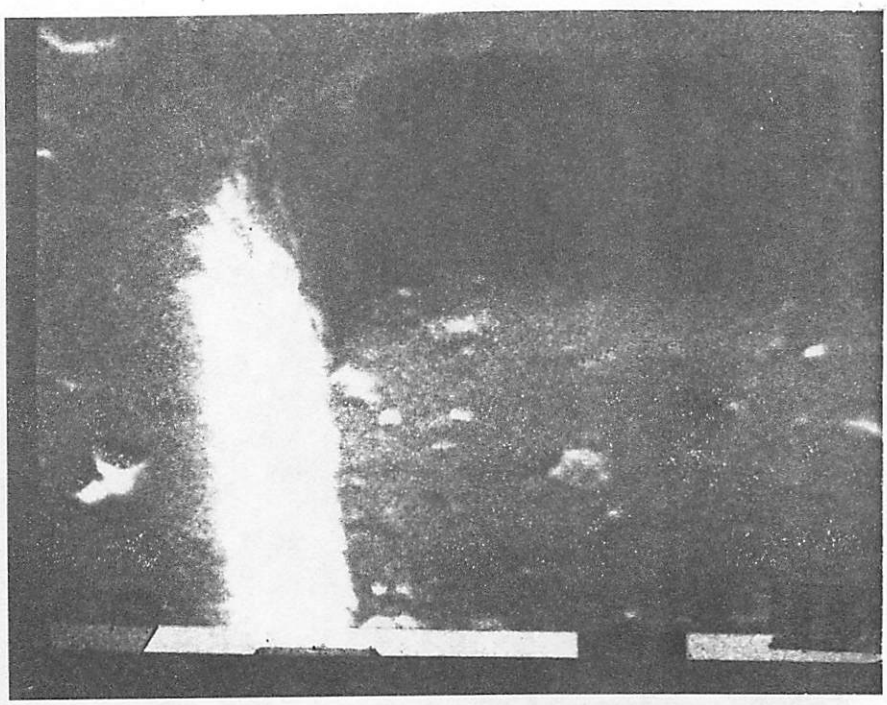

SEM view illustrating the relative smoothness of thin oxide and respectively metal defined edges.

Figure 3.E2



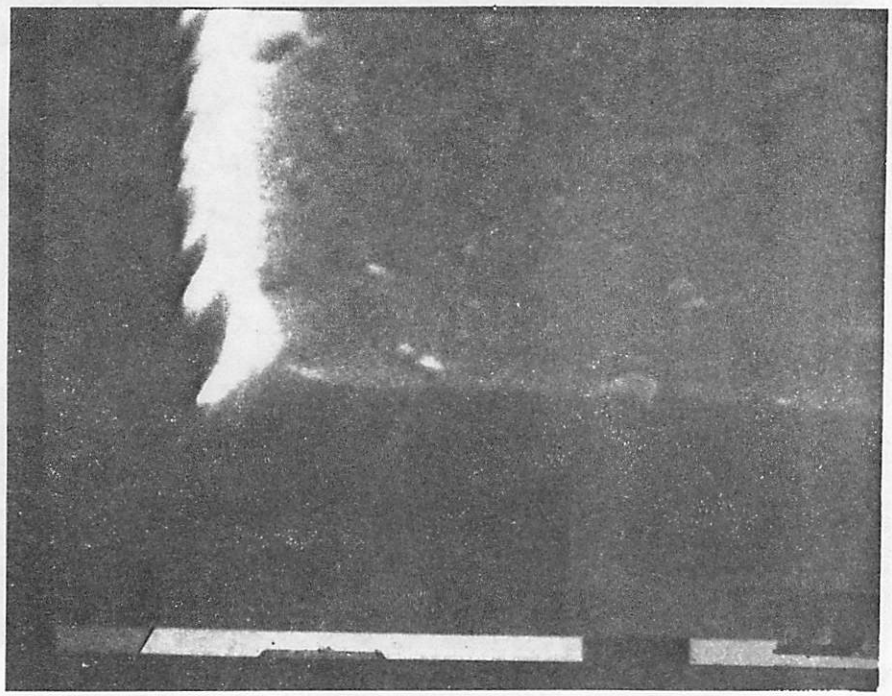
SEM view illustrating the inside edge of the MOS capacitor.

Figure 3.E3



SEM view illustrating the inside edge of the MOS capacitor.

Figure 3.E4



SEM view illustrating the edge of the top metal plate in the MOS capacitor.

Figure 3.E5

Figure 3.E6

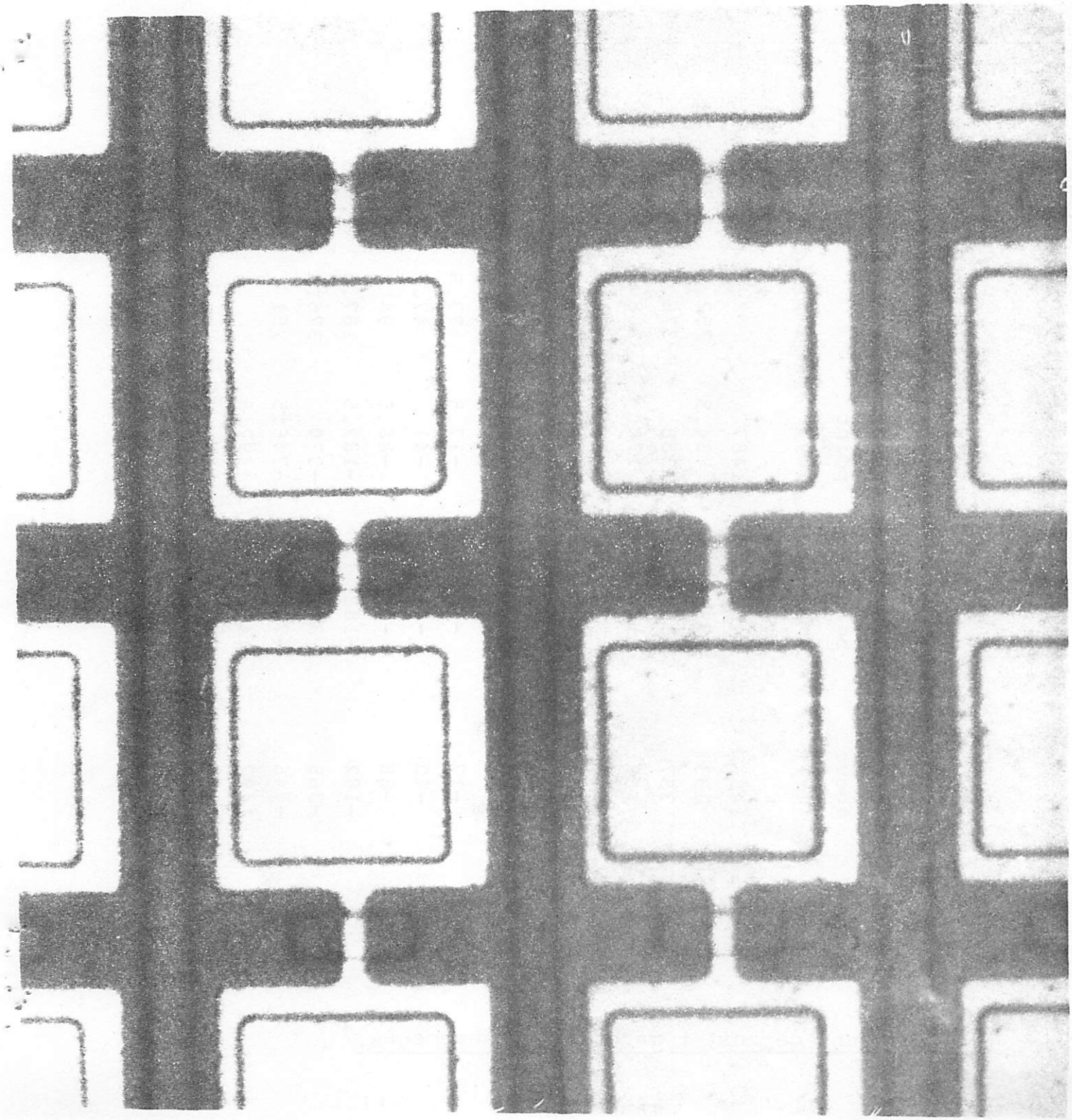


TABLE 3.E1

Segment capacitor matching measurements.

| Segment No. | Segment start from above (mV) | Segment start from below (mV) | Average starting point (mV) | Segment length (mV) | Segment ratio of consecutive segements |
|---|---|---|---|---|---|
| 8+ | 1486 | 1488 | 1487 | | |
| 7+ | 733 | 736 | 734.5 | 752.5 | 1.999 |
| 6+ | 357 | 359 | 358 | 376.5 | 2.003 |
| 5+ | 169 | 171 | 170 | 188 | 2. |
| 4+ | 75 | 77 | 76 | 94 | 2. |
| 3+ | 28 | 30 | 29 | 47 | 1.958 |
| 2+ | 4 | 6 | 5 | 24 | |
| 2- | -17 | -18 | -17.5 | 23.5 | |
| 3- | -40 | -42 | -41 | 47.5 | 2.021 |
| 4- | -88 | -89 | -88.5 | 94 | 1.979 |
| 5- | -182 | -183 | -182.5 | 187.5 | 1.995 |
| 6- | -369 | -371 | -370 | 376.5 | 2.008 |
| 7- | -746 | -747 | -746.5 | 751 | 1.995 |
| 8- | -1497 | -1498 | -1497.5 | | |

| Digital code | Step start from below (mV) | Step start from above (mV) | Average starting point (mV) | Step length (mV) | Step length adjusted for buffer offset (mV) |
|---|---|---|---|---|---|
| 00011111 | 751 | 751 | 751 | | |
| 00010010 | 1326 | 1326 | 1326 | 43.5 | 43.5 |
| 00010001 | 1369 | 1370 | 1369.5 | 42.5 | 42.5 |
| 00010000 | 1412 | 1412 | 1412 | 89.5 | 100.25 |
| 00001111 | 1501 | 1502 | 1501.5 | 108.5 | 85.5 |
| 00001110 | 1610 | 1610 | 1610 | 87 | 87 |
| 00001101 | 1697 | 1697 | 1697 | 87 | 87 |
| 00001100 | 1784 | 1784 | 1784 | | |
| | | | | | |
| 10011111 | 725 | 726 | 725.5 | | |
| 10010010 | 1280 | 1281 | 1280.5 | 43.5 | 43.5 |
| 10010001 | 1324 | 1324 | 1324 | 43 | 43 |
| 10010000 | 1367 | 1367 | 1367 | 111 | 100.25 |
| 10001111 | 1477 | 1479 | 1478 | 62.5 | 85.5 |
| 10001110 | 1540 | 1541 | 1540.5 | 87.5 | 87.5 |
| 10001101 | 1628 | 1628 | 1628 | 87 | 87 |
| 10001100 | 1715 | 1715 | 1715 | | |

Step size measurements showing quasi perfect capacitor matching and yielding buffer offset and parasitic capacitance in the step array (in this case the parasitic capacitance represents 131% of the unit)

TABLE 3.E2

## 3.2 THE CMOS BUFFER AMPLIFIER

In order to be able to generate the correct step voltages, the capacitor array used for this purpose has to be buffered from the segment capacitor array. This is accomplished with the aid of a unity gain buffer amplifier.

### 3.2.1 Design objectives.

The ideal buffer is characterized by the following parameters:

- the voltage gain is exactly 1
- the voltage offset is exactly 0
- the common mode range is rail-to-rail
- the input resistance is infinite
- the input capacitance is 0
- the output follows the input instantaneously

The practical question then is: how close do the practical parameters have to be to the ideal ones?

The acceptable tolerances of the static parameters can be found using XCODEC. The response time will depend on converter timing.

The XCODEC simulation was performed on a single parameter deviation basis, i.e. all the parameters except for the one under investigation were kept ideal. The results of this analysis are:

| | Coder | Decoder |
|---|---|---|
| Minimum gain | .865 | .952 |
| Maximum offset | 5.6% of $V_R$ | 5% of $V_R$ |

This implies an open loop gain greater than 6 in the coder and greater than 20 in the decoder and the practical gain is obviously much larger than that.

The voltage offset is less predictable than the gain.

The mean offset voltage can be brought arbitrarily close to 0 through proper design but the practical circuit will be sensitive to device mismatches which can not be arbitrarily minimized. The input stage with its relatively low gain will be the main contributor to the offset voltage.

Generally accepted remedies for this problem are large input devices and symmetrical layout of the input stage. Since the single stage gain is much lower in an MOS implementation than in a bipolar one the expected offset voltages will be sensibly larger in the MOS amplifier. The values generally quoted are of the order of tens of mV.

According to the XCODEC analysis, for a reference voltage of 3 Volts the tolerable offsets are equal to about 170 mV and respectively 150 mV. In the case of a 5 Volt reference the numbers are 280 mV and respectively 250 mV.

The practical offset voltages are likely to be much smaller than these values so that no attempt has been made to cancel the buffer amplifier offset voltage.

The common mode range of the buffer has to be sufficiently large to accomodate the references. The choice of references in turn depends on the combination between supply voltages and the type of analog switches that are used. The maximum supply voltages compatible with the CMOS process used for the

codec implementation were ± 7.5 Volts. Larger positive values require guard rings with the associated area penalty. With these supplies and nominal threshold voltages of ± 1.5V one can build CMOS amplifiers with a common mode range of about ± 5V. This then would be the maximum limit for the choice of references. This limit can be used only with CMOS analog switches capable to switch voltages up to the two supplies.

A true CMOS switch is obviously more space consuming than a p-channel or n-channel switch. Therefore an attempt has been made to use only single polarity switches. In the particular process used for the codec implementation the p-channel switch is the one capable of handling the largest voltages. The practical limits with ±7.5V supplies are ±3V.

These values have been chosen for the reference voltages to be used in the codec. From this point of view the practical common mode range of ±5V is obviously acceptable.

The input resistance of a CMOS amplifier can be safely neglected. The input capacitance depends on the type of input stage being used and on the loop gain of the feedback path. From this point of view the differential input stage seems to be quite adequate.

The response time of the buffer has to be such as to allow enough time for the various operations performed during a converter time slot. At a sampling rate

of 8kHz these time slots have a duration of about 10 μs and this becomes 5 μs at 16kHz, etc. The time within a time slot is used for various operations among them being the generation of step voltages. From this point of view it seems reasonable to ask for an acquisition time of about 1.5 μs. This would allow enough time for other operations such as comparator response, switch closure, etc. Since the step capacitor array generates only 16 voltage levels, it appears that the buffer output will be acceptable once it settles to within 3% of its final value (worst case at full scale). In fact from XCODEC results it follows that even worse settling accuracy would be acceptable (see gain requirements). Therefore a buffer settling in 1.5 μs to within 1% of the final output voltage will easily exceed the requirements for the codec application and will be useful from a design point of view for other applications as well.

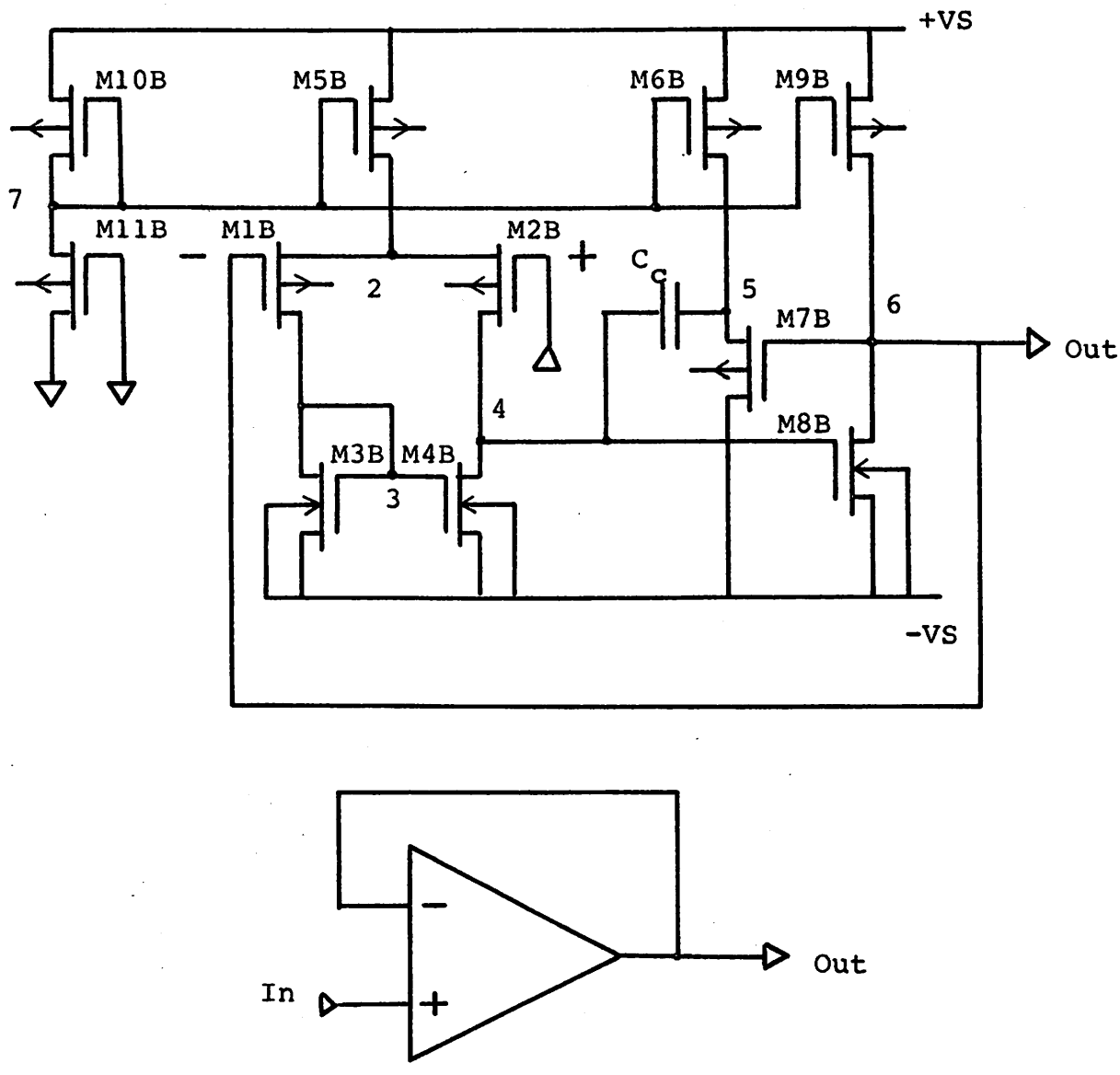
3.2.2 <u>The circuit.</u>

The circuit approach that was chosen is of the classical 741 type using a differential input stage and a common source second stage for level shifting and most of the gain. Since the load driven by the buffer is capacitive there is no need for an output stage with low dc output resistance. Due to the relatively low gm of the MOS transistor, the negative zero introduced by the compensation capacitor is relatively close to the unity gain frequency thus considerably degrading the phase margin. It has been shown ( 3 ) that this undesirable

effect can be eliminated by placing a close to unity gain buffer between the output of the second stage and that side of the compensation capacitor which would be connected otherwise directly to the second stage output. The circuit diagram containing all of the above mentioned components is shown in Figure 3.25.

In the CMOS process used for the codec implementation the n-channel transistors are built in a $p^-$ well which in turn is imbedded in the starting $n^-$ substrate. As a result of this sequence the n-channel transistors exhibit larger body effect than their p-channel counterpart; in fact they are quite ineffective in any other configuration than the one yielding 0 source to body bias. Therefore the circuit presented in Figure 3.25 contains only n-channel transistors which have the source and body connected and the number of such devices is kept to a minimum. A reversed version of the buffer schematic, i.e. n-channel drivers in the input stage etc., would require more than one $p^-$ well in order to accomodate all the n-channel devices and this is obviously space consuming. On the other hand one could argue that under similar bias conditions the p-channel transistor is larger than the n-chanel. This is so not because of the higher carrier mobility in the n-channel device but because of lower breakdown at equal channel length in the p-channel. The higher carrier mobility in the n-channel is counterbalanced by the larger body effect which yields a higher than nominal effective threshold voltage.

Therefore the size difference in favor of the n-channel




CMOS buffer amplifier.

Figure 3.25

(neglecting the $p^-$ well) is determined mainly by the breakdown limitation. The equivalent of the $p^-$ well needed for n-channel transistors is the guard ring required for the isolation of p-channel transistors operating in the analog section of the converters. But guard rings have to be used even between the $p^-$ wells so that it appears that the polarity of devices chosen for the buffer implementation yields less space consumption than the reversed choice would do.

An other argument in favor of the version that was chosen is the fact that p-channel transistors are claimed to be less noisy than n-channel transistors. This is probably the result of fewer processing steps used in the implementation of the p-channel (one diffusion vs. two) which leave the semiconductor material less damaged in the respective locations. If most of the noise is generated by the input stage drivers then the polarity choice that has been made should be helpful.

The bias circuitry consists of a simple two transistor string M10B and M11B. The ratio of the transistor aspect ratios was chosen such as to yield $V_7$ greater than $\frac{VS}{2}$. With VS = 7.5V and $V_{th}$ = -1.5V it turns out that transistors M5B, M6B and M9B will still be saturated when $V_2$, $V_5$ or respectively $V_6$ are within 3.75V - 1.5V = 2.25V of the positive rail; therefore the gain of the second stage will be practically constant up to positive output voltages as high as 5.25V.

The open loop gain will obviously be degraded at such

output (hence input) levels because M5B enters the linear region. But even so, the total gain will be at least equal to the gain of the second stage which is quite sufficient in the codec application. The common mode range can be extended by increasing $V_7$, the final choice being a compromise between common mode range requirements and area. This is so because at constant current the size of M5B, M6B and M9B increases with increasing $V_7$.

In the negative direction the gain will be practically constant until M4B and M8B enter the linear region. This happens when the output (hence input) voltage is equal to $V_3$ - 1.5V. Therefore the lower $V_3$, the more extended the useful negative common mode range will be. For a symmetrical common mode range the choice of $V_7$ is obviously more restrictive than that of $V_3$.

The nominal 0 offset voltage is obtained by mirroring the currents in the two stages.

The actual size of the devices will be determined by the required drive capability, by slew rate requirements and by the stability conditions. These conditions will be derived next.

3.2.3 Stability analysis.

Since the buffer is used in a closed loop configuration it has to satisfy the classical stability conditions:

$$A < 1 \text{ at } \varphi = 180^\circ \tag{3.1}$$

and

$$\varphi < 180^\circ \text{ at } A = 1 \tag{3.2}$$

where:

$$A_B = Ae^{j\varphi} \tag{3.3}$$

is the open loop gain of the buffer amplifier in the presence of the load.

The stability analysis will be performed for both compensation schemes, i.e. with nonbuffered and with buffered compensation capacitor. In order to be able to evaluate the performance of the buffer amplifier under various loading conditions, the amplifier will first be replaced with an equivalent voltage generator. The small signal equivalent circuits used for this exercise are shown in Figure 3.26.

In the section dealing with the CMOS comparator it will be shown that the input stage can be replaced with an equivalent current generator as shown in Figure 3.26. For the time being this replacement will be taken for granted.

The equations yielding the open loop open circuit voltage gain are:

$$gm_1 V_{in} + (G_{o1}+sC_{o1})V_4 + sC_F(V_4-V_6) = 0$$

$$sC_F(V_4-V_6) = gm_8 V_4 + (G_6+sC_6)V_6$$

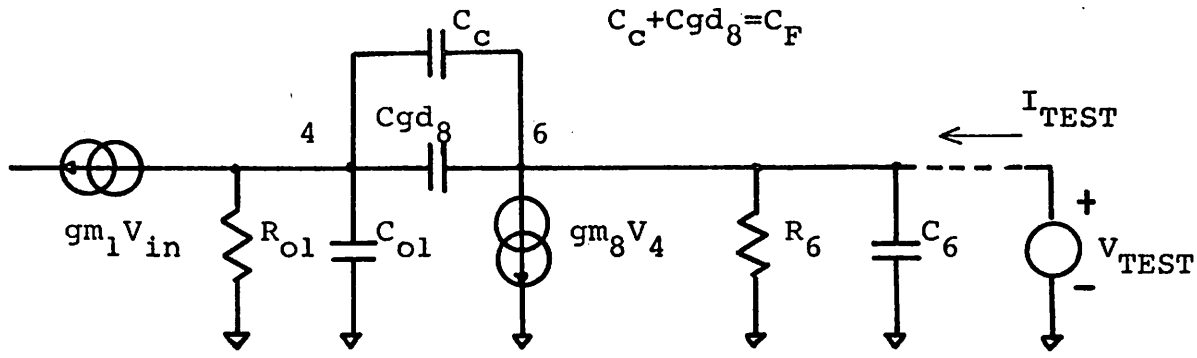
where: $V_{in} = \mathcal{L} v_{in}(t)$, etc.

The essence of this compensation scheme can be highlighted by initially neglecting all capacitors except $C_c$. The result of such an idealization is:

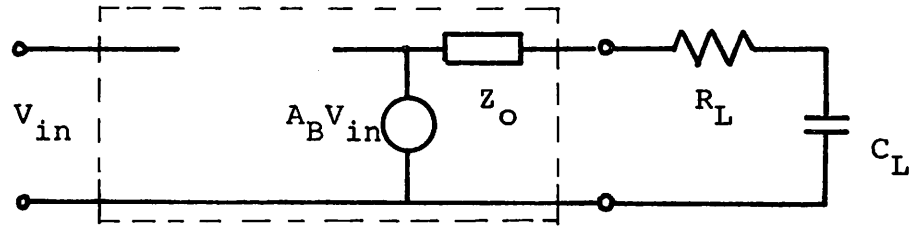
$$A_B^o = \frac{V_6}{V_{in}} = \frac{gm_8 R_6 gm_1 R_{o1}(1-s\frac{C_c}{gm_8})}{1+sC_c(gm_8 R_6 R_{o1}+R_{o1}+R_6)} \qquad (3.4)$$

There is a dominant pole in this expression at a frequency given by:

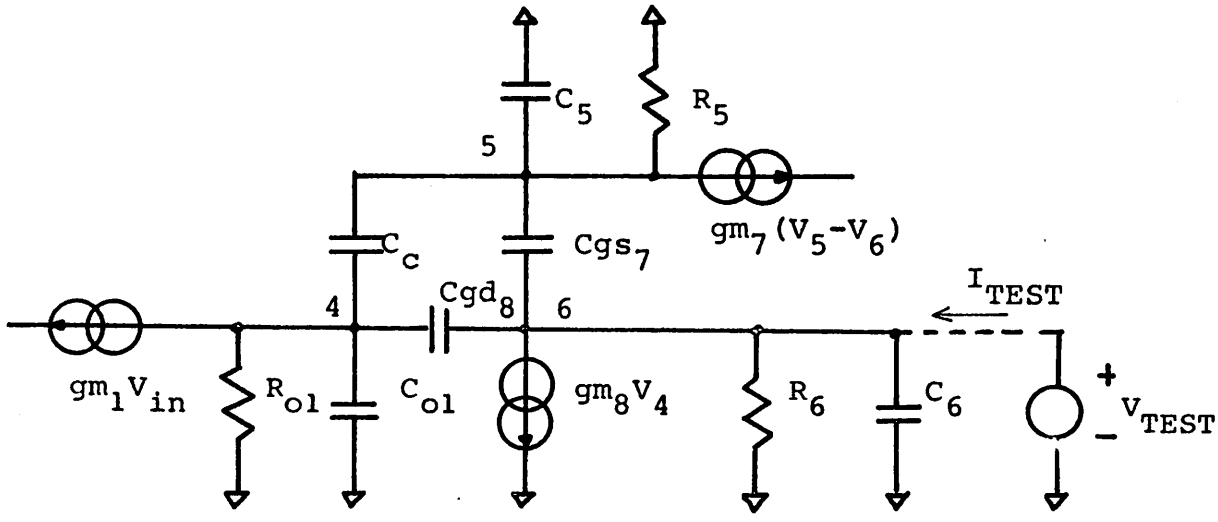
$$\omega_p = \frac{1}{C_c(gm_8 R_6 R_{o1}+R_{o1}+R_6)} \qquad (3.5)$$




(a) Small signal circuit of CMOS amplifier with non-buffered compensation capacitor.




(b) The CMOS amplifier as an equivalent voltage generator.




(c) Small signal circuit of CMOS amplifier with buffered compensation capacitor.

Figure 3.26

and there is clearly a negative zero at:

$$\omega_z = \frac{gm_8}{C_c} \tag{3.6}$$

The unity gain crossover frequency of the nonloaded amplifier will be:

$$\omega_{BW} = \frac{gm_1}{C_c} \tag{3.7}$$

provided that the negative zero occurs beyond this unity gain frequency.

The output impedance of the buffer is found by applying a test generator at node 6 and grounding the input. The equations are:

$$(G_{o1}+sC_{o1})V_4 + sC_F(V_4-V_6) = 0$$

$$I_{TEST} + sC_F(V_4-V_6) = gm_8V_4 + (G_6+sC_6)V_6$$

Neglecting again all capacitors except $C_c$ we find:

$$Z_o = \frac{V_{TEST}}{I_{TEST}} = \frac{V_6}{I_{TEST}} = \frac{R_6(1+sC_cR_{o1})}{1+sC_c(gm_8R_6R_{o1}+R_{o1}+R_6)} \tag{3.8}$$

and beyond the dominant pole, (3.8) can be expressed as:

$$Z_o = \frac{1}{gm_8} + \frac{1}{sgm_8R_{o1}C_c} = R_o + \frac{1}{sC_o} \tag{3.8'}$$

The open loop gain of the loaded amplifier can now be evaluated in a straightforward manner. According to Figure 3.26b and at frequencies beyond the dominant pole:

$$A_B = A_B^o \frac{C_o}{C_o+C_L} \frac{1 + sC_LR_L}{1 + \frac{sC_oC_L}{C_o+C_L}(R_o+R_L)} \tag{3.9}$$

From (3.9) it is apparent that the interaction between load and output impedance generates a doublet with a pole at:

$$\omega_{pL} = \frac{C_o+C_L}{(R_o+R_L)C_oC_L} \tag{3.10}$$

and a zero at:

$$\omega_{zL} = \frac{1}{C_LR_L} \tag{3.11}$$

The small signal equivalent circuit of the amplifier with buffered compensation capacitor is shown in Figure 3.26c.

The equations yielding the open circuit voltage gain are:

$$gm_1V_{in} + (G_{o1}+sC_{o1})V_4 + sCgd_8(V_4-V_6) + sC_c(V_4-V_5) = 0$$

$$sCgd_8(V_4-V_6) + sCgs_7(V_5-V_6) = gm_8V_4 + (G_6+sC_6)V_6$$

$$sC_c(V_4-V_5) + sCgs_7(V_6-V_5) = gm_7(V_5-V_6) + (G_5+sC_5)V_5$$

By following a similar procedure as earlier, we find:

$$A_B^o = \frac{V_6}{V_{in}} = \frac{gm_1R_{o1}gm_8R_6(1+\frac{sC_c}{gm_7})}{1 + sC_c(gm_8R_6R_{o1}+R_{o1}+\frac{1}{gm_7})} \tag{3.12}$$

the only approximation being $gm_7R_5 \gg 1$, i.e. a condition to be expected from a follower.

There is a dominant pole in this expression at:

$$\omega_p = \frac{1}{C_c(gm_8R_{o1}R_6 + R_{o1} + \frac{1}{gm_7})} \tag{3.13}$$

and there is now a true zero at a frequency given by:

$$\omega_z = \frac{gm_7}{C_c} \tag{3.14}$$

The unity gain frequency of the nonloaded amplifier is the same as before, namely the one given by (3.7). This is obviously true only if the zero occurs beyond $\omega_{BW}$.

The output impedance of the amplifier with buffered compensation capacitor is found in a similar manner as earlier:

$$(G_{o1}+sC_{o1})V_4 + sCgd_8(V_4-V_6) + sC_c(V_4-V_5) = 0$$

$$I_{TEST} + sCgd_8(V_4-V_6) + sCgs_7(V_5-V_6) = gm_8V_4 + (G_6+sC_6)V_6$$

$$sC_c(V_4-V_5) + sCgs_7(V_6-V_5) = (G_5+sC_5)V_5 + gm_7(V_5-V_6)$$

Neglecting again , in a first approximation, all the capacitors except $C_c$, we find:

$$Z_o = \frac{R_6(1 + sC_c(R_{o1}+ \frac{1}{gm_7}))}{1 + sC_c(gm_8R_6R_{o1}+R_{o1}+ \frac{1}{gm_7})} \tag{3.15}$$

this result being based on the same assumption of $gm_7R_5 \gg 1$.

The output impedance as given by (3.15) is practically the same as the one given by (3.8). Beyond the dominant pole, again the same in both cases, the output impedance can be expressed as in (3.8′). As a result of all these similarities, the open loop gain of the loaded amplifier with buffered compensation capacitor will be of the form of (3.9) except that $A_B^o$ is the one given by (3.12).

At this point it is clear that the influence of the load

is the same in both cases. By placing the negative and respectively the true zero at the same frequency, the magnitude of the open loop open circuit gain will also be the same. The important difference between the two compensation schemes lies in the way they affect the phase shift. The nonbuffered compensation capacitor will increase the phase shift while the buffered capacitor will decrease it. At the location of the zero the improvement in phase shift is of $90^{\circ}$, certainly a desirable situation.

The neglected capacitors will obviously generate additional singularities. The ratio between the frequencies at which these singularities will occur and the unity gain crossover frequency of the amplifier is of the same order of magnitude with the ratio between the value of the compensation capacitor and the value of those capacitors that have been neglected. These "upper" singularities are determined by process parameters and by the acceptable power dissipation. In the present case, although this may not be necessary, the bandwidth of the buffer has been "stretched" as far as the process would allow at the same time maintaining a comfortable safety margin.

### 3.2.4 Buffer response time.

The response time of the buffer amplifier under small signal conditions can be evaluated by using the gain derived in the previous section. The unity gain compensated amplifier can be considered in this case as being described by a single pole transfer function. If the open loop gain can be expressed

$$A_B = \frac{\omega_{BW}}{s + \omega_p} \tag{3.16}$$

then the closed loop gain can be expressed as:

$$A_B^C = \frac{\omega_{BW}}{s + \omega_{BW} + \omega_p} \cong \frac{\omega_{BW}}{s + \omega_{BW}} \tag{3.17}$$

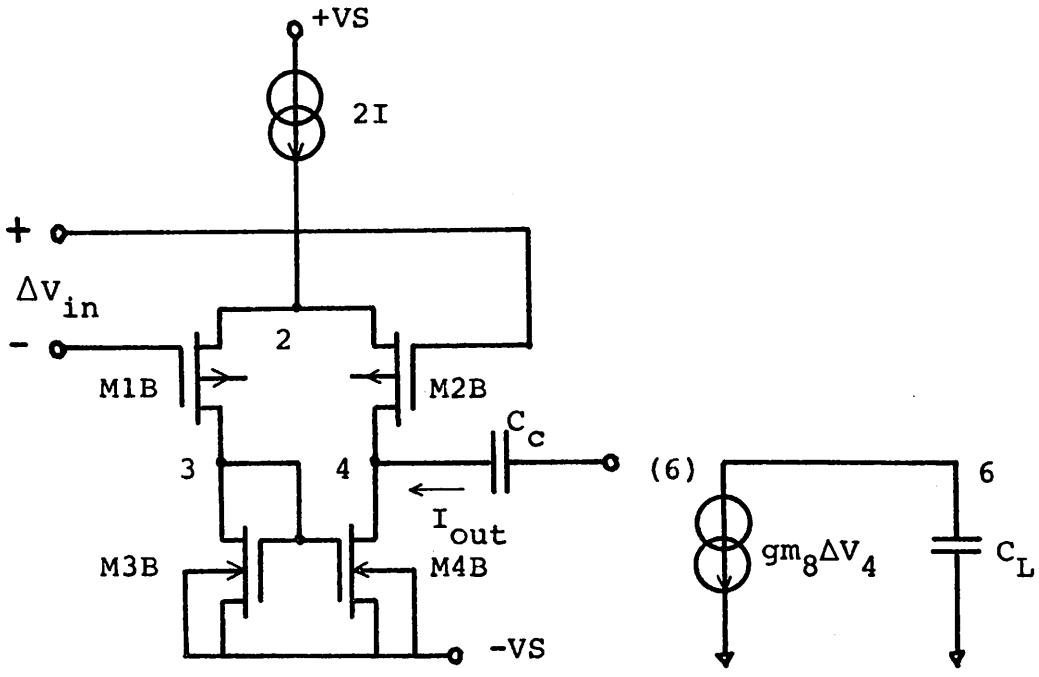
The response of a circuit described by (3.17) to a step input is an exponential with a time constant $\tau = \frac{1}{\omega_{BW}}$.

The output will settle to within .1% of its final value in a time given by:

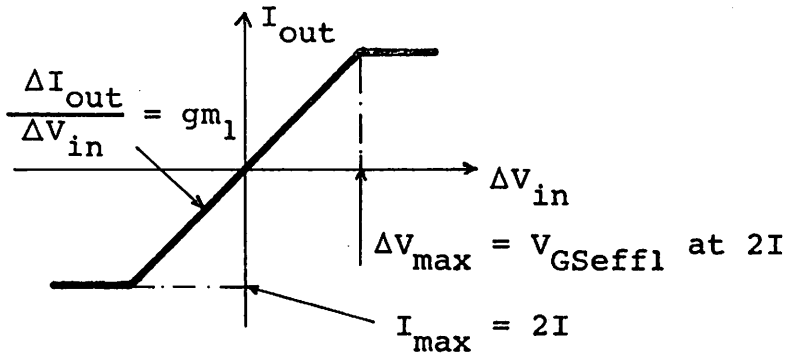
$$\Delta t = \tau \ln 1000 = 6.9\tau \tag{3.18}$$

For sufficiently large input signals, the response time will be limited by the slew rate rather than the small signal bandwith. The equivalent hybrid circuits used to analize this case are presented in Figure 3.27,where all the irrelevant elements have been omitted. The qualitative description of the slewing process goes as follows:

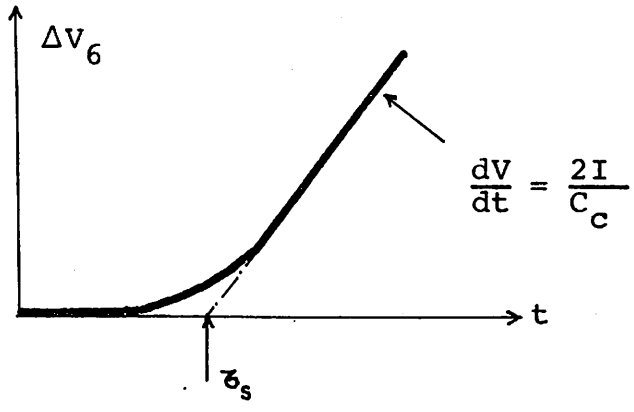
If a positive voltage step is applied to the gate of M2B and the step is sufficiently large, then M2B will be turned off and all of the tail current, 2I, will have to flow through M1B and M3B. Obviously under these conditions the first stage of the amplifier can no longer be described by its small signal parameters. The current 2I flowing through M3B will be mirrored by M4B and, as long as M4B is kept out of the linear region and M2B is shut off, the input stage will act as a current sink of value 2I. This behavior is described by the large signal transconductance characteristic shown in




(a) Hybrid circuit for slewing analysis.




(b) Input stage transconductance.




(c) Step response under slew-rate conditions.

Figure 3.27

Figure 3.27b. In spite of the "drastic" switching occuring in the first stage, the potential at the output of this stage will react more slowly. This is the result of the negative feedback through the compensation capacitor. As long as $V_4$ does not change appreciably, the second stage will still act as a linear amplifier and can be described like in Figure 3.27a.

The equations describing the hybrid circuit of Figure 3.27a are:

$$\Delta V_4 = \Delta V_6 \pm \frac{1}{C_c}\int I_o \, dt$$

$$\Delta V_6 = -\frac{1}{C_L} \, gm_8 \, \Delta V_4$$

With $I_o = 2I$ and using the Lapalce transform we find:

$$\mathcal{L}(\Delta V_4) = \mathcal{L}(\Delta V_6) \pm \frac{2I}{s^2 C_c} \tag{3.19}$$

$$\mathcal{L}(\Delta V_6) = -\frac{gm_8 \, \mathcal{L}(\Delta V_4)}{sC_L} \tag{3.20}$$

From (3.19) and (3.20) we find:

$$\Delta V_4 = \mp \frac{2I\tau_s}{C_c}\left(1 - e^{-t/\tau_s}\right) \tag{3.21}$$

$$\Delta V_6 = \pm \frac{2I}{C_c}\left(t - \tau_s(1-e^{-t/\tau_s})\right) \tag{3.22}$$

where: $$\tau_s = \frac{C_L}{gm_8} \tag{3.23}$$

Expression (3.22) is presented in graphical form in

Figure 3.27c. The results are consistent with the initial assumptions as long as M4B acts as a current sink of value 2I. The biasing parameter that changes at the beginning of the slewing process is the gate drive of M4B, trying to "force" the tail current 2I through M4B. If this can be done at constant $V_4$ then M4B will indeed start as a current sink of value 2I. If M4B is too small to carry the tail current, then M4B will start as a current sink of lesser value than 2I. In any event $V_4$ will tend to decrease in the case of positive step inputs applied at the gate of M2B. From (3.21) it is apparent that $\Delta V_4$ will reach the final value within a time interval of the same order of magnitude with $\tau_s$.

This final value will be:

$$\Delta V_{4\ max} = -\frac{2I}{gm_8}\cdot\frac{C_L}{C_c} = -V_{GSeff}\frac{gm_1}{gm_8}\cdot\frac{C_L}{C_c} \qquad (3.24)$$

where $V_{GSeff}$ is the effective gate to source voltage of M1B, respectively M2B, in equilibrium. Such a voltage step as given by (3.24) could possibly turn off the driver of the output stage, M8B. In this case the slew rate will be:

$$\frac{dV_6}{dt} = \frac{I_9}{C_L} \qquad (3.25)$$

where $I_9$ is the quiescent current of the output stage.

Similar arguments can be used in the case of negative step inputs except that such inputs will not turn off the second stage driver. The conclusions of this analysis are:

- under relatively light loading conditions, i.e. small $C_L$, the output slew rate will be determined by:

$$\frac{dV_6}{dt} = \frac{2I}{C_c} \tag{3.26}$$

- under "heavy" loading conditions, i.e. large $C_L$, the positive slew rate will be determined by (3.25). The fact that the amplifier will be slewing faster in the negative direction than in the positive one is a consequence of the polarity choice that has been made, i.e. n-channel driver and p-channel load in the second stage.

3.2.5 Device sizing.

The elements determining the absolute size of the devices are:

- the speed requirements
- the loading
- the stability conditions
- the available voltage differential

The relation between slew rate and the small signal bandwidth follows from (3.7) and (3.25), respectively (3.26).

For negative slewing:

$$\frac{dV}{dt} = \omega_{BW} V_{GSeff1}$$

For positive slewing under heavy loading:

$$\frac{dV}{dt} = \omega_{BW} V_{GSeff1} \frac{I_9}{2I} \frac{C_c}{C_L}$$

where $V_{GSeff1}$ is the effective gate drive of M1B or M2B.

$V_{GSeff1}$ will be more or less fixed by the available supplies and the nominal threshold voltages. For supplies of $\pm$ 7.5V and nominal thresholds of $\pm$ 1.5V, $V_{GSeff1}$ will be equal to about 2V.

The compensation scheme will be effective only if the unity gain frequency of the open loop configuration is sufficiently removed from the singularities which have been neglected in the stability analysis. Those singularities occur at frequencies of the order of:

$$\omega_T = \frac{gm}{C_{gs}}$$

In terms of process parameters and supplies $\omega_T$ can be expressed as:

$$\omega_T = \frac{2\beta V_{GSeff}}{C_{ox}L^2}$$

where:

$\beta_p$ = 5 $\mu A/V^2$ for p-channel transistors

$\beta_n$ = 10 $\mu A/V^2$ for n-channel transistors

$C_{ox}$ = .22pF/mil$^2$

$L_p$ = .3mil for p-channel transistors

$L_n$ = .2mil for n-channel transistors

With $V_{GSeff}$ of 2V as found earlier:

$$\omega_T \cong 1 \text{ Grad} \quad \text{or} \quad f_T \cong 160 \text{ MHz}$$

From this point of view it seems reasonable to place the unity gain frequency $f_{BW}$ at about 5 MHz., which would yield slew rates of tens of volts per $\mu$s and a small signal settling time of about .22 $\mu$s.

The bandwidth as given by (3.7) is strictly speaking the unity gain crossover frequency of the open loop and unloaded buffer amplifier, provided that $\omega_z$ of (3.14) will occur beyond $\omega_{BW}$. The load will affect the overall gain in the way shown earlier by generating the doublet described by (3.10) and (3.11).The maximum load seen by the buffer corresponds to the generation of step voltages in the last segment when $CX_{128}$ is connected to the buffer output and at the same time is connected in series with the parallel combination of all the other segment capacitors. The resulting capacitance is of about 50pF. A reasonable compensation capacitor size for the desired bandwidth of 5 MHz is equal to about 10pF. Therefore $C_o$ of (3.8') will have a value of about 200pF to 400pF, depending on the exact value of the gain coefficient $gm_8R_{o1}$. The series combination between $C_o$ and $C_L$ will therefore be clearly dominated by the load capacitor $C_L$. It also follows that the doublet will have little influence on the overall gain as long as $R_L \gg R_o$, case in which the pole and zero generated by the load tend to cancel each other. If $R_L \ll R_o$ then the zero of (3.11) will occur beyond the pole of (3.10), the distance between the two being proportional to the ratio of $R_L$ vs. $R_o$. The classical approach in such a case is to place the second pole at the unity gain crossover frequency $\omega_{BW}$. Due to the positive zero given by (3.14), such a choice will yield more than acceptable phase margin.

Thus:

$$\omega_{BW} = \frac{gm_1}{C_c} = \omega_{pL} = \frac{1}{R_o C_L} = \frac{gm_8}{C_L} = 31 \text{ Mrad}$$

It follows that:

$$gm_1 = .314 \text{ mA/V} \quad \text{and} \quad gm_8 = 1.57 \text{ mA/V}$$

The value found for $gm_8$ can now be used for the sizing of the output stage. For $V_{GS8}$ = 25% VS and using a "handmodel" for the transistor we find:

$$k_8 = \frac{gm_8}{2\beta_n (V_{GS8} - V_{th})} = 22$$

This result is deceptive since the handmodel is too simplified in the case of the n-channel transistors used in the particular CMOS process. The discrepancies between the designed and actual parameters are due mainly to the heavy body effect which effectively increases the threshold voltage (as a result of potential distribution along the channel).

The devices can be described more accurately with models of the type available in ISPICE ( 46 ). This has been done and the pertinent parameters have been adjusted for reasonable fitting of experimental data. Using ISPICE we find that for $gm_8$ = 1.57mA/V one needs $k_8$ = 80. The corresponding dc current flowing through the output stage is equal to 700 μA.

By choosing again $V_{GS9}$ = 25% VS we find:

$$k_9 = \frac{I_9}{\beta_p (V_{GS9} - V_{th})^2} = 40$$

This result is in good agreement with computer simulation based on fitted models since the handmodel is more accurate in the case of lightly doped substrate.

The ratio between the gm's of the drivers in the two stages of the amplifier can be realized approximately by setting:

$$I_5 = \frac{I_9}{2}$$

which in turn yields:

$$I_1 = I_2 = \frac{I_9}{4}$$

The size of the input stage drivers is found from:

$$k_1 = k_2 = \frac{\frac{gm_1^2}{4}}{\beta_p I_1} = \frac{gm_1^2}{\beta_p I_9} = 28$$

The sizes of M3B, M4B and M5B are the result of direct scaling:

$$k_5 = \frac{k_9}{2} = 20 \quad \text{and} \quad k_3 = k_4 = \frac{k_8}{4} = 20$$

The slew rates resulting from the choices made so far are:

$$\frac{dV^+}{dt} = \frac{I_9}{C_{Lmax}} = \frac{700\mu A}{50pF} = 14V/\mu s$$

and:

$$\frac{dV^-}{dt} = -\frac{I_5}{C_c} = -\frac{350\mu A}{10pF} = 35V/\mu s$$

The small signal settling time of (3.18) will be of about .22$\mu$s. Such values are quite acceptable in the codec application.

The current flowing through the follower used for the buffering of the compensation capacitor has to be at least equal with the tail current of the input stage. Otherwise the follower rather than the input stage would limit the slew rate. Therefore $I_6 = I_5$. For stability reasons the pozitive zero of (3.14) has to be placed beyond $\omega_{BW}$; otherwise the amplifier could be unstable in the absence of a heavier load. The location of the zero was arbitrarily chosen as:

$$\omega_z \cong 2\,\omega_{BW}$$

Such a choice yields $gm_7 = .68mA/V$ and $k_7 = 53$.

The size of M6B is obviously such as to yield $k_6 = k_5$.

Once the aspect ratios have been found, the absolute size of the devices depends on the choice of channel length.

The channel length that was chosen, .3mil for p-channel transistors and .2mil for n-channel transistors, is the minimum value compatible with reasonable breakdown voltages and saturated output resistance. The final values of the geometrical parameters are shown in TABLE 3.8 which contains the ISPICE circuit description of the CMOS buffer amplifier.

### 3.2.6 Computer evaluation.

The performance of the "paper amplifier" was evaluated using ISPICE. The circuit description that was used is shown in TABLE 3.8. The dc biasing conditions and small signal parameters are listed in TABLE 3.9. The computer analysis does obviously take into account all the elements which have been neglected during the simplified analysis performed earlier.

The open loop gain and the output impedance of the amplifier with buffered compensation capacitor are shown in Figure 3.28a, respectively 3.28b. The output impedance of the nonbuffered version is shown in Figure 3.28c. It is clear that the two output impedances are practically identical within the bandwidth of the amplifier; therefore it is indeed justified to compare the two compensation schemes based on the open loop gain alone.

The results of the computer analysis performed under maximum loading conditions are shown in Figure 3.29a for the buffered version and Figure 3.29b for the nonbuffered version.

The maximum load, $C_L$ = 50pF, is connected to the buffer output via an equivalent switch resistor of .5k. This resistor is comparable to the output resistance of the amplifier so that the case is indeed worst from a stability point of view.

The bandwidth in the presence of the load is practically the same in both cases. The nonbuffered version exhibits an additional phase shift of about $20^{o}$, but the phase margin of $45^{o}$ is still acceptable.

The step response under similar loading conditions is

Circuit description of CMOS buffer.

```
M1B 3 6 2 8 PSGX(6.4,6.4,8.0MI) 8.0MI,.3MI
M2B 4 1 2 8 PSGX(6.4,6.4,8.0MI) 8.0MI,.3MI
M3B 3 3 9 9 NSGX(3.2,3.2,4.0MI) 4.0MI,.2MI
M4B 4 3 9 9 NSGX(3.2,3.2,4.0MI) 4.0MI,.2MI
M5B 2 7 8 8 PSGX(2.4,2.4,6.0MI) 6.0MI,.3MI
M6B 5 7 8 8 PSGX(4.8,4.8,6.0MI) 6.0MI,.3MI
M7B 9 6 5 8 PSGX(12.8,12.8,16.0MI) 16.0MI,.3MI
M8B 6 4 9 9 NSGX(12.8,12.8,16.0MI) 16.0MI..2MI
M9B 6 7 8 8 PSGX(9.6,9.6,12.0MI) 12.0MI,.3MI
M10B 7 7 8 8 PSGX(.88,.88,1.5MI) 1.5MI,.3MI
M11B 0 0 7 8 PSGX(.88,.88,1.2MI) 1.2MI,.4MI
D 9 4 D
MODEL D D(CJO=54*.173p,IS=54*20p)
CC 4 5 10P
Vplus 8 0 7.5
Vminus 9 0 -7.5

PSGX MODEL
PSGX(DR,SO,W)
PSCM(VTO=1.5,PHI=.575,UO=300,NB=.95E+15,CO=4.0E-8,&
IS=1.0E-16,C1=8.7P,C2=8.7P,CBD=DR*.066P/W,CBS=SO*.066P/W,&
PB=.7,RS=10MI,RD=10MI,MN=1.2,KN=.0354)

NSGX MODEL
NSGX(DR,SO,W)
NSCM(VTO=1.5,PHI=.675,UO=700,NB=1.1E+16,CO=4.0E-8,&
IS=1.0E-16,C1=19.4P,C2=19.4P,PB=.7,RD=10MI,RS=10MI,&
CBD=DR*.173P/W,CBS=SO*.173P/W,KN=.007,MN=1.12,&
ECRIT=8.5E+4,KL=2)
```

TABLE 3.8

| | VGS (V) | VDS (V) | ID (μA) |
|---|---|---|---|
| M1B | -3.128 | -8.122 | 166.9 |
| M2B | -3.129 | -8.091 | 167.0 |
| M3B | 2.507 | 2.507 | 166.9 |
| M4B | 2.507 | 2.537 | 167.0 |
| M5B | -3.239 | -4.371 | 334.0 |
| M6B | -3.239 | -4.400 | 334.4 |
| M7B | -3.099 | -10.60 | 334.4 |
| M8B | 2.537 | 7.501 | 767.6 |
| M9B | -3.239 | -7.499 | 767.6 |
| M10B | -3.239 | -3.239 | 78.7 |
| M11B | -4.261 | -4.261 | 78.7 |

(a) Dc biasing conditions.

| | gm (mA/V) | gds (μA/V) | Cgs (pF) | Cgd (pF) |
|---|---|---|---|---|
| M1B | .33 | 4.54 | .6 | .17 |
| M2B | .33 | 4.54 | .6 | .17 |
| M3B | .33 | 3.50 | .34 | .19 |
| M4B | .33 | 3.48 | .34 | .19 |
| M5B | .36 | 16.50 | .44 | .13 |
| M6B | .36 | 16.50 | .44 | .13 |
| M7B | .68 | 8.85 | 1.18 | .35 |
| M8B | 1.46 | 10.23 | 1.37 | .79 |
| M9B | .84 | 31.63 | .88 | .26 |
| M10B | .08 | 4.45 | .11 | .03 |
| M11B | .06 | 1.95 | .11 | .02 |

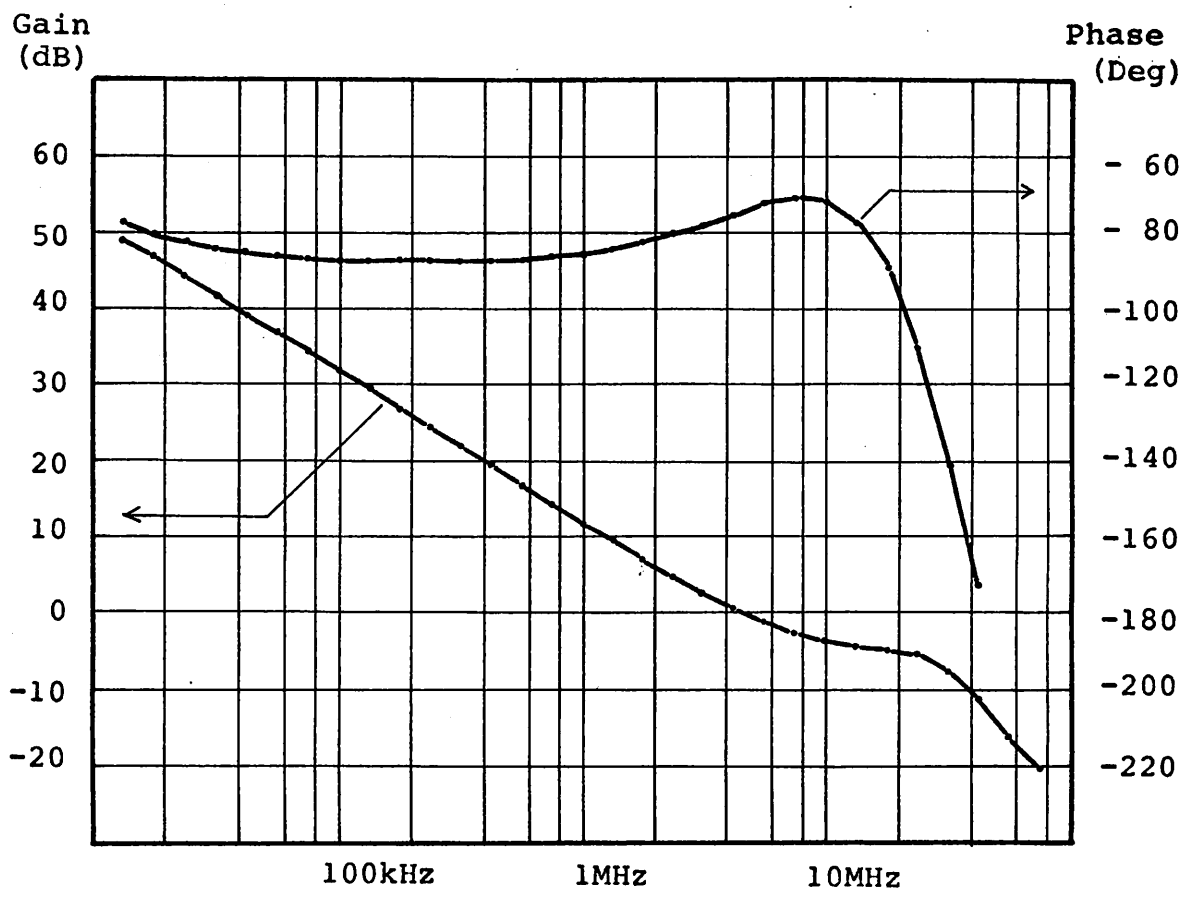
(b) Small signal parameters.

TABLE 3.9

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $Cjd_1$ | = | .10pF | $Cjd_10$ | = | .42pF | $V_{rev}$ | = 12.5V |
| $Cjs_1$ | = | .16pF | $Cjs_10$ | = | .42pF | $V_{rev}$ | = 4.4V |
| $Cjd_2$ | = | .10pF | $Cjd_20$ | = | .42pF | $V_{rev}$ | = 12.5V |
| $Cjs_2$ | = | .16pF | $Cjs_20$ | = | .42pF | $V_{rev}$ | = 4.4V |
| $Cjd_3$ | = | .26pF | $Cjd_30$ | = | .55pF | $V_{rev}$ | = 2.5V |
| $Cjd_4$ | = | .26pF | $Cjd_40$ | = | .55pF | $V_{rev}$ | = 2.5V |
| $Cjd_5$ | = | .06pF | $Cjd_50$ | = | .16pF | $V_{rev}$ | = 4.4V |
| $Cjd_6$ | = | .12pF | $Cjd_60$ | = | .32pF | $V_{rev}$ | = 4.4V |
| $Cjs_7$ | = | .31pF | $Cjs_70$ | = | .84pF | $V_{rev}$ | = 4.4V |
| $Cjd_8$ | = | .65pF | $Cjd_80$ | = | 2.21pF | $V_{rev}$ | = 7.5V |
| $Cjd_9$ | = | .18pF | $Cjd_90$ | = | .63pF | $V_{rev}$ | = 7.5V |
| $C_{j4}$ | = | 4.37pF | $C_{j4}0$ | = | 9.34pF | $V_{rev}$ | = 2.5V |

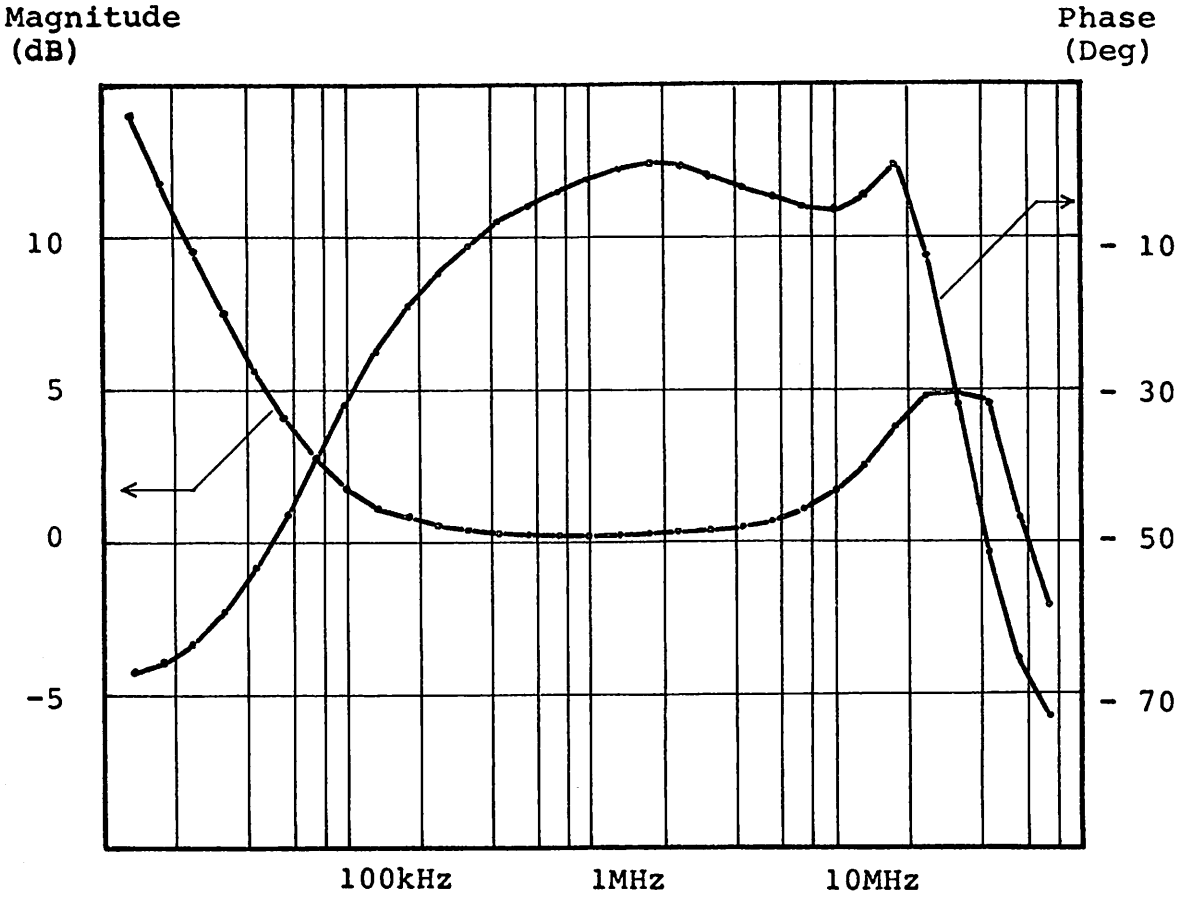
(c) <u>Junction capacitances.</u>

TABLE 3.9




(a) Open loop gain/phase characteristics of the CMOS buffer amplifier with buffered compensation capacitor. No load.

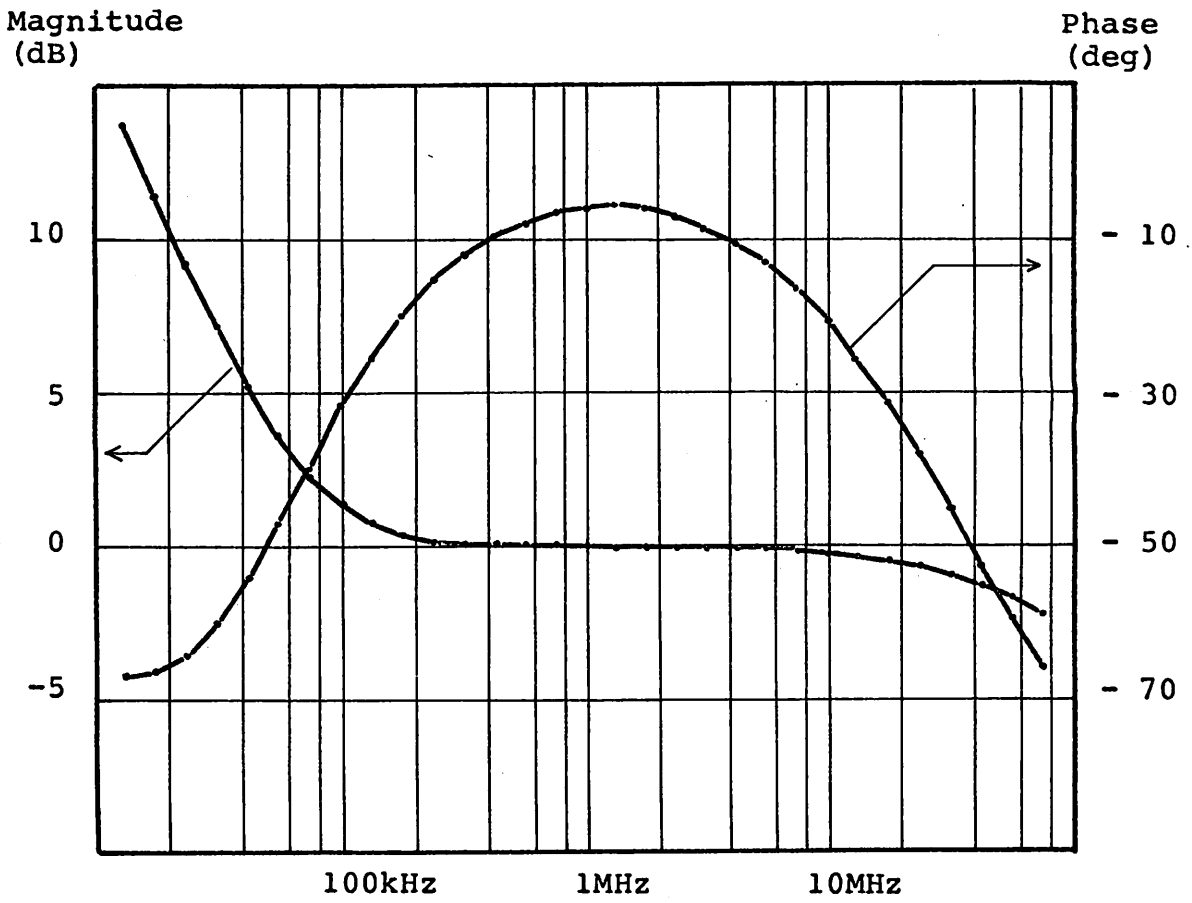
Figure 3.28




(b) Output impedance of the CMOS buffer amplifier with buffered compensation capacitor.

( 0dB corresponds to a 1k resistor)

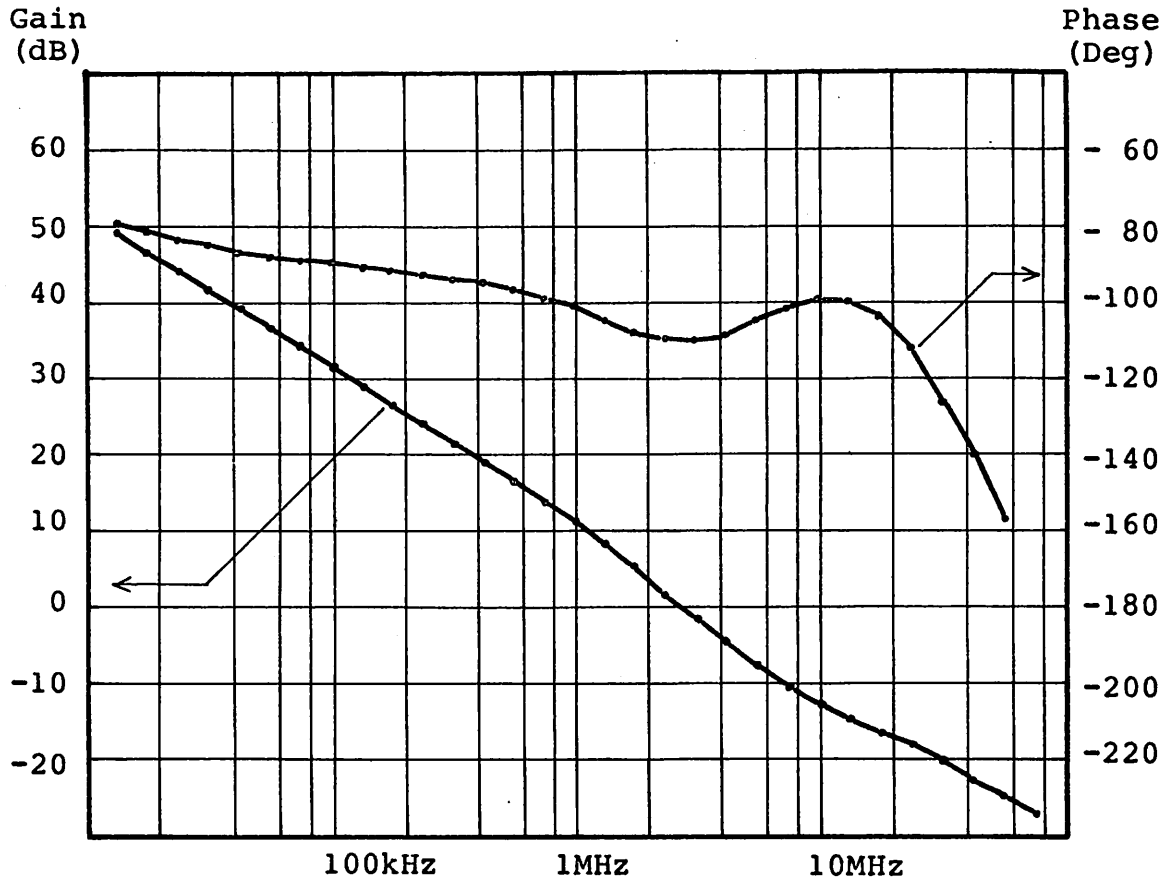
Figure 3.28




(c) <u>Output impedance of the CMOS buffer amplifier with nonbuffered compensation capacitor.</u>

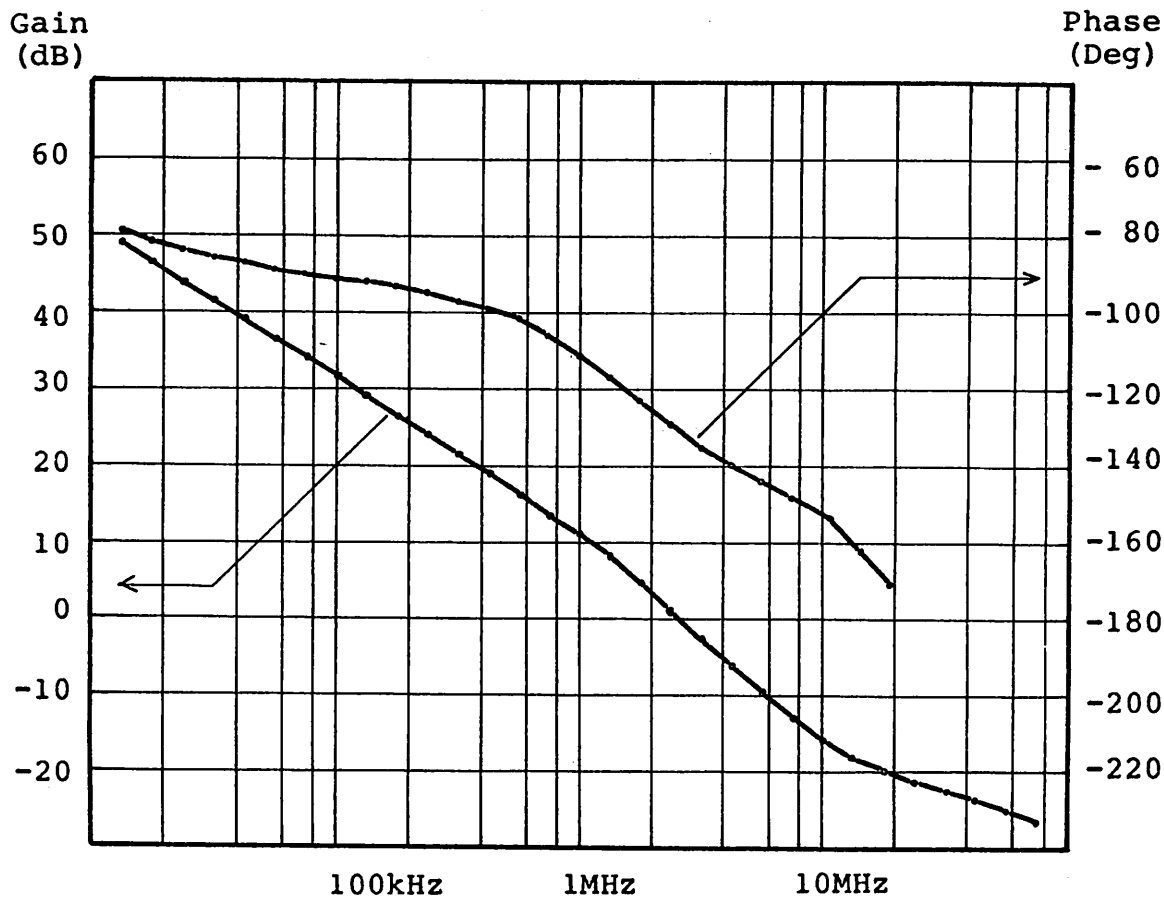
(0dB corresponds to a 1k resistor)

Figure 3.28




(a) Open loop gain/phase characteristics of the CMOS buffer amplifier with buffered compensation capacitor. The amplifier is loaded with $C_L$=50pF and $R_L$=.5k.

Figure 3.29




(b) Open loop gain/phase characteristics of the CMOS buffer amplifier with non-buffered compensation capacitor. The amplifier is loaded with $C_L$=50pF and $R_L$=.5k.

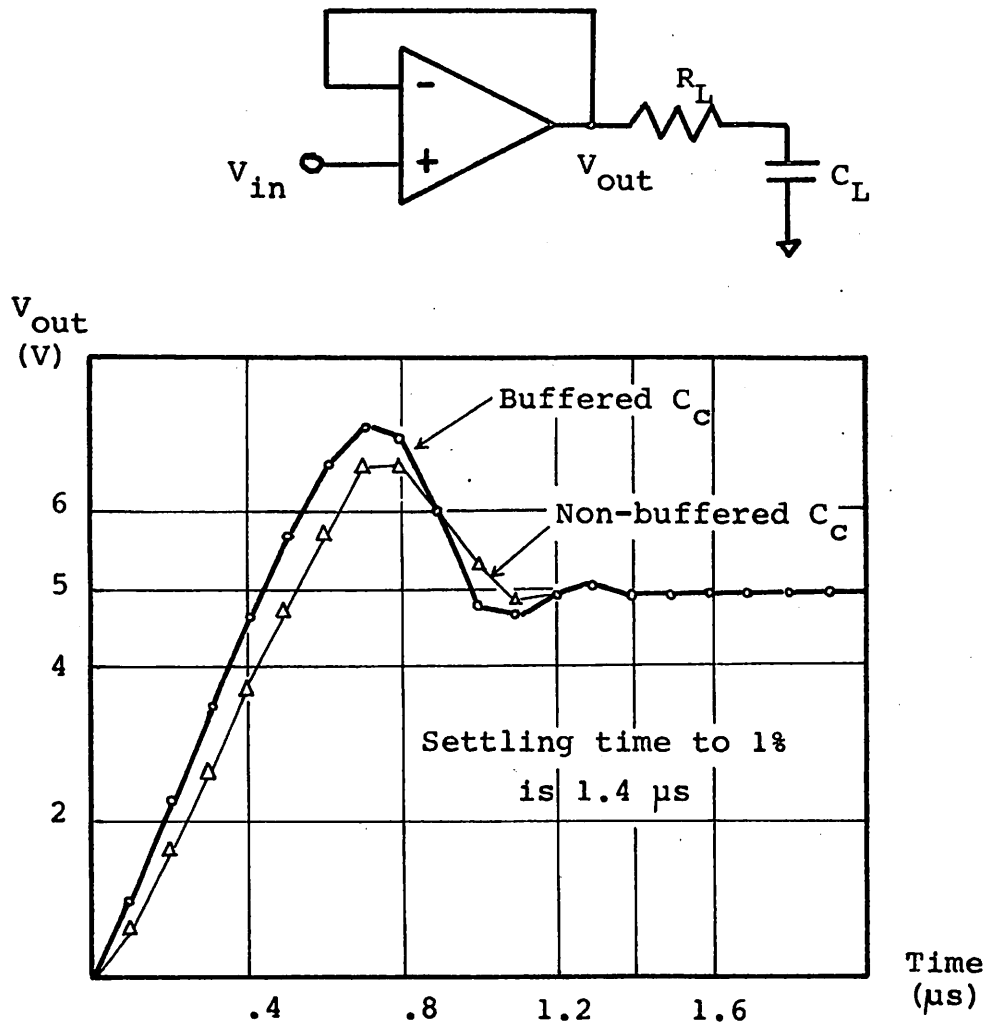
Figure 3.29

shown in Figure 3.30.

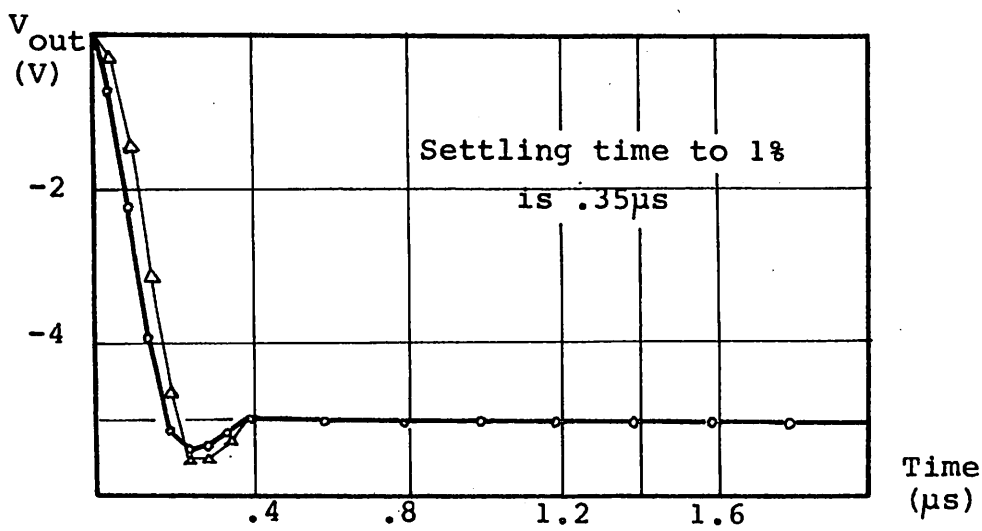
The computer results are consistent with the simplified analysis of the previous sections, showing that the approximations have been reasonable.

It appears that the follower used for the buffering of the compensation capacitor could be eliminated; the penalties are: $20^{\circ}$ more phase shift at the unity gain crossover frequency, 3V/μs less positive slew rate and 4V/μs less negative slew rate. The savings would be: 15% less area and 25% less power dissipation. Since it was felt that the advantages of the buffered version are worth the area and power penalties, the follower was nevertheless included in the practical circuit.

The final parameters of the buffer amplifier are listed in TABLE 3.10.




(a) Step response to positive input.




(b) Step response to negative input.

Figure 3.30

| | Simul. | Measr. |
|---|---|---|
| Open loop dc gain | 62dB | 60-66dB |
| Bandwidth (open circuit) | 5MHz | - |
| Phase margin (open circuit) | $106^{o}$ | - |
| Bandwidth ($C_L$ = 50pF and $R_L$ = .5k) | 3MHz | - |
| Phase margin ($C_L$ = 50pF and $R_L$ = .5k) | $70^{o}$ | - |
| Common mode range | $\pm$5V | $\pm$5V |
| Common mode rejection | - | 60dB |
| Input offset | - | 20mV |
| Positive slew rate (loaded with $C_L$, $R_L$) | 13V/us | 8V/us |
| Negative slew rate (loaded) | 34V/us | 33V/us |
| Power dissipation | 22mW | 20mW |
| Area | $560mil^2$ | $560mil^2$ |

Computed and measured performance of CMOS buffer amplifier.

TABLE 3.10

### 3.2.7 Experimental results.

The practical performance of the buffer amplifier was evaluated using a special metal mask which brings out the input and output terminals of the amplifier alone.

The experimental common mode range is shown in Figure 3.E7 and is practically $\pm 6V$ at $\pm 7.5V$ supplies.

The open loop gain is measured with the setup shown in Figure 3.E8 on the basis of:

$$A = \frac{\Delta V_{out}}{\Delta (V_{in} - V_{out} + V_{offs})}$$

where: $V_{offs} = V_{out}$ at $V_{in} = 0$

This experiment shows that $A > 1000$, i.e. adequate for the codec application.

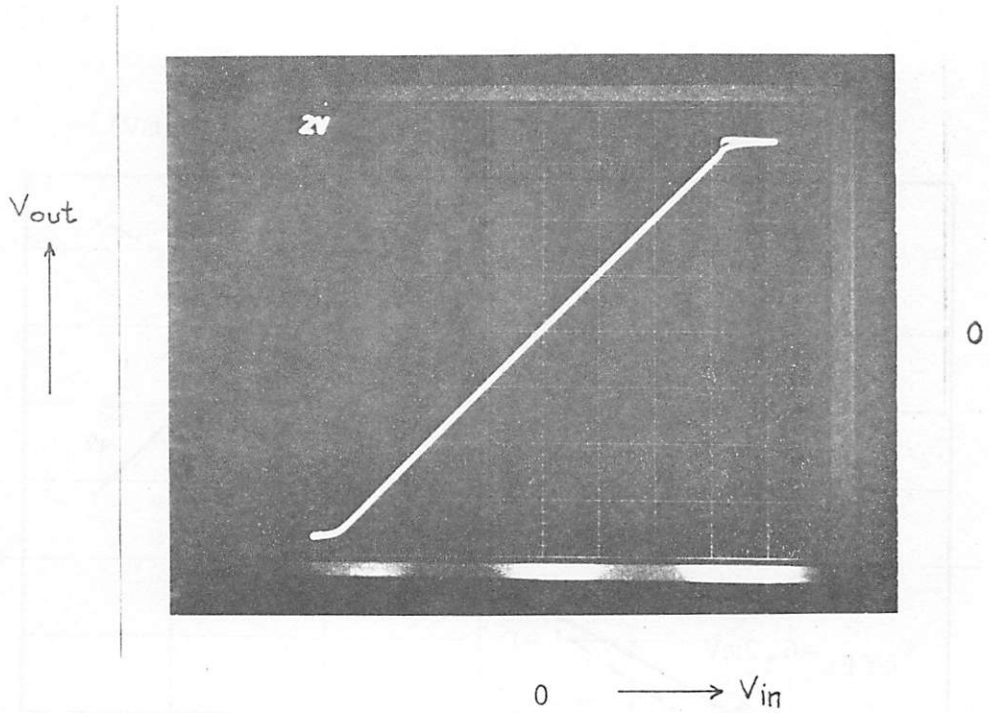
The measured offset voltage is of the order of a few tens of mV, which is again acceptable in the codec.

The step response is shown in Figures 3.E9 to 3.E12.

The magnitude of the input step is 5V and the load consisted of a 50pF capacitor connected to the amplifier output via a .5k resistor. The experimental slew rates are:

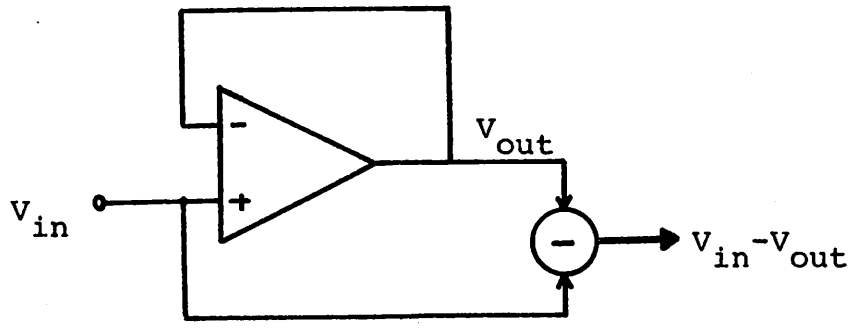
$$\frac{dV^+}{dt} = \frac{10V}{\mu s} \qquad \text{and} \quad \frac{dV^-}{dt} = -\frac{30V}{\mu s}$$

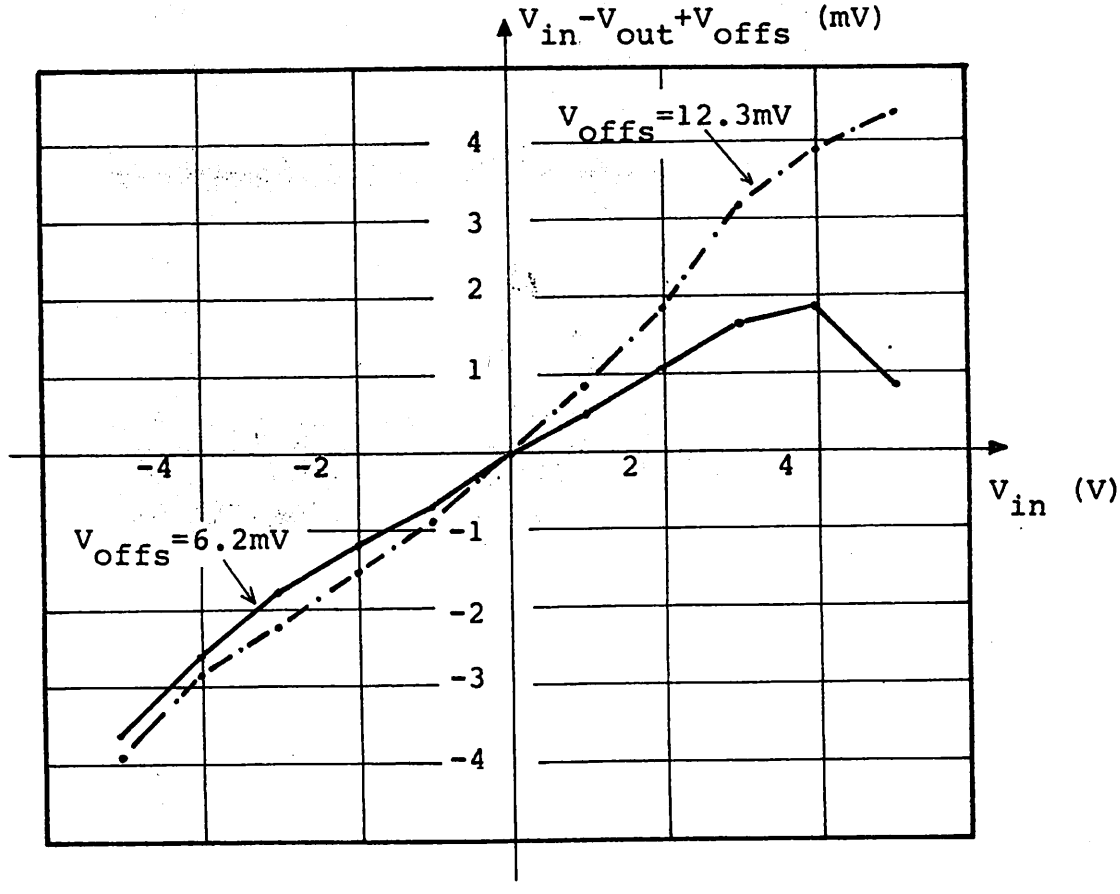
These results are reasonably close to the computer predictions; they happen to be equal to the idealized results obtained for the nonbuffered compensation version, which shows that the decision to keep the follower was justified since the practical degradation of slew rate could otherwise become critical.




Dc transfer characteristic of unity gain CMOS buffer amplifier.

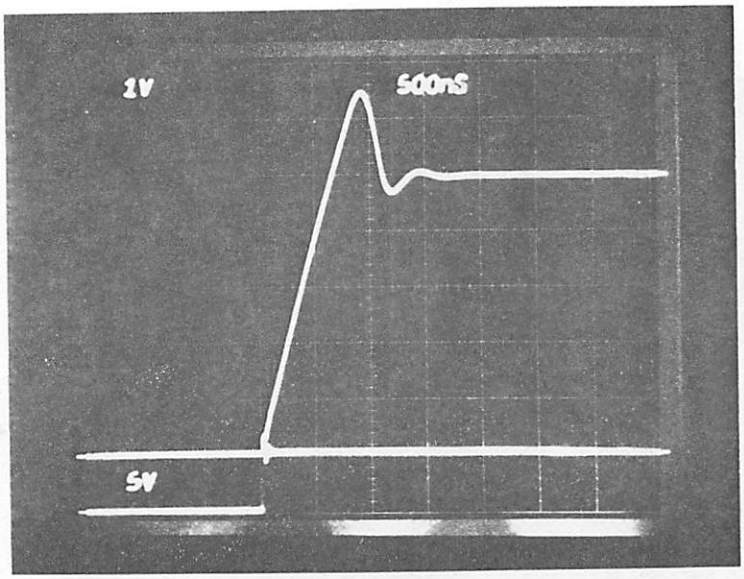
Figure 3.E7



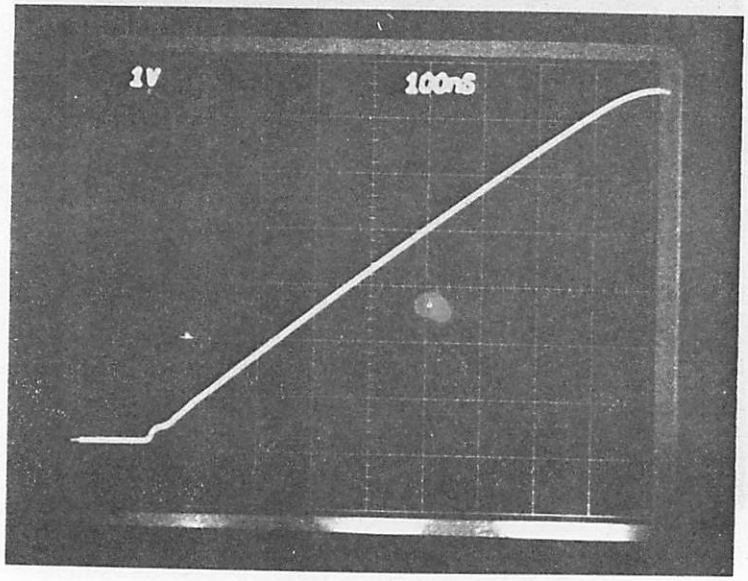

Experimental set-up for gain measurement.
and measured results for 2 samples.

Figure 3.E8



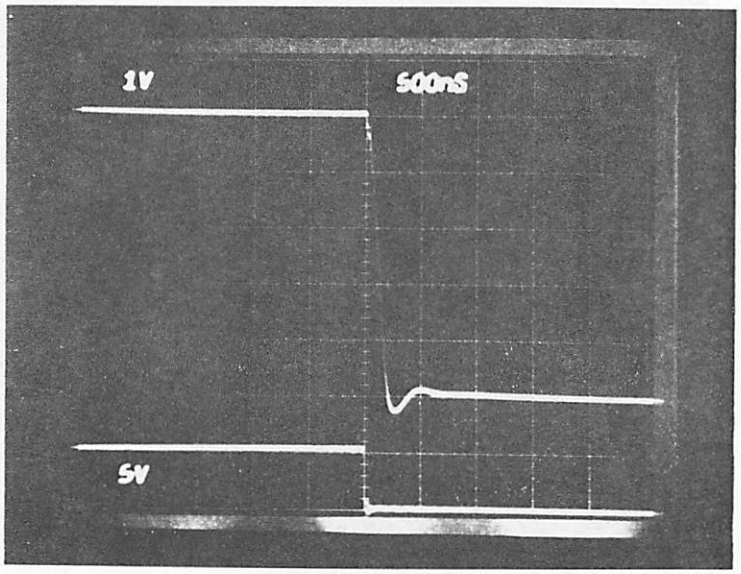

CMOS amplifier response to a positive 5V input step; $C_L$ = 50pF and $R_L$ = .5k.

Figure 3.E9



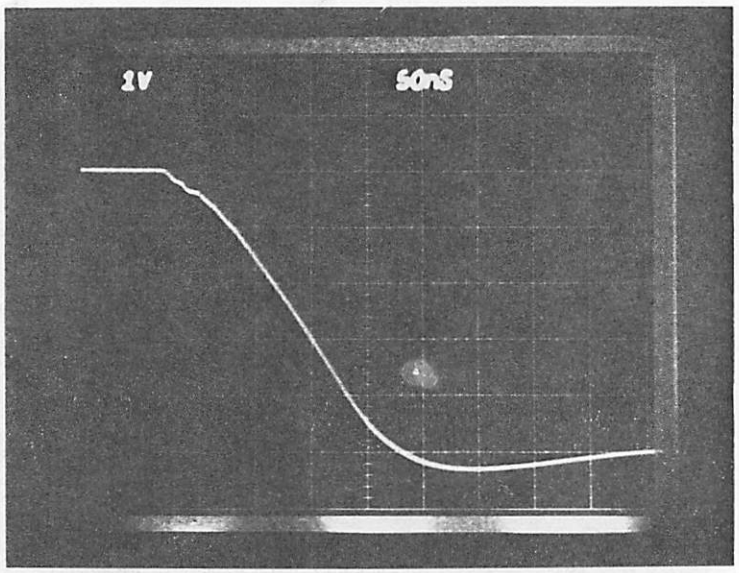

CMOS amplifier response to a positive 5V input step (magnified); $C_L$ = 50pF and $R_L$ = .5k.

Figure 3.E10




CMOS amplifier response to a negative 5V input step; $C_L$ = 50pF and $R_L$ = .5k.

Figure 3.E11




CMOS amplifier response to a negative 5V input step (magnified); $C_L$ = 50pF and $R_L$ = .5k.

Figure 3.E12

## 3.3 THE CMOS COMPARATOR.

The need for a comparator is obvious in an analog to digital converter. The circuitry used for this purpose in the first charge-redistribution converter (8) consisted of a broadband linear gain stage cascaded with a sense amplifier.

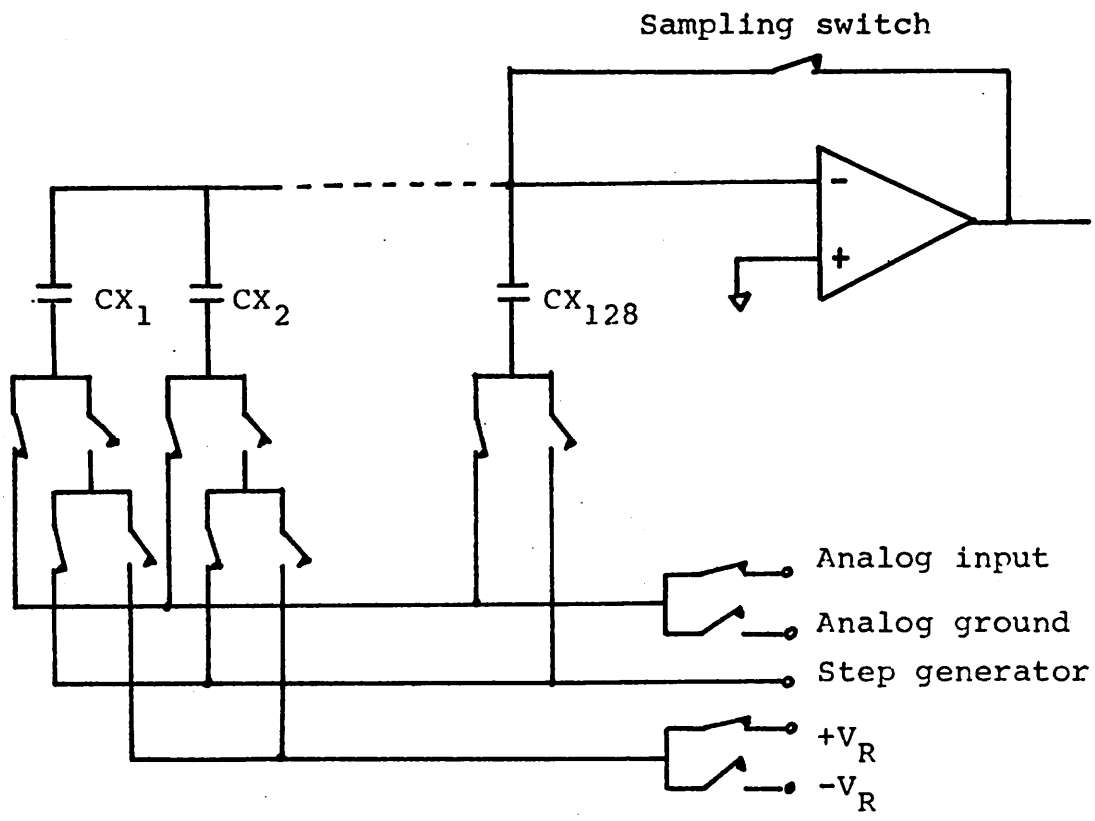
The linear stage is needed for offset cancellation and since the converter was built in n-channel technology, the moderate gain of this stage had to be supplemented by the "infinite" gain of the positive feedback sense amplifier.

The sense amplifier requires dedicated switching circuitry which can be space consuming and will certainly complicate the layout. A linear amplifier with sufficient gain would therefore be a more attractive solution and with the availability of complementary devices it can also become a practical one.

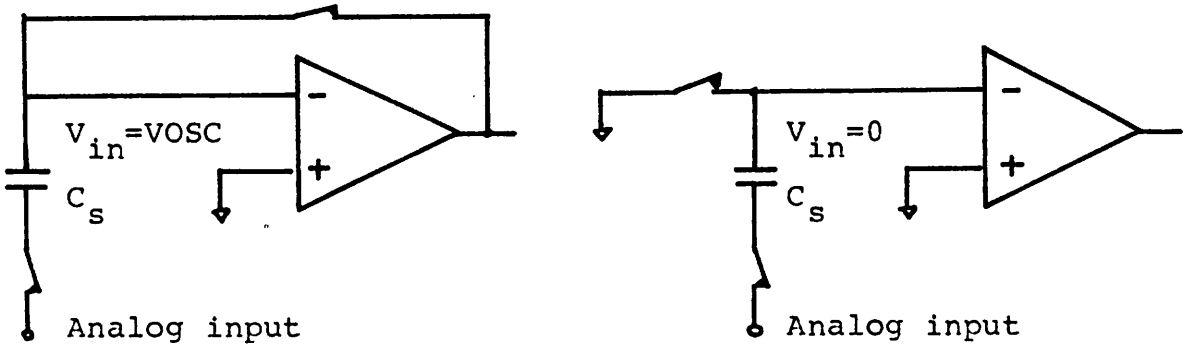
### 3.3.1 Design objectives.

The comparator has two roles in the PCM coder: during the sampling of the analog input signal it provides a virtual ground for the charging path and during the conversion it compares the voltage at the common top plate of the segment array capacitors against that virtual ground. The virtual ground is created by connecting one end of the "sampling switch" to the output of the comparator rather than directly to ground and by grounding the noninverting input of the comparator. This is shown in Figure 3.31. Such a connection will eliminate the effect of the finite comparator offset voltage.

If one would ground the top plates during sampling




(a) Switch configuration during input sampling




(b) (c)

Simplified sampling configuration
(b) with offset cancellation
(c) without offset cancellation

Figure 3.31

then the voltage presented at the inverting input of the comparator during the conversion would be referenced to the electrical ground and as a result the transfer curve of the coder would be shifted by an amount equal to the comparator offset voltage. If this shift is too pronounced the codec will fail passing SNR and GTRCK specifications.

The acceptable offset was found through computer simulation using XCODEC; it is equal to 2% of $V_R$, in the case when all the other parameters of the converters are perfect. With a reference voltage of 3V this implies an acceptable offset of about 60mV and since the practical offset is likely to be of the same order of magnitude it turns out that it has to be eliminated from the comparison. By connecting the sampling switch "around" the comparator, the offset is stored on the capacitor array itself and will no longer affect the comparison process. The effective comparator offset will be the result of feedthrough from the sampling switch and this then has to be less than 2% of $V_R$.

The sampling switch - comparator combination has to provide an acceptable impedance during sampling and the resulting feedback configuration has to be stable.

During conversion the comparator has to be able to switch state at an input overdrive as small as $V_R/8160$, corresponding to one half of a step in the middle segment of the transfer curve. Therefore the comparator has to exhibit a dc gain larger than:

$$G_{min} = \frac{dV_{out}}{dV_{in}} = 8160 \frac{V_T}{V_R}$$

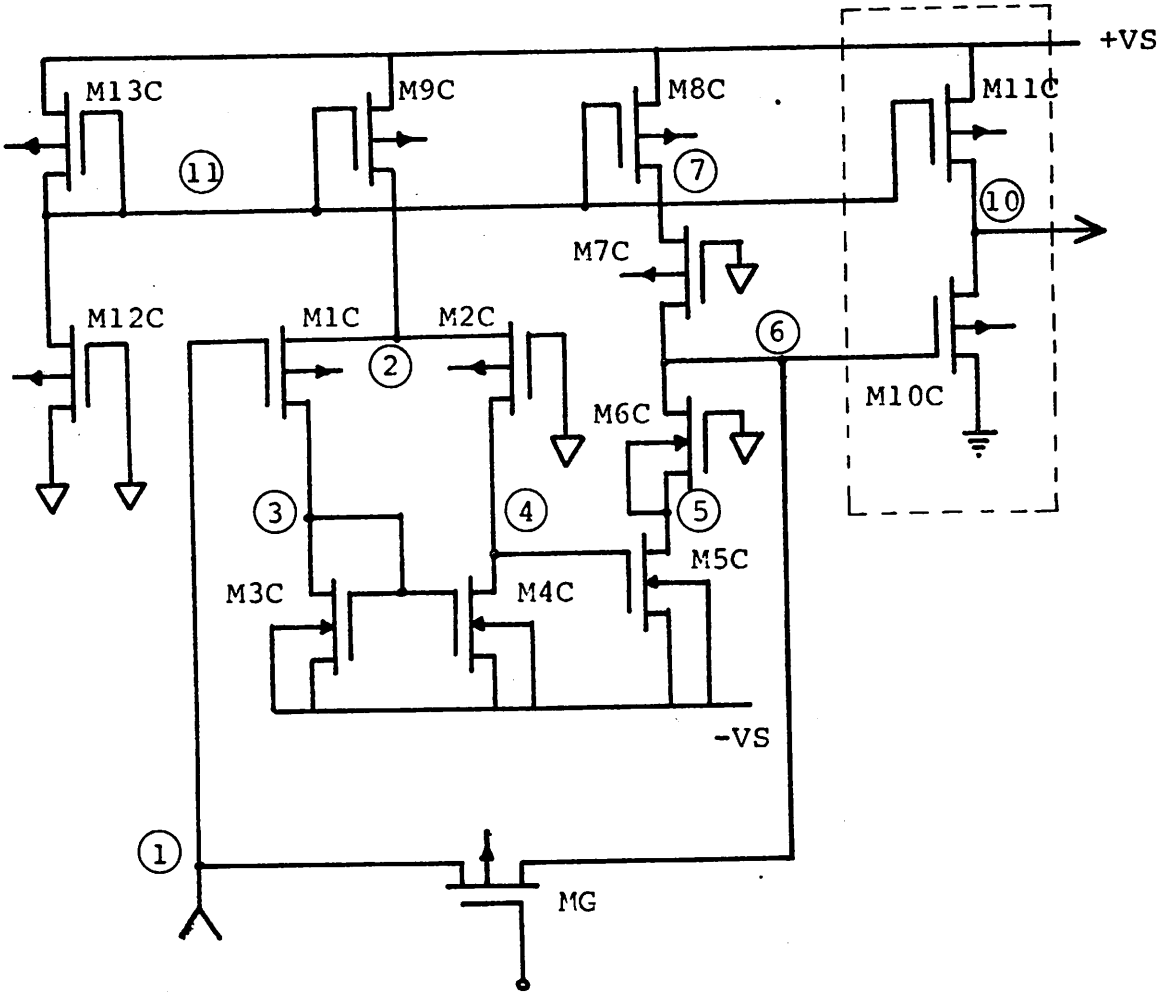
where $V_T$ is the trigger voltage of the inverter following the comparator. The maximum acceptable response time is determined by the length of the time slot alloted for one decision and the number of operations performed during that time slot. A reasonable limit is equal to about 2 $\mu$s; added to the 1.5 $\mu$s assigned for buffer settling this yields a total of 3.5 $\mu$s. The duration of an entire time slot is of 10 $\mu$s at a sampling rate of 8 kHz and 5 $\mu$s at 16 kHz. Therefore it appears that the choices made so far allow sufficient time for logic operations and charge redistribution.

### 3.3.2 The circuit.

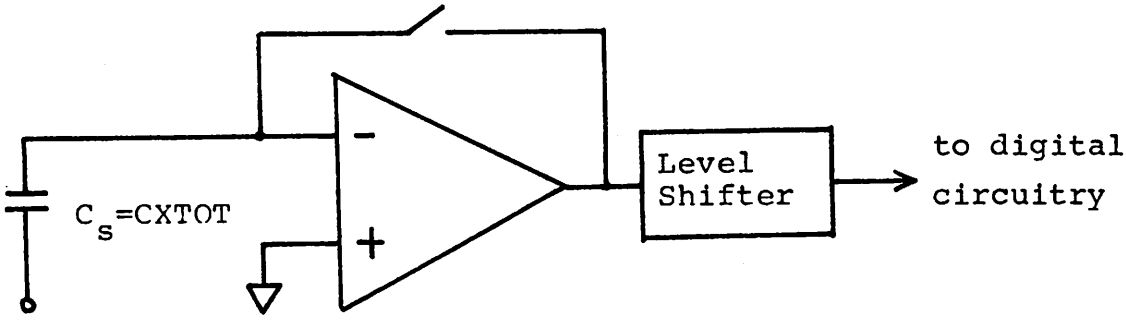
The circuit appproach chosen for the comparator is shown in Figure 3.32. The reasons for using p-channel drivers in the input stage and n-channel in the cascode are similar to the ones presented in the buffer section.

The differential input stage provides the possibility for choosing a convenient comparator threshold. One may be tempted to set this at the logic threshold of the digital circuitry but such a choice is unfavorable from a biasing point of view. The comparator has to exhibit the largest gain around its threshold and it turns out that the most convenient biasing arrangement for maximum gain requires setting of the threshold at ground. This solution does also provide the most flexibility for the choice of reference voltages.

The second stage of the comparator is a cascode, used here for its large dc gain and its small input capacitance.




Sampling switch




CMOS Comparator

Figure 3.32

The level shifter, M10C and M11C, translates the 0 centered voltage swing at the output of the comparator to the logic threshold centered voltage swing required to drive the digital section; it also buffers the comparator output from the capacitive load presented by the digital circuitry.

M10C and M11C are scaled with the bias string transistors M12C and M13C and these in turn are built of equal size; therefore the bias potential $V_{11}$ will be at about +VS/2, which is above the logic threshold of a CMOS inverter biased at +VS. As a result of the scaling $V_{10}$ will be equal with $V_{11}$ when $V_6 = 0$, i.e. during sampling. Therefore the digital circuitry will be set into a definite state during sampling and this process will not be affected by noise resulting from random switching.

By virtually setting the comparator threshold at ground potential the biasing of the cascode is greatly simplified, namely the gates of transistors M6C and M7C can be tied directly to ground. This connection saves unnecessary biasing circuitry and improves the dynamic behavior of the circuit.

The arrangement does also make the best use of the available supplies by evenly distributing the voltage over the four devices in the cascode. The gain of the comparator will be large over an output range of about $2V_{th}$ centered around 0; but this is exactly the region where the most gain is required, therefore the somewhat limited output common mode range resulting from the biasing of M6C and M7C is not "harmful" in this application.

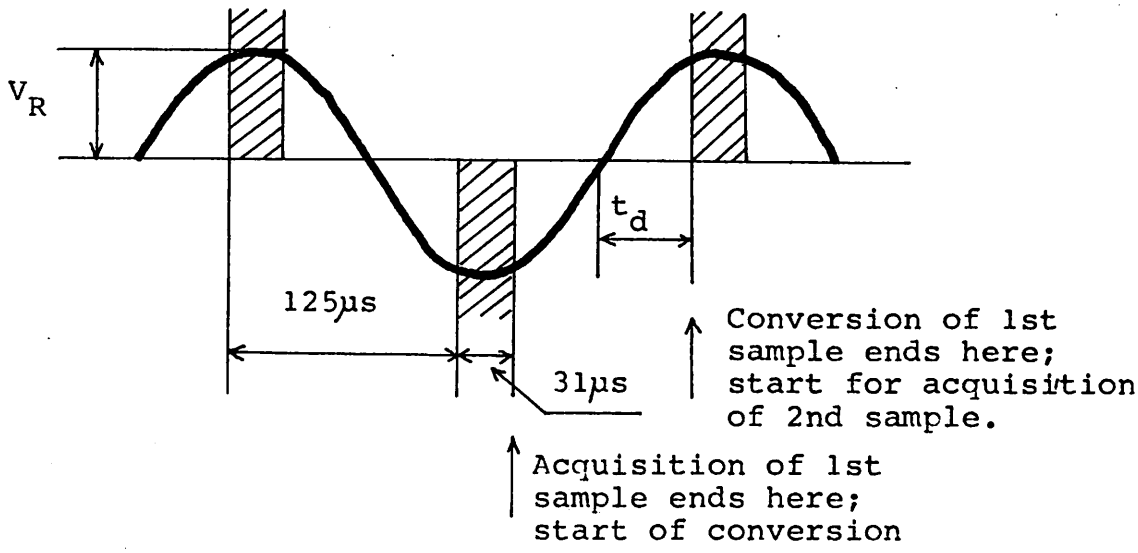
3.3.3 Sample acquisition.

As has been mentioned earlier, the time spent in sampling is of about 3 time slots, the conversion being divided into 12 equal time slots. This yields about 31 $\mu$s at a sampling rate of 8 kHz and 15 $\mu$s at 16 kHz. The capacitance of the "sampling" capacitor is of about 217 pF. The maximum frequency of the analog input signals is 4 kHz for voice and the maximum amplitude $V_R$. These numbers have to be used to design the circuit elements involved in the sampling process.

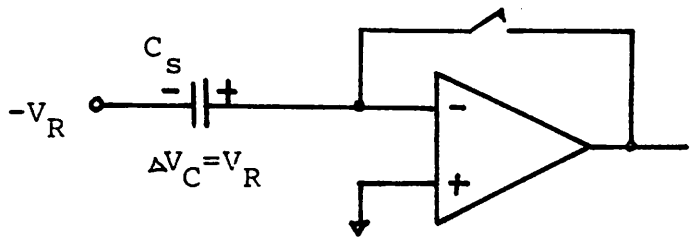
The worst case for sampling is illustrated in Figure 3.33 and corresponds to the sampling of the maximum amplitude 4 kHz sinewave. At the end of the first conversion the potential at the comparator input is close to 0 and the capacitors of the segment array are all charged up to $V_R$ with the polarity shown in Figure 3.33b. At the beginning of the second sampling operation the switches are thrown as shown in Figure3.33c. If the switch connecting the analog input to the bottom plate of $C_S$ is closed first, then the potential at the comparator input can momentarily go to $2V_R$ and if $2V_R > VS$ then such an event is undesirable. A safer procedure is to discharge $C_S$ first and then connect the analog input. If $2V_R < VS$, then such precautions are unnecessary.

A first order analysis of the sampling process can be made if one assumes that the comparator has infinite bandwidth and is described by the dc transconductance shown in Figure 3.34a. The equivalent circuits used to describe the behavior of the configuration during sampling are shown in Figure 3.34.

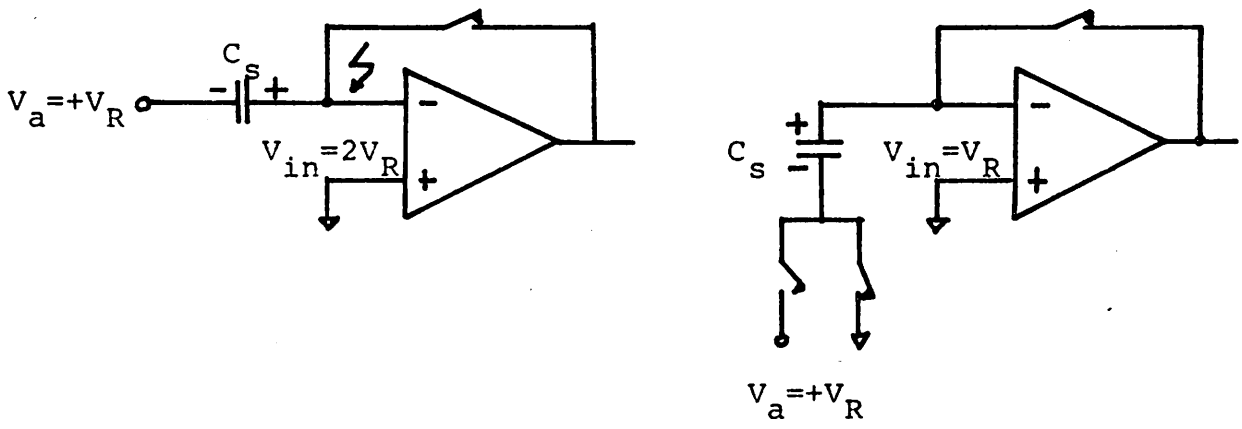
The discharging of the sampling capacitor $C_S$ and the




(a) Sampling of a 4kHz full scale sinewave

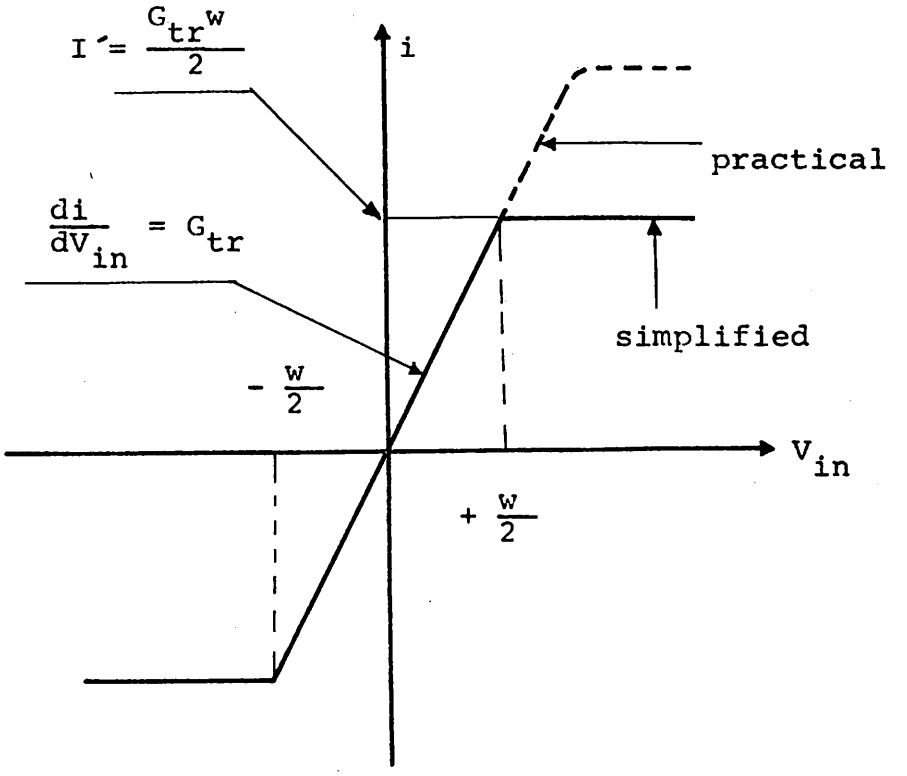



(b) Sampling capacitor at end of 1st conversion

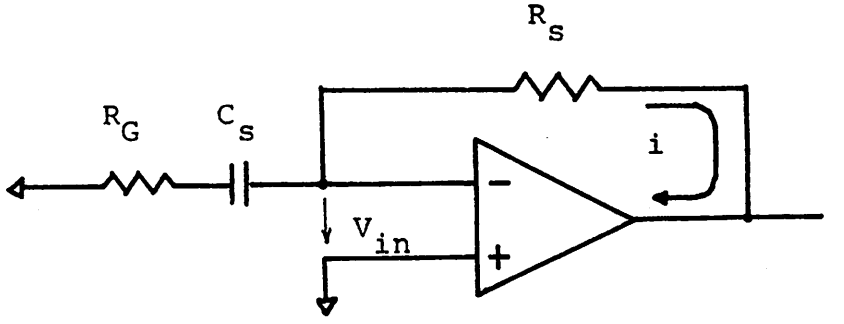



(c) Sampling capacitor at beginning of 2nd sample acquisition without (left) and with (right) initial discharging.

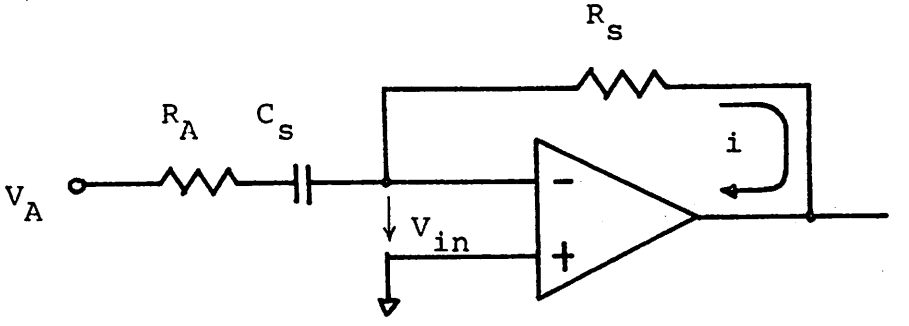
Figure 3.33




(a) Comparator dc transconductance




(b) Discharging the sampling capacitor




(c) Acquisition of the analog sample

Figure 3.34

acquisition of the new analog sample will be treated as separate steps in order to keep the analysis clean. The total time spent for discharging and sample acquisition will be the longer of the two as long as superposition holds.

At the beginning of the second sampling the capacitor is charged up to $V_R$ as shown in the right half of Figure 3.33c.

The discharging process will be described by the following equations:

If:
$$V_{in}(t=0) > \frac{w}{2} \tag{3.31}$$

then:
$$0 = R_G I' - V_R + \frac{I't}{C_s} + V_{in} \tag{3.32}$$

If:
$$V_{in}(t=0) < \frac{w}{2} \tag{3.33}$$

then:
$$0 = R_G i - V_R + \frac{1}{C_s}\int i\,dt + V_{in} \tag{3.34}$$

where:
$$i = G_{tr} V_{in} \tag{3.35}$$

From (3.32) we find:

$$V_{in}(t=0) = V_R - R_G I'$$

Therefore the condition of saturated operation can be written as:

$$R_G I' + \frac{w}{2} < V_R \tag{3.31'}$$

The opposite condition obviously implies linear operation:

$$R_G I' + \frac{w}{2} > V_R \tag{3.33'}$$

From (3.32) we can also find the time spent in saturation:

$$t_1 = \frac{\left[V_R - \frac{w}{2}\right] C_s}{I'} - R_G C_s \tag{3.36}$$

During the linear period, when (3.35) holds, the discharging process will be described by:

$$V_{in} = \frac{w}{2} e^{-t/\tau_G} \qquad (3.37)$$

or:

$$V_{in} = \frac{V_R}{1+G_{tr}R_G} e^{-t/\tau_G} \qquad (3.38)$$

where:

$$\tau_G = \frac{1+G_{tr}R_G\ C_s}{G_{tr}} \cong R_G C_s \qquad (3.39)$$

Equation (3.37) is valid with (3.31′) and (3.38) with (3.33′). The voltage across the sampling capacitor is described by:

$$V_{C_s} = -(1+G_{tr}R_G)V_{in}(t_1)e^{-t/\tau_G} \qquad (3.40)$$

where $V_{in}(t_1)$ is the input voltage at the end of saturated operation, i.e. $V_{in}(0)$ as given by (3.37) or respectively (3.38). From (3.40) we can find the time required to discharge the capacitor to the desired extent. An estimate of the discharging time can be obtained by arbitrarily imposing:

$$\left|V_{C_s}\right| < \frac{V_R}{255x16x2} = \frac{V_R}{8160}$$

(3.40) coupled with (3.37) and respectively (3.38) yields:

$$t_2 \cong \left[\ln 8160 - \ln \frac{V_R}{R_G I' + \frac{w}{2}}\right]\tau_G \qquad (3.41)$$

or:

$$t_2 \cong \tau_G \ln 8160 = 9\tau_G \qquad (3.42)$$

The total time spent for discharging will then be the sum of $t_1$ and $t_2$ or respectively only $t_2$. If the sampling time is sensibly larger than $t_1$ or $t_2$ then the capacitor

will in fact be discharged to a greater extent than just one half of a first segment step.

The acquisition of the analog sample is described by similar equations, i.e.:

$$V_A(t) = R_A I' + \frac{I't}{C_s} + V_{in}(t) \qquad (3.43)$$

if:

$$V_A(0) > \frac{w}{2} + R_A I' \qquad (3.44)$$

and:

$$V_A(t) = R_A i + \frac{1}{C_s}\int i\,dt + V_{in}(t) \qquad (3.45)$$

with i given by (3.35) and if (3.44) is not true.

During the sampling of the input signal the switch resistance associated with the analog input terminal could possibly be different from the one used for discharging; therefore $R_A$ takes the place of $R_G$ and $\tau_G$ is replaced by $\tau_A$ with the latter of the same form with (3.39).

The analog input will be represented by a sinewave:

$$V_A(t) = U\sin\omega(t+t_d)$$

where $\omega = 2\pi(4\text{kHz})$ and $t_d$ is the delay between the 0 crossing of the sinewave and the moment when acquisition starts. The sampling capacitor is being assumed as completely discharged.

The time spent in saturation is found from (3.43):

$$t_1 = \frac{\left[V_A(t_1) - \frac{w}{2}\right]C_s}{I'} - R_A C_s \qquad (3.36')$$

Under linear conditions the expressions for the input voltage and the acquisition error, $\varepsilon$ , are found on the basis of (3.45) and (3.35). Namely:

$$V_{in}(t+t_1) = \frac{(\omega\tau_A)^2 V_A(t+t_1) + \tau_A \frac{dV_A(t+t_1)}{dt}}{\left[1+G_{tr}R_A\right]\left[1+(\omega\tau_A)^2\right]} + \frac{\left[V_A(t_1) - \tau_A \frac{dV_A(t_1)}{dt}\right] e^{-t/\tau_A}}{\left[1+G_{tr}R_A\right]\left[1+(\omega\tau_A)^2\right]} - \frac{V_{C_s}(t_1)e^{-t/\tau_A}}{1+G_{tr}R_A} \tag{3.46}$$

and:

$$\varepsilon = V_A(t+t_1) - V_{C_s}(t+t_1) = (1+G_{tr}R_A)V_{in}(t+t_1) \tag{3.47}$$

where $t_1$ is the time spent in saturation.

It turns out that the ratio between the time length of the sampling interval and $\tau_A$ can be designed large enough as to minimize the exponential terms to an acceptable level. The same is not true for the periodic terms since $(\omega\tau_A)$ can not be made arbitrarily small. After the exponential terms have vanished and taking into account that $(\omega\tau_A)$ is nevertheless a small number, the input voltage can be written as:

$$V_{in}(t+t_1) \cong \frac{(\omega\tau_A)^2 V_A(t+t_1) + \tau_A \frac{dV_A(t+t_1)}{dt}}{1+G_{tr}R_A} \tag{3.48}$$

The acquisition error then will be:

$$\varepsilon \cong (\omega\tau_A)^2 V_A(t+t_1) + \tau_A \frac{dV_A(t+t_1)}{dt} \tag{3.49}$$

The maximum error occurs when the input signal goes through 0 at the end of the sampling interval and is given by:

$$\varepsilon_{max} = (\omega\tau_A)U \qquad (3.50)$$

In the case $U = V_R$ this error can be quite large, possibly larger than for instance one half of a first segment step. On the other hand one can see that the error is large when the maximum amplitude of the sinewave is large too. But the samples acquired with such large error occur with the lowest probability and therefore one would expect that the effect of such errors on SNR and GTRCK will not be too harmful. The situation could also be interpreted as the result of a variable offset voltage and this then could be analyzed in principle with a program like XCODEC. At this point it seems sufficient to mention the problem and to keep it in mind in the event of questionable experimental results.

An other interesting conclusion of the sampling analysis is the fact that the sampling switch resistance has no effect on the time constants. In order for this to be true the switch has to be able to carry the maximum current of the comparator, $I'$, otherwise the switch rather than the comparator would determine the maximum charging current. In the next section it will be shown that the switch resistance is nevertheless important from a stability point of view.

3.3.4 Comparator stability.

The equivalent small signal circuit of the sampling configuration is shown in Figure 3.35a, where:

- r is the equivalent resistance of the sampling switch at equilibrium, i.e. with $V_{DS}=0$.

- $Cs_A$ and $Cs_B$ are gate plus junction capacitances associated with the sampling switch.

- $C_s$ is the total capacitance of the segment array.

- $R_A$ is the equivalent resistance of the analog switches connecting $C_s$ to the input voltage source plus the output resistance of that source.

- $C_p$ and $R_p$ are the parasitic elements associated with $C_s$. The capacitors are built with the $n^+$ bottom plate imbedded into a $p^-$ well; $C_p$ is the capacitance of the $n^+p^-$ junction and $R_p$ is the equivalent resistance from the bottom plates to the negative supply, to which the $p^-$ well is tied.

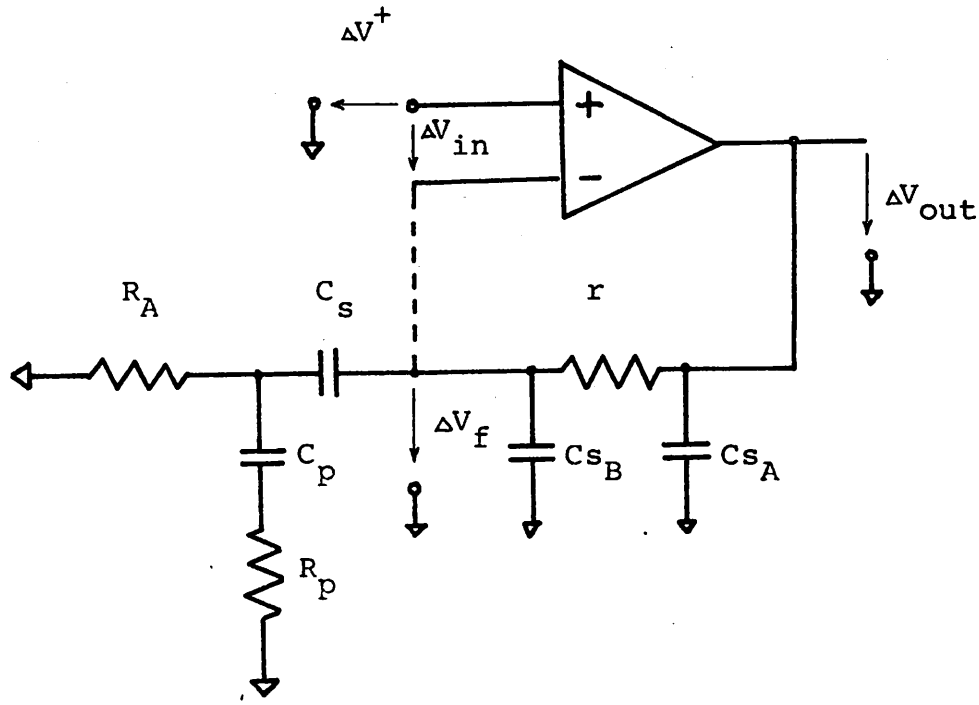
This configuration will now be analyzed from a stability point of view.

The closed loop voltage gain of the circuit shown in Figure 3.35a can be expressed as:

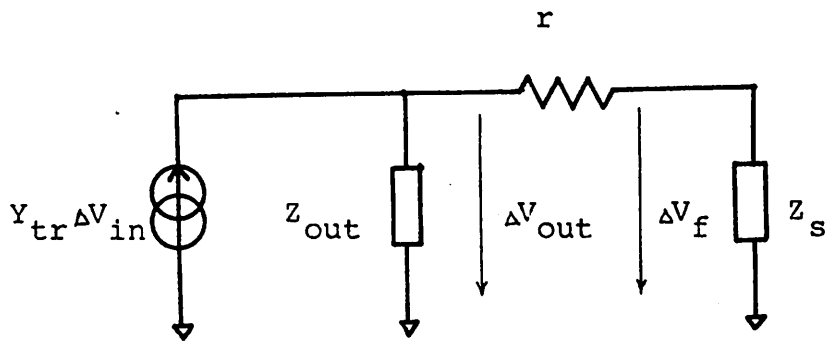
$$\frac{\Delta V_{out}}{\Delta V^+} = \frac{A}{1+fA} \tag{3.51}$$

where:

$A = \dfrac{\Delta V_{out}}{\Delta V_{in}}$ is the open loop voltage gain of the comparator in the presence of the feedback network (with




(a) Block diagram for stability analysis




(b) Equivalent circuit used for stability analysis

Figure 3.35

the loop, dashed line, broken) and $f = \frac{\Delta v_f}{\Delta v_{out}}$ is the feedback factor. By replacing the comparator with an equivalent current generator, as shown in Figure 3.35b, the open loop voltage gain can be expressed as:

$$A = \frac{Y_{tr} Z_{out} (r+Z_s)}{Z_{out}+r+Z_s} \tag{3.52}$$

where $Z_s$ is composed of $Cs_B$, $C_s$, $C_p$, $R_p$ and $R_A$, and $Z_{out}$ includes $Cs_A$. The feedback factor can obviously be expressed as:

$$f = \frac{Z_s}{Z_s+r} \tag{3.53}$$

From (3.52) and (3.53) we find the loop gain:

$$T = fA = \frac{Y_{tr} Z_{out} Z_s}{Z_{out}+r+Z_s} \tag{3.54}$$

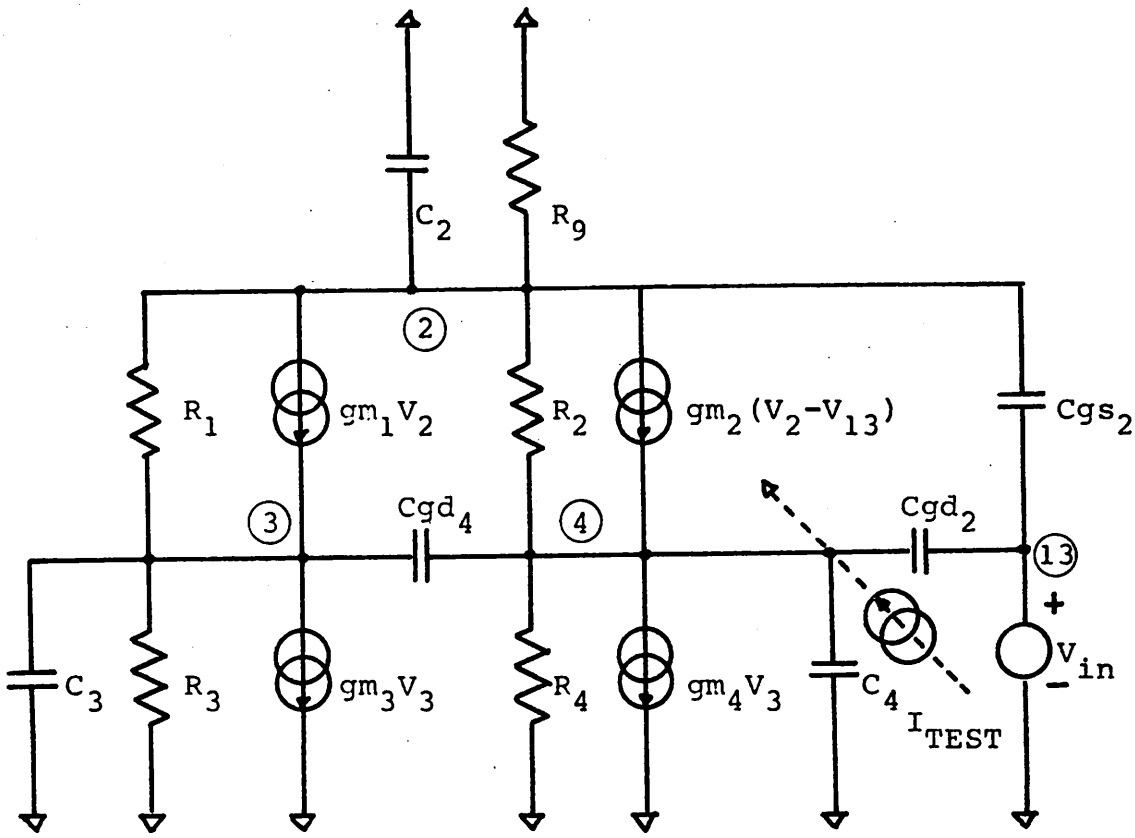
The well known stability conditions are:

$$|T| < 1 \quad \text{at} \quad \varphi(T) = 180^\circ$$

and:

$$\varphi(T) < 180^\circ \text{ at } |T| = 1$$

The transconductance, $Y_{tr}$, and output impedance, $Z_{out}$, will next be derived on a step by step basis, i.e. in order to make the complete comparator analysis more tractable we will first replace the input stage with an equivalent current generator. The equivalent small signal circuit of the input stage alone is shown in Figure 3.36. It should be mentioned that the separate analysis of the input stage is possible only if one can neglect the stage interaction via the biasing network.




$R_9=1/gds_9$; $R_1=1/gds_1$; $R_3=1/gds_3$; $R_4=1/gds_4$; $R_2=1/gds_2$

$C_2=Cjd_9+Cjs_1+Cjs_2+Cgs_1+(Cgd_9)$

$C_3=Cjd_1+Cgd_1+Cjd_3+Cgs_3+Cgs_4$

$C_4=Cjd_2+Cjd_4+Cgs_5$

<u>Equivalent small signal circuit of the comparator input stage.</u>

Figure 3.36

The short circuit current of the input stage is found by grounding node 4. The equations are:

$$I_{SHORT} = -sCgd_2V_{in}-gm_2(V_2-V_{in})-G_2V_2-sCgd_4V_3+gm_4V_3 \quad (3.55)$$

$$sCgs_2(V_2-V_{in})+gm_2(V_2-V_{in})+G_2V_2+(G_9+sC_2)V_2+gm_1V_2+ G_1(V_2-V_3) = 0 \quad (3.56)$$

$$gm_1V_2+G_1(V_2-V_3)=(gm_3+G_3+sC_3)V_3 + sCgd_4V_3 \quad (3.57)$$

Considering the "stacking" of the input stage devices it appears that the driver and load will be biased at approximately equal $V_{GS}$'s; therefore at equal nominal threshold voltages and obviously equal current the driver and load will exhibit similar gm's. Based on this observation one can make the following simplifications:

$$gm_1 = gm_2 = gm_3 = gm_4 = gm_{in}$$

Based on this observation and neglecting G's whenever they are added to gm's we find that equation (3.57) can be rewritten as:

$$V_3 = \frac{V_2}{1 + \frac{sC_{3t}}{gm_{in}}} \quad (3.57')$$

But $gm_{in}/C_{3t}$, where $C_{3t} = C_3+Cgd_4$, is a frequency of the same order of magnitude with the $\omega_T$ of the transistors.

Therefore $V_3$ can be considered equal to $V_2$ over a wide frequency range. If this is so then equation (3.56) can be rewritten as:

$$V_2 = \frac{V_{in}}{2} \quad \frac{1 + sCgs_2/gm_{in}}{1 + sC_{2t}/2gm_{in}} \quad (3.56')$$

where $C_{2t} = C_2+Cgs_2$ is the total capacitance at node 2.

The frequencies $gm_{in}/Cgs_2$ and $2gm_{in}/C_{2t}$ are again of the same order of magnitude with $\omega_T$. Therefore, if it was reasonable to consider $V_2 = V_3$, it will also be reasonable to consider over the same frequency range $V_2 = V_{in}/2$. Under such circumstances equation (3.55) can be rewritten as:

$$I_{SHORT} = gm_{in}V_{in}\left( 1 - s \frac{Cgd_2+Cgd_4/2}{gm_{in}}\right) \qquad (3.55')$$

The breakfrequency entering this last expression is even higher than the previous ones; therefore the short circuit current of the input stage can be expressed over a wide frequency range as:

$$I_{SHORT} = gm_{in}V_{in} \qquad (3.55'')$$

This expression will be valid for stability evaluation as long as the unity gain crossover frequency of the loop gain will be sufficiently smaller than the breakfrequencies mentioned during the previous analysis.

The output impedance is found by grounding the input, node 13, and applying a test generator at node 4. The equations are:

$$I_{TEST}=sCgd_2V_4-gm_2V_2+G_2(V_4-V_2)+sCgd_4(V_4-V_3)+gm_4V_3+(G_4+sC_4)V_4 \qquad (3.58)$$

$$gm_2V_2+sCgs_2V_2+G_2(V_2-V_4)+(G_9+sC_2)V_2+gm_1V_2+G_1(V_2-V_3)=0 \qquad (3.59)$$

$$G_1(V_2-V_3)+gm_1V_2=(gm_3+G_3+sC_3)V_3+sCgd_4(V_3-V_4) \qquad (3.60)$$

These equations can be rewritten in a more meaningful form as follows:

$$\frac{I_{TEST}}{V_4} = G_2+G_4+sC_{4t}+(gm_4-sCgd_4)\frac{V_3}{V_4} - (gm_2+G_2)\frac{V_2}{V_4} \qquad (3.58')$$

$$(gm_{2t}+sC_{2t})\frac{V_2}{V_4} - G_1\frac{V_3}{V_4} = G_2 \qquad (3.59')$$

$$(gm_1+G_1)\frac{V_2}{V_4} - (gm_{3t}+sC_{3t})\frac{V_3}{V_4} = -sCgd_4 \qquad (3.60')$$

where $gm_{2t}$, $gm_{3t}$ and $C_{2t}$, $C_{3t}$, $C_{4t}$ are the total conductances and capacitances "hanging" at the respective nodes. The possible simplifications are:

$gm_1=gm_2=gm_3=gm_4=gm_{in}$ and $G_1=G_2=1/R_1$

Using these simplifications and combining (3.58') with (3.60') we find:

$$\frac{I_{TEST}}{V_4} = \frac{1}{Z_{out_1}} = G_2+G_4+sC_{4t}+sCgd_4 - (G_1+G_3+sC_{3t}+sCgd_4)\frac{V_3}{V_4} \qquad (3.58'')$$

Solving (3.59') and (3.60') for $V_3/V_4$ we find:

$$\frac{V_3}{V_4} = \frac{G_1(gm_{in}+G_1)+gm_{2t}sCgd_4+s^2C_{2t}Cgd_4}{(gm_{2t}+sC_{2t})(gm_{3t}+sC_{3t})} \qquad (3.61)$$

By "forcing" the roots of the numerator, (3.61) can be rewritten as:

$$\frac{V_3}{V_4} = \frac{1}{gm_{3t}R_1}\;\frac{1+gm_{in}R_1}{gm_{2t}R_1}\;\frac{1+s\dfrac{gm_{2t}R_1}{1+gm_{in}R_1}R_1Cgd_4}{1+s\dfrac{C_{3t}}{gm_{3t}}} \qquad (3.61')$$

At frequencies below $1/2R_1Cgd_4$, (3.61') can be approximated as simply $1/2gm_{3t}R_1$ which is much smaller than 1. At higher

frequencies the ratio $V_3/V_4$ can be expressed as:

$$\frac{V_3}{V_4} = \frac{sCgd_4}{gm_{3t}} \quad \frac{1}{1 + sC_{3t}/gm_{3t}}$$

This last expression is again much less than 1 over a wide frequency range. Beyond $gm_{3t}/C_{3t}$ the ratio saturates to $Cgd_4/C_{3t}$ which is itself less than 1. Therefore one can safely assume that up to frequencies of the same order of magnitude with $\omega_T$ the output impedance of the input stage can be expressed as:

$$\frac{1}{Z_{out_1}} = G_2+G_4+sC_{4t}+sCgd_4 = \frac{1}{R_{o1}} + sC_{o1} \qquad (3.62)$$

The equivalent small signal circuit used for the derivation of $Y_{tr}$ and $Z_{out}$ is shown in Figure 3.37.

The short circuit current is found by grounding the output, node 6. The equations are:

$$I_{SHORT} = gm_6V_5 + (G_6+sC_{65})V_5 \qquad (3.63)$$

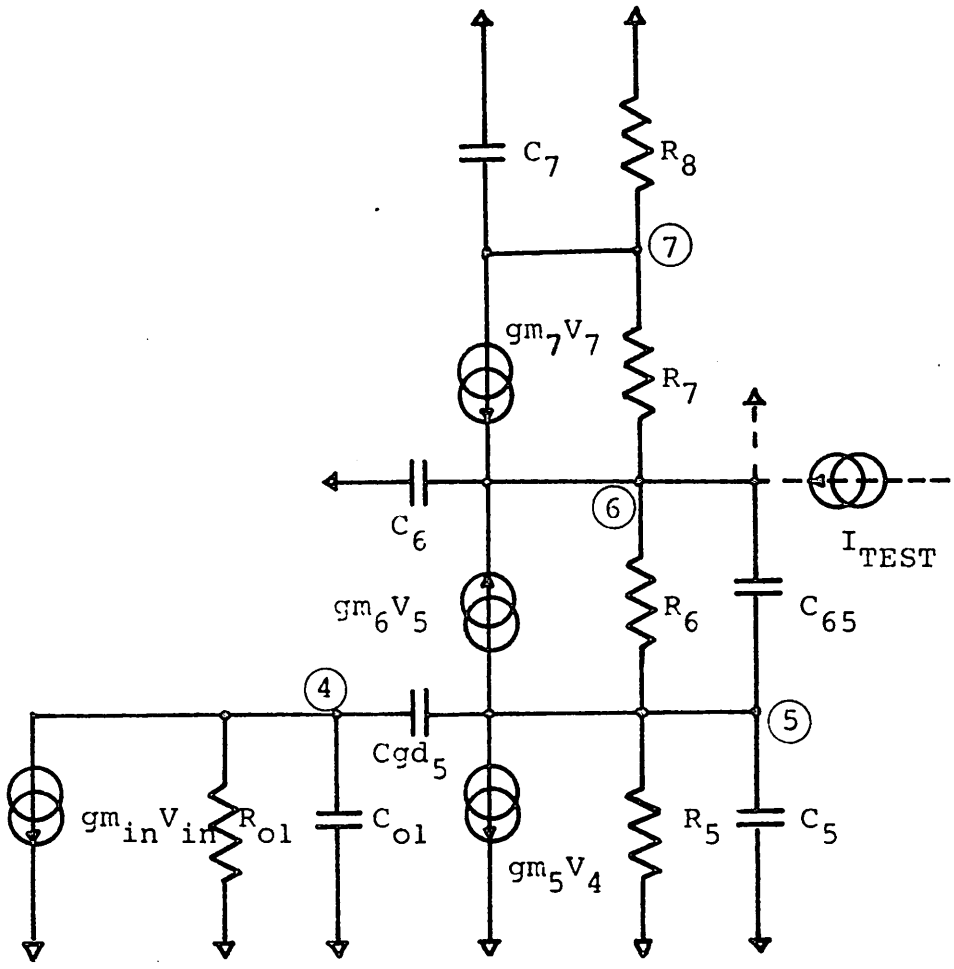
$$gm_{in}V_{in} + (G_{o1}+sC_{o1})V_4 + sCgd_5(V_4-V_5) = 0 \qquad (3.64)$$

$$sCgd_5(V_4-V_5) = gm_5V_4 + (G_5+sC_5)V_5 + I_{SHORT} \qquad (3.65)$$

From (3.63) we find:

$$I_{SHORT} = gm_6V_5(1 + s\frac{C_{65}}{gm_6+G_6}) \qquad (3.63')$$

But $(gm_6+G_6)/C_{65}$ is a frequency of the same order of magnitude with $\omega_T$; therefore, up to such frequencies, the short circuit current can be expressed as:




$R_8=1/gds_8$; $R_7=1/gds_7$; $R_6=1/gds_6$; $R_5=1/gds_5$

$C_7=Cjd_8+Cjs_7+Cgs_7+(Cgd_8)$

$C_6=Cjd_7+Cgd_7+Cjd_6+Cgd_6+Cs_A+Cgd_{10}$

$C_5=Cjd_5+Cgs_6+Cjp_5^-$

$C_{65}=Cjd_6$

<u>Simplified equivalent small signal circuit of CMOS comparator.</u>

Figure 3.37

$$I_{SHORT} = gm_6 V_5 \qquad (3.63'')$$

Using (3.63'') in (3.65) we find:

$$V_5 = -\frac{gm_5}{gm_6+G_5} V_4 \frac{1-s\dfrac{Cgd_5}{gm_5}}{1+s\dfrac{C_5+Cgd_5}{gm_6+G_5}} \qquad (3.65')$$

The breakfrequencies entering (3.65') are again close to $\omega_T$ so that $V_5$ can be approximated as:

$$V_5 = -\frac{gm_5}{gm_6} V_4 \qquad (3.65'')$$

Using (3.65'') in (3.64) we find:

$$V_4 = -\frac{gm_{in}R_{ol}V_{in}}{1+s\dfrac{C_{4t}+(gm_5/gm_6)Cgd_5}{G_{ol}}} \qquad (3.64')$$

where: $C_{4t} = C_{ol}+Cgd_5$

It follows that up to frequencies close to $\omega_T$ the comparator transconductance can be expressed as:

$$Y_{tr} = \frac{I_{SHORT}}{V_{in}} = \frac{gm_5 gm_{in} R_{ol}}{1 + sC'_{4t}R_{ol}} \qquad (3.66)$$

where:

$$C'_{4t} = C_{4t} + (gm_5/gm_6)Cgd_5 \qquad (3.67)$$

The effect of the cascode connection is clearly visible in (3.67) where $Cgd_5$ enters once with its full value and the second time multiplied by a factor close to 1, i.e. the major breakfrequency of $Y_{tr}$ is not influenced by excessive Miller effect.

The output impedance, $Z_{out}$, is found by grounding the input, i.e. $V_{in}$ of Figure 3.37 is zero, and by applying a test generator at node 6. The analysis can be simplified by separately considering the "upward" and "downward" path in the output stage.

Looking upwards through M7C and M8C we find:

$$I^u_{TEST} = -gm_7V_7 + G_7(V_6-V_7) \tag{3.68}$$

$$gm_7V_7 + G_7(V_7-V_6) + (G_8+sC_7)V_7 = 0 \tag{3.69}$$

Equation (3.69) can be rewritten as:

$$V_7 = \frac{G_7}{gm_7+G_7+G_8} V_6 \frac{1}{1+s\dfrac{C_7}{gm_7+G_7+G_8}} \tag{3.69'}$$

The breakfrequency $(gm_7+G_7+G_8)/C_7$ is of the same order of magnitude as $\omega_T$; therefore up to such high frequencies:

$$V_7 = \frac{G_7}{gm_7+G_7+G_8} V_6 \tag{3.69''}$$

Combining (3.68), (3.69) and (3.69'') we find:

$$Z^u_{out} = \frac{V_6}{I^u_{TEST}} = \frac{(gm_7R_8+1)R_7+R_8}{1+sC_7R_8} \tag{3.70}$$

Looking downwards through M6C and M5C we find:

$$I^d_{TEST} = -gm_6V_5 + (G_6+sC_{65})(V_6-V_5) \tag{3.71}$$

$$gm_6V_5 + (G_6+sC_{65})(V_5-V_6) + (G_5+sC_5)V_5 + gm_5V_4 + sCgd_5(V_5-V_4) = 0 \tag{3.72}$$

$$sCgd_5(V_4-V_5) + (G_{o1}+sC_{o1})V_4 = 0 \tag{3.73}$$

These equations can be rewritten in a more useful form as:

$$\frac{I^d_{TEST}}{V_6} = G_6+sC_{65} - (gm_6+G_6+sC_{65})\frac{V_5}{V_6} \qquad (3.71')$$

$$gm_5\left(1-s\frac{Cgd_5}{gm_5}\right)\frac{V_4}{V_6} + (gm_6+G_5+G_6)\left(1+s\frac{C_{5t}}{gm_6+G_5+G_6}\right)\frac{V_5}{V_6} \doteq (G_6+sC_{65}) \qquad (3.72')$$

$$\frac{V_4}{V_6} = \frac{V_5}{V_6}\,\frac{sCgd_5R_{o1}}{1+sC_{4t}R_{o1}} \qquad (3.73')$$

where: $C_{5t} = C_5+Cgd_5+C_{65}$

The breakfrequencies $gm_5/Cgd_5$ and $(gm_6+G_5+G_6)/C_{5t}$ are of the same order of magnitude as $\omega_T$; therefore up to such high frequencies (3.72′) can be rewritten as:

$$gm_5\frac{V_4}{V_6} + (gm_6+G_5+G_6)\frac{V_5}{V_6} = G_6+sC_{65} \qquad (3.72'')$$

Combining (3.71′), (3.73′) and (3.72″) and neglecting an additional high breakfrequency, namely $(gm_6+G_6)/C_{65}$, we find:

$$Z^d_{out} = \frac{V_6}{I^d_{TEST}} = ((gm_6R_5+1)R_6+R_5)\,\frac{1+s/z_1}{(1+s/p_1)(1+s/p_2)} \qquad (3.74)$$

where:

$$1/z_1 = C'_{4t}R_{o1}\ ;\quad 1/p_1 = (gm_5R_5Cgd_5+C_{4t})R_{o1};\ 1/p_2 = C_{65}R_6$$

The total output impedance, $Z_{out}$, will be a parallel combination between $Z^u_{out}$, $Z^d_{out}$ and $C_6$.

Considering the relatively large dc values of $Z^u_{out}$ and $Z^d_{out}$, it follows that the output impedance will exhibit a major breakfrequency at:

$$\omega_{Z_{out}} = \frac{\dfrac{G_5G_6}{gm_6+G_5+G_6} + \dfrac{G_7G_8}{gm_7+G_7+G_8}}{C_6} = \frac{1}{R_oC_6} \qquad (3.75)$$

Beyond this breakfrequency $Z_{out}$ will be dominated by $C_6$ which is most likely larger than the "residual" capacitive values of the two "unilateral" $Z_{out}$'s.

At this point all the parameters entering the expression of the loop gain, T, are known analytically.

$Z_s$ of Figure 3.35b can be replaced with a parallel combination between $Cs_B$ and the series combination of $R_A$ and $C_s$; this is so because $R_A$ is normally smaller than $R_p$.

Thus:

$$Z_s = \frac{1+sC_sR_A}{sC_s(1+sCs_BR_A)} \qquad (3.76)$$

where the only additional simplification has been $C_s \gg Cs_B$.

The breakfrequency $1/Cs_BR_A$ is most likely of the same order of magnitude as $\omega_T$; therefore up to such high frequencies $Z_s$ can be approximated as:

$$Z_s = R_A + \frac{1}{sC_s} \qquad (3.76')$$

Based on ( 3.66), (3.75) and (3.76') the loop gain, T, can be expressed as:

$$T = \frac{gm_5gm_{in}R_{o1}R_o(1+sC_sR_A)}{(1+sC'_{4t}R_{o1})(1+sC_s(R_o+R_A+r)+sC_6R_o+s^2C_sR_oC_6(r+R_A))} \qquad (3.77)$$

After some minor "root forcing" in the denominator, T can be rewritten as:

$$T = \frac{gm_5 gm_{in} R_o R_{o1} (1+sC_s R_A)}{(1+sC_s R_o)(1+sC'_{4t} R_{o1})(1+sC_6(r+R_A))} \qquad (3.77')$$

The dominant pole, $1/C_s R_o$, occurs at a very low frequency since both $C_s$ and $R_o$ are very large compared to other circuit elements. Beyond this low frequency pole, the loop gain can be written as:

$$T = \frac{gm_5}{sC_s} \times \frac{gm_{in} R_{o1}}{1+sC'_{4t} R_{o1}} \times \frac{1+sC_s R_A}{1+sC_6(r+R_A)} \qquad (3.78)$$

The two remaining important singularities of this expression are the pole at $1/C'_{4t} R_{o1}$ and the zero at $1/C_s R_A$; the pole occuring at $1/C_6(r+R_A)$ is a highfrequency "second order" pole and can be neglected for the time being.

If the zero occurs before the unity gain crossoverfrequency then this frequency will be expressed by:

$$\omega_{BW} = gm_5 R_A \frac{gm_{in}}{C'_{4t}} \qquad (3.79)$$

But $gm_{in}/C'_{4t}$ is a relatively high frequency of the same order of magnitude as $\omega_T$; therefore $\omega_{BW}$ has to be much smaller than $gm_{in}/C'_{4t}$, otherwise the phase shift contributed by all the neglected $\omega_T$ type singularities could become unacceptable. It follows that:

$$gm_5 R_A < 1 \qquad (3.80)$$

is a necessary condition for stability. Placing of the zero before the unity gain crossoverfrequency implies:

$$\frac{1}{C_s R_A} < (gm_5 R_A) \frac{gm_{in}}{C'_{4t}} \tag{3.81}$$

which can also be expressed as:

$$R_A^2 > \frac{C'_{4t}}{C_s} \times \frac{1}{gm_5 gm_{in}} \tag{3.81'}$$

If conditions (3.80) and (3.81') are satisfied then one may expect that the phase shift at the unity gain crossover frequency, and obviously before that, will not exceed $180^o$.

At this point one may also attempt to evaluate the contribution of the singularities that have been neglected so far. If $\omega_{BW}$ is placed at about 10% $\omega_T$, then the phase shift contributed by any one of the $\omega_T$ type singularities will be of about $5^o$, at $\omega_{BW}$. It seems reasonable to consider that there will be as many high order phase contributors as there are low impedance nodes. Therefore the phase shift contributed by the 6 principal nodes could be of about $30^o$.

This then would be added to the phase shift generated by the main singularities, which in the case of the arrangement mentioned earlier, would be of $90^o$ at $\omega_{BW}$. The resulting phase margin of about $60^o$ would certainly be acceptable.

The pole placed at $1/C_6(r+R_A)$ will become bothersome only if the output capacitance $C_6$ is large compared to the gate and junction capacitances associated with the sampling switch,

### 3.3.5 Comparator speed.

The comparator has to be able to switch state within a finite time interval under minimum overdrive conditions. This general statement implies at least two things, i.e. the gain of the comparator has to be large enough to ensure a detectable output swing at minimum overdrive and the dynamic behavior of the comparator has to be such that the output swing will be realized within the alloted time. It has been mentioned earlier that 2 $\mu$s would be adequate.

The acceptable overdrive in the PCM converter case can be found using XCODEC. In the pseudoideal case where only the overdrive is finite, XCODEC yields an acceptable value equal to .016% of $V_R$, the reference voltage; this corresponds to about 64% of a step in the smallest segment of the transfer characteristic. The overdrive as used in XCODEC is defined as follows: the comparator (with zero offset voltage) will exhibit a given output state for an input greater than OVERDR and will switch state if the input changes to a value smaller than -OVERDR. The comparator will not switch state for input signals in the range bordered by OVERDR and -OVERDR but will retain the previous output state. Such a definition implies a constant overdrive assumption, i.e. the overdrive is independent of the comparator input transition magnitude; since the codec's performance is dependent mainly on the uniformity of the transfer curve steps it is to be expected that the acceptable overdrive is in fact "segment dependent", i.e. a larger overdrive can be tolerated in the case of a sample falling into the larger steps of the transfer curve. Since the overdrive problem appears to be most critical in the smaller segments, at least from a dc gain point of view, it seems reasonable to analyse the dynamic behavior of the comparator in the middle segment of the transfer curve.

For input signals that are smaller than $V_R/255$ the PCM codec acts like any other pair of linear converters since only the middle segment of the transfer characteristic is involved. In order for all the steps to exist the minimum detectable overdrive has to be less than 50% of the ideal step "length". In order for this to be possible the dc gain of the comparator has to be at least:

$$G_{min} = \frac{V_T}{V_R/(255x16x2)} = 8160 \frac{V_T}{V_R}$$

where $V_T$ is the trigger voltage of the inverter following the level shifter. The dynamic behavior under minimum overdrive conditions can be analysed using a step by step approach.

The first stage of the comparator will react linearly for voltages corresponding to the middle segment. This is a result of the relation between the rail to rail voltage differential of about 15 V and the value of the reference voltage, 3 V, which yields first segment voltages smaller than 12 mV. The typical dc gain of a differential input CMOS amplifier is also small enough to keep the output transistors, in this case M2C and M4C, saturated. As a result of these observations the first stage can be treated as a linear amplifier with the equivalent circuit shown in Figure 3.36. After some conventional algebraic manipulation using the Laplace transform we find:

$$\Delta V_4 = \Delta V_1 \frac{gm}{g_4} + A\Delta V_1 e^{-t/\tau_2} + B\Delta V_1 e^{-t/\tau_3} + C\Delta V_1 e^{-t/\tau_4} \qquad (3.117)$$

where:

$$A = \frac{gm}{gm - g_4(C_{3t}/C_{4t})} \left[ \frac{(C_{3t}+C_{34})(C_{3t}+C_{13})}{C_{3t}C_{4t}} + \frac{(C_{3t}+C_{34})(C_{3t}-C_{12})}{(C_{2t}-2C_{3t})C_{4t}} \right]$$

$$B = -\frac{gm}{2gm - g_4(C_{2t}/C_{4t})} \times \frac{(C_{3t}+C_{34})(C_{2t}-2C_{12})}{(C_{2t}-2C_{3t})C_{4t}}$$

$$C = \frac{gm(gm - g_4(C_{12}/C_{4t}))}{(2gm - g_4(C_{2t}/C_{4t}))(gm - g_4(C_{3t}/C_{4t}))} \times \frac{C_{3t}+C_{34}}{C_{4t}} -$$

$$\frac{(gm+g_4(C_{13}/C_{4t}))(gm+g_4(C_{34}/C_{4t}))}{g_4(gm - g_4(C_{3t}/C_{4t}))}$$

$\Delta V_1$ is the amplitude of the input transition.

$gm \cong gm_1 \cong gm_2 \cong gm_3 \cong gm_4$

$C_{12} = Cgs_1$; $C_{13} = Cgd_1$; $C_{34} = Cgd_4$;

$C_{2t} = Cgs_1+Cgs_2+Cjs_1+Cjs_2+Cjd_9+Cgd_9$;

$C_{3t} = Cgs_3+Cgs_4+Cgd_1+Cgd_4$;

$C_{4t} = Cjd_4+Cgd_4+Cjd_2+Cgd_2+Cgs_5+2Cgd_5$;

( $2Cgd_5$ is the result of the cascode driver's unity gain)

$g_4 = gds_2+gds_4$

$\tau_2 = C_{2t}/2gm$

$\tau_3 = C_{3t}/gm$

$\tau_4 = C_{4t}/g_4$

The only approximations made on the way leading to (3.117) were: $C_{3t}C_{4t} \gg C_{34}^2$ and $C_{4t} \gg C_{34}$. The assumption of equal gm's is designed and is the consequence of the fact that for optimum "stacking" of the first stage transistors the VGS's are comparable.

From (3.117) and the definition of the parameters it is apparent that the response of the first stage is practically given by:

$$\Delta V_4 = \Delta V_1 \frac{gm}{g_4} (1-e^{-t/\tau_4}) \qquad (3.118)$$

The response time in the critical case of minimum overdrive

can be defined as corresponding to:

$$\Delta V_4 = \frac{\Delta V_1 - \text{OVERDR}/10}{\Delta V_1} \Delta V_{4final} \tag{3.119}$$

correspondingly the first stage delay will be:

$$\Delta t_1 = \tau_4 \ln \frac{10\ \Delta V_1}{\text{OVERDR}} \tag{3.120}$$

As a result of this definition the effect of the overdrive will be practically exhausted in the time $\Delta t_1$, at least as far as the response of the first stage is concerned. The longest delay corresponds to the largest input transition which in the first segment is equal to $V_R/(255x2)$; at an overdrive equal to one half of a first segment step (3.120) yields a delay of:

$$\Delta t_1 = \tau_4 \ln \frac{10V_R/(255x2)}{V_R/(255x16x2)} = 5\,\tau_4$$

The largest possible input transition is equal to $64V_R/255$ and corresponds to the switching of capacitor CX64 to either the reference or to ground. In this case the input stage of the comparator is obviously no longer a linear amplifier; nevertheless it may be interesting to use (3.120) as an indicator even for this largest possible transition; the result is:

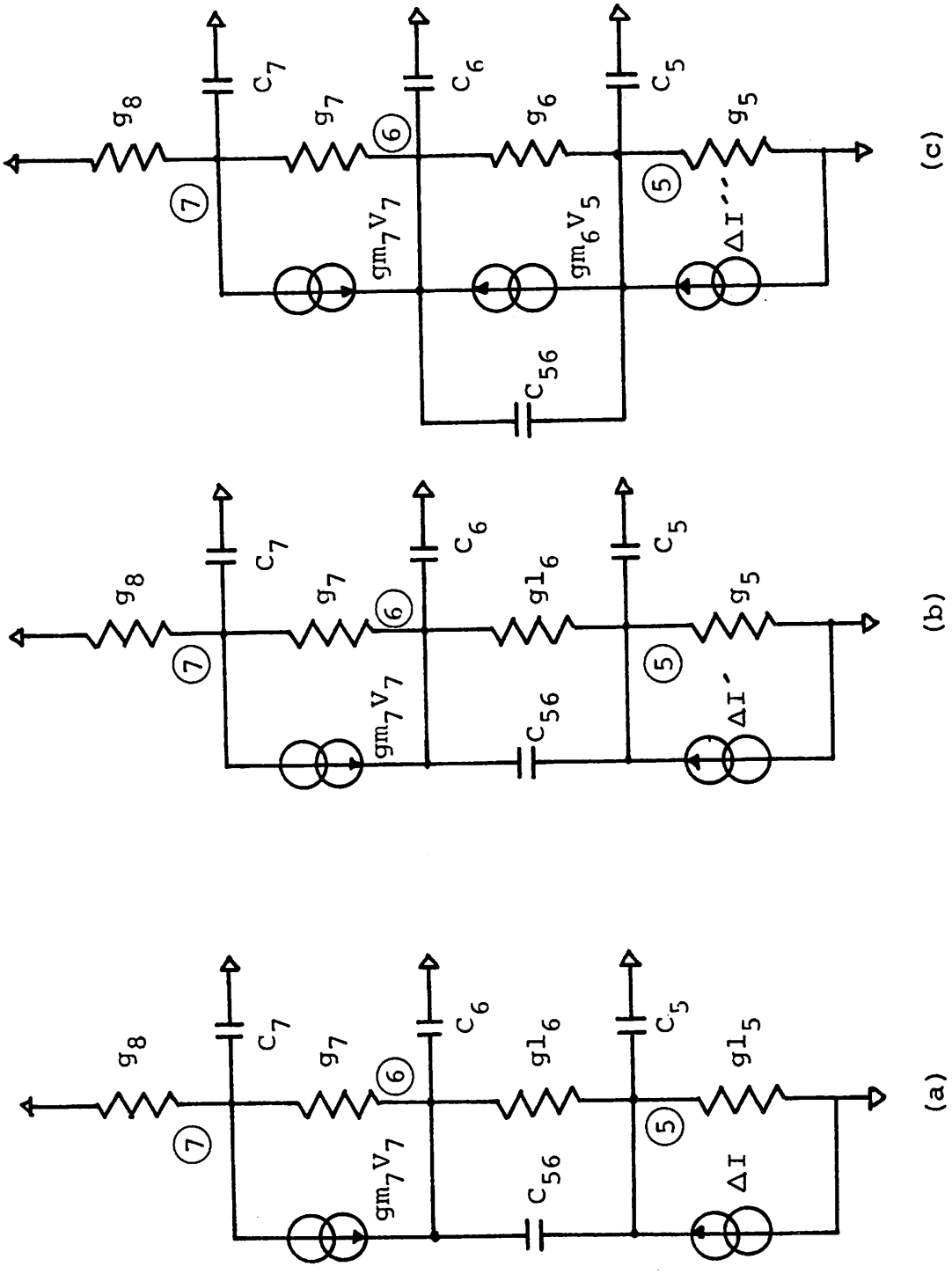
$$\Delta t_1 = \tau_4 \ln \frac{10x64V_R/255}{V_R/(255x16x2)} = 10\,\tau_4$$

This last result is a quite conservative estimate since the input stage will react faster than "linear".

In a worst case type of analysis the delay of the input stage can then be added to the delay of the cascode which in turn is excited with an input step equal to $\Delta V_1 (gm/g_4)$.

The switching of the cascode can be analysed using a piecewise linearized model for the transistors since some of them will start out of the linear region and end up saturated whereas other ones will undergo the opposite sequence. The two possible cases, along with the corresponding equivalent circuits, are illustrated in Figures 3.38 and 3.39. For input transitions corresponding to the steps of the middle segment the dc current flowing through the cascode does not undergo drastic changes; this is so because $\Delta V_4$ is in these cases reasonably small compared to the equilibrium value of $VGS_4$. Based on this observation one can easily relate the output resistance of a "linear" transistor to the equilibrium gm. By doing so the handanalysis becomes much more tractable.

The switching sequence in the case of a HIGH to LOW transition at the cascode input can be analysed on the basis of the equivalent circuits shown in Figure 3.38. Initially (Figure 3.38a) transistors M5C and M6C are linear and M7C and M8C are saturated. M5C will then exit the linear region (Figure 3.38b) and eventually M6C will follow suite (Figure 3.38c). The order of saturation, i.e. M5C first and then M6C, can be justified as follows: M6C will exit saturation when $V_6=-V_{th}$ (so that $VGS_6=VDS_6+V_{th}$). In order to keep M5C saturated at $V_6=0$ (for maximum gain) and at the same time use the ground connection for biasing the gate of M6C it turns out that M5C and M6C have to be of comparable sizes with $VGS_6 = VGS_5$. Therefore when M6C is at the border of saturation M5C is biased with $VGS_5=VDS_5=VS/2$, i.e. saturated. All the transistors will be saturated during zero crossing at node 6. This is the nominal switching point since the level shifter will translate the zero crossing at node 6 into a logic threshold crossing at the input of the following CMOS inverter.




Equivalent circuits used for the analysis of a LOW to HIGH transition at the comparator output.

Figure 3.38

The equations describing the circuit of Figure 3.40a are:

$$gl_5\mathcal{L}V_5 + sC_5\mathcal{L}V_5 + (gl_6+sC_{56})(\mathcal{L}V_5 - \mathcal{L}V_6) = \frac{\Delta I}{s}$$

$$(gl_6+sC_{56})(\mathcal{L}V_5-\mathcal{L}V_6) + gm_7\mathcal{L}V_7 = sC_6\mathcal{L}V_6 + g_7(\mathcal{L}V_6-\mathcal{L}V_7) \qquad (3.121)$$

$$gm_7\mathcal{L}V_7 + g_7(\mathcal{L}V_7-\mathcal{L}V_6) + (sC_7+g_8)\mathcal{L}V_7 = 0$$

The gl's are output conductances of linear transistors and the g's are output conductances of saturated transistors. Based on an earlier observation about the equivalence between gl's and gm's (3.121) can be rewritten as:

$$(gm_5+gm_6+sC_{5t})\mathcal{L}V_5 - (gm_6+sC_{56})\mathcal{L}V_6 = \frac{\Delta I}{s}$$

$$(gm_6+sC_{56})\mathcal{L}V_5 - (gm_6+g_7+sC_{6t})\mathcal{L}V_6 + (gm_7+g_7)\mathcal{L}V_7 = 0 \qquad (3.122)$$

$$-g_7\mathcal{L}V_6 + (gm_7+g_7+g_8+sC_7)\mathcal{L}V_7 = 0$$

From (3.122) we find $\mathcal{L}V_6$:

$$\mathcal{L}V_6 = \frac{\Delta I\ C_{56}C_7(s+gm_6/C_{56})(s+gm_7/C_7)}{s\ \alpha C_5C_6C_7(s^3+As^2+Bs+C)} \qquad (3.123)$$

where:

$$\alpha = 1 + \frac{C_{56}}{C_5} + \frac{C_{56}}{C_6}$$

$$A = \frac{gm_7}{C_7} + \frac{gm_6}{\alpha C_6} + \frac{gm_5(1+C_{56}/C_6)+gm_6}{\alpha C_5}$$

$$B = \frac{gm_7}{C_7} \times \frac{gm_5(1+C_{56}/C_6)+gm_6}{\alpha C_5} + \frac{gm_7}{C_7} \times \frac{gm_5}{\alpha C_6} + \frac{gm_5}{\alpha C_5} \times \frac{gm_6}{C_6}$$

$$C = \frac{gm_7}{C_7} \times \frac{gout}{C_6} \times \frac{gm_5+gm_6}{\alpha C_5}$$

$$gout = \frac{gm_5gm_6}{gm_5+gm_6} + \frac{g_7g_8}{g_7+g_8+gm_7} \cong \frac{gm_5gm_6}{gm_5+gm_6}$$

The coefficient C is the exact result following from (3.122) and coefficients A and B are found by neglecting output conductances of saturated transistors whenever they are added to gm's. It follows that $\mathcal{L}V_6$ can be expressed as:

$$\mathcal{L}V_6 = \frac{\Delta I\ C_{56}C_7(s+gm_n/C_{56})(s+gm_7/C_7)}{s\,\alpha C_5C_6C_7(s+gm_7/C_7)(s+2gm_n/\alpha C_5)(s+gm_n/2C_6)} \qquad (3.124)$$

where: $gm_n \cong gm_5 \cong gm_6$

In the time domain (3.124) is translated as:

$$v_6(t) = \frac{\Delta I}{gm_n}\left(1-pe^{-2gm_nt/\alpha C_5} - qe^{-gm_nt/2C_6}\right) \qquad (3.125)$$

where:

$$p = \frac{\alpha C_5 - 2C_{56}}{\alpha C_5 - 4C_6}\ ; \qquad q = \frac{4C_6 - 2C_{56}}{4C_6 - \alpha C_5}$$

This response will be valid as long as M5C is linear. The maximum rate of change is given by:

$$\left.\frac{dv_6(t)}{dt}\right|_{t=0} = \frac{\Delta I}{C_5+C_6+C_5C_6/C_{56}} \qquad (3.126)$$

After M5C enters saturation the operation of the cascode can be analized on the basis of the equivalent circuit shown in Figure 3.38b. The analysis will be started "from scratch" with $\Delta I'$ representing the remaining current deviation from the final equilibrium value. The equations are:

$$(g_5 - sC_5)\mathcal{L}V_5 + (gl_6 + sC_{56})(\mathcal{L}V_5 - \mathcal{L}V_6) = \frac{\Delta I'}{s}$$

$$(gl_6 - sC_{56})(\mathcal{L}V_5 - \mathcal{L}V_6) + gm_7\mathcal{L}V_7 + g_7(\mathcal{L}V_7 - \mathcal{L}V_6) = sC_6\mathcal{L}V_6 \qquad (3.127)$$

$$gm_7\mathcal{L}V_7 + g_7(\mathcal{L}V_7 - \mathcal{L}V_6) + (g_8 + sC_7)\mathcal{L}V_7 = 0$$

Solving for $\mathcal{L}V_6$ we find:

$$\mathcal{L}V_6 = \frac{\Delta I'\,(gm_6 + sC_{56})(gm_7 + g_7 + g_8 + sC_7)}{s\,\alpha C_5 C_6 C_7 (s^3 + As^2 + Bs + C)} \qquad (3.128)$$

where:

$$A = \frac{gm_7}{C_7} + \frac{gm_6}{\alpha C_5}\left(1 + \frac{C_5}{C_6}\right)$$

$$B = \frac{gm_7}{C_7} \times \frac{gm_6}{\alpha C_5}\left(1 + \frac{C_5}{C_6}\right)$$

$$C = \frac{gm_7}{C_7} \times \frac{gm_6}{\alpha C_5} \times \frac{gout}{C_6}$$

$$gout = \frac{gm_6 g_5}{gm_6 + g_5} + \frac{g_7 g_8}{gm_7 + g_7 + g_8} \cong g_5$$

$$\alpha = 1 + \frac{C_{56}}{C_5} + \frac{C_{56}}{C_6}$$

The roots of the denominator are found by inspection as in the previous case. In the time domain $v_6(t)$ will have fast and slow components. The final value corresponding to (3.128) is found again by inspection as being $\Delta I'/g_5$.

Therefore by neglecting the fast components we find:

$$v_6(t) \cong \frac{\Delta I'}{g_5}\left(1 - e^{-g_5 t/C_6}\right) \qquad (3.129)$$

and the maximum rate of change is given by:

$$\left.\frac{dv_6(t)}{dt}\right|_{t=0} = \frac{\Delta I'}{C_6} \tag{3.130}$$

When all the devices are saturated, Figure 3.38c, the cascode is described by:

$$\begin{aligned}
&(gm_6+g_5+sC_5)\mathcal{L}V_5 + (g_6+sC_{56})(\mathcal{L}V_5 - \mathcal{L}V_6) = \frac{\Delta I''}{s} \\
&gm_6\mathcal{L}V_5 + (g_6+sC_{56})(\mathcal{L}V_5 - \mathcal{L}V_6) + gm_7\mathcal{L}V_7 + \\
&\qquad g_7(\mathcal{L}V_7 - \mathcal{L}V_6) = sC_6\mathcal{L}V_6 \\
&g_7(\mathcal{L}V_7 - \mathcal{L}V_6) + (gm_7+g_8+sC_7)\mathcal{L}V_7 = 0
\end{aligned} \tag{3.131}$$

Here again the analysis is started from scratch with $\Delta I''$ being the remaining difference from the final dc value. Following a similar routine as earlier we find:

$$\mathcal{L}V_6 = \frac{\Delta I''\,(gm_6+g_6+sC_{56})(gm_7+g_7+g_8+sC_7)}{s\,\alpha C_5C_6C_7(s^3+As^2+Bs+C)} \tag{3.132}$$

where:

$$A = \frac{gm_7}{C_7} + \frac{gm_6}{\alpha C_5}$$

$$B = \frac{gm_7}{C_7} \times \frac{gm_6}{\alpha C_5}$$

$$C = \frac{gm_7}{C_7} \times \frac{gm_6}{\alpha C_5} \times \frac{gout}{C_6}$$

$$gout = \frac{g_7g_8}{gm_7+g_7+g_8} + \frac{g_5g_6}{gm_6+g_5+g_6}$$

The roots of the denominator are found again by inspection and the slow component of $v_6(t)$ coupled with the obvious final value yield:

$$v_6(t) = \frac{\Delta I''}{gout} \left( 1 - e^{-g_{out} t/C_6} \right) \tag{3.133}$$

The maximum rate of change is:

$$\left. \frac{dv_6(t)}{dt} \right|_{t=0} = \frac{\Delta I''}{C_6} \tag{3.134}$$

The response of the cascode in the case of a LOW to HIGH transition at node 4 can be derived in a manner very similar to the one used in the previous case. The equivalent circuits are shown in Figure 3.39, and the results are similar to to the ones obtained earlier.

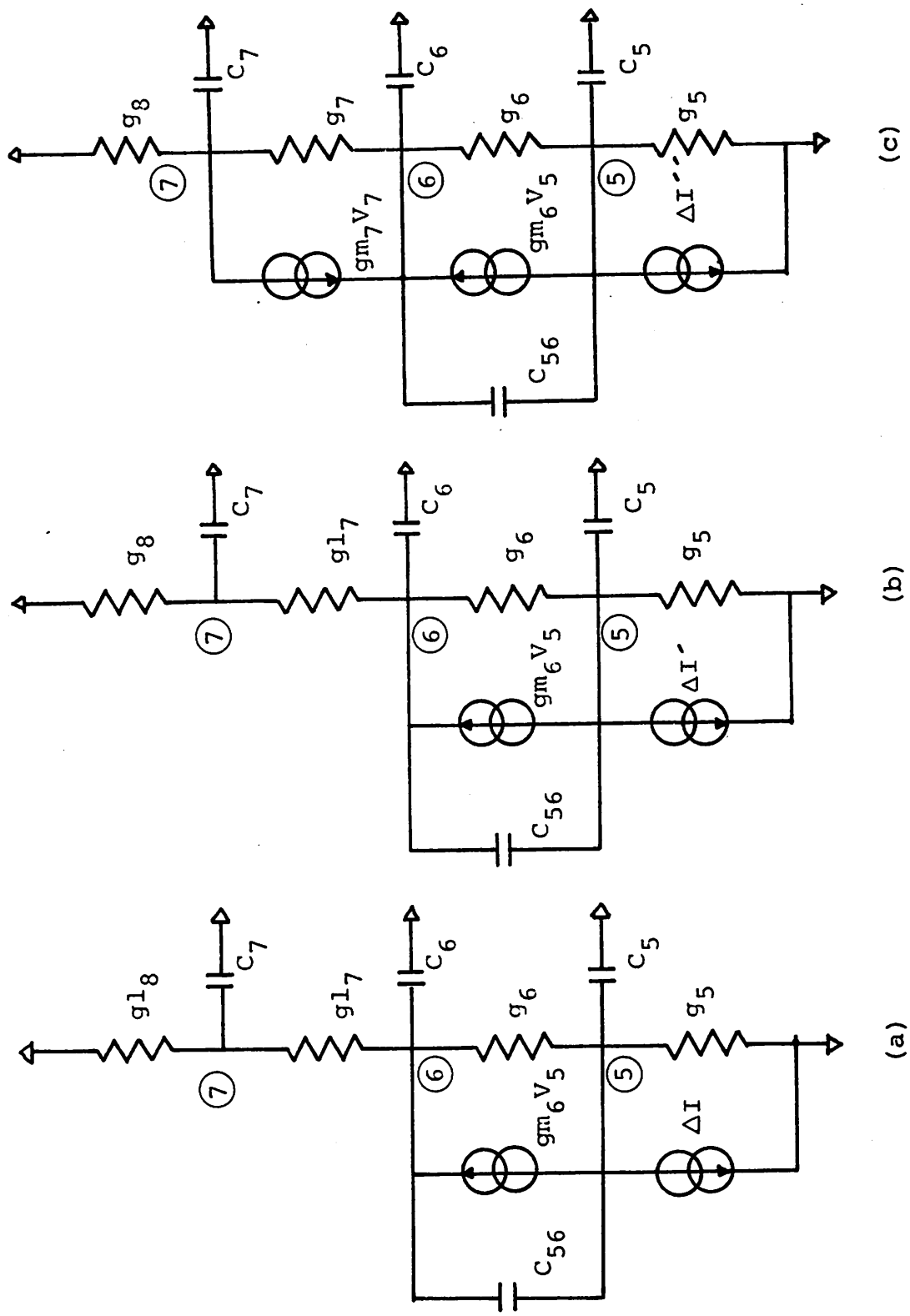
During the time when M8C is linear the output voltage is given by:

$$\mathcal{L}V_6 = - \frac{\Delta I \ (gm_6+sC_{56})(gm_7+gm_8+sC_7)}{s\,\alpha C_5 C_6 C_7 (s^3+As^2+Bs+C)} \tag{3.135}$$

where:

$$A = \frac{gm_7}{\beta C_6} + \frac{gm_7+gm_8}{C_7} + \frac{gm_6}{\alpha C_5}$$

$$B = \frac{gm_6}{\alpha C_5} \times \frac{gm_7+gm_8}{C_7} + \frac{gm_7}{\beta C_6} \times \frac{gm_8}{C_7} + \frac{gm_6}{\alpha C_5} \times \frac{gm_7}{C_6}$$




Equivalent circuits used for the analysis of a HIGH to LOW transition at the comparator output.

Figure 3.39

$$C = \frac{gm_6+g_5+g_6}{\alpha C_5} \times \frac{gm_7+gm_8}{C_7} \times \frac{gout}{C_6}$$

$$gout = \frac{g_5 g_6}{gm_6+g_5+g_6} + \frac{gm_7 gm_8}{gm_7+gm_8} \cong \frac{gm_p}{2}$$

$$gm_p \cong gm_7 \cong gm_8$$

$$\alpha = 1 + \frac{C_{56}}{C_5} + \frac{C_{56}}{C_6}$$

$$\beta = 1 + \frac{C_{56}C_5}{C_6(C_5+C_{56})} \cong 1$$

With some minor forcing, as has been the case before, $\mathcal{L}v_6$ can be rewritten as:

$$\mathcal{L}v_6 = - \frac{\Delta I \; C_{56}C_7(s+gm_6/C_{56})(s+2gm_p/C_7)}{s\,\alpha C_5 C_6 C_7 (s+2gm_p/C_7)(s+gm_6/\alpha C_5)(s+gm_p/2C_6)} \qquad (3.136)$$

With one additional simplification, i.e. $gm_6 \cong gm_p$, $\mathcal{L}v_6$ can be translated into the time domain as:

$$v_6(t) = - \frac{2\Delta I}{gm_p} \left( 1 - pe^{-gm_6 t/\alpha C_5} - qe^{-gm_p t/2C_6} \right) \qquad (3.137)$$

with:

$$p = \frac{\alpha C_5 - C_{56}}{\alpha C_5 - 2C_6} \; ; \qquad q = \frac{2C_6 - C_{56}}{2C_6 - \alpha C_5}$$

The maximum rate of change is:

$$\left.\frac{dv_6(t)}{dt}\right|_{t=0} = -\frac{\Delta I}{C_5+C_6+C_5C_6/C_{56}} \tag{3.138}$$

After M8C enters saturation:

$$\mathcal{L}v_6 = -\frac{\Delta I'\,(gm_6+g_6+sC_{56})\,(gm_7+g_8+sC_7)}{s\,\alpha C_5C_6C_7\,(s^3+As^2+Bs+C)} \tag{3.139}$$

where:

$$A = \frac{gm_6}{\alpha C_5} + gm_7\ (\ 1/C_7 + 1/\beta C_6\ )$$

$$B = \frac{gm_6}{\alpha C_5} \times gm_7\ (\ 1/C_7 + 1/C_6\ )$$

$$C = \frac{gm_6}{\alpha C_5} \times \frac{gm_7}{C_7} \times \frac{gout}{C_6}$$

$$gout = \frac{g_5g_6}{gm_6+g_5+g_6} + \frac{gm_7g_8}{gm_7+g_8} \cong g_8$$

$$\alpha = 1 + C_{56}/C_5 + C_{56}/C_6$$

$$\beta = 1 + \frac{C_{56}C_5}{C_6(C_5+C_{56})} \cong 1$$

Combining the slow component of $v_6(t)$ with its final value we find:

$$v_6(t) \cong -\frac{\Delta I'}{g_8}\left(1 - e^{-g_8 t/C_6}\right) \tag{3.140}$$

The maximum rate of change is:

$$\left.\frac{dv_6(t)}{dt}\right|_{t=0} = -\frac{\Delta I'}{C_6} \tag{3.141}$$

After all the devices enter saturation the behavior of the cascode can be described on the basis of Figure 3.39c.

Going through the same lengthy calculations and using similar arguments as in the case described by Figure 3,38c, we find:

$$v_6(t) \cong -\frac{\Delta I''}{gout}\left(1 - e^{-g_{out} t/C_6}\right) \tag{3.142}$$

with the same gout as in (3.134). Again the maximum rate of change is given by:

$$\left.\frac{dv_6(t)}{dt}\right|_{t=0} = -\frac{\Delta I''}{C_6} \tag{3.143}$$

At this point we can attempt to evaluate the delay of the cascode under minimum overdrive conditions. It has been shown that both the HIGH to LOW as well as the opposite transitions can be divided into three distinct phases; these phases might be called for convenience the linear phase, the semilinear phase and the saturated phase. The delay associated with the linear phase is of the same order of magnitude with the time constants involved; these time constants,

$\alpha C_5/2gm_n$, $2C_6/gm_n$, $\alpha C_5/gm_6$, $2C_6/gm_p$, are normally much smaller than the time constants associated with the first stage and can be safely neglected.

The delay associated with the semilinear phase can be evaluated by observing that the final "semilinear voltage" corresponds to a current equal to $\Delta I' - \Delta I''$.

Therefore the delay can be found on the basis of:

$$\frac{\Delta I' - \Delta I''}{g_5 \text{ or } g_8} = \frac{\Delta I'}{g_5 \text{ or } g_8} \left( 1 - e^{-(g_5 \text{ or } g_8)t/C_6} \right)$$

which yields:

$$\Delta t_{2semilin} = \frac{C_6}{g_5 \text{ or } g_8} \ln \frac{\Delta I'}{\Delta I''} \qquad (3.144)$$

The delay associated with the saturated phase can be estimated on the basis of the following observations.

The dc gain of the comparator has to exceed $8160(V_T/V_R)$.

Using a supply voltage of + 7.5V and a reference of 3V it turns out that the ratio $(V_T/V_R)$ is close to one; therefore the gain has to be larger than about 8160. But this requirement is easily exceeded with the cascode combination and therefore it is possible to assume that the output voltage will vary at constant rate during the saturated phase since the final value resulting from (3.133) or (3.142) is likely to be much larger than the output limits for this phase; these limits are $\pm V_{th}$. Therefore the "saturated delay " can be found by simply dividing the voltage excursion of $2V_{th}$ to the constant rate of change:

$$\Delta t_{2sat} \cong C_6 \frac{2V_{th}}{\Delta I''} \tag{3.145}$$

This last estimate is in fact conservative since the nominal switching point corresponds to the 0 crossing at node 6, i.e. a voltage swing of only $V_{th}$ in saturated operation. In a properly designed comparator the final value resulting from (3.133) or respectively (3.142) should be larger than $2V_{th}$, i.e.:

$$\Delta I'' > g_{out} 2V_{th} \tag{3.146}$$

Using this last condition and assuming that $\Delta I'$ represents practically the total current deviation, we can estimate (3.144) as:

$$\Delta t_{2semilin} < \frac{C_6}{g_5 \text{ or } g_8} \ln \frac{A_1 gm_{5eff} \Delta V_1}{g_{out} 2V_{th}} \tag{3.144'}$$

where $A_1$ is the dc gain of the input stage and $\Delta V_1$ is the total input voltage swing. This last expression can obviously be rewritten as:

$$\Delta t_{2semilin} < \frac{C_6}{g_5 \text{ or } g_8} \ln \frac{A_{tot} \Delta V_1}{2V_{th}} \tag{3.144''}$$

where $A_{tot}$ is the total gain of the comparator when it is largest, i.e. when all the devices in the cascode are saturated.

Obviously on the basis of (3.146) we can also estimate (3.145) as:

$$\Delta t_{2sat} < \frac{C_6}{g_{out}} \qquad (3.145')$$

The upper limit of the total delay will then be found by adding (3.120), (3.144'') and (3.145') and is:

$$\Delta t < \frac{C_{4t}}{g_4} \ln \frac{10\,\Delta V_1}{OVERDR} + \frac{C_6}{g_5 \text{ or } g_8} \ln \frac{A_{tot}\,\Delta V_1}{2V_{th}} + \frac{C_6}{g_{out}} \qquad (3.147)$$

where the $g_{out}$ used in the last equations is naturally the one corresponding to the saturated case, i.e. the smallest possible.

3.3.6 Device sizing.

After the analysis presented in the previous sections we should be able to decide on the actual size of the devices.

Some of the reasons underlying the choices to be made have been already presented. Thus it has been shown that from a gain point of view it is desirable to set the nominal threshold of the comparator equal to 0. This can be done by mirroring the currents in the two stages, i.e. (with reference to Figure 3.32) by attemting to realize: $V_7=V_2$ and $V_3=V_4=V_5$ so that $V_6=0$ at equilibrium. These voltage conditions can be translated into size relations as follows:

for $V_7=V_2$ $k_9 = \alpha k_8$ and $k_1+k_2= \alpha k_7$

for $V_3=V_4=V_5$ $k_3+k_4 = \alpha k_5$

The supplies are most efficiently used if one chooses $k_1+k_2 = k_7$, which also implies $k_7=k_8$. The other alternatives do either waste area or else degrade the common mode rejection.

In a process with symmetrical p and n-channel thresholds one can also choose $k_3=k_1$, etc., so that $V_4$ and respectively $V_7$ will be below -VS/2 when both M4C and M5C are saturated; such a choice leaves enough room for the cascode device M6C.

It follows that there are only two choices left to be made, namely the dc currents flowing through the two comparator stages. The current flowing through the output stage, $I'$ of Figure 3.34a, determines the time spent in saturated operation during the sampling of the analog input signal; this time, $t_1$ as given by (3.36') is inversely proportional to $I'$. But the same $I'$ does also determine the value of $gm_5$ which, for

stability reasons, has to satisfy condition (3.80). The final choice of $I'$ is therefore clearly the result of some compromise.

In order to be able to proceed with the design of the comparator it appears to be necessary to justify the choice made for $R_A$. This will be done next.

"Historically" the design of the PCM coder started with the sizing of the capacitor arrays. The total capacitance of the segment array, $C_s$=200pF, is therefore the result of the independent design considerations presented in section 3.1. The analog switches were designed next, but such as to yield acceptable time constants. Fortunately it turned out that the maximum time constant corresponding to a minimum size capacitor coupled with a minimum size switch and under worst biasing conditions is:

$$\tau = (.8pF)(57k) = 45.6ns$$

The worst case biasing conditions refer to the switching of the negative reference voltage. The resistance is derived with the classical formula:

$$r = \frac{1}{2\beta_p k(V_{GS}-V_{th})}$$

where: $V_{th} = V_{th}^{o} + \gamma_p\sqrt{V_{BS}}$ , $\beta_p$=5uA/$V^2$ and $\gamma_p$=.5$V^{-1/2}$.

The best case corresponds to the switching of the positive reference voltage and yields:

$$\tau = (.8pF)(12k) = 9ns$$

Since the time constants turn out to be relatively small, there is no need for accurate scaling of the analog switches.

The final switch sizes were therefore determined by convenient layout rather than by speed requirements.

The resulting equivalent resistances are: $R_A' = 1k$ at the switching of the negative reference and $R_A' = .2k$ at the switching of the positive reference voltage. $R_A'$ here refers only to the on-chip component of $R_A$. From a design point of view it was considered reasonable to add to $R_A'$ an external resistor of value .6k, quite typical in the telecommunication environment; this yields $R_{Amax}$=1.6k and $R_{Amin}$=.8k. Knowing $R_A$, we can now return to the task of setting the value of $I'$.

By imposing that $t_1$ of (3.36) be equal to about 10% of the time assigned for sample acquisition, which at a sampling rate of 16kHz is of about 15μs, we find:

$$I' = \frac{V_R C_s}{t_1} = \frac{3V \cdot 200pF}{1.5\mu s} = 400\mu A$$

Such a current will yield:

$$gm_5 = \frac{2I'}{V_{GS}-V_{th}} = .4mA/V$$

So that condition (3.80) reads:

$(.4mA/V)(1.6k) = .64 < 1$ or $(.4mA/V)(.8k) = .32 < 1$

Although condition (3.80) is not "strongly" satisfied for the chosen value of $gm_5$, it will be shown later that the choice is still acceptable. In any case it appears that there is some room left for improving on stability since $t_1$ could be easily increased with negligible penalty in speed.

The current flowing through the input stage is again the result of some compromise. From a speed point of view the time constant associated with node 4 should be as small as possible; therefore it would be desirable to minimize the capacitive load at this node. This can be done by building the input stage "stronger" than the output stage, so that the switching speed of the input stage will be determined by its "intrinsic" limits. From a stability point of view it would be desirable to "degrade" the output capacitance at node 4 so that the frequency $gm_{in}/C'_{4t}$ be sensibly smaller than $\omega_T$. Since speed turned out to be more critical than stability, the final choice was made for an input stage tail current of 1.6mA.

The final device sizes were determined initially by hand and then refined by using ISPICE.

3.3.7 Computer evaluation.

The performance of the "paper comparator" was analized using ISPICE. The circuit description used for this purpose is shown in TABLE 3.12; the biasing conditions at equilibrium are shown in TABLE 3.13, the small signal parameters in TABLE 3.14 and the junction capacitances in TABLE 3.15.

The dc transconductance characteristic of the CMOS comparator is shown in Figure 3.40. With reference to Figure 3.34a and the sample acquisition analysis we find:

$$w = 60mV$$

The time spent in saturated operation during sample acquisition can now be evaluated according to (3.36'); its

```
M1C 3 1 2 13 PSGX(12.8,9.99,16.0MI) 16.0MI,.4MI
M2C 4 0 2 13 PSGX(12.8,9.99,16.0MI) 16.0MI,.4MI
M3C 3 3 14 14 NSGX(9.0,9.0,6.0MI) 6.0MI,.22MI
M4C 4 3 14 14 NSGX(9.0,9.0,6.0MI) 6.0MI,.22MI
M5C 5 4 14 14 NSGX(2.4,2.4,3.0MI) 3.0MI,.22MI
M6C 6 0 5 5 NSGX(1.2,1.2,1.5MI) 1.5MI,.22MI
M7C 6 0 7 13 PSGX(7.2,2.0,8.0MI) 8.0MI,.4MI
M8C 7 11 13 13 PSGX(2.0,2.0,8.0MI) 8.0MI,.4MI
M9C 2 11 13 13 PSGX(19.88,19.88,32.0MI) 32.0MI,.4MI
M10C 0 6 10 13 PSGX(.64,1.5,.8MI) .8MI,.4MI
M11C 10 11 13 13 PSGX(1.5,.64,.8MI) .8MI,.4MI
M12C 0 0 11 13 PSGX(5.51,1.3,2.9MI) 2.9MI,.4MI
M13C 11 11 13 13 PSGX(1.3,1.3,2.9MI) 2.9MI,.4MI
DN 5 13 DN
MODEL DN D(CJO=.053Px9.61)
DP 6 13 DP
MODEL DP D(CJO=.0664PxSWA)
Vplus 13 0 7.5
Vminus 14 0 -7.5
```

<u>Circuit description of CMOS comparator</u>

TABLE 3.12

| | VGS (V) | VDS (V) | ID (μA) |
|---|---|---|---|
| M1C | -3.920 | -8.019 | 805.2 |
| M2C | -3.920 | -8.020 | 805.2 |
| M3C | 3.401 | 3.401 | 805.2 |
| M4C | 3.401 | 3.400 | 805.2 |
| M5C | 3.400 | 3.310 | 401.7 |
| M6C | 4.190 | 4.189 | 397.5 |
| M7C | -3.989 | -3.989 | 397.5 |
| M8C | -3.502 | -3.511 | 401.5 |
| M9C | -3.502 | -3.580 | 1610.4 |
| M10C | -3.998 | -3.998 | 40.1 |
| M11C | -3.502 | -3.502 | 40.1 |
| M12C | -3.998 | -3.998 | 145.5 |
| M13C | -3.502 | -3.502 | 145.5 |

Dc biasing conditions of CMOS comparator

TABLE 3.13

| | gm (mA/V) | gds (µA/V) | Cgs (pF) | Cgd (pF) |
|---|---|---|---|---|
| M1C | .82 | 16.56 | 1.45 | .35 |
| M2C | .82 | 16.56 | 1.45 | .35 |
| M3C | .82 | 13.91 | .53 | .30 |
| M4C | .82 | 13.91 | .53 | .30 |
| M5C | .41 | 7.04 | .27 | .15 |
| M6C | .28 | 6.33 | .13 | .07 |
| M7C | .39 | 9.63 | .73 | .18 |
| M8C | .38 | 16.34 | .73 | .18 |
| M9C | 1.51 | 64.79 | 2.91 | .70 |
| M10C | .04 | .97 | .07 | .02 |
| M11C | .04 | 1.64 | .07 | .02 |
| M12C | .14 | 3.53 | .26 | .06 |
| M13C | .14 | 5.93 | .26 | .06 |

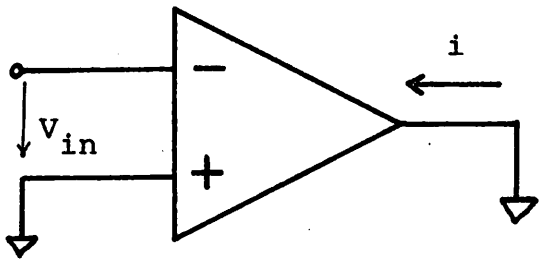
Small signal parameters of CMOS comparator

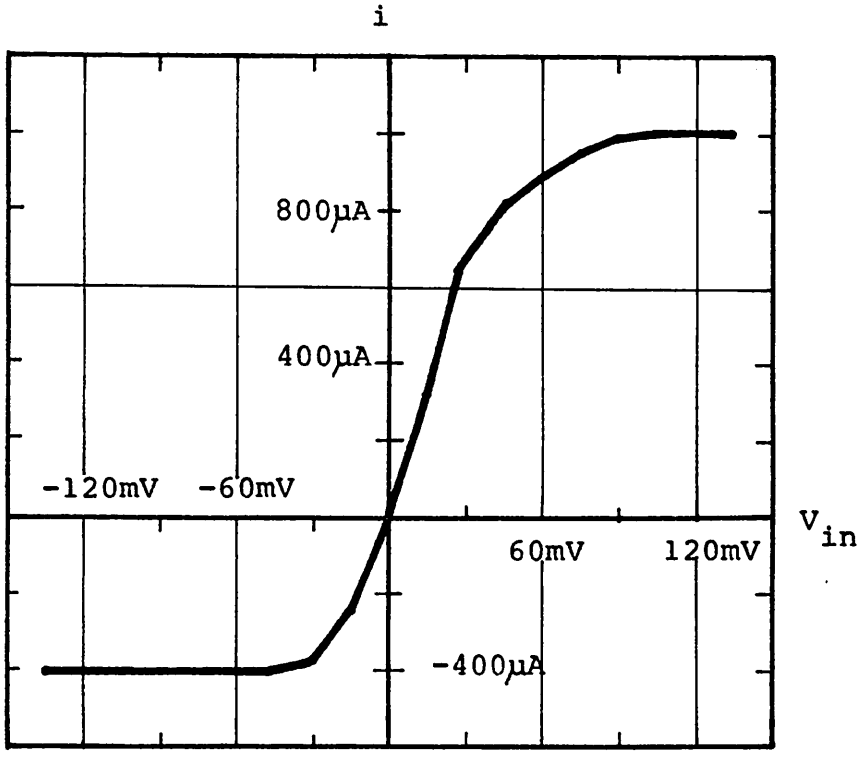
TABLE 3.14

| | | | |
|---|---|---|---|
| $Cjd_9$ | = .52pF; | $Cjd_90$ = 1.29pF; | $V_{rev}$ = 3.58V |
| $Cjs_1$ | = .26pF; | $Cjs_10$ = .65pF; | $V_{rev}$ = 3.58V |
| $Cjd_1$ | = .198pF; | $Cjd_10$ = .83pF; | $V_{rev}$ = 11.6V |
| $Cjd_3$ | = .643pF; | $Cjd_30$ = 1.56pF; | $V_{rev}$ = 3.4V |
| $Cjd_4$ | = .643pF; | $Cjd_40$ = 1.56pF; | $V_{rev}$ = 3.4V |
| $Cjd_2$ | = .198pF; | $Cjd_20$ = .83pF; | $V_{rev}$ = 11.6V |
| $Cjs_2$ | = .26pF; | $Cjs_20$ = .65pF; | $V_{rev}$ = 3.58V |
| $Cjd_5$ | = .173pF; | $Cjd_50$ = .42pF; | $V_{rev}$ = 3.31V |
| Cjp- | = .121pF; | Cjp-0 = .51pF; | $V_{rev}$ = 11.7V |
| $Cjd_6$ | = .079pF; | $Cjd_60$ = .21pF; | $V_{rev}$ = 4.19V |
| $Cjd_7$ | = .137pF; | $Cjd_70$ = .47pF; | $V_{rev}$ = 7.5V |
| $Cjs_7$ | = .053pF; | $Cjs_70$ = .13pF; | $V_{rev}$ = 3.5V |
| $Cjd_8$ | = .053pF; | $Cjd_80$ = .13pF; | $V_{rev}$ = 3.5V |
| $Cjd_{11}$ | = .04pF; | $Cjd_{11}0$ = .098pF; | $V_{rev}$ = 3.5V |
| $Cjs_{10}$ | = .04pF; | $Cjs_{10}0$ = .098pF; | $V_{rev}$ = 3.5V |
| $Cjd_{13}$ | = .035pF; | $Cjd_{13}0$ = .085pF; | $V_{rev}$ = 3.5V |
| $Cjs_{12}$ | = .035pF; | $Cjs_{12}0$ = .085pF; | $V_{rev}$ = 3.5V |

Junction capacitances for CMOS comparator.

TABLE 3.15




Dc transconductance characteristic of CMOS comparator.

Figure 3.40

maximum value will be:

$$t_1 = \left( \frac{3V - 30mV}{400uA} - .8k \right)(204pF) = 1.35\mu s$$

The time constant associated with nonsaturated sample acquisition, $\tau_A$ of (3.46) will have a maximum value of:

$$\tau_A = (1.6k)(204pF) = .326\mu s$$

Considering the time alloted for sample acquisition, about 31μs at 8kHz sampling rate and 15μs at 16kHz sampling rate, it turns out that one can safely neglect any initial condition effects.

The error multiplier, $\omega\tau_A$ of (3.50) will have a maximum value of:

$$\omega\tau_A = (2\pi\ 4kHz)(.326\mu s) = .75\%$$

The maximum acquisition error, $\varepsilon$ of (3.50) will therefore be of:

$$\varepsilon = .75\%\ 3V = 22.5mV$$

and it has been already mentioned that, even though such an error is greater than the whole first segment of the transfer characteristic, it should be nevertheless quite unharmful since it corresponds to low probability samples of a large signal. The specs for the codec being written for a signal frequency of 1kHz, it turns out that in this case $\varepsilon$ will be of about 5mV which is already within the magnitude of the first segment and possibly comparable to the dc offset of the transfer curve.

The results of the computer simulations supporting

the stability analysis of section 3.3.4 are presented in Figures 3.41 to 3.48. These computer simulation results do indeed fit very well with the simplified handanalysis. It is apparent that the differences due to the size of the sampling switch are quite small, thus making it possible to use a minimum size, minimum offset switch. The case $R_A$=.8k does correspond to the phase shift speculations made earlier; the unity gain crossover frequency of the loop gain is in this case equal to about 10% of the $\omega_T$ mentioned in the CMOS buffer section, and the phase margin is indeed close to $60^o$.

It should be mentioned that $R_A$ could in fact be smaller if the external component, due to finite source resistance, is less than .6k.

Using the circuit parameters shown in the tables we can evaluate the comparator delay on the basis of (3.147) with:

$C_{4t}$ = 1.91pF

$g_4$ = 30.5μA/V

$C_6$ = .4pF

$g_5$ = 6.33μA/V or $g_8$ = 16.34μA/V

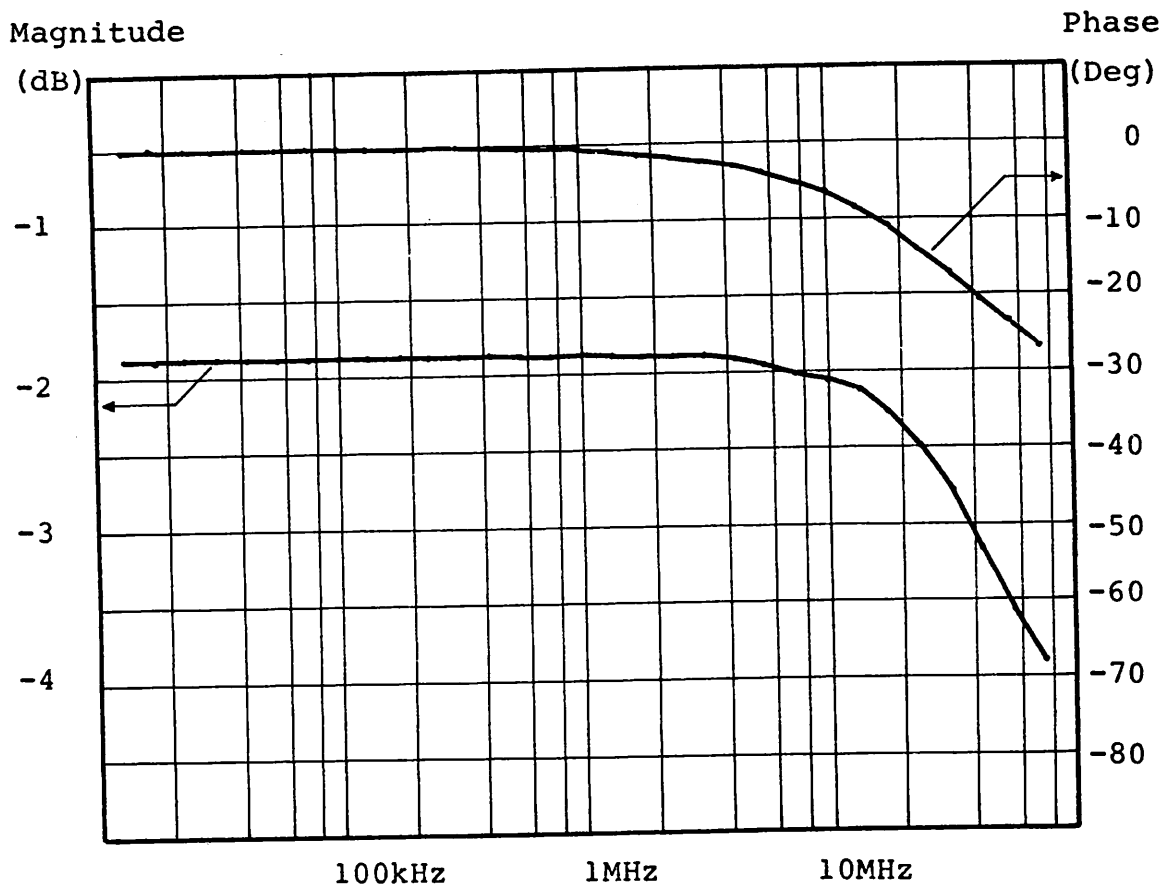
$\Delta V_1 = V_R/(255x2)$

OVERDR = $V_R/(255x16x2)$

$$g_{out} = \frac{g_5 g_6}{gm_6+g_5+g_6} + \frac{g_7 g_8}{gm_7+g_7+g_8} = .53\mu A/V$$

$$A_{tot} = (gm_2/g_4)(gm_5/g_{out}) = (27)(773) = 20,000$$

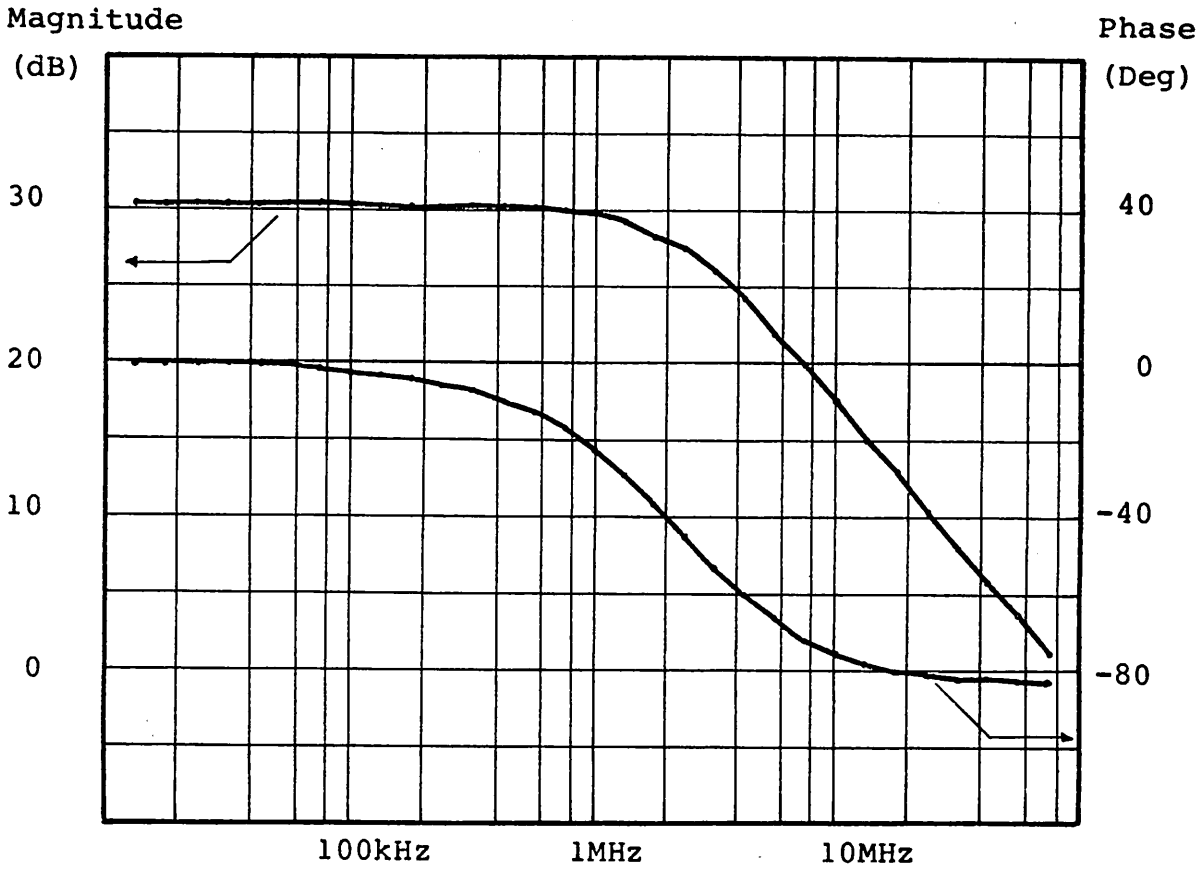
$V_{th}$ = 1.5V




Input stage transadmitance magnitude/phase characteristics.

( 0dB corresponds to a transconductance of 1mA/V )

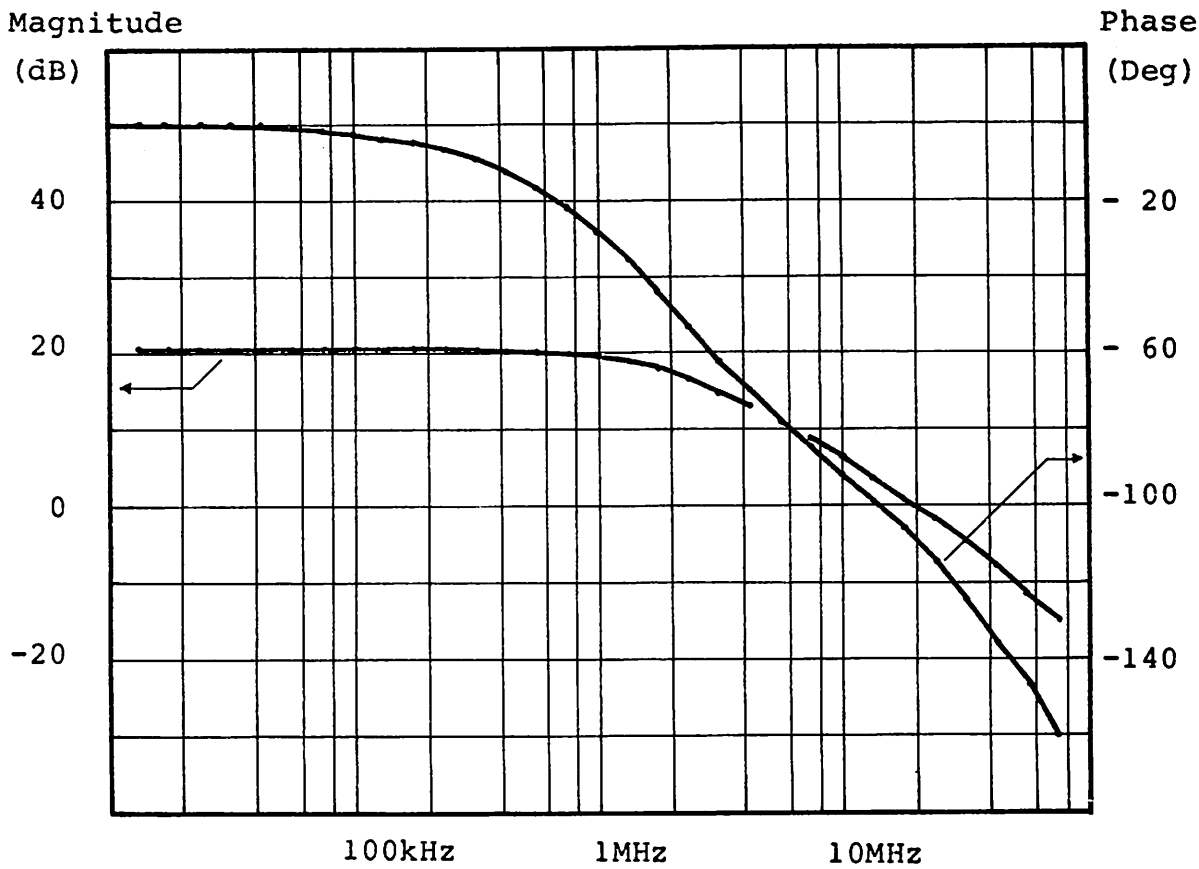
Figure 3.41




Input stage output impedance magnitude/phase characteristics.

( 0dB corresponds to a 1k resistor )

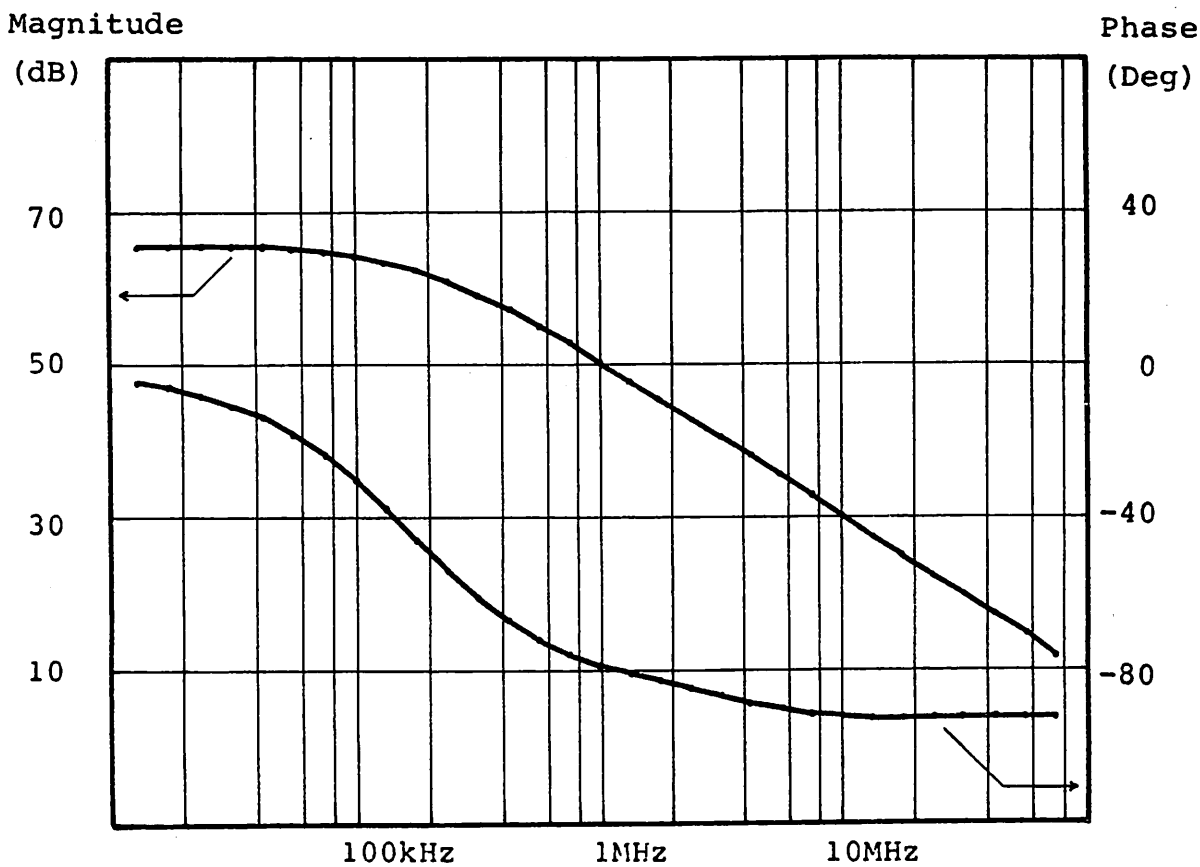
Figure 3.42




CMOS comparator transadmitance magnitude/phase characteristics.

( 0dB corresponds to a transconductance of 1mA/V )

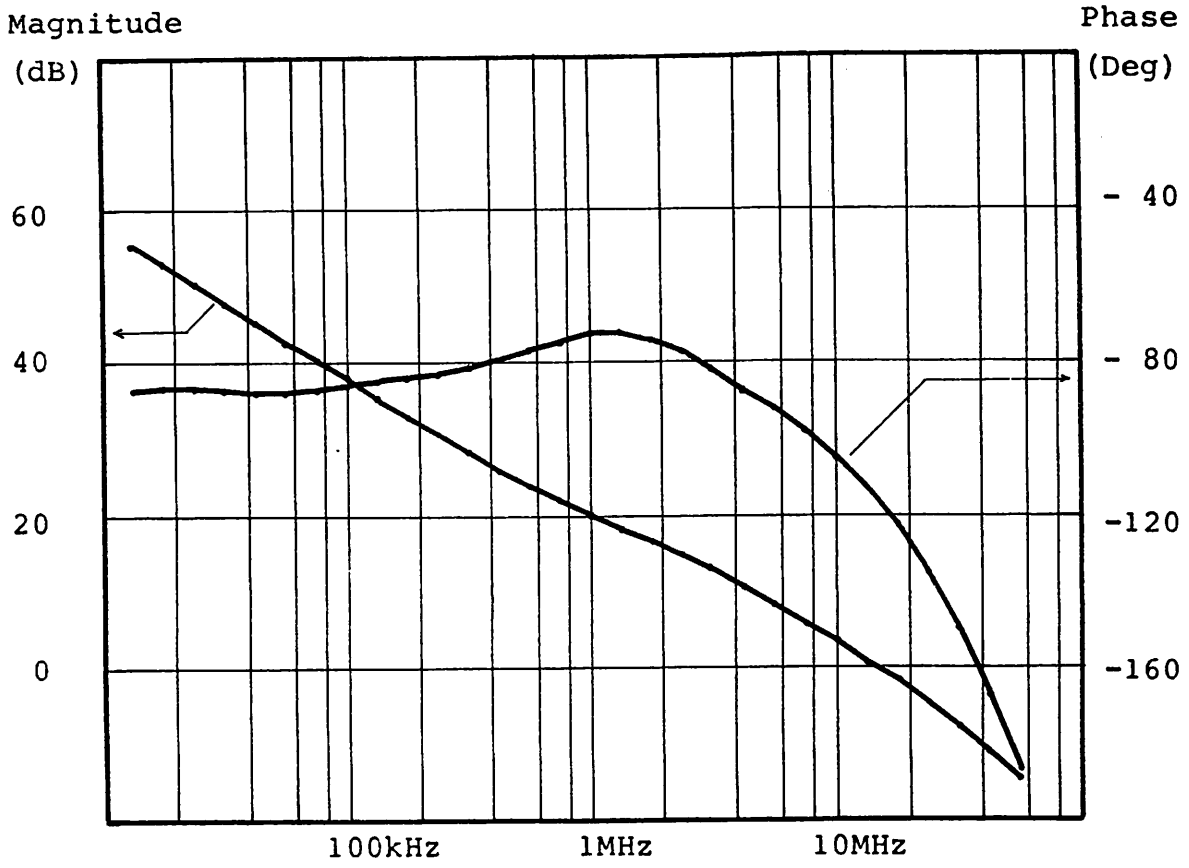
Figure 3.43




CMOS comparator output impedance magnitude/phase characteristics.

( 0dB corresponds to a 1k resistor )

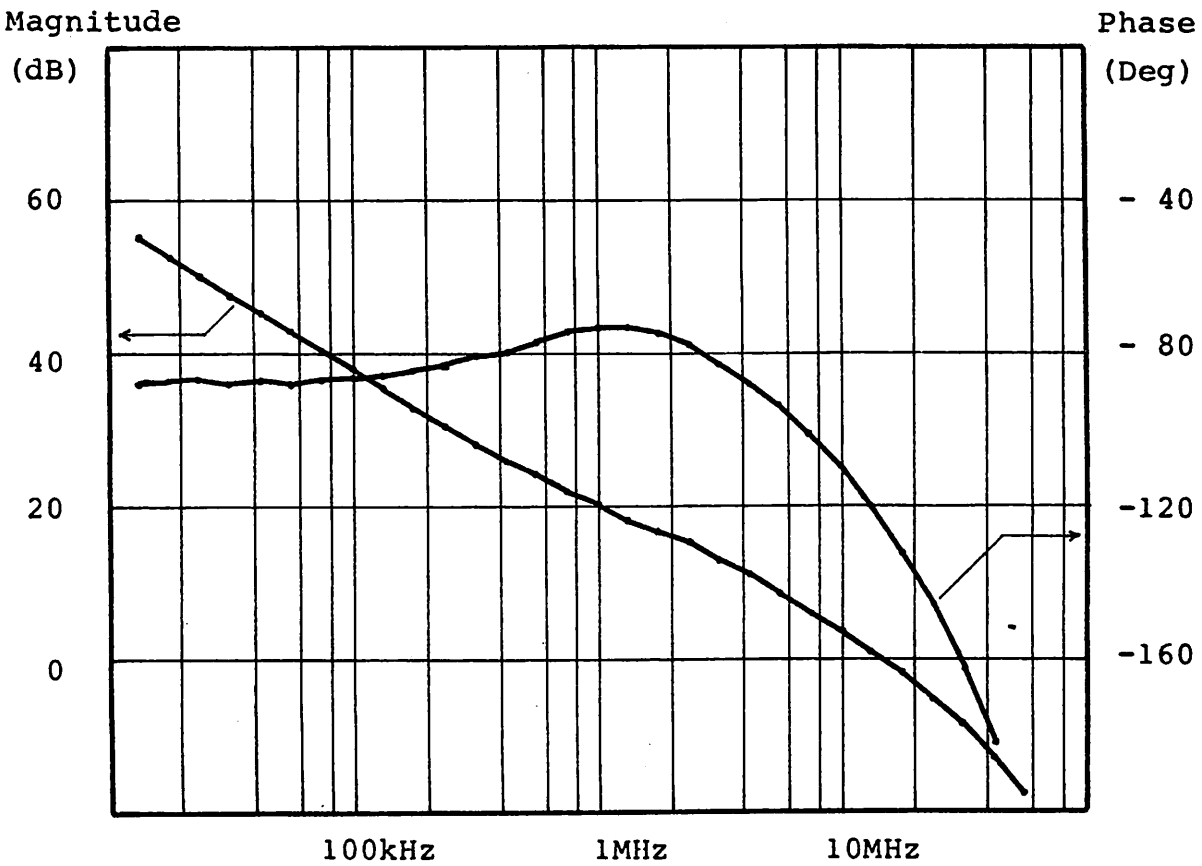
Figure 3.44




Loop gain magnitude/phase characteristics with $R_A$=.8k and large sampling switch.

Unity gain crossover frequency is 15MHz
Phase margin is $63^{o}$

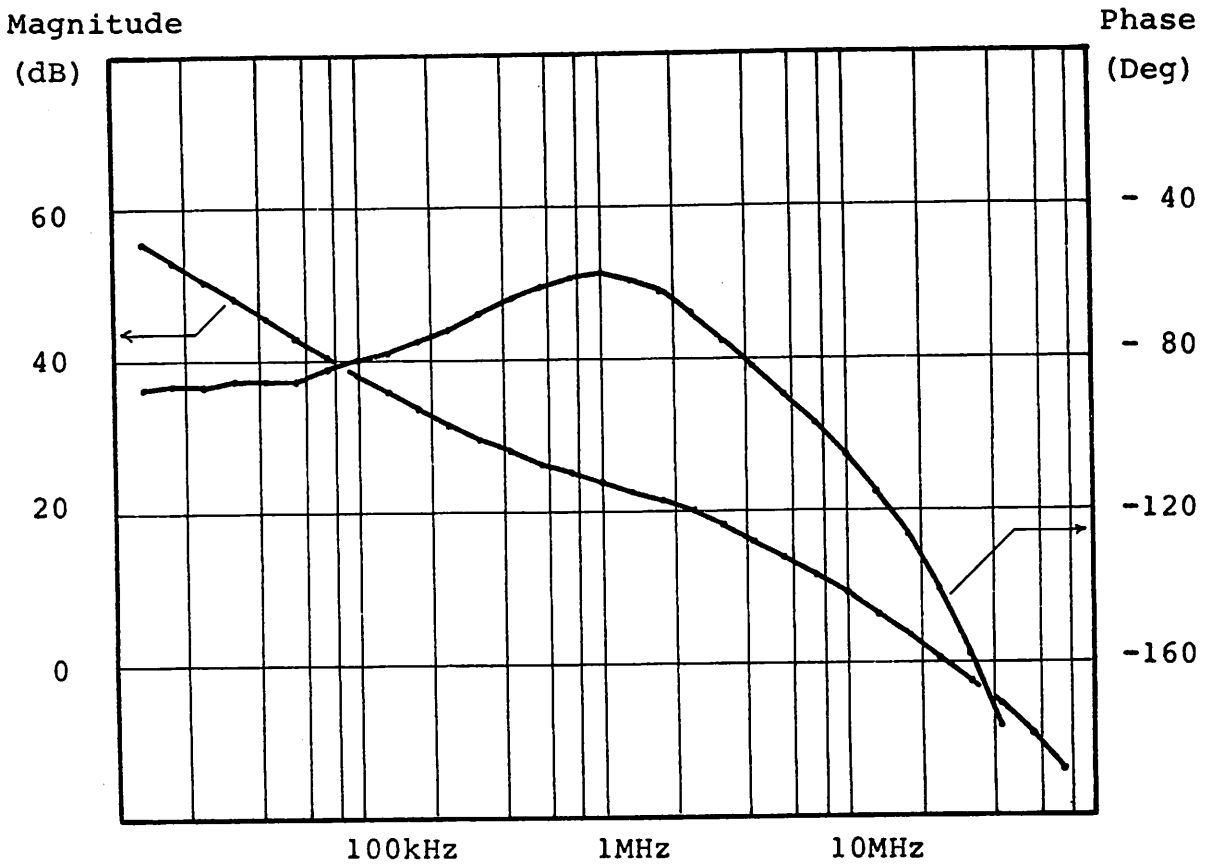
Figure 3.45




Loop gain magnitude/phase characteristics with $R_A$=.8k and minimum size sampling switch.

Unity gain crossover frequency is 14.5MHz
Phase margin is $56^{o}$

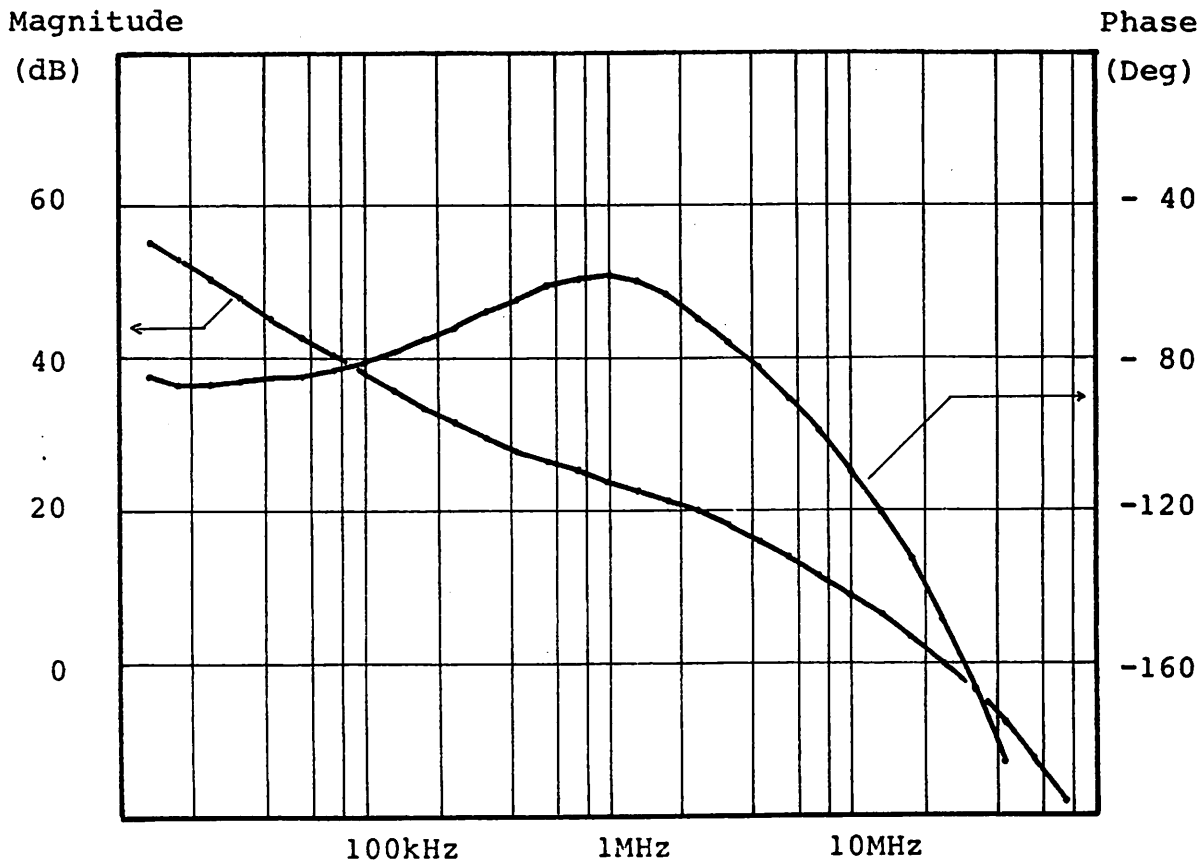
Figure 3.46




Loop gain magnitude/phase characteristics with $R_A$=1.6k and large sampling switch.

Unity gain crossover frequency is 24.5MHz
Phase margin is $37^{o}$

Figure 3.47




Loop gain magnitude/phase characteristics with $R_A$=1.6k and minimum size sampling switch.

Unity gain crossover frequency is 23.5MHz
Phase margin is $32^{o}$

Figure 3.48

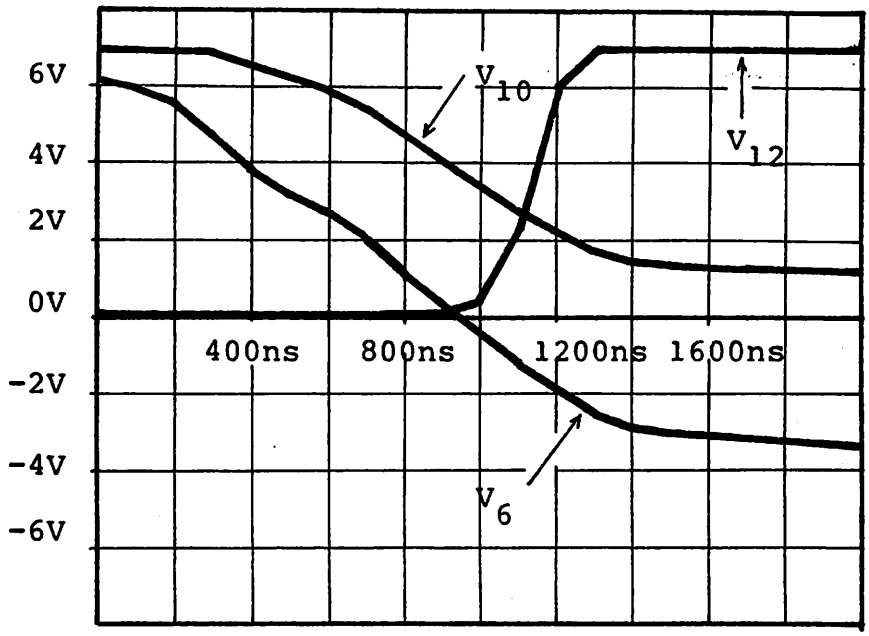
Using these numbers we find:

$$\Delta t = .325\mu s + .232\mu s + .755\mu s = 1.312\mu s \qquad (3.147)$$

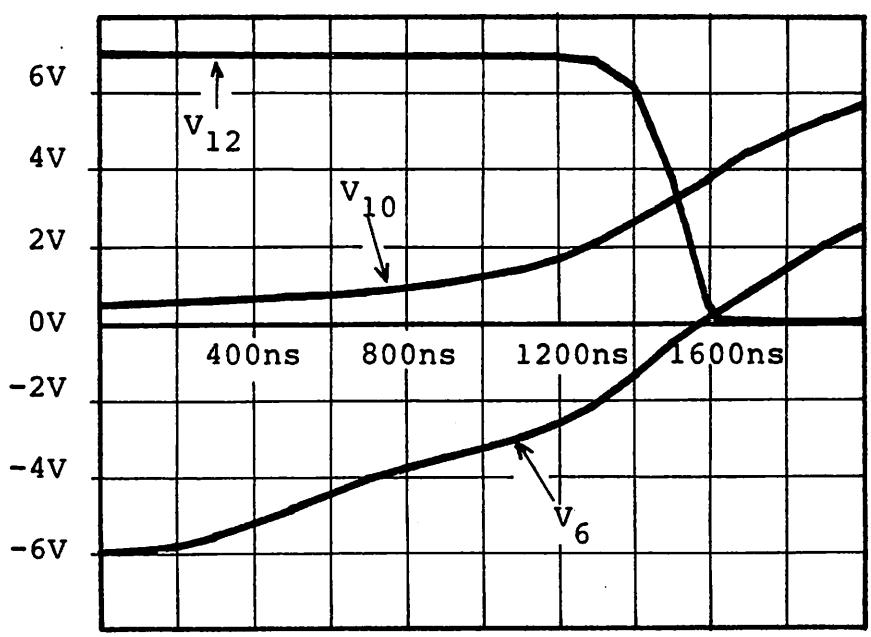
Both the gain and the delay exceed the required performance but are obviously based on the less predictable output resistance of saturated transistors. This is indeed the weak point of the linear amplifier approach chosen for the implementation of the comparator. In order to compensate for this weakness every reasonable effort has been made to fit the device models used in ISPICE to existing devices. The relatively high yield of the finished chips shows that such an approach hasn't been totally wrong.

The computer simulated response under minimum overdrive conditions is presented in Figure 3.49. During this simulation the supplies were of 7V and the input voltage swing was equal to the length of the first segment, i.e. $V_R/255$. The total delay as given by (3.147) is reasonably close to the computer results although the partial delays, semilinear, saturated, etc. do not seem to fit very well. Apparently the comparator spends most of the time in the semilinear phase with a shorter period of saturated operation. The simplified hand analysis of the switching process is nevertheless useful at least qualitatively.

The experimental performance of the comparator can be evaluated only in the context of the complete coder and will be discussed in the final conclusions of this report.




$V_6$ is the comparator output voltage
$V_{10}$ is the level shifter output voltage
$V_{12}$ is the output voltage of the inverter following the level shifter




Comparator response under minimum overdrive conditions.

Figure 3.49

## 3.4 THE CMOS SAMPLE AND HOLD BUFFER AMPLIFIER.

The sample and hold (S/H) buffer amplifier is used in the decoder section of the PCM codec, where it buffers the segment capacitor array from the outside world. The amplifier will produce a staircaise output so that the gain requirements imposed on the filter following the decoder are considerably simplified.

### 3.4.1 Design objectives.

One of the most important design objectives imposed on the codec implementation was to eliminate as many external components as possible; therefore an attempt was made to incorporate a complete S/H amplifier on the decoder chip.

It may be necessary to mention that the task of the S/H amplifier is in this case rather simple compared to the many possible tasks encountered by a general purpose S/H amplifier. For instance: in the sample mode the amplifier is presented with inputs that are stable throughout the whole sampling interval; therefore aperture time is zero. The dc offset of the amplifier has practically no influence on the codec performance since the dc component of the output waveform is filtered out.

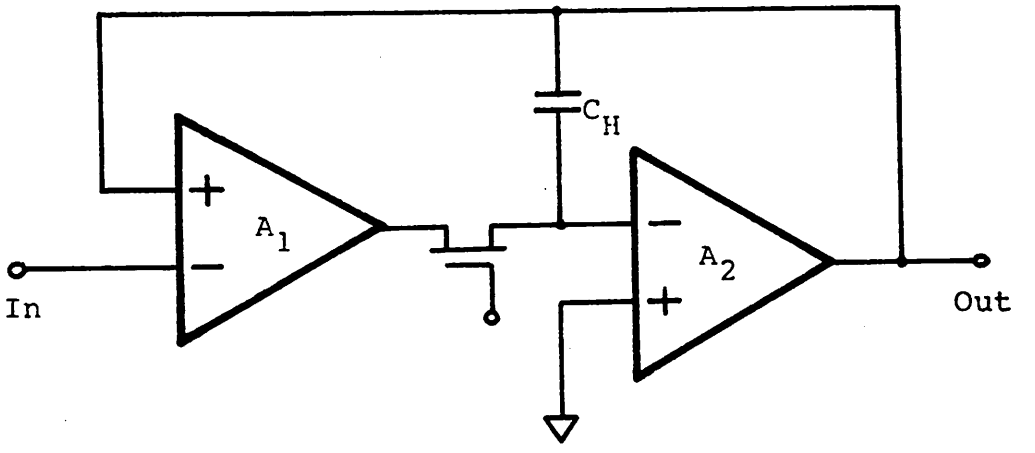
The S/H amplifier should be able to handle a common mode range of $\pm V_R$. At a sampling frequency of 8kHz and with a staircaise output the amplifier should be fast enough to allow the output to settle within 1% of its final value in less than 5μs, corresponding to about 4% of the sampling period. This has to be done in the presence of a typical

load consisting of a parallel combination between a 10k resistor and a 50pF capacitor.

The solution that was chosen for the implementation of the S/H buffer amplifier is of the integrating type, Figure 3.50, and has been used before for the implementation of a completely monolithic S/H amplifier ( 17 ).

The important advantage of this configuration is that the sampling switch operates at ground potential so that the feedthrough at switch opening, hence the dc offset introduced at the output, is constant. As mentioned earlier, this constant dc offset is practically unharmful as far as the operation of the codec is concerned. The fact that the dc offset is tollerable does also simplify the construction of the switch itself and of the associated driving circuitry. Thus for instance there appears to be no need for clamping the output of the transconductance amplifier $A_1$ in order to reduce the gate drive of the sampling switch. Obviously, the reduced gate drive itself would require more than a regular switch driver operating between the two supplies. Since the size of the sampling switch is not constrained by feedthrough considerations, one can design the switch for stability, i.e. such that the undesired pole resulting from the combination between the equivalent switch resistance and the output capacitance of the transconductance amplifier will be sufficiently removed from the system bandwidth.

It may be intersting to mention that CMOS is in this case perfectly suited for the implementation of a broadband




Integrating sample and hold amplifier.

Figure 3.50

transconductance amplifier, a low input leakage hold amplifier, low leakage bidirectional sampling switch and a good quality integrated hold capacitor.

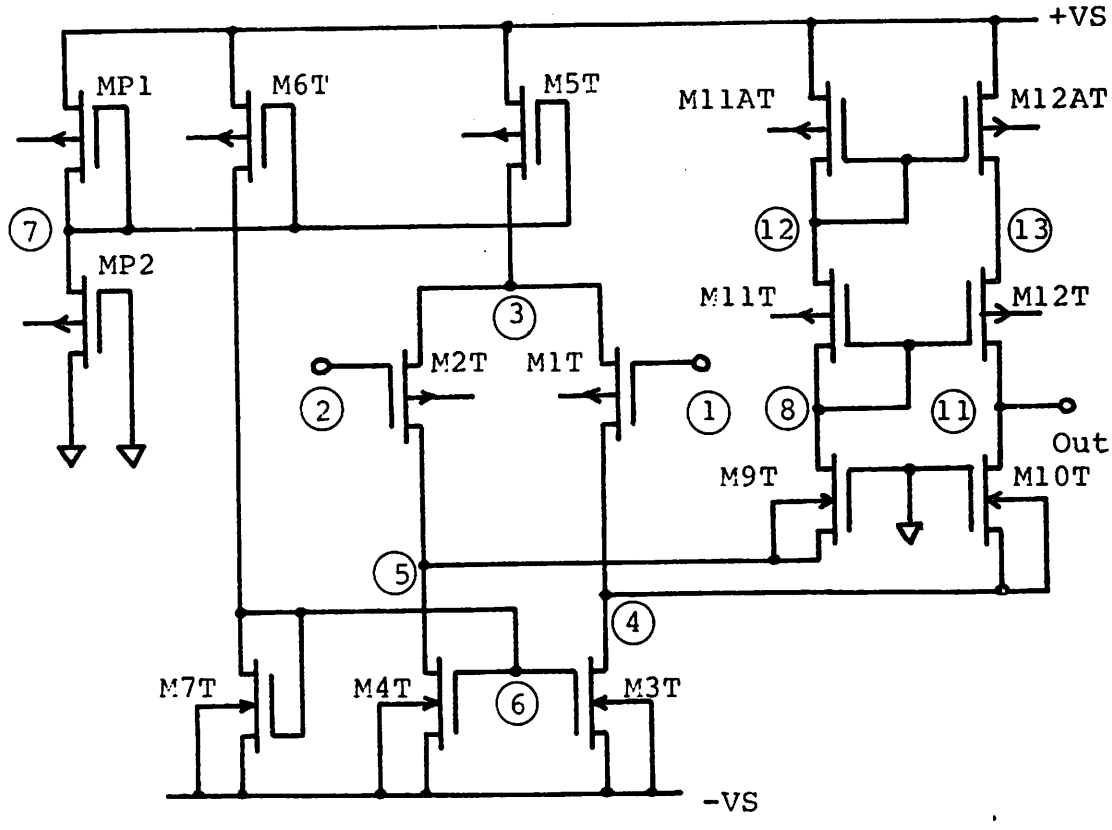
3.4.2 The transconductance amplifier.

The topology chosen for the transconductance amplifier is shown in Figure 3.51. This amplifier supplies the charging current to the hold capacitor $C_H$ and has to be broadbanded for stability reasons.

The circuit contains a differential input stage used to steer the current flowing through a current mirror type output stage. At zero differential input voltage the tail current flowing through M5T is equal to the current flowing through M3T and respectively M4T. As a result of this equality and due to symmetry, the currents flowing through M1T, M2T, M9T, M11T, M11AT, M10T, M12T and M12AT are all equal. Therefore the maximum current capability of the output stage is equal to the tail current of the input stage. The stacking of devices M11T, M11AT and M12T, M12AT is used in order to reduce the nominal dc offset of the amplifier and to increase the dc output resistance.

The scaling of the currents in the two stages was chosen such as to yield the best use of the available power. More quiescent current flowing through the output stage would represent a waste of current; with less quiescent current the output stage would not be able to handle the maximum current which the input stage can switch.

This combination of input and output stage provides




CMOS transconductance amplifier.

Figure 3.51

a convenient means of differentially driving a current source whose output nominally operates at ground potential.

In order to evaluate the stability of the sample and hold configuration one has to replace the individual components with the appropriate small-signal equivalent circuits. The transconductance amplifier will be naturally replaced with an equivalent current generator.

The low frequency transadmitance of the amplifier can be found "by inspection" on the basis of Figure 3.52.

At equal currents and approximately equal $V_{GS}$'s the gm's of transistors M1T, M2T, M9T, M10T, M11T and M12T are approximately equal. The low frequency load seen by transistors M1T and M2T at nodes 4 and respectively 5 will therefore be equal to $1/gm_T$ (where $gm_T=gm_1=gm_2=...$). Since the gm's of M1T and M2T are also equal to $gm_T$ it follows that:

$$V_4 - V_5 = V_2 - V_1$$

With the output stage acting as a current mirror, the short circuit current of the transconductance amplifier will be equal to:

$$I_{SHORT} = gm_T V_4 - gm_T V_5 = gm_T (V_2 - V_1)$$

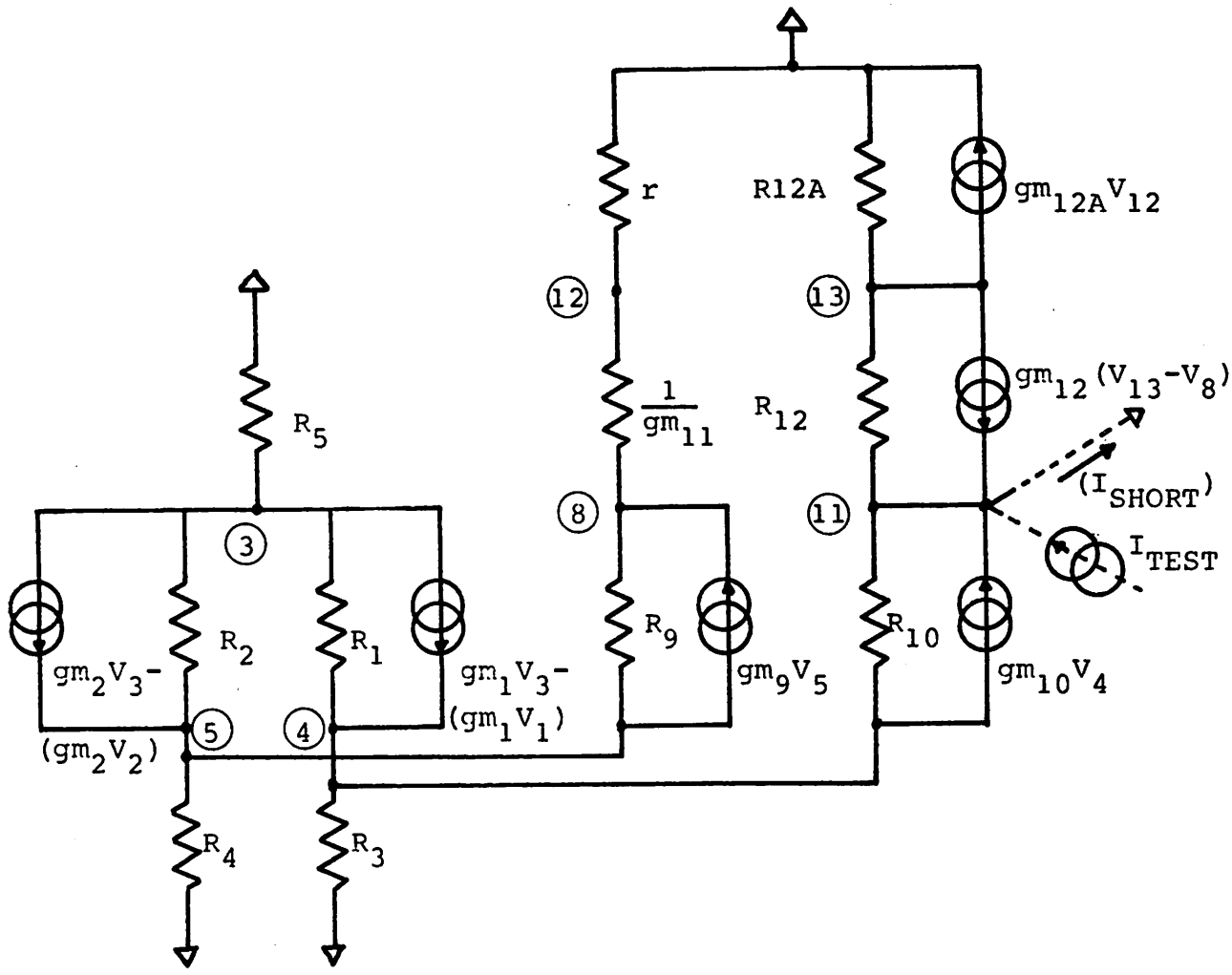
The "upper" branch contribution, $-gm_T V_5$, is the result of:

$$V_8 = gm_T V_5 (r + \frac{1}{gm_T}) = (1 + gm_T r) V_5$$

$$V_{12} = gm_T r V_8 / (1 + gm_T r)$$

$$gm_{12A} V_{12} = V_{12}/r = gm_T V_5$$

where: $r = 1/gm_{11A} = 1/gm_{12A}$ .




Small-signal equivalent circuit of transconductance amplifier.

Figure 3.52

It follows that the low frequency transadmitance of the transconductance amplifier is equal to $gm_T$, the common gm of transistors M1T, M2T, M9T, M10T, M11T and M12T.

The only high impedance node in the amplifier is the output, node 11; therefore the transadmitance will be constant and equal to $gm_T$ up to breakfrequencies generated by the internal nodes. These breakfrequencies are approximately equal to:

$$\omega_4 = \omega_5 = gm_T/C_{4t} \quad \text{where } C_{4t} = Cjd_1+Cgd_1+Cjd_3+Cgd_3+Cgs_9$$

$$\omega_8 = gm_T/C_{8t} \quad \text{where } C_{8t} = Cgs_{11}+Cgs_{12}+Cjd_{11}+Cgd_{12}+Cgd_9$$

$$\omega_{12} = (gm_T+1/r)/C_{12t} \quad \text{where } C_{12t} = Cgs_{11}+Cgs_{11A}+Cgs_{12A}+Cjd_{11A}+Cjs_{11}+Cgd_{12A}$$

$$\omega_{13} = gm_T/C_{13t} \quad \text{where } C_{13t} = Cgs_{12}+Cgd_{12A}+Cjd_{12A}+Cjs_{12}$$

and are of the same order of magnitude with $\omega_T$, the frequency at which the common gate current gain of the MOS transistors equals 1/2.

The output impedance at node 11 is found by grounding both inputs, nodes 1 and 2, and applying a test generator at node 11. The analysis can be considerably simplified by observing that the relatively large dc output resistance (a result of the cascode type connection) coupled with the node capacitance $C_{11}$ will generate a low frequency break beyond which the output impedance will be dominated by $C_{11}$.

As a result of this observation it appears justified to consider that the real part of the output impedance will be equal to the dc output resistance and the imaginary part equal to

the output capacitance. The purely resistive part of the output impedance will in fact decrease with increasing frequency but this will start happening at frequencies far beyond the first break and at those frequencies the output impedance will by dominated anyway by the node capacitance $C_{11}$.

The output resistance is found on the basis of the same Figure 3.52. Rather than writing a complete set of nodal equations it seems to be more instructive to proceed on a step by step basis. The output resistance at node 11 can be considered as being the result of a parallel combination between an "upward" and a "downward" component. The value of the downward component is found by looking only towards M10T.

Going through M10T, M1T, M3T, etc. it turns out that one has to go as far as node 12 and start working backwards from there. Thus:

$$V_{12} = \frac{rV_8}{\frac{1}{gm_T} + r} \quad \text{or} \quad \frac{V_{12}}{V_8} = \frac{gm_T r}{1+gm_T r}$$

$$(V_5-V_8)G_9+gm_9V_5 = \frac{V_8}{\frac{1}{gm_T}+r} \quad \text{or} \quad \frac{V_8}{V_5} \cong 1+gm_T r$$

$$(V_3-V_5)G_2+gm_2V_3=G_4V_5+gm_9V_5+G_9(V_5-V_8) \quad \text{or} \quad \frac{V_5}{V_3} \cong 1$$

$$(V_4-V_3)G_1-gm_1V_3 = G_5V_5+G_2(V_3-V_5)+gm_2V_3 \quad \text{or} \quad \frac{V_3}{V_4} \cong \frac{1}{2gm_T R_1}$$

Based on these results one can now evaluate the output resistance at node 4, looking "into" the input stage:

$$\frac{1}{R_{o4}} = G_3 + \frac{G_1(V_4-V_3)-gm_1V_3}{V_4} \cong G_3 + G_1/2 = \frac{R_3 + 2R_1}{2R_1R_3}$$

The downward contribution to $R_{o11}$ can thus be expressed with the well known formula:

$$R^d_{o11} = R_{o4} + (1+gm_{10}R_{o4})R_{10} \cong \frac{2gm_T R_1 R_3 R_{10}}{2R_1+R_3}$$

The upward component, looking through M12T is found on the basis of the following computation:

$$\frac{V_4}{V_{11}} = \frac{R_{o4}}{R_{o4}+(1+gm_T R_{o4})R_{10}} \cong \frac{1}{gm_T R_{10}}$$

$$\frac{V_3}{V_{11}} = \frac{V_3}{V_4} \times \frac{V_4}{V_{11}} \cong \frac{1}{2gm_T^2 R_1 R_{10}}$$

$$\frac{V_5}{V_{11}} = \frac{V_5}{V_3} \times \frac{V_3}{V_{11}} \cong \frac{1}{2gm_T^2 R_1 R_{10}}$$

$$\frac{V_8}{V_{11}} = \frac{V_8}{V_5} \times \frac{V_5}{V_{11}} \cong \frac{1+gm_T r}{2gm_T^2 R_1 R_{10}}$$

$$\frac{V_{12}}{V_{11}} = \frac{V_{12}}{V_8} \times \frac{V_8}{V_{11}} \cong \frac{r}{2gm_T R_1 R_{10}}$$

$$gm_{12}(V_{13}-V_8)+G_{12}(V_{13}-V_{11})+gm_{12A}V_{12}+G_{12A}V_{13}=0$$

Thus:

$$\frac{V_{13}}{V_{11}} \cong \frac{G_{12}+(r/2R_1R_{10})}{gm_T+G_{12}+G_{12A}} \cong \frac{G_{12}}{gm_T+G_{12}+G_{12A}}$$

and:

$$\frac{1}{R^u_{o11}} = \frac{G_{12A}V_{13}+V_{12}/r}{V_{11}} \cong \frac{G_{12}G_{12A}}{gm_T+G_{12}+G_{12A}} + \frac{1}{2gm_T R_1 R_{10}}$$

The total output resitance can now be expressed as:

$$\frac{1}{R_{oT}} = \frac{1}{R^u_{o11}} + \frac{1}{R^d_{o11}} \cong \frac{1}{gm_T R_{12} R_{12A}} + \frac{R_1+R_3}{gm_T R_1 R_3 R_{10}} \qquad (3.148)$$

The output capacitance is simply:

$$C_{oT} = Cjd_{10}+Cjd_{12}+Cgd_{10}+Cgd_{12}+C_{SW} \qquad (3.149)$$

where $C_{SW}$ is the capacitance associated with the switch connecting the transconductance amplifier to the hold capacitor.

The transconductance amplifier can thus be replaced with an equivalent current generator described by:

$$Y_{tr} = gm_T \qquad (3.150)$$

and $$Y_{oT} = sC_{oT} + G_{oT} \qquad (3.151)$$

where $C_{oT}$ is given by (3.149) and $G_{oT}$ by (3.148).

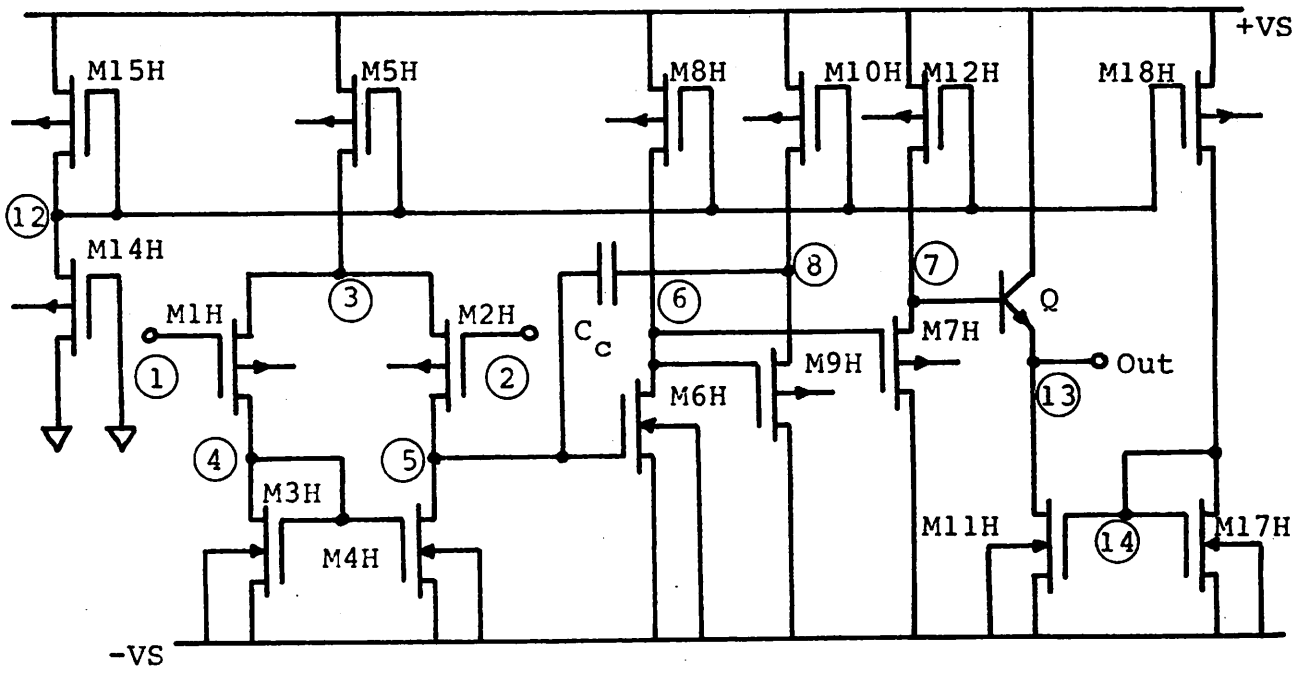
3.4.3 <u>The hold amplifier.</u>

The circuit topology chosen for the hold amplifier is shown in Figure 3.53. It contains a "basic amplifier", similar to the ones used in conjunction with the step capacitor arrays, followed by an output stage with very low output resistance.

The low output resistance is obtained through a double buffering of the basic amplifier. The bipolar transistor is implemented with a substrate npn structure "naturally" available in CMOS and was used solely for its very low output resistance. This type of output stage was added because at the time of the original design it was felt that the decoder should be able to directly drive relatively low resistance loads.

The unity gain compensated basic amplifier is needed because the hold amplifier has to be stable in the hold mode, when it operates in a unity gain configuration.

The stability conditions in the hold mode as well as in




CMOS hold amplifier ("opamp").

Figure 3.53

the sampling mode can be spelled out in a suggestive manner by replacing the hold amplifier with an equivalent voltage generator. The necessary analysis is considerably simplified if one makes use of the results obtained in the CMOS buffer section. Thus the "basic amplifier" portion can be replaced itself with an equivalent voltage generator described by:

$$A_B = \frac{gm_1 R_{o1} gm_6 R_6 (1+sC_c/gm_9)}{1+sC_c gm_6 R_6 R_{o1}} \cong \frac{gm_1}{sC_c} + \frac{gm_1}{gm_9} \qquad (3.152)$$

$$Z_{oB} = \frac{R_6 (1+sC_c R_{o1})}{1+sC_c gm_6 R_6 R_{o1}} \cong \frac{1}{sC_c gm_6 R_{o1}} + \frac{1}{gm_6} \qquad (3.153)$$

where $R_{o1}$ is the output resistance of the input stage, $R_6$ is the equivalent resitance at node 6, etc.

The voltage gain and output impedance of the complete hold amplifier can be found on the basis of Figure 3.54.

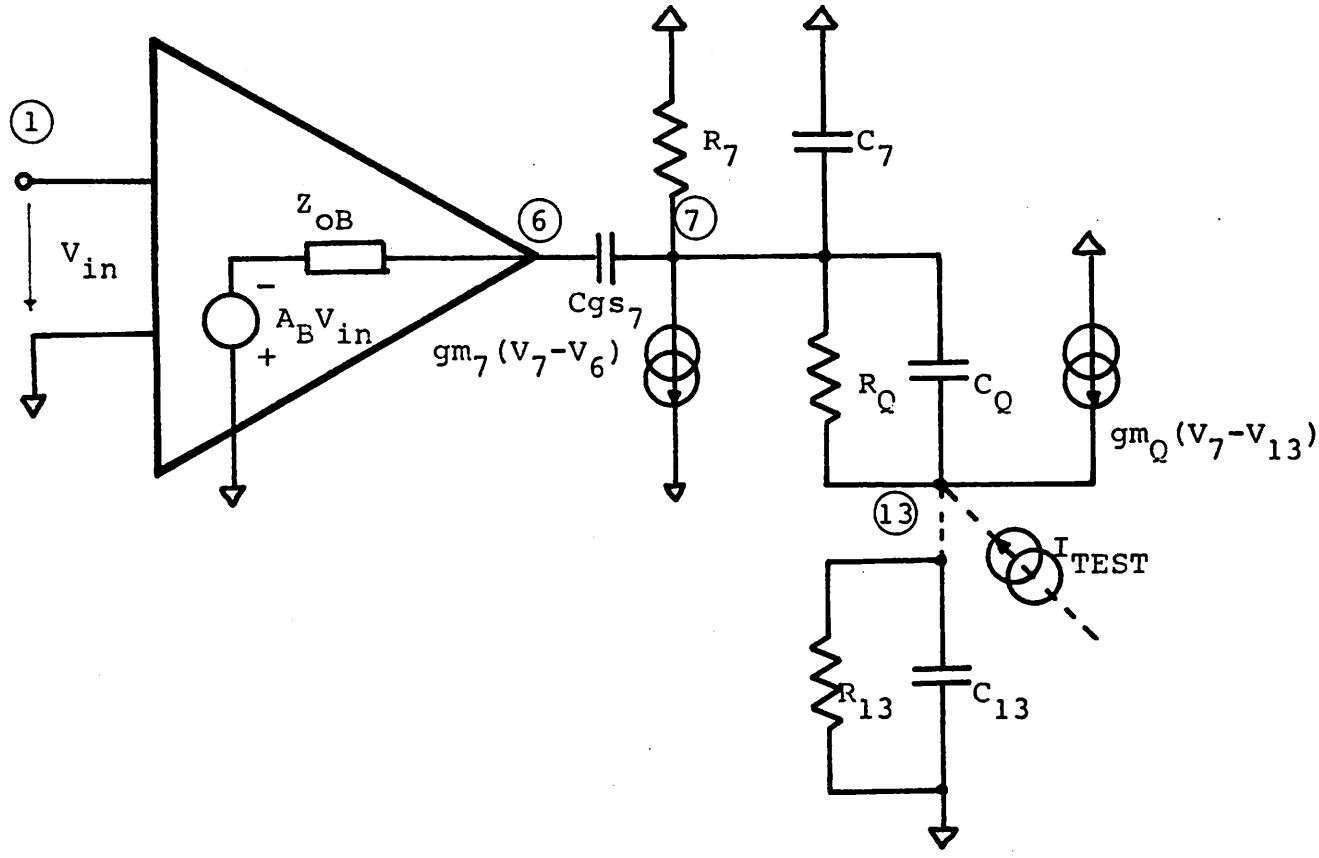
Observing that normally: $gm_6 R_{o1} C_c \gg Cgs_7$, one can replace the series combination between these two capacitors with $Cgs_7$ alone. The open circuit voltage gain is now found as follows:

$$(V_7+A_B V_{in}) \frac{sCgs_7 gm_6}{gm_6+sCgs_7} + gm_7(V_7-V_6) + (G_7+sC_7)V_7 + (V_7-V_{13})(g_Q+sC_Q) = 0 \qquad (3.154)$$

$$(V_6+A_B V_{in}) gm_6 = sCgs_7 (V_7-V_6) \qquad (3.155)$$

$$(V_7-V_{13})(g_Q+sC_Q)+gm_Q(V_7-V_{13})=V_{13}(G_{13}+sC_{13}) \qquad (3.156)$$

From (3.156) and with $gm_Q \gg G_{13}$, $C_Q \gg C_{13}$ we find:




Small-signal equivalent circuit of hold amplifier.

Figure 3.54

$$V_7 \cong V_{13} \tag{3.156'}$$

Combining this result with (3.154) and (3.155) we find:

$$A_H^o = \frac{V_{13}}{V_{in}} \cong -\frac{A_B(1 + sCgs_7/gm_7)}{1 + s(Cgs_7+C_7)/gm_7 + s^2(Cgs_7/gm_7)(C_7/gm_6)}$$

If $gm_6 \cong gm_7$ then this last expression can be simplified to:

$$A_H^o \cong -\frac{A_B}{1 + sC_7/gm_6} \tag{3.157}$$

The output impedance is found by grounding the input, i.e. $V_{in}=0$ in Figure 3.54 and applying a test generator at node 13.

The intermediate output impedance at node 7 (neglecting for the time being $R_7$ and $C_7$) is found on the basis of:

$$I_{TEST} = gm_7(V_7-V_6) + \frac{V_7 sCgs_7 gm_6}{sCgs_7+gm_6}$$

$$V_6 = \frac{sCgs_7 V_7}{sCgs_7+gm_6}$$

Thus:

$$\frac{I_{TEST}}{V_7} = gm_6 \frac{gm_7+sCgs_7}{gm_6+sCgs_7} \cong gm_6$$

The total intermediate output impedance can thus be replaced with the parallel combination between $C_7$ and $1/gm_6$.

The partial output impedance at node 13, neglecting $R_{13}$ and $C_{13}$ is found on the basis of:

$$I_{TEST} = -(gm_Q+g_Q+sC_Q)(V_7-V_{13}) \tag{3.158}$$

$$(g_Q+sC_Q)(V_7-V_{13}) + V_7(gm_6+sC_7) = 0 \tag{3.159}$$

Thus:

$$Z'_{o13} = \frac{V_{13}}{I_{TEST}} = \frac{g_Q+gm_6+sC_Q}{(gm_Q+sC_Q)(gm_6+sC_7)} \qquad (3.160)$$

The zero in (3.160), $(g_Q+gm_6)/C_Q$, occurs at a frequency about $\beta$ times smaller than the frequency corresponding to the pole $gm_Q/C_Q$ and the pole $gm_6/C_7$ is normally also quite removed from the zero. Therefore the output impedance can be expressed over a wide frequency range as:

$$Z'_{o13} \cong \frac{g_Q+gm_6}{gm_Q gm_6} + \frac{sC_Q}{gm_Q gm_6} \qquad (3.160')$$

or:

$$Z'_{o13} \cong \frac{1}{\beta gm_6} + \frac{1}{gm_Q} + \frac{s}{\omega_{TQ} gm_6} \qquad (3.160'')$$

where $\omega_{TQ}$ is the unity current gain frequency of the common base connected substrate npn and $\beta$ is the current gain.

For simplicity the neglected contribution, $R_{13}$ and $C_{13}$, can be included in the load seen by the amplifier. Thus:

$$Z_{oH} = Z'_{o13} \qquad (3.161)$$

Since this impedance has an inductive character it seems reasonable to write:

$$Z_{oH} = R_{oH} + sL_{oH} \qquad (3.161')$$

with:

$$R_{oH} = (1/gm_Q) + (1/\beta gm_6)$$

and:

$$L_{oH} = 1/\omega_{TQ} gm_6$$

3.4.4 Stability analysis.

The stability of the hold amplifier operating in the hold mode can be evaluated using Figure 3.55 . Since the input capacitance of the hold amplifier is normally much smaller than the value of the hold capacitor it turns out that the feedback factor is equal to 1; therefore the amplifier has to be unity gain stable.

The open loop gain in the presence of the load can be expressed as:

$$A_H^L = A_H^o \frac{Z_L}{Z_L + Z_{oH}} = \frac{A_H^o}{1+Y_L Z_{oH}} \qquad (3.162)$$

where $A_H^o$ is given by (3.157), $Z_{oH}$ by (3.161') and $Z_L$ is typically a parallel combination between $R_L$ and $C_L$. After replacing $Y_L$ and $Z_{oH}$ with their respective analytical expressions, the denominator of (3.162) can be written as:

$$1+Y_L Z_{oH} = 1+ \frac{R_{oH}}{R_L} + s(C_L R_{oH} + \frac{L_{oH}}{R_L}) + s^2 C_L L_{oH} \qquad (3.163)$$

(3.163) represents the typical description of a resonant circuit. The absolute value of (3.163) will reach a minimum at:

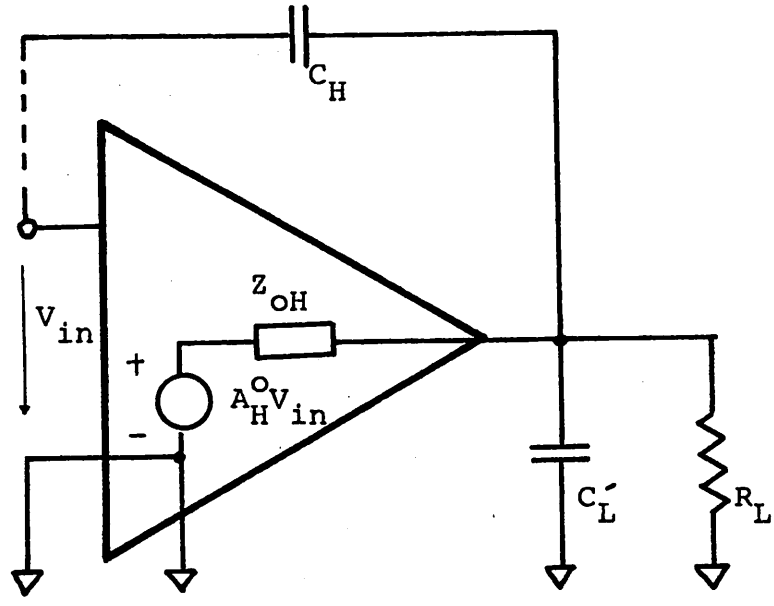
$$\omega_r^2 = \omega_a^2 \left[ 1 + \frac{R_{oH}}{R_L} - \frac{\omega_a^2}{\omega_b^2} \right] \qquad (3.164)$$

where:

$$\omega_a = \frac{1}{\sqrt{L_{oH} C_L}} = \sqrt{\omega_{TQ} \frac{gm_{6H}}{C_L}}$$

and:

$$\frac{1}{\omega_b} = C_L R_{oH} + \frac{L_{oH}}{R_L} = \frac{\frac{1}{R_L C_L} + \frac{\omega_{TQ}}{\beta}(1+ \frac{gm_{6H}}{g_Q})}{\omega_{TQ} \frac{gm_{6H}}{C_L}}$$




$$C_L' = C_L + C_{jH}$$

Equivalent circuit used for the stability analysis of the hold mode.

Figure 3.55

The minimum absolute value of (3.163), occuring at $\omega_r$, is:

$$\left|1+Y_L Z_{oH}\right|_{min} = \frac{\omega_a}{\omega_b}\sqrt{1+\frac{R_{oH}}{R_L}} \qquad (3.165)$$

and the corresponding phase shift is given by:

$$tg\left[\arg(1+Y_L Z_{oH})\right] = \frac{\omega_b}{\omega_a}\sqrt{1+\frac{R_{oH}}{R_L}-\frac{\omega_a^2}{\omega_b^2}} \qquad (3.166)$$

The ratio:

$$\frac{R_{oH}}{R_L} = \frac{1}{gm_{6H}R_L} + \frac{1}{gm_Q R_L}$$

is normally much smaller than 1. If the circuit is designed such that $\omega_a \ll \omega_b$ then:

$$\omega_r \cong \omega_a \qquad (3.164')$$

$$\left|1+Y_L Z_{oH}\right|_{min} \cong \frac{\omega_a}{\omega_b} \qquad (3.165')$$

and:

$$tg\left[\arg(1+Y_L Z_{oH})\right] \cong \frac{\omega_b}{\omega_a} \qquad (3.166')$$

and if $\omega_r$ occurs near the desired unity gain crossover frequency (which is the unity gain crossover frequency of $A_H^o$) then the overshoot and phase shift generated by (3.163) can make the hold configuration unstable.

The stability of the complete S/H configuration will be evaluated with reference to Figure 3.56. The equations for the open loop, open circuit voltage gain are:

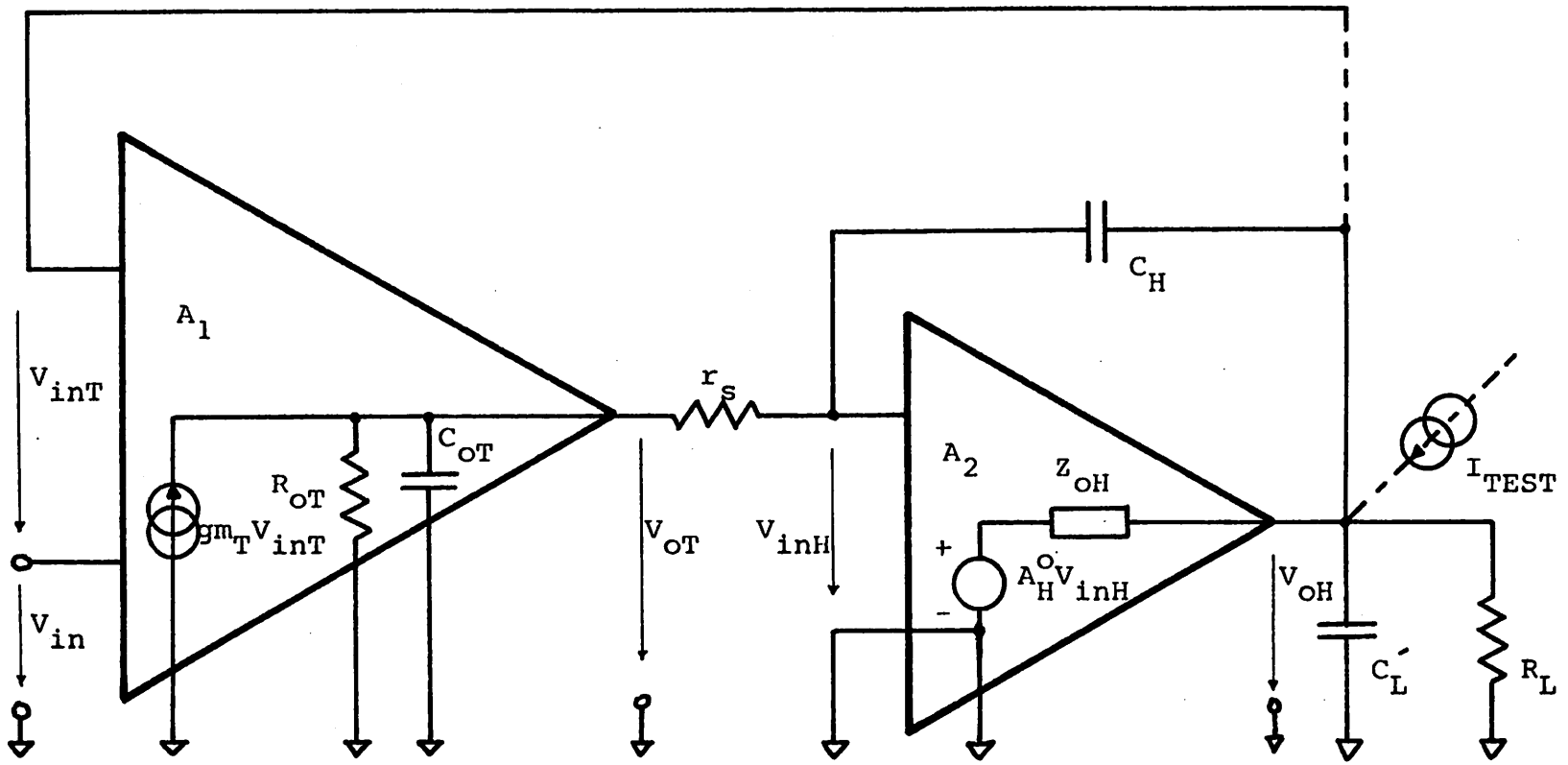



Figure 3.56

Equivalent circuit used for the stability analysis of the sampling mode.

$$gm_T V_{inT} = (C_{oT}+sC_{oT})V_{oT} + g_s(V_{oT}-V_{inH})$$

$$g_s(V_{oT}-V_{inH}) = sC_H(V_{inH}-V_{oH})$$

$$sC_H(V_{inH}-V_{oH}) = V_{oH}(V_{oH} + A_H^o\ V_{inH})$$

Solving for $V_{oH}$ and with $R_{oT} \gg r_s$ and $C_H \gg C_{oT}$, we find:

$$A_{SH}^o = \frac{V_{oH}}{V_{inT}} = -\frac{gm_T}{sC_H} \times \frac{A_H^o - sC_H Z_{oH}}{sC_{oT}Z_{oH} + (1+sC_{oT}r_s)(1+A_H^o)} \qquad (3.167)$$

From a stability point of view it would be desirable to have:

$$A_{SH}^o \cong -\frac{gm_T}{sC_H} \qquad (3.167')$$

The "perturbing" terms in (3.167) can be evaluated as follows:

$$sC_{oT}Z_{oH} = sC_{oT}R_{oH} + s^2C_{oT}L_{oH} = \frac{s}{\omega_x} + \frac{s^2}{\omega_y^2}$$

where:

$$\frac{1}{\omega_x} = \frac{1}{\beta\frac{gm_{6H}}{C_{oT}}} + \frac{1}{\frac{gm_Q}{C_{oT}}} \quad \text{and} \quad \omega_y = \sqrt{\omega_{TQ}\frac{gm_{6H}}{C_{oT}}}$$

$$sC_H Z_{oH} = sC_H R_{oH} + s^2 C_H L_{oH} = \frac{s}{\omega_p} + \frac{s^2}{\omega_q^2}$$

where:

$$\frac{1}{\omega_p} = \frac{1}{\beta\frac{gm_{6H}}{C_H}} + \frac{1}{\frac{gm_Q}{C_H}} \quad \text{and} \quad \omega_q = \sqrt{\omega_{TQ}\frac{gm_{6H}}{C_H}}$$

The frequencies $\omega_x$, $\omega_y$, $\omega_p$ are normally much larger than the desired unity gain crossover frequency of $A_H^o$ ( which is $gm_{1H}/C_c$); therefore the respective terms can be safely neglected. The pole generated by $C_{oT}$ and $r_s$ can easily be

placed far beyond $gm_{1H}/C_c$. The frequency $\omega_q$ should be placed reasonably far beyond $gm_T/C_H$ at least. In the presence of this perturbation and beyond the dominant pole of $A_H^o$, $A_{SH}^o$ can be expressed as:

$$A_{SH}^o = -\frac{gm_T}{sC_H} \times \frac{1 - \dfrac{s^3}{\omega_{TQ}\dfrac{gm_{6H}}{C_H}\dfrac{gm_{1H}}{C_c}}}{1 + sC_c/gm_{1H}} \qquad (3.167'')$$

and one can see that the action of the numerator singularity is similar to that of a true zero. It is also apparent that the bandwidth of the open loop, open circuit hold amplifier becomes the second pole of $A_{SH}^o$. If the numerator singularity occurs beyond $gm_{1H}/C_c$ then the open loop, open circuit gain of the complete sample and hold amplifier can be conveniently expressed as:

$$A_{SH}^o = -\frac{gm_T}{sC_H} \times \frac{A_H^o}{1+A_H^o} \qquad (3.168)$$

The output impedance of the complete S/H amplifier is found using again Figure 3.56 with $V_{inT} = 0$. Thus:

$$(G_{oT}+sC_{oT})V_{oT} + g_s(V_{oT}-V_{inH}) = 0$$

$$g_s(V_{oT}-V_{inH}) = sC_H(V_{inH}-V_{oH})$$

$$sC_H(V_{oH}-V_{inH}) + Y_{oH}(V_{oH}+A_H^oV_{inH}) = I_{TEST}$$

Solving for $V_{oH}$ and observing again that $R_{oT} \gg r_s$ and $C_H \gg C_{oT}$, we find:

$$Z_{oSH} = \frac{Z_{oH}}{1 + A_H^o + sC_{oT}R_{oH} + s^2C_{oT}L_{oH}} \qquad (3.169)$$

It has been already shown that the coupling between $C_{oT}$ and $Z_{oH}$ causes no trouble within the bandwith of either $A_H^o$ or $A_{SH}^o$ ; therefore the output impedance can be expressed as:

$$Z_{oSH} \cong \frac{Z_{oH}}{1 + A_H^o} \qquad (3.169')$$

The open loop gain of the complete S/H amplifier in the presence of the load can now be easily evaluated as:

$$A_{SH}^L = A_{SH}^o \frac{Z_L}{Z_L + Z_{oSH}} = \frac{A_{SH}^o}{1 + Y_L Z_{oSH}} \qquad (3.170)$$

Using (3.168) for $A_{SH}^o$ and (3.169') for $Z_{oSH}$, we find:

$$A_{SH}^L = - \frac{gm_T}{sC_H} \times \frac{A_H^o}{A_H^o + (1+Y_L Z_{oH})} \qquad (3.170')$$

This time the troublesome term $1+Y_L Z_{oH}$ is added to $A_H^o$; therefore if $\omega_r$ of (3.164') occurs beyond the unity gain crossover frequency of $A_H^o$ then $A_{SH}^L$ can be safely approximated as:

$$A_{SH}^L \cong - \frac{gm_T}{sC_H} \qquad (3.170'')$$

If this is the case then the S/H configuration will be stable. An intersting conclusion of this analysis is the fact that the complete sample and hold configuration seems to be more stable than the hold amplifier alone. The necessary modifications needed to improve or eaven assure stability will be analized after the presentation of the actual original design.

### 3.4.5 Device sizing.

The devices should be sized such as to yield the desired speed and stable operation. The sample and hold amplifier was designed for maximum speed within the limits of the chosen circuit configuration.

The slew rate of the S/H amplifier is given by:

$$\frac{dV}{dt} = \frac{I_{5T}}{C_H} \qquad (3.171)$$

where $I_{5T}$ is the tail current of the transconductance amplifier input stage. The bandwidth of the S/H amplifier is found from (3.170´´):

$$\omega_{BWSH} = \frac{gm_T}{C_H} \qquad (3.172)$$

Thus:

$$\frac{dV}{dt} = \frac{I_{5T}\omega_{BWSH}}{gm_T} = \omega_{BWSH}VGS_{eff1T} \qquad (3.173)$$

where $VGS_{eff1T}$ is the effective gate drive of M1T. This last expression does in fact set the limit that can be reached with this type of circuit configuration. Considering the value of the power supplies, the threshold voltages and the device "stacking", it turns out that $VGS_{eff1T}$ is equal to about 1.5V.

For stability reasons (mentioned earlier) the bandwidth of the complete S/H amplifier, $\omega_{BWSH}$, has to be smaller than the bandwidth of the hold amplifier, $\omega_{BWH}$. It has been shown in a previous section that the practical bandwidth of a CMOS buffer amplifier can reach about 5MHz. Applying a comfortable safety factor one can set the bandwidth of the S/H amplifier

at about 1.5MHz. Thus:

$$\frac{dV}{dt} \cong 9.5V/\mu s$$

With a practical compensation capacitor value of 10pF and $gm_{1H} \cong 150\%\ gm_{1T}$, we find:

$$C_H \cong C_c \frac{gm_{1H}}{gm_{1T}} = 25pF$$

With $C_H$ = 25pF and dV/dt = 9.5V/μs, it follows that $I_{5T}$ = 240μA. As a result of the current scaling in the transconductance amplifier, all the devices can be sized once $I_{5T}$ is known. The final choices are presented in TABLE 3.16.

The input stage of the hold amplifier is scaled with the input stage of the transconductance amplifier, so that the bandwidth relation, $\omega_{BWH} \cong 3.3\ \omega_{BWSH}$, is built in. At the time of the original design the stability analysis had been performed in a simplified manner which yielded no strong design condition for the second stage of the basic amplifier, M6H and M8H; therefore the dc current of this stage was more or less arbitrarily set equal to the current flowing through the input stage drivers. The compensation capacitor buffer, M9H and M10H, was sized such as to carry the same current as M5H; this is done in order not to limit the slew rate of the hold amplifier and it also places the true zero mentioned earlier beyond the bandwidth of the hold amplifier.

The output stage, containing a substrate npn structure, was sized to carry a current of about 5mA, which (at the time of the original design) was felt to be necessary. The follower stage, containing M7H and M12H, coupled with the bipolar transistor

yields the low output resistance, which would otherwise be $R_6/\beta$ .

The final device sizes are presented in TABLE 3.20.

3.4.6 Computer evaluation.

The original design was evaluated using ISPICE and was based on the circuit description shown in TABLE 3.16 and 3.20. A minum size switch, with built in feedthrough cancellation, was used to connect the two amplifiers.

The result of the dc operating point analysis is shown in TABLE 3.17 and respectively 3.21. The corresponding small-signal parameters are listed in TABLE 3.18 and 3.19 and respectively 3.22 and 3.23.

The transconductance amplifier performance is described by the magnitude/phase plots shown in Figure 3.57 and 3.58; these computer results are in very good agreement with the simplified analysis presented earlier. The "early" phase shift of the transadmitance is a result of the relatively reduced $\omega_T$ and this in turn is the result of the somewhat exagerated channel length chosen for the transistors. The longer channel length was chosen at the time of the original design in order to avoid breakdown problems. As it turned out, such precautions are not justified so that the performance of the transconductance amplifier could be further improved by reducing the channel length, hence the area, and by increasing in this way the bandwidth. An interesting conclusion of this analysis is the fact that the current mirror stage in a CMOS amplifier should be built, if possible, using n-channel transistors since they normally yield larger $\omega_T$. This was

```
TRANSCO
NODES(9.10,1.2,11)
M1 4 1 3 9 PSGX(10.5,6,7.5MI) 7.5MI,.4MI
M2 5 2 3 9 PSGX(10.5,6,7.5MI) 7.5MI,.4MI
M11 8 8 12 9 PSGX(6,6,7.5MI) 7.5MI,.4MI
M12 11 8 13 9 PSGX(6,6,7.5MI) 7.5MI,.4MI
M11A 12 12 9 9 PSGX(1.8,1.8,4.5MI) 4.5MI,.6MI
M12A 13 12 9 9 PSGX(1.8,1.8,4.5MI) 4.5MI,.6MI
M3 4 6 10 10 NSGX(3.84,3.84,4.8MI) 4.8MI,.32MI
M4 5 6 10 10 NSGX(3.84,3.84,4.8MI) 4.8MI,.32MI
M9 8 0 4 4 NSGX(1.92,1.92,2.4MI) 2.4MI,.32MI
M10 11 0 5 5 NSGX(1.92,1.92,2.4MI) 2.4MI,.32MI
M5 3 7 9 9 PSGX(3.6,3.6,9.0MI) 9.0MI,.6MI
M6 6 7 9 9 PSGX(4.65,4.65,1.5MI) 1.5MI,.6MI
M7 6 6 10 10 NSGX(.64,.64,.8MI) .8MI,.32MI
MP1 7 7 9 9 PSGX(1.08,1.08,1.5MI) 1.5MI,.3MI
MP2 0 0 7 9 PSGX(1.08,1.08,1.2MI) 1.2MI,.4MI
D4 4 9 D
D5 5 9 D
MODEL D D(CJO=2.12P)
```

Circuit description of CMOS transconductance amplifier.

TABLE 3.16

| | VGS (V) | VDS (V) | ID (μA) |
|---|---|---|---|
| M1 | -3.16 | - 6.21 | 113.6 |
| M2 | -3.16 | - 6.22 | 113.5 |
| M11 | -3.27 | - 3.27 | 150.0 |
| M12 | -3.26 | - 3.96 | 150.0 |
| M11A | -3.53 | - 3.53 | 150.0 |
| M12A | -3.53 | - 3.54 | 150.0 |
| M3 | 2.95 | 4.45 | 263.6 |
| M4 | 2.95 | 4.44 | 263.6 |
| M9 | 3.05 | 3.75 | 150.0 |
| M10 | 3.06 | 3.06 | 150.1 |
| M5 | -3.24 | - 4.34 | 227.1 |
| M6 | -3.24 | -12.05 | 43.2 |
| M7 | 2.95 | 2.95 | 43.2 |
| MP1 | -3.24 | - 3.24 | 78.7 |
| MP2 | -4.26 | - 4.26 | 78.7 |

Dc biasing conditions for transconductance amplifier.

TABLE 3.17

| | gm (mA/V) | gds (μA/V) | Cgs (pF) | Cgd (pF) |
|---|---|---|---|---|
| M1 | .22 | 2.3 | .68 | .17 |
| M2 | .22 | 2.3 | .68 | .17 |
| M11 | .24 | 3.6 | .68 | .17 |
| M12 | .24 | 3.5 | .68 | .17 |
| M11A | .14 | 3.9 | .56 | .10 |
| M12A | .14 | 3.9 | .56 | .10 |
| M3 | .36 | 2.7 | .51 | .24 |
| M4 | .36 | 2.7 | .51 | .24 |
| M9 | .19 | 1.7 | .26 | .12 |
| M10 | .19 | 1.9 | .26 | .12 |
| M5 | .25 | 5.1 | 1.13 | .20 |
| M6 | .05 | 61.7 | .19 | .03 |
| M7 | .06 | 54.2 | .09 | .04 |
| MP1 | .08 | 4.4 | .11 | .03 |
| MP2 | .07 | 2.0 | .11 | .03 |

Small - signal parameters of transconductance amplifier.

TABLE 3.18

| | At $V_{rev}$ (pF) | At $V_{rev}=0$ (pF) | $V_{rev}$ (V) |
|---|---|---|---|
| $Cjd_1$ | .17 | .69 | 10.55 |
| $Cjs_1$ | .15 | .40 | 4.34 |
| $Cjd_2$ | .17 | .69 | 10.55 |
| $Cjs_2$ | .15 | .40 | 4.34 |
| $Cjd_{11}$ | .12 | .40 | 6.8 |
| $Cjs_{11}$ | .16 | .40 | 3.53 |
| $Cjd_{12}$ | .12 | .40 | 7.5 |
| $Cjs_{12}$ | .16 | .40 | 3.54 |
| $Cjd_{11A}$ | .05 | .12 | 3.53 |
| $Cjd_{12A}$ | .05 | .12 | 3.54 |
| $Cjd_3$ | .25 | .67 | 4.45 |
| $Cjd_4$ | .25 | .66 | 4.44 |
| $Cjd_9$ | .13 | .33 | 3.75 |
| $Cjd_{10}$ | .14 | .33 | 3.06 |
| $Cjd_5$ | .09 | .24 | 4.34 |
| $Cjd_6$ | .07 | .31 | 12.05 |
| $Cjd_7$ | .05 | .11 | 2.95 |
| $Cjd_{P1}$ | .01 | .02 | 3.24 |
| $Cjs_{P2}$ | .01 | .02 | 3.24 |

<u>Junction capacitances in the transconductance amplifier.</u>

TABLE 3.19

```
CMOSOPA
NODES(9,10,1,2,13)
M1 4 1 3 9 PSGX(14.0,8.0,10.0MI) 10.0MI,.4MI
M2 5 2 3 9 PSGX(14.0,8.0,10.0MI) 10.0MI,.4MI
M3 4 4 10 10 NSGX(2.4,2.4,3.0MI) 3.0MI,.32MI
M4 5 4 10 10 NSGX(2.4,2.4,3.0MI) 3.0MI,.32MI
M5 3 12 9 9 PSGX(4.8,4.8,12.0MI) 12.0MI,.6MI
M6 6 5 10 10 NSGX(2.4,2.4,3.0MI) 3.0MI,.32MI
M8 6 12 9 9 PSGX(4.8,4.8,6.0MI) 6.0MI,.6MI
M9 10 6 8 9 PSGX(9.6,9.6,12.0MI) 12.0MI,.3MI
M10 8 12 9 9 PSGX(6.6,6.6,6.0MI) 6.0MI,.3MI
M7 10 6 7 9 PSGX(4.8,4.8,6.0MI) 6.0MI,.3MI
M12 7 12 9 9 PSGX(1.2,1.2,3.0MI) 3.0MI,.3MI
Q 9 7 13 ARB
M11 13 14 10 10 NSGX(7.68,7.68,9.6MI) 9.6MI,.12MI
M17 14 14 10 10 NSGX(.48,.48,.6MI) .6MI,.12MI
CCOMP 5 8 10P
D5 10 5 D
MODEL D D(CJO=7.79P)
M14 0 0 12 9 PSGX(1,1,1.2MI) 1.2MI,.4MI
M15 12 12 9 9 PSGX(1,1,1.5MI) 1.5MI,.3MI
M18 14 12 9 9 PSGX(3.2,3.2,4.0MI) 4.0MI,.3MI
```

Circuit description of CMOS hold amplifier.

TABLE 3.20

| | VGS (V) | VDS (V) | ID (μA) |
|---|---|---|---|
| M1 | -3.14 | -7.59 | 150.0 |
| M2 | -3.15 | -7.53 | 152.8 |
| M3 | 3.06 | 3.06 | 187.7 |
| M4 | 3.06 | 3.12 | 187.9 |
| M5 | -3.24 | -4.35 | 302.9 |
| M6 | 3.12 | 6.33 | 210.9 |
| M8 | -3.24 | -8.67 | 164.2 |
| M9 | -3.25 | -9.58 | 267.8 |
| M10 | -3.24 | -5.42 | 351.0 |
| M7 | -3.04 | -9.35 | 75.0 |
| M12 | -3.24 | -5.66 | 177.3 |
| M11 | 4.28 | 7.55 | 5014.0 |
| M17 | 4.28 | 4.28 | 290.6 |
| M14 | -4.26 | -4.26 | 78.7 |
| M15 | -3.24 | -3.24 | 78.7 |
| M18 | -3.24 | -10.72 | 290.6 |

<u>Dc biasing conditions in the hold amplifier.</u>

(the apparent current discrepancies are the result of the "fixing" resistors introduced in order to ensure dc convergence)

TABLE 3.21

| | gm (mA/V) | gds (μA/V) | Cgs (pF) | Cgd (pF) |
|---|---|---|---|---|
| M1 | .30 | 2.9 | .91 | .22 |
| M2 | .30 | 2.99 | .91 | .22 |
| M3 | .24 | 2.33 | .32 | .15 |
| M4 | .24 | 2.31 | .32 | .15 |
| M5 | .34 | 6.79 | 1.50 | .26 |
| M6 | .26 | 1.84 | .32 | .15 |
| M8 | .18 | 2.7 | .75 | .13 |
| M9 | .52 | 6.8 | .88 | .26 |
| M10 | .38 | 15.96 | .44 | .13 |
| M7 | .20 | 1.88 | .44 | .13 |
| M12 | .19 | 7.94 | .22 | .07 |
| M11 | 3.17 | 103.7 | .68 | .47 |
| M17 | .19 | 7.8 | .04 | .03 |
| M14 | .07 | 1.95 | .11 | .03 |
| M15 | .09 | 4.45 | .11 | .03 |
| M18 | .32 | 11.16 | .29 | .09 |

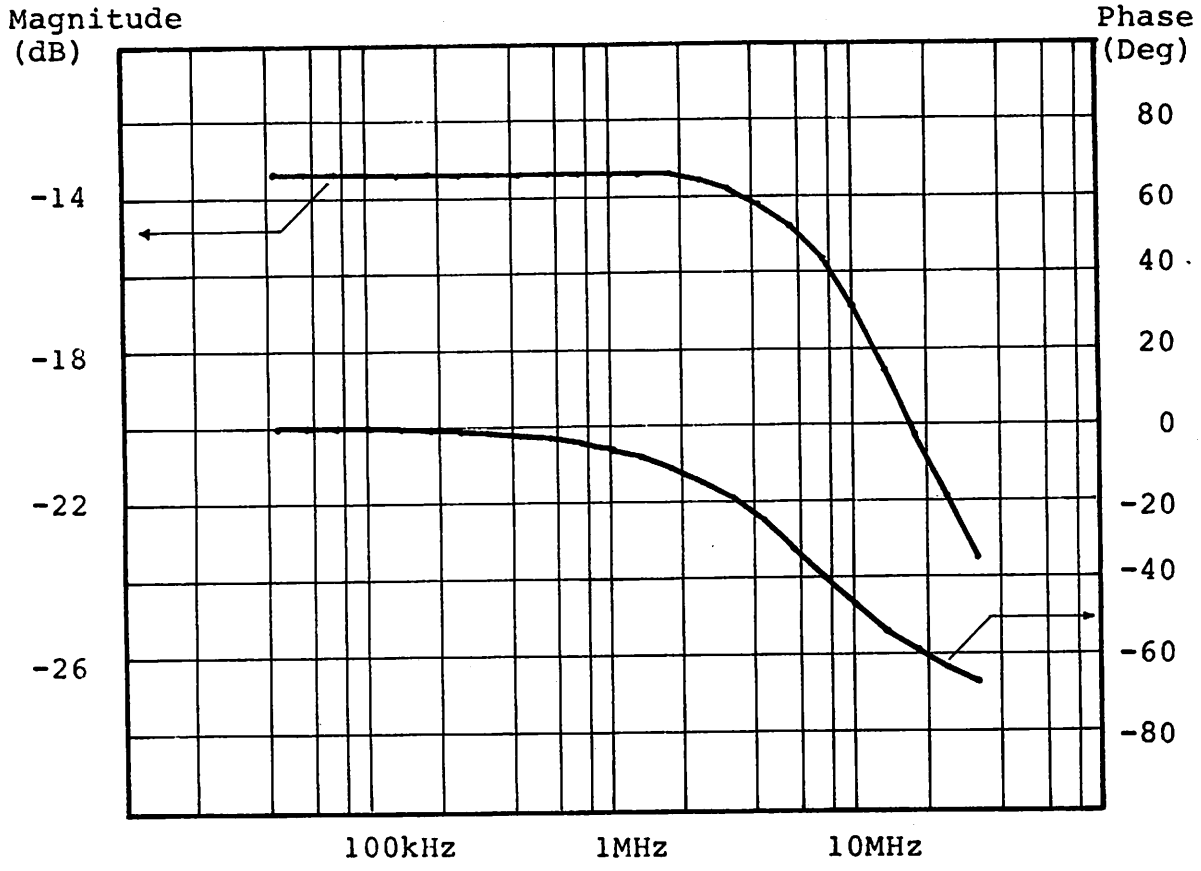
Small-signal parameters of the hold amplifier transistors.

TABLE 3.22

| | At $V_{rev}$ (pF) | At $V_{rev}=0$ (pF) | $V_{rev}$ (V) |
|---|---|---|---|
| $Cjd_1$ | .22 | .92 | 11.94 |
| $Cjs_1$ | .20 | .53 | 4.35 |
| $Cjd_2$ | .22 | .92 | 11.94 |
| $Cjs_2$ | .20 | .53 | 4.35 |
| $Cjd_3$ | .18 | .42 | 3.06 |
| $Cjd_4$ | .18 | .42 | 3.12 |
| $Cjd_5$ | .12 | .32 | 4.35 |
| $Cjd_6$ | .13 | .42 | 6.33 |
| $Cjd_8$ | .09 | .32 | 8.67 |
| $Cjs_9$ | .21 | .63 | 3.42 |
| $Cjd_{10}$ | .15 | .44 | 3.42 |
| $Cjs_7$ | .11 | .32 | 5.66 |
| $Cjd_{12}$ | .03 | .08 | 5.66 |
| $Cjd_{11}$ | .38 | 1.33 | 7.55 |
| $Cjd_{17}$ | .03 | .08 | 4.28 |
| $Cjd_{14}$ | .03 | .07 | 4.26 |
| $Cjs_{15}$ | .03 | .07 | 4.26 |
| $Cjd_{18}$ | .05 | .21 | 10.72 |

Junction capacitances in the hold amplifier.

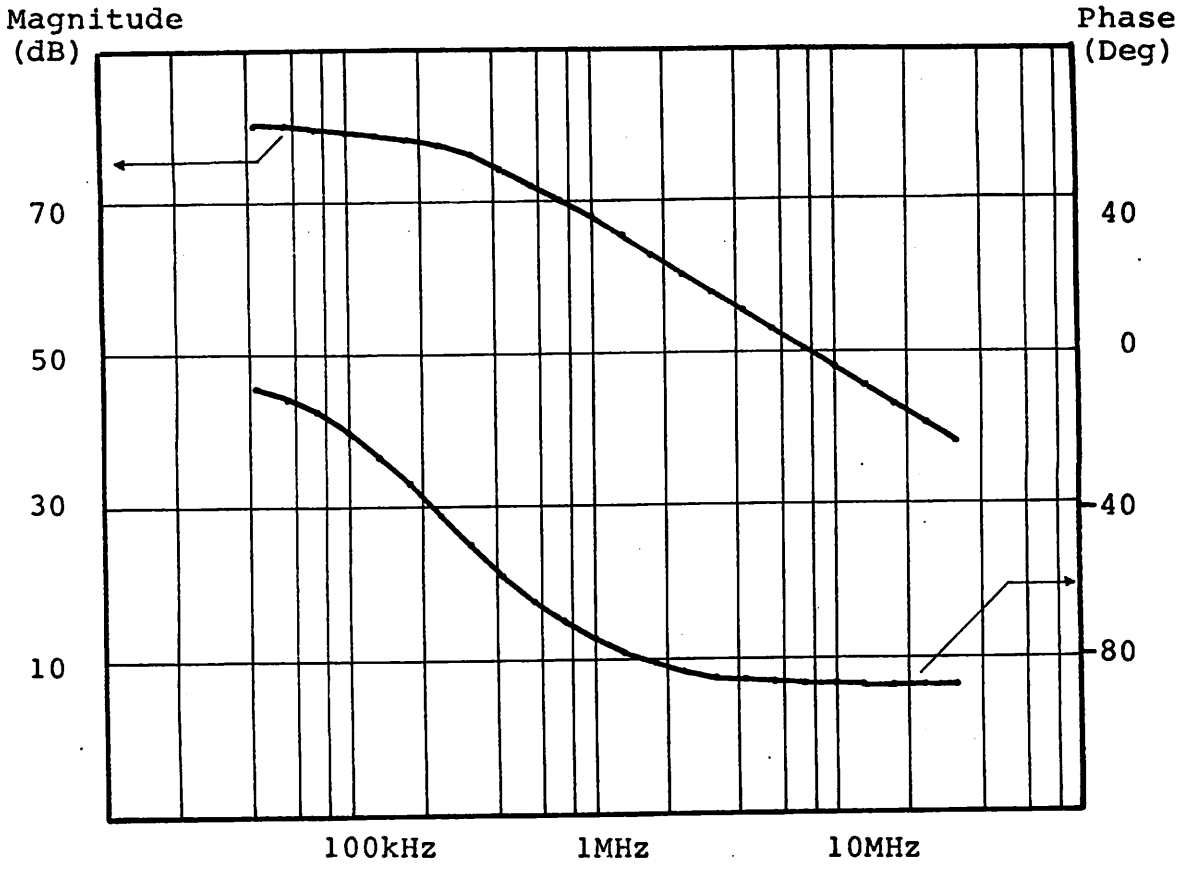
TABLE 3.23




Magnitude/phase characteristics of the transconductance amplifier transadmitance.

( 0dB corresponds to 1mA/V)

Figure 3.57




Magnitude/phase characteristics of the transconductance amplifier output impedance.

( 0dB corresponds to a 1k resistor)

Figure 3.58

not done in the case of the transconductance amplifier because the input stage was built such as to be "intrinsically" scaled with the input stage of the hold amplifier. Obviously in a process with reasonable control of the threshold ratio between n-type and p-type transistors such an arguement does not apply as strictly and the transconductance amplifier could be further broadbanded by reversing the polarity of the devices.

The frequency as well as time analysis of the hold amplifier alone and of the complete S/H configuration was unfortunately altered by choosing an arbitrary model for the description of the bipolar transitor. This model incorporated an excessively large $\omega_{TQ}$ so that the effects mentioned during the previous stability analysis where unobservable. As a result the computer analysis predicted satisfactory performance and the circuit was implemented according to the descriptions presented in the tables.

3.4.7 Critique of the original S/H amplifier design.

As mentioned earlier, the bipolar transistor was originally taken for granted by arbitrarily choosing a model description available in the ISPICE library. This was certainly a bad choice since the transistor was implemented using the substrate npn structure "naturally" available in a CMOS process. Such a transistor is built with the $n^-$ substrate acting as collector, the $p^-$ well (used for the implementation of the n-channel transistors) acting as base and the $n^+$ drain and source diffusion acting as emitter. The resulting practical base width is of about 7μm. Using the most simple model for

the derivation of $f_{TQ}$ (14), we find:

$$f_{TQ} = \frac{2D_{nB}}{2\pi w^2} = \frac{2x20cm^2/s}{2\pi (7\mu m)^2} = 13MHz$$

and with the clear advantage of hindsight we recognize that this frequency is dangerously close to the desired bandwidth of the hold amplifier. In fact the cutoff frequency of the bipolar transistor is even smaller than that of its MOS counterpart. As a result of this relatively low $f_{TQ}$, the resonance frequency, $\omega_r$ of (3.164') can possibly fall within the desired bandwidth of the hold amplifier. Thus, in the presence of the typical load, $R_L$=10k, $C_L$=50pF and with $gm_{6H}$=.26mA/V, we find:

$$f_r = \frac{1}{2\pi}\sqrt{\omega_{TQ}\frac{gm_{6H}}{C_L}} = \sqrt{(13MHz)(.8MHz)} \cong 3.22MHz$$

which is obviously undesirable. It also turns out that the choice of $gm_{6H}$ can no longer be arbitrary, although it is also apparent that the practical possibilities of increasing $gm_{6H}$ are limited.

The effect of $f_{TQ}$ will be analized next numerically by considering a possible value of $f_{TQ}$ = 10MHz. The overshoot and phase shift caused by the resonance effect mentioned earlier can be computed as follows, with:

$$f_{TQ} = 10MHz,\ R_L=10k,\ C_L=50pF,\ \beta=100,\ gm_Q = \frac{5mA}{25mV} = 200mA/V,$$

$$g_Q = 2mA/V,\ gm_{6H} = .26mA/V$$

$$f_a = 2.83MHz,\ f_b = 18.57MHz,\ f_r \cong f_a = 2.83MHz$$

$$\left|1+Y_L Z_{oH}\right|_{min} = .152 \quad \text{and} \quad tg\left[\arg(1+Y_L Z_{oH})\right] = 6.56$$

The corresponding overshoot is of about 16dB and the phase shift of $81^{\circ}$. Such contributions near the bandwidth of the amplifier can obviously be very unpleasant.

The stability analysis as presented earlier was performed relatively late. In the mean time the decoder chip had been built according to the original design and as it turned out the sample and hold amplifier did oscillate in the presence of heavier capacitive loads. The oscillation was most aptly eliminated ( 18 ) so that the reason of the present critique is to explain why the circuit does perform adequately in the present configuration and how it can be further improved.

After the discovery of the resonance effect, the hold amplifier was again subject to computer analysis, but this time a more appropriate model was used for the substrate npn transistor. The analysis was performed only in the frequency domain by replacing the MOS devices with their equivalent small-signal circuits available from the ISPICE analysis. This was done because the author had no access to ISPICE or to a comparably powerful computer program. The analysis was performed using ANDREI (22) a computer program similar to SPICE 1 (23) and implemented on a VARIAN 73 minicomputer.

The bipolar transistor was described with:

$$f_{TQ} = 10\text{MHz},\ gm_Q = (I_C/V_T) = (5\text{mA}/25\text{mV}) = 200\text{mA/V}$$

$$\beta = 100,\ g_Q = (gm_Q/\beta) = 2\text{mA/V},\ C_Q = (gm_Q/\omega_{TQ}) = 3\text{nF}$$

This description is more realistic than the original one but still somewhat idealized since it does not take into

account second order effects, such as the dependence of $f_{TQ}$ on $I_c$.

The open loop gain of the unloaded hold amplifier is shown in Figure 3.59. During this simulation the amplifier is in fact loaded with the junction capacitance associated with the hold capacitor; at $V_{out} = 0$, the junction capacitance is of about 6pF, yielding:

$$f_r = 8.3\text{MHz},\ f_b = 23.7\text{MHz}\ (\text{with } R_L = R_{11})$$

$$\left|1+Y_L Z_{oH}\right|_{min} = .35,\quad tg\left[\arg(1+Y_L Z_{oH})\right] = 2.86$$

The corresponding overshoot is of about 9dB and the phase shift of $71^{\circ}$. The gain plot of Figure 3.59 doesn't seem to show these effects; the reason is that at 8.3MHz the output impedance of the hold amplifier, presented in Figure 3.60, isn't any longer strongly inductive so that the simplified model doesn't hold any longer. In the presence of the typical load $f_r$ moves to 3.22MHz, as shown earlier; this is sufficiently low in order to yield unfavorable coupling between the inductive output impedance and the capacitive load. The corresponding open loop gain is presented in Figure 3.61 and the amplifier would obviously be unstable if operated closed loop.

In principle one could try to move $f_r$ beyond the desired bandwidth by increasing $gm_{6H}$. But the necessary increase is quite unpractical. With $C_L = 50\text{pF}$ and $gm_{6H} = .26\text{mA/V}$ we find:

$$\frac{gm_{6H}}{2\pi C_L} = 827\text{kHz}$$

Placing $f_r$ sufficiently far beyond the unity gain crossover frequency would therefore require at least a ten fold increase of $gm_{6H}$. In any case, the limitation imposed by $f_{TQ}$ is practically unsurmountable.

A possible cure, implying no major reconstruction of the amplifier would be the damping of the resonant circuit by placing a resistor between the emitter of the npn and the load (including the hold capacitor connection). This is shown in Figure 3.62a. The penalty is obviously higher output resistance but as it turned out there seems to be no real need for a very low output resistance. The open loop gain in the presence of the load can now be written as:

$$A_H^L = \frac{A_H^o}{1 + Y_L(Z_{oH}+R_A)} \tag{3.174}$$

The denominator of (3.174) can be written as:

$$1+Y_L(Z_{oH}+R_A) = 1+(G_L+sC_L)(R_{oH}+sL_{oH}+R_A)$$

and with $R_A \gg R_{oH}$:

$$1+Y_L(Z_{oH}+R_A) = 1+\frac{R_A}{R_L} + s\left[\frac{L_{oH}}{R_L} + C_L R_A\right] + s^2 C_L L_{oH}$$

The resonance analysis can be repeated, yielding:

$$\omega_r^2 = \omega_a^2\left[1 + \frac{R_A}{R_L} - \frac{\omega_a^2}{\omega_b^2}\right]$$

$$\omega_a = \frac{1}{\sqrt{L_{oH}C_L}} = \sqrt{\omega_{TQ}\frac{gm_{6H}}{C_L}}$$

$$\frac{1}{\omega_b} = R_A C_L + \frac{1}{gm_{6H}R_L\omega_{TQ}}$$

In the presence of a heavier load:

$$\omega_b = \frac{1}{R_A C_L}$$

With $R_A$ = 1k, and $C_L'$ = 56pF, we find:

$f_a$ = 2.71MHz, $f_b$ = 2.84MHz, $f_r$ = 513kHz

Thus:

$$\left|1+Y_L(Z_{oH}+R_A)\right|_{min} = .95 \quad \text{and} \quad tg\left[\arg(1+Y_L(Z_{oH}+R_A))\right] = 1.05$$

The corresponding overshoot is only .45dB but the phase shift is still large, about $45^o$. The corresponding gain characteristics are shown in Figure 3.62b and it is apparent that the amplifier is still on the verge of oscillation.

A more drastic improvement can be obtained by isolating the load from the feedback tap point. This can be done by placing an additional resistor between the load and the junction of $R_A$ with $C_H$. In this case, illustrated in Figure 3.63a, the open loop gain can be expressed as:

$$A_H^L = A_H^o \frac{R_B+Z_L}{R_A+R_B+Z_L+Z_{oH}} = \frac{A_H^o\ (1+R_BY_L)}{1+(R_A+R_B)Y_L+Y_LZ_{oH}} \qquad (3.175)$$

The numerator of (3.175) can be written as:

$$1+R_BY_L = 1 + \frac{R_B}{R_L} + sR_BC_L \cong 1 + sR_BC_L$$

The denominator can be written as:

$$1+(R_A+R_B)Y_L + Y_LZ_{oH} = 1 + (R_A+R_B)/R_L + s(R_AC_L+R_BC_L+\frac{L_{oH}}{C_L})+ s^2L_{oH}C_L$$

Since it was possible to implement the condition $f_a = f_b$,

it should also be possible to implement $f_b < f_a$. Thus it turns out that resonance can be entirely eliminated by correspondingly sizing $R_A$ and $R_B$. The true zero introduced by the coupling of $R_B$ with $C_L$ is obviously also an important contributor toward stability. In fact the addition of $R_A$ transforms the resonance situation into a doublet type of situation with the associated relative benefits. The computer simulation corresponding to the case $R_A=R_B=1k$ is shown in Figure 3.63b and the amplifier is now clearly stable.

The obvious observation at this point of the analysis is that the very low output resistance offered by the npn transistor has been in fact rendered ineffective by adding series resistance to it. Thus it appears that the bipolar transitor is in fact useless, to say the least, in this application. Since it turns out that the typical load does not require low output resistance it appears that the npn transistor, together with the buffer follower M7H and M12H, could be very well eliminated. A reasonable output resitance could be obtained by implementing the output stage as an all n-channel MOS transistor follower. The buffering of the load through a series resistor could still be used in order to take advantage of the resulting true zero.

3.4.8 Experimental results.

As mentioned earlier, the original design had to be modified in order to obtain stable opeartion. Fortunately this could be done by simply rearranging some of the crossunders.

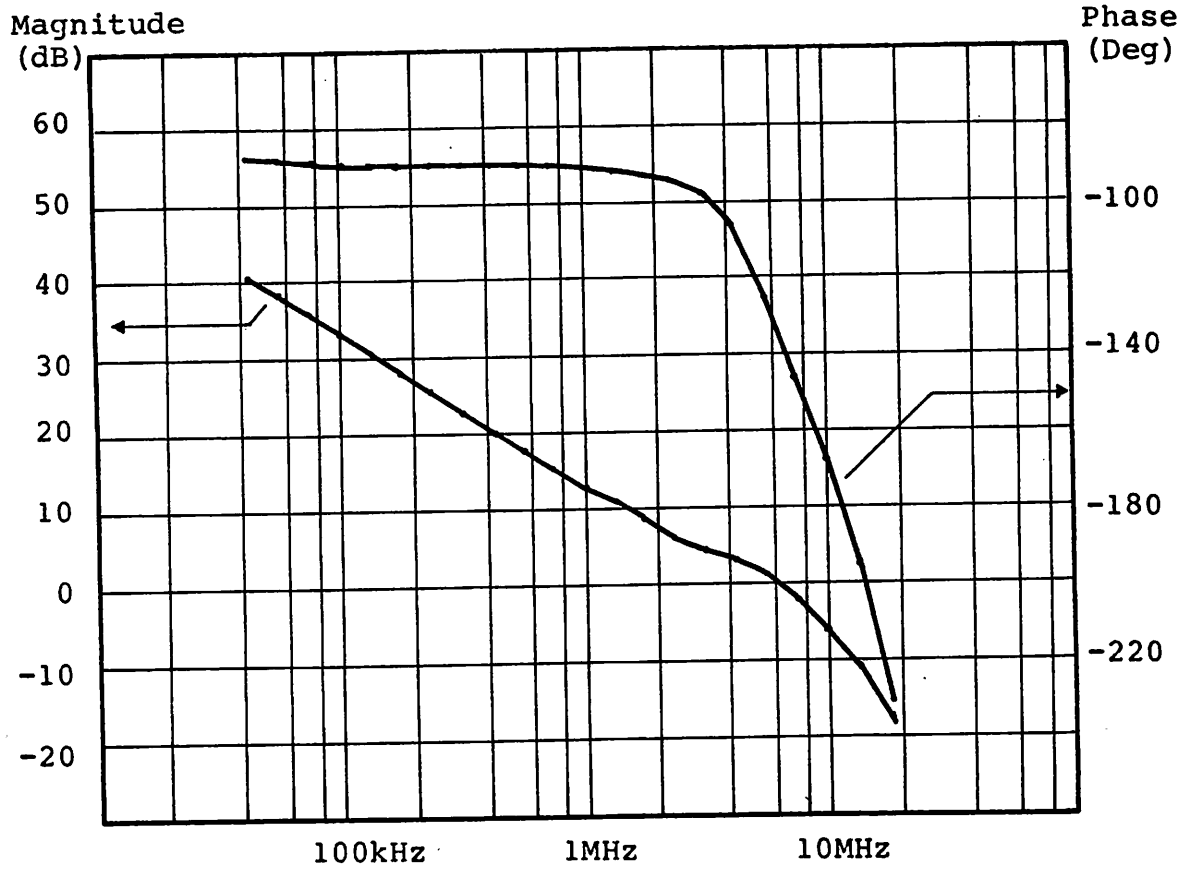
The "fixed" sample and hold amplifier did perform

adequately. The typical performance in the presence of a load consisting of $R_L$=10k and $C_L$=50pF is described by:

Acquisition time (1%, 3V step): less than 1μs

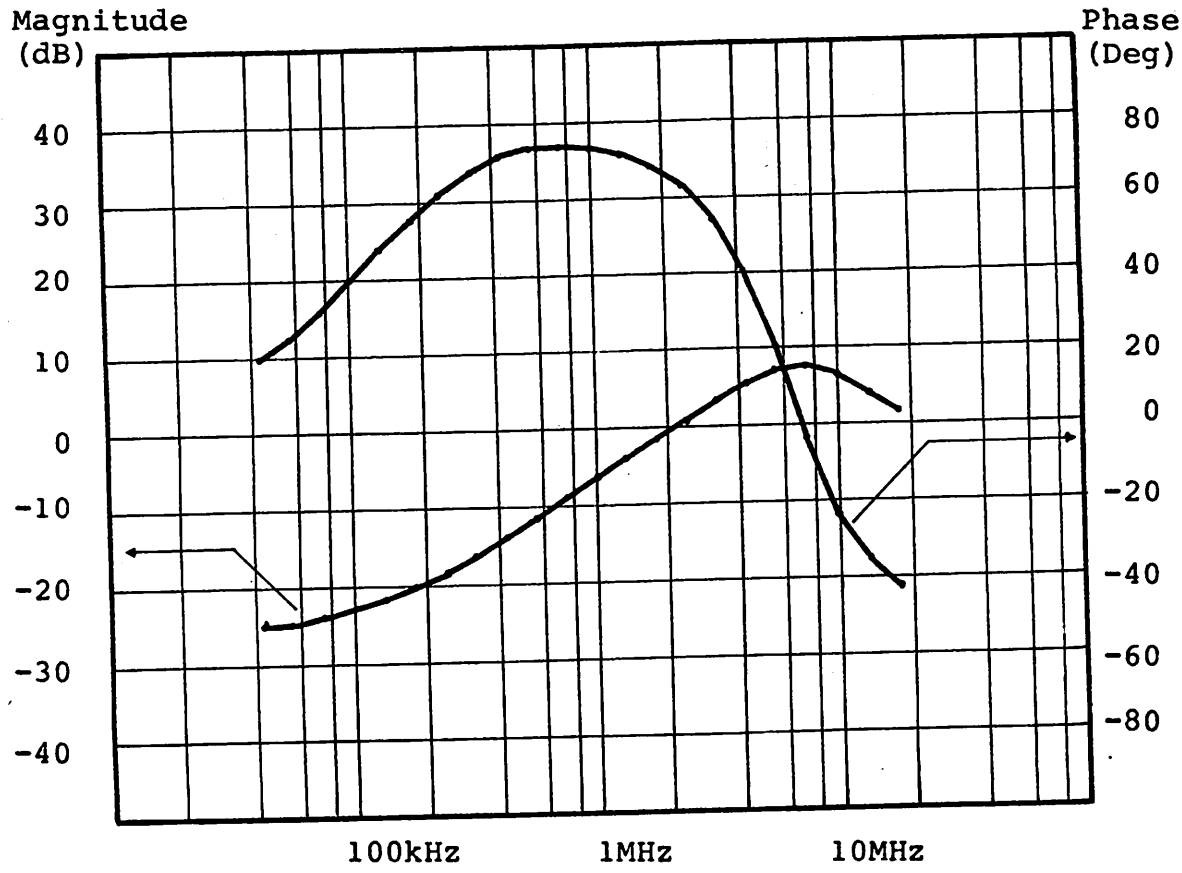
Droop rate: less than 50mV/s

and this is quite adequate for the present application.




Open loop, open circuit voltage gain of the hold amplifier ( in the presence of the junction capacitance associated with the hold capacitor).

Figure 3.59

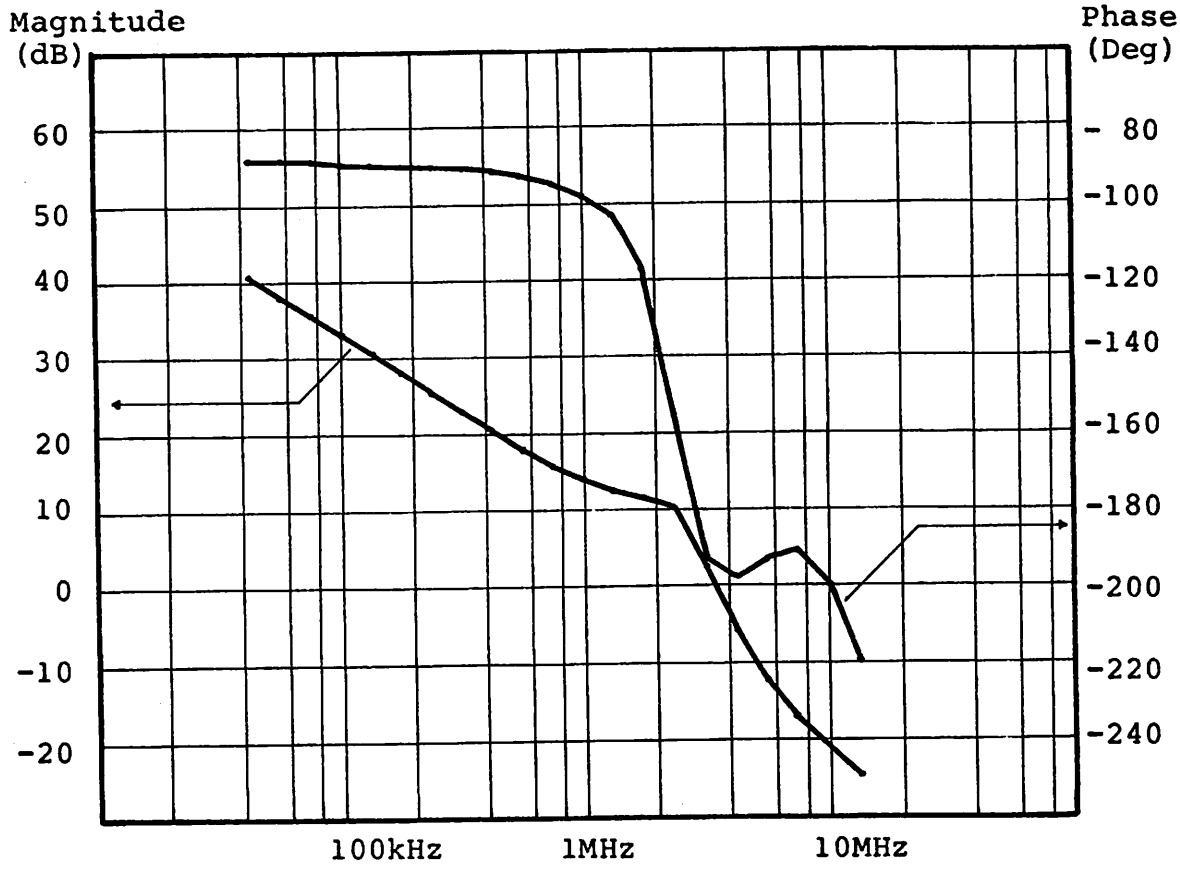



Hold amplifier output impedance characteristics.

( in the presence of the hold capacitor junction)

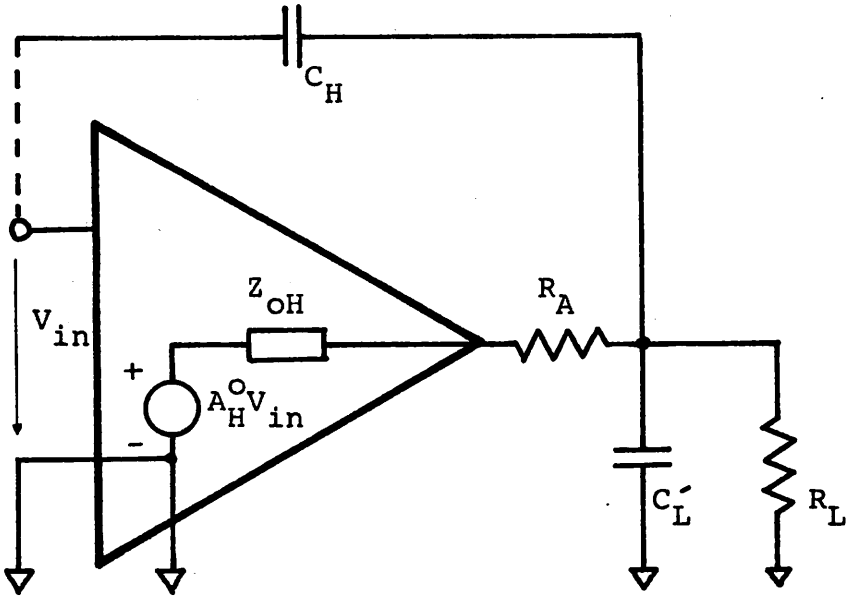
( 0dB corresponds to a 1k resistor)

Figure 3.60




Open loop gain of the hold amplifier with the load connected directly to the emitter of the substrate npn transistor ($C_L$=50pF, $R_L$=10k).

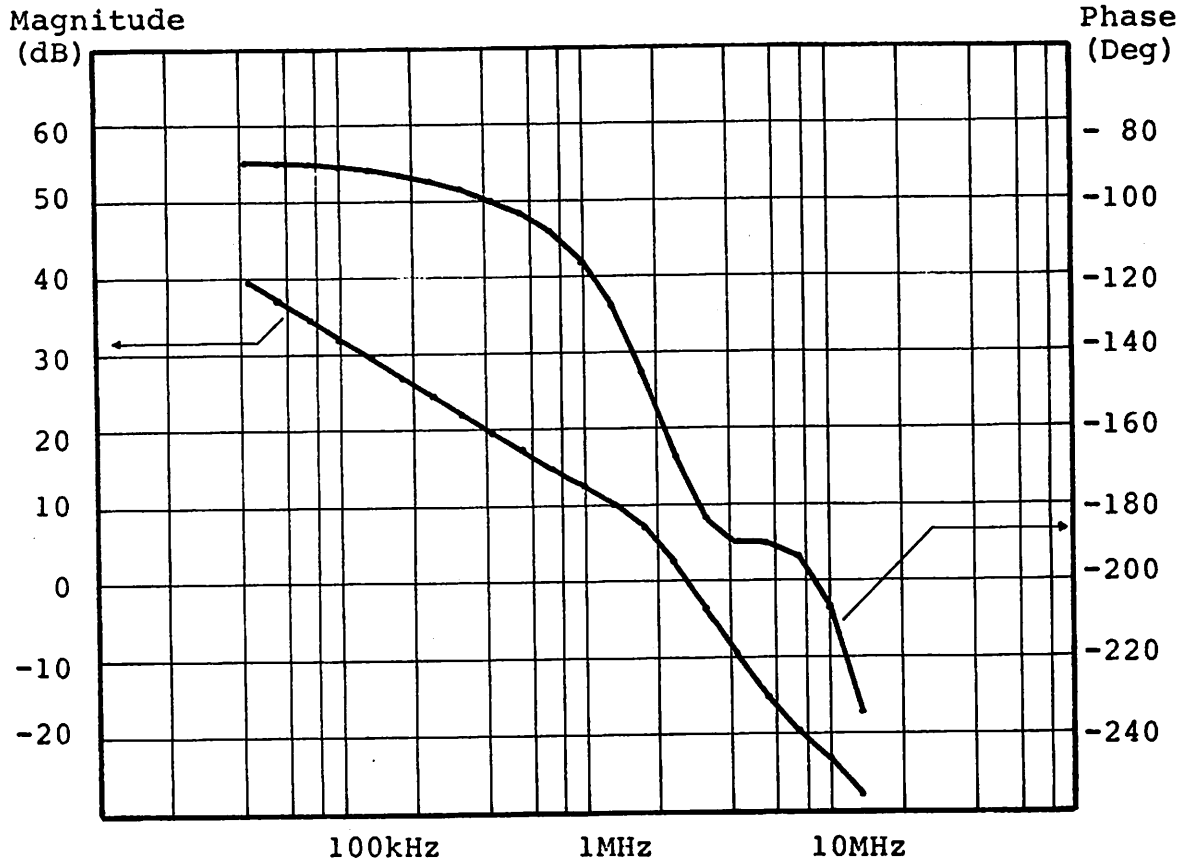
Figure 3.61




$C_L' = C_L + C_{jH}$

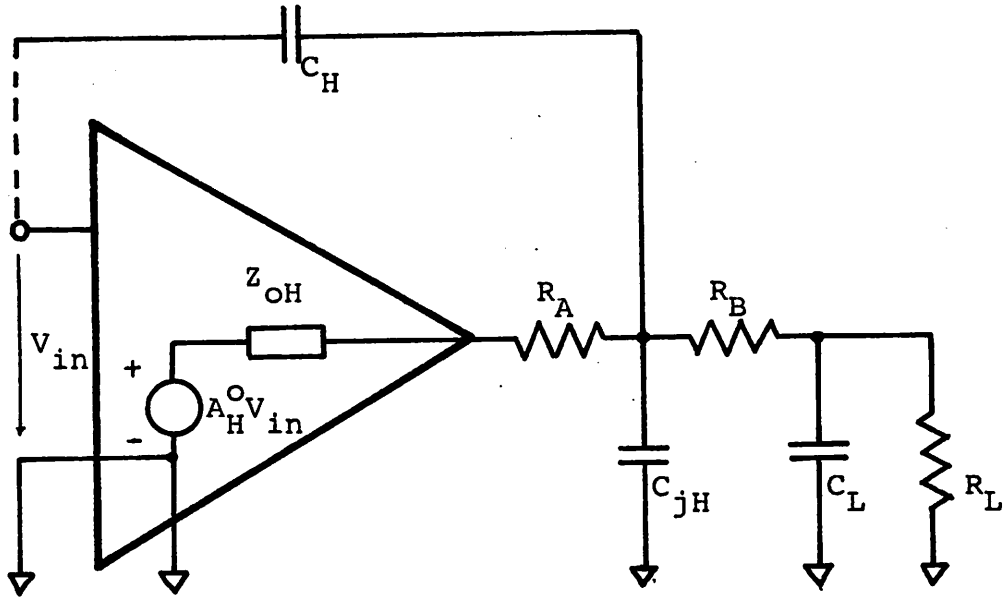
Equivalent circuit used for the stability analysis of the hold mode in the presence of simple buffering ($R_A$).

Figure 3.62a



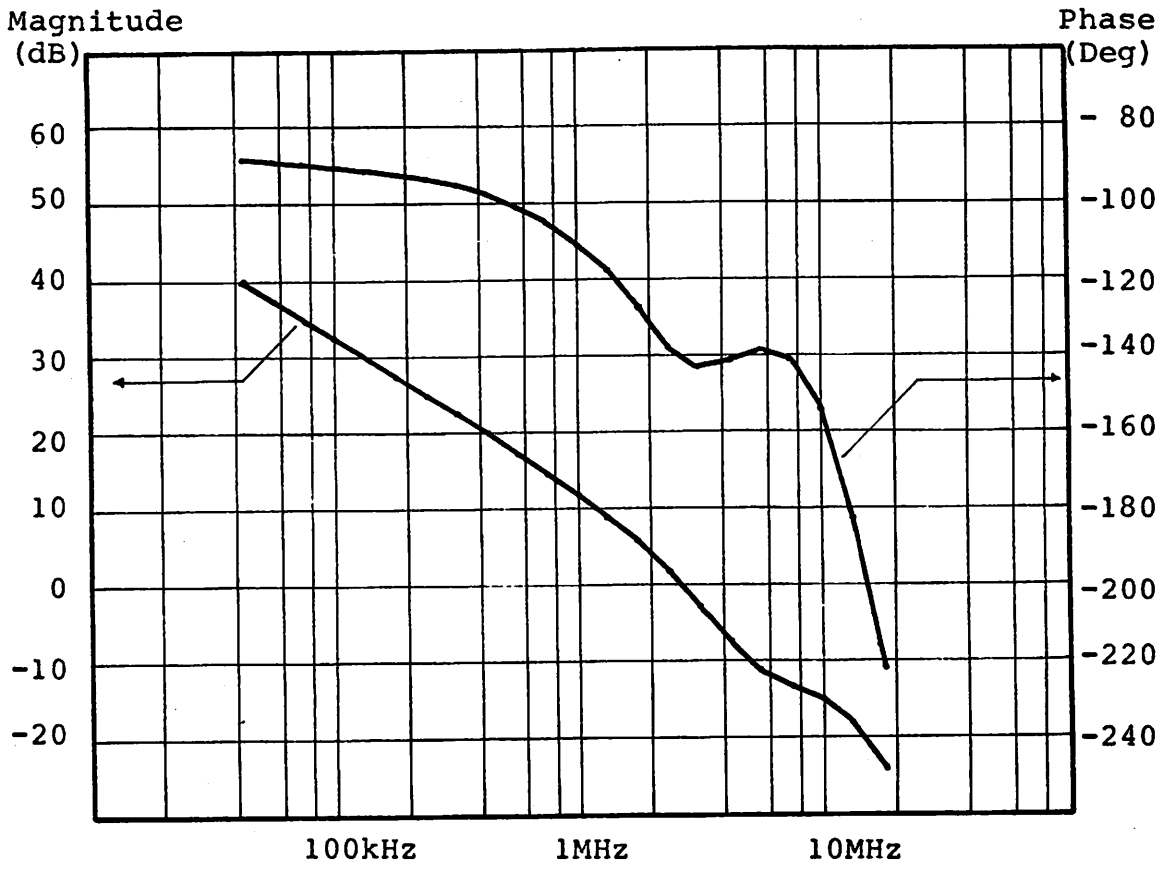

Open loop gain of the hold amplifier with the load and the hold capacitor buffered from the emitter through a 1k resistor ($C_L$=50pF, $R_L$=10k).

Figure 3.62b




Equivalent circuit used for the stability analysis of the hold mode in the presence of double buffering ($R_A$ and $R_B$).

Figure 3.63a




Open loop gain of the hold amplifier with the hold capacitor "tapping" the buffer resistor which connects the load to the emitter of the substrate npn transistor (the tap is taken at the middle of a 2k resistor with $C_L$=50pF, $R_L$=10k).

Figure 3.63b

# CHAPTER 4

## 4. EXPERIMENTAL RESULTS.

The ADC and DAC converters as described in the previous chapters were implemented at Siliconix Inc. using standard CMOS technology.

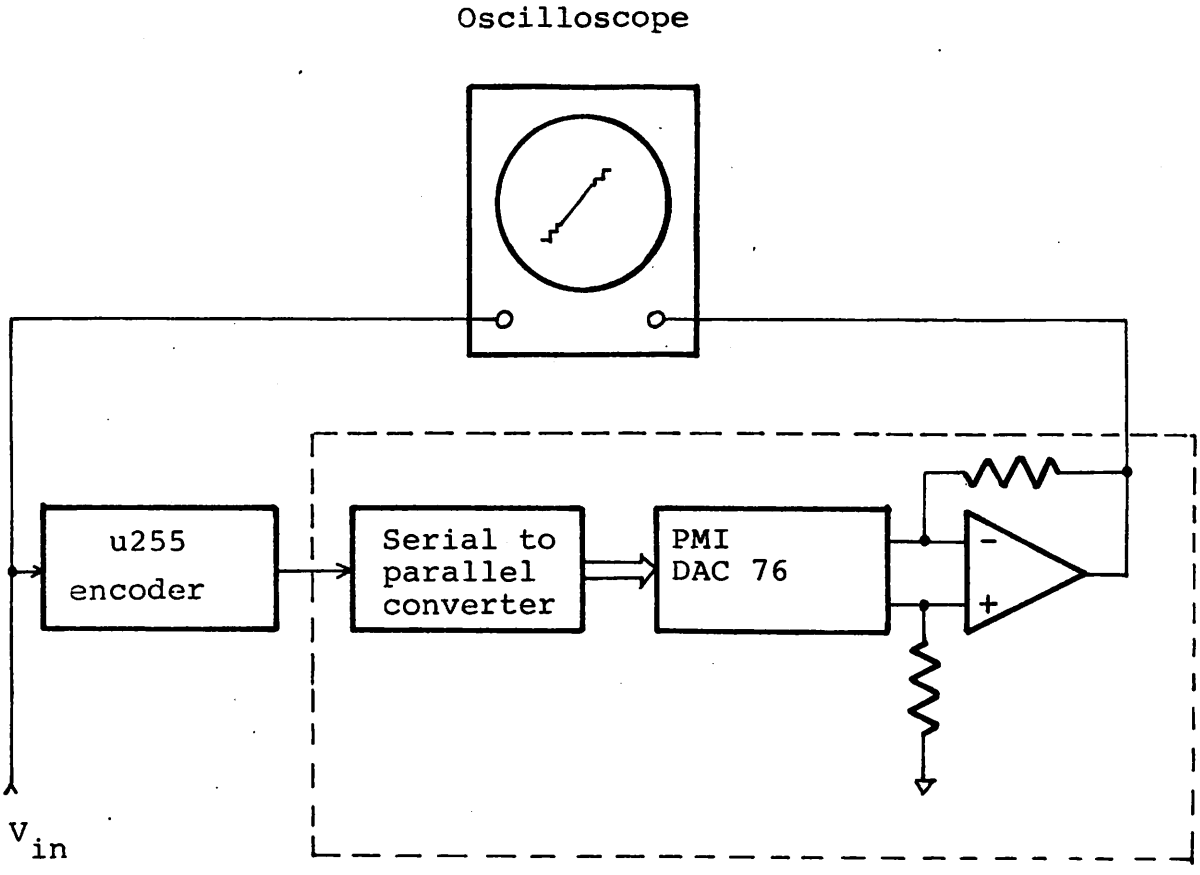
The coder being more complicated was realized first.

It has been already mentioned that the capacitor matching was well within the limits prescribed by the XCODEC analysis.

Some trimming of the original design was performed after measuring the parasitic capacitance in the step capacitor arrays and the offset of the transfer curve due to imperfect feedthrough cancellation at the comparator input. These measurements can be performed using the coder alone and observing the digital output transitions.

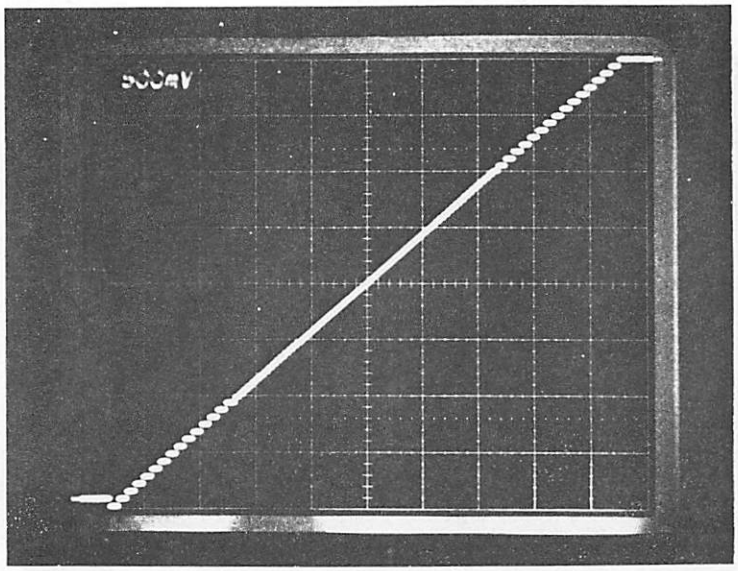
The behavior of the PCM coder in a complete codec configuration was evaluated initially using an existing commercial decoder ( 4 ). The transfer curve obtained with the set-up shown in Figure 4.1 is illustrated in Figure 4.E1.

More detailed views of the most positive and respectively most negative portions of the transfer curve are shown in Figures 4.E2 and 4.E3. The apparent nonmonotonicity at the negative end of the transfer curve is due to the imposed suppresssion of the ideal code corresponding to negative full scale. The nonidealities causing deviations from the ideal transfer curve, such as parasitic capacitance in the step capacitor array, buffer offset voltage and comparator offset voltage can be conveniently visualized with the set-up shown in Figure 4.1, although they can be very well measured in



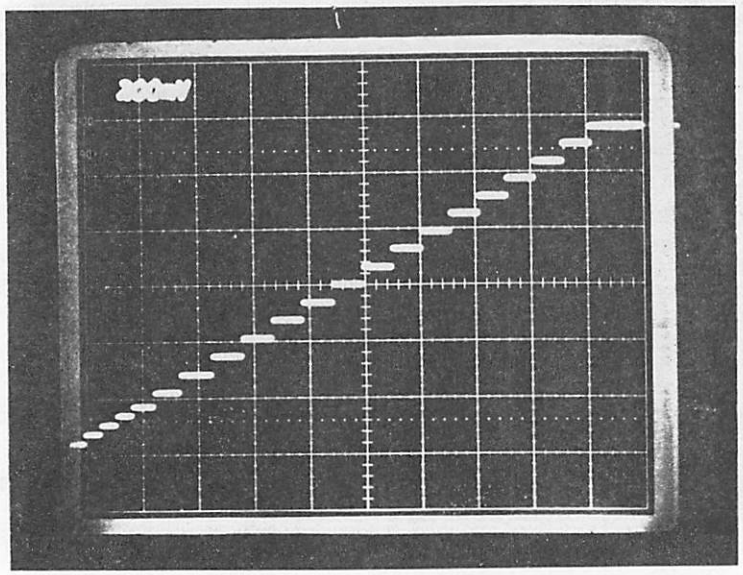

Experimental set-up for visualyzing the overall transfer characteristic of a codec composed of a charge redistribution encoder and a "classical" decoder.

Figure 4.1



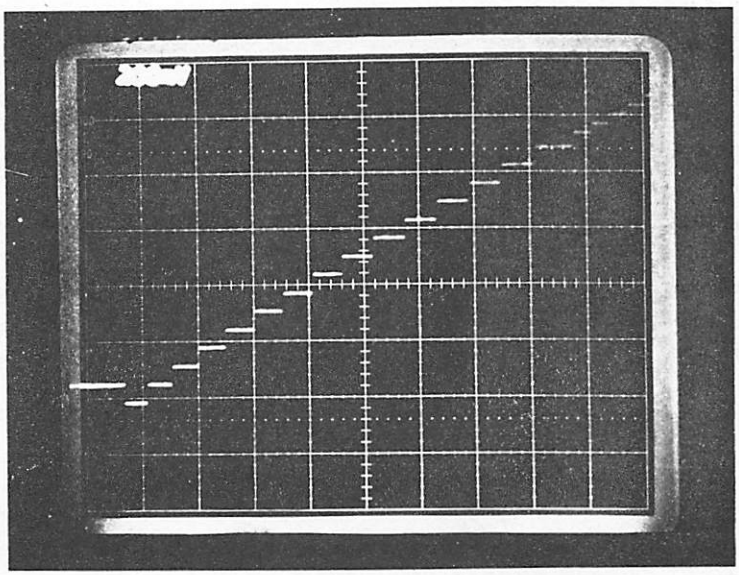

Overall transfer curve of the codec obtained with the set-up shown in Figure 4.1

Figure 4.E1




Most positive segment of the codec transfer characteristic.

Figure 4.E2



Most negative segment of the codec transfer characteristic.

Figure 4.E3

a "digital" manner. These nonidealities were within the limits prescribed by XCODEC so that the trimming was made more for "cosmetical" reasons.

The functionality of the coder in the digital channel bank type of environment was tested by measuring SNR and GTRCK. The set-up used for this purpose is shown in Figure 4.2.

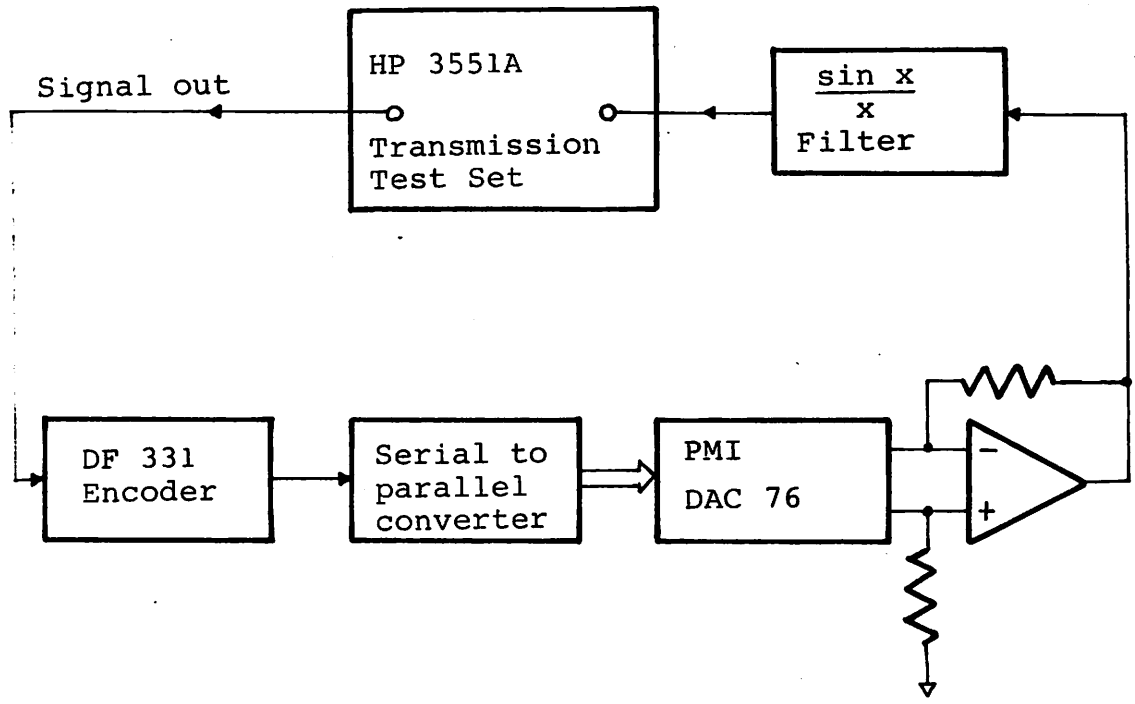
Experimental SNR and GTRCK measurement results are shown in Figure 4.E4.

Since the circuit was intended for real world application it did include the possibility of handling signaling information, i.e. periodically the last bit in the digital output word is replaced with a bit carrying signaling information. This feature was perfectly functional.

The decoder chip, processed later, was also functional from the first run but originally the sample and hold amplifier output did oscillate in the presence of heavier capacitive loads. After this problem was fixed ( 18 ) the decoder performed adequately.

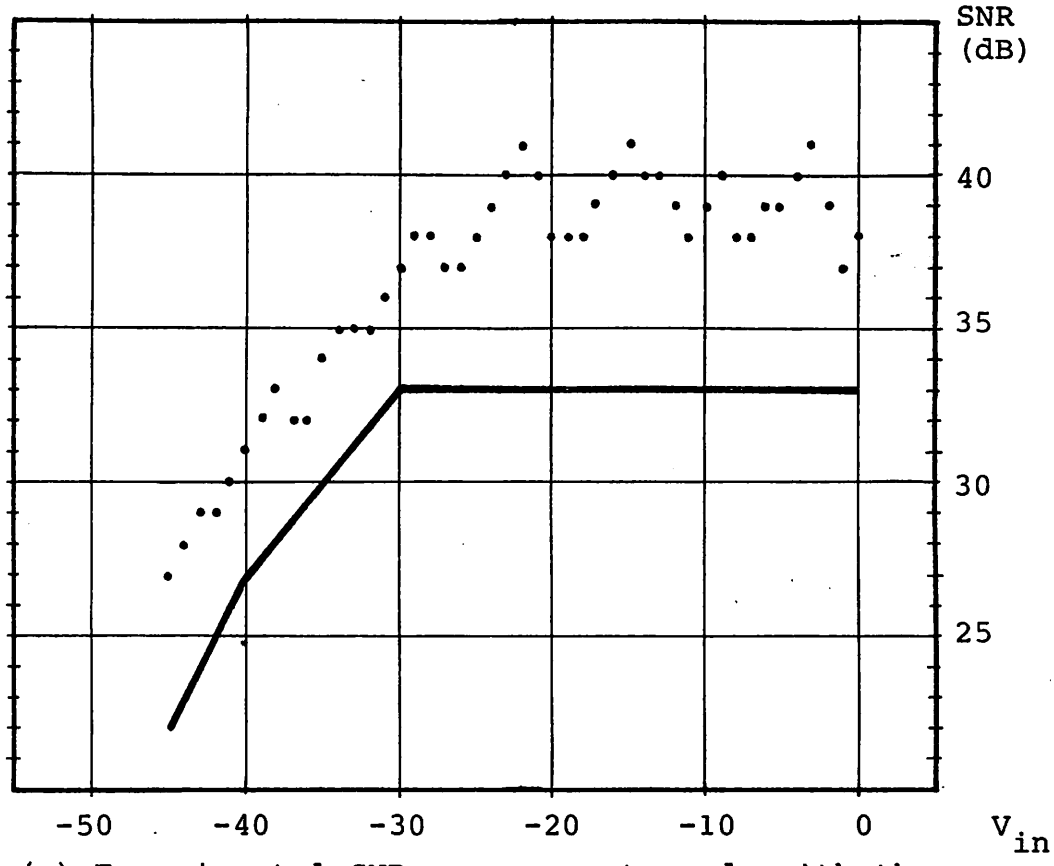
Typical specs describing the performance of the two converters are presented in TABLE 4.E1.

A complete encoder die is shown in Figure 4.E5; overall dimensions are 120 by 120 mils. The decoder chip is somewhat smaller.

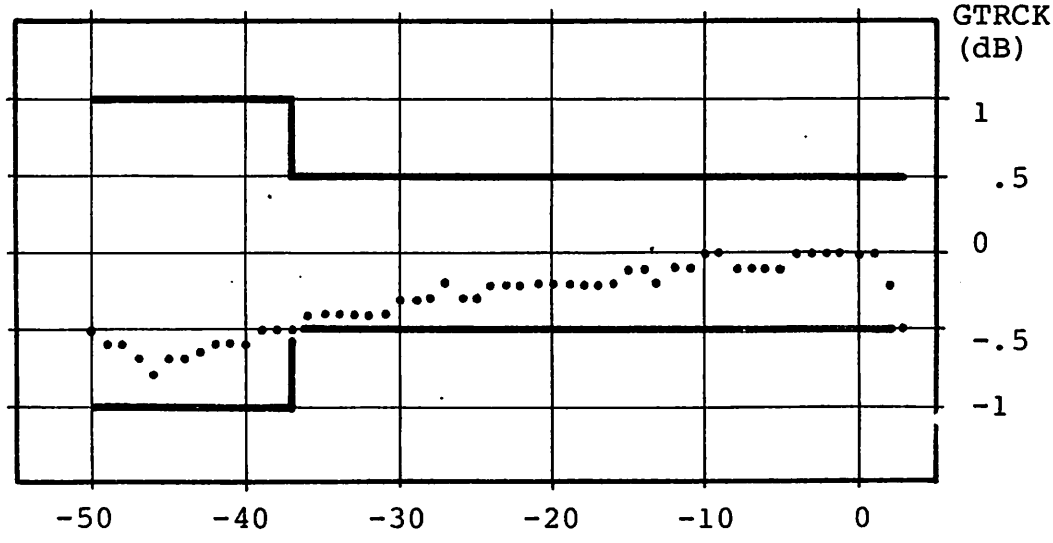



Experimental set-up used for SNR and GTRCK measurements.

Figure 4.2




(a) Experimental SNR measurements made with the set-up shown in Figure 4.2




(b) Experimental GTRCK measurements made with the set-up shown in Figure 4.2

Figure 4.E4

TABLE 4.E1

# Siliconix DF331 Coder - DF332 Decoder Specs (Typical)

| | | | |
|---|---|---|---|
| Supply Voltages | | +5 to +7.5, −7.5 to −15 | |
| Supply Current | | ±3 mA @ ±7.5 V | |
| Reference Current (Peak) | | ±2 mA @ ±3 V | |
| Analog Input Current During Sampling | | 0.5 mA | |
| Clock Frequency | | 1.544 MHz (3.5 MHz Max) | |
| Conversion Rate | Coder | 16 kHz Max | 8 kHz Typ |
| | Decoder | 64 kHz Max | |
| Coder Digital Output | | Open Drain – Sinks 3 TTL Loads | |
| Decoder Analog Output | | Source/Sink 1.5 mA | |
| "A" & "B" Channel Signaling: | | Decoder Outputs – 1 TTL Load | |
| Exceeds D3/D4 Specifications | | | |

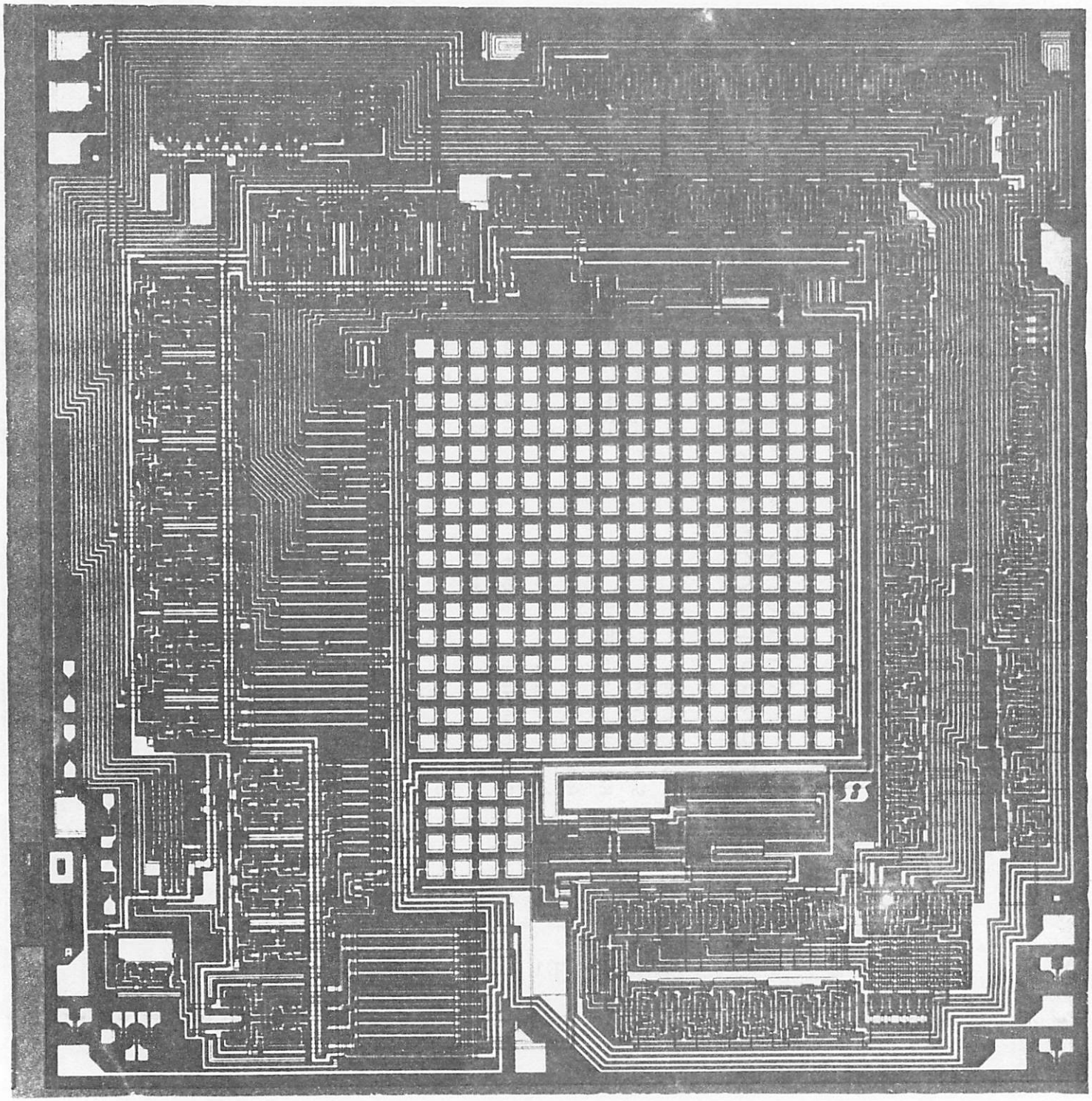


Figure 4.E5

# CHAPTER 5

## 5. CONCLUSIONS.

The work described in this report led to the commercial manufacturing of what is believed to be the first economically feasable channel dedicated codec.

Complementary MOS technology was employed to produce a PCM voice encoder and decoder which meet standard telephone transmission specifications. Operating speed is adequate for multiplexing of two channels through each encoder and decoder, although this would not be the intended use of the converter pair. Die size and yield suggest that these components will become economically competitive with high-speed shared PCM codecs.

Several possibilities for extension of this work are evident. A single reference supply would suffice if a buffer amplifier were added to the chip to provide the opposite polarity reference; demonstrated closed-loop gain accuracy of the amplifier discussed earlier is ample. Power switching of the buffer amplifier and comparator could drastically cut the power consumption of codecs not in use.

A modified version of the codec meeting the European A-law specs is clearly feasable.

A single chip codec could be developed based on time-shared use of one pair of capacitor arrays. If asynchronous (incoherent) encoding and decoding is required, addition of a separate sample and hold amplifier to the encoder would permit interruptions when decode operations are required.

Switchable analog attenuators, now desired at the decoder output in many applications, can be realized simply based on precision-ratioed capacitor arrays on the chip (19).

Another possibility is incorporation of the sharp-cutoff low-pass pre and post-sampling filters on the same chip.

Recent work shows attractive possibilities for realizing such filters based on precision-ratioed capacitors and operational amplifiers (20, 21).

# APPENDIX

## XCODEC users manual.

XCODEC is a computer program capable of analyzing the performance of a codec in terms of signal-to-noise ratio (SNR) and gain tracking (GTRCK). A practical codec is described through user supplied subroutines. XCODEC itself has built in subroutines for ideal coders and decoders. The original version of XCODEC (7) has been modified for the purpose of the present work in order to automatically determine the maximum allowable parameter deviations. This automatic search routine is written for the particular practical codecs being investigated ( in the present case charge redistribution converters ). The coder and respectively decoder under consideration are of the charge redistribution type described in this report. The parameters affecting the performance of the codec are capacitor matching, finite amplifier offset voltages, nonideal amplifier gain, reference voltage matching etc. The program can analyze any one of the four possible combinations between practical and ideal coder or decoder. The output listing will contain the transfer characteristic of the particular codec under investigation and the results of the SNR and GTRCK analysis. In the case of practical converters the parameter deviations affecting the transfer curves will also be displayed.

The parameters describing the practical coder or decoder are defined as follows:

In the segment array for both the coder and the decoder:

$$CX_i = \frac{i}{255}, \text{ where } i = 1, 2, 4, \ldots 128$$

Thus $CX_1+CX_2+\ldots+CX_{128}=CX_{tot}=1$

Nonidealities are introduced as percentage deviations such that the practical capacitances will have the following values:

$$CX_{ipr} = CX_i(1+DCX_i/100)$$

The parasitic capacitance is introduced as a percentage of the total capacitance, i.e.:

$$CX_{totpr}= CX_{tot}+CX_{par}/100$$

In the coder step array:

$$CY_i = \frac{i}{16}, \text{ where } i=1, 2, 4, 8$$

The terminator is expressed as: CYT = 1/16. Such a definition yields again a total array capacitance of 1.

The deviations are introduced in a similar manner to the case of the segment array. The parasitic capacitance is expressed again as a percentage of the total array capacitance.

In the decoder step array:

$CY_i = \frac{2i}{33}$, where i=1, 2, 4, 8. The two terminators (used for 7 and respectively 8 bit decoding) are expressed as:

$$CYT_2 = 2/33 \text{ and } CYT_1 = 1/33$$

The deviations from the ideal values and the parasitic capacitance are introduced like before.

The comparator offset voltage, VOSC, is introduced as a percentage of the reference voltage. The same applies for comparator overdrive, OVERDR, buffer amplifier offset in the decoder, VOSAY, and buffer amplifier offset in the coder, VOSA. The offset voltage of the sample and hold amplifier has no influence on SNR or GTRCK and is therefore assumed to be ideal. The nonideal amplifier gain is described with:

$$GAIN = 1 - DGAIN/100$$

in the coder ( and with DGAINY in the decoder).

The reference voltage mismatch is introduced as a deviation of the negative reference:

$$V_R^- = -V_R^+(1+DVRN/100)$$

The automatic search procedure consists of an iterative analysis. One of the parameters describing the practical codec is modified such that initially the codec will fail to pass SNR and GTRCK specs. The nonideal parameter will then be modified by the program until the specs are met (or the maximum number of iterations is reached). In order to perform the automatic search routine the program has to be supplied with four numbers as follows:

DPARM(1) which is a deviation from the ideal value of the parameter being investigated that would yield spec "proof" codecs; DPARM(2) which is the initial deviation supplied by the user; JEM an integer which designates the particular parameter to be investigated and JUP, an integer representing the maximum number of iterations to be performed. The search algorithm operates as follows:

The parameter under investigation is modified with DPARM(2), the codec transfer characteristics are computed and the resulting combination is subject to SNR and GTRCK tests.

If the codec does not pass the specs then the next run is performed with:

$$DPARM(3) = DPARM(2) - \frac{DPARM(2)-DPARM(1)}{2}$$

If the test is successful then the next run is performed with:

$$DPARM(3) = 2 \times DPARM(2)$$

This last modification of DPARM applies only in the case when the specs are passed the first time. Otherwise the modification of DPARM is performed on the basis of a successive approximation routine. Continuing this procedure, the program will find the largest acceptable deviation of the particular parameter being investigated. If the specs are still not being passed at the end of the routine then either DPARM(2) or JUP, or both, have to be modified. After completing the search the program will repeat the run corresponding to the largest possible deviation which does still yield acceptable performance and will prepare an output. The sequence of DPARM´s used in the search algorithm will be printed thus simplifying the interpretation of the final result. The output will also contain a list of the parameter deviations for all the parameters describing the practical coder or respectively decoder. This is followed by the results of the SNR and GTRCK analysis and the listing of the

transfer characteristics.

The input deck contains the following cards:

1. A card specifying the positive reference voltage, with the format F10.3.

2. A card specifying the combination of coder and decoder being investigated:

11 for ideal coder and decoder

21 for practical coder and ideal decoder

22 for practical coder and decoder

12 for ideal coder and practical decoder

3. A card containing the deviations from their ideal values of the capacitors in the coder segemnt array, $DCX_i$, with the format 8F10.3.

4. A card containing the deviations from their ideal values of the capacitors in the coder step array, $DCY_i$, DCYT, with the format 5F10.3

5. A card containing the deviations from their ideal values of the remaining coder parameters, DVRN, VOSC, OVERDR, VOSA, DGAIN, CXP, CYP, with the format 7F10.5

6. A card containing the deviations from their ideal values of the decoder segement array capacitors, $DCX_i$, with the format 8F10.3.

7. A card containing the deviations from their ideal values of the decoder step array capacitors, $DCY_i$, $DCYT_2$, $DCYT_1$, with the format 6F10.3.

8. A card containing the deviations from their ideal values of the remaining decoder parameters, DVRND, VOSAY, DGAINY,

CYPD, with the format 4F10.5.

9. A card containing the parameters used for the SNR and GTRCK analysis, DBUP, DBLOW, NPA. DBUP is the upper limit of the test sinewave, DBLOW is the lower limit and NPA is the number of points to be tested (amplitudes). An amplitude equal to the magnitude of the reference voltage is defined as +3dB. The format for this card is: 2F10.4,I10.

10. This card contains the parameters for the automated search routine, DPARM(1), DPARM(2), JEM, JUP. The format is 2F10.3,2I2. This card should be left out for single pass analysis.

The listing reproduced in this Appendix is a modified version of the original XCODEC; the modification was necessary in order to adapt the program to a VARIAN V73 minicomputer. The subroutines describing the practical coder and decoder have been obviously written for the particular type of codec described in this report.

The sample run reproduced in this Appendix corresponds to the automated search for the maximum allowable comparator overdrive.

```
C       ************************************************************
C
C       PROGRAM XCODEC ADAPTED TO AUTOMATIC SEARCH
C
C       ************************************************************
C
        REAL NO
        COMMON XFL,PRC,PRD
       //CODER/DCXB(8),DCYB(5),DCX(8),DCY(5),DVRN,VOSC,OVERDR,
       /VOSA,GAIN,CXP,CYP,VGL(2,8,16),VGU(2,8,16)
       //DECOD/DCXBD(8),DCYBD(6),DCXD(8),DCYD(6),DVRND,VOSAY,
       /GAINY,CYPD,VGO(2,8,16)
       //VALUES/DBUP,DBLOW,NPA,XPZ(54),SDRDBZ(54),GTRACZ(54),
       /XFUNDZ(54),BOPTZ(54),ZAPZ(54),DBINZ(54),SMARZ(54),
       /GMARZ(54)
        DIMENSION DPARM(15),INDEX(15)
        DATA Y,NO,OK/1HY,2HNO,2HOK/
        IR=4
        IW=5
        PRC=0.
        PRD=0.
        READ(IR,11) XFL
     11 FORMAT (F10.4)
        READ(IR,16) KC,KD,ISA
     16 FORMAT (3I1)
        IF(KC.EQ.1) GO TO 1003
        READ(IR,1000) (DCXB(I),I=1,8)
   1000 FORMAT(8F10.3)
        READ(IR,1001) (DCYB(I),I=1,5)
   1001 FORMAT(5F10.3)
        READ(IR,1002) DVRN,VOSC,OVERDR,VOSA,GAIN,CXP,CYP
   1002 FORMAT(7F10.5)
   1003 IF(KD.EQ.1) GO TO 1007
        READ(IR,1004) (DCXBD(I),I=1,8)
   1004 FORMAT(8F10.3)
        READ(IR,1005) (DCYBD(I),I=1,6)
   1005 FORMAT(6F10.3)
        READ(IR,1006) DVRND,VOSAY,GAINY,CYPD
   1006 FORMAT(4F10.5)
   1007 READ(IR,521) DBUP,DBLOW,NPA
    521 FORMAT (2F10.4,I10)
        IF(ISA.EQ.1) GO TO 1009
        READ(IR,1008) DPARM(1),DPARM(2),JEM,JUP
   1008 FORMAT(2F10.3,2I2)
        JAR=1
```

```
      DO 3500 NPAR=1,JUP
 3500 INDEX(NPAR)=0
      DO 3000 NPAR=2,JUP
      DPARAM=DPARM(NPAR)
 4000 GO TO (4001,4002,4003,4004,4005,4006,4007,4008,4009,
     /4010,4011,4012,4013,4014,4015,4016,4017,4018,4019,4020
     /,4021,4022,4023,4024,4025,4026,4027,4028,4029,4030,
     / 4031,4032,4033,4034,4035,4036,4037,4038),JEM
 4001 DCXB(1) =DPARAM
      GO TO 4100
 4002 DCXB(2) =DPARAM
      GO TO 4100
 4003 DCXB(3) =DPARAM
      GO TO 4100
 4004 DCXB(4) =DPARAM
      GO TO 4100
 4005 DCXB(5) =DPARAM
      GO TO 4100
 4006 DCXB(6) =DPARAM
      GO TO 4100
 4007 DCXB(7) =DPARAM
      GO TO 4100
 4008 DCXB(8) =DPARAM
      GO TO 4100
 4009 CXP     =DPARAM
      GO TO 4100
 4010 DCYB(1) =DPARAM
      GO TO 4100
 4011 DCYB(2) =DPARAM
      GO TO 4100
 4012 DCYB(3) =DPARAM
      GO TO 4100
 4013 DCYB(4) =DPARAM
      GO TO 4100
 4014 DCYB(5) =DPARAM
      GO TO 4100
 4015 CYP     =DPARAM
      GO TO 4100
 4016 DVRN    =DPARAM
      GO TO 4100
 4017 VOSC    =DPARAM
      GO TO 4100
 4018 OVERDR  =DPARAM
      GO TO 4100
 4019 VOSA    =DPARAM
```

```
      GO TO 4100
 4020 GAIN    =DPARAM
      GO TO 4100
 4021 DCXBD(1)=DPARAM
      GO TO 4100
 4022 DCXBD(2)=DPARAM
      GO TO 4100
 4023 DCXBD(3)=DPARAM
      GO TO 4100
 4024 DCXBD(4)=DPARAM
      GO TO 4100
 4025 DCXBD(5)=DPARAM
      GO TO 4100
 4026 DCXBD(6)=DPARAM
      GO TO 4100
 4027 DCXBD(7)=DPARAM
      GO TO 4100
 4028 DCXBD(8)=DPARAM
      GO TO 4100
 4029 DCYBD(1)=DPARAM
      GO TO 4100
 4030 DCYBD(2)=DPARAM
      GO TO 4100
 4031 DCYBD(3)=DPARAM
      GO TO 4100
 4032 DCYBD(4)=DPARAM
      GO TO 4100
 4033 DCYBD(5)=DPARAM
      GO TO 4100
 4034 DCYBD(6)=DPARAM
      GO TO 4100
 4035 CYPD    =DPARAM
      GO TO 4100
 4036 DVRND   =DPARAM
      GO TO 4100
 4037 VOSAY   =DPARAM
      GO TO 4100
 4038 GAINY   =DPARAM
 4100 CONTINUE
 1009 IF (KC.EQ.2) GO TO 12
      IF((ISA.NE.1).AND.(PRC.EQ.1.).AND.(JEM.GE.21))GO TO 17
      CALL IDCODR
      GO TO 17
   12 IF((ISA.NE.1).AND.(PRC.EQ.1.).AND.(JEM.GE.21))GO TO 17
      CALL OVLAY(0,0,5HOVER1)
```

```
C       THIS IS THE SUBROUTINE DESCRIBING THE PRACTICAL CODER
   17 IF (KD.EQ.2) GO TO 14
      IF((ISA.NE.1).AND.(PRD.EQ.1.).AND.(JEM.LE.20))GO TO 19
      CALL IDECOD
      GO TO 19
   14 IF((ISA.NE.1).AND.(PRD.EQ.1.).AND.(JEM.LE.20))GO TO 19
      CALL PDECOD
   19 CONTINUE
      CALL OVLAY(0,0,5HOVER2)
C     THIS IS DISTAC
      IF(ISA.EQ.1) GO TO 1010
      IF(JAR.EQ.2) GO TO 1010
      SZAP=0.
      DO 8000 I=1,NPA
 8000 SZAP=SZAP+ZAPZ(I)
      IF(SZAP.NE.0.) GO TO 7100
      INDEX(NPAR)=1
 7100 DELTA=(DPARM(NPAR-1)-DPARM(NPAR))/2.
      DELTA=SIGN(DELTA,DPARAM)
      DO 3002 KAP=2,NPAR
      IF(INDEX(KAP).EQ.0) GO TO 3008
 3002 CONTINUE
      DPARM(NPAR+1)=2.*DPARM(NPAR)
      IF(DPARM(NPAR+1).LT.-100.)
     /DPARM(NPAR+1)=DPARM(NPAR)/2.-50.
      GO TO 3000
 3008 DPARM(NPAR+1)=DPARM(NPAR)+DELTA
      IF(INDEX(NPAR).EQ.0) DPARM(NPAR+1)=DPARM(NPAR)-DELTA
 3000 CONTINUE
      JUPM=JUP-1
      JUPP=JUP+1
      DO 3004 K=1,JUPM
      KR=JUPP-K
      IF(INDEX(KR).EQ.0) GO TO 3004
      DPARAM=DPARM(KR)
      GO TO 3005
 3004 CONTINUE
      DPARAM=DPARM(JUP)
 3005 JAR=2
      GO TO 4000
 1010 CONTINUE
      IF(ISA.EQ.1) GO TO 7805
      WRITE(IW,1)
      WRITE(IW,7800) JEM
 7800 FORMAT(/10X,
```

```
      /'THE SENSITIVITY TO PARAMETER NO.',I2,
      /' HAS BEEN TESTED')
       WRITE(IW,7801) JEM
 7801 FORMAT(10X,
      /'THE VALUES USED FOR PARAMETER NO.',I2,' HAVE BEEN:')
       DO 7804 I=2,JUP
       IF(INDEX(I).EQ.1) WRITE(IW,7802) DPARM(I)
 7802 FORMAT(/10X,F8.3,5X,'PASSING VALUE')
       IF(INDEX(I).EQ.0) WRITE(IW,7803) DPARM(I)
 7803 FORMAT(/10X,F8.3,23X,'FAILING VALUE')
 7804 CONTINUE
 7805 IF(KC.EQ.1) GO TO 7004
       WRITE(3,2006)
 2006 FORMAT(/1X,'DO YOU WANT CODER NONIDEALITIES ? Y/NO')
       READ(3,2002) XLIST
       IF(XLIST.EQ.NO) GO TO 7004
       WRITE(IW,1)
       WRITE(IW,7000)
 7000 FORMAT(/10X,
      /'THE NONIDEALITIES OF THE PRACTICAL CODER ARE:'//)
       DO 7001 I=1,8
 7001 DCX(I)=DCX(I)*100.
       DO 7002 I=1,5
 7002 DCY(I)=DCY(I)*100.
       WRITE(IW,7003) (DCX(I),I=1,8),CXP,(DCY(I),I=1,5),CYP,
      /DVRN,VOSC,OVERDR,VOSA,GAIN
 7003 FORMAT(10X,' 1 DCX1    =',F8.3/
      /        10X,' 2 DCX2    =',F8.3/
      /        10X,' 3 DCX4    =',F8.3/
      /        10X,' 4 DCX8    =',F8.3/
      /        10X,' 5 DCX16   =',F8.3/
      /        10X,' 6 DCX32   =',F8.3/
      /        10X,' 7 DCX64   =',F8.3/
      /        10X,' 8 DCX128  =',F8.3/
      /        10X,' 9 CXP     =',F8.3/
      /        10X,'10 DCY1    =',F8.3/
      /        10X,'11 DCY2    =',F8.3/
      /        10X,'12 DCY4    =',F8.3/
      /        10X,'13 DCY8    =',F8.3/
      /        10X,'14 DCYTM   =',F8.3/
      /        10X,'15 CYP     =',F8.3/
      /        10X,'16 DVRN    =',F8.3/
      /        10X,'17 VOSC    =',F8.3/
      /        10X,'18 OVERDR  =',F8.3/
      /        10X,'19 VOSA    =',F8.3/
```

```
      /        10X,'20 DGAIN  =',F8.3/)
 7004 IF(KD.EQ.1) GO TO 7005
      WRITE(3,2008)
 2008 FORMAT(/1X,'DO YOU WANT DECODER NONIDEALITIES ? Y/NO')
      READ(3,2002) XLIST
      IF(XLIST.EQ.NO) GO TO 7777
      WRITE(IW,1)
      WRITE(IW,7006)
 7006 FORMAT(/10X,
     /'THE NONIDEALITIES OF THE PRACTICAL DECODER ARE:'//)
      DO 7007 I=1,8
 7007 DCXD(I)=DCXD(I)*100.
      DO 7008 I=1,6
 7008 DCYD(I)=DCYD(I)*100.
      WRITE(IW,7009) (DCXD(I),I=1,8),(DCYD(I),I=1,6),CYPD,
     /DVRND,VOSAY,GAINY
 7009 FORMAT(10X,'21 DCX1    =',F8.3/
     /        10X,'22 DCX2    =',F8.3/
     /        10X,'23 DCX4    =',F8.3/
     /        10X,'24 DCX8    =',F8.3/
     /        10X,'25 DCX16   =',F8.3/
     /        10X,'26 DCX32   =',F8.3/
     /        10X,'27 DCX64   =',F8.3/
     /        10X,'28 DCX128  =',F8.3/
     /        10X,'29 DCY1    =',F8.3/
     /        10X,'30 DCY2    =',F8.3/
     /        10X,'31 DCY4    =',F8.3/
     /        10X,'32 DCY8    =',F8.3/
     /        10X,'33 DCYTM   =',F8.3/
     /        10X,'34 DCYHS   =',F8.3/
     /        10X,'35 CYP     =',F8.3/
     /        10X,'36 DVRN    =',F8.3/
     /        10X,'37 VOSAY   =',F8.3/
     /        10X,'38 DGAINY  =',F8.3/)
 7005 CONTINUE
 7777 CONTINUE
      WRITE(3,2001)
 2001 FORMAT(/1X,'DO YOU WANT MEASUREMENTS ?  Y/NO')
      READ(3,2002) XLIST
 2002 FORMAT(A4)
      IF(XLIST.EQ.NO) GO TO 2003
C
C     MEASUREMENT RESULTS
C
      DO 1013 IZ=1,NPA
```

```
      IF((IZ.NE.1).AND.(IZ.NE.36)) GO TO 50
      WRITE (3,2100)
 2100 FORMAT(/1X, 'CHANGE PAPER ! ')
      READ (3,2101) PAPER
 2101 FORMAT (A4)
      IF(PAPER.NE.OK) GO TO 2005
      WRITE(IW,1)
      IF (KC.NE.1) GO TO 22
      WRITE(IW,13)
      GO TO  23
   22 WRITE(IW,18)
   23 IF (KD.NE.1) GO TO 25
      WRITE(IW,3)
      GO TO 26
   25 WRITE(IW,15)
   26 XX=XFL*(10.**(-3./20.))
      WRITE(IW,509) XX,XFL
  509 FORMAT(/  1X, 'THE 0 DB REFERENCE IS',F6.2, 'V AT',F6.2,
     /'V FULL SCALE'/)
      WRITE(IW,516)
  516 FORMAT(1X,69(1H*)//3X, 'INPUT',3X, 'INPUT',4X, 'SDR',4X,
     /'GAIN',4X, 'OUTPUT',3X, 'OUTPUT',5X, 'SDR',6X, 'GTRCR'/19X
     /, 'C-MES',3X, 'TRCK',4X, 'FUNDM',5X, 'DC',8X, 'MARGIN',3X,
     /'MARGIN'/4X, '(V)',5X, '(DB)',4X, '(DB)',3X, '(DB)',5X,
     /'(V)',6X, '(V)',7X, '(DB)',5X, '(DB)'//1X,69(1H*)/)
   50 XP=XPZ(IZ)
      DBIN=DBINZ(IZ)
      SDRDB=SDRDBZ(IZ)
      GTRAC=GTRACZ(IZ)
      XOFUND=XFUNDZ(IZ)
      BOPT=BOPTZ(IZ)
      SMAR=SMARZ(IZ)
      GMAR=GMARZ(IZ)
      IF(DBIN.GT.3.) WRITE(IW,680) XP,DBIN,SDRDB,GTRAC,
     /XOFUND,BOPT
      IF((DBIN.GT.0.).AND.(DBIN.LE.3.)) WRITE(IW,681) XP,
     /DBIN,SDRDB,GTRAC,XOFUND,BOPT,GMAR
      IF((DBIN.GE.-45.).AND.(DBIN.LE.0.)) WRITE(IW,682) XP,
     /DBIN,SDRDB,GTRAC,XOFUND,BOPT,SMAR,GMAR
      IF((DBIN.GE.-50.).AND.(DBIN.LT.-45.))WRITE(IW,681) XP,
     /DBIN,SDRDB,GTRAC,XOFUND,BOPT,GMAR
      IF(DBIN.LT.-50.) WRITE(IW,680) XP,DBIN,SDRDB,GTRAC,
     /XOFUND,BOPT
  680 FORMAT(1X,F7.4,2X,F6.2,3X,F5.2,2X,F5.2,1X,F7.4,2X,F7.4
     /,6X, 'UNDEF',4X, 'UNDEF')
```

```
  681 FORMAT(1X,F7.4,2X,F6.2,3X,F5.2,2X,F5.2,1X,F7.4,2X,F7.4
     /,6X,'UNDEF',3X,F6.2)
  682 FORMAT(1X,F7.4,2X,F6.2,3X,F5.2,2X,F5.2,1X,F7.4,2X,F7.4
     /,5X,F6.2,3X,F6.2)
 1013 CONTINUE
 2003 WRITE(3,2004)
 2004 FORMAT(1X,
     /'DO YOU WANT TRANSFER CHARACTERISTICS ? Y/NO')
      READ(3,2002) XLIST
      IF(XLIST.EQ.NO) GO TO 2005
      DO 8 KS=1,2
      DO 8 KL=1,8
      IF(MOD(KL,2)) 40,41,40
   40 WRITE (3,2100)
      READ (3,2101) PAPER
      IF(PAPER.NE.OK) GO TO 2005
      WRITE(IW,1)
    1 FORMAT(1H1,69(1H*)//1X,'PROGRAM XCODEC'//1X,69(1H*)/)
      IF(KC.EQ.2) GO TO 1011
      WRITE(IW,13)
   13 FORMAT (1X,'THE CODER IS IDEAL')
      GO TO 1020
 1011 WRITE(IW,18)
   18 FORMAT (1X,'THE CODER IS PRACTICAL')
 1020 IF(KD.EQ.2) GO TO 1012
      WRITE(IW,3)
    3 FORMAT (1X,'THE DECODER IS IDEAL')
      GO TO 1021
 1012 WRITE(IW,15)
   15 FORMAT (1X,'THE DECODER IS PRACTICAL')
 1021 CONTINUE
C
C     EVALUATING CODEC INPUT - OUTPUT CHARACTERISTICS
C
      WRITE(IW,4)
    4 FORMAT(1X,'S=SIGN BIT'/1X,
     /'L=ONES COMPLEMENT OF SEGMENT WORD IN DECIMAL'/1X,
     /'V=ONES COMPLEMENT OF STEP WORD IN DECIMAL'//1X,
     /69(1H*)//1X,'S',1X,'L',2X,'V',5X,'INPUT',5X,'INPUT',4X
     /,'INPUT',4X,'INPUT',5X,'OUTPUT',3X,'TRACKING'/12X,
     /'LOWER',5X,'UPPER',4X,'STEP',5X,'MIDDLE',4X,'LEVEL',4X
     /,'ERROR'/12X,'LIMIT',5X,'LIMIT',4X,'SIZE',5X,'POINT'/
     /13X,'(V)',7X,'(V)',5X,'(MV)',6X,'(V)',7X,'(V)'//1X,
     /69(1H*))
   41 WRITE(IW,42)
```

```
   42 FORMAT(/)
      DO 8 KV=1,16
      VVGL=VGL(KS,KL,KV)
      VVGU=VGU(KS,KL,KV)
      DVG=1000.*(VVGU-VVGL)
      VGMID=(VVGL+VVGU)/2.0
      VVGO=VGO(KS,KL,KV)
      NS=2-KS
      NL=KL-1
      NV=KV-1
      IF (VVGO.EQ.0.0) GO TO 5
      TRER=1.0-VGMID/VVGO
      WRITE(IW,6) NS,NL,NV,VVGL,VVGU,DVG,VGMID,VVGO,TRER
    6 FORMAT(1X,I1,1X,I1,1X,I2,2X,F8.4,2X,F8.4,4X,F5.1,2X,
     /F8.4,2X,F8.4,4X,F7.3)
      GO TO 8
    5 WRITE(IW,7) NS,NL,NV,VVGL,VVGU,DVG,VGMID,VVGO
    7 FORMAT(1X,I1,1X,I1,1X,I2,2X,F8.4,2X,F8.4,4X,F5.1,2X,
     /F8.4,2X,F8.4,4X,'UNDEF.')
    8 CONTINUE
 2005 STOP
      END
0 ERRORS COMPILATION COMPLETE
```

```
PAGE    1  07/28/77  FAST       VORTEX  FTN IV                2338 HOURS

      1          SUBROUTINE IDCODR
      2          COMMON XFL,PRC,PRD
      3         //CODER/DCXB(8),DCYB(5),DCX(8),DCY(5),DVRN,VOSC,OVERDR,
      4         /VOSA,GAIN,CXP,CYP,YL(2,8,16),YU(2,8,16)
      5          SCALIN =XFL/4079.5
      6          DO 201 IL=1,8
      7          DO 201 IV=1,16
      8          KL=IL-1
      9          KV=IV-1
     10          GV=FLOAT(KV)
     11          YU(1,IL,IV)=((2.0**KL)*(GV+17.0)-16.5)*SCALIN
     12          YL(2,IL,IV)=-YU(1,IL,IV)
     13          IF(IV-1) 203,202,203
     14      202 IF(IL-1) 205,204,205
     15      204 YL(1,1,1)=0.0
     16          GO TO 206
     17      205 YL(1,IL,1)=YU(1,KL,16)
     18          GO TO 206
     19      203 YL(1,IL,IV)=YU(1,IL,KV)
     20      206 YU(2,IL,IV)=-YL(1,IL,IV)
     21      201 CONTINUE
     22          PRC=1.
     23          PRC=1.
     24          RETURN
     25          END
   0 ERRORS COMPILATION COMPLETE
```

```
PAGE    1   07/28/77  FAST       VORTEX   FTN IV                2341 HOURS

      1          SUBROUTINE IDECOD
      2          COMMON XFL,PRC,PRD
      3         //DECOD/DCXBD(8),DCYBD(6),DCXD(8),DCYD(6),DVRND,VOSAY,
      4         /GAINY,CYPD,YO(2,8,16)
      5          SCALIN =XFL/4079.5
      6          DO 301 IL=1,8
      7          DO 301 IV=1,16
      8          KL=IL-1
      9          KV=IV-1
     10          GV=FLOAT(KV)
     11          YO(1,IL,IV)=((2.0**KL)*(GV+16.5)-16.5)*SCALIN
     12      301 YO(2,IL,IV)=-YO(1,IL,IV)
     13          PRD=1.
     14          RETURN
     15          END
   0 ERRORS COMPILATION COMPLETE
```

```
      SUBROUTINE PDECOD
      COMMON XFL,PRC,PRD
     //DECOD/DCXBD(8),DCYBD(6),DCXD(8),DCYD(6),DVRND,VOSAY,
     /GAINY,CYPD,VOU(2,8,16)
      DIMENSION CX(8),CYD(8)
      VR=XFL
      VRN=-(1.+DVRND/100.)*XFL
      VA=XFL*VOSAY/100.
      GA=1.-GAINY/100.
      SCX=0.
      SUM=0.
      DO 10 I=1,8
      VAL=2.**(I-1)
      IF(DCXBD(I).EQ.0.) SCX=SCX+VAL
   10 SUM=SUM-DCXBD(I)*VAL/100.
      DEV=SUM/SCX
      DO 11 I=1,8
      DCXD(I)=DCXBD(I)/100.
      IF(DCXBD(I).EQ.0.) DCXD(I)=DEV
   11 CX(I)=(2.**(I-1))*(1.+DCXD(I))/255.
      SCY=0.
      SUMY=0.
      DO 13 I=1,4
      VAL=2.**I
      IF(DCYBD(I).EQ.0.) SCY=SCY+VAL
   13 SUMY=SUMY-DCYBD(I)*VAL/100.
      SUMY=SUMY-DCYBD(5)/50. -DCYBD(6)/100.
      IF(DCYBD(5).EQ.0.) SCY=SCY+2.
      IF(DCYBD(6).EQ.0.) SCY=SCY+1.
      DEVY=SUMY/SCY
      DO 14 I=1,6
      DCYD(I)=DCYBD(I)/100.
      IF(DCYBD(I).EQ.0.) DCYD(I)=DEVY
   14 CONTINUE
      DIV=33.*(1.+ CYPD/100.)
      DO 15 I=1,4
      J=2**I
      K=2**(I-1)
   15 CYD(K)=FLOAT(J)*(1.+DCYD(I))/DIV
      DO 1 I=1,2
      B1=FLOAT(I-1)
      DO 1 J=1,8
      VOUT=0.
      IF(J.EQ.1) GO TO 2
      KAP=J-1
```

```
      CSUM=0.
      DO 3 KAL=1,KAP
    3 CSUM=CSUM+CX(KAL)
      VOUT=CSUM*(VR*(1.-B1)+VRN*B1)
    2 DO 1 K=1,16
      LSTP=K-1
      L5=LSTP/8
      L56=MOD(LSTP,8)
      L6=L56/4
      L67=MOD(L56,4)
      L7=L67/2
      L8=MOD(L67,2)
      B5=FLOAT(L5)
      B6=FLOAT(L6)
      B7=FLOAT(L7)
      B8=FLOAT(L8)
      VYT=CYD(1)*B8+CYD(2)*B7+CYD(4)*B6+CYD(8)*B5
    1 VOU(I,J,K)=VOUT+(VYT*(VR*(1.-B1)+VRN*B1)-VA)*GA*CX(J)
      PRD=1.
      RETURN
      END
0 ERRORS COMPILATION COMPLETE
```

```
      SUBROUTINE PCODER
      COMMON XFL,PRC,PRD
     //CODER/DCXB(8),DCYB(5),DCX(8),DCY(5),DVRN,VOSC,OVERDR,
     /VOSA,GAIN,CXP,CYP,VLO(2,8,16),VUP(2,8,16)
      DIMENSION VX(8),VXN(8),VY(15),VYN(15),CX(8),CY(16)
      VR=XFL
      VRN=-(1.+DVRN/100.)*XFL
      VOSCEF=-(1.+CXP/100.)*VOSC*XFL/100.
      VA=XFL*VOSA/100.
      GA=1.-GAIN/100.
      OVDR=OVERDR*XFL/100.
      SCX=0.
      SUM=0.
      DO 10 I=1,8
      VAL=2.**(I-1)
      IF(DCXB(I).EQ.0.) SCX=SCX+VAL
   10 SUM=SUM-DCXB(I)*VAL/100.
      DEV=SUM/SCX
      DO 11 I=1,8
      DCX(I)=DCXB(I)/100.
      IF(DCXB(I).EQ.0.) DCX(I)=DEV
   11 CX(I)=(2.**(I-1))*(1.+DCX(I))/255.
      VX(1)=CX(1)*VR
      VXN(1)=CX(1)*VRN
      DO 12 I=1,7
      VX(I+1)=VX(I)+CX(I+1)*VR
   12 VXN(I+1)=VXN(I)+CX(I+1)*VRN
      SCY=0.
      SUMY=0.
      DO 13 I=1,4
      VAL=2.**(I-1)
      IF(DCYB(I).EQ.0.) SCY=SCY+VAL
   13 SUMY=SUMY-DCYB(I)*VAL/100.
      SUMY=SUMY-DCYB(5)/100.
      IF(DCYB(5).EQ.0.) SCY=SCY+1.
      DEVY=SUMY/SCY
      DO 14 I=1,5
      DCY(I)=DCYB(I)/100.
      IF(DCYB(I).EQ.0.) DCY(I)=DEVY
   14 CONTINUE
      DIV=16.*(1.+CYP/100.)
      DO 15 I=1,4
      J=2**(I-1)
   15 CY(J)=FLOAT(J)*(1.+DCY(I))/DIV
      DO 16 I=1,15
```

```
      LA=I/8
      LAB=MOD(I,8)
      LB=LAB/4
      LBC=MOD(LAB,4)
      LC=LBC/2
      LD=MOD(LBC,2)
      C=0.
      IF(LA.EQ.1) C=CY(8)
      IF(LB.EQ.1) C=C+CY(4)
      IF(LC.EQ.1) C=C+CY(2)
      IF(LD.EQ.1) C=C+CY(1)
      CY(I)=C
      VY(I)=(CY(I)*VR-VA)*GA
   16 VYN(I)=(CY(I)*VRN-VA)*GA
      DO 1 I=1,2
      DO 1 J=1,8
      LSG=J-1
      L2=LSG/4
      L23=MOD(LSG,4)
      L3=L23/2
      L4=MOD(L23,2)
      MARK=2+4*L2
      MIKE=1+2*L3+4*L2
      B2=FLOAT(L2)
      B3=FLOAT(L3)
      B4=FLOAT(L4)
      IF(I.EQ.2) GO TO 2
      V2=VX(4)-OVDR
      D2=V2*(1.-B2)+VR*B2
      S2=V2*B2+VRN*(1.-B2)
      V3=VX(MARK)-OVDR*B2+OVDR*(1.-B2)
      D3=V3*(1.-B3)+VR*B3
      S3=V3*B3+VRN*(1.-B3)
      V4=VX(MIKE)-OVDR*B3+OVDR*(1.-B3)
      D4=V4*(1.-B4)+VR*B4
      S4=V4*B4+VRN*(1.-B4)
      T=VX(MIKE)-CX(J)*VR*(1.-B4)
      V5=T+CX(J)*VY(8)-OVDR*B4+OVDR*(1.-B4)
      GO TO 3
    2 V2=VXN(4)+OVDR
      S2=V2*(1.-B2)+VRN*B2
      D2=V2*B2+VR*(1.-B2)
      V3=VXN(MARK)-OVDR*(1.-B2)+OVDR*B2
      S3=V3*(1.-B3)+VRN*B3
      D3=V3*B3+VR*(1.-B3)
```

```
      V4=VXN(MIKE)-OVDR*(1.-B3)+OVDR*B3
      S4=V4*(1.-B4)+VRN*B4
      D4=V4*B4+VR*(1.-B4)
      T=VXN(MIKE)-CX(J)*VRN*(1.-B4)
      V5=T+CX(J)*VYN(8)-OVDR*(1.-B4)+OVDR*B4
    3 DO 1 K=1,16
      LSTP=K-1
      L5=LSTP/8
      L56=MOD(LSTP,8)
      L6=L56/4
      L67=MOD(L56,4)
      L7=L67/2
      L8=MOD(L67,2)
      JACK=4+8*L5
      JIM=2+4*L6+8*L5
      JAN=1+2*L7+4*L6+8*L5
      B5=FLOAT(L5)
      B6=FLOAT(L6)
      B7=FLOAT(L7)
      B8=FLOAT(L8)
      IF(I.EQ.2) GO TO 4
      D5=V5*(1.-B5)+VR*B5
      S5=V5*B5+VRN*(1.-B5)
      V6=T+CX(J)*VY(JACK)-OVDR*B5+OVDR*(1.-B5)
      D6=V6*(1.-B6)+VR*B6
      S6=V6*B6+VRN*(1.-B6)
      V7=T+CX(J)*VY(JIM)-OVDR*B6+OVDR*(1.-B6)
      D7=V7*(1.-B7)+VR*B7
      S7=V7*B7+VRN*(1.-B7)
      V8=T+CX(J)*VY(JAN)-OVDR*B7+OVDR*(1.-B7)
      D8=V8*(1.-B8)+VR*B8
      S8=V8*B8+VRN*(1.-B8)
      GO TO 5
    4 S5=V5*(1.-B5)+VRN*B5
      D5=V5*B5+VR*(1.-B5)
      V6=T+CX(J)*VYN(JACK)-OVDR*(1.-B5)+OVDR*B5
      S6=V6*(1.-B6)+VRN*B6
      D6=V6*B6+VR*(1.-B6)
      V7=T+CX(J)*VYN(JIM )-OVDR*(1.-B6)+OVDR*B6
      S7=V7*(1.-B7)+VRN*B7
      D7=V7*B7+VR*(1.-B7)
      V8=T+CX(J)*VYN(JAN)-OVDR*(1.-B7)+OVDR*B7
      S8=V8*(1.-B8)+VRN*B8
      D8=V8*B8+VR*(1.-B8)
    5 CONTINUE
```

```
      DREPT=AMIN1(D2,D3,D4,D5,D6,D7,D8)
      STING=AMAX1(S2,S3,S4,S5,S6,S7,S8)
      IF((I.EQ.1).AND.(STING.LT.0.)) STING=0.
      IF((I.EQ.1).AND.(DREPT.LT.0.)) DREPT=0.
      IF((I.EQ.2).AND.(STING.GT.0.)) STING=0.
      IF((I.EQ.2).AND.(DREPT.GT.0.)) DREPT=0.
      VLO(I,J,K)=2.*XFL
      VUP(I,J,K)=2.*XFL
      IF((I.EQ.1).AND.(J.EQ.8).AND.(K.EQ.16))DREPT=3.*XFL
      IF((I.EQ.2).AND.(J.EQ.8).AND.(K.EQ.16))STING=-3.*XFL
      IF(STING.GT.DREPT) GO TO 1
      VLO(I,J,K)=STING+VOSCEF
      VUP(I,J,K)=DREPT+VOSCEF
    1 CONTINUE
      DO 20 J=1,8
      DO 20 K=1,16
      JR=9-J
      KR=17-K
      IF(VUP(1,JR,KR).NE.2.*XFL) GO TO 20
      IF(KR.NE.16) GO TO 21
      VUP(1,JR,KR)=VLO(1,JR+1,1)
      VLO(1,JR,KR)=VUP(1,JR,KR)
      GO TO 20
   21 VUP(1,JR,KR)=VLO(1,JR,KR+1)
      VLO(1,JR,KR)=VUP(1,JR,KR)
   20 CONTINUE
      DO 22 J=1,8
      DO 22 K=1,16
      JR=9-J
      KR=17-K
      IF(VLO(2,JR,KR).NE.2.*XFL) GO TO 22
      IF(KR.NE.16) GO TO 23
      VLO(2,JR,KR)=VUP(2,JR+1,1)
      VUP(2,JR,KR)=VLO(2,JR,KR)
      GO TO 22
   23 VLO(2,JR,KR)=VUP(2,JR,KR+1)
      VUP(2,JR,KR)=VLO(2,JR,KR)
   22 CONTINUE
      PRC=1.
      RETURN
      END
0 ERRORS COMPILATION COMPLETE
```

```
      SUBROUTINE DISTAC
      COMMON XFL,PRC,PRD
     //CODER/DCXB(8),DCYB(5),DCX(8),DCY(5),DVRN,VOSC,OVERDR,
     /VOSA,GAIN,CXP,CYP,VL(2,8,16),VU(2,8,16)
     //DECOD/DCXBD(8),DCYBD(6),DCXD(8),DCYD(6),DVRND,VOSAY,
     /GAINY,CYPD,VO(2,8,16)
     //VALUES/DBUP,DBLOW,NPA,XPZ(54),SDRDBZ(54),GTRACZ(54),
     /XFUNDZ(54),BOPTZ(54),ZAPZ(54),DBINZ(54),SMARZ(54),
     /GMARZ(54)
      PI=3.1415926
      PI2=PI/2.
      NPB=NPA+1
      QN=FLOAT(NPA)-1.
C     THE 0 DB REFERENCE IS DEFINED AT 3 DB BELOW XFL
      XP=XFL*(10.**(-3./20.))
      DO 2 LG=1,NPB
      IZ=LG-1
      IF(IZ) 200,201,200
  200 ZAPZ(IZ)=0.
  201 CONTINUE
      IF(LG.EQ.1) GO TO 3
      QL=FLOAT(LG)-2.
      DBIN=DBUP+(DBLOW-DBUP)*(QL/QN)
      XP=XFL*(10.**((DBIN-3.)/20.))
    3 X1=0.
      X2=0.
      X3=0.
      BOPT=VO(1,8,16)
      IF(VU(1,8,16).LT.-XP) GO TO 100
      BOPT=VO(2,8,16)
      IF(VL(2,8,16).GT.XP) GO TO 100
      IF(VL(1,1,1).GE.XP) GO TO 4
      IF(VU(1,1,1).LE.XP) GO TO 5
      BOPT=VO(1,1,1)
      IF(VL(1,1,1).LE.-XP) GO TO 100
      XA=PI2-ASIN(VL(1,1,1)/XP)
      XB=SQRT(XP**2-VL(1,1,1)**2)
      X1=X1+VO(1,1,1)*XA
      X2=X2+(VO(1,1,1)**2)*XA
      X3=X3+VO(1,1,1)*XB
      GO TO 4
    5 DO 6 J=1,8
      JLP=J
      DO 6 K=1,16
      KLP=K
```

```
      IF(VL(1,J,K).GT.-XP) GO TO 7
    6 CONTINUE
    7 DO 8 J=1,8
      JUP=J
      DO 8 K=1,16
      KUP=K
      IF(VU(1,J,K).GT.XP) GO TO 9
    8 CONTINUE
    9 KL1=(JLP-1)*16+KLP
      KU1=(JUP-1)*16+KUP-1
      IF(KL1.EQ.1) GO TO 10
      BOPT=VO(1,JUP,KUP)
      IF((KL1-KU1).EQ.2) GO TO 100
      XA=ASIN(VL(1,JLP,KLP)/XP)+PI2
      XB=-SQRT(XP**2-VL(1,JLP,KLP)**2)
      KL1M=KL1-1
      IF(MOD(KL1M,16)) 800,801,800
  800 J=KL1M/16+1
      K=KL1M-16*(J-1)
      GO TO 802
  801 J=KL1M/16
      K=16
  802 XO=VO(1,J,K)
      X1=X1+XO*XA
      X2=X2+(XO**2)*XA
      X3=X3+XO*XB
      IF((KL1-KU1).EQ.1) GO TO 12
   10 DO 11 I=KL1,KU1
      IF(MOD(I,16)) 803,804,803
  803 J=I/16+1
      K=I-16*(J-1)
      GO TO 805
  804 J=I/16
      K=16
  805 XA=ASIN(VU(1,J,K)/XP)-ASIN(VL(1,J,K)/XP)
      XB=SQRT(XP**2-VL(1,J,K)**2)-SQRT(XP**2-VU(1,J,K)**2)
      X1=X1+VO(1,J,K)*XA
      X2=X2+(VO(1,J,K)**2)*XA
   11 X3=X3+VO(1,J,K)*XB
   12 XA=PI2-ASIN(VL(1,JUP,KUP)/XP)
      XB=SQRT(XP**2-VL(1,JUP,KUP)**2)
      X1=X1+VO(1,JUP,KUP)*XA
      X2=X2+(VO(1,JUP,KUP)**2)*XA
      X3=X3+VO(1,JUP,KUP)*XB
    4 IF(VU(2,1,1).LE.-XP) GO TO 101
```

```
      IF(VL(2,1,1).GE.-XP) GO TO 13
      BOPT=VO(2,1,1)
      IF(VU(2,1,1).GE.XP) GO TO 100
      XA=ASIN(VU(2,1,1)/XP)+PI2
      XB=-SQRT(XP**2-VU(2,1,1)**2)
      X1=X1+VO(2,1,1)*XA
      X2=X2+(VO(2,1,1)**2)*XA
      X3=X3+VO(2,1,1)*XB
      GO TO 101
   13 DO 14 J=1,8
      JUN=J
      DO 14 K=1,16
      KUN=K
      IF(VU(2,J,K).LT.XP) GO TO 15
   14 CONTINUE
   15 DO 16 J=1,8
      JLN=J
      DO 16 K=1,16
      KLN=K
      IF(VL(2,J,K).LT.-XP) GO TO 17
   16 CONTINUE
   17 KL2=(JLN-1)*16+KLN-1
      KU2=(JUN-1)*16+KUN
      IF(KU2.EQ.1) GO TO 18
      BOPT=VO(2,JLN,KLN)
      IF((KU2-KL2).EQ.2) GO TO 100
      XA=PI2-ASIN(VU(2,JUN,KUN)/XP)
      XB=SQRT(XP**2-VU(2,JUN,KUN)**2)
      KU2M=KU2-1
      IF(MOD(KU2M,16)) 806,807,806
  806 J=KU2M/16+1
      K=KU2M-16*(J-1)
      GO TO 808
  807 J=KU2M/16
      K=16
  808 XO=VO(2,J,K)
      X1=X1+XO*XA
      X2=X2+(XO**2)*XA
      X3=X3+XO*XB
      IF((KU2-KL2).EQ.1) GO TO 20
   18 DO 19 I=KU2,KL2
      IF(MOD(I,16)) 809,810,809
  809 J=I/16+1
      K=I-16*(J-1)
      GO TO 811
```

```
  810 J=I/16
      K=16
  811 XA=ASIN(VU(2,J,K)/XP)-ASIN(VL(2,J,K)/XP)
      XB=SQRT(XP**2-VL(2,J,K)**2)-SQRT(XP**2-VU(2,J,K)**2)
      X1=X1+VO(2,J,K)*XA
      X2=X2+(VO(2,J,K)**2)*XA
   19 X3=X3+VO(2,J,K)*XB
   20 XA=ASIN(VU(2,JLN,KLN)/XP)+PI2
      XB=-SQRT(XP**2-VU(2,JLN,KLN)**2)
      X1=X1+VO(2,JLN,KLN)*XA
      X2=X2+(VO(2,JLN,KLN)**2)*XA
      X3=X3+VO(2,JLN,KLN)*XB
C     XA1=E(XO), XA2=E(XO**2),  XA3=E(XI*XO), XA4=E(XI**2)
  101 XA1=X1/PI
      XA2=X2/PI
      XA3=X3/PI
      XA4=(XP**2)/2.
      IF(LG.NE.1) GO TO 21
      GOL=XA3/XA4
      GO TO 2
   21 D=XA2-XA1**2-(XA3**2)/XA4
      S=(XA3**2)/XA4
      SDR=S/D
      SDRDB=10.*ALOG10(SDR)+2.9
      G=XA3/XA4
      GTRAC=20.*ALOG10(G/GOL)
      AGTRAC=ABS(GTRAC)
      XOFUND=G*XP
      BOPT=XA1
  102 SMAR=SDRDB-33.
      IF(DBIN.GE.-30.) GO TO 22
      SMAR=SDRDB-27.-.6*(DBIN+40.)
      IF(DBIN.GE.-40.) GO TO 22
      SMAR=SDRDB-DBIN-67.
   22 GMAR=.5-AGTRAC
      IF(DBIN.GE.-37.) GO TO 23
      GMAR=1.-AGTRAC
   23 IF((DBIN.LE.0.).AND.(DBIN.GE.-45.).AND.(SMAR.LE.0.))
     /ZAPZ(IZ)=1.
      IF((DBIN.LE.3.).AND.(DBIN.GE.-50.).AND.(GMAR.LE.0.))
     /ZAPZ(IZ)=1.
   24 XPZ(IZ)=XP
      SDRDBZ(IZ)=SDRDB
      GTRACZ(IZ)=GTRAC
      XFUNDZ(IZ)=XOFUND
```

```
      BOPTZ(IZ)=BOPT
      DBINZ(IZ)=DBIN
      SMARZ(IZ)=SMAR
      GMARZ(IZ)=GMAR
    2 CONTINUE
  304 CONTINUE
      RETURN
  100 IF(IZ) 300,301,300
  301 DO 303 I=1,NPA
  303 ZAPZ(I)=1.
      GO TO 304
  300 SDRDB=0.
      GTRAC=1.
      AGTRAC=1.
      XOFUND=0.
      GO TO 102
      END
0 ERRORS COMPILATION COMPLETE
```

**********

PROGRAM XCODEC

**********

THE SENSITIVITY TO PARAMETER NO.18 HAS BEEN TESTED
THE VALUES USED FOR PARAMETER NO.18 HAVE BEEN:

| | | |
|---|---|---|
| .030 | | FAILING VALUE |
| .015 | PASSING VALUE | |
| .023 | | FAILING VALUE |
| .019 | | FAILING VALUE |
| .017 | | FAILING VALUE |
| .016 | PASSING VALUE | |
| .016 | | FAILING VALUE |
| .016 | | FAILING VALUE |
| .016 | PASSING VALUE | |

```
*****************************************************************

PROGRAM XCODEC

*****************************************************************
```

THE NONIDEALITIES OF THE PRACTICAL CODER ARE:

```
 1 DCX1    =   0.000
 2 DCX2    =   0.000
 3 DCX4    =   0.000
 4 DCX8    =   0.000
 5 DCX16   =   0.000
 6 DCX32   =   0.000
 7 DCX64   =   0.000
 8 DCX128  =   0.000
 9 CXP     =   0.000
10 DCY1    =   0.000
11 DCY2    =   0.000
12 DCY4    =   0.000
13 DCY8    =   0.000
14 DCYTM   =   0.000
15 CYP     =   0.000
16 DVRN    =   0.000
17 VOSC    =   0.000
18 OVERDR  =    .016
19 VOSA    =   0.000
20 DGAIN   =   0.000
```

```
*****************************************************************
PROGRAM XCODEC
*****************************************************************
```

THE NONIDEALITIES OF THE PRACTICAL DECODER ARE:

```
21 DCX1    =   0.000
22 DCX2    =   0.000
23 DCX4    =   0.000
24 DCX8    =   0.000
25 DCX16   =   0.000
26 DCX32   =   0.000
27 DCX64   =   0.000
28 DCX128  =   0.000
29 DCY1    =   0.000
30 DCY2    =   0.000
31 DCY4    =   0.000
32 DCY8    =   0.000
33 DCYTM   =   0.000
34 DCYHS   =   0.000
35 CYP     =   0.000
36 DVRN    =   0.000
37 VOSAY   =   0.000
38 DGAINY  =   0.000
```

**********

PROGRAM XCODEC

**********

THE CODER IS PRACTICAL
THE DECODER IS PRACTICAL

THE 0 DB REFERENCE IS 2.12V AT 3.00V FULL SCALE

**********

| INPUT (V) | INPUT (DB) | SDR C-MES (DB) | GAIN TRCK (DB) | OUTPUT FUNDM (V) | OUTPUT DC (V) | SDR MARGIN (DB) | GTRCK MARGIN (DB) |
|---|---|---|---|---|---|---|---|
| 3.0000 | 3.00 | 41.84 | -.02 | 2.9029 | 0.0000 | UNDEF | .48 |
| 2.6738 | 2.00 | 41.72 | .01 | 2.5941 | -.0000 | UNDEF | .49 |
| 2.3830 | 1.00 | 40.93 | .01 | 2.3130 | .0000 | UNDEF | .49 |
| 2.1238 | 0.00 | 40.71 | 0.00 | 2.0588 | -.0000 | 7.71 | .50 |
| 1.8929 | -1.00 | 39.33 | .02 | 1.8386 | .0000 | 6.33 | .48 |
| 1.6870 | -2.00 | 38.51 | -.00 | 1.6350 | 0.0000 | 5.51 | .50 |
| 1.5036 | -3.00 | 39.80 | .03 | 1.4624 | -.0000 | 6.80 | .47 |
| 1.3401 | -4.00 | 41.78 | -.00 | 1.2986 | .0000 | 8.78 | .50 |
| 1.1943 | -5.00 | 41.21 | .00 | 1.1579 | .0000 | 8.21 | .50 |
| 1.0644 | -6.00 | 40.35 | -.02 | 1.0299 | .0000 | 7.35 | .48 |
| .9487 | -7.00 | 39.84 | .01 | .9211 | .0000 | 6.84 | .49 |
| .8455 | -8.00 | 38.90 | .02 | .8213 | -.0000 | 5.90 | .48 |
| .7536 | -9.00 | 40.27 | .04 | .7336 | .0000 | 7.27 | .46 |
| .6716 | -10.00 | 40.86 | -.01 | .6503 | .0000 | 7.86 | .49 |
| .5986 | -11.00 | 40.58 | -.02 | .5787 | .0000 | 7.58 | .48 |
| .5335 | -12.00 | 39.54 | .01 | .5177 | -.0000 | 6.54 | .49 |
| .4755 | -13.00 | 40.17 | -.01 | .4603 | .0000 | 7.17 | .49 |
| .4238 | -14.00 | 39.89 | .00 | .4110 | .0000 | 6.89 | .50 |
| .3777 | -15.00 | 41.23 | .01 | .3666 | -.0000 | 8.23 | .49 |
| .3366 | -16.00 | 41.56 | -.01 | .3260 | .0000 | 8.56 | .49 |
| .3000 | -17.00 | 40.74 | -.01 | .2905 | -.0000 | 7.74 | .49 |
| .2674 | -18.00 | 40.23 | -.01 | .2588 | .0000 | 7.23 | .49 |
| .2383 | -19.00 | 38.79 | -.01 | .2308 | .0000 | 5.79 | .49 |
| .2124 | -20.00 | 37.90 | -.00 | .2058 | .0000 | 4.90 | .50 |
| .1893 | -21.00 | 37.67 | -.02 | .1831 | .0000 | 4.67 | .48 |
| .1687 | -22.00 | 41.11 | -.02 | .1632 | .0000 | 8.11 | .48 |
| .1504 | -23.00 | 40.19 | -.02 | .1455 | .0000 | 7.19 | .48 |
| .1340 | -24.00 | 39.46 | -.03 | .1295 | -.0000 | 6.46 | .47 |
| .1194 | -25.00 | 38.28 | -.01 | .1156 | .0000 | 5.28 | .49 |
| .1064 | -26.00 | 37.10 | -.06 | .1024 | .0000 | 4.10 | .44 |
| .0949 | -27.00 | 36.57 | -.06 | .0913 | -.0000 | 3.57 | .44 |
| .0846 | -28.00 | 38.10 | .01 | .0821 | -.0000 | 5.10 | .49 |
| .0754 | -29.00 | 38.76 | -.06 | .0725 | .0000 | 5.76 | .44 |
| .0672 | -30.00 | 38.24 | -.10 | .0644 | -.0000 | 5.24 | .40 |
| .0599 | -31.00 | 36.67 | -.07 | .0575 | .0000 | 4.27 | .43 |

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PROGRAM XCODEC

**********

THE CODER IS PRACTICAL
THE DECODER IS PRACTICAL

THE 0 DB REFERENCE IS 2.12V AT 3.00V FULL SCALE

**********

| INPUT (V) | INPUT (DB) | SDR C-MES (DB) | GAIN TRCK (DB) | OUTPUT FUNDM (V) | OUTPUT DC (V) | SDR MARGIN (DB) | GTRCK MARGIN (DB) |
|---|---|---|---|---|---|---|---|
| .0533 | -32.00 | 35.39 | -.06 | .0514 | .0000 | 3.59 | .44 |
| .0475 | -33.00 | 34.78 | -.16 | .0453 | .0000 | 3.58 | .34 |
| .0424 | -34.00 | 34.89 | -.13 | .0405 | .0000 | 4.29 | .37 |
| .0378 | -35.00 | 35.22 | -.14 | .0360 | -.0000 | 5.22 | .36 |
| .0337 | -36.00 | 33.96 | -.05 | .0324 | .0000 | 4.56 | .45 |
| .0300 | -37.00 | 33.46 | -.08 | .0288 | -.0000 | 4.66 | .42 |
| .0267 | -38.00 | 32.58 | -.23 | .0252 | .0000 | 4.38 | .77 |
| .0238 | -39.00 | 31.40 | -.07 | .0229 | -.0000 | 3.80 | .93 |
| .0212 | -40.00 | 30.60 | -.19 | .0201 | -.0000 | 3.60 | .81 |
| .0189 | -41.00 | 30.64 | -.34 | .0176 | .0000 | 4.64 | .66 |
| .0169 | -42.00 | 28.97 | -.23 | .0159 | -.0000 | 3.97 | .77 |
| .0150 | -43.00 | 28.97 | -.54 | .0137 | .0000 | 4.97 | .46 |
| .0134 | -44.00 | 27.95 | -.50 | .0123 | -.0000 | 4.95 | .50 |
| .0119 | -45.00 | 26.99 | -.37 | .0111 | .0000 | 4.99 | .63 |
| .0106 | -46.00 | 25.35 | -.21 | .0101 | .0000 | UNDEF | .79 |
| .0095 | -47.00 | 24.99 | -.48 | .0087 | -.0000 | UNDEF | .52 |
| .0085 | -48.00 | 22.78 | -.45 | .0078 | .0000 | UNDEF | .55 |
| .0075 | -49.00 | 23.63 | -1.00 | .0065 | .0000 | UNDEF | .00 |
| .0067 | -50.00 | 22.11 | -.96 | .0058 | -.0000 | UNDEF | .04 |

**********

PROGRAM XCODEC

**********

THE CODER IS PRACTICAL
THE DECODER IS PRACTICAL
S=SIGN BIT
L=ONES COMPLEMENT OF SEGMENT WORD IN DECIMAL
V=ONES COMPLEMENT OF STEP WORD IN DECIMAL

**********

| S | L | V | INPUT LOWER LIMIT (V) | INPUT UPPER LIMIT (V) | INPUT STEP SIZE (MV) | INPUT MIDDLE POINT (V) | OUTPUT LEVEL (V) | TRACKING ERROR |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0.0000 | .0012 | 1.2 | .0006 | 0.0000 | UNDEF. |
| 1 | 0 | 1 | .0012 | .0020 | .7 | .0016 | .0007 | -1.222 |
| 1 | 0 | 2 | .0020 | .0020 | 0.0 | .0020 | .0014 | -.369 |
| 1 | 0 | 3 | .0020 | .0034 | 1.5 | .0027 | .0021 | -.256 |
| 1 | 0 | 4 | .0034 | .0039 | .5 | .0037 | .0029 | -.289 |
| 1 | 0 | 5 | .0039 | .0039 | 0.0 | .0039 | .0036 | -.102 |
| 1 | 0 | 6 | .0039 | .0047 | .7 | .0043 | .0043 | -.005 |
| 1 | 0 | 7 | .0047 | .0064 | 1.7 | .0055 | .0050 | -.105 |
| 1 | 0 | 8 | .0064 | .0071 | .7 | .0067 | .0057 | -.180 |
| 1 | 0 | 9 | .0071 | .0078 | .7 | .0075 | .0064 | -.164 |
| 1 | 0 | 10 | .0078 | .0078 | 0.0 | .0078 | .0071 | -.099 |
| 1 | 0 | 11 | .0078 | .0083 | .5 | .0081 | .0078 | -.031 |
| 1 | 0 | 12 | .0083 | .0098 | 1.5 | .0091 | .0086 | -.061 |
| 1 | 0 | 13 | .0098 | .0098 | 0.0 | .0098 | .0093 | -.059 |
| 1 | 0 | 14 | .0098 | .0105 | .7 | .0102 | .0100 | -.020 |
| 1 | 0 | 15 | .0105 | .0122 | 1.7 | .0114 | .0107 | -.066 |
| 1 | 1 | 0 | .0122 | .0137 | 1.5 | .0130 | .0118 | -.103 |
| 1 | 1 | 1 | .0137 | .0152 | 1.5 | .0145 | .0132 | -.096 |
| 1 | 1 | 2 | .0152 | .0157 | .5 | .0154 | .0146 | -.056 |
| 1 | 1 | 3 | .0157 | .0181 | 2.4 | .0169 | .0160 | -.054 |
| 1 | 1 | 4 | .0181 | .0196 | 1.5 | .0189 | .0175 | -.080 |
| 1 | 1 | 5 | .0196 | .0201 | .5 | .0199 | .0189 | -.051 |
| 1 | 1 | 6 | .0201 | .0216 | 1.5 | .0208 | .0203 | -.026 |
| 1 | 1 | 7 | .0216 | .0230 | 1.5 | .0223 | .0217 | -.026 |
| 1 | 1 | 8 | .0230 | .0255 | 2.4 | .0243 | .0232 | -.047 |
| 1 | 1 | 9 | .0255 | .0270 | 1.5 | .0262 | .0246 | -.066 |
| 1 | 1 | 10 | .0270 | .0275 | .5 | .0272 | .0260 | -.045 |
| 1 | 1 | 11 | .0275 | .0289 | 1.5 | .0282 | .0275 | -.027 |
| 1 | 1 | 12 | .0289 | .0314 | 2.4 | .0301 | .0289 | -.044 |
| 1 | 1 | 13 | .0314 | .0319 | .5 | .0316 | .0303 | -.043 |
| 1 | 1 | 14 | .0319 | .0333 | 1.5 | .0326 | .0317 | -.028 |
| 1 | 1 | 15 | .0333 | .0358 | 2.4 | .0346 | .0332 | -.042 |

**********

PROGRAM XCODEC

**********

THE CODER IS PRACTICAL
THE DECODER IS PRACTICAL
S=SIGN BIT
L=ONES COMPLEMENT OF SEGMENT WORD IN DECIMAL
V=ONES COMPLEMENT OF STEP WORD IN DECIMAL

**********

| S | L | V | INPUT LOWER LIMIT (V) | INPUT UPPER LIMIT (V) | INPUT STEP SIZE (MV) | INPUT MIDDLE POINT (V) | OUTPUT LEVEL (V) | TRACKING ERROR |
|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 0 | .0358 | .0387 | 2.9 | .0372 | .0353 | -.055 |
| 1 | 2 | 1 | .0387 | .0417 | 2.9 | .0402 | .0381 | -.054 |
| 1 | 2 | 2 | .0417 | .0436 | 2.0 | .0426 | .0410 | -.040 |
| 1 | 2 | 3 | .0436 | .0475 | 3.9 | .0456 | .0439 | -.040 |
| 1 | 2 | 4 | .0475 | .0505 | 2.9 | .0490 | .0467 | -.049 |
| 1 | 2 | 5 | .0505 | .0525 | 2.0 | .0515 | .0496 | -.039 |
| 1 | 2 | 6 | .0525 | .0554 | 2.9 | .0539 | .0524 | -.029 |
| 1 | 2 | 7 | .0554 | .0593 | 3.9 | .0574 | .0553 | -.038 |
| 1 | 2 | 8 | .0593 | .0622 | 2.9 | .0608 | .0581 | -.046 |
| 1 | 2 | 9 | .0622 | .0652 | 2.9 | .0637 | .0610 | -.045 |
| 1 | 2 | 10 | .0652 | .0672 | 2.0 | .0662 | .0638 | -.037 |
| 1 | 2 | 11 | .0672 | .0701 | 2.9 | .0686 | .0667 | -.030 |
| 1 | 2 | 12 | .0701 | .0740 | 3.9 | .0721 | .0695 | -.037 |
| 1 | 2 | 13 | .0740 | .0760 | 2.0 | .0750 | .0724 | -.036 |
| 1 | 2 | 14 | .0760 | .0789 | 2.9 | .0775 | .0752 | -.030 |
| 1 | 2 | 15 | .0789 | .0819 | 2.9 | .0804 | .0781 | -.030 |
| 1 | 3 | 0 | .0819 | .0887 | 6.8 | .0853 | .0824 | -.036 |
| 1 | 3 | 1 | .0887 | .0946 | 5.9 | .0917 | .0881 | -.041 |
| 1 | 3 | 2 | .0946 | .0995 | 4.9 | .0971 | .0938 | -.035 |
| 1 | 3 | 3 | .0995 | .1064 | 6.8 | .1029 | .0995 | -.035 |
| 1 | 3 | 4 | .1064 | .1122 | 5.9 | .1093 | .1052 | -.039 |
| 1 | 3 | 5 | .1122 | .1172 | 4.9 | .1147 | .1109 | -.035 |
| 1 | 3 | 6 | .1172 | .1230 | 5.9 | .1201 | .1166 | -.030 |
| 1 | 3 | 7 | .1230 | .1289 | 5.9 | .1260 | .1223 | -.030 |
| 1 | 3 | 8 | .1289 | .1358 | 6.8 | .1324 | .1280 | -.034 |
| 1 | 3 | 9 | .1358 | .1417 | 5.9 | .1387 | .1337 | -.038 |
| 1 | 3 | 10 | .1417 | .1466 | 4.9 | .1441 | .1394 | -.034 |
| 1 | 3 | 11 | .1466 | .1525 | 5.9 | .1495 | .1451 | -.030 |
| 1 | 3 | 12 | .1525 | .1593 | 6.8 | .1559 | .1508 | -.034 |
| 1 | 3 | 13 | .1593 | .1642 | 4.9 | .1618 | .1565 | -.034 |
| 1 | 3 | 14 | .1642 | .1701 | 5.9 | .1672 | .1622 | -.031 |
| 1 | 3 | 15 | .1701 | .1760 | 5.9 | .1730 | .1679 | -.031 |

**********

PROGRAM XCODEC

**********

THE CODER IS PRACTICAL
THE DECODER IS PRACTICAL
S=SIGN BIT
L=ONES COMPLEMENT OF SEGMENT WORD IN DECIMAL
V=ONES COMPLEMENT OF STEP WORD IN DECIMAL

**********

| S | L | V | INPUT LOWER LIMIT (V) | INPUT UPPER LIMIT (V) | INPUT STEP SIZE (MV) | INPUT MIDDLE POINT (V) | OUTPUT LEVEL (V) | TRACKING ERROR |
|---|---|---|---|---|---|---|---|---|
| 1 | 4 | 0 | .1760 | .1887 | 12.7 | .1824 | .1765 | -.033 |
| 1 | 4 | 1 | .1887 | .2005 | 11.8 | .1946 | .1879 | -.036 |
| 1 | 4 | 2 | .2005 | .2113 | 10.8 | .2059 | .1993 | -.033 |
| 1 | 4 | 3 | .2113 | .2240 | 12.7 | .2176 | .2107 | -.033 |
| 1 | 4 | 4 | .2240 | .2358 | 11.8 | .2299 | .2221 | -.035 |
| 1 | 4 | 5 | .2358 | .2466 | 10.8 | .2412 | .2335 | -.033 |
| 1 | 4 | 6 | .2466 | .2583 | 11.8 | .2525 | .2449 | -.031 |
| 1 | 4 | 7 | .2583 | .2711 | 12.7 | .2647 | .2563 | -.033 |
| 1 | 4 | 8 | .2711 | .2828 | 11.8 | .2770 | .2677 | -.034 |
| 1 | 4 | 9 | .2828 | .2946 | 11.8 | .2887 | .2791 | -.034 |
| 1 | 4 | 10 | .2946 | .3054 | 10.8 | .3000 | .2906 | -.033 |
| 1 | 4 | 11 | .3054 | .3172 | 11.8 | .3113 | .3020 | -.031 |
| 1 | 4 | 12 | .3172 | .3299 | 12.7 | .3235 | .3134 | -.032 |
| 1 | 4 | 13 | .3299 | .3407 | 10.8 | .3353 | .3248 | -.032 |
| 1 | 4 | 14 | .3407 | .3525 | 11.8 | .3466 | .3362 | -.031 |
| 1 | 4 | 15 | .3525 | .3652 | 12.7 | .3588 | .3476 | -.032 |
| 1 | 5 | 0 | .3652 | .3887 | 23.5 | .3770 | .3647 | -.034 |
| 1 | 5 | 1 | .3887 | .4122 | 23.5 | .4005 | .3875 | -.033 |
| 1 | 5 | 2 | .4122 | .4348 | 22.6 | .4235 | .4103 | -.032 |
| 1 | 5 | 3 | .4348 | .4593 | 24.5 | .4471 | .4332 | -.032 |
| 1 | 5 | 4 | .4593 | .4828 | 23.5 | .4711 | .4560 | -.033 |
| 1 | 5 | 5 | .4828 | .5054 | 22.6 | .4941 | .4788 | -.032 |
| 1 | 5 | 6 | .5054 | .5289 | 23.5 | .5172 | .5016 | -.031 |
| 1 | 5 | 7 | .5289 | .5525 | 23.5 | .5407 | .5244 | -.031 |
| 1 | 5 | 8 | .5525 | .5770 | 24.5 | .5647 | .5472 | -.032 |
| 1 | 5 | 9 | .5770 | .6005 | 23.5 | .5887 | .5701 | -.033 |
| 1 | 5 | 10 | .6005 | .6230 | 22.6 | .6118 | .5929 | -.032 |
| 1 | 5 | 11 | .6230 | .6466 | 23.5 | .6348 | .6157 | -.031 |
| 1 | 5 | 12 | .6466 | .6711 | 24.5 | .6588 | .6385 | -.032 |
| 1 | 5 | 13 | .6711 | .6936 | 22.6 | .6824 | .6613 | -.032 |
| 1 | 5 | 14 | .6936 | .7172 | 23.5 | .7054 | .6841 | -.031 |
| 1 | 5 | 15 | .7172 | .7407 | 23.5 | .7289 | .7070 | -.031 |

**********

PROGRAM XCODEC

**********

THE CODER IS PRACTICAL
THE DECODER IS PRACTICAL
S=SIGN BIT
L=ONES COMPLEMENT OF SEGMENT WORD IN DECIMAL
V=ONES COMPLEMENT OF STEP WORD IN DECIMAL

**********

| S | L | V | INPUT LOWER LIMIT (V) | INPUT UPPER LIMIT (V) | INPUT STEP SIZE (MV) | INPUT MIDDLE POINT (V) | OUTPUT LEVEL (V) | TRACKING ERROR |
|---|---|---|---|---|---|---|---|---|
| 1 | 6 | 0 | .7407 | .7887 | 48.0 | .7647 | .7412 | -.032 |
| 1 | 6 | 1 | .7887 | .8358 | 47.1 | .8122 | .7868 | -.032 |
| 1 | 6 | 2 | .8358 | .8819 | 46.1 | .8588 | .8324 | -.032 |
| 1 | 6 | 3 | .8819 | .9299 | 48.0 | .9059 | .8781 | -.032 |
| 1 | 6 | 4 | .9299 | .9770 | 47.1 | .9534 | .9237 | -.032 |
| 1 | 6 | 5 | .9770 | 1.0230 | 46.1 | 1.0000 | .9693 | -.032 |
| 1 | 6 | 6 | 1.0230 | 1.0701 | 47.1 | 1.0466 | 1.0150 | -.031 |
| 1 | 6 | 7 | 1.0701 | 1.1181 | 48.0 | 1.0941 | 1.0606 | -.032 |
| 1 | 6 | 8 | 1.1181 | 1.1652 | 47.1 | 1.1417 | 1.1062 | -.032 |
| 1 | 6 | 9 | 1.1652 | 1.2122 | 47.1 | 1.1887 | 1.1519 | -.032 |
| 1 | 6 | 10 | 1.2122 | 1.2583 | 46.1 | 1.2353 | 1.1975 | -.032 |
| 1 | 6 | 11 | 1.2583 | 1.3054 | 47.1 | 1.2819 | 1.2431 | -.031 |
| 1 | 6 | 12 | 1.3054 | 1.3534 | 48.0 | 1.3294 | 1.2888 | -.032 |
| 1 | 6 | 13 | 1.3534 | 1.3995 | 46.1 | 1.3765 | 1.3344 | -.032 |
| 1 | 6 | 14 | 1.3995 | 1.4466 | 47.1 | 1.4230 | 1.3800 | -.031 |
| 1 | 6 | 15 | 1.4466 | 1.4936 | 47.1 | 1.4701 | 1.4257 | -.031 |
| 1 | 7 | 0 | 1.4936 | 1.5887 | 95.1 | 1.5412 | 1.4941 | -.031 |
| 1 | 7 | 1 | 1.5887 | 1.6828 | 94.1 | 1.6358 | 1.5854 | -.032 |
| 1 | 7 | 2 | 1.6828 | 1.7760 | 93.2 | 1.7294 | 1.6766 | -.031 |
| 1 | 7 | 3 | 1.7760 | 1.8711 | 95.1 | 1.8235 | 1.7679 | -.031 |
| 1 | 7 | 4 | 1.8711 | 1.9652 | 94.1 | 1.9181 | 1.8592 | -.032 |
| 1 | 7 | 5 | 1.9652 | 2.0583 | 93.2 | 2.0118 | 1.9504 | -.031 |
| 1 | 7 | 6 | 2.0583 | 2.1525 | 94.1 | 2.1054 | 2.0417 | -.031 |
| 1 | 7 | 7 | 2.1525 | 2.2466 | 94.1 | 2.1995 | 2.1330 | -.031 |
| 1 | 7 | 8 | 2.2466 | 2.3417 | 95.1 | 2.2941 | 2.2242 | -.031 |
| 1 | 7 | 9 | 2.3417 | 2.4358 | 94.1 | 2.3887 | 2.3155 | -.032 |
| 1 | 7 | 10 | 2.4358 | 2.5289 | 93.2 | 2.4824 | 2.4068 | -.031 |
| 1 | 7 | 11 | 2.5289 | 2.6230 | 94.1 | 2.5760 | 2.4980 | -.031 |
| 1 | 7 | 12 | 2.6230 | 2.7181 | 95.1 | 2.6706 | 2.5893 | -.031 |
| 1 | 7 | 13 | 2.7181 | 2.8113 | 93.2 | 2.7647 | 2.6806 | -.031 |
| 1 | 7 | 14 | 2.8113 | 2.9054 | 94.1 | 2.8583 | 2.7718 | -.031 |
| 1 | 7 | 15 | 2.9054 | 9.0000 | 6094* | 5.9527 | 2.8631 | -1.079 |

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PROGRAM XCODEC

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THE CODER IS PRACTICAL
THE DECODER IS PRACTICAL
S=SIGN BIT
L=ONES COMPLEMENT OF SEGMENT WORD IN DECIMAL
V=ONES COMPLEMENT OF STEP WORD IN DECIMAL

**********

| S | L | V | INPUT LOWER LIMIT (V) | INPUT UPPER LIMIT (V) | INPUT STEP SIZE (MV) | INPUT MIDDLE POINT (V) | OUTPUT LEVEL (V) | TRACKING ERROR |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | -.0012 | 0.0000 | 1.2 | -.0006 | 0.0000 | UNDEF. |
| 0 | 0 | 1 | -.0020 | -.0012 | .7 | -.0016 | -.0007 | -1.222 |
| 0 | 0 | 2 | -.0020 | -.0020 | 0.0 | -.0020 | -.0014 | -.369 |
| 0 | 0 | 3 | -.0034 | -.0020 | 1.5 | -.0027 | -.0021 | -.256 |
| 0 | 0 | 4 | -.0039 | -.0034 | .5 | -.0037 | -.0029 | -.289 |
| 0 | 0 | 5 | -.0039 | -.0039 | 0.0 | -.0039 | -.0036 | -.102 |
| 0 | 0 | 6 | -.0047 | -.0039 | .7 | -.0043 | -.0043 | -.005 |
| 0 | 0 | 7 | -.0064 | -.0047 | 1.7 | -.0055 | -.0050 | -.105 |
| 0 | 0 | 8 | -.0071 | -.0064 | .7 | -.0067 | -.0057 | -.180 |
| 0 | 0 | 9 | -.0078 | -.0071 | .7 | -.0075 | -.0064 | -.164 |
| 0 | 0 | 10 | -.0078 | -.0078 | 0.0 | -.0078 | -.0071 | -.099 |
| 0 | 0 | 11 | -.0083 | -.0078 | .5 | -.0081 | -.0078 | -.031 |
| 0 | 0 | 12 | -.0098 | -.0083 | 1.5 | -.0091 | -.0086 | -.061 |
| 0 | 0 | 13 | -.0098 | -.0098 | 0.0 | -.0098 | -.0093 | -.059 |
| 0 | 0 | 14 | -.0105 | -.0098 | .7 | -.0102 | -.0100 | -.020 |
| 0 | 0 | 15 | -.0122 | -.0105 | 1.7 | -.0114 | -.0107 | -.066 |
| 0 | 1 | 0 | -.0137 | -.0122 | 1.5 | -.0130 | -.0118 | -.103 |
| 0 | 1 | 1 | -.0152 | -.0137 | 1.5 | -.0145 | -.0132 | -.096 |
| 0 | 1 | 2 | -.0157 | -.0152 | .5 | -.0154 | -.0146 | -.056 |
| 0 | 1 | 3 | -.0181 | -.0157 | 2.4 | -.0169 | -.0160 | -.054 |
| 0 | 1 | 4 | -.0196 | -.0181 | 1.5 | -.0189 | -.0175 | -.080 |
| 0 | 1 | 5 | -.0201 | -.0196 | .5 | -.0199 | -.0189 | -.051 |
| 0 | 1 | 6 | -.0216 | -.0201 | 1.5 | -.0208 | -.0203 | -.026 |
| 0 | 1 | 7 | -.0230 | -.0216 | 1.5 | -.0223 | -.0217 | -.026 |
| 0 | 1 | 8 | -.0255 | -.0230 | 2.4 | -.0243 | -.0232 | -.047 |
| 0 | 1 | 9 | -.0270 | -.0255 | 1.5 | -.0262 | -.0246 | -.066 |
| 0 | 1 | 10 | -.0275 | -.0270 | .5 | -.0272 | -.0260 | -.045 |
| 0 | 1 | 11 | -.0289 | -.0275 | 1.5 | -.0282 | -.0275 | -.027 |
| 0 | 1 | 12 | -.0314 | -.0289 | 2.4 | -.0301 | -.0289 | -.044 |
| 0 | 1 | 13 | -.0319 | -.0314 | .5 | -.0316 | -.0303 | -.043 |
| 0 | 1 | 14 | -.0333 | -.0319 | 1.5 | -.0326 | -.0317 | -.028 |
| 0 | 1 | 15 | -.0358 | -.0333 | 2.4 | -.0346 | -.0332 | -.042 |

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PROGRAM XCODEC

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THE CODER IS PRACTICAL
THE DECODER IS PRACTICAL
S=SIGN BIT
L=ONES COMPLEMENT OF SEGMENT WORD IN DECIMAL
V=ONES COMPLEMENT OF STEP WORD IN DECIMAL

**********

| S | L | V | INPUT LOWER LIMIT (V) | INPUT UPPER LIMIT (V) | INPUT STEP SIZE (MV) | INPUT MIDDLE POINT (V) | OUTPUT LEVEL (V) | TRACKING ERROR |
|---|---|---|---|---|---|---|---|---|
| 0 | 2 | 0 | -.0387 | -.0358 | 2.9 | -.0372 | -.0353 | -.055 |
| 0 | 2 | 1 | -.0417 | -.0387 | 2.9 | -.0402 | -.0381 | -.054 |
| 0 | 2 | 2 | -.0436 | -.0417 | 2.0 | -.0426 | -.0410 | -.040 |
| 0 | 2 | 3 | -.0475 | -.0436 | 3.9 | -.0456 | -.0439 | -.040 |
| 0 | 2 | 4 | -.0505 | -.0475 | 2.9 | -.0490 | -.0467 | -.049 |
| 0 | 2 | 5 | -.0525 | -.0505 | 2.0 | -.0515 | -.0496 | -.039 |
| 0 | 2 | 6 | -.0554 | -.0525 | 2.9 | -.0539 | -.0524 | -.029 |
| 0 | 2 | 7 | -.0593 | -.0554 | 3.9 | -.0574 | -.0553 | -.038 |
| 0 | 2 | 8 | -.0622 | -.0593 | 2.9 | -.0608 | -.0581 | -.046 |
| 0 | 2 | 9 | -.0652 | -.0622 | 2.9 | -.0637 | -.0610 | -.045 |
| 0 | 2 | 10 | -.0672 | -.0652 | 2.0 | -.0662 | -.0638 | -.037 |
| 0 | 2 | 11 | -.0701 | -.0672 | 2.9 | -.0686 | -.0667 | -.030 |
| 0 | 2 | 12 | -.0740 | -.0701 | 3.9 | -.0721 | -.0695 | -.037 |
| 0 | 2 | 13 | -.0760 | -.0740 | 2.0 | -.0750 | -.0724 | -.036 |
| 0 | 2 | 14 | -.0789 | -.0760 | 2.9 | -.0775 | -.0752 | -.030 |
| 0 | 2 | 15 | -.0819 | -.0789 | 2.9 | -.0804 | -.0781 | -.030 |
| 0 | 3 | 0 | -.0887 | -.0819 | 6.8 | -.0853 | -.0824 | -.036 |
| 0 | 3 | 1 | -.0946 | -.0887 | 5.9 | -.0917 | -.0881 | -.041 |
| 0 | 3 | 2 | -.0995 | -.0946 | 4.9 | -.0971 | -.0938 | -.035 |
| 0 | 3 | 3 | -.1064 | -.0995 | 6.8 | -.1029 | -.0995 | -.035 |
| 0 | 3 | 4 | -.1122 | -.1064 | 5.9 | -.1093 | -.1052 | -.039 |
| 0 | 3 | 5 | -.1172 | -.1122 | 4.9 | -.1147 | -.1109 | -.035 |
| 0 | 3 | 6 | -.1230 | -.1172 | 5.9 | -.1201 | -.1166 | -.030 |
| 0 | 3 | 7 | -.1289 | -.1230 | 5.9 | -.1260 | -.1223 | -.030 |
| 0 | 3 | 8 | -.1358 | -.1289 | 6.8 | -.1324 | -.1280 | -.034 |
| 0 | 3 | 9 | -.1417 | -.1358 | 5.9 | -.1387 | -.1337 | -.038 |
| 0 | 3 | 10 | -.1466 | -.1417 | 4.9 | -.1441 | -.1394 | -.034 |
| 0 | 3 | 11 | -.1525 | -.1466 | 5.9 | -.1495 | -.1451 | -.030 |
| 0 | 3 | 12 | -.1593 | -.1525 | 6.8 | -.1559 | -.1508 | -.034 |
| 0 | 3 | 13 | -.1642 | -.1593 | 4.9 | -.1618 | -.1565 | -.034 |
| 0 | 3 | 14 | -.1701 | -.1642 | 5.9 | -.1672 | -.1622 | -.031 |
| 0 | 3 | 15 | -.1760 | -.1701 | 5.9 | -.1730 | -.1679 | -.031 |

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PROGRAM XCODEC

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THE CODER IS PRACTICAL
THE DECODER IS PRACTICAL
S=SIGN BIT
L=ONES COMPLEMENT OF SEGMENT WORD IN DECIMAL
V=ONES COMPLEMENT OF STEP WORD IN DECIMAL

**********

| S | L | V | INPUT LOWER LIMIT (V) | INPUT UPPER LIMIT (V) | INPUT STEP SIZE (MV) | INPUT MIDDLE POINT (V) | OUTPUT LEVEL (V) | TRACKING ERROR |
|---|---|---|---|---|---|---|---|---|
| 0 | 4 | 0 | -.1887 | -.1760 | 12.7 | -.1824 | -.1765 | -.033 |
| 0 | 4 | 1 | -.2005 | -.1887 | 11.8 | -.1946 | -.1879 | -.036 |
| 0 | 4 | 2 | -.2113 | -.2005 | 10.8 | -.2059 | -.1993 | -.033 |
| 0 | 4 | 3 | -.2240 | -.2113 | 12.7 | -.2176 | -.2107 | -.033 |
| 0 | 4 | 4 | -.2358 | -.2240 | 11.8 | -.2299 | -.2221 | -.035 |
| 0 | 4 | 5 | -.2466 | -.2358 | 10.8 | -.2412 | -.2335 | -.033 |
| 0 | 4 | 6 | -.2583 | -.2466 | 11.8 | -.2525 | -.2449 | -.031 |
| 0 | 4 | 7 | -.2711 | -.2583 | 12.7 | -.2647 | -.2563 | -.033 |
| 0 | 4 | 8 | -.2828 | -.2711 | 11.8 | -.2770 | -.2677 | -.034 |
| 0 | 4 | 9 | -.2946 | -.2828 | 11.8 | -.2887 | -.2791 | -.034 |
| 0 | 4 | 10 | -.3054 | -.2946 | 10.8 | -.3000 | -.2906 | -.033 |
| 0 | 4 | 11 | -.3172 | -.3054 | 11.8 | -.3113 | -.3020 | -.031 |
| 0 | 4 | 12 | -.3299 | -.3172 | 12.7 | -.3235 | -.3134 | -.032 |
| 0 | 4 | 13 | -.3407 | -.3299 | 10.8 | -.3353 | -.3248 | -.032 |
| 0 | 4 | 14 | -.3525 | -.3407 | 11.8 | -.3466 | -.3362 | -.031 |
| 0 | 4 | 15 | -.3652 | -.3525 | 12.7 | -.3588 | -.3476 | -.032 |
| 0 | 5 | 0 | -.3887 | -.3652 | 23.5 | -.3770 | -.3647 | -.034 |
| 0 | 5 | 1 | -.4122 | -.3887 | 23.5 | -.4005 | -.3875 | -.033 |
| 0 | 5 | 2 | -.4348 | -.4122 | 22.6 | -.4235 | -.4103 | -.032 |
| 0 | 5 | 3 | -.4593 | -.4348 | 24.5 | -.4471 | -.4332 | -.032 |
| 0 | 5 | 4 | -.4828 | -.4593 | 23.5 | -.4711 | -.4560 | -.033 |
| 0 | 5 | 5 | -.5054 | -.4828 | 22.6 | -.4941 | -.4788 | -.032 |
| 0 | 5 | 6 | -.5289 | -.5054 | 23.5 | -.5172 | -.5016 | -.031 |
| 0 | 5 | 7 | -.5525 | -.5289 | 23.5 | -.5407 | -.5244 | -.031 |
| 0 | 5 | 8 | -.5770 | -.5525 | 24.5 | -.5647 | -.5472 | -.032 |
| 0 | 5 | 9 | -.6005 | -.5770 | 23.5 | -.5887 | -.5701 | -.033 |
| 0 | 5 | 10 | -.6230 | -.6005 | 22.6 | -.6118 | -.5929 | -.032 |
| 0 | 5 | 11 | -.6466 | -.6230 | 23.5 | -.6348 | -.6157 | -.031 |
| 0 | 5 | 12 | -.6711 | -.6466 | 24.5 | -.6588 | -.6385 | -.032 |
| 0 | 5 | 13 | -.6936 | -.6711 | 22.6 | -.6824 | -.6613 | -.032 |
| 0 | 5 | 14 | -.7172 | -.6936 | 23.5 | -.7054 | -.6841 | -.031 |
| 0 | 5 | 15 | -.7407 | -.7172 | 23.5 | -.7289 | -.7070 | -.031 |

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PROGRAM XCODEC

**********

THE CODER IS PRACTICAL
THE DECODER IS PRACTICAL
S=SIGN BIT
L=ONES COMPLEMENT OF SEGMENT WORD IN DECIMAL
V=ONES COMPLEMENT OF STEP WORD IN DECIMAL

**********

| S | L | V | INPUT LOWER LIMIT (V) | INPUT UPPER LIMIT (V) | INPUT STEP SIZE (MV) | INPUT MIDDLE POINT (V) | OUTPUT LEVEL (V) | TRACKING ERROR |
|---|---|---|---|---|---|---|---|---|
| 0 | 6 | 0 | -.7887 | -.7407 | 48.0 | -.7647 | -.7412 | -.032 |
| 0 | 6 | 1 | -.8358 | -.7887 | 47.1 | -.8122 | -.7868 | -.032 |
| 0 | 6 | 2 | -.8819 | -.8358 | 46.1 | -.8588 | -.8324 | -.032 |
| 0 | 6 | 3 | -.9299 | -.8819 | 48.0 | -.9059 | -.8781 | -.032 |
| 0 | 6 | 4 | -.9770 | -.9299 | 47.1 | -.9534 | -.9237 | -.032 |
| 0 | 6 | 5 | -1.0230 | -.9770 | 46.1 | -1.0000 | -.9693 | -.032 |
| 0 | 6 | 6 | -1.0701 | -1.0230 | 47.1 | -1.0466 | -1.0150 | -.031 |
| 0 | 6 | 7 | -1.1181 | -1.0701 | 48.0 | -1.0941 | -1.0606 | -.032 |
| 0 | 6 | 8 | -1.1652 | -1.1181 | 47.1 | -1.1417 | -1.1062 | -.032 |
| 0 | 6 | 9 | -1.2122 | -1.1652 | 47.1 | -1.1887 | -1.1519 | -.032 |
| 0 | 6 | 10 | -1.2583 | -1.2122 | 46.1 | -1.2353 | -1.1975 | -.032 |
| 0 | 6 | 11 | -1.3054 | -1.2583 | 47.1 | -1.2819 | -1.2431 | -.031 |
| 0 | 6 | 12 | -1.3534 | -1.3054 | 48.0 | -1.3294 | -1.2888 | -.032 |
| 0 | 6 | 13 | -1.3995 | -1.3534 | 46.1 | -1.3765 | -1.3344 | -.032 |
| 0 | 6 | 14 | -1.4466 | -1.3995 | 47.1 | -1.4230 | -1.3800 | -.031 |
| 0 | 6 | 15 | -1.4936 | -1.4466 | 47.1 | -1.4701 | -1.4257 | -.031 |
| 0 | 7 | 0 | -1.5887 | -1.4936 | 95.1 | -1.5412 | -1.4941 | -.031 |
| 0 | 7 | 1 | -1.6828 | -1.5887 | 94.1 | -1.6358 | -1.5854 | -.032 |
| 0 | 7 | 2 | -1.7760 | -1.6828 | 93.2 | -1.7294 | -1.6766 | -.031 |
| 0 | 7 | 3 | -1.8711 | -1.7760 | 95.1 | -1.8235 | -1.7679 | -.031 |
| 0 | 7 | 4 | -1.9652 | -1.8711 | 94.1 | -1.9181 | -1.8592 | -.032 |
| 0 | 7 | 5 | -2.0583 | -1.9652 | 93.2 | -2.0118 | -1.9504 | -.031 |
| 0 | 7 | 6 | -2.1525 | -2.0583 | 94.1 | -2.1054 | -2.0417 | -.031 |
| 0 | 7 | 7 | -2.2466 | -2.1525 | 94.1 | -2.1995 | -2.1330 | -.031 |
| 0 | 7 | 8 | -2.3417 | -2.2466 | 95.1 | -2.2941 | -2.2242 | -.031 |
| 0 | 7 | 9 | -2.4358 | -2.3417 | 94.1 | -2.3887 | -2.3155 | -.032 |
| 0 | 7 | 10 | -2.5289 | -2.4358 | 93.2 | -2.4824 | -2.4068 | -.031 |
| 0 | 7 | 11 | -2.6230 | -2.5289 | 94.1 | -2.5760 | -2.4980 | -.031 |
| 0 | 7 | 12 | -2.7181 | -2.6230 | 95.1 | -2.6706 | -2.5893 | -.031 |
| 0 | 7 | 13 | -2.8113 | -2.7181 | 93.2 | -2.7647 | -2.6806 | -.031 |
| 0 | 7 | 14 | -2.9054 | -2.8113 | 94.1 | -2.8583 | -2.7718 | -.031 |
| 0 | 7 | 15 | -9.0000 | -2.9054 | 6094* | -5.9527 | -2.8631 | -1.079 |

/FINI

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