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THE DESIGN OPTIMIZATION OF INTEGRATED
BROADBAND AMPLIFIERS

by

Bruce A. Wooley

Memorandum No. ERL-M284

23 September 1970
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CHAPTER I

INTRODUCTION

From an economic standpoint, the circuits best suited to monolithic realization are generally those that can be used as basic functional blocks in a wide range of electronic applications. The field of commercial analog integrated circuits is dominated by a class of circuit of this type—the operational amplifier. There are, however, a number of analog functions, with widespread applications, that cannot be realized effectively with such multipurpose circuits; one of these is broadband lowpass amplification. The bandwidths that can be achieved using operational amplifiers are typically two or more orders of magnitude below those obtainable with amplifier designs intended specifically for broadband performance. For this reason, broadband lowpass amplifiers have emerged as a separate class of single-purpose linear integrated circuit.

In the design of integrated circuits, it is highly desirable to maximize the range of performance specifications that can be met with a single design. For this reason, an extensive design optimization effort is warranted. The emphasis of the work reported in this dissertation is on the development and application of a practical automated design optimization procedure for monolithic broadband amplifiers.

In Chap. II, the basic problems of broadband amplifier design are introduced, and a subclass of such amplifiers is defined by a set of general design requirements. This subclass, namely dc-coupled integrated broadband voltage amplifiers, serves as a focus for the application of
ABSTRACT

A circuit design automation program has been implemented to optimize the design of dc-coupled monolithic broadband amplifiers. In this program, dc conditions, device geometry, and all passive elements are adjusted to obtain the maximum small-signal -3dB bandwidth for a specified gain and quiescent power dissipation. The program is used to compare several basic configurations suitable for broadband monolithic voltage amplification by establishing optimum amplifier designs for each configuration.

The principal subsections of the design optimization program are a frequency response analysis subroutine, a subroutine for determining response sensitivity, and a subroutine for minimizing a scalar function of several variables. The circuit analysis is formulated on a nodal admittance matrix basis and the results are used to generate a scalar index of performance. The gradient of this index is then evaluated from analysis of the response sensitivity to circuit elements. The adjoint network approach is used for this sensitivity analysis. The subroutine for minimizing the performance index is based on the Fletcher-Powell algorithm.

The design program is used to optimize eight complete differential amplifiers developed from basic feedback configurations that are suitable for voltage amplification in integrated circuits. A voltage gain of 34dB and a power dissipation of 96 mW, with ±6V power supplies, are specified for the complete amplifiers. The optimization criterion is to achieve the maximum -3dB bandwidth obtainable without peaking. The results of the
design optimization procedure are used to compare the effectiveness of the basic feedback configurations considered. The best overall performance is obtained for the amplifier based on a series-shunt feedback pair with an emitter-follower included within the feedback loop. This amplifier achieves a bandwidth of 123 MHz for devices with a typical $f_T$ of 580 MHz at collector current of 1 mA. The input resistance of the amplifier is 850 kΩ, the first-order gain variation over the temperature range -55°C to 125°C is .6%. The predicted drift in the dc output level over this temperature is 30 mV, and the available output voltage is ±2.4V for ±6V supplies.
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the design procedures to be described. Basic amplifier configurations suitable for meeting the set of design requirements are also introduced in Chap. II.

In Chap. III, a program for optimizing the design of broadband amplifiers is described. This program significantly increases the number of available degrees of freedom that can be utilized in achieving an optimum design. The program adjusts dc biasing conditions, device geometry, and all passive elements to optimize the small-signal amplifier response. In the work described here, the optimum is defined as the maximum small-signal bandwidth consistent with a specified low-frequency gain and total quiescent power dissipation.

The circuit modeling used in the design optimization procedure is described in Chap. IV. The form of the assumed device structure is presented along with an appropriate small-signal transistor model. The model is characterized on an experimental basis for a typical bipolar integrated circuit processing schedule.

In Chap. V, complete amplifier designs are developed from the basic configurations introduced in Chap. II. Optimum designs are established for each of these amplifiers and are presented in Chapter VI. These designs are used to compare the relative effectiveness of the basic configurations. In Chapter VII, the performance of discrete component and monolithic amplifier realizations is described.
CHAPTER II

THE BROADBAND AMPLIFIER PROBLEM

2.1 Limitations on Performance and Design

The frequency response of a broadband amplifier is limited essentially by the charge storage in active devices and parasitic elements. As a result, a relatively complex circuit model is needed for precise analysis of the response. The nonautomated design of such amplifiers, therefore, usually entails severe analytical approximations and extensive experimental work.

A nonautomated design procedure, for either discrete component or monolithic amplifiers, generally begins with an initial, somewhat arbitrary, design choice. The low-frequency characteristics may be determined precisely for this design, but a rough, first-order estimate must often be used for the bandedge response. Once the initial design choice is made, the amplifier is realized experimentally. In the case of a discrete amplifier, the final design is often arrived at simply by adjusting components of the preliminary realization. However, for monolithic amplifiers such adjustments are rarely feasible. Instead the performance of the preliminary realization is used as a basis for refining the initial analytical approximations and establishing an improved design.

The need for preliminary experimental realizations in a conventional nonautomated design procedure can be eliminated by using precise frequency response analysis to refine the initial design choice. Because of the high cost associated with realizing an integrated design prototype, this substitution of precision analysis for experimental work represents a significant
advantage in design of monolithic amplifiers. The improved analysis capability required for such a substitution is provided by computer-aided circuit analysis. Through automated analysis, it is possible to analyze efficiently circuit models that accurately reflect broadband amplifier performance. Repeated analyses can be performed as a design is modified and, in effect, a sequential form of optimization can be carried out with respect to a small number of design variables.

In a nonautomated design procedure, or in a procedure where only the analysis function is automated, there is little opportunity for optimization in the design of broadband amplifiers. The complexity of the relationship between the amplifier response and the design variables precludes an algebraic approach to optimization. If computer-aided analysis is used, a limited form of optimization can be achieved. However, the procedure is usually restricted to a small number of variables that are considered sequentially, or one-at-a-time. For example, while elements in a feedback network can be adjusted to achieve maximum amplifier bandwidth, convenient but fixed, choices must be made for dc conditions and device geometry. Even with automated analysis, optimization in terms of a substantial number of the available degrees of freedom remains impractical.

To optimize the design of broadband amplifiers with respect to a large number of design parameters, it is necessary to automate a design procedure wherein the parameters are simultaneously adjusted in an iterative numerical search for an optimum. Effective means for directing such a search are available in the form of algorithms for finding the minimum of a scalar multivariable function. In this dissertation, the implementation and application of such a design procedure is presented for a particular class of integrated broadband amplifiers.
2.2 General Design Requirements

The class of amplifier of principal interest in this study is defined by the design requirements given in Table II.1. The first two requirements restrict consideration to circuits that are basically voltage, as opposed to current, amplifiers. Implied in these requirements is the assumption of a low source impedance (50Ω), characteristic of a voltage source. A moderate gain level, in the range of 20 to 40 dB, is typical of amplifiers intended for broadband applications. The amplifier output is of a voltage source nature by virtue of the specification for low output impedance. A high input impedance is specified to minimize interaction with low impedance sources. In addition, the severe mismatching of input and output impedance levels minimizes the interaction between cascaded amplifiers, and the response of such a cascade can be accurately estimated on the basis of individual amplifier characteristics.

The third requirement of Table II.1 is for a low gain sensitivity to both environment (temperature) and processing. As indicated by the next requirement, a standard, junction-isolated, bipolar transistor process is to be used. Thin-film elements are excluded from consideration.

Listed fifth in Table II.1 is a requirement for dc-coupling with zero volt quiescent levels at both input and output. This requirement implies that dc level shifting must be incorporated within the monolithic amplifier; it is then possible to cascade amplifiers directly, without intermediate coupling elements. It is assumed that the zero volt dc output level should be relatively insensitive to both temperature and processing.

The final requirement of Table II.1 is to achieve the maximum -3dB bandwidth, without bandedge peaking, for a given quiescent power dissipation. Satisfaction of this small-signal criterion is the principal objective of the automated optimization procedure.
### TABLE II.1

**DESIGN REQUIREMENTS**

1. Moderate Voltage Gain (34dB)
2. High input and low output impedance levels
3. Low gain sensitivity
4. Standard IC processing
5. DC-coupled with zero volt output level
6. Maximum -3dB bandwidth
2.3 Commercial Amplifiers

A brief description of a number of commercially available integrated amplifiers provides a suitable introduction to basic approaches for meeting the requirements of Table II.1. These amplifiers more-or-less satisfy all of the requirements except that for dc level shifting. All but one of the circuits are based on a feedback approach.

The RCA CA3040 [1] is a differential cascode amplifier with emitter-follower stages at both input and output. The output emitter-follower is needed to meet the low output impedance requirement of Table II.1. The input emitter-follower is used to achieve a high input impedance and to buffer the input stage from the source. The inductive output of this emitter-follower also provides some shunt peaking at the input of the cascode. The performance of the the CA3040 configuration is described in Sec. 2.5.1.

The Fairchild μA733 [2] is a differential amplifier based on a series-shunt local feedback cascade, with an output emitter-follower included in the shunt feedback stage. The basic amplifier configuration is shown in Fig. 2.1(c). As brought out in Sec. 2.4, inclusion of the emitter-follower within the shunt feedback loop eliminates the loading of the feedback resistor at the output of the shunt feedback stage, thereby increasing the loop gain. A high input impedance is achieved in the μA733 through the use of series feedback in the input stage.

Two commercial monolithic broadband amplifiers, the Sylvania SA-20 [3] and the SLG11C [4] from Plessey Microelectronics of England, are based a series-shunt overall feedback pair. As for the μA733, the output emitter-follower is included within the feedback loop. The basic configuration is illustrated in Fig. 2.1(a). Both of the commercial amplifiers are single-ended, rather than differential, circuits.
The Motorola MC1553 [5] is a single-ended broadband amplifier based on a series-series feedback triple driving an output emitter-follower, as shown in Fig. 2.1(e). The design of the MC1553 has been described in detail by Solomon and Wilson [6]. This work is representative of the limits of complexity to which nonautomated broadband amplifier design can be extended.

2.4 A Feedback Approach

As is evident from the above description of commercial monolithic amplifiers, a feedback approach is commonly used to meet requirements similar to those given in Table II.1. Other approaches are possible but, as brought out in Sec. 2.5, these generally fail to satisfy one or more of the requirements.

Eight basic feedback configurations suitable for meeting the requirements of Table II.1 are shown on Fig. 2.1. These configurations are arrived at through consideration of the possible applications of single-loop negative feedback in a cascade of two or three common-emitter gain stages with an output emitter-follower.* At most three gain stages have been considered because this is generally the largest number that can be effectively employed within an overall feedback loop.

In the arriving at the configurations of Fig. 2.1, only series feedback is allowed for the input stage because of the high input impedance requirement. In the cases where two or more feedback loops are cascaded, consideration is restricted to configurations with low interaction between the cascaded loops. For example, the series-shunt pair formed by the first and

---

*A single transistor stage is referred to as a common-emitter stage, even in the presence of series emitter feedback, if the transistor base and collector currents are defined, respectively, as the input and output currents of the stage. Such a stage is capable of providing both voltage and current gain and there is a phase inversion between input and output.
Fig. 2.1: Basic feedback configurations for voltage amplification.
second stages in Fig. 2.1(g) must be followed by a series feedback stage. If a shunt feedback stage were used instead, its low input impedance would severely load, and degrade the performance of, the preceding pair.

An output emitter-follower is included in the configurations of Fig. 2.1, because it is needed in all of the complete amplifier designs developed in Chapter V as a buffer stage and as a means of establishing a low output impedance for the basic amplifier. In all but two of the circuits in Fig. 2.1, the emitter-follower is simply cascaded with a basic feedback configuration. However, in Fig. 2.1 (a) and (c) it has been included within a feedback loop. This inclusion eliminates the loading of the feedback network at the output of the basic amplifier, thereby significantly increasing the loop gain of these configurations relative to the corresponding circuits in Fig. 2.1(b) and (d). As indicated by the results presented in Chapter VI, the increase in loop gain leads to a significant improvement in the optimum performance achievable.

The configurations of Fig. 2.1 represent the basis for the complete amplifier designs developed in Chapter V. A balanced amplifier approach is employed and each of the designs is optimized for a specified gain and power dissipation. The optimization results are presented in Chapter VI and are used to establish the relative effectiveness of the basic configurations for broadband voltage amplification in integrated circuits.

2.5 Alternative Approaches

The feedback approach is not, in general, a necessary one for broadband amplification. Two notable monolithic exceptions to this approach are the RCA CA3040, introduced in Sec. 2.3, and a circuit developed by Gilbert [7]. Both of these amplifiers offer good broadband performance
under certain conditions but are not suitable for meeting all of the requirements of Table II.1.

2.5.1 The CA3040

The basic configuration of the CA3040 is shown in Fig. 2.2, along with the corresponding ac differential-mode half circuit [8]. The low-frequency voltage gain for this amplifier is given approximately by

$$A_v \approx \frac{q}{kT} \left( \frac{I_1}{2} \right) R_1$$

(2.1)

where, as indicated in Fig. 2.2, $I_1$ is the quiescent current supplied to the differential cascode and $R_1 (= R'_1)$ is the differential load resistance for the cascode. In (2.1), $T$ is the absolute temperature in °K, $q$ is the magnitude of the charge on an electron, and $k$ is Boltzmann's constant. To achieve a low gain sensitivity to temperature, the temperature dependence of the source current, $I_1$, must cancel the sensitivities of $R_1$ and $q/kT$. If this is the case, however, the quiescent voltage level at the output of the cascode is relatively sensitive to temperature. This dc level may be approximately expressed as

$$V_{C2} \approx V_{CC} - \frac{1}{2} I_1 R_1$$

(2.2)

where $V_{CC}$ is the positive supply voltage. For a low gain sensitivity, it is necessary to have $I_1 R_1 \propto T$. The corresponding condition in (2.2) is a linear dependence on $T$. As a numerical example, typical design values might be $V_{CC} = 6V$ and $V_{C2} = 3V$ at a nominal temperature of 300°K. For these values, under the condition $I_1 R_1 \propto T$, the dependence of $V_{C2}$ on temperature
Fig. 2.2: (a) Basic configuration of RCA CA3040 wideband amplifier.  
(b) Ac differential-mode half circuit.
Fig. 2.3: Cascode circuit with series feedback.
is

\[ V_{C2} = 6 - \left( \frac{T}{100^\circ K} \right) V \]  \hspace{1cm} (2.3)

Over the temperature range -55°C to 125°C, the total variation in \( V_{C2} \) is 1.8 volts, 60% of the nominal value.

To establish a low temperature sensitivity for \( V_{C2} \), the term \( I_1 R_1 \) in (2.2) must be temperature insensitive. Therefore, the temperature dependence of the current source must be adjusted to cancel that of the diffused resistor, and some other means must be found to reduce the gain sensitivity. One obvious approach is to introduce a series feedback resistor into the cascode, as shown in Fig. 2.3. The low-frequency gain and sensitivity performance of this configuration is essentially the same as that for a single common-emitter stage with local series feedback. As such, the performance is insufficient for meeting the requirements of Table II.1.

2.5.2 The Gilbert "gain cell"

The amplifier shown in Fig. 2.4 is a wideband "gain cell" first described by Gilbert [9]. This circuit is a significant departure from conventional amplifier configurations and can be used to achieve stable gain with a large bandwidth and low distortion. Essentially, a common-base differential stage is connected in shunt with a common-emitter pair; the collector outputs for each pair are connected so that the output signals add in phase. Feedback is not used and the response of the configuration depends primarily on the ratio of the dc biasing currents, \( I_1 \) and \( I_2 \), and the matching between the active devices. The current gain is given by
Fig. 2.4: Gilbert gain cell.
\[
A_I = \frac{i_{\text{out}}}{i_{\text{in}}} = 1 + \frac{I_2}{I_1}
\] (2.4)

if ideal matching is assumed.

The Gilbert circuit is not suitable for meeting the requirements of Table II.1 because, to achieve good performance, it must be loaded by a low impedance. This condition is not compatible with the emitter-follower output stage needed to provide a low output impedance. If a high load impedance is used, the Miller effect capacitance [10] is increased at the input of the common-emitter pair and, in a similar manner, the inductive effect at the input of the common-base devices is increased [11], [12]. As a result, the amplifier bandwidth is reduced and, if the load impedance is high enough, the increased LC product at the input of the gain cell may lead to severe response peaking.
CHAPTER III
AN AUTOMATED DESIGN PROGRAM

3.1 Introduction

In previous work [13], computer-aided analysis has been used extensively in the design of integrated broadband amplifiers. This work was carried out with programs that were currently available for small-signal circuit analysis in the complex frequency domain [14-16]. A number of feedback configurations were considered and the design results provide significant insight into the operation of these amplifiers. However, design optimization could be achieved only in a very limited form, such as the adjustment of compensation elements to provide maximum bandwidth. Convenient, but fixed, choices were made for transistor geometry, dc biasing, and many passive elements. Consequently, a definitive comparison of the basic feedback configurations could not be made. Such a comparison is feasible only if, for a given set of overall design specifications, the best performance obtainable can be established for each configuration under consideration. That is, each of the configurations must be optimized with respect to most, if not all, of the available degrees of design freedom.

In this chapter, a program that has been implemented to optimize the design of monolithic amplifiers is described. The program, ADOP, adjusts transistor geometry, dc operating conditions, and all passive elements to achieve an optimum small-signal amplifier response. Included in the circuit modeling for the program is the nonlinear dependence of the small-signal response on both dc conditions and device geometry. In this dissertation,
the program is used to determine the maximum -3dB bandwidth obtainable for amplifier without peaking; however, the program may be used for optimization with respect to any design criteria that can be related to the small-signal response of a circuit.

The essential requirements for automated circuit design are a scalar performance index, efficient automated circuit analysis, efficient evaluation of the performance index gradient, and an optimization algorithm. In the following sections, each of the requirements is described in detail in relation to the design of monolithic broadband amplifiers. An outline of the program ADOP is presented in Appendix F, a complete listing of the program is given in Appendix G.

3.2 Performance Index

The basic procedure of automated circuit design is an iterative numerical search for the minimum of a scalar performance index. This index is a multivariable function of the design parameters and is formulated such that its minimum corresponds to an optimum design. A least squared error criterion has been used as a performance index for achieving a specified gain and maximum small-signal bandwidth:

\[ E = \sum_{i=1}^{m} W(\omega_i) [|A_{V}(\omega_i)| - A]^2 \]  

(3.1)

where \( \omega_i, i=1, \ldots, m \) is a set of specified frequency points, \( |A_{V}(\omega_i)| \) is the magnitude of the small-signal voltage gain at \( \omega_i \), \( A \) is the specified low-frequency voltage gain, and \( W(\omega_i), i=1, \ldots, m \) is a set of arbitrary, non-negative, scalar weighting parameters. The weighting parameters are included in (3.1) to permit the selective emphasis of various segments of
the amplifier frequency response. For example, to ensure an adequately close realization of the specified gain at dc, the point \( \omega_i = 0 \) may be given a larger weighting than points near the response bandedge.

The points \( \omega_i \) define the frequency range over which the response error is evaluated. The choice of this range is critical if the minimum of the performance index (3.1) is to correspond to the maximum -3dB bandwidth obtainable without peaking. If frequency points are selected too far beyond the amplifier bandedge, the optimization procedure may lead to a heavily peaked response in order to reduce the error beyond the bandedge. Conversely, if the frequency points are limited to a range well below the bandedge, the performance index is relatively insensitive to the response shape at the bandedge and the convergence properties of the iterative optimization procedure may be impaired. The choice of the frequency points, \( \omega_i \), thus requires an approximate knowledge of the amplifier response. This can often be established from a preliminary analysis of the initial design choice in the optimization procedure; at worst, the frequency points can be rechosen after several design iterations.

3.3 Analysis

The performance index (3.1) is related directly to the gain-frequency response, \( A_v(\omega) \). This response is evaluated at each frequency point, \( \omega_i \), through analysis of an appropriate linear, small-signal circuit model. The nonlinear dependence of the response on dc conditions and transistor geometry is incorporated in the elements of the circuit model. A nodal admittance matrix formulation is used for the analysis, and the admittance equations are solved by means of an LU factorization [17-18]. The nodal admittance matrix, \( Y \), is factored into a product of lower and upper triangular matrices, \( L \) and \( U \), using a straightforward Gaussian elimination procedure.
Because of the iterative nature of the automated design procedure, many analyses are needed to arrive at an optimum design. Consequently, the principal factor governing the overall cost of the procedure is the efficiency of the analysis routine. For the designs considered in this work, the typical CPU time required for evaluation of a performance index (3.1) with \( m = 10 \) is 0.2 seconds on a CDC 6400. Sparse matrix techniques have not yet been implemented for solving the admittance equations, but preliminary considerations indicate that such an implementation may result in as much as an order of magnitude reduction in the analysis time.

3.4 Gradient Evaluation

The most effective algorithms for finding the minimum of a multi-variable objective function by direct numerical search generally rely on repeated evaluation of both the function and its gradient. The classical technique for evaluation of the gradient is based on perturbations. Each of the variables is perturbed individually and the corresponding change in the objective function is determined. This information is then used to establish an approximation to the gradient.

For application to practical automated circuit design, the perturbation approach has two serious disadvantages. First, for \( n \) design variables, \( n \) additional analyses are needed for each trial design to determine the performance index gradient. These additional analyses represent an unacceptable increase in computational effort. The second limitation associated with the perturbation approach is the approximate nature of the gradient information. This information is accumulated in the optimization algorithm, and the possible error build-up may seriously degrade the convergence properties of the algorithm.
An approach based on the formulation of the adjoint relations to a set of network equations overcomes both of the disadvantages associated with the perturbation approach [19, 20]. Director and Rohrer have identified these adjoint relations in terms of the so-called linear adjoint network [21-23]. The adjoint network is topologically equivalent to the original circuit under consideration; there is a one-to-one correspondence between branches in the two networks. Under appropriate exitation of the adjoint network, the sensitivity of the performance index (3.1) to any element in a circuit may be expressed as a product of branch responses in the circuit and its adjoint network. Since the design variables are necessarily related to one or more of the circuit elements, evaluation of the performance index sensitivities to these elements leads directly to the gradient of the index with respect to the design variables. The derivation of the adjoint network and its properties is outlined in Appendix A for a restricted case; the derivation for the general case is described thoroughly in the references [21-23].

The adjoint network is an essential concept for practical circuit design automation. Through its use, the additional computational effort required for evaluation of the performance index gradient becomes less than that needed for evaluation of the index itself. It can be shown that the nodal admittance matrix for the adjoint network is simply the transpose of the nodal admittance matrix for the original circuit [24]. Hence, computations performed in decomposing the admittance matrix into an LU form need not be repeated. If

\[ Y = LU \]  

(3.2)

then
\[ \hat{Y} = Y^t = U^t L^t \]  \hspace{1cm} (3.3)

where \( Y \) is the nodal admittance matrix of the original circuit and \( \hat{Y} \) is the admittance matrix of the adjoint network.

The adjoint network approach, in addition to being extremely efficient, also has the advantage of providing a theoretically exact evaluation of the performance index gradient. The precision of the gradient is limited only by the computational machine accuracy.

3.5 Optimization

The direct numerical search for a minimum of a performance function generally consists of repeating a specified sequence of operations for a number of iterations until convergence to the minimum is obtained. The first step at each iteration is to choose a direction for continuing the search. A one-dimensional search is then conducted to locate a minimum of the function in this direction. The directional minimum is taken as the starting point for the next iteration. The procedure has converged when the directional minimum corresponds to a true minimum of the performance function.

When the gradient of the performance function is known, the classical search direction is that of steepest descent (the negative of the gradient direction). However, the steepest descent method exhibits limited convergence ability if the search encounters a narrow valley in n-dimensional surface of the performance function [25]. A number of algorithms have been developed to overcome this limitation; among the most powerful is the method of Fletcher and Powell [26-29]. In the Fletcher-Powell algorithm, the search direction is chosen on the basis of the gradient and an
approximation to the inverse of the matrix of second order derivatives in a Taylor Series expansion of the performance function. The approximation is established from the gradient information of preceding iterations; though necessarily poor at the beginning of the search, it continues to improve as the search proceeds. For the initial iteration, the direction of steepest descent is used. The method of Fletcher and Powell has been used with considerable success in the program ADOP. A brief description of the basis for the method is given in Appendix B.

Once a search direction has been chosen, steps are taken along it until a directional minimum is bounded. A cubic interpolation is then used to locate an approximate minimum. This method was suggested by Fletcher and Powell [30] and has proven satisfactory. No additional effort to locate the directional minimum more accurately appears to be warranted.
CHAPTER IV
MODELING

4.1 Introduction

The precision and effectiveness of any theoretical circuit design procedure depends, in large part, on the models used for the circuit components. The principal benefit of using computer-aided analysis in a design procedure is the capability to deal efficiently with more complex circuit models than could otherwise be considered. In a procedure based on nonautomated circuit analysis, the highly approximate nature of the models that must be used for circuits of a practical complexity limits the precision of theoretical design work and results in the need for extensive experimental work.

Introduced in this chapter are the device structures and models used in the program ADOP for the design optimization of integrated broadband amplifiers. The vertical component geometry is defined by the assumption of a specific diffusion processing schedule. The general form of the planar transistor geometry is described and the design variables associated with this geometry are identified. A small-signal transistor model is then presented and the elements of the model are characterized on the basis of dc conditions, planar geometry, and the assumed processing schedule. Finally, the modeling of the significant parasitic elements associated with passive components is considered.
4.2 **Device Structure**

In this study, a specific bipolar integrated circuit processing schedule is assumed. The schedule is one of those commonly used in the integrated circuits processing facility at the University of California, Berkeley; it results in final base diffusion depth of 3.5 μm, a base diffusion sheet resistance of 125 Ω/square, and a basewidth of 0.8 μm. An epitaxial resistivity of 1 Ω-cm is used. The diffusion depths for this particular processing schedule are somewhat large for high frequency performance and the low base sheet resistance results in a relatively high emitter-base junction transition capacitance. However, the low base sheet resistance is an asset for realizing relatively small resistances in a feedback network and, more importantly, consistently reproducible results have been obtained for the schedule.

The restriction to a particular processing schedule represents the only major arbitrary choice in the design procedure presented in this dissertation. Virtually all other significant degrees of freedom are incorporated actively into the design optimization procedure. The diffusion processing, and consequently the vertical component geometry, has not been included in the procedure because it is presently neither characterized nor controlled well enough to be represented by a set of continuously adjustable design parameters.

The general form assumed for the planar transistor geometry is illustrated by mask geometries shown in Fig. 4.1. The figures are drawn to scale and the minimum allowed values are used for all mask dimensions except the emitter stripe length in Fig. 4.1(b). These minimum dimensions are well within present industrial capabilities.
Fig. 4.1: (a) Minimum area planar device geometry—\( n_a = 1, n_b = 1 \) and minimum emitter stripe length, \( l_e = .6 \) mil.
(b) Device structure with \( n_e = 1, n_b = 2 \) and nonminimum \( l_e \).
The device geometry design parameters are the emitter stripe length, \( l_e \), the number of emitter stripes, \( n_e \), and the number of base contact stripes, \( n_b = (n_e + 1) \) or \( n_e \). These variables govern the dependence of the ohmic resistances \( r_b' \) and \( r_c' \) and junction transition capacitances on the planar geometry; this dependence reflects the principal effect of geometry on the frequency response in the amplifier configurations to be considered. Minimum values are used for all planar dimensions except the emitter stripe length.

The structure shown in Fig. 4.1(a) represents the minimum size device allowed; it has a single base contact and the minimum emitter stripe length, \( l_e = 0.6 \) mil, resulting in a square emitter. Fig. 4.1(b) is an example of a device with \( n_e = 1, n_b = 2 \), and a nonminimum emitter stripe length.

An \( n^+ \) buried layer structure is assumed for all devices. The buried layer is located under the region encompassed by the \( n^+ \) collector contact ring and the base diffusion. The collector contact window may be positioned anywhere along the 0.2 mil wide \( n^+ \) ring without significantly affecting the device characteristics.

### 4.3 A Small-Signal Transistor Model

The small-signal transistor circuit model used in this work is shown in Fig. 4.2. The model is basically a hybrid-\( \pi \) configuration [31-33] with RC \( \pi \)-sections used to represent the distributed base and collector structures. It represents a compromise between precise representation of device performance and modeling complexity. For device design work [34], a far more complicated distributed model [35] may be appropriate; however, such models are hopelessly inefficient for the repeated circuit analyses needed in an automated circuit design procedure. Conversely, the model of Fig. 4.2 is
Fig. 4.2: Small-signal transistor model.
too complex for many nonautomated design problems. If carefully characterized, the model of Fig. 2.4 provides a good representation of small-signal device performance up to frequencies on the order of the common-emitter unity current gain frequency, $f_T$ [36].

The design variables that are associated with the transistor biasing conditions and planar geometry are brought into the design optimization procedure through the elements of the small-signal device model. The characterization of the model elements for the assumed diffusion processing is described below; this characterization is based both on experimental data and first-order geometrical considerations. In the experimental processing facility presently available at Berkeley, the minimum mask dimensions are somewhat larger than those indicated in Fig. 4.1; for example, the smallest emitter stripe width (and length) is 1.6 mil rather than 0.6 mil. As a result, experimental data has, in some cases, been extrapolated to the smaller dimension devices. The resulting characterization is typical of devices that can be realized easily in most commercial processing facilities.

A summary of the device characterization results is presented in Table IV.1. The basis for the characterization is empirical, and a number of the relationships in the table represent the best fit to experimental data. The relationships are not necessarily meaningful from either a physical or theoretical standpoint. In any given design situation, the characterization should be carried out on the basis of the actual processing facility to be used.

Transconductance, $g_m$: The small-signal transconductance of a bipolar transistor is given directly by the well known relationship

$$g_m = \frac{q}{kT} f_C$$ (4.1)
TABLE IV.1

DEVICE CHARACTERIZATION

\[ g_m = \frac{q}{kT} I_C \]
\[ r_T = \beta_0 / g_m \quad , \quad \beta_0 = 120 \]
\[ r_0 = 1 / n g_m \quad , \quad n = .00065 \]
\[ C_{\pi} = C_{je} + g_m \tau_t \quad , \quad \tau_t = .22 \text{ ns} \]
\[ C_{je/\text{Area}} = 1.25 \text{ pF/mil}^2 \]
\[ C_{cb/\text{Area}} = \frac{.11}{(\psi_c - V_{BC})} \text{ pF/mil}^2 \]
\[ C_{cs/\text{Area}} = \frac{.044}{(\psi_s - V_{SC})} \text{ pF/mil}^2 \]

where
\[ \psi_b = .4V \quad k_b = .275 \]
\[ \psi_c = .4V \quad k_s = .34 \]
\[ r^t_b = \frac{1}{n_b} \left[ 210 + \frac{200}{(I_C + 1.3)} \right] \left( \frac{1}{.525 \lambda_e + .15} \right) \Omega \]
\[ r^t_c = 30 \left[ \frac{3.5}{(2.3 + .9n_e + .5n_b + \lambda_e)} + \frac{2}{n_e} \right] \Omega \]

where \( I_C \) is in mA and \( \lambda_e \) is in mils.
where $I_C$ is the quiescent collector current. This parameter is independent of device geometry.

Input resistance, $r_\pi$: The small-signal resistance, $r_\pi$, models the effects which contribute to a nonzero base current in a bipolar transistor. This resistance is given by

$$r_\pi = \frac{\beta_0}{g_m}$$

(4.2)

where $\beta_0$ is the incremental, low-frequency, common-emitter current gain of the device. In the designs to be described, the constant value

$$\beta_0 = 120$$

(4.3)

has been assumed.

The current gain, $\beta_0$, is nominally a function of both biasing and geometry. However, this parameter is governed by recombination mechanisms that are not well characterized and, over the ranges of interest in this study, the dependence on current level and geometry is masked by run-to-run and slice-to-slice variations. In addition, for the amplifiers considered, the response is relatively insensitive to $\beta_0$; this is a necessary condition for any bipolar integrated circuit design that is to be insensitive to temperature and processing.

Output resistance, $r_o$: The small-signal output resistance, $r_o$, models the effect of basewidth modulation [37,38] and may be expressed as

$$r_o = \frac{1}{n g_m}$$

(4.4)

where $n$ is the basewidth modulation factor. A typical value measured for $r_o$ at a collector current of $I_C = 1mA$ is 40 kΩ. This corresponds to a basewidth
modulation factor of

\[ \eta = 0.00065 \] \hspace{1cm} (4.5)

Base resistance, \( r'_b \): The principle influence of the ohmic base resistance, \( r'_b \), in a configuration such as those of Fig. 2.1 is with respect to the bandedge response. For this reason, \( r'_b \) has been evaluated experimentally for a number of devices using the method of high-frequency input impedance measurements [39]; this method leads to values of \( r'_b \) appropriate to the bandedge performance. The method has also been found to yield results that closely agree with noise measurements of \( r'_b \) [40]. A brief description of the method and some typical results are given in Appendix C.

The base resistance is strongly dependent on both geometry and dc current level. Typical measured values for \( r'_b \) as a function quiescent collector current is given in Fig. 4.3 for a minimum area, single base contact device. As indicated in the figure, the dependence of base resistance on current is modeled well by the relationship

\[
\left. r'_b \right|_{\text{min}} = \left[ 210 \Omega + \frac{200}{I_C + 1.3} \right] \Omega \] \hspace{1cm} (4.6)

where \( I_C \) is in mA.

As noted previously, limitations in the available processing system have restricted the minimum planar dimensions for experimental devices to values somewhat larger than those indicated in Fig. 4.1. Consequently, the data of Fig. 4.3 corresponds to a device that has the same form as Fig. 4.1(a) but is scaled upward in size. Nominally, in the presence of dc crowding, such a scaling alters the base resistance, \( r'_b \). However, because of
Figure 4.3: Dependence of base resistance on collector current.

**Fig. 4.3:** Dependence of base resistance on collector current.
counteracting effects associated with the dimensional scaling, it is reasonable to assume that $r'_b$ is not changed substantially. For a given dc current level, an increase in emitter area reduces the dc crowding and tends to increase $r'_b$. At the same time, however, the increase in the emitter stripe length tends to reduce $r'_b$ as long as a significant component of the resistance is associated with the active base region under the emitter. The relatively large magnitudes measured for $r'_b$ indicate that this latter condition is certainly satisfied for the case of Fig. 4.3, even in the region of heavy dc crowding. Thus, the expression (4.6) is assumed to be typical for devices with the dimensions shown in Fig. 4.1(a), as well as for the actual experimental devices. In another design situation, measurements of the effects of dc crowding on $r'_b$ should be made corresponding to the actual processing schedule and mask dimensions to be used.

The expression (4.6) is the characterization assumed for the base resistance of the minimum area device in Fig. 4.1(a). The characterization of $r'_b$ for the general device form is obtained by including the dependence on planar geometry, resulting in

$$
  r'_b = \frac{1}{n_b} \left[ 210 + \frac{200}{(I_C+1.3)} \right] \left( \frac{1}{1.42 \frac{e}{e} + .15} \right) \Omega \tag{4.7}
$$

where $e$ is the emitter stripe length in mils, $I_C$ is the collector current in mA, and $n_b$ is the number of base stripes. The geometrical dependence in (4.7) is arrived at through simple first-order estimates based on the mask dimensions given in Fig. 4.1.

Collector resistance, $r'_c$: For planar geometries such as shown in Fig. 4.1, with an $n^+$ buried layer structure, the principal component of $r'_c$ is the vertical resistance between the $n^+$ collector ring and the buried layer.
In this situation, an appropriate representation of the collector resistance as a function of geometry is

$$r'_c = 30 \left[ \frac{3.5}{2.3 + 0.9n_e + 0.5n_{e,b} + \frac{2}{n_e}} \right] \Omega$$

(4.8)

where $l_e$ is in mils. This relationship corresponds to a resistance of 30Ω for the minimum area geometry of Fig. 4.1(a). The dependence on geometry is relatively weak and for most of the devices to be considered, $r'_c$ is in the range of 25Ω to 30Ω.

Base-emitter Capacitance, $C_{\Pi}$: The base-emitter capacitance, $C_{\Pi}$, represents two components of charge storage and may be expressed as

$$C_{\Pi} = C_{je} + g_m \tau_t$$

(4.9)

The first term in this expression, $C_{je}$, is the transition capacitance of the emitter-base junction. The second term models the storage of injected minority carriers in the base. $\tau_t$ is the transit time of the injected carriers and includes the transit time for both the intrinsic base region and the collector depletion region [41].

For the current levels of interest in this work, the increase in $\tau_t$ at high currents [41,42] may be neglected and a constant value assumed. A typical value of $\tau_t$ for the specified diffusion processing is

$$\tau_t = 0.22 \text{ nsec}$$

(4.10)

This value was determined from measurements of $f_T$ as a function of collector current in the range below that where $\tau_t$ begins to increase.

A plot of the emitter-base transition capacitance per unit area as a
function of voltage, for the specified diffusion schedule, is given in
Fig. 4.4. Based on this data, a value of 1.25 pF/mil$^2$ is assumed for all
devices in the circuits to be considered. The capacitance per unit area
together with the emitter-base junction area is used to determine \( C_{je} \).
The junction area is given by

\[
A_e = n_e (0.93 \xi_e + 0.27) \text{ mil}^2
\]

where \( \xi_e \) is in mils. In establishing (4.11), both lateral diffusion and
sidewall area are considered.

Base-collector Capacitance, \( C_{cb1} \) and \( C_{cb2} \): The collector-base
capacitance may be regarded entirely as the transition capacitance of the
collector-base junction. The basewidth modulation component generally
associated with the collector-base capacitance [44,45], is given by

\[
C_{\eta} = g_m \tau \eta
\]

For the values given above for \( \eta \) (4.5) and \( \tau \) (4.10), the value of \( C_{\eta} \) at a
collector current of 1mA is 0.0055pF. This is completely negligible in
comparison with the transition capacitance.

A plot of collector-base capacitance per unit area as a function of
voltage for a typical device is given in Fig. 4.5. This data is well
fit by the relationship

\[
\frac{C_{cb}}{\text{Area}} = \frac{0.11}{k} \text{ pF/mil}^2
\]

where \( \psi_c = 0.4 \) volts, \( k_c = 0.275 \) and \( V_{BC} \) is in volts. This expression
represents a best fit to experimental data and is not meaningful in terms
Fig. 4.4: Emitter-base transition capacitance per unit area.
Fig. 4.5: Collector-base transition capacitance per unit area.
of an ideal pn junction. The low value of built-in voltage, $\psi_c$, can be used because, for all devices considered, the collector-base junction is reverse biased ($V_{BC}<0$).

The total collector-base capacitance has been modeled with two capacitors, $C_{cb1}$ and $C_{cb2}$, in order to represent the distributed nature of the device structure. The principal component of the base resistance, $r'_b$, occurs in the active base region near the perimeter of the emitter diffusion window. For this reason, the collector-base capacitance is divided on the basis of the junction area associated with the active and passive base regions.

$$C_{cb1} = (C_{cb}/\text{Area})(A_e) \quad (4.14)$$

$$C_{cb2} = (C_{cb}/\text{Area})(A_b-A_e) \quad (4.15)$$

where $A_e$ is the emitter-base junction area, given by (4.11), and $A_b$ is the collector-base junction area, which is given by

$$A_b = (\ell_e + .82)(.9n_e + .5n_b + .52) - .078 \text{ mil}^2 \quad (4.16)$$

where $\ell_e$ is in mils.

Collector-substrate Capacitance, $C_{cs1}$ and $C_{cs2}$: The parasitic collector-substrate transition capacitance is modeled in the same manner as collector-base junction, with two capacitances, $C_{cs1}$ and $C_{cs2}$. Since the major component of $r'_c$ is the resistance between the $n^+$ collector ring and the buried layer, $C_{cs1}$ is regarded as the capacitance associated with the collector region that is shaded in the device layout shown in Fig. 4.6. The junction area corresponding to this region is given by

$$A_{cs1} = (\ell_e + 2.3)(.9n_e + .5n_b + 1.1) \text{ mil}^2 \quad (4.17)$$
Fig. 4.6: Collector area associated with $C_{cs1}$. 
where \( e \) is in mils. The total collector-substrate junction area is given by

\[
A_{cs} = (e + 3.7)(.9n_e + .5n_b + 3.9) - .64 \text{ mil}^2 \tag{4.18}
\]

For both (4.17) and (4.18), lateral diffusion and sidewall area is considered.

A plot of measured values for the collector-substrate capacitance per unit area, corresponding to a typical device, is given in Fig. 4.7. The data is well fit by the expression

\[
\frac{C_{cs}}{\text{Area}} = \frac{0.044}{k_s} \text{pF/mil}^2 \tag{4.19}
\]

where \( \psi_s = .4 \) volts and \( k_s = .34 \). As for the collector-base junction, the collector-substrate junction will always be reversed biased (\( V_{sc} \leq 0 \)) in the designs considered here. The appropriate expressions for \( C_{cs1} \) and \( C_{cs2} \) are

\[
C_{cs1} = \left( \frac{C_{cs}}{\text{Area}} \right) A_{cs1} \tag{4.20}
\]

\[
C_{cs2} = \left( \frac{C_{cs}}{\text{Area}} \right) (A_{cs} - A_{cs1}) \tag{4.21}
\]

For most cases, the collector substrate junction will be heavily reverse biased in the range of 6 to 9 volts and can be reasonably modeled with a voltage independent capacitance per unit area of .06 pF/mil\(^2\).

4.4 Passive Component Parasitics

For the designs considered in this study, the only significant parasitic elements related to passive components are the distributed capacitances associated with the diffused collector load resistors in each amplifier stage. Since one end of these resistors is connected to the
Fig. 4.7: Collector-substrate transition capacitance per unit area.
Fig. 4.8: Modeling of diffused collector load resistors.
(a) Distributed model.
(b) Single-pole approximation.
positive dc supply, or a virtual ground node in a differential configuration, the resistors may be viewed as a resistive one-port, such as shown in Fig. 4.8(a).

If, to a first-order approximation, a uniform capacitance per unit area is assumed, the distributed one-port can be modeled by the single pole network shown in Fig. 4.8(b). In the figure, C is the total capacitance associated with the resistor. This capacitance is given approximately by

\[ C = \frac{R}{\rho_a} A \cdot C_{AV} \]  

(4.22)

where \( \rho_a \) is the sheet resistance of the base diffusion, \( A \) is the junction area of a square of resistance, and \( C_{AV} \) is the average capacitance per unit area. For the assumed processing schedule, \( \rho_a = 125 \ \Omega/\text{square} \), and \( C_{AV} = 0.08 \ \text{pF/mil}^2 \). A typical resistor line width for the collector load resistors is 0.3 mil; for this case \( A = 0.27 \ \text{mil}^2 \) if sidewall area is considered.
5.1 Introduction

The subject of this chapter is the development of complete amplifier designs based on the configurations first introduced in Fig. 2.1. A common overall design approach is used and is adapted individually to each of the basic feedback configurations. The designs are then optimized to provide the maximum -3dB bandwidth consistent with specified gain, power supplies, and power dissipation. The results of the design optimization are presented in Chapter VI and are used to compare the configurations of Fig. 2.1.

The eight basic feedback configurations introduced in Chapter II are repeated in Fig. 5.1, and are identified by the notation P1 through P4 and T1 through T4. The configurations with two common-emitter stages* are henceforth referred to as pairs and are denoted by P1 through P4. Those configurations with three gain stages are referred to as triples and are identified by the notation T1 through T4. For corresponding numbers, such as T1 and P1, the connection of the feedback resistor \( R_f \) is the same in both the pair and the triple. As indicated by Fig. 5.1, the difference between the corresponding pairs and triples is that the third stage in the pair is operated as an emitter follower, while in the triple it is used as a common-emitter gain stage.

*See footnote in Sec. 2.3, pg. 8.
Fig. 5.1: Basic configurations with identifying notation, P1-P4 and T1-T4.
In all of the triples, T1-T4, in Fig. 5.1, and in two of the pairs, P2 and P4, a basic feedback configuration is simply cascaded with the output emitter-follower. However, for the other two pairs, P1 and P3, the emitter-follower is included within a feedback loop. As indicated by the comparison of optimum designs presented in Sec. 6.4, the inclusion of the emitter-follower within a feedback loop results in a significant increase in the maximum achievable bandwidth.

5.2 Overall Design Approach

The general design approach adopted for meeting the requirements of Table II.1 is illustrated in Fig. 5.2. A basic amplifier configuration, enclosed within the dashed lines, is employed in a balanced, or differential, manner and is biased with common-mode current sources such as I₁ and I₂. The emitter-follower of the basic amplifier is incorporated in a dc level shifting stage and an output emitter-follower is added to establish a low output impedance.

A balanced amplifier approach has been used in order to achieve a dc-coupled response with zero volt input and output quiescent levels, temperature and processing insensitive biasing, and a differential input-output capability. As brought below, the common-mode current sources in Fig. 5.2 are realized in manner that establishes relatively insensitive dc voltage levels at the collectors in the basic amplifier configuration.

The balanced amplifier approach permits a partial separation of the dc and ac design problems. Once an optimum set of dc current levels is established from ac considerations, these currents can be easily realized without affecting the differential-mode response of the amplifier. This response is not directly influenced by the nature of the current source realization.
Fig. 5.2: General design approach.
As noted in Chapter II, dc level-shifting must be incorporated within the complete monolithic design. In the approach of Fig. 5.2, the dc voltage level is shifted across the resistor $R_1$. The level shifting network is isolated from the basic amplifier by the emitter-follower $Q_L$ and the dc current in the stages is supplied through the resistor $R_2$. Resistive biasing has been used, despite its associated attenuation, because previous work [46] has demonstrated that this is the only level shifting configuration, compatible with standard monolithic processing, that does not limit the overall amplifier bandwidth. For example, if $R_2$ is replaced with a transistor current source, the attenuation is eliminated but the frequency response is severely degraded by the output capacitance of the current source.

In the following sections, complete amplifier designs based on the configurations of Fig. 5.1 are presented. Designs for the series-series triple, $T_1$, and the series-shunt pair, $P_1$, are first described in detail. The designs for the remaining configurations are then presented with emphasis of features differing from the first two descriptions. All of the designs are developed and optimized on the basis of the principal specifications that are summarized in Table V.1: 1) a differential voltage gain of 34dB, 2) ± 6 V power supplies, and 3) a quiescent power dissipation of 96 mW, corresponding to total dc current of 8 mA between the supplies.

5.3 Series-Series Triple, $T_1$

5.3.1 dc Considerations

Shown in Fig. 5.3 is a complete amplifier with the series-series triple, $T_1$, used as the basic amplifier configuration. Dc currents for the triple are supplied by the common-mode current source configuration of
TABLE V.1
PRINCIPAL OVERALL DESIGN SPECIFICATIONS

1. Differential Voltage Gain = 34dB
2. ±6 V Power Supplies
3. Power Dissipation = 96 mW
Fig. 5.3: Complete amplifier design based on configuration II.
Q_6, Q_7 and R_7. All of the quiescent current for the third stage of the triple, Q_3, is provided by the current source transistor Q_6 and is drained through the feedback resistor, R_f; as a result, this resistor is important from the standpoint of both biasing and gain. The distribution of current among the three stages of the triple is governed by R_f, R_7 and the ratio of currents in Q_6 and Q_7. As is demonstrated in Appendix D, this form of biasing leads to a dc voltage at the collector of Q_3, the output of the triple, that is relatively insensitive to both processing and environment.

The dc collector-emitter voltages of the first two stages in the series-series triple are specified at 1.4V. This specification is also adopted for the first two stages in the other triple (T2-T4) designs, as well as the first stage in all of the pair (P1-P4) designs. These voltages could be incorporated as independent variables in the design optimization procedure; however, little is gained by doing this because of the limited range over which the voltages may be adjusted. For values much below the 1.4V specification, amplifier linearity may be impaired, while significantly larger values limit the available output voltage swing. The collector voltage for the third stage of the triple is determined after consideration of the level shifting and output stage design.

5.3.2 Level Shifting and Output Stages

The dc voltage level in the amplifier of Fig. 5.3 is shifted across the resistor R_4, with the emitter-follower Q_4 isolating the basic triple from the level shifting network. Dc current for the stage is supplied through the resistor R_5 and the common-mode diode string, D_1-D_5. The output emitter-follower, Q_5, provides the required low output impedance and also buffers the level shifting network from the load. Such buffering is needed if
the attenuation in the level shifting stage is to be relatively independent of the load.

The common-mode diode string is used in the level shifting stage to cancel the effects on the quiescent output voltage of changes in the base emitter voltages of $Q_4$ and $Q_5$ with temperature. The basis for this cancellation can be demonstrated through consideration of the generalized n-diode configuration shown in Fig. 5.4. In this figure, $V_{C3}$ corresponds to the voltage at the collector of $Q_5$ in Fig. 5.3. If the transistors $Q_4$ and $Q_5$ and the diodes $D_1-D_5$ are fabricated such that $V_{BE(Q_4)} = V_{BE(Q_5)} = \phi$, then the dc output voltage may be expressed as

$$V_0 = -V_{EE} + (V_{EE} + V_{C3})A_{LV} + \phi\left[n-1-(n+1)A_{LV}\right]$$

(5.1)

where

$$A_{LV} = \frac{R_5}{R_4+R_5}$$

(5.2)

is the small-signal differential voltage transmission of the level shifting stage. The dependence of $V_0$ on the junction voltages in the level shifting and output stages can be eliminated by setting the coefficient of $\phi$ in (5.2) to zero, resulting in the requirement

$$A_{LV} = \frac{n-1}{n+1}$$

(5.3)

Under the condition (5.3), the specified zero volt quiescent output level ($V_0 = 0$) is obtained when

$$V_{C3} = V_{EE}\left(\frac{1}{A_{LV}} - 1\right)$$

(5.4)
Fig. 5.4: Generalized level shifting and output stage configuration.
A zero volt dc output that is relatively insensitive to temperature and processing can be established through a consistent choice of \( n \) and \( V_{C3} \) satisfying (5.3) and (5.4). The output voltage is, however, sensitive to the negative supply voltage, \( V_{EE} \), and the output voltage of the basic amplifier, \( V_{C3} \). As indicated in Appendix D the common-mode current source biasing used for the basic amplifier in Fig. 5.3 results in a voltage for \( V_{C3} \) that is relatively insensitive to temperature and processing.

Several factors must be considered in choosing \( n, V_{C3} \) and \( A_{LV} \). First, \( n \) is obviously restricted to integer values. Second, the voltage \( V_{C3} \) should correspond to a near-maximum available voltage swing at the output of the amplifier. Finally, the voltage transmission, \( A_{LV} \), should be the maximum consistent with the first two considerations.

Values of \( V_{C3} \) and \( A_{LV} \) for several choices of \( n \) are given in Table V.2 for \( \pm 6V \) supplies. For the amplifier of Fig. 5.3, \( n=5 \) has been chosen. This corresponds to a 3V dc level at the collector of \( Q_3 \) and a voltage transmission of .67 for the level shifting stage. The corresponding voltage swing available in the negative direction at the collector of \( Q_3 \) is approximately 2.3V, as determined from the 1.4 volt collector-emitter voltages of the first two stages and the assumption of a base-emitter voltage of .7 volts for \( Q_1, Q_2 \) and \( Q_3 \).

The values of the resistors \( R_4, R_5 \) and \( R_6 \) are determined from the dc current specifications for the level shifting and output stages. The values of the resistors \( R_4 \) and \( R_5 \) must be low enough so that the RC time constant at the base of \( Q_5 \) does not limit the amplifier bandwidth, and the current in the output emitter-follower must be high enough to provide a reasonable output current capability. For the total specified power dissipation of
<table>
<thead>
<tr>
<th>Number of Diodes ( n )</th>
<th>Quiescent Input Voltage Level ( V_{C3'} ) volts</th>
<th>Differential Voltage Transmission ( A_{LV} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>4.0</td>
<td>.60</td>
</tr>
<tr>
<td>5</td>
<td>3.0</td>
<td>.67</td>
</tr>
<tr>
<td>6</td>
<td>2.4</td>
<td>.715</td>
</tr>
<tr>
<td>7</td>
<td>2.0</td>
<td>.75</td>
</tr>
</tbody>
</table>
96mW, 48mW is allotted to the level shifting and output stages. Current levels of 1mA can then be specified for each of the transistors in these stages. The corresponding resistors values are 1.6 kΩ for R₅ and 6.0 kΩ for R₆. The net differential mode resistance from the base of Q₅ to ground is 1.07 kΩ. For these values of resistance, computer-aided analysis has verified that the overall frequency response of any of the designs considered is not limited by the response of the level shifting and output stages.

5.3.3 Frequency Compensation

The level shifting stage, output emitter-follower and the common-mode elements of the amplifier of Fig. 5.3 do not directly affect the overall differential frequency response of the amplifier. Therefore, this response can be determined from analysis of the differential mode half-circuit [47] for the basic triple, shown in Fig. 5.5. Design variables that are not explicitly present as elements of the half-circuit are entered into the design optimization process either through the elements of the small-signal models or as constraints on the half-circuit components. The loading on the triple is represented in the circuit of Fig. 5.5 by the resistor R₃ and the capacitor C₉. The capacitor models both the input capacitance of the level shifting stage and the parasitic capacitance associated with R₃.

The input resistance of the level shifting network is much greater than R₃ and may be neglected.

A common approach to the frequency compensation of feedback configurations such as Fig. 5.5 is to introduce a zero into the feedback transmission (a phantom zero) with a shunt capacitor across the resistor Rₙ [48]. In the series-series triple, however, compensation can instead be established with an effective feedback zero that is inherent in the configuration.
Fig. 5.5: Differential-mode half circuit for the basic triple in the amplifier of Fig. 5.3.
In any circuit with a series feedback connection at the output, the feedback network samples the emitter current of the output transistor rather than the actual output signal ($v_0$ in Fig. 4). This situation results in a zero of the feedback transmission that is given approximately by [49]

$$Z_0 \approx -\frac{1}{R_3 (C_{cb} + C_{cs} + C_L)}$$

(5.5)

where $C_{cb}$ and $C_{cs}$ are the collector-base and collector-substrate capacitances of the output transistor, $Q_3$.

Optimal compensation of the triple can be achieved through suitable choices for the resistor $R_3$ and the capacitor $C_L$. Introduction of a common-mode resistor, $R_g$ in Fig. 5.3, allows $R_3$ to be varied below an upper bound without disturbing the dc conditions. Small values of $R_3$ should, however, be avoided because they limit the available voltage swing at the output of the triple. If necessary, the capacitance $C_L$ can be increased by enlarging the area of the diffused resistor $R_3$; it should not be necessary to add separate capacitive elements for compensation.

5.3.4 Design Variables and Constraints

The variables in the design optimization procedure for the amplifier of Fig. 5.3 are the feedback resistors $R_{e1}$, $R_{e2}$ and $R_f$; the differential collector load resistors, $R_1$, $R_2$ and $R_3$, which can be varied independently of the dc conditions, below an upper bound, through the use of common-mode resistors such as $R_g$; the dc currents in the triple as governed by $R_7$ and the ratio of currents in $Q_6$ and $Q_7$; and the planar geometry variables, described in Chapter IV, for the devices $Q_1$, $Q_2$ and $Q_3$. Design constraints imposed on these variables are: 1) all passive elements must be nonnegative
2) the specified collector-emitter voltage of 1.4V for Q₁ and Q₂, 3) the 3V dc level at the collector of Q₃, as determined by the output stage design, 4) the dc voltage drop across the resistor Rₚ, through which the emitter current of Q₃ is drawn, 5) the upper bound on the differential collector load resistors imposed by dc conditions, 6) a total quiescent current of 2mA for each side of the balanced triple, resulting from the specifications of Table V.1 and the 48mW dissipation in the level shifting and output stages, and 7) a minimum emitter stripe length of 0.6 mil for the devices Q₁, Q₂ and Q₃.

5.4 Series-Shunt Pair, P₁

A complete amplifier based on the series-shunt pair, P₁, is shown in Fig. 5.6. The biasing approach is the same as that used in the amplifier of Fig. 5.3; the common-mode current source supplies the currents for the basic pair and the current drain through Rₚ. As shown in Appendix E, this configuration results in a relatively insensitive quiescent voltage level at the collector of Q₂. Therefore, the same general level shifting and output stage configuration as used for the amplifier of Fig. 5.3 can be employed to achieve an insensitive, zero volt quiescent output level.

The collector-emitter voltage in the first stage of the pair, Q₁, is specified at 1.4V, and the available output voltage swing is determined by voltage at the collector of Q₂. This voltage may be less than the collector voltage of Q₃ in the triple, while a comparable output swing is achieved, because the voltage at the emitter of Q₂ in Fig. 5.6 is less than that at the emitter of Q₃ in Fig. 5.3. Therefore, a six-diode string has been used for the level shifting network in Fig. 5.6. From the data in Table V.2, for n=6, V₉₂=2.4 volts and A₁₉=.715. The use of six diodes increases the
Fig. 5.6: Complete amplifier design based on configuration Pt.
voltage transmission and also reduces the current needed in the level shifting resistors to maintain the same resistance level at the base of the output emitter-follower as was achieved for the triple design. To realize the 1.07 kΩ equivalent resistance from the base of Q₄ to ground in Fig. 5.6, the dc current needed is .667mA and the resistor values are R₃=1.5 kΩ and R₄=3.75 kΩ. As for the triple design, a 1mA current is specified in the output emitter-follower, corresponding to R₅=6 kΩ.

The differential-mode half-circuit suitable for determining the differential frequency response of the amplifier in Fig. 5.6 is given in Fig. 5.7. The emitter-follower, Q₃, is included in the half circuit because it is contained within the feedback loop and, therefore, significantly influences the amplifier response. As indicated in Figs. 5.6 and 5.7, compensation is achieved for the pair with a capacitor, Cₓ, in shunt with the feedback resistor Rₓ. Unlike the series-series triple, the pair cannot, in general, be compensated without the addition of an actual capacitive element.

The design variables for the series-shunt pair amplifier of Fig. 5.6 are the feedback resistors Rₑ and Rₓ, and the feedback capacitance, Cₓ; the differential collector load resistors, R₁ and R₂, which can be adjusted by introducing common-mode resistors; the dc currents in Q₁, and Q₂ and Q₃ as governed by R₆ and the ratio of currents in Q₅ and Q₆; and the device geometry variables for Q₁, Q₂ and Q₃. The design constraints are: 1) all passive elements must be nonnegative, 2) the 1.4V collector-emitter voltage for Q₁, 3) the 2.4 volt dc level at the collector of Q₂, 4) the upper bound on the differential collector load resistances, 5) the dc voltage drop across Rₓ, through which part of the current in Q₃ is drawn, 6) for each
Fig. 5.7: Differential-mode half circuit for the basic pair in the amplifier of Fig. 5.6.
side of the balanced configuration, a total quiescent current of 3mA available to Q₁, Q₂ and Q₃, 7) the drain of .667mA from the emitter current of Q₃ through the level shifting resistors, and 8) a minimum emitter stripe length of 0.6 mil for Q₁, Q₂ and Q₃.

5.5 Other Triple Designs, T2-T4

Complete amplifier designs based on the configurations T2, T3 and T4 are shown in Figs. 5.8, 5.9 and 5.10, respectively. These designs are all quite similar to that presented in Fig. 5.3 for the configuration T1, except that the common-mode current source, Q₈, must be added to supply the current for the third stage transistor, Q₃. Also, the differing connections of the feedback resistor $R_f$ impose different constraints on the variables in the design optimization procedure for each configuration. Frequency compensation, if necessary, can be achieved for the amplifiers of Figs. 5.8 and 5.10 with a shunt capacitance across $R_f$. The shunt-series pair in Fig. 5.9 can be compensated in the same manner as used for the series-series triple in Fig. 5.3; no capacitive element should be needed.

Except for the current source biasing, the dc design is essentially the same for all of the triple amplifiers. A 1.4V collector-emitter voltage is specified for Q₁ and Q₂, and the level shifting and output stage design is identical to that used in the amplifier of Fig. 5.3. As for the amplifier of Fig. 5.3, the current source biasing leads to a relatively insensitive voltage level at the collector of Q₃.

5.5.1 Configuration T2

The amplifier of Fig. 5.8 is based on the feedback configuration T2 in Fig. 5.1. This configuration is a series-shunt overall feedback pair
followed by a local series feedback stage. The dc constraint imposed on
the feedback resistor $R_f$ in Fig. 5.8 is that the current in $R_f$ must be
drawn through the interstage resistor $R_2$. The voltage drop across $R_f$ is
higher, by the base-emitter junction of $Q_3$, than in Fig. 5.3.

5.5.2 Configuration T3

A complete amplifier based on configuration T3 is shown in Fig. 5.9.
For the basic configuration, a local series feedback input stage is followed
by an overall shunt-series feedback pair. If a forward biased base-emitter
voltage of .7 volts is assumed for $Q_2$ and $Q_3$ in Fig. 5.9, then there is no
dc current in $R_f$; hence this resistor may be adjusted without regard to dc
conditions and the constraint associated with $R_f$ in all of the other con-
figurations is eliminated.

5.5.3 Configuration T4

The amplifier in Fig. 5.10 is based on the configuration T4, a series-
shunt-series local feedback cascade. The dc current in the resistor $R_f$
is drawn through the resistor $R_2$ and sunk by the collector of $Q_1$. It is
possible to eliminate the resistor $R_1$ and supply all of the first stage
collector current through $R_f$. This is, in fact, the condition specified by
the design optimization results of the next chapter.

5.6 Other Pair Designs

Shown in Figs. 5.11, 5.12 and 5.13 are complete amplifier designs
based on the pair configurations P2, P3 and P4. These designs are essen-
tially the same as that used for the series-shunt pair in Fig. 5.3, except
for the different connections of the feedback resistor $R_f$. The same form
of current source biasing is used in all of the pair designs and leads to
Fig. 5.8: Complete amplifier design based on configuration T.2.
Fig. 5.9: Complete amplifier design based on configuration T3.
Fig. 5.10: Complete amplifier design based on configuration T4.
an insensitive voltage level at the collector of $Q_2$. A collector-emitter voltage of 1.4V is specified for the first stage transistor, $Q_1$. The level shifting and output stage design in Figs. 5.11 - 5.13 is identical to that used in Fig. 5.6 except that for Figs. 5.11 and 5.13 the current in the emitter follower $Q_3$ does not include the dc current in $R_f$. Frequency compensation can if needed, be established with a shunt capacitor across $R_f$ in all of the configurations.

### 5.6.1 Configuration P2

The amplifier in Fig. 5.11 is based on the configuration P2, a series-shunt overall feedback pair. Unlike the configuration P1, the emitter-follower is not included within the feedback loop. As a result, in Fig. 5.11 the dc voltage drop across $R_f$ is somewhat higher than in Fig. 5.6, and the dc current in $R_f$ must be drawn through the resistor $R_2$. In Fig. 5.11, the current in the emitter-follower $Q_3$ is simply the dc current of .667 mA needed in the level shifting stage. A total current of 2.33 mA is thus available to $Q_1$ and $Q_2$.

### 5.6.2 Configuration P3

The amplifier in Fig. 5.12 is based on configuration P3, a local series-shunt feedback cascade with the emitter-follower $Q_3$ included in the local shunt feedback loop. The current in $R_f$ is drawn from the emitter of $Q_3$ and fed to the collector of $Q_1$. It would be possible to provide all of the first stage collector current through $R_f$; this, however, is not the optimum situation indicated by the results in Sec. 6.2.3.
Fig. 5.12: Complete amplifier design based on configuration P3.
Fig. 5.13: Complete amplifier design based on configuration P4.
5.6.3 Configuration P4

A complete amplifier design based on configuration P4 is shown in Fig. 5.13. The basic configuration is a local series-shunt feedback cascade with the emitter-follower not included in the shunt feedback loop. The dc current in $R_f$ is drawn through $R_2$ rather than from the emitter of $Q_3$. As for the design of Fig. 5.12, the resistor $R_1$ can be eliminated, but the automated design results indicate this is not the optimum design situation.
CHAPTER VI
DESIGN OPTIMIZATION RESULTS

6.1 Introduction

The complete amplifier designs developed in Chapter V have been optimized using the program ADOP to achieve the maximum possible -3dB bandwidth for each design. The results of the optimization procedure are presented in this chapter and are used to compare the effectiveness of the basic feedback configurations first introduced in Chapter II and repeated in Fig. 5.1.

The complete amplifier designs proposed in Chapter V are based on the specification of a 34dB low-frequency voltage gain, ±6 V power supplies, and a total quiescent power dissipation of 96 mW. These specifications represent the overall constraints in the design optimization procedure. Additional constraints arising from dc conditions, device geometry considerations, and the design of the level shifting and output stages are presented in Chapter V in the course of developing the complete amplifier designs.

Two constraints arising from monolithic processing considerations are also included in the design procedure. First, the minimum value allowed for a diffused resistor is 50Ω. This limitation is relevant only to the series emitter feedback resistors; it is imposed because these resistors must match and track other larger feedback resistors if low gain sensitivity to processing and environment is to be achieved. For values below the minimum resistance, contact effects make such matching
increasingly difficult to establish. The second design constraint arising from processing considerations is that the series emitter resistors in the first and third stages of the triples, $T_1 - T_4$, be equal. This condition is imposed to ensure good matching between these relatively small resistors. Since the gain of the triples depends strongly on the four diffused resistors $R_{e1}$, $R_{e2}$, $R_f$, and $R_3$, the constraint $R_{e1} = R_{e2}$ reduces the need for accurately matching unequal resistors from four to three values of resistance.

For the optimum amplifier designs presented in this chapter, the first-order temperature dependence of both the low-frequency voltage gain and quiescent output voltage has been investigated using the nonlinear dc circuit analysis program BIAS-3 [50]. The principal effects considered in the analysis are the first-order temperature sensitivities of the diffused resistors and transistor $\beta_0$'s. Values of 2000 ppm/°C and 6600 ppm/°C at room temperature are assumed, respectively, for these sensitivities [51]; variations in the gain and dc output voltage are then determined over the full temperature range -55°C to 125°C. The assumption of a linear temperature dependence over this full range for the resistances values $\beta_0$ is, of course, in error. However, the deviation from a linear dependence is typically less than 10%; consequently, the analysis does provide a suitable basis for comparing the first-order temperatures sensitivities of the optimum designs. It is reasonable to assume that the temperature dependence in an actual realization of any of the designs is influenced less by nonlinear components of the resistance and $\beta_0$ temperature dependence, than by the variation of resistance ratios with temperature. This latter effect is difficult to predict and can be effectively incorporated in a
design procedure only on the basis of an extensive characterization of the processing to be used.

6.2 Optimum Pair Designs

6.2.1 Configuration PI

The design optimization results for the amplifier of Fig. 5.6, which is based on configuration PI, are summarized in Fig. 6.1 and Tables VI.2a, b and c. The frequency responses represented by the dashed lines in the figure correspond to several designs that were used as starting points in the optimization procedure. Component values and current levels for two of the initial designs (denoted by 1 and 2) are given in Tables VI.2a and b. For both of these initial designs, Q1, Q2 and Q3 are single emitter, single base contact structures with an emitter stripe length of 1.0 mil. All of the design runs converged to the same optimum design. The frequency response for this optimum is indicated by the solid line in Fig. 6.1.

The optimum PI design provides the specified low-frequency voltage gain of 34dB and has -3dB bandwidth of 123 MHz. As indicated in Fig. 6.1, a near maximally flat magnitude frequency response is achieved. The bandwidth is the second largest obtained for designs presented in this chapter; it is exceeded only by the 133 MHz bandwidth of the optimum T3 design. As brought out in the comparison of Sec. 6.4, however, the optimum PI design provides the best overall performance of any of the designs considered.

The passive element values for the optimum PI design are given in Table VI.2a. The values shown for the differential collector load resistances, R1 and R2, are the maximum allowed by dc conditions. This situation is the case for all of the pair designs; consequently, the
Fig. 6.1: Frequency response of optimum design for configuration P1.
### TABLE VI.1a

**COMPONENT VALUES AND CURRENT LEVELS FOR INITIAL DESIGN (1) IN FIG. 6.1**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_e )</td>
<td>250( \Omega )</td>
</tr>
<tr>
<td>( R_f )</td>
<td>2.4( k\Omega )</td>
</tr>
<tr>
<td>( R_1 )</td>
<td>10.6( k\Omega )</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>4.2( k\Omega )</td>
</tr>
<tr>
<td>( C_f )</td>
<td>0</td>
</tr>
<tr>
<td>( I_C(Q_1) )</td>
<td>.5 mA</td>
</tr>
<tr>
<td>( I_C(Q_2) )</td>
<td>.85 mA</td>
</tr>
<tr>
<td>( I_C(Q_3) )</td>
<td>1.65 mA</td>
</tr>
</tbody>
</table>

### TABLE VI.1b

**COMPONENT VALUES AND CURRENT LEVELS FOR INITIAL DESIGN (2) IN FIG. 6.1**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_e )</td>
<td>67( \Omega )</td>
</tr>
<tr>
<td>( R_f )</td>
<td>9.1( k\Omega )</td>
</tr>
<tr>
<td>( R_1 )</td>
<td>5.3( k\Omega )</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>3.4( k\Omega )</td>
</tr>
<tr>
<td>( C_f )</td>
<td>.5 pF</td>
</tr>
<tr>
<td>( I_C(Q_1) )</td>
<td>1 mA</td>
</tr>
<tr>
<td>( I_C(Q_2) )</td>
<td>1.07 mA</td>
</tr>
<tr>
<td>( I_C(Q_3) )</td>
<td>.93 mA</td>
</tr>
</tbody>
</table>

\[
\frac{I_C(Q_2)}{I_C(Q_3)} = 1.75 \\
\frac{I_C(Q_5)}{I_C(Q_6)} = 1.18
\]
### TABLE VI.2a

**Passive Element Values for Optimum PI Design**

<table>
<thead>
<tr>
<th>Element</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_e )</td>
<td>50( \Omega )</td>
</tr>
<tr>
<td>( R_f )</td>
<td>3.5k( \Omega )</td>
</tr>
<tr>
<td>( R_1 )</td>
<td>50k( \Omega )</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>6.2k( \Omega )</td>
</tr>
<tr>
<td>( R_6 )</td>
<td>4.5k( \Omega )</td>
</tr>
<tr>
<td>( C_f )</td>
<td>0.3pF</td>
</tr>
</tbody>
</table>

### TABLE VI.2b

**Device Specifications for Optimum PI Design**

<table>
<thead>
<tr>
<th>Device</th>
<th>( n_e )</th>
<th>( n_b )</th>
<th>( e_{mils} )</th>
<th>( I_C ), mA</th>
<th>( f_t ), MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Q_1 )</td>
<td>1</td>
<td>2</td>
<td>1.07</td>
<td>1.06</td>
<td>580</td>
</tr>
<tr>
<td>( Q_2 )</td>
<td>1</td>
<td>1</td>
<td>0.6</td>
<td>0.58</td>
<td>560</td>
</tr>
<tr>
<td>( Q_3 )</td>
<td>1</td>
<td>1</td>
<td>0.6</td>
<td>1.36</td>
<td>640</td>
</tr>
</tbody>
</table>

\[ I_C(Q_5)/I_C(Q_6) = 2.99 \]

### TABLE VI.2c

**Temperature Dependence of Gain and DC Output Voltage for PI Design**

<table>
<thead>
<tr>
<th>( T ), °K</th>
<th>( A_V(0) )</th>
<th>( V_0 ), mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>218</td>
<td>49.21</td>
<td>-116</td>
</tr>
<tr>
<td>258</td>
<td>49.46</td>
<td>-90</td>
</tr>
<tr>
<td>300</td>
<td>49.52</td>
<td>-88</td>
</tr>
<tr>
<td>348</td>
<td>49.51</td>
<td>-96</td>
</tr>
<tr>
<td>398</td>
<td>49.46</td>
<td>-110</td>
</tr>
</tbody>
</table>
maximum theoretically available voltage swing at the output of these amplifiers is, in all cases, ±2.4 volts.

A compensation capacitance, $C_f$, of 0.3 pF is specified in Table VI.2a. This capacitance can be realized with a base-collector junction area of 5 mil$^2$ under a reverse bias of approximately 6 volts. The P1 amplifier is the only configuration for which a feedback capacitance is needed in the optimum design. The amplifier can be optimized under the constraint $C_f = 0$, but the maximum bandwidth obtainable is then reduced to 100 MHz.

The device specifications for the optimum P1 design are presented in Table VI.2b. The optimum geometry and dc current level are given for each of the transistors $Q_1$, $Q_2$ and $Q_3$, and the transistor $f_T$ corresponding to these conditions is included in the table. Minimum area, single base contact geometries are specified for both $Q_2$ and $Q_3$; the optimum geometry for $Q_1$ is a single emitter, double base contact device with an emitter stripe length of 1.07 mil. Also given in Table VI.2b is the ratio of quiescent currents in the current source transistors, $Q_5$ and $Q_6$, that is needed to establish the optimum distribution of dc current among $Q_1$, $Q_2$ and $Q_3$; the ratio $I_C(Q_5)/I_C(Q_6) = 3.0$ is specified.

Analysis results for the first-order temperature dependence of gain and dc output voltage in the optimum P1 design are given in Table VI.2c. The estimated total variation in the low-frequency voltage gain over the temperature range -55°C to 125°C is only .6% of the gain value at room temperature. This variation is the lowest obtained for the designs considered; it corresponds to an average sensitivity of 33ppm/°C. This very low dependence on temperature is due to a relatively high loop gain for the P1 configuration and to the fortuitous existence of a first-order
zero in the gain sensitivity near room temperature.

The quiescent output voltage of the optimum PI design also exhibits a first-order sensitivity zero near room temperature. As a result, the total variation in this voltage is less than 30 mV over the -55°C to 125°C temperature range. This is the lowest output level drift obtained for any of the amplifiers considered.

6.2.2 Configuration P2

The frequency response of the optimum design for the amplifier in Fig. 5.11, which is based on configuration P2, is included in Fig. 6.2. The maximum bandwidth for this configuration is 95 MHz, the lowest value obtained for any of the designs based on a pair configuration.

The P2 configuration is an overall series-shunt feedback pair where, in contrast to the PI amplifier, the output emitter-follower is not included within the feedback loop. The maximum bandwidth for the P2 design is 23% less than that for the PI configuration, indicating that a substantial improvement is gained by including the emitter-follower within the overall feedback loop.

The passive component values for the optimum P2 design are given in Table VI.3a. As for the other pair designs, the optimum values for R1 and R2 are the maximum allowed by dc conditions. No compensation capacitance is needed for the optimum design.

The device specifications are given in Table VI.3b for the optimum P2 design. As for the PI configuration, minimum area structures are specified for Q2 and Q3, while a single emitter, double base contact device is optimum for Q1. The emitter stripe length for Q1 is 1.23 mil. The ratio of currents in the current source devices is \( I_C(Q_5)/I_C(Q_6) = 2.43 \).
Fig. 6.2: Frequency response of optimum designs for configurations P2, P3, and P4.
TABLE VI.3a
PASSIVE ELEMENT VALUES FOR OPTIMUM P2 DESIGN

<table>
<thead>
<tr>
<th>R_e</th>
<th>R_6</th>
</tr>
</thead>
<tbody>
<tr>
<td>53Ω</td>
<td>3.0kΩ</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>R_f</th>
<th>C_f</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.9kΩ</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R_1</th>
<th>R_2</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1kΩ</td>
<td>2.5kΩ</td>
</tr>
</tbody>
</table>

TABLE VI.3b
DEVICE SPECIFICATIONS FOR OPTIMUM P2 DESIGN

<table>
<thead>
<tr>
<th>Device</th>
<th>n_e</th>
<th>n_b</th>
<th>l_e, mils</th>
<th>I_C, mA</th>
<th>f_t, MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q_1</td>
<td>1</td>
<td>2</td>
<td>1.23</td>
<td>.87</td>
<td>530</td>
</tr>
<tr>
<td>Q_2</td>
<td>1</td>
<td>1</td>
<td>.6</td>
<td>.68</td>
<td>575</td>
</tr>
<tr>
<td>Q_3</td>
<td>1</td>
<td>1</td>
<td>.6</td>
<td>.67</td>
<td>580</td>
</tr>
</tbody>
</table>

I_C(Q_5)/I_C(Q_6) = 2.43

TABLE VI.3c
TEMPERATURE DEPENDENCE OF GAIN AND DC OUTPUT VOLTAGE FOR P2 DESIGN

<table>
<thead>
<tr>
<th>T, °K</th>
<th>A_V(0)</th>
<th>V_0, mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>218</td>
<td>48.99</td>
<td>-350</td>
</tr>
<tr>
<td>258</td>
<td>49.77</td>
<td>-180</td>
</tr>
<tr>
<td>300</td>
<td>49.98</td>
<td>-23</td>
</tr>
<tr>
<td>348</td>
<td>49.94</td>
<td>+138</td>
</tr>
<tr>
<td>398</td>
<td>49.73</td>
<td>+289</td>
</tr>
</tbody>
</table>
The analysis results for the first-order temperature dependence of the P2 design are given in Table VI.3c. The total gain variation over -55°C to 125°C is 2.0% of the nominal value. As for the PI design, a first-order zero in the gain sensitivity exists near room temperature. However, the lower loop gain of the P2 design results in a somewhat larger total variation in the gain. A higher loop gain is obtainable for the PI design because the inclusion of the emitter-follower within the feedback loop significantly reduces the loading of the feedback network on the forward amplifier.

The total drift in the output dc level for the P2 amplifier is 640 mV over the range -55°C to 125°C. This is the largest drift exhibited by any of the designs considered and is more than an order of magnitude greater than that obtained for the PI design.

6.2.3 Configuration P3

The design results for the amplifier for Fig. 5.12, which is based on configuration P3, are given in Fig. 6.2 and Tables VI.4a, b, and c. The basic configuration is a series-shunt cascade with the emitter-follower included in the feedback loop of the shunt stage. The bandwidth of the optimum P3 design is 122 MHz, almost identical to the optimum bandwidth for the PI amplifier. The sensitivity to temperature is, however, considerably higher for the local feedback cascade. The total variation in gain over the range -55°C to 125°C is 10.2% of the room temperature value and the total drift in the dc output voltage level over this temperature range is 190 mV.

The passive elements and device specifications for the optimum P3 design are given in Tables VI.4a and b. The values for $R_1$ and $R_2$ on the
TABLE VI.4a

PASSIVE ELEMENT VALUES FOR OPTIMUM P3 DESIGN

<table>
<thead>
<tr>
<th>Re</th>
<th>Rf</th>
<th>Ri</th>
<th>R6</th>
<th>Cf</th>
</tr>
</thead>
<tbody>
<tr>
<td>50Ω</td>
<td>5.1kΩ</td>
<td>4.9kΩ</td>
<td>2.5kΩ</td>
<td>0</td>
</tr>
</tbody>
</table>

TABLE VI.4b

DEVICE SPECIFICATIONS FOR OPTIMUM P3 DESIGN

<table>
<thead>
<tr>
<th>Device</th>
<th>n_e</th>
<th>n_b</th>
<th>le,mils</th>
<th>Ic, mA</th>
<th>ft,MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>1</td>
<td>2</td>
<td>.92</td>
<td>1.28</td>
<td>590</td>
</tr>
<tr>
<td>Q2</td>
<td>1</td>
<td>1</td>
<td>.6</td>
<td>1.05</td>
<td>516</td>
</tr>
<tr>
<td>Q3</td>
<td>1</td>
<td>1</td>
<td>.6</td>
<td>.86</td>
<td>605</td>
</tr>
</tbody>
</table>

\[ \frac{I_c(Q_5)}{I_c(Q_6)} = 1.21 \]

TABLE VI.4c

TEMPERATURE DEPENDENCE OF GAIN AND DC OUTPUT VOLTAGE FOR P3 DESIGN

<table>
<thead>
<tr>
<th>T, °K</th>
<th>Av(0)</th>
<th>V0,mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>218</td>
<td>51.24</td>
<td>+42</td>
</tr>
<tr>
<td>258</td>
<td>50.58</td>
<td>+8</td>
</tr>
<tr>
<td>300</td>
<td>49.29</td>
<td>-35</td>
</tr>
<tr>
<td>348</td>
<td>47.71</td>
<td>-87</td>
</tr>
<tr>
<td>398</td>
<td>46.11</td>
<td>-144</td>
</tr>
</tbody>
</table>
maximum allowed by dc conditions, and no compensation capacitance is needed for the optimum design. A minimum area geometry is optimum for both Q_2 and Q_3, while a double base contact device is specified for Q_1, with a stripe length of .92 mil. The current ratio in the common-mode transistors Q_5 and Q_6 is $I_C(Q_5)/I_C(Q_6) = 1.21$ for the optimum design.

The difference in performance between the optimum designs based on the P1 and P3 configurations is essentially that expected from a consideration of ideal feedback systems [52]. Though comparable bandwidths are obtainable for similar local and overall feedback configurations, the latter represents a more efficient use of feedback and results in a significantly greater reduction in gain sensitivity.

6.2.4 Configuration P4

The design optimization results for the P4 amplifier of Fig. 5.13 are given in Fig. 6.2 and Tables VI.5 a,b and c. The basic configuration is a local series-shunt cascade followed by an emitter-follower. The bandwidth for the optimum design is 105 MHz, 14% below the maximum bandwidth for the P3 configuration, a local feedback cascade with the emitter follower included in the shunt feedback loop.

The maximum allowed values are optimum for the resistors $R_1$ and $R_2$ in the P3 design. No compensation capacitance is needed. The optimum geometry for the transistor Q_1 is a device with two emitters, three base contacts, and an emitter stripe length of 1.3 mil. A minimum area structure is optimum for Q_2, and for Q_3 a single emitter, single base contact device is specified, with an emitter stripe length of 1.2 mil. The current ratio in the source transistors is $I_C(Q_5)/I_C(Q_6) = 2.44$. 
### TABLE VI.5a

**PASSIVE ELEMENT VALUES FOR OPTIMUM P4 DESIGN**

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_e$</td>
<td>50Ω</td>
<td>$R_f$</td>
<td>5.1kΩ</td>
</tr>
<tr>
<td>$R_f$</td>
<td>5.1kΩ</td>
<td>$R_1$</td>
<td>4.0kΩ</td>
</tr>
<tr>
<td>$R_1$</td>
<td>4.0kΩ</td>
<td>$C_f$</td>
<td>0</td>
</tr>
<tr>
<td>$R_2$</td>
<td>3.6kΩ</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### TABLE VI.5b

**DEVICE SPECIFICATIONS FOR OPTIMUM P4 DESIGN**

<table>
<thead>
<tr>
<th>Device</th>
<th>$n_e$</th>
<th>$n_b$</th>
<th>$l_e$, mils</th>
<th>$I_C$, mA</th>
<th>$f_t$, MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1$</td>
<td>2</td>
<td>3</td>
<td>1.33</td>
<td>1.65</td>
<td>520</td>
</tr>
<tr>
<td>$Q_2$</td>
<td>1</td>
<td>1</td>
<td>0.6</td>
<td>0.68</td>
<td>575</td>
</tr>
<tr>
<td>$Q_3$</td>
<td>1</td>
<td>1</td>
<td>1.22</td>
<td>0.67</td>
<td>520</td>
</tr>
</tbody>
</table>

$I_C(Q_5)/I_C(Q_6) = 2.44$

### TABLE VI.5c

**TEMPERATURE DEPENDENCE OF GAIN AND DC OUTPUT VOLTAGE FOR P4 DESIGN**

<table>
<thead>
<tr>
<th>$T$, °K</th>
<th>$A_V(0)$</th>
<th>$V_0$, mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>218</td>
<td>51.70</td>
<td>+73</td>
</tr>
<tr>
<td>258</td>
<td>51.46</td>
<td>+38</td>
</tr>
<tr>
<td>300</td>
<td>50.40</td>
<td>+1</td>
</tr>
<tr>
<td>348</td>
<td>48.94</td>
<td>-41</td>
</tr>
<tr>
<td>398</td>
<td>47.41</td>
<td>-84</td>
</tr>
</tbody>
</table>
The total variation in the low-frequency voltage gain for the optimum P4 design is 8.6% over the range -55°C to 125°C. The drift in the quiescent output level over this temperature range is 160 mV.

6.3 Optimum Triple Designs

6.3.1 Configuration T1

The amplifier of Fig. 5.3 is based on configuration T1, an overall series-series feedback triple. The design optimization results for this amplifier are given in Fig. 6.3 and Tables VI.6 a, b and c. In the figure, the dashed-line responses correspond to designs used as starting points in the optimization procedure. All of the design runs converged to the optimum, represented by the solid line response.

The optimum design for the T1 amplifier provides the specified voltage gain of 34dB and has a -3dB bandwidth of 90 MHz. This bandwidth is the same as that obtained for the T4 design described in Sec. 6.3.4, but it is substantially below the optimum bandwidth of 133 MHz obtained for the T3 configuration.

Passive element values for the optimum T1 design are listed in Table VI.6a. The values of the differential collector load resistors R1 and R2 are the maximum allowed by dc conditions. For the third stage in triple, the common-mode resistance \( R_8 = 1.1 \, k\Omega \) is introduced to establish the optimum value of 2.1 kΩ for the differential load, \( R_3 \), on the stage. Unlike the second, or output, gain stage in the pairs, the third gain stage in the triples is a series feedback stage. As a result, the load on the stage has an important influence on the frequency response; for all of the triples, the optimum value of \( R_3 \) is less than the maximum permitted by dc conditions. The need for the common-mode resistor \( R_8 \) in all
INITIAL DESIGNS

OPTIMUM DESIGN

-3 dB BW = 90 MHz

FREQUENCY (MHz)

VOLTAGE GAIN (dB)

Fig. 6.3: Frequency response of optimum design for configuration T1.
### TABLE VI.6a

**PASSIVE ELEMENT VALUES FOR OPTIMUM T1 DESIGN**

| R_e1 = R_e2 | 270Ω | R_1 | 11.0kΩ |
| R_f | 2.0kΩ | R_2 | 5.6kΩ |
| R_3 | 2.1kΩ | R_7 | 3.1kΩ |
| C_f | 0 | R_8 | 1.1k |

### TABLE VI.6b

**DEVICE SPECIFICATIONS FOR OPTIMUM T1 DESIGN**

<table>
<thead>
<tr>
<th>Device</th>
<th>n_e</th>
<th>n_b</th>
<th>(e, \text{mils} )</th>
<th>I_C, mA</th>
<th>f_t, MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q_1</td>
<td>1</td>
<td>1</td>
<td>1.05</td>
<td>.48</td>
<td>475</td>
</tr>
<tr>
<td>Q_2</td>
<td>1</td>
<td>1</td>
<td>.93</td>
<td>.83</td>
<td>560</td>
</tr>
<tr>
<td>Q_3</td>
<td>1</td>
<td>1</td>
<td>.69</td>
<td>.69</td>
<td>565</td>
</tr>
</tbody>
</table>

\[ I_C(Q_6)/I_C(Q_7) = 1.35 \]

### TABLE VI.6c

**TEMPERATURE DEPENDENCE OF GAIN AND DC OUTPUT VOLTAGE IN P4 DESIGN**

<table>
<thead>
<tr>
<th>T, °K</th>
<th>A_V(0)</th>
<th>V_0, mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>218</td>
<td>48.67</td>
<td>+118</td>
</tr>
<tr>
<td>258</td>
<td>49.18</td>
<td>+134</td>
</tr>
<tr>
<td>300</td>
<td>49.48</td>
<td>+154</td>
</tr>
<tr>
<td>348</td>
<td>49.65</td>
<td>+187</td>
</tr>
<tr>
<td>398</td>
<td>49.73</td>
<td>+221</td>
</tr>
</tbody>
</table>
of the triple designs limits the available unclipped output voltage swing for these amplifiers to values significantly below the \( \pm 2.4V \) achieved for all of the pair designs described in Sec. 6.2. For the optimum T1 design, the maximum unclipped swing is \( \pm 1.5V \), the largest obtained for any of the triples.

The optimum series emitter resistance, \( R_{e1} = R_{e2} \), for T1 amplifier is \( 270 \Omega \). This is the largest value obtained for any of the designs considered. Because of this relatively large value for the smallest diffused resistors, the optimum T1 design is comparatively easy to realize monolithically. As pointed out in Sec. 5.3, no feedback capacitor is needed to compensate the T1 configuration.

The device specifications for the optimum T1 design are given in Table VI.5b. A single emitter, single base contact structure is optimum for \( Q_1 \), \( Q_2 \) and \( Q_3 \); the emitter stripe lengths are 1.05 mil, .93 mil, and .69 mil, respectively. The ratio of currents in the current source transistors \( Q_6 \) and \( Q_7 \) is \( I_C(Q_6)/I_C(Q_7) = 1.35 \) for the optimum design.

Analysis results for the first-order temperature dependence of gain and output level in the optimum T1 design are given in Table VI.6c. The total gain variation over the temperature range \(-55°C \) to \(125°C \) is 2.1% of the room temperature gain. This is by far the lowest temperature sensitivity obtained for any of the triple designs and reflects the relatively high loop gain obtained with the series-series triple. For all of the other triples, at least two feedback loops are cascaded and the sensitivity to temperature is relatively high.

The total drift in the quiescent output voltage for the T1 design is 100mV over the \(-55°C \) to \(125°C \) range. Of the designs considered, this
performance is exceeded only by the 30 mV drift obtained for the PI configuration.

6.3.2 Configuration T2

The frequency response for the optimum design of the amplifier in Fig. 5.8, which is based on configuration T2, is included in Fig. 6.4. The maximum -3dB bandwidth for this amplifier is 78 MHz, the lowest of the designs considered.

The passive element values for the optimum T2 design are given in Table VI.7a. Because of very low current in the third stage, a high value of $R_g$ is needed and the unclipped output voltage swing is limited to ±0.13 volts.

The low third stage current results from the need to drain a substantial current through the feedback resistor $R_f$. This current is larger for the triple configuration than for the corresponding pair design of Fig. 5.11, even though the latter has a larger voltage drop across $R_f$, because the optimum values for $R_f$ are generally smaller for the triple designs than for the pairs. As for all of the triples, the optimum collector load resistors for the first two stages, $R_1$ and $R_2$, are the maximum permitted by dc conditions; also, no compensation capacitance is needed.

The device characteristics for the optimum T2 design are given in Table VI.7b. A minimum area structure is optimum for all of the devices, $Q_1$, $Q_2$ and $Q_3$, in the basic feedback configuration. Three current source transistors are needed in the T2 amplifier because, unlike the T1 design, a separate current source must be provided for the third stage of the triple. The ratios of quiescent currents in the transistors $Q_6$ and $Q_8$ to the current in the diode connected transistor, $Q_7$, are $I_C(Q_6)/I_C(Q_7) = 3.39$.
Fig. 6.4: Frequency response of optimum designs for configurations T2, T3, and T4.
TABLE VI.7a

PASSIVE ELEMENT VALUES FOR OPTIMUM T2 DESIGN

<table>
<thead>
<tr>
<th>Resistor Values</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>9.3 kΩ</td>
</tr>
<tr>
<td>R2</td>
<td>3.4 kΩ</td>
</tr>
<tr>
<td>R3</td>
<td>1.9 kΩ</td>
</tr>
<tr>
<td>R4</td>
<td>6.0 kΩ</td>
</tr>
<tr>
<td>C1</td>
<td>21.4 kΩ</td>
</tr>
<tr>
<td>R5</td>
<td>2.3 MΩ</td>
</tr>
</tbody>
</table>

TABLE VI.7b

DEVICE SPECIFICATIONS FOR OPTIMUM T2 DESIGN

<table>
<thead>
<tr>
<th>Device</th>
<th>n_e</th>
<th>n_b</th>
<th>I_C, mA</th>
<th>f, MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>1</td>
<td>1</td>
<td>.57</td>
<td>550</td>
</tr>
<tr>
<td>Q2</td>
<td>1</td>
<td>1</td>
<td>.44</td>
<td>520</td>
</tr>
<tr>
<td>Q3</td>
<td>1</td>
<td>1</td>
<td>.07</td>
<td>225</td>
</tr>
</tbody>
</table>

\[
\begin{align*}
I_C(Q_6)/I_C(Q_7) &= 3.39 \\
I_C(Q_8)/I_C(Q_7) &= .152
\end{align*}

TABLE VI.7c

TEMPERATURE DEPENDENCE OF GAIN AND DC OUTPUT VOLTAGE FOR T2 DESIGN

<table>
<thead>
<tr>
<th>Temperature, °K</th>
<th>A_V(0)</th>
<th>V_0, mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>218</td>
<td>58.53</td>
<td>-317</td>
</tr>
<tr>
<td>258</td>
<td>53.41</td>
<td>-240</td>
</tr>
<tr>
<td>300</td>
<td>48.32</td>
<td>-201</td>
</tr>
<tr>
<td>348</td>
<td>43.37</td>
<td>-176</td>
</tr>
<tr>
<td>398</td>
<td>39.09</td>
<td>-160</td>
</tr>
</tbody>
</table>
and \( I_C(Q_8)/I_C(Q_7) = 0.16 \) for the optimum design.

The temperature dependence of the gain and dc output level for the optimum T2 design is given in Table VI.7c. Over the temperature range -55°C to 125°C, the total variation in the low-frequency gain is 38.8% and the total drift of the output voltage level is 160 mV. The sensitivity of the gain to temperature in the T2 design is exceeded only by that of the amplifier based on configuration T4, a series-shunt-series local feedback cascade.

6.3.3 Configuration T3

Design results for the amplifier based on configuration T3, and shown in Fig. 5.9, are given in Fig. 6.4 and Tables VI.8a,b, and c. The -3dB bandwidth of 133 MHz for the optimum design is the largest obtained for any of the amplifiers considered.

The amplifier based on configuration T3 is unique with respect to the other designs in that no dc current flows through the feedback resistor \( R_f \). As a result, this resistor can be adjusted without affecting the dc conditions. The optimum value of \( R_f \) given in Table VI.8a is significantly lower than the values for the other designs, indicating that dc constraints on \( R_f \) may degrade the bandwidth in the other amplifiers. Of the configurations considered, it is generally practical to establish a dc independent \( R_f \) only for the T3 configuration.

The resistor values and device specifications for the optimum design are given in Tables VI.8a and b. The values of \( R_1 \) and \( R_2 \) are the maximum allowed. The available unclipped voltage swing at the amplifier output is ±0.9 volts, the second largest value obtained for the triple designs. The optimum device geometries are single emitter, single base contact.
TABLE VI.8a
PASSIVE ELEMENT VALUES FOR OPTIMUM T3 DESIGN

<table>
<thead>
<tr>
<th>$R_{e1} = R_{e2}$</th>
<th>$R_1$</th>
<th>$R_f = 280\Omega$</th>
<th>$R_2 = 5.6k\Omega$</th>
<th>$R_3 = 1.5k\Omega$</th>
<th>$R_7 = 3.2k\Omega$</th>
<th>$C_f = 0$</th>
<th>$R_8 = 1.8k\Omega$</th>
</tr>
</thead>
</table>

TABLE VI.8b
DEVICE SPECIFICATIONS FOR OPTIMUM T3 DESIGN

<table>
<thead>
<tr>
<th>Device</th>
<th>$n_e$</th>
<th>$n_b$</th>
<th>$l_e$, mils</th>
<th>$I_C$, mA</th>
<th>$f_t$, MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q₁</td>
<td>1</td>
<td>2</td>
<td>2.40</td>
<td>.58</td>
<td>385</td>
</tr>
<tr>
<td>Q₂</td>
<td>1</td>
<td>1</td>
<td>.6</td>
<td>.82</td>
<td>590</td>
</tr>
<tr>
<td>Q₃</td>
<td>1</td>
<td>1</td>
<td>.66</td>
<td>.60</td>
<td>555</td>
</tr>
</tbody>
</table>

$\frac{I_C(Q_6)}{I_C(Q_7)} = .71$
$\frac{I_C(Q_8)}{I_C(Q_7)} = .73$

TABLE VI.8c
TEMPERATURE DEPENDENCE OF GAIN AND DC OUTPUT VOLTAGE FOR T3 DESIGN

<table>
<thead>
<tr>
<th>$T$, °K</th>
<th>$A_V(0)$</th>
<th>$V_0$, mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>218</td>
<td>53.36</td>
<td>+63</td>
</tr>
<tr>
<td>258</td>
<td>51.89</td>
<td>-54</td>
</tr>
<tr>
<td>300</td>
<td>49.88</td>
<td>+160</td>
</tr>
<tr>
<td>348</td>
<td>47.64</td>
<td>+273</td>
</tr>
<tr>
<td>398</td>
<td>45.53</td>
<td>+389</td>
</tr>
</tbody>
</table>
structures for $Q_2$ and $Q_3$ and a single emitter, double base contact device for $Q_1$; the emitter stripe lengths are 2.4 mil, .6 mil, and .66 mil, respectively, for $Q_1, Q_2$, and $Q_3$. The current ratios in the common-mode source transistors of the optimum T3 design are $I_{C}(Q_6)/I_{C}(Q_7) = 0.71$ and $I_{C}(Q_8)/I_{C}(Q_7) = 0.73$.

As indicated by the data of Table VI.8c, the variation in low-frequency gain over the range -55°C to 125°C for the T3 design is 15.7% of the nominal gain, this is substantially lower than the variations for the T2 and T4 designs, but it is much greater than that for the overall feedback configuration, T1. The total drift in the quiescent output level for the optimum T3 design is 450 mV over the -55°C to 125°C range.

6.3.4 Configuration T4

The design optimization results for the amplifier of Fig. 5.10 are given in Fig. 6.4 and Tables VI.9 a, b, and c. This amplifier is based on the configuration T4, a series-shunt-series local feedback cascade. The maximum -3dB bandwidth obtainable for the T4 amplifier is 90 MHz, the same as the maximum bandwidth of the series-series triple configurations, T1.

As indicated in Table VI.9a, all of the collector current in the first stage of the optimum T4 design is supplied through the feedback resistor $R_f$; no collector resistor $R_1$, is needed. The optimum value of the differential load resistance, $R_2$, on the second stage is the maximum permitted by dc conditions. Just as in the T2 amplifier design, the low current in the third stage results in a limited available output voltage swing. For optimum T4 design this swing is ±0.3V.
TABLE VI.9a
PASSIVE ELEMENT VALUES FOR OPTIMUM T4 DESIGN

<table>
<thead>
<tr>
<th>Element</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{e1} = R_{e2}$</td>
<td>50Ω</td>
</tr>
<tr>
<td>$R_f$</td>
<td>1.1kΩ</td>
</tr>
<tr>
<td>$R_3$</td>
<td>970Ω</td>
</tr>
<tr>
<td>$C_f$</td>
<td>0</td>
</tr>
<tr>
<td>$R_1 = \infty$</td>
<td></td>
</tr>
<tr>
<td>$R_2 = 2.7kΩ$</td>
<td></td>
</tr>
<tr>
<td>$R_7 = 2.4kΩ$</td>
<td></td>
</tr>
<tr>
<td>$R_8 = 4.2kΩ$</td>
<td></td>
</tr>
</tbody>
</table>

TABLE VI.9b
DEVICE SPECIFICATIONS FOR OPTIMUM T4 DESIGN

<table>
<thead>
<tr>
<th>Device</th>
<th>$n_e$</th>
<th>$n_b$</th>
<th>$l_e$, mils</th>
<th>$I_C$, mA</th>
<th>$f_t$, MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>2</td>
<td>3</td>
<td>3.17</td>
<td>.62</td>
<td>245</td>
</tr>
<tr>
<td>Q2</td>
<td>1</td>
<td>1</td>
<td>.6</td>
<td>1.11</td>
<td>615</td>
</tr>
<tr>
<td>Q3</td>
<td>1</td>
<td>1</td>
<td>.80</td>
<td>.27</td>
<td>425</td>
</tr>
</tbody>
</table>

$\frac{I_C(Q_6)}{I_C(Q_7)} = .56$

$\frac{I_C(Q_8)}{I_C(Q_7)} = .24$

TABLE VI.9c
TEMPERATURE DEPENDENCE OF GAIN AND DC OUTPUT VOLTAGE FOR T4 DESIGN

<table>
<thead>
<tr>
<th>$T$, °K</th>
<th>$A_V(0)$</th>
<th>$V_0$, mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>218</td>
<td>64.71</td>
<td>+3</td>
</tr>
<tr>
<td>258</td>
<td>57.38</td>
<td>-13</td>
</tr>
<tr>
<td>300</td>
<td>50.32</td>
<td>-36</td>
</tr>
<tr>
<td>348</td>
<td>43.66</td>
<td>-66</td>
</tr>
<tr>
<td>398</td>
<td>38.12</td>
<td>-100</td>
</tr>
</tbody>
</table>
TABLE IV.19
PASSIVE ELEMENT VALUES FOR OPTIMUM TA DESIGN

<table>
<thead>
<tr>
<th>R1</th>
<th>R2</th>
<th>R3</th>
<th>R4</th>
<th>R5</th>
<th>R6</th>
<th>R7</th>
<th>R8</th>
<th>C1</th>
</tr>
</thead>
<tbody>
<tr>
<td>500Ω</td>
<td>1.1kΩ</td>
<td>2kΩ</td>
<td>2.5kΩ</td>
<td>5.7kΩ</td>
<td>10kΩ</td>
<td>0.4MΩ</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
The optimum device characteristics for the T4 amplifier are given in Table VI.9b. A double emitter, three base contact device, with an emitter stripe length of 3.17 mil, is specified for Q₁. The optimum structure for Q₂ is a minimum area device and a single emitter single base contact device with a stripe length of 0.8 mil is optimum for Q₃. Current ratios in the source transistors are \( I_C(Q_6)/I_C(Q_7) = 0.56 \) and \( I_C(Q_8)/I_C(Q_7) = 0.24 \).

Results of the first-order temperature sensitivity analysis for the optimum T4 design are given in Table VI.9c. The total gain variation over -55°C to 125°C is 53.2% of the gain at room temperature. This is the highest gain sensitivity obtained for any of the designs considered. It is explained by the fact that the T4 configuration is a cascade of three local feedback loops. The bandwidth is comparable to that of the overall feedback amplifier, T1, but, as noted in Sec. 6.2.3 the overall feedback results in a much lower gain sensitivity. The total drift in the quiescent output voltage of the T4 design is 100 mV over -55°C to 125°C. This is comparable to the drift obtained with the T1 configuration.

6.4 Comparison of the Optimum Designs

A summary of the performance characteristics for all of the optimum amplifier designs is given in Table VI.10. Included in the table for each design are the -3dB bandwidth, the input resistance, the maximum available unclipped swing in the output voltage, and the total variations in low-frequency gain and quiescent output voltage over the temperature range -55°C to 125°C. All of the designs have a low-frequency differential voltage gain of 34dB and quiescent power dissipation of 96 mW.

The data summarized in Table VI.10 indicates that of the designs considered, the optimum design based on configuration P1 provides the best
TABLE VI.10
CHARACTERISTICS OF OPTIMUM DESIGNS

<table>
<thead>
<tr>
<th>Configuration</th>
<th>-3dB BW (MHz)</th>
<th>R\text{in} (k\Omega)</th>
<th>Max.</th>
<th></th>
<th>\text{Over } T = -55°C to 125°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>\text{Max. }</td>
<td>\Delta V(0) \text{ (mv)}</td>
<td>\Delta V\text{0} \text{ (mv)}</td>
</tr>
<tr>
<td>P1</td>
<td>123</td>
<td>850</td>
<td>2.4</td>
<td>.6%</td>
<td>30</td>
</tr>
<tr>
<td>P2</td>
<td>95</td>
<td>330</td>
<td>2.4</td>
<td>2.0%</td>
<td>640</td>
</tr>
<tr>
<td>P3</td>
<td>122</td>
<td>17</td>
<td>2.4</td>
<td>10.2%</td>
<td>190</td>
</tr>
<tr>
<td>P4</td>
<td>105</td>
<td>17</td>
<td>2.4</td>
<td>8.6%</td>
<td>160</td>
</tr>
<tr>
<td>T1</td>
<td>90</td>
<td>2,900</td>
<td>1.5</td>
<td>2.1%</td>
<td>100</td>
</tr>
<tr>
<td>T2</td>
<td>78</td>
<td>940</td>
<td>0.13</td>
<td>38.8%</td>
<td>160</td>
</tr>
<tr>
<td>T3</td>
<td>133</td>
<td>26</td>
<td>0.9</td>
<td>15.7%</td>
<td>450</td>
</tr>
<tr>
<td>T4</td>
<td>90</td>
<td>22</td>
<td>0.3</td>
<td>53.2%</td>
<td>100</td>
</tr>
</tbody>
</table>
overall performance. The bandwidth for this design is 123 MHz, second only to the 133 MHz obtained for the T3 configuration. The input resistance of 850 kΩ is surpassed only by the 2.9 MΩ and 940 kΩ of the T1 and T2 designs. The unclipped output swing for the P1 amplifier is the maximum achieved, ±2.4V. The .6% variation in gain over the temperature range -55°C to 125°C is the lowest obtained, as is the 30 mV drift in the quiescent output voltage.

The optimum amplifier designs based on configurations P3 and T3 exhibit bandwidths of 122 MHz and 133 MHz; only these configurations provide bandwidths comparable to the 123 MHz obtained for the P1 design. However, both the P3 and T3 configurations have local series feedback in the input stage and consequently are characterized by the relatively low input resistances of 17 kΩ and 26 kΩ, respectively. The variation of the low-frequency gain over the temperature range -55°C to 125°C is 10.2% for the P3 amplifier and 15.7% for the T3 designs; these values are more than an order of magnitude greater than the .6% variation for the optimum P1 design.

Three of the designs included in Table VI.10 have gain sensitivities to temperature that are substantially lower than those of the other five amplifiers. The amplifier based on the P1 configuration exhibits the smallest variation in gain, .6%, over the range -55°C to 125°C. The variations for the designs based on the P2 and T1 configurations are 2.0% and 2.1%, respectively. The distinguishing feature of these three configurations with low gain sensitivity is that all of the common-emitter gain stages are included within a single overall feedback loop. As expected from a consideration of ideal feedback systems, overall feedback results in a significantly greater reduction in gain sensitivity than is achieved with local feedback. Of the three configurations, P1, P2 and T1, providing a
The optimum multiplet selection is based on a combination of the 123 MHz and 133 MHz bands. The preliminary data shows a correlation between the two frequencies and the signal strength. Further experiments are required to confirm these observations.
low gain sensitivity to temperature, the 123 MHz bandwidth of the PI design is 29% greater than the 95 MHz obtained for the P2 design and 37% greater than the 90 MHz of the T1 amplifier.

The excellent performance obtainable with the PI configuration is to a large extent, the result of three interrelated factors. First, as for all of the pairs, there are only two gain stages; consequently, the dc current level per stage is higher than for the triples and the transistors operate at a higher $f_T$. Second, overall feedback is used in the PI design, resulting in low gain sensitivity and a high input resistance. Finally, an output emitter-follower is included within the overall feedback loop of the PI configuration, a series-shunt pair. The inclusion of the emitter-follower within the feedback loop reduces the loading of feedback network on the forward amplifier and results in a significant increase in loop gain. This is easily demonstrated by comparing the input resistances, given in Table VI.9, of the PI and P2 designs; the latter configuration is an overall series-shunt pair cascaded with an emitter follower. The open-loop input resistance is higher for the P2 design because of the larger emitter resistor, $R_e$, in the input stage; however, the closed-loop input resistance is more than a factor of two larger for the PI configuration. This indicates that the inclusion of the emitter-follower within the feedback loop results in better than a factor of two increase in the loop gain.

The only significant disadvantage of the PI amplifier is that a capacitive feedback element must be used in order to achieve the maximum bandwidth obtainable. The 0.3 pF for the capacitance is, however, quite small and does not require a large amount of silicon area. Because of the small value needed, it may be feasible to adjust the area of the diffused feedback resistor, $R_f$, such that compensation can be achieved by connecting the
to gain sensitivity to compressors, the 123-MHz bandwidth of the

\[ \text{SOI} \]

saturates from the 20 MHz of the IT amplifier.

The excellent performance obtained with the 12 configuration is to

\[ \text{SOI} \]

retract the result of three interacting factors. First as for

\[ \text{SOI} \]

the data of the figure, there are only two gain stages, consequently, the 12

\[ \text{SOI} \]

cannot show better results in higher gain for the tips and the transistors

\[ \text{SOI} \]

can operate at a higher gain. Second, overall feedback is more in the 12 gain

\[ \text{SOI} \]

as it is in gain sensitivity and a higher input resistance. Finally, a

\[ \text{SOI} \]

certain configuration is obtained with the amplifiers of the

\[ \text{SOI} \]

output. The feedback amplifiers of the input are

\[ \text{SOI} \]

ly connected to the input. Therefore, the amplifiers of the output are

\[ \text{SOI} \]

independent of the input and can be used as a

\[ \text{SOI} \]

input.
parasitic capacitance of this resistor as shown in Fig. 6.5. The surrounding n region is connected to the more positive end of the resistor.
Fig. 6.5: Connection of parasitic capacitance for compensation in a feedback network.
CHAPTER VII
EXPERIMENTAL RESULTS

7.1 Introduction

All of the amplifier designs developed in Chaps. V and VI should be readily integrable in most processing facilities. The configurations do not differ substantially from commonly realized circuits. Nonetheless, in order to verify the feasibility of realizing these configurations, and to confirm the suitability of the device models used in the automated design procedure, both discrete component and monolithic amplifiers have been fabricated.

7.2 Discrete Component Realization

The complete amplifier configuration of Fig. 5.3, which is based on a series-series feedback triple, has been realized with discrete components, including matched transistor pairs. The transistors have a typical $\beta_0$ of 110 and $f_T$ of 425 MHz at a collector current of 1 mA. The discrete realization has been constructed primarily to verify the set up of dc conditions in the amplifier; consequently, the design has not been optimized for the discrete components.

The component values and current levels for the discrete amplifier are given in Table VII.1; the notation is that used in Fig. 5.3. The ratio of currents in the current source transistors $Q_6$ and $Q_7$ is established with emitter resistors of 250$\Omega$ for $Q_5$ and 750$\Omega$ for $Q_6$. The dc conditions in the amplifier set up as expected and the specified 34dB low-frequency gain is achieved. The frequency response of the amplifier
TABLE VII.1

COMPONENT VALUES AND CURRENT LEVELS FOR DISCRETE AMPLIFIER REALIZATION

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{e1}$</td>
<td>$200 \Omega$</td>
</tr>
<tr>
<td>$R_{e2}$</td>
<td>$200 \Omega$</td>
</tr>
<tr>
<td>$R_f$</td>
<td>$1.2k\Omega$</td>
</tr>
<tr>
<td>$R_1$</td>
<td>$12k\Omega$</td>
</tr>
<tr>
<td>$R_2$</td>
<td>$10k\Omega$</td>
</tr>
<tr>
<td>$R_3$</td>
<td>$2k\Omega$</td>
</tr>
<tr>
<td>$R_4$</td>
<td>$1.65k\Omega$</td>
</tr>
<tr>
<td>$R_5$</td>
<td>$3.3k\Omega$</td>
</tr>
<tr>
<td>$R_6$</td>
<td>$4.7k\Omega$</td>
</tr>
<tr>
<td>$R_7$</td>
<td>$5k\Omega$</td>
</tr>
<tr>
<td>$R_8$</td>
<td>$1k\Omega$</td>
</tr>
<tr>
<td>$I_{C(Q_1)}$</td>
<td>$0.5 mA$</td>
</tr>
<tr>
<td>$I_{C(Q_2)}$</td>
<td>$0.5 mA$</td>
</tr>
<tr>
<td>$I_{C(Q_3)}$</td>
<td>$1 mA$</td>
</tr>
<tr>
<td>$I_{C(Q_4)}$</td>
<td>$1 mA$</td>
</tr>
<tr>
<td>$I_{C(Q_5)}$</td>
<td>$1.3 mA$</td>
</tr>
<tr>
<td>$I_{C(Q_6)}$</td>
<td>$1.3 mA$</td>
</tr>
<tr>
<td>$I_{C(Q_7)}$</td>
<td>$3$</td>
</tr>
</tbody>
</table>

$\frac{I_{C(Q_6)}}{I_{C(Q_7)}} = 3$
Fig. 7.1: Response of discrete component amplifier.
is shown in Fig. 7.1; the -3dB bandwidth is 34 MHz. Capacitive compensation is not used for the feedback triple. As described in Sec. 5.3.3, compensation is established through a suitable choice of the differential load resistance for the triple.

7.3 Monolithic Realization

In addition to the discrete component amplifier, the balanced series-series triple portion of the amplifier in Fig. 5.3 has been fabricated in the Integrated Circuits Laboratory at Berkeley. As noted in Chapter IV, because of optical limitations, the minimum mask dimensions presently achievable in this facility are somewhat larger than those assumed for the designs of Chap. VI. For example, the minimum emitter stripe width is 1.6 mil instead of the .6 mil in Fig. 4.1. The mask dimensions for a minimum area device are illustrated in Fig. 7.2.

To establish a design for monolithic realization, it was necessary to repeat the design optimization procedure for the larger minimum dimensions. These larger dimensional restrictions also preclude realization of the full configuration in Fig. 5.3. However, as indicated in Chap. V, the limitations on the frequency response of the complete amplifier arise entirely from the balanced series-series triple. The configuration of the monolithic amplifier realization is given in Fig. 7.3.

The overall specifications assumed for the amplifier of Fig. 7.3 are a low-frequency differential voltage gain of 37.5 dB, ± 6V power supplies, and a quiescent power dissipation of 48 mW. These specifications are equivalent to those used in Chap. V for the complete amplifier of Fig. 5.3. Except for the minimum dimensions, the other constraints in the design optimization procedure are also the same as those used for the
Fig. 7.2: Minimum area device topology for monolithic amplifier realization.
Fig. 7.3: Balanced series-series triple configuration.
Fig. 7.3: Balanced series-series triple configuration.
Fig. 7.3: Balanced series-series triple configuration.
amplifier of Fig. 5.3. A 1.4V collector-emitter voltage is specified for $Q_1$ and $Q_2$, while the assumed quiescent output voltage at the collector of $Q_3$ is 3V. The emitter resistors, $R_{e1}$ and $R_{e2}$, are constrained to be equal for the reasons presented in Sec. 6.1, and the minimum value allowed for a diffused resistor is 50Ω.

The diffusion process used for the monolithic realization is the same as that employed for the device characterization of Chap. IV. This process results in a base diffusion depth of 3.5 μm, a base sheet resistance of 125 Ω/square, and a basewidth of 0.8 μm. The starting material is a 1Ω-cm, 10 μm n-type epitaxial layer on a 5Ω-cm p-type substrate. As is evident from the large value given in Table VII.3 for $r'_T$, a buried layer structure was not used.

The results of the design optimization procedure for the amplifier of Fig. 7.3 are summarized in Tables VII.2 and VII.3. Given in Table VII.2 are the passive element values for the optimum design, the optimum dc collector currents for $Q_1$, $Q_2$, and $Q_3$, and the ratio of quiescent currents in the current source transistors, $Q_4$ and $Q_5$. The values shown for $R_1$ and $R_2$ are the maximum allowed by dc conditions. The optimum ratio of currents in $Q_4$ and $Q_5$, $I_C(Q_4)/I_C(Q_5) = 3.3$, is established by using a minimum area device for $Q_5$ and increasing the emitter stripe length of $Q_4$.

The optimum planar geometry for the devices $Q_1$, $Q_2$, and $Q_3$, as indicated by the results of automated design procedure, is the minimum area topology illustrated in Fig. 7.2. Devices with this geometry have been characterized experimentally and the results are summarized in Table VII.3. The devices have a typical $f_T$ of 170 MHz at a collector current of 1 mA and collector-emitter voltage of 1.5 V. A constant $\beta_0$ of 120 has been assumed because
### TABLE VII.2

**OPTIMUM DESIGN FOR SERIES-SERIES TRIPLE OF FIG. 7.3**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{e1} = R_{e2}</td>
<td>210Ω</td>
</tr>
<tr>
<td>R_{f}</td>
<td>1.24kΩ</td>
</tr>
<tr>
<td>R_{1}</td>
<td>12.7kΩ</td>
</tr>
<tr>
<td>R_{2}</td>
<td>10.0kΩ</td>
</tr>
<tr>
<td>R_{3}</td>
<td>2.06kΩ</td>
</tr>
<tr>
<td>R_{4}</td>
<td>5.8kΩ</td>
</tr>
<tr>
<td>R_{5}</td>
<td>300Ω</td>
</tr>
</tbody>
</table>

| IC(Q_{1}) | 0.41 mA |
| IC(Q_{2}) | 0.46 mA |
| IC(Q_{3}) | 1.13 mA |
| \( \frac{IC(Q_4)}{IC(Q_5)} \) | 3.3 |

The table lists the optimum design parameters for a series-series triple configuration as depicted in Fig. 7.3. Each parameter is specified with its respective value in ohms (Ω) or kiloohms (kΩ), along with the currents flowing through the respective components."
### TABLE VII.3

**CHARACTERISTICS FOR MINIMUM AREA TRANSISTOR OF FIG. 7.2**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_0$</td>
<td>120</td>
</tr>
<tr>
<td>$r'_b$</td>
<td>$\left(210 + \frac{200}{I_c+1.3}\right) \Omega$ where $I_c$ is in mA.</td>
</tr>
<tr>
<td>$r'_c$</td>
<td>400(\Omega)</td>
</tr>
<tr>
<td>$\tau_t$</td>
<td>.22 nsec</td>
</tr>
<tr>
<td>$C_{je}$</td>
<td>5.5 pF</td>
</tr>
</tbody>
</table>
| $C_{cb}$  | \[
|           | \begin{cases}
|           | 1.4 \text{ pF} @ V_{BC} = -.7V \\
|           | 1.15 \text{ pF} @ V_{BC} = -1.6V 
|           | \end{cases}
|           | \] |
| $C_{cs}$  | \[
|           | \begin{cases}
|           | 1.25 \text{ pF} @ V_{SC} = -6.7V \\
|           | 1.23 \text{ pF} @ V_{SC} = -7.4V \\
|           | 1.16 \text{ pF} @ V_{SC} = -9.0V 
|           | \end{cases}
|           | \] |
the variation in $\beta_0$ over the current range of interest is relatively small.

Given in Table VII.3 are the values of the total collector-base and collector-substrate capacitances corresponding to the quiescent voltages specified for $Q_1$, $Q_2$, and $Q_3$. If a .7V base-emitter voltage is assumed, the reverse bias voltage on the collector-base junction is .7V for $Q_1$, .7V for $Q_2$, and 1.4V for $Q_3$. The collector-substrate reverse voltages are 6.7V for $Q_1$, 7.4V for $Q_2$, and 9V for $Q_3$. For the device models in the design program, these capacitances are divided into two components as described in Sec. 4.3 and Fig. 4.2. As indicated in Sec. 4.3, this division is established from geometrical estimates. For the minimum area device of Fig. 7.2, the components in the model of Fig. 4.2 are given by

$$C_{cb1} = 0.33 \ C_{cb}$$
$$C_{cb2} = 0.67 \ C_{cb}$$
$$C_{cs1} = 0.40 \ C_{cs}$$
$$C_{cs2} = 0.60 \ C_{cb}$$

where $C_{cb}$ and $C_{cs}$ are the total capacitances given Table VII.3.

A photograph of the monolithic balanced triple is shown in Fig. 7.4. The experimental set up for measuring the voltage gain-frequency response of the amplifier is described in Appendix E. Discrete emitter-followers are used to provide a very high impedance load for the monolithic amplifier. The capacitive loading of these emitter-followers, as well as parasitic capacitance associated with the packaging, have been taken into account in the design optimization of the amplifier. The amplifier is
Fig. 7.4: Photograph of monolithic balanced triple.
mounted in a TO-5 can with a typical pin-to-header capacitance of .8 pF.

Initial experimental measurements indicated an amplifier response with severe bandedge peaking. It was subsequently discovered that an incorrect value had been used in the design program for the transistor collector-substrate capacitance. The value used was much too low. When the correct value of capacitance was used, a frequency response analysis of the realized design displayed the experimentally observed peaked. Additional analysis runs indicated that the peaking could be eliminated with a 1.8 pF feedback capacitor in shunt across the resistor $R_f$. Discrete capacitors of this value were added to the experimental amplifier and the expected response shape was obtained.

The measured response for a typical realization, with the compensation capacitors added, is shown in Fig. 7.5. Included in the figure is the theoretically predicted response when the correct collector substrate capacitances and the compensation capacitor are used. The experimental response exhibits the predicted low frequency differential gain of 37.5 dB with a -3dB bandwidth of 34 MHz. The bandwidth is within 6% of the expected value.

The average of the differential offset voltage measured for several units is 2.5 mV referred to the input. This value is typical for differential amplifiers with a bipolar transistor input transistor pair.
Fig. 7.5: Response of monolithic amplifier.
CHAPTER VIII

CONCLUSION

An effective program has been developed for the automated design of monolithic broadband amplifiers. This program utilizes most of the available degrees of design freedom to achieve optimum amplifier performance. For a given configuration, dc conditions, device geometry, and all passive elements are adjusted to obtain the maximum -3dB bandwidth consistent with a specified gain and quiescent power dissipation.

In this study, the design program has been used to examine a particular class of monolithic amplifiers. This class is defined by the requirements for a dc-coupled voltage gain response with a large bandwidth, restricted quiescent power dissipation, low gain sensitivity to temperature and processing, and zero volt quiescent levels at input and output. The latter specification permits the direct cascading of amplifiers without coupling elements.

Complete differential amplifiers suitable for meeting the specified requirements have been developed from eight basic feedback configurations. The automated design program has been used to optimize each of these amplifiers under the specifications for a voltage gain of 34dB and a power dissipation of 96 mW. The results of the design optimization procedure have then been used to establish the relative effectiveness of the basic feedback configurations.

Of the basic configurations considered, the series-shunt feedback pair with an output emitter-follower included in the feedback loop provides
the best overall performance. The amplifier based on this configuration achieves a relatively large bandwidth, very low gain and dc output level sensitivities, a high input resistance, and a large available output voltage swing. As for all of the designs considered, the bandwidth is limited by the restricted power dissipation.

The comparison of basic configurations presented in this study differs significantly from the results of previous work [53]. The earlier work was based on computer-aided analysis, and a trial and error approach was used to establish designs for various feedback configurations. Arbitrary choices were made for dc conditions and device geometry. A comparison of the final designs arrived at in this preliminary work indicated that the series-series feedback triple provided performance superior to that of the series-shunt pair. However, the emitter-follower was not included within the feedback loop of the pair and, also, it was not possible to establish the best possible performance for each of the configurations.

The amplifier bandwidths achieved in this report using automated design optimization are typically a factor of two greater than those of similar commercial designs with comparable transistor $f_T$'s. In a given design situation, the improvement obtainable with automated design relative to nonautomated results depends on two factors. The first is the influence on the response of parameters, such as dc conditions, that are fixed in a nonautomated procedure. The second is whether or not a fortunate choice is made for these fixed parameters on a nonautomated basis.

At least as significant as the improved performance obtainable with an automated design procedure is the capability to document the existence of a design optimum. As noted above, conclusions with regard to the relative effectiveness of alternative design approaches may depend
significantly on whether or not the best possible performance is obtained for each approach. Once the automated design procedure is completed successfully for an amplifier, no further improvement can be obtained under the constraints assumed in the procedure.

The design approach described in this dissertation is based on relatively new techniques that have not heretofore been applied to practical design problems. The principal results of this work are a demonstration of the effectiveness of these techniques, as well as an indication of their potential for application to a much broader class of circuit design problems. While in this study consideration has been given to a very specific class of circuits, the approach is readily extended to more general circuit design work.

There are, of course, significant problems yet to be considered if automated design is to become a reality for a large class of circuits. For example, the choice of a performance index is critical in a fully automated design procedure. The effectiveness and efficiency of the procedure depends in large part on establishing a suitable index. Even for the work presented in this report, it is not clear that the least squared error formulation that has been used is the most effective index for achieving a near maximally flat frequency response with maximum -3dB bandwidth.

The choice of optimization algorithm is also critical in determining the efficiency of an automated design procedure. The Fletcher-Powell algorithm has been used here because of its successful applications in other fields. For circuit design, however, some other search formulation may well be more effective.

A general concern of automated circuit design procedures is the existence of local minima. In any numerical search procedure, there are
no direct means for determining whether or not a minimum is global. The only solution to this problem is to attempt to locate all of the minima in the space of allowable design parameters by conducting numerous searches starting at different initial designs. Fortunately, for the designs considered in this case only a single physically realistic optimum has been found in each case. Apparently, the restriction to physically realizable designs does much to alleviate the local minima problem.
APPENDIX A
THE ADJOINT NETWORK

The development of the adjoint network concept for evaluating network
response sensitivities has been described for the general case by Director
and Rohrer [21-23]. In this appendix, the development is presented
for the restricted case of a two-port network with a single current source
excitation; consideration is restricted to a frequency domain response
formulation and to networks with only conductance (G), capacitance (C),
and transconductance (g_m) elements.

Consider the linear, time invariant two-port network \( \mathcal{N} \), shown in
Fig. A.1, that is comprised of G, C and g_m elements, with the current
source excitation \( I_S(j\omega) \) and the open-circuit voltage response \( V_0(j\omega) \).
The intent of following formulation is to establish the sensitivity of
\( V_0(j\omega) \) to any element, \( P \), of the network under a given excitation.

Let \( \mathcal{N} \) represent a network that is topologically equivalent to \( \mathcal{N} \),
but for which the branch relations are as yet defined. Let the branch
current and voltage responses in \( \mathcal{N} \) be denoted by \( I_B(j\omega) \) and \( V_B(j\omega) \) and
those in \( \mathcal{N} \) be denoted by \( \psi_B(j\omega) \) and \( \phi_B(j\omega) \). Then, by Tellegen's theorem
[54]

\[
\sum_B V_B(j\omega)\phi_B(j\omega) = 0 \tag{A.1a}
\]

\[
\sum_B \psi_B(j\omega)I_B(j\omega) = 0 \tag{A.1b}
\]
Fig. A.1: Linear, time-invariant two-port network with current source excitation and open circuit output.

Fig. A.2: Representation of a voltage controlled current source in $\mathcal{H}$.
where the summation is carried out over all branches, including
the current source, the open circuit output branch, and the open circuit
that is associated with the input of any transconductances, as indicated
in Fig. A.2. If the elements of \( \mathcal{H} \) are perturbed, the responses in the
network are altered. Nonetheless, the relationship (A.1) between \( \mathcal{H} \)
and \( \mathcal{H} \), arising from Tellegen's theorem is not changed as long as the topology
of \( \mathcal{H} \) is not modified. That is, if \( \Delta V_B(j\omega) \) and \( \Delta I_B(j\omega) \) represent the
changes in the responses of \( \mathcal{H} \) due to perturbations in the network elements,

\[
\sum_B [V_B(j\omega) + \Delta V_B(j\omega)] \phi_B(j\omega) = 0 \quad \text{(A.2a)}
\]

\[
\sum_B \psi_B(j\omega) [I_B(j\omega) + \Delta I_B(j\omega)] = 0 \quad \text{(A.2b)}
\]

Subtracting (A.1a) from (A.2a) and (A.1b) from (A.2b) yields

\[
\sum_B \Delta V_B(j\omega) \phi_B(j\omega) = 0 \quad \text{(A.3a)}
\]

\[
\sum_B \psi_B(j\omega) \Delta I_B(j\omega) = 0 \quad \text{(A.3b)}
\]

and subtracting (A.3b) from (A.3a) results in

\[
\sum_B [\Delta V_B(j\omega) \phi_B(j\omega) - \Delta I_B(j\omega) \psi_B(j\omega)] = 0 \quad \text{(A.4)}
\]

The summation of (A.4) may be broken into branch types and expressed as
where the parenthetical inclusion of \( j\omega \) has been dropped from the frequency domain notation, as is done in the remainder of this appendix. In the representation (A.5), transconductances are regarded as two branch elements as shown in Fig. A.2. The open-circuit controlling branch is denoted by the subscript VCI and the dependent current source branch by the subscript VDI.

The next step is to introduce the branch relationships of \( \mathbf{g} \) into (A.5) and define the branch relations for \( \mathbf{g} \). The branch relationships for the conductance branches of \( \mathbf{g} \) are of the form

\[
I_G = GV_G
\]  

(A.6)

If the conductance is perturbed by \( \Delta G \), then

\[
(I_G + \Delta I_G) = (G + \Delta G)(V_G + \Delta V_G) \]

(A.7)

If the second-order term is neglected and (A.6) is introduced into (A.7),

\[
\Delta I_G = G\Delta V_G + V_G\Delta G
\]  

(A.8)
The summation in (A.5) corresponding to the conductance branches may then be expressed as

$$\sum \left[ (\phi_G - G\psi_G) \Delta V_G - V_G \psi_G \Delta G \right]$$  \hspace{1cm} (A.9)

Similarly, for the capacitance branches

$$I_C = j\omega C V_C$$  \hspace{1cm} (A.10)

and if $C$ is perturbed by $\Delta C$ then

$$\Delta I_C = j\omega C \Delta V_C + j\omega V_C \Delta C$$  \hspace{1cm} (A.11)

where the second-order term is neglected. If (A.11) is introduced into the capacitance-branch summation of (A.5), the summation becomes

$$\sum \left[ (\phi_C - j\omega C \psi_C) \Delta V_C - j\omega V_C \psi_C \Delta C \right]$$  \hspace{1cm} (A.12)

The branch relationships for the voltage dependent current source shown in Fig. A.1 are

$$I_{VCI} = 0$$  \hspace{1cm} (A.13a)

$$I_{VDI} = g_m V_{VCI}$$  \hspace{1cm} (A.13b)

If $g_m$ is perturbed and second-order terms are neglected,

$$\Delta I_{VCI} = 0$$  \hspace{1cm} (A.14a)

$$\Delta I_{VDI} = g_m \Delta V_{VCI} + V_{VCI} \Delta g_m$$  \hspace{1cm} (A.14b)
The summation in (A.5) corresponding to the controlling and controlled branches of voltage dependent current sources may be combined and expressed as

\[ \sum_{\phi_m} [\Delta V_{\phi_1} \Delta V_{\phi_2} + (\phi_{\psi_1} \psi_{\phi_1} \phi_{\psi_2} \psi_{\phi_2}) \Delta V_{\phi_1} \phi_{\psi_1} \psi_{\phi_1} \phi_{\psi_2} \psi_{\phi_2}] = 0 \]  

(A.15)

For the current source branch in (A.5)

\[ \Delta I_S = 0 \]  

(A.16)

while for the output branch

\[ I_0 = 0 \]  

(A.17)

and hence

\[ \Delta I_0 = 0 \]  

(A.18)

The first two terms in (A.5) may therefore be reduced to

\[ \Delta V_S \phi_S + \Delta V_0 \phi_0 \]  

(A.19)

In order to arrive at a formulation of the response sensitivity for \( \mathcal{H} \) it is necessary to eliminate the dependence of (A.9) on \( \Delta V_0 \), (A.12) on \( \Delta V_0 \), and (A.15) on \( \Delta V_{\phi_1} \) and \( \Delta V_{\phi_2} \). This can be accomplished by defining the following branch relations for the network \( \mathcal{H} \)

\[ \phi_G = G \psi_G \]  

(A.20)

\[ \phi_C = j \omega C \psi_C \]  

(A.21)
\[ \phi_{VCI} = 0 \quad (A.22a) \]

\[ \phi_{VDI} = g_m \psi_{VDI} \quad (A.22b) \]

The network \( \hat{\mathcal{R}} \) with the branch relations defined by (A.20) - (A.22) is referred to as the linear adjoint network corresponding to the original network, \( \mathcal{N} \). The relationships (A.20) and (A.21) indicate that conductance and capacitance branches in \( \mathcal{N} \) correspond to identical branches in \( \hat{\mathcal{R}} \). The expressions (A.22) characterize the voltage controlled current source in \( \hat{\mathcal{R}} \) shown in Fig. A.3. The roles of the controlling and controlled branches are reversed from those in the original network \( \mathcal{N} \).

If branch relations for \( \hat{\mathcal{R}} \) are defined by equations (A.20) - (A.22) and (A.9), (A.12), (A.15), and (A.19) are used in (A.5),

\[ \Delta V_S \phi_S + \Delta V_0 \phi_0 = \sum_G V_G \psi_G \Delta G + \sum_C j \omega C \psi_C \Delta C + \sum_{g_m} V_{VCI} \psi_{VDI} \Delta g_m \quad (A.23) \]

In order to determine the sensitivity of \( V_0 \) directly, the following excitations are applied to the adjoint network.

\[ \phi_S = 0 \quad (A.24a) \]

\[ \phi_0 = 1 \quad (A.24b) \]

as indicated in Fig. A.4. Note the direction of the independent source \( \phi_0 \) in the figure; consistent branch voltage and current definitions are followed for all branches.

When the excitations of (A.24) are applied, then (A.23) may be
Fig. A.3: Voltage controlled current source in \( \hat{\eta} \) corresponding to the voltage controlled current source of \( \eta \) shown in Fig. A.2.

Fig. A.4: Linear adjoint network \( \hat{\eta} \), corresponding to network \( \eta \).
expressed as

\[ \Delta V_0 = \mathbf{z}^T \mathbf{P} \]  

where \( \Delta \mathbf{P} \) is a column vector of the network elements and \( \mathbf{z} \) is a column vector of sensitivity components, \( \frac{\partial V_0}{\partial \mathbf{P}} \). The corresponding components of \( \Delta \mathbf{P} \) and \( \mathbf{z}^T \) are given in Table A.1. The sensitivity component for a conductance branch is the product of branch voltages in the original and adjoint networks; for a capacitance branch it is the product of branch voltages multiplied by \( j \omega \). For the voltage controlled current sources the sensitivity component is the product of controlling branch voltages \( \mathbf{\eta} \) and \( \mathbf{\hat{\eta}} \).

In the limit as \( \Delta \mathbf{P} \to 0 \), (A.25) may be expressed as

\[ \nabla_{\mathbf{P}} V_0 = \mathbf{z} \]  

(A.26)

Thus \( \mathbf{z} \) is simply the gradient of the response \( V_0 \) with respect to the network elements of \( \mathbf{\eta} \).
<table>
<thead>
<tr>
<th>( \Delta P_i )</th>
<th>( \frac{\partial V}{\partial P_i} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \Delta G )</td>
<td>( V_G \psi_G )</td>
</tr>
<tr>
<td>( \Delta C )</td>
<td>( j \omega V_C \psi_C )</td>
</tr>
<tr>
<td>( \Delta g_m )</td>
<td>( V_{VC1} \psi_{VDI} )</td>
</tr>
</tbody>
</table>
APPENDIX B
THE FLETCHER-POWELL ALGORITHM

When the gradients of a performance index are relatively easy to obtain, as in the case where the adjoint network approach is used, the algorithm of Fletcher and Powell is regarded as one of the most effective approaches for finding the minimum of the index. This algorithm is based on a procedure introduced by Davidson [55], and it is well described in the original article by Fletcher and Powell [56]. In this appendix, a brief summary of the algorithm is given.

In the following equations the notation $\mathbf{x}$ is used to represent the column vector of $n$ independent variables

$$
\mathbf{x} = \begin{bmatrix}
  x_1 \\
  x_2 \\
  \vdots \\
  x_n
\end{bmatrix} \quad \text{(B.1)}
$$

and the notation for the corresponding row vector is $\mathbf{x}^T$. The scalar objective function of the variables represented by $\mathbf{x}$ is expressed as $f$ and the vector $\mathbf{g}$ is the gradient of $f$ with respect to $\mathbf{x}$.

The development of the algorithm for minimizing $f$ is based on assuming an ideal quadratic form for this function.

$$
f = f_0 + \mathbf{a}^T \mathbf{x} + \frac{1}{2} \mathbf{x}^T \mathbf{G} \mathbf{x} \quad \text{(B.2)}
$$

where $\mathbf{G}$ is a positive definite $n \times n$ nonsingular matrix. For the case where
the objective function is quadratic, the method of Fletcher and Powell guarantees convergence to the minimum in \( n+1 \) iterations. For the more practical case where \( f \) is not quadratic, convergence takes longer and cannot be guaranteed. However, in the neighborhood of the minimum the objective function is usually well approximated by a quadratic form; when the search reaches this neighborhood, the algorithm rapidly converges to the minimum.

If \( x^* \) denotes the point corresponding to the minimum of \( f \), the step needed to reach \( x^* \) from any point \( \tilde{x} \) is given by

\[
\tilde{x}^* - \tilde{x} = -G^{-1}g
\]  \hspace{1cm} (B.3)

The gradient \( g \), but not the matrix of second order derivatives \( G \), is assumed to be computationally available. The form of (B.4) suggests, however, that a search direction other than that of steepest descent (the negative gradient direction) be used. Hence a positive definite matrix \( H \) is substituted for \( G^{-1} \) in the iterative search procedure. The initial choice of \( H \) is arbitrary, but \( H \) is modified as the search proceeds to better approximate \( G^{-1} \). Upon convergence of the search to the minimum, \( H \) converges to \( G^{-1} \); thus, the algorithm not only locates the minimum but provides curvature information valuable for testing convergence.

At the \( i^{th} \) iteration, the starting point is denoted by \( \tilde{x}_i \), with the corresponding gradient \( \tilde{g}_i \) and matrix \( H_i \). Let \( s_i \) denote the direction of search from \( \tilde{x}_i \). The initial choice for the matrix \( H \) is often the unit matrix.
and the search consequently begins in the direction of steepest descent, 
$-g_i$. The iterative procedure at the $i^{th}$ iteration is as follows:

1. Choose the search direction

$$s_i = -H_i g_i$$  \hspace{1cm} \text{(B.5)}

2. Find the scalar $\alpha_i > 0$ such that $f(x_i + \alpha_i s_i)$ is a minimum

with respect to $\lambda$ along the line

$$x = x_i + \lambda s_i$$  \hspace{1cm} \text{(B.6)}

3. Let

$$\Delta x_{-i} = \alpha_i s_i$$  \hspace{1cm} \text{(B.7)}

4. Then the starting point for the next iteration is given by

$$x_{i+1} = x_i + \Delta x_{-i}$$  \hspace{1cm} \text{(B.8)}

5. Evaluate $f(x_{i+1})$ and $g_{i+1}$. Note that $g_{i+1}$ is orthogonal to $\Delta x_{-i}$,

$$\Delta x_{-i}^t g_{i+1} = 0$$  \hspace{1cm} \text{(B.9)}
6. To update the matrix $H_i$, let

$$\Delta g_i = g_{i+1} - g_i$$  \hspace{1cm} (B.10)

7. Then

$$H_{i+1} = H_i + A_i + B_i$$  \hspace{1cm} (B.11)

where

$$A_i = \frac{\Delta x_i \Delta x_i^t}{\Delta x_i^t \Delta g_i}$$  \hspace{1cm} (B.12)

and

$$B_i = -\frac{H_i \Delta g_i \Delta g_i^t H_i}{\Delta g_i^t H_i \Delta g_i}$$  \hspace{1cm} (B.13)

Fletcher and Powell have proven both the stability and convergence properties of this algorithm for quadratic functions and have demonstrated that the matrices $H_i$ converge to $G^{-1}$ as $x_i$ converges to the optimum $x^*$.

In an appendix to their article, Fletcher and Powell suggest that the use of cubic interpolation to locate the directional minimums, that is, to define $\alpha_i$ at each iteration. To form this interpolation the minimum must first be bounded; this is accomplished by first finding a point $z_i$ along the line $x = x_i + \lambda z_i$ with $\lambda > 0$ such that the directional derivative has changed sign from negative to positive. If $g_z$ is the gradient at $z_i$

$$g_z^t s_i > 0$$  \hspace{1cm} (B.14)

whereas, if $g_x$ denotes the gradient at $x_i (g_x \frac{\Delta}{x_i} g_i)$,

$$g_x^t s_i < 0$$  \hspace{1cm} (B.15)
If \( f_x \) and \( f_z \) denote the function values at the points \( x_i \) and \( z_i \), then \( \alpha_i \) can be estimated with a cubic interpolation using \( f_x, f_y \) and the gradient components (directional derivatives) along \( s_i \):

\[
\alpha_i = \lambda_i \left( 1 - \frac{\mathbf{t}^t \mathbf{s}_i + w - \gamma}{\mathbf{g}_x \mathbf{s}_i - \mathbf{g}_x \mathbf{s}_i + 2w} \right)
\]

where \( \lambda_i \) is the scalar step corresponding to the point \( z_i \),

\[
z_i = x_i + \lambda_i \mathbf{s}_i
\]

and

\[
\gamma = \frac{3}{\lambda_i} (f_x - f_y) + \mathbf{g}_x \mathbf{s}_i - \mathbf{g}_y \mathbf{s}_i
\]

\[
w = \frac{1}{2} \left[ z^2 - \left( \mathbf{g}_x \mathbf{s}_i \right) \left( \mathbf{g}_y \mathbf{s}_i \right) \right]^{1/2}
\]

In the program ADOP, the point \( z_i \) is located by first choosing \( \lambda \) such that

\[
\lambda = \text{minimum of} \left\{ \phi, \frac{-2(f_x - \hat{f})}{\mathbf{g}_x \mathbf{s}_i} \right\}
\]

where \( \hat{f} \) is an estimated lower bound for \( f \) and \( \phi \) is the step such that the maximum change in any component of \( x \) is 25% of its value at \( x_i \). If the first step does not bound a minimum, an additional step is taken. Thereafter, the step size is doubled until the minimum is bounded. When several steps are necessary, \( x_i \) is changed so that the minimum is bounded by the smallest possible interval among the points examined along \( s_i \).
Equations (B.14) and (B.15) represent the conditions needed to bound a directional minimum.

Once interpolation is used, the estimate of the minimum must be checked by determining whether or not \( f(x_i + \alpha \cdot s_i) \) is less than \( f_x \) and \( f_y \). If not the interpolation is repeated over a smaller interval defined by the test point \( x_i + \alpha \cdot s_i \) and one of the endpoints \( x_i \) or \( z_i \). Which interval is used is determined from the directional derivative at the test point.
Importance (N) and \( N' \) represent the contributions toward forming a reduction minimum.

Since integration is used, the estimate of the minimum must go through the zero crossings of the function \( f(x, \alpha, \beta) \) is less than \( x \) and \( f(x, \alpha, \beta) \) is greater than \( x \) where the integration is performed over a smaller interval.

Let \( y \) be the test point \( x + \epsilon \) and one of the endpoints \( x \). If the intervals is next is determined from the integration performed at the test point.
APPENDIX C
MEASUREMENT OF BASE RESISTANCE

The empirical characterization of $r'_b$ given in Chapt. IV is based on measurements of transistor input impedance at high frequencies. The basic assumption of the method is that the input impedance may be modeled by the RC network shown in Fig. C.1. The input impedance of this circuit is given by

$$Z_{\text{in}}(j\omega) = (r'_b + r_{\pi}) \frac{1+j\omega(r'_b/r_{\pi})C_t}{1+j\omega C_t}$$  \hspace{1cm} (C.1)

A plot of the real vs. imaginary parts of (C.1) as a function of frequency results in the circular locus shown in Fig. C.2, with intercepts on the real axis of $r'_b + r_{\pi}$ at $\omega = 0$ and $r'_b$ at $\omega = \infty$.

To determine $r'_b$, the real and imaginary parts of the input impedance are measured for several frequency points in a range where they lie on a circular locus. There are usually deviations from the circle at very high frequencies. Once the circular locus is established, $r'_b$ is easily estimated by extrapolating the measurements to the $\omega = \infty$ intercept of the real axis. The bandedge of the amplifiers of interest generally lies in or near the range of frequencies where the experimental points lie on the circle. Thus, this form of measurement leads to an estimate of $r'_b$ appropriate to the bandedge response. It is in this region of the response where $r'_b$ has its most significant effect on the amplifiers considered in this study.
APPENDIX C

MEASUREMENT OF BASE RESISTANCE

The comprehensive characterization of npn transistors in Chapter VI is based on the measurement of transistor input impedance at high frequencies. The basic expression for the method is that the input impedance may be modeled by the small-signal model in Fig. C.1. The input impedance of the circuit is

\[
\frac{1}{Z_{in}} = \frac{1}{Z_{m} + Z_{C}}
\]
Fig. C.1: Circuit model for transistor input impedance.
Fig. C.2: Locus of Real vs. Imag. parts of $Z_{in}(j\omega)$ in (C.1).
An example of the measurement $r_0$ for a typical device is illustrated in Fig. C.3. The input impedance is obtained from measurements of the equivalent shunt input conductance, $G_p$, and capacitance, $C_p$, made with a Wayne-Kerr VHF Admittance Bridge, Model B801. The experimental setup is illustrated in Fig. C.4. From the equivalent $G_p$ and $C_p$ at a frequency $\Omega$, the real and imaginary parts of the input impedance are given by

\[
\text{Re}\left[Z_{\text{in}}(j\omega)\right] = \frac{G_p(\omega)}{[G_p(\omega)^2 + \omega^2 C_p(\omega)^2]} \tag{C.2}
\]

\[
\text{Im}\left[Z_{\text{in}}(j\omega)\right] = \frac{-\omega C_p(\omega)}{[G_p(\omega)^2 + \omega^2 C_p(\omega)^2]} \tag{C.3}
\]
Fig. C.3: Measured data for determining $r_b'$ in a typical device.
Fig. C.4: Experimental set up for determining $r'_b$. 

HP 606A SIGNAL GENERATOR

W-K BRIDGE

NULL DETECTOR (RECEIVER)

DEVICE UNDER TEST
APPENDIX D

DC OUTPUT LEVEL SENSITIVITY

The common-mode equivalent half circuit of Fig. D.1 can be used to show that the current source biasing in the amplifiers of Figs. 5.3 and 5.6 desensitizes the quiescent output collector voltage for the basic feedback amplifiers. For the series-series triple of Fig. 2, $I_3 = I_f$, and, neglecting base currents, the dc voltage, $V_{C3}$, may be expressed as

$$V_{C3} = V_{CC} + \frac{V_{CC} + V_{EE} - (\phi_2 + \phi_4) - \left( \frac{R_1}{R_2} + \frac{R_B}{R_2} \right) \left( V_{CC} + \phi_1 + \phi_2 \right)}{\frac{R_f}{R_3} \left( \frac{R_1}{R_2} + \frac{R_B}{R_2} \right) + \frac{R_1}{R_3}}$$

(D.1)

where $\gamma = I_C(\phi_4)/I_C(\phi_S)$. If the supply voltages and resistor ratios in (D.1) are assumed to be temperature insensitive, and if $\phi_1 = \phi_2 = \phi_3 = \phi_4$, then the temperature dependence of $V_{C3}$ is given approximately by:

$$\frac{\partial V_{C3}}{\partial T} \approx - \frac{2}{\frac{R_f}{R_3} \left( \frac{R_1}{R_2} + \frac{R_B}{R_2} \right) + \frac{R_1}{R_3}} \frac{\partial \phi}{\partial T}$$

(D.2)

For the data of Tables VI.6a and b,

$$\frac{\partial V_{C3}}{\partial T} \approx - 0.23 \frac{\partial \phi}{\partial T}$$

(D.3)

Thus, the change in $V_{C3}$ with temperature corresponds to approximately 25%
Fig. D.1: Common-mode half circuit for the basic amplifiers of Figs. 5.3 and 5.6.
of the change in a single base-emitter drop.

The voltage $V_{C2}$ in Fig. 11 corresponds to the quiescent voltage at the collector of the second stage of the feedback pair in Fig. 7. Independent of the current in $Q_3$, this voltage is given by

$$V_{C2} = V_{CC} - \frac{V_{CC} + V_{EE} - (\phi_2 + \phi_4) + \frac{R_1}{R_f} (V_{CC} + \phi_1 - \phi_3)}{2R_2 + \frac{R_2}{R_f} + \gamma}$$

Under the same assumptions as used for (D.2),

$$\frac{\partial V_{C2}}{\partial T} \approx - \frac{2R_B}{2R_2 + \frac{R_2}{R_f} + \gamma} \frac{\partial \phi}{\partial T}$$

For the data of Tables VI.2a and b,

$$\frac{\partial V_{C2}}{\partial T} \approx -0.32 \frac{\partial \phi}{\partial T}$$
A schematic of the experimental set up used to measure the frequency response of the monolithic realizations is shown in Fig. E.1. The emitter-followers $Q_1$ and $Q_2$ are used to provide low capacitance (<1pF) probes of the amplifier outputs. The amplifier is packaged in a 12 pin TO5 can and mounted in a corresponding AUGET socket. The emitter-followers are mounted as close to the output pins as possible and the inputs are brought in through 50Ω coaxial cable. The entire configuration is mounted on copper-clad board used as a ground plane.
Fig. E.1: Experimental setup for determining the gain-frequency response of the monolithic amplifier realizations.
APPENDIX F

DESCRIPTION OF DESIGN PROGRAM ADOP

The program ADOP is organized according to the flow chart shown in Fig. F.1. The subroutines in ADOP are described below.

Main Program ADOP:

1. Sets up labelled common.
2. Specifications and frequency range are entered in a data statement.
3. Reads independent variables.
4. Initializes circuit excitation.
5. Initializes tolerances for subroutine FMFP.
6. Calls the search subroutine FMFP.
7. Prints returned values of independent variables upon completion of search by FMFP.

Subroutine FMFP:

This subroutine directs the search for the minimum of the performance index. It is based on the Fletcher-Powell algorithm described in Appendix B. The routine used is an extensive modification of that available in the IBM Scientific Subroutine Package/System 360. In conducting the search for the independent variables that minimize the performance index, FMFP repeatedly calls the subroutine SOLVE which, for a given set of independent variables, evaluates the performance index and its gradient.
Fig. F.1: Organization of the program ADOP.
Subroutine SOLVE:

SOLVE is the basic routine controlling the analysis portion of ADOP. It is called from FMFP and given the values of the independent variables; it then proceeds as follows:

1. Sets up frequency iteration loop for the frequency points specified.
2. Calls subroutine NOMA which sets up the circuit equations.
3. Calls subroutine ZDCOMP which decomposes the equations into an LU form.
4. Calls subroutine ZSOLV which solves the decomposed equations for circuit response.
5. Evaluates the performance index from circuit response.
6. Sets up the excitation to the adjoint equations.
7. Calls subroutine ZSOLTR which solves for adjoint network solution from the decomposed equations and adjoint network excitation.
8. Calls subroutine GREVAL which evaluates the performance index gradient.
9. Repeats iteratively over all frequency points.
10. Prints independent variables and corresponding solutions for the performance index and its gradient.

Subroutine NOMA:

Given the independent variables, NOMA sets up the complex variable nodal admittance matrix. NOMA is configuration dependent and must be changed for each configuration. A data statement is used to enter...
all parameters pertinent to setting up the admittance matrix. NOMA also sets up the partial derivatives of elements with respect to the independent variables and places them in labelled common; these are needed in the subroutine GREVAL.

**Subroutine GREVAL:**

Given the solutions to the original and adjoint circuits, along with the partial derivatives of the branch elements with respect to the independent variables, GREVAL evaluates the gradient components of the performance index.

**Subroutine ZDCOMP:**

ZDCOMP decomposes the nodal admittance matrix, $Y$, into LU form using a Gaussian elimination

$$ Y = LU $$  \hspace{1cm} (F.1)

**Subroutine ZSOLV:**

This subroutine solves the system of equations

$$ LU\vec{v} = \vec{i} $$  \hspace{1cm} (F.2)

where $\vec{v}$ is the vector of node voltages and $\vec{i}$ is the current source vector set up in ADOP.

**Subroutine ZSOLTR:**

Recognizing that the nodal admittance matrix of the adjoint network, $\hat{Y}$, is given by

$$ \hat{Y} = Y = (LU)^t = U^t L $$  \hspace{1cm} (F.3)
ZSO LTR solves the system of equations

\[ U^T L \hat{v} = \hat{i} \quad \text{(F.4)} \]

where \( \hat{v} \) and \( \hat{i} \) are the node voltages and current excitation for the adjoint network.
APPENDIX G

LISTING OF THE PROGRAM ADOP
PROGRAM ACCP (INPUT,OUTPUT)

SERIES-SERIES TRIPLE

EXTERNAL SCLVE
COMPLEX A,V,C
DIMENSION X(15), C(15), H(165), WFA(15)

CMMCN/MATRIX/A(12,12)/SIG/VC(12),C(12)/VCLT/VR(12),VI(17)/
1 DIPI/NC,NLI/FREC/NG/POINTS/NFP,WF(10)/WEIGHT/W(13)/
2 SPEC/CASP

DATA NC,NLI,CASP/*12,15*>*1
1 NFP,WF(I),I=1,16
2 WT,IC,5,,4,,2,,1,,1,,1,,1,,1,,/
3 WFA/C,0,,C,1,,2,,3,,4,,5,,5,,5,,6,,6,,7,,7,,8,,9/

N = 11

READ 6, (X(I),I=1,N)
6 FORMAT(FIC5)
IF(X(I) .LT. C)
PRINT 13, CASP
13 FORMAT(1C11,F16.5)

SET UP CIRCUIT EXCITATION

DC 1 J=1,NC
1 C(J) = (C,C,C,C)
C(I) = (2C,,C,,C)

EPS = 1C.**4(-5)
LIMIT = 2CC
EST = 0.
CALL FVP(SCLVE,N,X,F,E,GST,EST,ESP,LIMIT,IER,H)
PRINT 2, F, (I,X(I),I=1,1)
2 FORMAT(1X,14HRETURNED FCINT//1X,IER,FCN = ,E12.5//(1X,1H,12)
1 3F = ,E12.5,10X,4FCR,12,?T = ,E12.5))
PRINT 3, IER
3 FORMAT(1//5X,22HFCRFECH COMPLETE, IER = ,12 //////)

CONTINUE
PRINT 2C
20 FORMAT(5X,32HFCR RESPONSE FOR RETURNED FCINT//1X,FREC,
1 10X,4GAIN,10X,5PHASE,11X,2HVF,12X,2HV1//)
DC 21 I=1,15
h = WFA(I)
CALL NCFA(N,X)
CALL ZCCLMP
CALL ZSCLV
AVR = REAL(V(NC11))
AVI = IMAG(V(NC11))
GAIN = SQRT((AVR**2 + AVI**2))
PHASE = ATAN2(AVI,AVR)
PRINT 201, h, (AVR, PHASE, AVR, AVI
201 FORMAT(7X,1F7.4,4X,E12.5,3X,E12.5,2X,E12.5,2X,E12.5)
SUBROUTINE FMFF(FLNCT,N,X,F,G,EST,EPS,LIMIT,IER,H)

PURPOSE
TO FIND A LOCAL MINIMUM OF A FUNCTION OF SEVERAL VARIABLES
BY THE METHOD OF FLETCHER AND POWELL

USAGE
CALL FMFF(FLNCT,N,X,F,G,EST,EPS,LIMIT,IER,H)

DESCRIPTION OF PARAMETERS
FUNCT - USER-WRITTEN SUBROUTINE CONCERNING THE FUNCTION TO
BE MINIMIZED. IT MUST BE OF THE FORM
SUBROUTINE FLMCT(ARG,VAL,GRAD)
AND MUST SERVE THE FOLLOWING PURPOSE
FOR EACH N-DIMENSIONAL ARGUMENT VECTOR ARG,
FUNCTION VALUE AND GRADIENT VECTOR MUST BE COMPUTED
AND, ON RETURN, STORED IN VAL AND GRAD RESPECTIVELY
N - NUMBER OF VARIABLES
X - VECTOR OF DIMENSION N CONTAINING THE INITIAL
ARGUMENT WHERE THE ITERATION STARTS. ON RETURN,
X HOLDS THE ARGUMENT CORRESPONDING TO THE
COMPUTED MINIMUM FUNCTION VALUE
F - SINGLE VARIABLE CONTAINING THE MINIMUM FUNCTION
VALUE ON RETURN, I.E. F=F(X)
G - VECTOR OF DIMENSION N CONTAINING THE GRADIENT
VECTOR CORRESPONDING TO THE MINIMUM ON RETURN,
I.E. G=G(X)
EST - IS AN ESTIMATE OF THE MINIMUM FUNCTION VALUE.
EPS - TOLERANCE REPRESENTING THE EXPECTED ABSOLUTE ERROR.
A REASONABLE CHOICE IS 10**(-6), I.E.
SCHEMATIC GREATER THAN 10**(-6), WHERE 0 IS THE
NUMBER OF SIGNIFICANT DIGITS IN FLOATING POINT
REPRESENTATION.
LIMIT - MAXIMUM NUMBER OF ITERATIONS.
IER - ERROR PARAMETER
IER = 0 MEANS CONVERGENCE WAS OBTAINED
IER = 1 MEANS NO CONVERGENCE IN LIMIT ITERATIONS
IER =-1 MEANS ERRORS IN GRADIENT CALCULATION
IER = 2 MEANS LINEAR SEARCH TECHNIQUE INDICATES
IT IS LIKELY THAT THERE EXISTS NO MINIMUM.
H - WORKING STORAGE OF DIMENSION N*(N+7)/2.

REMARKS
I) THE SUBROUTINE NAME REPLACING THE DUMMY ARGUMENT FLMCT
MUST BE DECLARED AS EXTERNAL IN THE CALLING PROGRAM.
II) IER IS SET TO 2 IF, STEPPING IN ONE OF THE COMPUTED
DIRECTIONS, THE FUNCTION WILL NEVER INCREASE WITHIN
A TOLERABLE RANGE OF ARGUMENT.
IER = 2 IF THE INTERVAL WHERE F INCREASES IS SMALL AND THE INITIAL ARGUMENT WAS RELATIVELY FAR AWAY FROM THE MINIMUM SUCH THAT THE MINIMUM WAS OVERLAPPED. THIS IS DUE TO THE SEARCH TECHNIQUE WHICH CUTS THE STEPSIZE UNTIL A POINT IS FOUND WHERE THE FUNCTION INCREASES.

SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED
FUNCT

METHOD
THE METHOD IS DESCRIBED IN THE FOLLOWING ARTICLE
R. FLETCHER AND M.J.C. P.COMELL, A RAPID DESCENT METHOD FOR MINIMIZATION,

*****************************************

DIMENSION FC Dummy Variables

DIMENSION H(165), X(15), G(15), XCHC(15), ASHx(15)

INTERPOLATION LIMIT
INTLT = 10

DIAGNOSTIC KEYS
NKEY3 = 1

COMPUTE FUNCTION VALUE AND GRADIENT VECTOR FOR INITIAL ARGUMENT
PRINT 1001
1001 FORMAT(5X,13HINITIAL PONIT/)
CALL FUNCT(N,X,F,G,)

RESET ITERATION COUNTER AND GENERATE IDENTITY MATRIX
IER=C
KCLAT=C
N2=N+1
N3=N2+1
N31=N3+1

1 K=N31
DC 4 J=1,N
H(K)=1.
NJ=N-J
IF(NJ)5,5,2
2 DC 3 L=1,NJ
KL=K+L
3 H(KL)=C.
4 K=KL+1

START ITERATION LOOP
5 CONTINUE
KCLAT=KCLAT +1
PRINT SC, KCOUNT
90 FORMAT(5X,17HITERATION NUMBER ,13/1)
SAVE FUNCTION VALUE, ARGUMENT VECTOR AND GRADIENT VECTOR

OLCF = F
DC S J = 1, N
K = N + J
H(K) = C(J)
K = K + N
H(K) = X(J)

DETERMINE DIRECTION VECTOR F

K = J + N
T = 0.
DO 8 L = 1, N
T = T - G(L) * H(K)
IF(L—J)6, 7, 7
6 K = K + N - L
GO TO 8
7 K = K + 1
8 CONTINUE
9 H(J) = T
PRINT 80, (I, H(I), I = 1, M
80 FORMAT (1CX, 10FX) DIRECTION VECTOR // (1CX, 1FX, 12, 3H, , 12.5))
PRINT 81
81 FORMAT (//5X, 3CF) -----------------------------/

CHECK WHETHER FUNCTION WILL DECREASE STEPPING ALONG H.

DY = 0.
HNRM = C.
GNRM = C.

CALCULATE DIRECTIONAL DERIVATIVE AND TEST VALUES FOR DIRECTION
VECTOR F AND GRADIENT VECTOR G.

DO 10 J = 1, N
HNRM = HNRM + ABS(H(J))
GNRM = GNRM + ABS(C(J))
10 DY = CY + H(J) * G(J)

REPEAT SEARCH IN DIRECTION OF STEEPEST DESCENT IF DIRECTIONAL
DERIVATIVE APPEARS TO BE POSITIVE OR ZERO.

IF(CY)11, 511, 511
11 IF(HNRM/GNRM—EPS 1 S 12, !: I 2, 12
SEARCH MINIMUM ALONG DIRECTION F
SEARCH ALONG F FOR POSITIVE DIRECTIONAL DERIVATIVE
12 FY = F
ALFA = 2. * (EST - F) / CY
PC = .249
DO 121 J = 1, N
IF(X(J) .EC. C.) CLTO 2121
ASHX(J) = ABS(F(J)/X(J))
GOTO 121
2121 ASX(J) = C.
121 CONTINUE
   ETA = 0.
   DC 121 K=1,N
   ASH = ASH*X(K)
   IF(ETA .GT. ASH) CCTO 1211
   ETA = ASH
121 CONTINUE
   AMECA = PC/ETA
   PRINT 122, ALFA, AMECA
122 FORMAT(1CX,7FAI I / ^ , b 1
   <. A // 1C X , <,» PC
   TA = , b 1 <!
   
   USE ES7IMA7F FCR STEFSIZE CNLY IF 17 IS PIJSIT AND LESS THAN
   IFCALFA )lf ,15,12
13 IF(ALFA-AMECA)14,15,15
14 AMECA=ALFA
15 ALFA=C.
C C SAVE FUNCTION AND DERIVATIVE VALUES FCR OLD ARGUMENT
C 16 FX=FY
   DX=CY
C C STEP ARGUMENT ALNNG F
DC 17 I=1,N
17 X(I)=X(I)+AMECA*F(I)
C C COMPUTE FUNCTION VALUE AND GRADIENT FCR NEW ARGUMENT
PRINT 1CC2
1002 FORMAT(5X,13HLINEAR SEARCH HEINT/)
   CALL FUNCT(N,X,F,C)
171 FY = F
C C COMPUTE DIRECTICAL DERIVATIVE CY FCR NEW ARGUMENT. TERMINATE
C SEARCH, IF CY IS POSITIVE. IF CY IS ZERO THE MINIMUM IS FOUND
   DY=C.
   DC 16 I=1,N
18 DY=DY+G(I)*H(I)
   IF(CY)19,26,22
C C TERMINATE SEARCH ALSO IF THE FUNCTION VALUE INDICATES THAT
C A MINIMUM HAS BEEN PASSED
19 IF(FY-FX)20,22,22
C C REPEAT SEARCH AND COUPLE STEPSIZE FCR FURTHER SEARCHES
20 AMECA=AMECALALFA
   ALFA=AMECA
C C END OF SEARCH CCCP
C C TERMINATE IF THE CHANGE IN ARGUMENT GETS VERY LARGE
   IF(1RN/R*AMECA-1,EL1C)16,15,21
C C LINEAR SEARCH TECHNIQUE INDICATES THAT NO MINIMUM EXISTS
21 IER=2
   RETURN
INTERPOLATION CLEICALLY IN THE INTERVAL DEFINED BY THE SEARCH
ABOVE AND COMPLETE THE ARGUMENT X FOR WHICH THE INTERPOLATION
POLYNOMIAL IS MINIMIZED.

22  INTCT = C
23  T = C
24  INTCT = INTCT + 1
25  IF(INTCT .GT. INTLT) CALL 262
26  Z = 3.*((FX-FY)/AMBCE+CX*CY
27  ALFA = AMBCE*(ABS(Z),ABS(CX),ABS(CY))
28  DALFA = Z/ALFA
29  DALFA = DALFA*DALFA-LX/ALFA*CY/ALFA
30  IF(CALFA) 513, 25, 25
31  W = ALFA*SQRT(CALFA)
32  ALFA = (CY+ALFA-Z)*AMBCE/(DY*2.*ALFA-CX)
33  DC 2c I = 1, 1
34  X(I) = X(I)+((T-ALFA)*T(I))

TERMINATE, IF THE VALUE OF THE ACTUAL FUNCTION AT X IS LESS
THAN THE FUNCTION VALUES AT THE INTERVAL ENDS. OTHERWISE REDUCE
THE INTERVAL BY CHOOSING ONE END-POINT EQUAL TO X AND REPEAT
THE INTERPOLATION, WHICH ENC-CONTIN7 IS CHOSEN DEPENDS ON THE
VALUE OF THE FUNCTION AND ITS GRADIENT AT X.

PRINT 1003
1003 FORMAT(5X,19H-INTERPOLATION PCINT/)
CALL FUNCTION(X,F,G)
261 IF(F-FX) 27, 27, 28
27  IF(F-FY) 27, 28, 28
28  DALFA=0.
29  DO 29 I = 1, 1
30  DALFA = DALFA+G(I)*T(I)
31  IF(CALFA) 32, 33, 33
32  IF(F-FX) 32, 33, 33
33  IF(FY-F) 34, 35, 35
34  IF(CY-CALFA) 35, 36, 36
35  FY = F
36  DX = CALFA
37  T = ALFA
38  AMBCE = ALFA
39  GC TC 23
40  IF(FY-F) 25, 24, 25
41  IF(CY-CALFA) 35, 36, 35
42  FY = F
43  DX = CALFA
44  AMBCE = AMBCE-ALFA
45  GC TC 221

COMPUTE DIFFERENCE VECTCRS OF ARGUMENT AND GRADIENT FROM
THE CONSECUTIVE ITERATIONS.

361 IF(NKEY3 .EQ. 1) PRINT 361C
362 IF(NKEY3 .EQ. 1) PRINT 362C
363 IF(NKEY3 .EQ. 1) PRINT 363C
GOTC 36
3610 FORMAT(5X,17HAMEQA EQUALS ZEPQ/5X, 1 3CH----------------------------------/)
3620 FORMAT(5X,15HINTERFCLATION LIMIT///5X, 1 3CH----------------------------------/)
3630 FORMAT(5X,4CHECUAL ERRCKS AND DIRECTIONAL DERIVATIVES///5X, 1 3CH----------------------------------/)
C
36 DO 37 J=1,N
   K=N+J
   H(K)=C(J)-F(K)
   K=N+K
37 XCFG(J) = X(J) - F(K)
C
TERMINATE, IF FUNCTION HAS NOT DECREASED DURING LAST ITERATION
IF(CLCF-F-EPS)51,2E,3E
C
TEST LENGTH OF ARGUMENT DIFFERENCE VECTOR AND DIRECTION VECTOR
IF AT LEAST N ITERATIONS HAVE BEEN EXECUTED, TERMINATE, IF
BOTH ARE LESS THAN EPS
38 IER=C.
39 T=C.
   Z=C.
   DC 4C J=1,N
   T = T + AES(XCFG(J))
40 Z = Z + F(K(J)) XCFG(J)
   IF(KCLNT.GF.N . ANC . HNRN . LE.EPS . ANC . 1.LE.EPS) GOTO 561
C
TERMINATE, IF NUMBER OF ITERATIONS WOULD EXCEED LIMIT
42 IF(KCLNT-LIMIT)43,5C,5C
C
PREPARE UPDATING OF MATRIX F
43 ALFA=C.
   DC 4C J=1,N
   K=J+N2
   W=C.
   DC 4C J=1,N
   KL=N+L
   W=W+F(KL)*F(K)
   IF(L-J)44,45,45
44 K=K+K-L
   GC TC 46
45 K=K+1
46 CONTINUE
   K=N+J
   ALFA=ALFA+W*F(K)
47 H(J)=W
C
REPEAT SEARCH IN DIRECTION OF STEEPEST DESCENT IF RESULTS
ARE NOT SATISFACTORY
IF(Z#ALFA)48,491,58
471 PRINT 471C
471C FORMAT(5X,29HUPDATING FAILS - REINITIALIZE///5X, 1 3CH----------------------------------/)
GOTC 1
C
C UPDATE MATRIX F

48 K=N31
DC 49 L=1,N
DO 49 J=L,N
H(K) = H(K) + XCHC(L)*XCHC(J)/Z - H(L)*H(J)/ALFA
49 K=K+1
GC TO 5
C END OF ITERATION LOC

C NC CONVERGENCE AFTER LIMIT ITERATIONS
50 IER=1
RETURN

C RESTORE OLD VALUES OF FUNCTION AND ARGUMENTS

511 PRINT 511C
GCTC 51
512 PRINT 512C
GCTC 51
513 PRINT 513C
GCTC 51
5110 FORMAT(5X,49H DIRECTIONAL DERIVATIVE NOTNEGATIVE - REINITIALIZE///
1 5X,3CH-------------------------------------------------///)
512C FORMAT(5X,22H DIRECTION VECTOR SMALL///
1 5X,3CH-------------------------------------------------///)
513C FORMAT(5X,43H NEGATIVE SCRT ARGUMENT CLFING INTERPOLATION///
1 5X,3CH-------------------------------------------------///)

C
51 DO 52 J=1,N
K=N2+J
52 X(J)=F(K)
CALL FUNCT(N,X,F,G)
C REPEAT SEARCH IN DIRECTION OF STEEPEST DESCENT IF DERIVATIVE
C FAILS TO BE SUFFICIENTLY SMALL
IF(GNRM-EFS)55,55,53
53 IF(IER)56,54,54
54 IER=-1
GCTC 1
55 IER=C
PRINT 562C
GCTC 56
5620 FORMAT(5X,22H GRADIENT LESS THAN EPS///5X,
1 3CH-------------------------------------------------///)
C
561 PRINT 561C
5610 FORMAT(5X,5EX CHANCE AND FARM LESS THAN EPS WITH AT LEAST N ITERA
1 TIONS///5X,3CF----------------------------------------///)
56 PRINT 563, KCLNT
563 FORMAT(5X,2CH AC CF ITERATIONS = ,I4///)
RETURN
C END
SUBRCLTINE SOLVE(N,X,E,F,ERGRAC)
FCR AN N-DIMENSIONAL PARAMETER XS, THE FUNCTION VALUE AND THE N-DIMENSIONAL GRADIENT VECTOR ARE RETURNED IN ER AND ERGRAD.

COMPLEX A, V, C, VA, CA
DIMENSION XS(M, N, ERGRAD(N, ERGRAD(N), ERCRC(15))

CCMNCN/MATRIX/1(12,12)/SIG/V(12), C(12)/ASIG/V(12), CA(12)/
1 VELI/VRI(12), VI(12)/AVELI/VRI(12), VI(12)/DIY/AD, NGUT/
2 FREQ/W/PCCNTS/AF, WF(12)/HEIGHT/wT(12)/SPEC/GASP/
3 ELGRAD/EGG1, ECG2, ECG, CTCECL

GI1G = C
GI2G = C
GCLC = C
TGCLG = C

CLEAR ER AND ERCRC.

ER = C
DO 101 J = 1, N
101 ERCRC(J) = C

BEGIN FREQUENCY ITERATION

I = C
102 I = I + 1
W = WF(I)

SET UP Y-MATRIX IN A

CALL ACMF(A, XS)

CECCMFCESE A INTO LU FCR - CECCMFPOSITION STORED IN A WITH
DIAGONAL ONES CF L NCT STCREC

CALL ZCCMF

SOLVE FCR ACCE VOLTAGES V

CALL ZSCLV

STORE REAL AND IMAG PARTS CF V IN VR AND VI

DO 103 J = 1, N
VR(J) = REAL(V(J))
103 VI(J) = AIMAG(V(J))

EVALUATE ER CCFCENY AND ACC TO ER

GAIA = SCFT(VR(NCLT)**2 + VI(NCLT)**2)
PHASE = ATN2(VI(NCLT), VR(NCLT))

ERC = WU(I)*((GAIA - GASF)**2)/2
ER = ER + ERC
SET UP ADJACENT EXCITATION

DC 104 J=1,NC

104 CA(J) = (C*C,C,C)

FAML = WT(I)*(1. - GASP/GAIN).

CA (INCLT) = (1.,0,C)*(-FAML*VM(NCLT)) + (C,0,1.)*FAML*VI(NCLT))

SOLVE FOR ADJACENT ACCE VOLTAGES VA

CALL ZSCLTR

STCRE REAL AND IMAG PARTS OF VA IN VAR AND VAI

DC 105 J=1,NC

VAR(J) = REAL(VA(J))

105 VAI(J) = AIMAG(VA(J))

EVALUATE ERCRAC COMPONENT AND ACCE TC ERGRAD

CALL GEREVAL(N,ERERF)

DC 106 J=1,N

106 ERCRAC(J) = ERCRAC(J) + ERERF(J)

G11G = G11G + CGI1

G12G = G12G + CGI2

CLG = CLG + CCL

TCCULG = TCCULG + CTCCU

IF(I.LT.NFP)GCTC 1C2

PRINT 115, ERI, (1,XS(I),I,ERGRAC(I),I=1,N)

115 FORMAT(10X,8HERRCR = ,E12.5//1CX,1H4,12,3H = ,E12.5,10X,4HGRAD,

1 12,2F = ,E12.5)

PRINT 116, CI1G, G12G, CLG, TCCULG

116 FORMAT(/1HERRCR = ,E12.5//1CX,1H4,12,3H = ,E12.5//5X,

1 1HGrd/1CCL = ,E12.5//5X,

3 3C-------------------------------/)

RETURN

END

SUBROUTINE NCMA(N,XP)

SERIES-SERIES TRIPLE

NCMA SETS UP THE COMPLEX Y-MATRIX IN YR AND YI WHEN GIVEN

THE N-DIMENSIONAL PARAMETER VECTOR XP. THE SUBROUTINE IS

CONFIGURATION DEPENDENT.

COMPLEX A

DIMENSION XP(N),YR(2,12,12),YI(2,12,12)

CCMN= MATRIX/A(12,12)/

1 FRECU/CIMY/NC,NCLT/PARTIAL/PECM(5),PQGM2(4),PQCM3(4),

2 PDNL(7),PEEL2(7),PEEL3(7),PCX4,PCX9,PX11(12),PX11(2)/

3 JNAC/VTF
EQUIVALENCE (YP(1), YI(1), A(1))

PARAMETER INDEPENDENT VALUES ARE ENTERED THROUGH
A DATA DECLARATION.

DATA EC1, EC2, EC3/2.120., TE1, TE2, TH3/3.22/,
  1  CS/2C17, BWF/0.0065/, VCC, VTF, TCCL/C ..020., 2/,
  2  VCE1, VCE2/1.4, 1.4/, CCC1, CCG2/CEC, .08/, CEW/1.25/,
  3  FC1, AS1, AS2/125., C6, C6/

AS1, AS2 EQUAL ONE-HALF THE AREA PER SQUARE FOR GI1, GI2

DEFINE PARAMETERS

GE1 = XP(1)
GM1 = XP(2)
GM2 = XP(3)
GL = XP(4)
EL1 = XP(5)
EL2 = XP(6)
EL3 = XP(7)
CL = 2*XP(E)**2
CF = XP(9)**2
GI1 = GM1*VTF/(VCC+.7-VCE1) + XP(1C)**2
GI2 = GM2*VTF/(VCC+1.4-VCE1-VCE2) + XP(11)**2
NE1 = 1
NE2 = 1
NE3 = 1
NR1 = 1
NB2 = 1
NB3 = 1

PARAMETER DEPENDENT ELEMENTS

GE2 = GE1
GM3 = TCCL/VTF - (CM1+CM2)
GP11 = CM1/EC1
GP12 = CM2/EC2
GP13 = CM3/EC3
GC1 = BWF*CM1
GC2 = BWF*CM2
GC3 = BWF*CM3
VCE3 = 5.1 - VCE1 - VCE2
GF = CM3*VTF/(VCE1+VCE2-1.4)
CC11 = (1./GI1)*(AS1/RH1C)*CCG1
CC12 = (1./GI2)*(AS2/RH1C)*CCG2
SCL1 = .5*NE1 + .5*NB1 - .2
SCL2 = .5*NE2 + .5*NB2 - .2
SCL3 = .5*NE3 + .5*NB3 - .2
GC1 = 33.2/(3.5*(.1+SCL1+EL1) + .2/NE1)
GC2 = 33.2/(3.5*(.1+SCL2+EL2) + .2/NE2)
GC3 = 33.2/(3.5*(.1+SCL3+EL3) + .2/NE3)
RXM1 = .21 + .2/(CM1*VTF + 1.3)
RXM2 = .21 + .2/(CM2*VTF + 1.3)
RXM3 = .21 + .2/(CM3*VTF + 1.3)
GX1 = NE1*(1.42*EL1 + .15)/RXM1
\[ GX_2 = ANB_2 \times (1.42 \times EL_2 + 0.15) / RXM_2 \]
\[ GX_3 = ANB_3 \times (1.42 \times EL_2 + 0.15) / RXM_2 \]
\[ EA_1 = NE_1 \times (0.52 \times EL_1 + 0.27) \]
\[ EA_2 = NE_2 \times (0.92 \times EL_2 + 0.27) \]
\[ EA_3 = NE_3 \times (0.93 \times EL_3 + 0.27) \]
\[ BA_1 = (EL_1 + 0.82) \times (SCL_1 + 0.82) - .78 \]
\[ BA_2 = (EL_2 + 0.82) \times (SCL_2 + 0.82) - .78 \]
\[ HA_3 = (EL_3 + 0.82) \times (SCL_3 + 0.82) - .78 \]

\[ CAA_1 = (EL_1 + 0.82) \times (SCL_1 + 1.4) \]
\[ CAA_2 = (EL_2 + 0.82) \times (SCL_2 + 1.4) \]
\[ CAA_3 = (EL_3 + 0.82) \times (SCL_3 + 1.4) \]
\[ CAT_1 = (EL_1 + 3.7) \times (SCL_1 + 4.2) - .64 \]
\[ CAT_2 = (EL_2 + 3.7) \times (SCL_2 + 4.2) - .64 \]
\[ CAT_3 = (EL_3 + 3.7) \times (SCL_3 + 4.2) - .64 \]
\[ CAP_1 = CAT_1 - CAA_1 \]
\[ CAP_2 = CAT_2 - CAA_2 \]
\[ CAP_3 = CAT_3 - CAA_3 \]
\[ CPI_1 = CEE \times EA_1 + TR \times GM_1 \]
\[ CPI_2 = CEE \times EA_2 + TR \times GM_2 \]
\[ CPI_3 = CEE \times EA_3 + TR \times GM_3 \]
\[ CCB_1 = 0.11 / (VCE_1 - 0.2) \times 1.25 \]
\[ CCB_2 = 0.11 / (VCE_2 - 0.3) \times 1.25 \]
\[ CCB_3 = 0.11 / (VCE_3 - 0.4) \times 1.25 \]
\[ CU_1 = CCP_1 \times EA_1 \]
\[ CU_2 = CCP_2 \times EA_2 \]
\[ CU_3 = CCP_3 \times EA_3 \]
\[ CY_1 = CCB_1 \times (BA_1 - EF_1) \]
\[ CY_2 = CCB_2 \times (BA_2 - EF_2) \]
\[ CY_3 = CCB_3 \times (BA_3 - EF_3) \]
\[ CS_1 = 0.44 / (VCC + 1.1 - VCE_1) \times 0.34 \]
\[ CS_2 = 0.44 / (VCC + 1.7 - VCE_1 - VCE_2) \times 0.34 \]
\[ CS_3 = 0.44 / (3.4) \times 0.34 \]
\[ CCB_1 = CA_1 \times CS_1 \]
\[ CCB_2 = CA_2 \times CS_2 \]
\[ CCB_3 = CA_3 \times CS_3 \]
\[ CCB_1 = CA_1 \times CS_1 \]
\[ CCB_2 = CA_2 \times CS_2 \]
\[ CCB_3 = CA_3 \times CS_3 \]

**PARTIAL DERIVATIVES W.R.T. GM_1.**

\[ PDGM_1(1) = -1. \]
\[ PDGM_1(2) = 1. / EC_1 \]
\[ PDGM_1(3) = TB_1 \]
\[ PDGM_1(4) = VTH / (VCC + 1.7 - VCE_1) \]
\[ PDGM_1(5) = (GM_1 / RXM_2) \times (0.2 \times VTH) / ((GM_1 \times VTH + 1.3) \times 2) \]
\[ PDGM_1(6) = 2 \times FP \]
\[ PDGM_1(7) = -(CC_11 / C_11) \times PDGM_1(4) \]

**PARTIAL DERIVATIVES W.R.T. GM_2.**

\[ PDGM_2(1) = -1. \]
\[ PDGM_2(2) = 1. / FC_2 \]
\[ PDGM_2(3) = TB_2 \]
\[ PDGM_2(4) = VTH / (VCC + 1.4 - VCE_1 - VCE_2) \]
\[ PDGM_2(5) = (GM_2 / RXM_2) \times (0.2 \times VTH) / ((GM_2 \times VTH + 1.3) \times 2) \]
\[ PCCM2(6) = EWMF \]
\[ PCCM2(7) = -(CC12/C12)*FCGM2(4) \]

**PARTIAL DERIVATIVES W.R.T. CM3.**

\[ PCDM2(1) = F/C2 \]
\[ PCDM2(2) = F/B2 \]
\[ PCDM2(3) = VTH/(VCE1+VCE2-1.4) \]
\[ PCDM2(4) = (CX2/RXM2)*(1.2*VTH)/((CM3*VTH + 1.3)**2) \]
\[ PCDM2(5) = EWMF \]

**PARTIALS W.R.T. EMITTER STRIFE LENGTHS**

\[ PDEL1(1) = NPI*1.42/RXM1 \]
\[ PDEL1(2) = CEP*NE1*9.2 \]
\[ PDEL1(3) = CCR*NE1*9.2 \]
\[ PDEL1(4) = CCE1*(SCL1+.22) - PDEL1(3) \]
\[ PDEL1(5) = CS1*(SCL1+1.4) \]
\[ PDEL1(6) = CS1*2.6 \]
\[ PDEL1(7) = (3.5/33.3)*(C11/(2.6+SCL1+EL1))**2 \]

\[ PDEL2(1) = NE2*1.42/RXM2 \]
\[ PDEL2(2) = CEP*NE2*9.2 \]
\[ PDEL2(3) = CCR*NE2*9.2 \]
\[ PDEL2(4) = CCE2*(SCL2+.22) - PDEL2(3) \]
\[ PDEL2(5) = CS2*(SCL2+1.4) \]
\[ PDEL2(6) = CS2*2.6 \]
\[ PDEL2(7) = (3.5/33.3)*(C12/(2.6+SCL2+EL2))**2 \]

**PARTIAL DERIVATIVES W.R.T. CL**

\[ PDX8 = 2.*XP(E) \]

**PARTIAL DERIVATIVES W.R.T. CF**

\[ PDX9 = 2.*XP(9) \]

**PARTIAL DERIVATIVES W.R.T. C11**

\[ PDX10(1) = 2.*XP(11) \]
\[ PDX10(2) = -(CC11/C11)*FLX1C(1) \]

**PARTIAL DERIVATIVES W.R.T. C12**

\[ PDX11(1) = 2.*XP(11) \]
\[ PDX11(2) = -(CC12/C12)*FCX11(1) \]

**CLEAR Y-MATRIX**
DC 2C1 J=1,NC
DC 201 K=1,NC
2C1 A(J,K) = (C*C*C*C)

DEFINE NON-ZERO ELEMENTS CF Y-MATRIX

YR(1,1,1) = CS + GX1
YR(1,1,2) = -GX1
YR(1,2,1) = -CX1
YR(1,2,2) = CX1 + GFI1
YR(1,2,3) = -GPI1
YR(1,3,2) = -GM1 + CPI1
YR(1,3,3) = CM1 + GFI1 + CC1 + GE1 + CF
YR(1,4,1) = -GCI1
YR(1,4,2) = -CF
YR(1,4,3) = CM1
YR(1,4,4) = -GM1 + CC1
YR(1,4,5) = CC1
YR(1,5,4) = -CC1
YR(1,5,5) = CC1 + G11 + GX2
YR(1,5,6) = -CX2
YR(1,6,5) = -CX2
YR(1,6,6) = GX2 + GFI2
YR(1,7,6) = CM2
YR(1,7,7) = CC2 + GC2
YR(1,7,8) = CC2
YR(1,8,7) = GC2
YR(1,8,8) = CC2 + GI2 + GX3
YR(1,9,8) = -CX3
YR(1,9,9) = -CX3
YR(1,10,9) = GX3 + CF13
YR(1,10,10) = -CF
YR(1,10,11) = -CF
YR(1,11,11) = CM3 + CPI3
YR(1,11,12) = CM3 + CPI3 + GC3 + CE2 + CF
YR(1,11,13) = -CC3
YR(1,11,14) = CM2
YR(1,11,15) = -CM3 + GC3
YR(1,11,16) = GC3 + CC3
YR(1,12,16) = -CC3
YR(1,12,17) = -CC3
YR(1,12,18) = GC3 + CL

YL(2,1,1) = w*CY1
YL(2,1,4) = -w*CY1
YL(2,2,2) = w*(CFI1 + CL1)
YL(2,2,3) = -w*CFI1
YL(2,2,4) = -w*CL1
YL(2,3,2) = -w*CFI1
YL(2,3,3) = w*(CFI1 + CF)
YL(2,3,10) = -w*CF
YL(2,4,1) = -w*CY1
YL(2,4,2) = -w*CL1
YL(2,4,4) = w*(CL1 + CCS1 + CY1)
YI(2,5,5) = W*(CCW1 + CC11 + CY2)
YI(2,5,6) = W*CY2
YI(2,6,6) = h*(CFI2 + CL2)
YI(2,7,5) = W*CY2
YI(2,7,6) = W*CY2
YI(2,7,7) = h*(CL2 + CCS2 + CY2)
YI(2,8,8) = h*(CCW2 + CC12 + CY3)
YI(2,9,11) = W*CY3
YI(2,9,11) = W*CY3
YI(2,11,11) = W*CY3
YI(2,11,11) = W*CY3
YI(2,12,12) = W*(CCW2 + CY3)

RETURN
END

SUBROUTINE ZCCCMP

ZCCCMP DECOMPOSES THE COMPLEX MATRIX A INTO THE LU FORM. THE NON-ZERO ELEMENTS OF L AND U ARE STORED IN THE LOWER AND UPPER TRIANGLES OF A. THE DIAGONAL ELEMENTS OF L ARE STORED IN THE A DIAGONAL. THE DIAGONAL ELEMENTS OF U ARE UNITY AND ARE NOT STORED. ALL DIAGONAL ELEMENTS OF A ARE ASSUMED TO BE NON-ZERO.

CCFLEX A, FACTCR, MLLT
CCMCMATRX/A(12,12)/CIMY/ND, NCLT

A(NMIN1 = N-1
DC 1CC J=1, NMIN1
FACTCR = (1, C, C, C)/A(J,J)
JPLUS1 = J+1
DC 1CC K = JPLUS1, NC
MLLT = -A(K,J)*FACTCR
A(K,J) = -MLLT
DC 1CC L = JPLUS1, NC
100 A(K,L) = A(K,L) + MLLT*A(J,L)
RETURN
ENC

SUBROUTINE ZSCLV

CALCULATES SOLUTION FOR LINEAR EQUATION UNKNOWN VECTOR V FROM SCALPE VECTOR C AND LU DECOMPOSITIONS OF COEFFICIENT MATRIX A. ALL VARIABLES ARE COMPLEX AND A HAS BEEN DECOMPOSED BY SUBROUTINE ZCCCMP.

CCOMPLEX A,C,V, SLM
CCMCMATRX/A(12,12)/SIC/V(12), C(12)/CIMY/ND, NOUT

V(1) = C(1).
SUBROUTINE ZSCLTR

CALCULATES SOLUTION FOR LINEAR EQUATION UNKNOWN VECTOR VA FROM
SOURCE VECTOR CA AND COEFFICIENT MATRIX A-TRANPOSE. ALL VARIABLES
ARE COMPLEX AND LU FORM OF A IS USED AS FOUND BY SUBROUTINE ZDCOMP.

COMPLEX A, CA, VA, SLW
CMATRIX/A/12,12/AISC/VA/12,CA/12/DMY/ND,NGUT

VA(1) = CA(1)/A(1,1)
DC 2CC I=2,NC
SLW = (C,C,C,C)
IMIN1 = I-1
DC 1CC J=1,IMIN1
1CC SLW = SLW * A(I,J) * VA(J)
2CC VA(I) = (VA(I) - SLW)/A(I,I)
RETURN
END

SUBROUTINE GREVAL(N,ERGFC)

SERIES-SERIES TRIPLE
EVALUATES COMPONENT OF FUNCTION GRADIENT AT FREC POINT
AND RETURNS VALUE IN N-DIMENSIONAL VECTOR ERGFC.
SUBROUTINE GREVAL IS CONFIGURATION DEPENDENT.

DIMENSION ERGFC(N)
SENSITIVITIES OF CIRCULIT ELEMENTS

DGM1 = (VR(2)-VR(3))*(VAR(4)-VAR(3)) - (VI(2)-VI(3))
1 (VAI(4)-VAI(3))

DGM2 = VR(6)*VAR(7) - VI(6)*VAI(7)

DGM3 = (VR(9)-VR(1C))*(VAR(11)-VAR(1C)) - (VI(9)-VI(11))
1 (VAI(11)-VAI(1C))

DCPI1 = (VR(2)-VR(3))*(VAR(2)-VAR(3)) - (VI(2)-VI(3))
1 (VAI(2)-VAI(3))

DCPI2 = VR(6)*VAR(6) - VI(6)*VAI(6)

DCPI3 = (VR(5)-VR(1C))*(VAR(5)-VAR(1C)) - (VI(5)-VI(1C))
1 (VAI(5)-VAI(1C))

DGC1 = (VR(4)-VR(3))*(VAR(4)-VAR(3)) - (VI(4)-VI(3))
1 (VAI(4)-VAI(3))

DGC2 = VR(7)*VAR(7) - VI(7)*VAI(7)

DGC3 = (VR(11)-VR(10))*(VAR(11)-VAR(1C)) - (VI(11)-VI(11))
1 (VAI(11)-VAI(1C))

DCPI1 = -k*((VR(2)-VR(3))*(VAR(2)-VAR(3)) + (VI(2)-VI(3))
1 (VAR(2)-VAR(3))

DCPI2 = -k*(VR(6)*VAR(6) + VI(6)*VAR(6))

DCPI3 = -k*((VR(5)-VR(1C))*(VAR(5)-VAR(1C)) + (VI(5)-VI(1C))
1 (VAR(5)-VAR(1C))

DG1 = VR(5)*VAR(5) - VI(5)*VAI(5)

DG2 = VR(6)*VAR(6) - VI(6)*VAI(6)

DCC1 = -k*(VR(5)*VAR(5) + VI(5)*VAR(5))

DCC2 = -k*(VR(6)*VAR(6) + VI(6)*VAR(6))

DGL = VR(12)*VAR(12) - VI(12)*VAI(12)

DCF = (VR(1C)-VR(3))*(VAR(1C)-VAR(3)) - (VI(1C)-VI(3))
1 (VAI(10))-VAI(1C))

DG1 = VR(2)*VAR(3) - VI(2)*VAI(3)

DG2 = VR(1C)*VAR(1C) - VI(1C)*VAI(1C)

DCF = -k*((VR(1C)-VR(3))*(VAR(1C)-VAR(3)) + (VI(1C)-VI(3))
1 (VAR(10)-VAR(3))

DCL = -k*(VR(12)*VAR(12) + VI(12)*VAR(12))

DGX1 = (VR(1)-VR(2))*(VAR(1)-VAR(2)) - (VI(1)-VI(2))
1 (VAI(1)-VAI(2))

DGX2 = (VR(5)-VR(1C))*(VAR(5)-VAR(1C)) - (VI(5)-VI(6))
1 (VAI(5)-VAI(6))

DGX3 = (VR(6)-VR(5))*(VAR(6)-VAR(5)) - (VI(6)-VI(5))
1 (VAI(6)-VAI(5))

DCL1 = -k*((VR(2)-VR(4))*(VAR(2)-VAR(4)) + (VI(2)-VI(4))
1 (VAR(2)-VAR(4))

DCL2 = -k*((VR(6)-VR(7))*(VAR(6)-VAR(7)) + (VI(6)-VI(7))
1 (VAR(6)-VAR(7))

DCL3 = -k*((VR(5)-VR(11))*(VAR(5)-VAR(11)) + (VI(5)-VI(11))
1
$DCY_1 = -w^*((VF(1)-VR(4))*(VAI(1)-VAI(4)) + (VI(1)-VI(4))*$

$DCY_2 = -w^*((VF(5)-VR(7))*(VAI(5)-VAI(7)) + (VI(5)-VI(7))*$

$DCY_3 = -w^*((VF(12)-VR(11))*(VAI(8)-VAI(11)) + (VI(8)-VI(11))*$

$DCCS_1 = -w^*(VF(4)*VI(4) + VI(4)*VR(4))$

$DCCS_2 = -w^*(VF(7)*VI(7) + VI(7)*VR(7))$

$DCCS_3 = -w^*(VF(11)*VI(11) + VI(11)*VR(11))$

$DCCW_1 = -w^*(VF(5)*VI(5) + VI(5)*VR(5))$

$DCCW_2 = -w^*(VF(12)*VI(12) + VI(12)*VR(12))$

**GRADIEN COMPONENTS**

$ERCRC(1) = CC11*ECL2$

$ERCRC(2) = CC11*PCG(N3) + DC11*FCGM1(6) + DCPI1*PCGM1(0)$

$ERCRC(3) = CC2*LC12*PCCM2(2) + DC2*FCGM2(6) + DCPI2*PCG(M3(2))$

$ERCRC(4) = CC11*PCG(M2) + DC11*FCGM1(6) + DCPI1*PCG(M3(2))$

$ERCRC(5) = CC11*PCG(N3) + DC11*FCGM1(6) + DCPI1*PCG(M3(2))$

$ERCRC(6) = CC2*PCG(M2) + DC2*FCGM2(6) + DCPI2*PCG(M3(2))$

$ERCRC(7) = CC2*PCG(M2) + DC2*FCGM2(6) + DCPI2*PCG(M3(2))$

$ERCRC(8) = PC12*ECL2$

$ERCRC(9) = PC12*PC11*CCF$

$ERCRC(10) = PC12*PC11*CCF$

$ERCRC(11) = PC12*PC11*CCF$

**ERCRC DERIVERATIVE W.R.T. TOTAL CC CURRENT**

$CTCCU = (CCM2 + PCGM3(1)*CGF13 + FCGM3(2)*DCPI3 + PCGM3(3)*GJF$

$+ FCGM3(4)*CCX3 + PCGM3(5)*DCC3)/VTH$

RETURN ENC
REFERENCES

19. Ibid.
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