

Copyright © 1999, by the author(s).  
All rights reserved.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission.

**A COMPACT AND UNIVERSAL RTD-BASED  
CNN CELL: CIRCUIT, PIECEWISE-LINEAR  
MODEL, AND FUNCTIONAL CAPABILITIES**

by

Radu Dogaru, Leon O. Chua and Martin Hanggi

Memorandum No. UCB/ERL M99/72

21 December 1999

COVER

**A COMPACT AND UNIVERSAL RTD-BASED  
CNN CELL: CIRCUIT, PIECEWISE-LINEAR  
MODEL, AND FUNCTIONAL CAPABILITIES**

by

Radu Dogaru, Leon O. Chua and Martin Hanggi

Memorandum No. UCB/ERL M99/72

21 December 1999

**ELECTRONICS RESEARCH LABORATORY**

College of Engineering  
University of California, Berkeley  
94720

# A Compact and Universal RTD-Based CNN Cell: Circuit, Piecewise-Linear Model, and Functional Capabilities

**Radu Dogaru, Leon O. Chua, and Martin Hänggi**

Electronics Research Laboratory  
Department of Electrical Engineering and Computer Sciences  
University of California at Berkeley  
Berkeley, CA 94720, USA  
E-mail: radu\_d@ieee.org

## Abstract

*A novel Cellular Neural Network (CNN) cell and its circuit realization are proposed. The theory of the multi-nested universal cell [1] is applied, and the non-monotonic current-voltage characteristic of (quantum effect based) resonant tunneling diodes (RTD) is exploited to achieve a high functionality. The proposed cell is capable of implementing arbitrary local Boolean functions with  $n$  inputs. The cell has a complexity of only  $O(n)$  in the number of devices and template elements. For comparison, the digital  $n$ -to-1 multiplexor, a functionally equivalent system has a complexity of  $O(2^n)$ . This paper presents the design principles and gives the corresponding schematic diagram of a "generic RTD-CNN cell" circuit. The design is particularly well suited for vertical integration of RTDs with FETs in high speed nanotechnologies based on III-V semiconductors. A simple, piecewise-linear mathematical model is derived and used to evaluate the functional capabilities of the RTD-CNN cell. The model was proved to be accurate enough, and, as shown in [2], only minor tuning of some of the parameters is necessary to achieve the same functionality using a Spice simulation of the same circuit, which is based on more refined physical device models.*

## 1. Introduction

The demand for high speed in signal processing parallels the increasing requirements for more memory and computing power embedded in a single chip. If the industrial VLSI technologies continue to be used, in the near future (some predictions reach as far as the year 2015) a plateau is expected to be reached in Moore's law which has accurately predicted the constant increase in density of components per chip over the last 3 decades. To avoid this event, several new devices and technologies (often referred to as nano-technologies) were proposed in the last decade to reduce the size of the active components and achieve greater functionality. While some of them are, at present, described theoretically (e.g. the "quantum dots"), and others require special operating conditions, we focused our attention on a relatively mature technology; namely the vertical integration of resonant tunneling diodes (RTD) with FETs in high speed III-V semiconductors [3]. This technology provides an increase in functionality while operating at room temperature. Our goal is to exploit the particularities of this technology to build a new generation of cellular neural networks (CNN) [4] with increased functional capability, a processing speed in the order of picoseconds, and a larger number of cells on a single CNN chip. Such intelligent chips with increased computational power and processing speed are essential to many high-tech applications, including microrobotics and integrated vision.

The CNN cell described in this paper exploits the non-monotone current-voltage (I-V) characteristic of the resonant tunneling diode (RTD) [5] to build a programmable system capable

of representing any Boolean function with  $n$  inputs while using a very limited number of devices. Up-to-date, RTD-based technologies were developed and tested for applications such as RTD-based logic gates [6,7] and memory cells [8]. However, the most advanced RTD-based logic gates families reported in the literature are *neither* programmable *nor* universal. They are usually circuits designed to implement a set of basic two-inputs gates (e.g. AND, NOT, OR, XOR) which are the building blocks of more sophisticated digital systems. Our solution is radically different and leads to a tremendous increase in functionality. Indeed, while most of the RTD-based systems reported in the literature exploit only the switching properties resulted from the region with negative differential resistance in the RTD characteristic, we exploit the *entire non-monotonic* I-V characteristic  $I = f_{RTD}(V)$  using the results of a new theory on "multi-nested" universal CNN cells [1]. The *analog and recurrently nonlinear* nature of computation in the proposed cell leads to a dramatic decrease in complexity, and, at the same time, an increase in functionality. Instead of  $O(2^n)$  devices per chip as in the case of the digital multiplexor, our cell needs only  $O(n)$  devices to achieve the same functionality<sup>1</sup>. Both the *digital multiplexor* and the *RTD-based CNN cell* are programmable systems capable of representing any of the  $2^{2^n}$  Boolean functions with  $n$  inputs. However, while in the first case, the basic building block is the *logic gate*, and such blocks are connected by a connectivity network with a complexity of  $O(2^n)$ , the RTD-CNN cell achieves the same functionality by *nonlinear analog* computation in a system where the number of connecting nodes is only  $O(n)$ .

In this paper, we investigate the class of an uncoupled CNN cell. Compared to the *standard CNN cell* [4] our design has several advantages: (a) It uses a simple synapse made of only two n-FET transistors, where the synaptic weights (or CNN templates) are always positive; (b) It expands the domain of realizable Boolean functions beyond the small class of *linearly separable* Boolean functions, while it uses exactly the same number of parameters ( $n+1$ ) to code the template; (c) It targets a promising nanotechnology, from which very high processing speeds and densities are expected.

This paper is organized as follows: The proposed RTD-CNN cell circuit and its design rules are described in Section 2. After briefly reviewing the "nesting" theory in [1], we show how it can be applied to RTD-based devices. Then we provide a detailed description and design rules for each of the three sub-circuits composing the generic RTD-CNN cell. A piecewise linear model of the cell is also given in Section 2. The functional capabilities of our RTD-CNN cell and one solution to the problem of finding the CNN genes for all Boolean functions are discussed in Section 3. Conclusions and topics of further research issues are given in Section 4.

## 2. The generic RTD-CNN cell circuit

The schematic of the generic RTD-CNN cell circuit is presented in Fig. 1. The circuit and its design rules presented in this section apply to any RTD-based technology. Within this paper the RTD-CNN cell circuit and its design rules are exemplified for a particular RTD-FET technology [3] which has been implemented and tested and for which measurements of the

---

<sup>1</sup> The most efficient solution to implement a programmable Boolean function in a digital system is to use a multiplexor with  $n$  control inputs and  $2^n$  inputs. The  $2^n$  multiplexor inputs are used as the selection inputs to specify the Boolean function and the  $n$  control inputs correspond to the  $n$  inputs of the programmed Boolean function.

devices were made available. Consequently, the RTD and FET device parameters used throughout this paper correspond to the same technology.

## RTD-CNN Cell Circuit ( $n=2$ inputs, $m=2$ nests)

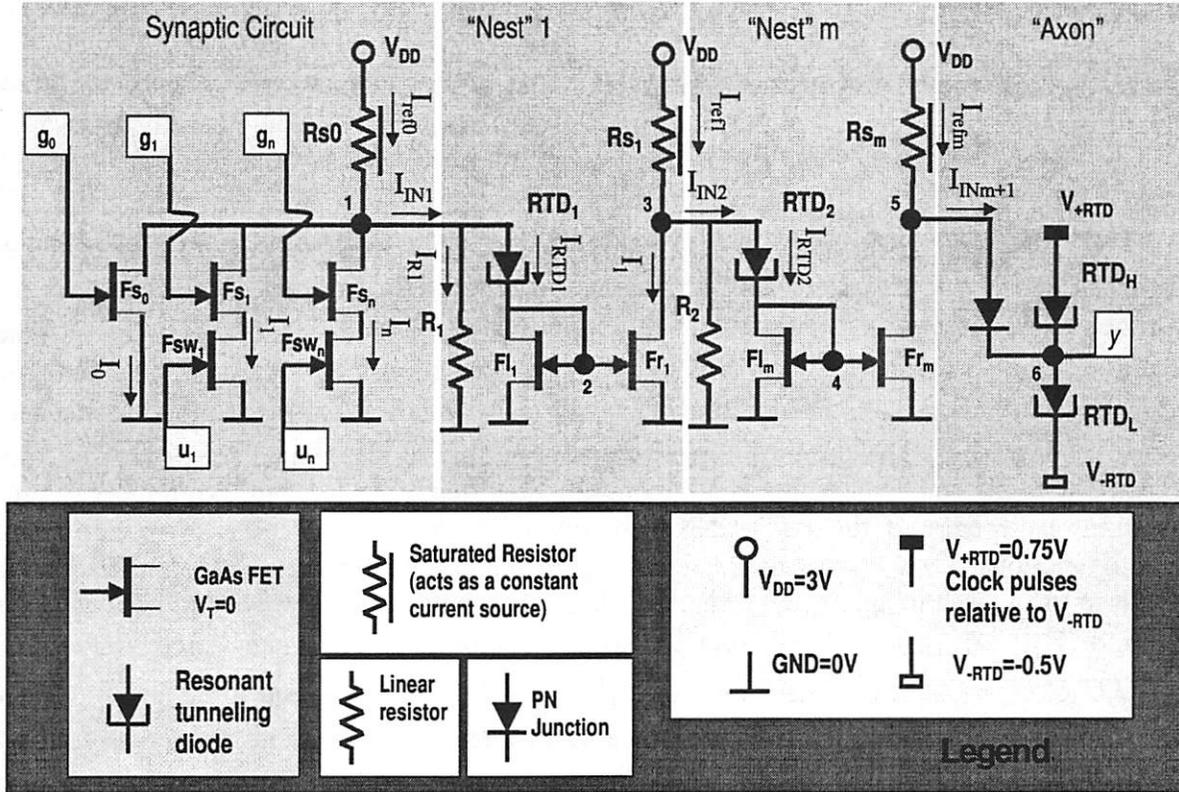


Figure 1: The schematic diagram of the generic RTD-based CNN cell. All symbols are standard except the "saturated resistor", which is defined as an active load acting as a current stabilizer or constant current source [11].

To simplify our design we have chosen the threshold voltage  $V_T = 0$  for all FET transistors which is a realistic value and can be realized by varying the technology parameters. The FET transistors are allowed to have different gate widths and lengths and therefore different gains, depending on their specific function within the circuit. All RTDs are identical. Since our purpose is to give a first-step design model for our cell, we will consider the simplest device models that are able to correctly capture the qualitative aspects and, roughly, the quantitative aspects. A piecewise-linear model is used for the RTDs and the simple generic heterojunction FET model in [9,p.330] is used for the FET transistors. The parameters of both models were determined to achieve the best match with the measured characteristics given in [3].

The piecewise-linear model derived from the RTD-CNN circuit in Fig. 1 is technology-independent, and its major role is to facilitate the theoretical analysis of our cell and, particularly, to speed up the computation in the stage of function selection (the determination of *template* (gene) parameters associated with each Boolean realization). As shown in Fig.1, all signals used for inputs ( $u_i$ ), outputs ( $y$ ) and control ( $g_i$ ), are *voltages*. However, internally, the circuit is divided into three functionally distinct sub-circuits, each one processing *currents*. The design

rules and models for each sub-circuit are derived, and the restrictions imposed by the coupling are considered. In particular, we will always ensure that the voltage in the coupling node is large enough to keep the FETs saturated.

**The binary coding of inputs and outputs:** Our cell is supposed to process binary code while using analog signals for both inputs and output. Therefore we must assign a binary code to these analog signals. Let us introduce the *binary variable*  $U_i$  to code the binary inputs, where

$$U_i = \begin{cases} 0, & \text{if } u_i < V_T \\ 1, & \text{if } u_i > V_T \end{cases}, \text{ and } u_i, i = 1, \dots, n, \text{ are the effective input voltage signals. The binary variable}$$

$Y$  is defined similarly by substituting  $U_i$  with  $Y$  and  $u_i$  with the effective output voltage  $y$  in the above definition.

The  $n+1$  *control*, or *gene inputs*, are labeled  $g_0$  (corresponding to  $z_0$  in the standard CNN cell), and  $g_i, i = 1, \dots, n$ , (corresponding to the B template parameters  $b_i, i = 1, \dots, n$  in the standard CNN cell) and they correspond to a set of parameters defining a particular Boolean realization, called a *gene* [4]. Our goal is to define a circuit modeled by the nonlinear function  $F$  so that  $Y = F(U_i, g_i, g_0)$  represents Boolean functions when all possible binary combinations of inputs are considered. The design *problem* consists in finding the whole set of (robust) genes associated with the entire set of Boolean functions (identified by an integer ID number) admitting realizations by means of the RTD-CNN cell. For example, if  $n=4$ , there are 65536 distinct Boolean functions, each being characterized by an integer ID ranging from 0 to 65535. The notation in [4] is used to specify the identifier, i.e., ID is the decimal representation of the binary number  $Y_{15}Y_{14}, \dots, Y_1$ , where  $Y_{15}$  corresponds to the combination of inputs  $U_1U_2U_3U_4 = 0000$ ,  $Y_{14}$  to  $U_1U_2U_3U_4 = 0001$ , ..., and  $Y_1$  to  $U_1U_2U_3U_4 = 1111$ . The cell is said to be *universal* if and only if at least one distinct *gene* leading to a valid circuit realization exists for *any* Boolean function with  $n$  inputs. Observe that both the space of the *gene* parameters and the space of internal cell states (voltages, currents) are *analog* while the observable cell behavior is *binary*. This is the major difference between our solution and the *digital multiplexor* for implementing a programmable CNN cell. In the case of the digital multiplexor both internal and gene parameter spaces are *binary*, leading to an *exponential* increase in the number of devices with the number of inputs  $n$ .

In defining our RTD-CNN circuit we apply the theory of universal CNN cells [1]. This theory shows that a cell is *universal* in the sense mentioned above if  $F$  is of the form:

$$Y = F(U_i, b_i, b_0) = \text{sgn}(w(\sigma)), \quad \sigma = b_0 + \sum_{i=1}^n b_i U_i \quad (1)$$

where  $\sigma$  is a *linear* projection by the orientation vector  $b_i$  of the  $n$ -dimensional input hypercube onto an analog, one dimensional *projection tape*. In the RTD-CNN circuit, the evaluation of  $\sigma$  is performed by the *synaptic sub-circuit*, and the evaluation of the sign function in the output or "*axon*" *sub-circuit*. The *discriminant function*  $w(\sigma)$  is a one-dimensional, multiple-folded function, and it plays a fundamental role in achieving the *universality*. This function is realized in our cell circuit by exploiting the non-monotone I-V characteristic of the RTDs when arranged in a cascade of similar *nesting subcircuits*. If the discriminant function is *linear* (or it is nonlinear but the equation  $w(\sigma) = 0$  has only one real root), as in the case of the standard CNN cell, only a very small fraction of the Boolean functions (the linearly separable functions) admit

realizations, therefore the standard CNN cell is *not universal*. In what follows we define the *folding degree*  $f_w$  of a *discriminant function*  $w$  as the maximum number of real roots of the equation  $w(\sigma) = z$ , where  $z$  is any real number. It is conjectured that if  $f_w \geq 2^{n-1}$ , then there *exists* an orientation (described by the set of parameters  $b_i$ ) for any of the  $2^{2^n}$  Boolean functions so that (1) is a realization of the Boolean function. This conjecture was proved for  $n \leq 4$  in [1] as well as in this paper by listing all Boolean functions and their associate genes. If the discriminant function is a canonical piecewise-linear representation [10], the above conjecture has a proof for arbitrary  $n$  [1], but in this case,  $O(2^{n-1})$  devices are required to implement the discriminant function. It is thus essential to find an efficient way of implementing a function with a *folding degree* of  $2^{n-1}$ , using a much smaller number of non-linear devices. A solution to this problem was given in the framework of the "multi-nested" CNN cell theory in [1]. It requires only  $O(n)$  non-monotone devices. In the next sub-section we generalize this idea and apply it to the case of RTD devices, exploiting their non-monotone characteristic.

## 2.1 The "nesting" principle and its RTD realization

**Proposition 1 (the "nesting" principle):** For a properly chosen set of parameters  $z_0, z_1, \dots, z_m$ , the discriminant function  $w^m(x)$  defined by the iterative mapping

$$w^0(\sigma) = z_0 + \sigma, \quad w^1(\sigma) = z_1 + g(w^0(\sigma)), \quad \dots, \quad w^m(\sigma) = z_m + g(w^{m-1}(\sigma)), \quad (2)$$

has a folding degree equal to  $p^m$ , where  $p$  is the folding degree of the *seed* function  $g(x)$ . The seed function  $g(x)$  is a non-monotonic function (e.g. a polynomial of *degree*  $p$ , or a canonical piecewise linear representation [10] with  $p-1$  absolute value terms). In [1] we called each iteration in (2) a "nesting". We do not give here the proof due to space limitations; however one may easily see it thinking of  $g(x)$  as polynomials of degree  $p$ .

The I-V characteristic of the RTD can be modeled by the following seed function with  $p = 3$  (where  $x$  plays the role of the voltage):

$$g_{RTD}(x) = \alpha x + \beta + \gamma(|x - V_p| - |x - V_v|), \quad (3)$$

where  $\alpha = g_+$ ,  $\gamma = \frac{g_+ - g_-}{2}$ ,  $\beta = \gamma(V_v - V_p)$ . Here  $g_+ = \frac{I_p}{V_p}$  is the RTD conductance on the positive resistance regions,  $g_- = \frac{I_v - I_p}{V_v - V_p}$ ,  $I_v, I_p$  are the valley and peak currents, and  $V_v, V_p$  are the valley and peak voltages of the RTD. For our example, we take  $I_v = 0.1mA$ ,  $I_p = 0.15mA$ ,  $V_v = 0.8V$ , and  $V_p = 0.4V$  which correspond to an RTD device that was effectively realized [3].

These values correspond to a negative resistance  $R_- = 1/g_- = -8k\Omega$ . The RTD characteristics and its defining parameters are presented in Fig. 2.

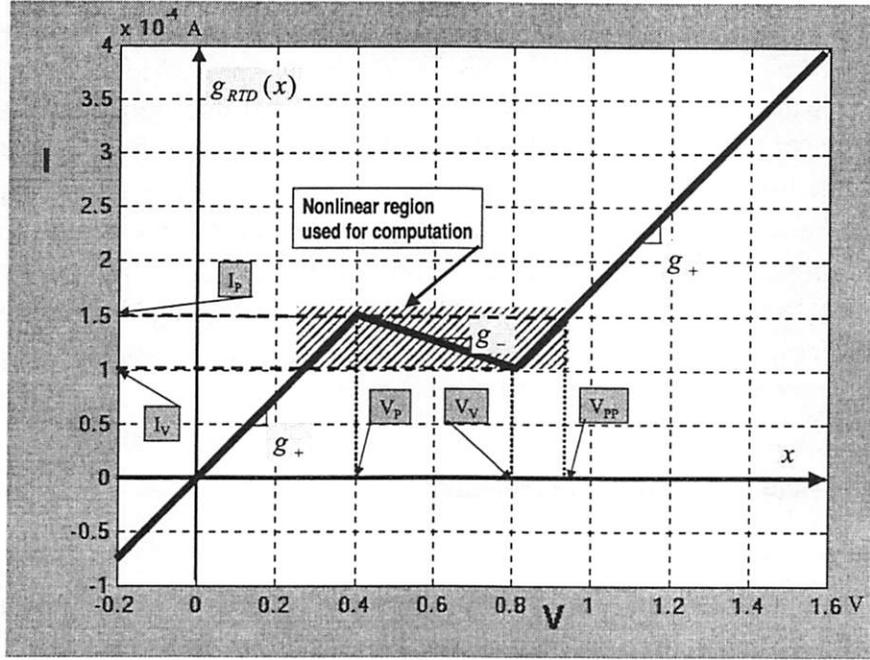


Figure 2: The current-voltage characteristic of the RTD (a canonical piecewise linear model)

Observe that the RTD alone cannot implement the "nesting principle". An ideal device would be one which uses the same type of input and output signal (i.e. a voltage, or a current). However, in the case of the RTD, the output in (3) is a current, while the input variable  $x$  is a voltage. This problem is solved by adding several FETs and designing a "nesting" sub-circuit (section 2.3) with a similar input-output characteristic, but where both the input and the output are current signals. Cascading  $m$  such circuits is equivalent to implementing Eq. (2), where  $w^m$  is substituted by  $I_{IN\ m+1}$  in our circuit diagram. This will lead to the realization of a discriminant function with a folding degree of  $3^m$ .

**Proposition 2:** For the case of a synaptic circuit with *positive* synaptic weights (or templates)  $b_i \mid_{i=0,\dots,n}$ , described by

$$\sigma = z_0 - b_0 - \sum_{i=1}^n b_i U_i \quad (4)$$

any Boolean function with  $n$  inputs  $U_i \in \{0,1\}$  has a realization (i.e. a set of parameters  $b_i \mid_{i=0,\dots,n}$  and  $z_0$ ) given by Eq. (1) where  $\sigma$  in (1) is substituted by (4) provided that the discriminant function  $w(\sigma)$  has a folding degree  $f_w \geq 1 + 2^{n-1}$ . For  $n < 4$ , we are able to prove the above proposition by listing all Boolean functions with 3 and 4 inputs and their realizations. For the general case, a formal proof is difficult to obtain. Since (4) defines our synaptic circuit, this proposition is very important because it shows that we can avoid *negative synaptic weights* if we accept one additional folding in the discriminant function. From a practical perspective, it leads

to a substantial simplification of the synaptic sub-circuit. A corollary of this proposition is that *the set of linearly separable* Boolean functions is a subset of the realizable Boolean functions obtained using a discriminant function with a folding degree  $f_w = 2$ , attainable with only one "nesting" unit. In this case, by sacrificing universality, a very compact equivalent of the uncoupled *standard* CNN cell can be realized.

**Example:** For the case  $n=4$  inputs, Proposition 2 indicates that a discriminant function with a folding degree of  $f_w \geq 9$  is required. A cascade of  $m$  RTD-based "nesting" circuits provides a discriminant function with a folding degree of  $3^m$ . The number of  $m$  of "nest" circuits equals the smallest integer greater than  $\log_3 f_w$ , and in our case it follows that  $m = 2$  "nests". The same number is required for the case of  $n=3$  inputs.

In what follows a set of design rules for the generic RTD-CNN cell circuit in Fig.1 is given, showing that it implements the theoretical principles discussed above. A simple, piecewise-linear model of the generic RTD-CNN cell is also derived, to investigate its computational capabilities. In order to have a simple description of the circuit it is assumed that all FET transistors are operated in the saturated mode<sup>2</sup> (where their drain current does not depend on the drain-source voltage), therefore being modeled by the simple parabolic model:  $I_{DS} = g(V_{GS} - V_T)^2$ . The gain  $g$  depends on the technology and the geometry of the gate. Observe that any two adjacent sub-circuits are connected via a unique node. Therefore the simple KCL expresses the coupling between two sub-circuits. With the assumption that the node voltage is large enough to keep the FET transistors in saturated mode it is possible to analyze each circuit individually and verify the assumption mentioned above for each case. The overall characteristic of the RTD-CNN circuit can then be determined by simply writing the KCL for the nodes 1,2, and 5. Design procedures for the other circuit elements are provided, such that the assumptions mentioned above are fulfilled.

## 2.2. The synaptic circuit

The role of the synaptic circuit is to implement Eq. (4) with a minimum of devices. For a programmable RTD-CNN cell, it is composed of a *saturated resistor*<sup>3</sup> source  $Rs_0$  and  $n+1$  pairs of FET cascades, each cascade being formed by a synaptic transistor  $Fs_i \big|_{i=0,\dots,n}$  and a "switch" transistor  $Fsw_i \big|_{i=1,\dots,n}$ . The first synaptic transistor  $Fs_0$  lacks its corresponding switch transistor. The geometry of all synaptic transistors is identical; therefore they are all characterized by the same gain  $g_s$ . This also applies to the "switch" transistors except that their gain  $g_{sw}$  is usually higher to ensure a low drain-source voltage drop and, accordingly, to facilitate the saturated-mode assumption for the synaptic transistors. For a custom-designed CNN cell, the synaptic

---

<sup>2</sup> Except for the switch transistors: They are operated in the linear mode when in "ON" state (i.e. the control gate voltage is larger than the threshold voltage), otherwise they cut off any current flow through the corresponding cascade.

<sup>3</sup> A saturated resistor is a convenient implementation of a constant current source [11].

transistors are removed (their drains being short-circuited to their sources), and the geometry of the "switch" transistors is variable, coding different template profiles. Applying KCL at node 1 it follows that:

$$I_{IN1} = I_{ref0} - I_0 - \sum_{i=1}^n I_i U_i \quad (5)$$

which resembles equation (4) in the theoretical model. The synaptic currents  $I_i \big|_{i=0,\dots,n}$  associated with the synaptic weights  $b_i$  in (4) are uniquely determined by the gene inputs  $g_i$  through the monotonic (and invertible) transfer function of the synaptic transistors. We restrict the variation range of the gate voltages of the synaptic transistors to:  $V_T < g_i < V_V$ . Given the maximum value of the synaptic current  $I_i^{\max}$ , it follows from the FET model that the gain of the synaptic transistors is  $G_s = I_i^{\max} / (V_V)^2$ . The gene voltages  $g_i$  should be smaller than  $V_V$  (the valley voltage of the RTD) in order to guarantee that the synaptic transistors operate in the saturated mode. The value of  $I_i^{\max}$  is determined with the formula  $I_i^{\max} = I_{ref0} / (n+1)$ , so that when all  $n+1$  synaptic transistors are turned "ON", the output current of the synaptic circuit will drop to 0. The value of the bias current  $I_{ref0}$  generated by the saturated resistor  $R_{s0}$  is determined such that it will induce a voltage equal to  $V_{pp}$  across node 1 when all synaptic transistors are "OFF". The voltage at node 1 is assumed to be almost equal to the voltage across RTD<sub>1</sub> and  $V_{pp}$  is defined as the second point on the I-V characteristic for which the current trough the RTD equals the peak current  $I_p$  (Fig.2). This value can be easily determined from (3), and is, in our case,  $V_{pp} = 1.2V$ . Assuming that the current  $I_{RTD1}$  through the RTD is much smaller than  $I_{R1}$  (see next section), the voltage on the node 1 can be approximated as  $V_1 = R_1 I_{IN1}$ . It follows that  $I_{ref0} = V_{pp} / R_1$ . For a choice of  $R_1 = 2k\Omega$  (see next sub-section), it follows that  $I_{ref0} = 0.6mA$ .

### 2.3. The "nesting" units

The purpose of a "nesting" unit is to implement one step of the iteration (2), while both the input and the output are coded as currents. Therefore, a cascade of  $m$  nesting units will implement the entire iteration (2). In what follows we will discuss the first nesting unit in Fig.1. The same design principle applies to all similar units. In addition, the  $m$  parameters  $I_{ref1}, \dots, I_{refm}$  corresponding to  $z_1, \dots, z_m$  in (2) should be optimized globally (for the whole chain of "nesting" units) so that the degree of folding reaches its maximum of  $3^m$  and the roots of  $I_{INm+1}(I_{IN1})$  are as uniformly distributed as possible. The nonlinear discriminant  $w^0(\sigma)$  in (2) corresponds to the input current  $I_{IN1}$  in our nesting sub-circuit, and the output current  $I_{INm+1}$  of the whole cascade of  $m$  nesting circuits corresponds to  $w^m(\sigma)$  in (2).

Let us now derive the design rules for the "nesting" unit. The linear resistor  $R_1$  plays the role of a current-to-voltage converter. Therefore, the voltage across the RTD will be proportional to the input current and will cause a current flow through the RTD according to the non-

monotone law (3). The value of  $R_1$  should be carefully selected. A large value leads to unstable (bi-stable) behaviors. A small value of  $R_1$  provides a low impedance voltage source for the RTD providing a good current-to-voltage converter, but will also lead to an increase in power consumption. In what follows we will consider that the geometry of the transistor  $F_{l1}$  from the current mirror ( $F_{l1}, F_{r1}$ ) is chosen such that it has a very large gain and, consequently, the voltage across node 2 is negligible for the ranges of currents flowing through this transistor. Under this assumption, we can consider the input impedance of the "nesting" unit as formed of the linear resistor in parallel to the RTD modeled by the PWL equation (3). In order to avoid instability the conductance  $1/R_1$  should be larger than the absolute value of the largest negative conductance

$g_-$  of the RTD. It follows that  $R_1 < \frac{V_v - V_p}{I_p - I_v}$ . For our example,  $R_1 < 8k\Omega$  and our choice is

$R_1 = 2k\Omega$ . The same resistor value is used for all "nesting" circuits. It follows that the relationship between the current through the RTD and the input current  $I_{IN1}$  (associated here with the generic variable  $x$ ) also has a piecewise-linear characteristic similar to (3) but with slightly changed parameters:

$$g'_{RTD}(x) = \alpha'x + \beta' + \gamma'(|x - V'_p| - |x - V'_v|) \quad (6)$$

$$\text{where} \quad \alpha' = R_1 \frac{\alpha}{1 + \alpha R_1}, \quad \gamma' = \frac{\gamma}{(1 + \alpha R_1)(1 + \alpha R_1 + 2\gamma R_1)}, \quad \beta' = \frac{\beta}{1 + \alpha R_1},$$

$V'_p = V_p(\alpha + \gamma + 1/R_1) - \gamma V_v + \beta$ , and  $V'_v = V_v(\alpha + \gamma + 1/R_1) - \gamma V_p + \beta$ . The current mirror formed of FET transistors ( $F_{l1}, F_{l2}$ ) can be described by a simple piecewise linear mathematical model and therefore the input-output relationship describing the "nesting" circuit can be written as:

$$I_{IN2}(I_{IN1}) = I_{ref1} - k \cdot \text{rect}(g'_{RTD}(R_1 I_{IN1})) \quad (7)$$

where  $k$  is the current mirror gain (in our example  $k=10$ ) and the function  $\text{rect}(x) = (x + |x|)/2$  models the rectification property of the current mirror (i.e. only positive currents  $I_{RTD1}$  entering the current mirror are reflected and amplified). The choice of  $k$  is in relation to the value of  $R_1$ . A larger  $R_1$  will imply a lower  $k$  and therefore a more compact realization ( $k$  corresponds to the ratio between the widths of the gates of the two transistors in the current mirror), but also an increased risk of unstable behavior. For our generic example, which is not yet optimized for area, the value  $k=10$  is a good choice. A similar equation can be written for any additional nesting circuit. For our example, the equation corresponding to the second (and last one in the "nesting" chain) is:

$$I_{IN3}(I_{IN2}) = I_{ref2} - k \cdot \text{rect}(g'_{RTD}(R_2 I_{IN2})) \quad (8)$$

The characteristic resulting from the cascade of the two nesting circuits (equations 7 and 8) for the optimized values of the parameters  $I_{ref1}$  and  $I_{ref2}$  is presented in Fig. 3.

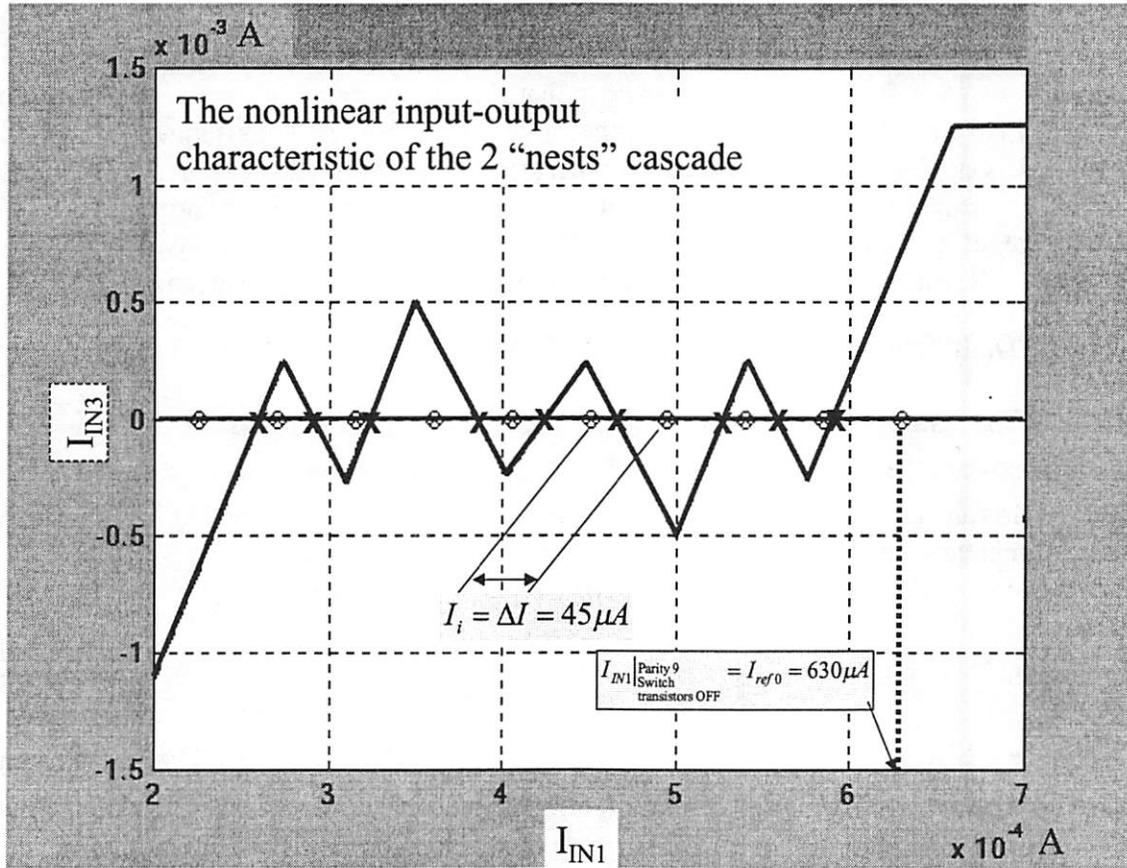


Figure 3: The input-output characteristic of the 2 "nesting"-circuit chain. Observe the folding degree of 9 and the almost uniform distribution of the roots (marked with X). The operating points corresponding to the implementation of the Parity 9 function are shown as circles.

In this case, the parameter  $I_{ref1}$  was fine-tuned to  $I_{ref1} = 1.675mA$  to obtain an almost uniformly distributed folding of degree 9. This optimization was done by simulating the input-output characteristic of the "nesting" cascade for a set of 20 samples in the interval  $I_{ref1} \in [1.2, 2]mA$ . The value of  $I_{ref2}$  is optimized such that the 9 roots of  $I_{IN3}(I_{IN1})$  are as uniformly distributed on the  $I_{IN1}$  axis as possible. The corresponding value for our example is  $I_{ref2} = 1.214mA$ .

#### 2.4. The output or "axon" unit

The output sub-circuit acts like a neural axon: when the input current exceeds a certain threshold value  $I_{TH}$ , the output will switch to an "ON" state otherwise, it remains "OFF". It is assumed that before each new operating cycle the output state is reset to the "OFF" state, by turning the power supply off (the power supply is acting as a clock signal to avoid hysteresis). The subcircuit consisting of the two connected RTDs in Fig.1 is often referred to as a MOBILE cell in the RTD literature [12]. It is characterized by two stable states corresponding to the

voltage outputs  $V_{HIGH}$  (associated to the state "ON"), and  $V_{LOW}$  (associated to the state "OFF"), and by a threshold current  $I_{TH}$  corresponding to the transition from the "OFF" to the "ON" state.

The MOBILE circuit can be described by a nonlinear ODE, and simulated numerically to determine the parameters mentioned above. Note that these parameters also depend on the choice of the voltage supply ( $V_{+RTD} - V_{-RTD}$ ) which is acting as a clock signal to avoid the hysteresis (i.e., a different current threshold for the "ON"- "OFF" transition). For our example, by choosing<sup>4</sup>  $V_{+RTD} - V_{-RTD} = 1.25V$  and using the piecewise-linear model (3), these parameters are:  $V_{OFF} = 0.45V$ ,  $V_{ON} = 0.95V$ , and  $I_{TH} = 0.044mA$ . The voltages are measured relative to  $V_{-RTD}$ . In order to provide an output voltage which satisfies our binary convention ( $Y = 1$  if  $y > 0$ , and  $Y = 0$  if  $y < 0$ ) we need to consider a floating voltage supply  $V_{-RTD} < -V_{OFF}$ . Our choice is:  $V_{-RTD} = -0.5V$ . It follows that  $V_{+RTD} = 1.25V - 0.5V = 0.75V$ . The PN junction added between nodes 5 and 6 provides a voltage translation to ensure the saturated mode operation of the FET transistor. Based on the behavior described above, the piecewise linear model of the above circuit is described by the following simple equation:

$$Y = 0.5 + 0.5 \operatorname{sgn}(I_{IN_{m+1}} - I_{TH}) \quad (9)$$

Here,  $Y$  is a Boolean variable while its corresponding analog voltage  $y$  realizes our binary coding scheme. Spice simulations described in detail in [2] have shown that the MOBILE element composed of the two RTDs can be eliminated if the quality the FET transistor and of the saturated resistor in the output is good enough to provide large enough parasitic load resistors.

### 3. Functional capabilities of the RTD-CNN cell

The piecewise-linear model of the *generic RTD-CNN cell* circuit represented by the equations (5),(7)-(9) was found to be accurate enough to capture the essential characteristic of our RTD-CNN cell. Indeed, the essential feature of our cell is its capability to provide a discriminant function with  $3^m$  folds while using only  $O(m)$  devices. Extensive Spice simulations described in [2] show that the same characteristic is obtained when our simplified model is replaced by a more accurate device description. However, the computation time required by the Spice evaluation of the input-output characteristic of the RTD-CNN cell is several orders larger (at least 100 times) than that using a simple piecewise-linear model. Therefore, our simplified model allows to evaluate the functional capabilities (the number of realizable Boolean functions and their associated genes) of the RTD-CNN cell substantially faster. An algorithmic method was developed to indicate how many distinct Boolean function realizations correspond to the RTD-CNN cell modeled by Eqs. (5)-(9). The gene realization (given as a set of synaptic currents  $I_i |_{i=0,n}$ ) is provided for each Boolean function, as well as additional information regarding the robustness of the ensemble of Boolean function realizations.

<sup>4</sup> In fact, a careful analysis indicates that the bistable behavior described above can be obtained only within a limited range of the power supply voltage, for our example:  $V_{sup} \in [0.75, 1.5]V$ , where  $V_{sup} = V_{+RTD} - V_{-RTD}$

Given the mathematical model of the RTD-CNN cell:

$$Y = F(U_i, I_{\ast}, I_o) \Big|_{i=1,n} \quad (10)$$

where  $F$  is the piecewise-linear model specified by Eqs. (5),(7)-(9), it follows that (10) determines a partition of the  $n+1$  dimensional parameter space (here, our gene parameters are the synaptic currents  $I_i$ ) into a number of polyhedrons bounded by the planar failure boundaries [4] determined by  $Y = 0.5$  (or equivalently, the argument of the sign function in Eq. (9) equals to 0). Each polyhedron is associated with the realization of a Boolean function and in general there may be one or more disjoint polyhedrons associated with the same Boolean function. In general, these polyhedrons have *different volumes* corresponding to *different degrees of robustness* for the associated Boolean function realization. The larger the volume, the better is the robustness. The *function selection* problem is defined as an analytical or algorithmic procedure to find all Boolean function realizations, and give for each one at least one (if possible the most robust) associated parameter point  $(I_i \Big|_{i=0,n})$ , or gene, within each polyhedron. The algorithm is applied only once for a given cell model and the result is stored in a list (or a table) which then allows to *select* a specified Boolean function realization using the predetermined gene. Unfortunately, the geometrical complexity of the partition induced by the piecewise-linear model in the parameter space makes an analytical solution to this problem difficult. Another possibility is to treat it as a nonlinear optimization problem and solve it with specific methods, e.g. using evolutionary algorithms or algorithms from the Simulated Annealing family. This hard optimization problem (due to the very "rugged" landscape of the error surface) should be applied iteratively for all  $2^{2^n}$  Boolean functions and it leads to very large computation times when running on usual computers. Surprisingly, it turns out that for small values of  $n$ , the fastest method is the *random exploration* of the parameter space. Each step of this process consists of randomly generating a set of parameters  $(I_i \Big|_{i=0,n})$   $0 < I_i < \frac{I_{ref0}}{n+1}$ , and evaluating (10) for all  $2^n$  binary input vectors to determine the Boolean function ID which corresponds to the polyhedron enclosing our randomly generated parameter point. Each time a new function is discovered, a list is updated with the new function ID, its actual realization, and its robustness. An improved version of this algorithm evaluates the degree of robustness *rbf* for the realization associated with a given parameter point and updates the list with the most robust realization found for each function. For the case  $n=3$ , the algorithm required only two minutes to run, a list of all 256 Boolean functions and their realizations being available at [ftp://fred.eecs.berkeley.edu/pub/radu/RTD/all\\_2bool3.mat](ftp://fred.eecs.berkeley.edu/pub/radu/RTD/all_2bool3.mat). This result confirms Proposition 2. We should stress that *all* 256 Boolean functions with 3 inputs have 2 "nests" RTD-CNN realizations with *positive* synaptic parameters  $I_i \Big|_{i=0,n}$  (and their associated gate control voltages  $g_i$ ) leading to an important reduction in the number of devices for the synaptic circuit. For the case  $n=4$  and  $m=2$  nests, the algorithm is much more time-consuming when using Matlab. After 24 hours, the realizations associated with 46000 of the 65536 Boolean functions with 4 inputs were found (i.e. 70%), the list being available at [ftp://fred.eecs.berkeley.edu/pub/radu/RTD/all\\_2bool4.mat](ftp://fred.eecs.berkeley.edu/pub/radu/RTD/all_2bool4.mat). The rate of newly discovered Boolean realizations was found to approximate the logarithmic rule  $N_f(t) = \alpha \log(\beta t)$ , where  $N_f(t)$  is the number of Boolean function realizations discovered before iteration  $t$ . The two parameters  $\alpha = 7545.7$ , and  $\beta = 262.7 \cdot 10^{-6}$  were estimated from the data available after the first 100.000 iterations. Using this formula we estimate that more than 30 days are necessary to compute the

remaining set of 30% using a SUN-ULTRA-1 workstation. However we expect that a speedup of at least a factor of 50 can be achieved in the near future by re-coding the algorithm in C and by using faster processing units. Note that this computationally intensive problem has to be solved *only once* for a given cell. It is also important to observe that the same simple algorithm can be applied without changes to the physical realization of the cell since no step of the algorithm requires any knowledge about the exact shape of the function  $F$ .

#### 4. Conclusions and perspectives

A highly compact RTD-CNN cell is proposed based on the theory of multi-nested universal CNN cells [1], and the full description of its circuit realization using resonant tunneling diodes is given. Our circuit fully supports recently reported nanotechnologies allowing operation at room temperature, such as monolithic and vertical integration of RTDs with FET transistors using III-V semiconductors [3]. The design rules and a simple piecewise-linear model for our cell are provided and the functional capabilities were evaluated for this model, expanding the theoretical results previously reported in [1] to a new class of nonlinear devices. Further simulations in Spice using realistic device models [2] show that the generic RTD CNN cell described herein and its simple piecewise linear model are accurate enough models for the starting iteration in the design process. Only minor tuning of the parameters found according to our design rules was necessary to achieve the same functionality [2]. The functional capabilities of our cell are impressive, it was demonstrated to be capable of realizing all or most (if certain robustness is imposed) Boolean functions with  $n$  inputs while having a complexity of only  $O(n)$  in the number of devices. The vertical integration of RTDs results in a significant increase in the density of cells per chip since the RTD devices do not occupy additional area. In addition, many of the linearly not separable Boolean functions with more than  $n$  inputs can be realized using the same RTD-CNN cell designed for  $n=4$  by adding only the corresponding number of synaptic and switch transistors. Indeed, as shown in Fig.3. (the operating points drawn as circles), the Parity function with 9 inputs can be realized with the RTD-CNN circuit in Fig.1 by choosing  $I_i \Big|_{i=1,n} = 0.045mA$ ,  $I_0 = 0mA$ , and  $I_{ref0} = 0.63mA$ , and keeping all other circuit elements unchanged. From right to left, each operating point corresponds to an number of 0,1,2, ...,9 binary inputs in the "1" state, and it can be easily seen that the sign of the output current toggles from +1 for an even number of "1" inputs to -1 for an odd number of "1" inputs.

The research reported herein can be extended beyond CNN architectures, and may lead to very compact implementations of other re-configurable systems which are traditionally implemented using logic gates (e.g. field programable gate arrays (FPGAs)). Concerning the RTD-CNN architecture described herein, there are still several important issues to address: (i) The improvement in terms of speed of the algorithmic method to find Boolean realizations for all possible Boolean functions; (ii) The optimization of the RTD-CNN circuit for speed, power, and occupied area; (iii) The development of a new family of RTD-CNN cells, optimized for area but with functional capability limited to linearly separable Boolean functions. In the latter case we estimate a very significant reduction in area by eliminating the current mirrors while the resulting cell will be functionally equivalent to the *standard* uncoupled CNN cell but much faster and more compact. This solution has the advantage that it will be easy to convert all existing CNN templates and information processing solutions to the new hardware platform.

**Acknowledgments:** This work was supported in part by the ONR grant N00014-99-1-0339 and by the MURI ONR grant N00014-98-1-0594. We would also like to thank Dr. D. M. Chow and Dr. J. N. Schulman for helpful discussions during the initial phase of the work.

## References

- [1] R. Dogaru and L. O. Chua, "Universal CNN cells", *Intl. Journal of Bifurcation and Chaos*, vol. 9, pp. 1-48, Jan. 1999.
- [2] M. Hänggi, R. Dogaru and L.O. Chua, "Physical modeling of RTD based CNN cells", in *IEEE International Workshop on Cellular Neural Networks and their Applications*, May 2000. submitted for publication.
- [3] K. J. Chen, T. Akeyoshi and K. Maezawa, "Monolithic integration of resonant tunneling diodes and FET's for monostable-bistable transition logic elements (MOBILE)", *IEEE Electron Device Letters*, vol. 16, pp. 70-72, February 1995.
- [4] L.O. Chua, *CNN: A paradigm for complexity*, World Scientific, 1998.
- [5] H. Mizuta and T. Tanoue, *The physics and Applications of Resonant Tunneling Diodes*, Cambridge University Press, 1995.
- [6] R.H. Mathews, J.P. Sage, T.C.L.G. Solner, S.D. Calawa, Chang-Lee. Chen, L.J. Mahoney, P.A. Maki and K.M. Molvar, "A new RTD-FET logic family", *Proceedings of the IEEE*, vol. 87, pp. 596-604, April 1999.
- [7] W. Williamson III, S. B. Enquist, D.H. Chow, H.L. Dunlap, S. Subramaniam, P. Lei, G.H. Bernstein, B.K. Gilbert, "12 GHz clocked operation of ultralow power interband resonant tunneling diode pipelined logic gates", *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 222-230, February 1997.
- [8] J.P.A. van der Wagt, A.C. Seabaugh, and E.A. Beam, III, "RTD/HFET low standby power SRAM gain cell", *IEEE Electron Device Letters*, vol. 19, pp. 7-9, January 1998.
- [9] W. Liu, I, *Fundamentals of III-V devices*, John Wiley & Sons., 1999.
- [10] L.O. Chua and S.M. Kang, "Section-wise piecewise-linear functions: canonical representation, properties and applications", *Proceedings of the IEEE*, vol. 65, pp. 915-929, June 1977.
- [11] C.P. Lee, B.M. Welch and R. Zucca, "Saturated resistor load for GaAs integrated circuits", *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-30, pp. 1007-1013, July 1982.
- [12] K. Maezawa, T. Akeyoshi, and T. Mizutani, "Functions and applications of monostable-bistable transition logic elements (MOBILE's) having multiple-input terminals", *IEEE Trans. Electron Devices*, vol. 41, pp. 148-154, 1994.