# BSIMSOI v2.0 MOSFET MODEL
# -USER'S MANUAL FOR BSIMFD2.0

by

BSIM Research Group
Professor Chenming Hu
Manual authors: JianNong Feng, WeiDong Liu,
Samuel K. H. Fung, Pin Su & Stephen Tang

Memorandum No. UCB/ERL M99/44

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**How to get a copy of this manual and source code for the model:**

**http://www-device.eecs.berkeley.edu/~bsim3soi**

**Please note that the SPICE3 core engine is distributed separately by ILP at:**

**http://www.eecs.berkeley.edu/~sotfware**

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# Part I

## Chapter 1: Introduction

BSIMSOI is the officially released SOI MOSFET model from the Device Group at the University of California at Berkeley. The model can be used for both Partially Depleted (PD) and Fully Depleted (FD) devices. This manual is just about FD. The basic IV model is modified from BSIM3v3.1 equation set. The major features are summarized as follows:

- Supports external body bias and backgate bias; a total of 6 nodes.
- Real floating body simulation in both I-V and C-V. Body potential is properly bounded by diode and C-V formulation.
- Self heating implementation improved over the alpha version.
- An improved impact ionization current model.
- Various diode leakage components and parasitic bipolar current included.
- New depletion charge model (EBCI) introduced for better accuracy in capacitive coupling prediction. An improved BSIM3v3 based model is added as well.
- Single I-V expression as in BSIM3v3.1 to guarantee continuities of $I_{ds}$, $G_{ds}$ and $G_m$ and their derivatives for all bias conditions.

# Chapter 2: Install

BSIMFD2.0 is a UNIX application. It can be run at any computers with UNIX operating systems, such as SUN Solaris, SUN4 and so on. To display curves of simulation results, the X window system is needed. To run this model, the Berkeley SPICE3f4/3E2 engine is to be installed.

When the Berkeley SPICE is installed, two of subdirectories, *src* and *util*, can be found under the SPICE home directory. BSIMFD2.0 code has to be placed at the directory of *src/lib/dev/b3soi*. There are two SPICE engine files should be replaced by the files provided with this model code, *inp2m.c* and *inpdomod.c*. The two engine files are to be placed in the directory of *src/lib/inp*. There are two model card files named *nmosfd.mod* and *pmosfd.mod* which should be placed in user directory. The source code of this model can be downloaded from the BSIMSOI webpage at *http://www-device.eecs.berkeley.edu/~bsim3soi*. After downloading the file named *bsimdd2.c.tar.Z*, it needs to be decoded by the UNIX utilities of *tar* and *compress* to get the source code. The command lines for decoding are:

```
> uncompress bsimfd2.c.tar
> tar –xvf  bsimfd2.c.tar
```

When the model source code is got, place the files in correct directories described above. Then run compiling command in SPICE home directory as following,

```
> util/build solaris     ( suppose you work with Solaris computer )
```

When finishing the compiling, the executable code named *spice3* will be placed in the directory of solaris/obj/bin which is located in outside SPICE home directory.

**We strongly recommend you read the content of *BsimTerms_use* file before you run the model code.**

# Chapter 3: Get Started

Because the executable code is located in the directory of *solaris/obj/bin* which is outside SPICE home directory, so the path need to be set in the file of *.cshrc* or *.login* so that it can be accessed anywhere.

To run the source code, type the name of executable code in user directory,

> spice3

**Remember that the model card files should be placed in this directory for BSIMSOI models.**

If the *init* file is not built ( usually like this ), the message as following will appear on the screen:

Note: can't find init file.
Program: Spice, version: 3f4
Date built: Mon Jan 11 11:27:57 PST 1999
Spice1-> _

Use *source* command to input deck file containing the circuit description you want to simulate. Suppose the deck name is *mycircuit.cir*, it is

Spice1-> source mycircuit.cir

Circuit: * This is an example for SPICE3

Spice2-> _

Typing `run` can get the simulation results. Then by typing `display`, all displayable parameters will be displayed on screen. Each displayable parameter can be printed or plotted by print command or plot command. More detail information about SPICE command refer to SPICE Manual.

# Chapter 4: Example

Here is an example to show how the model works. The example is to simulate a single transistor, doing DC analysis by sweeping $v_d$ and $v_g$, and then plot out its $I_{ds}$ curve. The circuit deck is as following.

```
* filename: exam1.cir
*
*model = bsimsoi
*Berkeley Spice Compatibility
*
* FD SOI NMOSFET, floating body simulation

vd d 0 dc 1.5
vs s 0 dc 0
ve e 0 dc 0
vg g 0 dc 3
m1 d g s e n1 w=10u l=0.25u debug=-1

.option gmin=1e-25 itl1=500
.dc vd 0 3 0.01 vg 0.5 3 0.5
.include nmosfd.mod
```

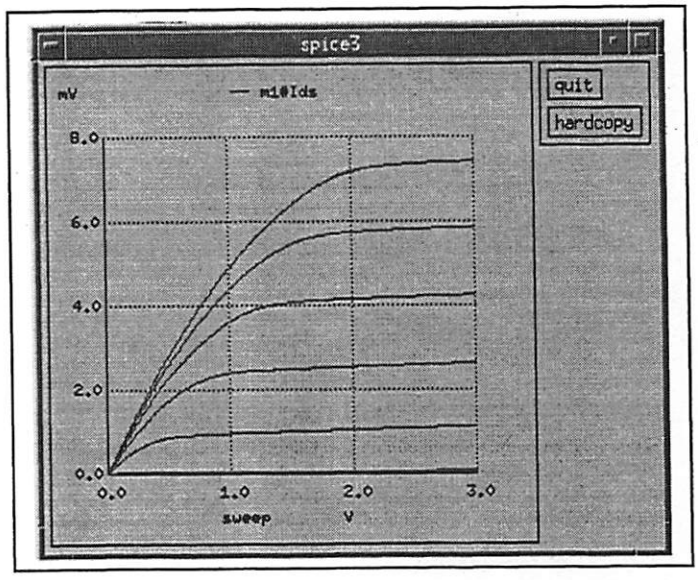
Put the file named *exam1.cir* in user's directory, and set SPICE path to *solaris/obj/bin* (suppose the computer is SUN Solaris Workstation with X-window). In user's directory, invoke `spice3`. The screen shows (the words with underline are typed by user):

Note: can't find init file.
Program: Spice, version: 3f4
Date built: Mon Jan 11 11:27:57 PST 1999
Spice 1 -> source exam1.cir

Circuit: *model = bsimsoi

Spice 2 -> run
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Spice 3 -> plot m1#Ids
Spice 4 -> quit

Are you sure you want to quit (yes)? y
Spice-3f4 done



# Part II

# Chapter 5: MOS I-V Model

## 5.1. General Information

A typical SOI MOSFET structure is shown in Fig. 5-1. The device is formed on a thin SOI film of thickness $T_{si}$ on top of a layer of buried oxide with thickness $T_{box}$. In the floating body configuration, there are four external biases which are gate voltage ($V_g$), drain voltage ($V_d$), source voltage ($V_s$) and substrate bias ($V_e$). The voltage of internal body node ($V_b$) is usually iterated in circuit simulation. If a body contact is applied, there will be one more external bias, the external body contact voltage ($V_p$).

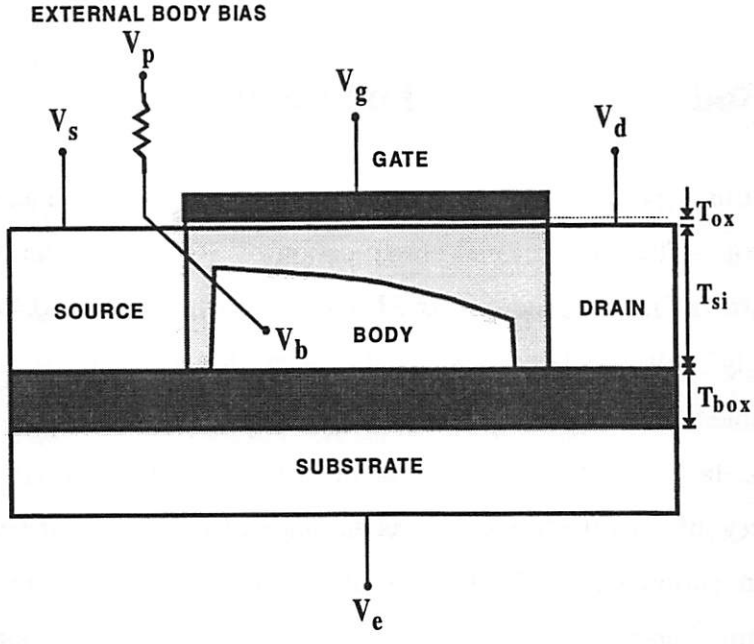



Fig. 5-1 Schematic of a typical SOI MOSFET.

There are a few FD SOI models proposed so far [5-3,4]. These models assume that the body is fully depleted in all bias configurations. FD device has very strong backgate effect. Unlike a NFD model, the body is not floating and the body charge is constant in the model derivation. The bulk charge effect and the body-drain diode characteristic are different than in a NFD device.

## 5.2. Notes on Floating Body Operation

One important question to ask is whether the body should be floating or not in a SOI model. In some proposed FD SOI models, the body voltage is directly derived from diode, leakage and impact ionization current. Therefore the body is not floating in these models. The advantages of non-body floating approach are a simpler model and faster computation time. In addition, it can model the DC kink but not the frequency or time dependent kink effect [5-9, 10]. For these reasons, the body is always floating in BSIMSOI. The floating body voltage is iterated by the SPICE engine. The result of iteration is determined by the body currents. In the case of DC, body currents include diode current, impact ionization, GIDL and body contact current. For AC or transient simulations, the displacement currents originated from the capacitance also contribute.

## 5.3. Body Potential for Full Depletion

Let us denote this potential to be $V_{bs0}$ at strong inversion and $V_{bs0eff}$ for all regions of operation. The conventional classification of SOI can be phrased as : *if $V_{bs0}$ is larger than 0, it is FD. Otherwise, it is PD/NFD.* $V_{bs0}$ higher than 0.4V can be considered as a "strongly" fully depleted device. It means that kink and floating body effect will be negligible. On the other hand, if $V_{bs0}$ is less than $-V_{dd}$, the device will be operated as NFD most of the time. Backgate bias can have strong effect on $V_{bs0}$ if the buried oxide is thin. It is very informative to use $V_{bs0}$ as an index of the degree of partial depletion instead of the conventional NFD/PD/FD classification. The relationship between $V_{bs0eff}$ and the transistor characteristic is explained first and then the formulation will be derived.

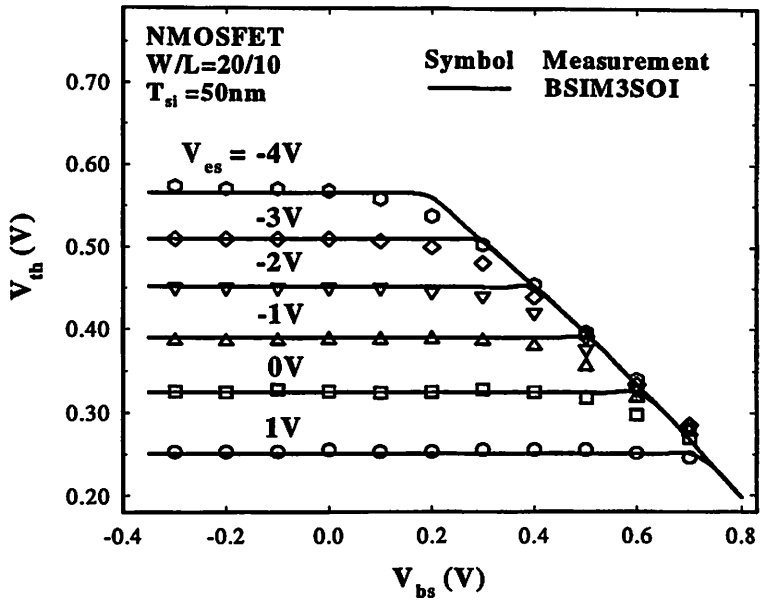



Fig. 5-2 Threshold voltage versus body bias with various backgate biases for a body-contacted FD device.

The turn-on characteristics can be affected by both the backgate bias and the external bias as shown in Fig. 5-2 and Fig. 5-3. When the device becomes FD by increasing $V_{es}$ or decreasing $V_{ps}$ (i.e. $V_{ps} < V_{bs0eff}$), the backgate bias takes over the control of $V_{th}$. In subthreshold operation, $V_{bs0eff}$ increases as $V_{gs}$ increases. As long as $V_{bs0eff}$ is smaller than the external body bias ($V_{ps}$), the subthreshold swing S is the non-ideal one. When $V_{bs0eff}$ is larger than $V_{ps}$, the device becomes FD and $V_{bs}$ is tied to $V_{bs0eff}$. Since $V_{bs}$ increases with $V_{gs}$, the subthreshold swing S is reduced.

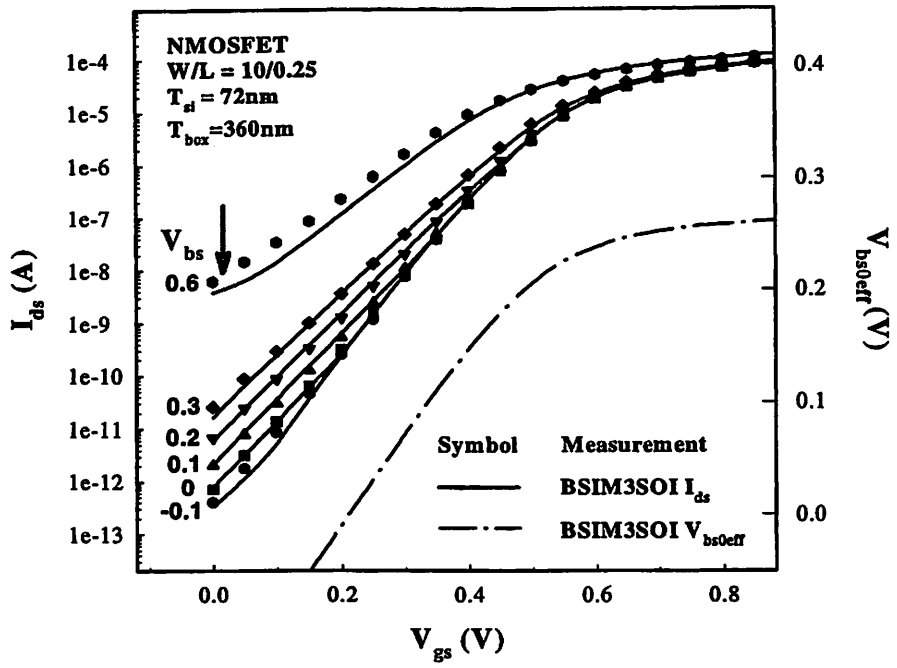



Fig. 5-3 Subthreshold characteristic of a body-contacted FD device with $T_{si}$=72nm under different body biases. The full depletion body voltage ($V_{bs0eff}$) calculated by BSIMSOI is also plotted. The device is FD or PD depending on both $V_{bs}$ and $V_{gs}$. It is PD when $V_{bs}$ has significant effect on $I_{ds}$.

In short channel devices, the source and drain junction depletion can increase $V_{bs0}$ [5-5]. Fig. 5.4 illustrates how this effect affects the turn-on characteristics. The long channel devices are partially depleted for $V_{es}$=0 and 2V. As a result, $V_{th}$ is the same for these two biases. However, short channel devices show different $V_{th}$. It is because $V_{bs0}$ becomes positive in shorter devices, i.e. the devices become FD. It is therefore necessary to model the channel length dependence of $V_{bs0}$.

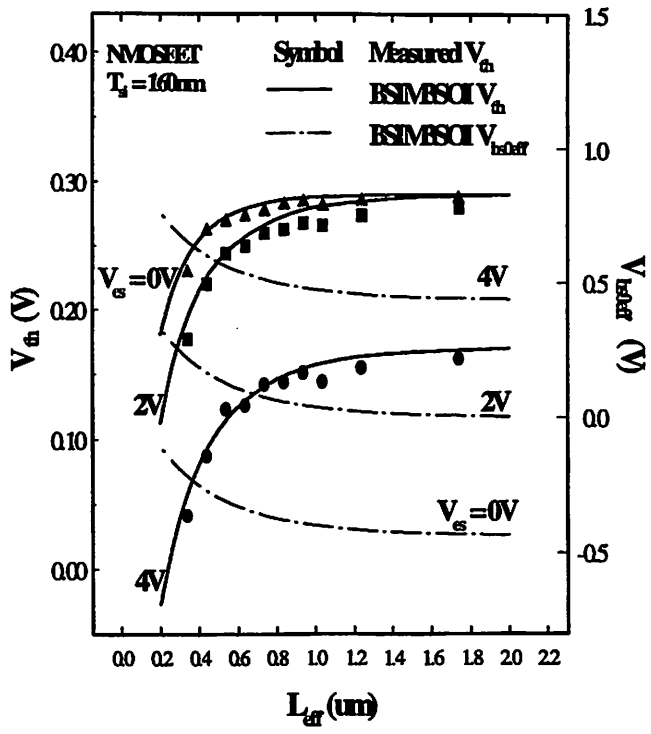



Fig. 5-4 Threshold voltage ($V_{th}$) versus effective channel length ($L_{eff}$) as a function of backgate bias for $T_{si}$ = 160nm devices. The full depletion body voltage ($V_{bs0eff}$) calculated by BSIMSOI is also plotted. At $V_{es}$=2V, $V_{bs0eff}$ is raised above zero as channel length is reduced and causes a transition to FD operation, i.e. shorter channel devices are FD while long channel devices are PD.

$V_{bs0}$ is derived as follows. With charge sheet approximation, the surface potential at source end is assumed to be clamped to $\Phi_s$ at strong inversion. Hence $V_{bs0}$ is a constant for a given backgate bias. Let us denote the $V_{bs0}$ at back interface flatband condition to be $V_{bs0t}$. $V_{bs0t}$ is also the $V_{bs0}$ for infinitely thick buried oxide. $V_{bs0t}$ is formulated as

$$V_{bs0t} = \phi_s - 0.5 \cdot Q_{si}/C_{si} + V_{bsa} + D_{vbd0} \cdot \left[ \exp\left( - D_{vbd1} \frac{L_{eff}}{2litl} \right) + 2\exp\left( - D_{vbd1} \frac{L_{eff}}{litl} \right) \right] \cdot (V_{bi} - \phi_s) \quad (5.1)$$

where $Q_{si}$ is the total body charge, $C_{si}$ is the silicon film capacitance, *litl* is the characteristic length and $V_{bi}$ is the PN junction built-in potential. $V_{bsa}$, $D_{vbd0}$ and $D_{vbd1}$ are fitting parameters. The exponential terms account for the short channel effect on $V_{bs0}$,

using a similar functional form as $V_{th}$ [12]. $V_{bsa}$ is used to account for the error between experimental measurement and the ideal $V_{bs0t}$ (equal to $\phi_s - 0.5 \cdot Q_{si}/C_{si}$). This error can be induced by non-uniform body doping. The *electrical* $T_{si}$, $C_{si}$ and $Q_{si}$ are then recalculated based on the non-zero $V_{bsa}$.

$$T_{sieff} = \sqrt{T_{si}^2 - 2\frac{\varepsilon_{si} V_{bsa}}{qN_a}}, \; C_{sieff} = \frac{\varepsilon_{si}}{T_{sieff}}, \; Q_{sieff} = qN_a T_{sieff} \tag{5.2}$$

These parameters are used in all I-V calculation.

In general $V_{bs0}$ can be expressed as a function of $V_{bs0t}$ and the backgate bias $V_{es}$ as follow

$$V_{bs0} = V_{bs0t} - K_{b1} \frac{V_{bs0t} - V_{es} + V_{fbb}}{1 + C_{sieff}/C_{box}} \tag{5.3}$$

where $K_{b1}$ is a fitting parameter and $V_{fbb}$ is the back interface flatband voltage. To keep the formulation simple, the derivation does not distinguish between back interface depletion or accumulation.

In order to extend the full depletion body potential into weak inversion, the full depletion threshold voltage ($V_{thfd}$) is first calculated by using normal $V_{th}$ calculation with $V_{bs}$ substituted by $V_{bs0}$. In subthreshold, $V_{bs0eff}$ and $V_{bs0teff}$ are formulated as linear functions of $V_{gs}$

$$V_{bs0eff} = V_{bs0} + n_{Fb}\left(V_{gs} - V_{thfd}\right) \tag{5.4}$$

$$V_{bs0teff} = V_{bs0t} + \left(V_{gs} - V_{thfd}\right) \tag{5.5}$$

where $n_{Fb}$ is the front gate to body potential coupling ratio. This ratio is one for infinite $T_{box}$ but less than one for finite $T_{box}$ (Fig. 5.5). $n_{Fb}$ is derived as follows:

At the threshold of full depletion, $V_{bseff} = V_{bs0mos}$ where $V_{bs0mos}$ is the effective $V_{bs}$ if $V_{bs}=V_{bs0}$. The gate to body charge capacitance in our CV model is

$$\frac{dQ_b}{dV_g} = \frac{C_{ox}}{\sqrt{1 + \frac{4}{K_1^2}\left(\phi_s + K_1\sqrt{\phi_s - V_{bs0mos}} - V_{bs0mos}\right)}} \tag{5.6}$$

Since the body-to-gate coupling factor is $\frac{\frac{dQ_b}{dV_g}}{\frac{dQ_b}{dV_g}+C_{box}}$, then

$$n_{Fb}=\frac{1}{1+K_{3b}\frac{C_{box}}{C_{ox}}\sqrt{1+\frac{4}{K_1{}^2}\left(\phi_s+K_1\sqrt{\phi_s-V_{bs0mos}}-V_{bs0mos}\right)}} \tag{5.7}$$

where $K_{3b}$ is a fitting parameter. This formulation allows the best match for the coupling factor between I-V and C-V models.

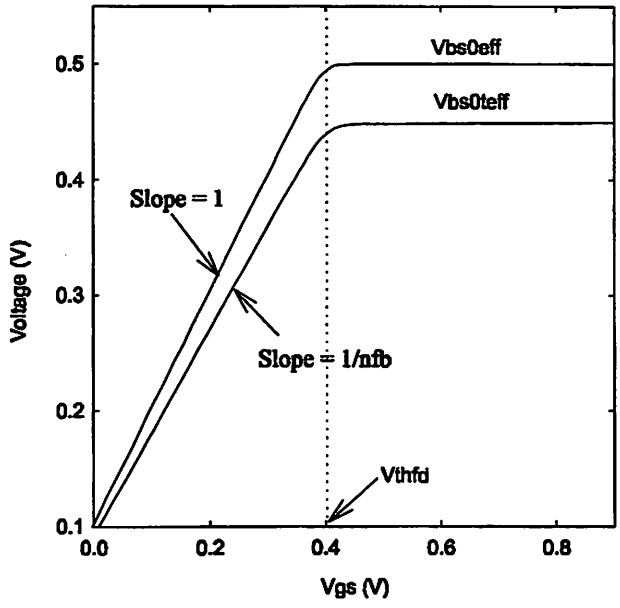



Figure 5-5 $V_{bs0eff}$ and $V_{bs0teff}$ vs. $V_{gs}$.

## 5.4. Effective $V_{bs}$

In BSIMSOI, the bulk equation for threshold and mobility calculation are used directly by replacing $V_{bs}$ with $V_{bseff}$. In bulk, $V_{bs}$ refers to the body bias of a neutral body region. An alternative interpretation is that the electric field coming from the surface channel is terminated in the body. This condition is not always true in SOI. When $V_{bs} < V_{bs0teff}$, the channel depletion can reach the buried oxide and the electric field terminates in the substrate below the buried oxide. In other words, the channel is coupled to the backgate. Since device parameters $V_{th}$ and $\mu_{eff}$ at small $V_{ds}$ depend on the vertical E-field at channel,

it is necessary to derive an effective $V_{bs}$ that gives the same vertical electric field. The $V_{bseff}$ calculation is illustrated in Fig. 5-6 and the expression of $V_{bseff}$ is

$$V_{bseff} = V_{bs} - \frac{C_{sieff}\left(V_{bs0teff} - V_{bs}\right)^2}{2 \cdot Q_{sieff}} \tag{5.8}$$

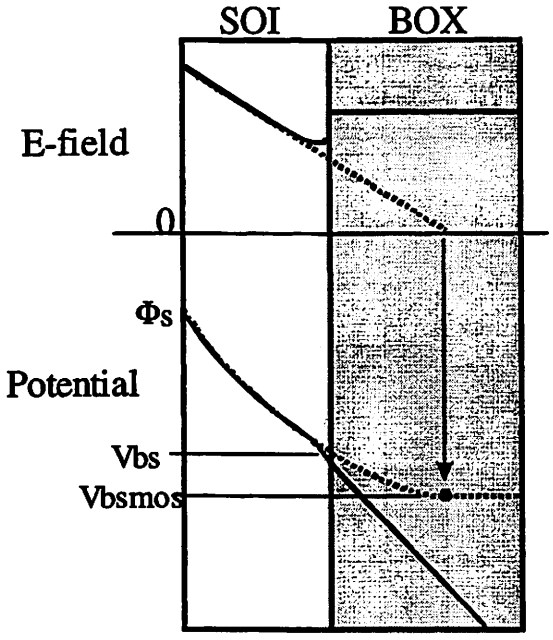



Figure 5-6 Diagram to illustrate the calculation of $V_{bseff}$. The electric field at the bottom of silicon film is extrapolated to zero. By assuming the absence of buried oxide, the potential at this point is $V_{bseff}$.

The difference between $V_{bseff}$ and $V_{bs}$ becomes significant only if a large negative $V_{es}$ is applied.

In BSIMSOI, $V_{bs}$ is used for diode and BJT calculation while $V_{bseff}$ is used for MOS calculation. When $V_{bs} < V_{bs0teff}$, $V_{bseff}$ is smaller than $V_{bs}$. $V_{bs}$ has a lower bound of $V_{bs0eff}$. When $V_{bs} > V_{bs0teff}$, $V_{bs}$ and $V_{bseff}$ are equal up to the point when $V_{bs}$ is close to the strong inversion surface potential $\Phi_s$. This is because the MOS model becomes invalid at this body bias. $V_{bseff}$ is clamped below $\Phi_s$ by a smoothing function.

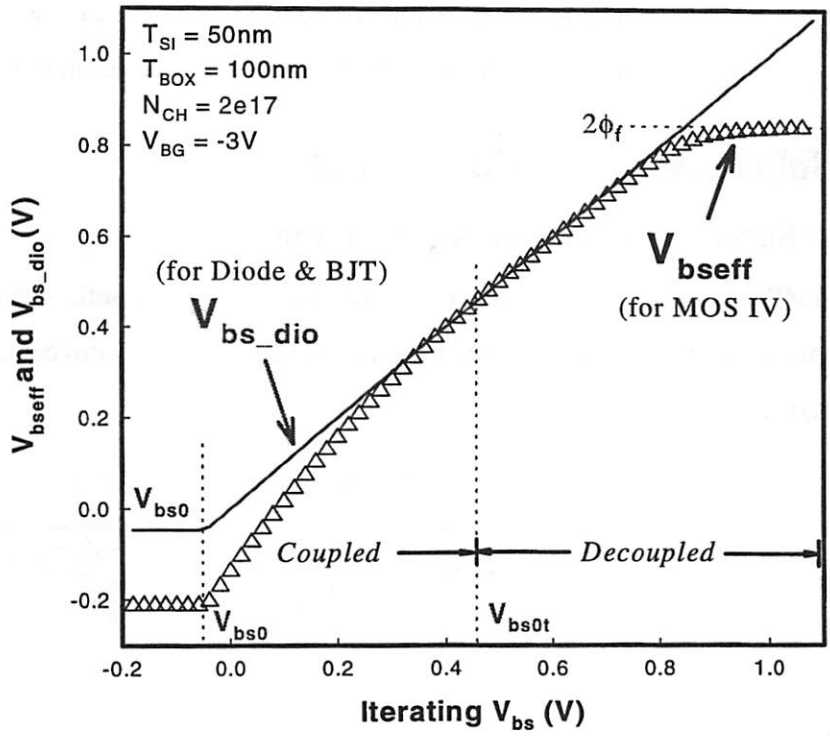



Figure 5-7 $V_{bs\_dio}$ and $V_{bseff}$ vs. the $V_{bs}$ being iterated by SPICE. $V_{bs\_dio}$ is used for diode & BJT calculation while $V_{bseff}$ is used for MOSFET.

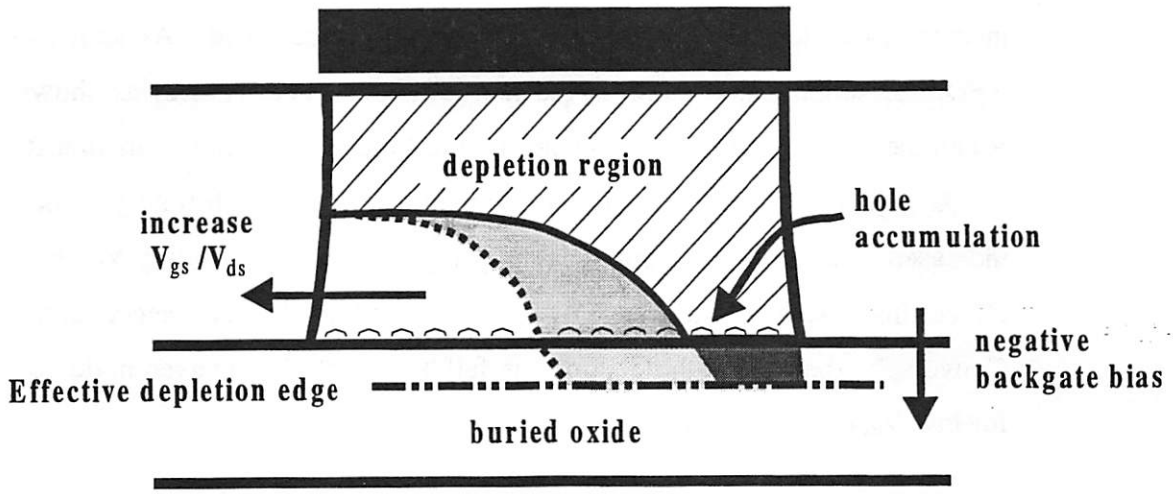



Fig. 5-8 Illustration for the dynamic depletion bulk charge effect. When a negative backgate bias is applied, a hole accumulation layer is formed. It extends the effective depletion edge into the buried

oxide and then the bulk charge effect is increased. This backgate effect is stronger under large gate and drain biases.

## 5.5. Subthreshold Drain Current

### 5.5.1 Subthreshold current expression

BSIMSOI uses a single current formula with a smooth transition from strong inversion to subthreshold. The formula is based upon $V_{gsteff}$ concept, directly borrowed from BSIM3v3:

$$V_{gsteff} = \frac{2nv_t \ln[1+\exp(\frac{V_{gs\_eff}-V_{th}}{2nv_t})]}{1+2nC_{ox}\sqrt{\frac{2\Phi_s}{q\varepsilon_{si}N_{ch}}}\exp\left(-\frac{V_{gs\_eff}-V_{th}-2V_{off}}{2nv_t}\right)} \quad (5\text{-}9)$$

### 5.5.2. Ideal, non-ideal, supra-ideal swing

The $V_{bs0eff}$ and $V_{bseff}$ formulation described in sections 5.4 and 5.5 can yield the experimentally observed SOI subthreshold phenomena. Assume $V_{ds}$=0. When the device is in accumulation, the depletion layer width is zero, and the device is NFD. As $V_{gs}$ increases, the device is NFD until the film is fully depleted. As long as the device is NFD, the subthreshold slope is the non-ideal one (>60mV/dec) as shown in Fig. 5.3. When the device is FD, the non-ideal subthreshold slope becomes an almost ideal one.

At high $V_{ds}$, body potential can be modulated by the substrate current $I_{sub}$. As $V_{gs}$ is increased, $I_{sub}$ increases to appreciably change equilibrium floating $V_{bs}$. Because of body effect, this translates to a change of $V_{th}$ vs. $V_{gs}$, and results in a steeper subthreshold slope. Conversely, the subthreshold slope can fall below 60mV/dec even in devices that are FD for low $V_{ds}$ (see Fig. 5.9).

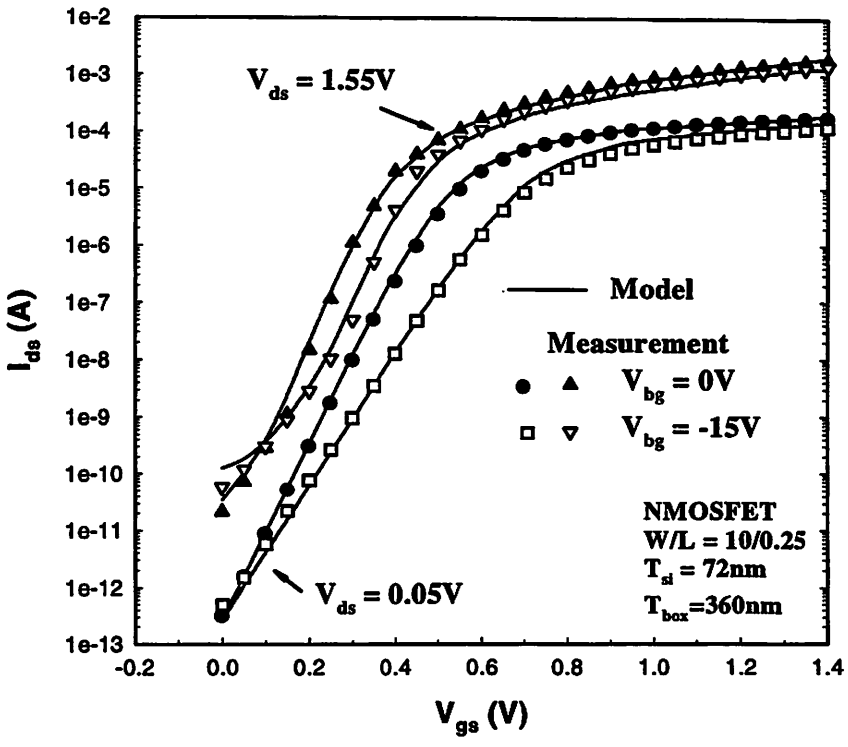



Figure 5-9 Subthreshold characteristic of a floating body "FD" device under different backgate and drain bias. The non-ideal subthreshold swing at low $V_{ds}$ and anomalous swing at high $V_{ds}$ are PD like behaviors brought on by negative $V_{bg}$.

## 5.6. Single Drain Current Equation

The effective drain voltage $V_{dseff}$ and effective gate overdrive voltage $V_{gsteff}$ in BSIM3v3 are used in this model to link subthreshold, linear and saturation operation regions into an single expression. With the use of effective body voltage ($V_{bseff}$) and effective bulk charge factor ($A_{beff}$), the single continuous drain current formulation from BSIM3v3 can be used directly,

$$I_{ds,MOSFET} = \frac{I_{ds0}(V_{dseff})}{1+\frac{R_{ds}I_{dso}(V_{dseff})}{V_{dseff}}}\left(1+\frac{V_{ds}-V_{dseff}}{V_A}\right) \tag{5-10}$$

where $R_{ds}$ is the source/drain series resistance, $\mu_{eff}$ is the mobility, $E_{sat}$ is the critical electrical field at which the carrier velocity becomes saturated and $V_A$ accounts for

channel length modulation (CLM) and DIBL as in BSIM3v3. The substrate current body effect (SCBE) on $V_A$ is eliminated because it has been taken into account explicitly by the floating body in SOI.

## 5.7. Modified Impact Ionization Current

DC I-V curves in SOI depend on impact ionization current $I_{ii}$ and so does the frequency dependence of output resistance [5-10]. That is why, unlike in bulk MOSFET simulations, it is crucial to model $I_{ii}$ correctly. The classical $I_{ii}$ model [5-11] is recalled as

$$I_{ii} = \frac{\alpha_0 + \alpha_1 L_{eff}}{L_{eff}} \cdot I_d \cdot (V_{ds} - V_{dsat}) \cdot \exp\left(-\frac{\beta_0}{V_{ds} - V_{dsat}}\right) \tag{5-11}$$

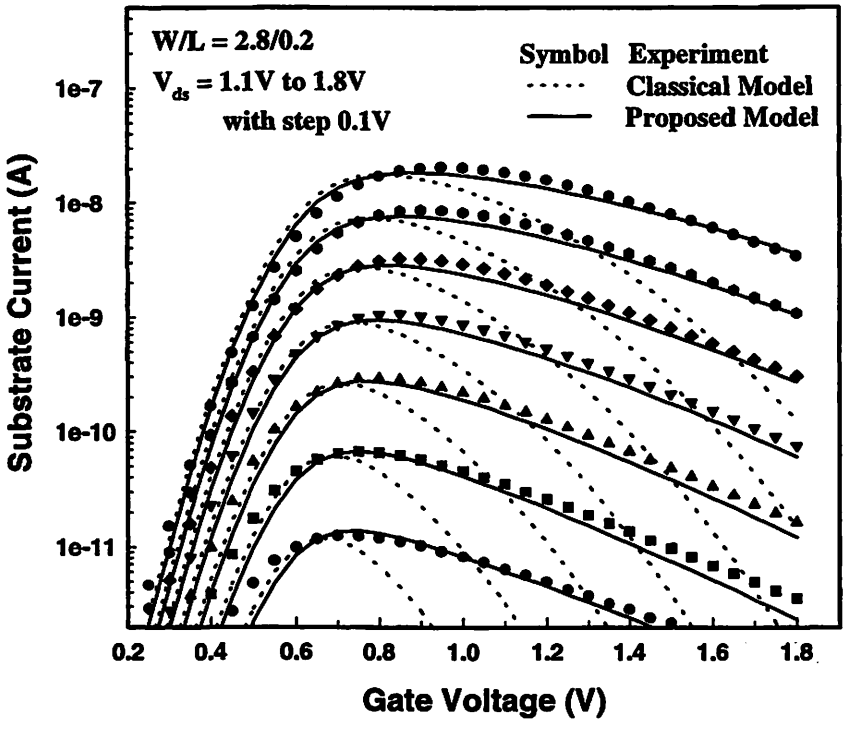



Fig. 5-10 Substrate current of a L=0.2μm device as a function of gate voltage.

Notice that $\alpha_1$ is added in BSIM3v3.2 to improve the channel length dependence. The classical model works well for long channel and predicting the peak $I_{ii}$. The $I_{sub}$ versus $V_{gs}$ plot of long channel devices usually shows a bell-shape. However, such plot of a

0.2μm device from current technology shows flatter curves as shown in Fig 5.13. Significant discrepancy is observed, especially for high gate bias. It is believed that $V_{dsat}$ is not well modeled, causing a discrepancy. By using (5-12), $V_{dsat}$ is extracted from the measured $I_{ii}$ for the 0.2um device with $\alpha_0$, $\alpha_1$ and $\beta_0$ extracted at the threshold region. In Fig. 5.11, the extracted $V_{dsat}$ is compared with the $V_{dsat}$ used for drain current computation. The extracted $V_{dsat}$ has a weaker gate voltage dependence. The slope of curves also has a strong $V_{ds}$ dependency.

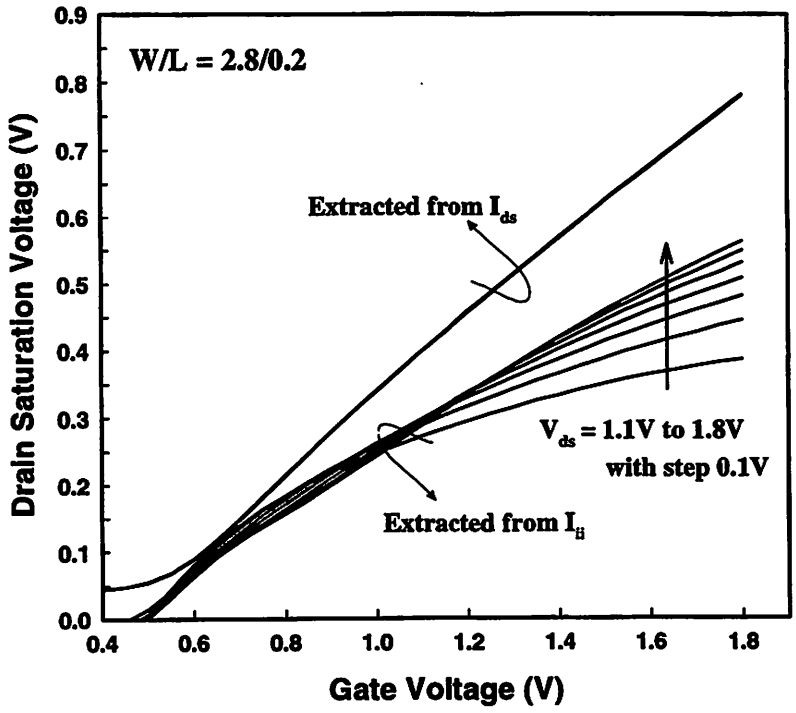



Fig. 5-11 $V_{dsat}$ extracted from measured $I_{ii}$ in comparison with $V_{dsat}$ extracted from $I_d$ characteristics for a L=0.2μm device.

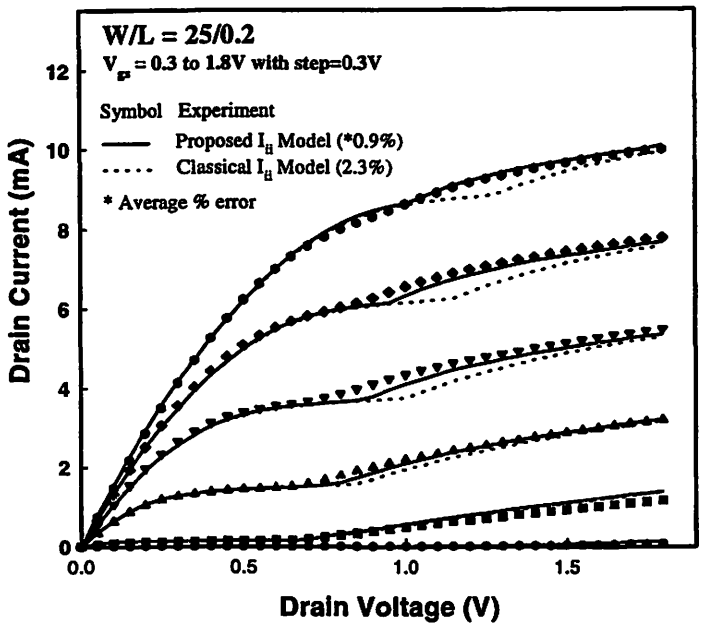



Fig. 5-12 Drain current characteristics of a L=0.2μm device.

One possible physical explanation is the channel length modulation at saturation that reduces the effective channel length. To model such behavior, we propose to use a different drain saturation voltage $V_{dsatii}$ to replace the $V_{dsat}$ in (5.15). $V_{dsatii}$ is formulated by adding two modifiers $M_1$ and $M_2$ to the original $V_{dsat}$ formula,

$$V_{dsatii} = \frac{E_{sat}L_{eff}V_{gst}}{M_1 E_{sat}L_{eff} + M_2 V_{gst}},\quad M_1 = A_{ii} + \frac{B_{ii}}{L_{eff}},\quad M_2 = 1 + \left(\frac{C_{ii}}{V_{ds} - D_{ii}}\right)^2 \tag{5-12}$$

$M_1$ and $M_2$ are used to correct the channel length and drain bias dependence respectively. $M_2$ is properly bounded to avoid problem when $V_{ds}$ is close to $D_{ii}$. The proposed model agrees extremely well with measurement data as shown in Fig. 5.10. Fig. 5.12 shows the $I_d$-$V_d$ fit for a 0.2μm device. Using the classical $I_{ii}$ model, the simulated kink looks more abrupt and the onset drain voltage is higher. Using the proposed $I_{ii}$ model, the average percentage error is reduced to below 1%. The DC output resistance fit is also improved as shown in Fig. 5.13. By modeling the impact ionization and diode current accurately, the self body bias can be modeled accurately as well. Hence the frequency dependence behavior can also be modeled accurately.

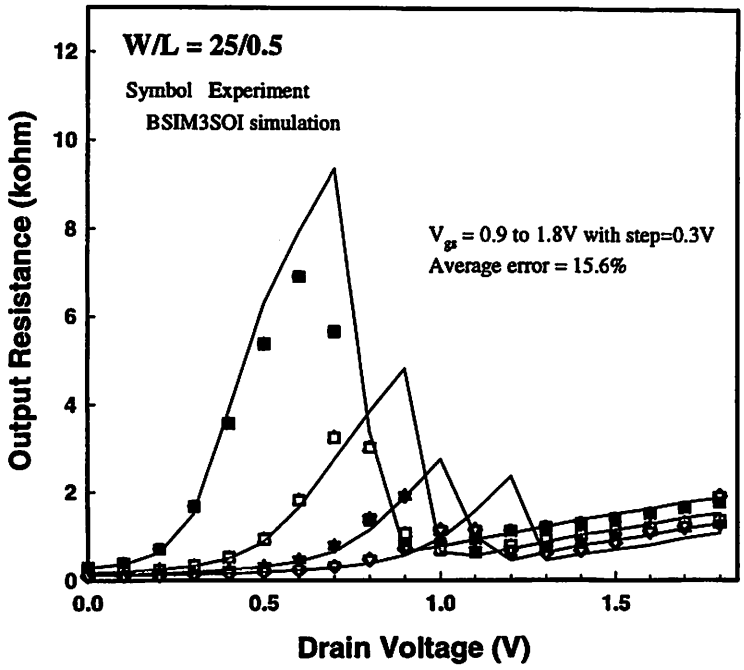



Fig. 5-13 DC output resistance characteristics of a L=0.2μm device.

## 5.8. Gate Induced Drain Leakage Current

Gate Induced Drain Leakage (GIDL) can be important in SOI, because it can affect the DC body potential at low $V_{gs}$ and high $V_{ds}$ in long channel devices. The formula for GIDL current is:

$$I_{dgidl} = \alpha_{gidl} \cdot E_s \cdot \exp\left(-\frac{\beta_{gidl}}{E_s}\right), \quad E_s = \frac{V_{ds} - V_{gs} - \chi}{3 \cdot T_{ox}} \tag{5-13}$$

Here $\chi$ is the fitting parameter with a default value 1.2 which is the correct value for uniformly doped substrates with no LDD or fully overlapped LDD. However, in general $\chi$ can be different from 1.2, depending on the doping profile at the drain edge [5-12]. For the sake of symmetry, GIDL current is accounted for both at the drain and source side.

## 5.9. Body Contact Current

For thick silicon film device, the body resistance is roughly constant. However, for thinner film, the body resistance becomes a function of body bias and backgate bias as well. When a device approaches full depletion, the body resistance becomes infinite and

the device effectively turns into a floating body device. In BSIMSOI, the body resistance is expressed as

$$R_{body} = \frac{R_{bp}}{\sqrt{V_{bs} - V_{bs0eff}}} + R_{bodyext}$$

$$\text{where } R_{bp} = R_{body0}\frac{W_{eff}}{L_{eff}},\ R_{bodyext} = R_{sh}N_{rb} \tag{5-14}$$

Here the first and second term represent the intrinsic and extrinsic body resistance respectively. $N_{rb}$ is the number of square from the body contact to the device edge and $R_{bsh}$ is the sheet resistance of the body contact diffusion.

## 5.10. Temperature Dependence

The temperature dependence of threshold voltage, mobility, saturation velocity and series resistances in BSIMSOI is identical to BSIM3v3. Temperature dependence of diode current from literature is used. Thermal resistance expression [5-6] is :

$$\text{where } R_{th} = \frac{R_{th0}}{W_{eff}}\sqrt{\frac{T_{box}}{T_{si}}} \tag{5-15}$$

## 5.11. Notes on Compatibility with BSIM3v3.1

The physical $V_{bseff}$ formulation allows complete compatibility with the bulk BSIM3v3.1 model. Basic equations for $\mu_{eff}$, $V_{th}$, $V_{gsteff}$, $V_{dseff}$, $I_{ds0}$, $V_A$ are the same or almost the same in both BSIMSOI and BSIM3v3.1. As a result the smoothness of BSIM3v3.1 is retained in BSIMSOI. Just like in BSIM3v3.1, all the parameters are physical and can be conveniently extracted. All parameters that are related to general MOSFET operation (not SOI-specific) are directly imported from BSIM3v3.1, and have the same name, which ensures parameter compatibility. The list of parameters can be found in Appendix B.

# Chapter 6: MOS C-V Model

## 6.1. General Information

BSIMSOI addresses physical short-channel capacitance modeling in partially and fully depleted devices. Backgate and SOI-specific parasitic capacitances are also included. The model incorporates features listed below. The new SOI-specific features are bold-faced and italicized.

- Separate effective channel length and width for IV and CV models.
- The CV model is not piece-wise (i.e. divided into inversion, depletion, and accumulation). Instead, a single equation is used for each nodal charge covering all regions of operation. This ensures continuity of all derivatives and enhances convergence properties. Just like in BSIM3v3.1, the inversion and body capacitances are continuous at the threshold voltage.
- Threshold voltage formulation is consistent with the IV model. Body effect and DIBL are automatically incorporated in the capacitance model.
- Intrinsic capacitance model has four options. The capmod =0 or 1 model option is based on simple piece-wise model from BSIM3v3.1 with the same capmod. The capmod = 2 option yields capacitance model based on BSIM3v3.1 short channel capacitance model. ***The channel depletion charge induced by drain voltage ($Q_{subs}$) is modified to account for dynamic depletion. But it returns to the original BSIM3v3.1 formulation when silicon film is very thick as compared to depletion width. A new option (capmod=3) is introduced for better capacitive coupling prediction. This option has the same charge formulations as capmod=2 except for $Q_{subs}$. $Q_{subs}$ is derived from direct integration of depletion charge from channel potential and it can yield better precision for high positive biased $V_{bs}$.***

- Front gate overlap capacitance is comprised of two parts: 1) a bias independent part which models the effective overlap capacitance between the gate and the heavily doped source/drain, and 2) a gate bias dependent part between the gate and the LDD region.
- Bias independent fringing capacitances are added between the gate and source as well as the gate and drain. ***A sidewall source/drain to substrate (under the buried oxide) fringing capacitance is added.***
- ***A source/drain-buried oxide-Si substrate parasitic MOS capacitor is added.***
- ***Junction capacitance model accounting for dynamic depletion has been developed. It can predicts correct capacitive coupling between the source/drain and body.***
- ***Front gate to back gate coupling charge for FD and PD devices has been developed. In a PD device, this charge is only in the fully depleted drain side region.***
- ***Body to back gate coupling charge.***

Device geometry dependencies related to $L_{active}$ and $W_{active}$ are the same as in BSIM3v3.1. The capacitance parameters can be found in Appendix B.

There has been significantly less work in the area of charge modeling in SOI and in MOSFETs in general. This is primarily due to the difficulty in measuring intrinsic capacitances in deep submicron MOSFETs. An alternative is the use of a 2D simulator. However, the results of a simulation are not always satisfactory.

A good intrinsic charge model is important in bulk MOSFETs because intrinsic capacitance comprises a sizable portion of the overall capacitance, and because a well behaved charge model is required for robust large circuit simulation convergence. In analog applications there are devices biased near the threshold voltage. Thus, a good charge model must be well behaved in transition regions as well. To ensure proper behavior, both the I-V and C-V model equations should be developed from an identical set of charge equations so that $C_{ij}/I_d$ is well behaved.

A good physical charge model of SOI MOSFETs is even more important than in bulk. This is because transient behavior of a floating body node (and steady-state drain current) depends on capacitive currents, as well as the external bias point. Also, because of an extra floating body node (or a body node connected to a voltage through a body resistance), convergence issues in SOI are more volatile than in bulk, so that charge smoothness and robustness are important. For example, a large negative (floating) $V_{bs}$ guess by SPICE can force a device into depletion, and a

smooth transition between depletion and inversion is a must. Since gate/source/drain to body capacitive coupling is important in SOI, the $C_{body,j}=dQ_b/dV_j$ (j=gate, body, source, drain, backgate) capacitances are important as well.

As BSIMFD is developed for FD, the challenge of modeling body charge is even higher. When the silicon film thickness is comparable to the depletion width, the source/drain to body junction charge or capacitance becomes a strong function of backgate bias. Such dependence is important to model because the junction capacitance can affect the capacitive coupling in short channel devices. Besides, channel depletion is different than bulk because of possible partial depletion near the drain end. To meet the challenge, dynamic depletion approach is adopted. Full depletion body voltage and partial depletion factor described in IV section are included in the charge derivation.

## 6.2. Charge Conservation

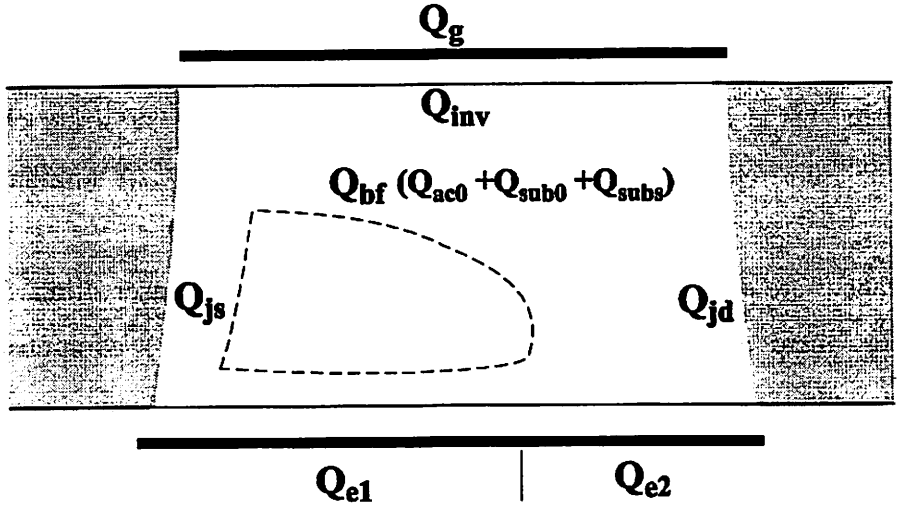



Figure 6-1 Intrinsic charge components in BSIMSOI CV model

To ensure charge conservation, terminal charges instead of terminal voltages are used as state variables. The terminal charges $Q_g$, $Q_d$, $Q_s$, $Q_b$, and $Q_e$ are the charges associated with the gate,

drain, source, body, and backgate respectively. These charges can be expressed in terms of inversion charge ($Q_{inv}$), accumulation charge ($Q_{acc}$), front body interface charge ($Q_{bf}$), source junction charge ($Q_{js}$), drain junction charge ($Q_{jd}$), back body interface charge ($Q_{bb}$), and front to back gate coupling charge ($Q_{e2}$). The intrinsic charges are distributed between the nodes as as shown in Fig. 6.1. The charge conservation equations are:

$$Q_{Bf} = Q_{ac0} + Q_{sub0} + Q_{subs} \tag{6.1}$$

$$Q_{inv} = Q_{inv,s} + Q_{inv,d} \tag{6.2}$$

$$Q_g = -\left(Q_{inv} + Q_{Bf} + Q_{e2}\right) \tag{6.3}$$

$$Q_e = Q_{e1} + Q_{e2} \tag{6.4}$$

$$Q_b = Q_{Bf} - Q_{e1} + Q_{js} + Q_{jd} \tag{6.5}$$

$$Q_s = Q_{inv,s} - Q_{js} \tag{6.6}$$

$$Q_d = Q_{inv,d} - Q_{jd} \tag{6.7}$$

$$Q_g + Q_e + Q_b + Q_s + Q_d = 0 \tag{6.8}$$

The substrate charge can be divided into two components: the substrate charge at $V_{ds}$=0 ($Q_{sub0}$), and the substrate charge induced by the drain bias ($Q_{subs}$) (similar to $\delta Q_{sub}$ in BSIM3v3.1).

All capacitances are derived from the charges to ensure charge conservation. Since there are 5 charge nodes, there are 25 (as compared to 16 in BSIM3v3.1) components. For each component: $C_{ij} = \frac{dQ_i}{dV_j}$, where $i$ and $j$ denote transistor nodes. In addition, $\sum_i C_{ij} = \sum_j C_{ij} = 0$.

## 6.3. Intrinsic Charges

### *6.3.1 Accumulation and Inversion Charges*

BSIMSOI uses the same expressions for accumulation charge ($Q_{acc0}$), body charge at $V_{ds}$=0V ($Q_{sub0}$) and inversion charges ($Q_{inv}$) as in BSIM3v3.2. The three partitioning schemes for inversion charge (50/50, 40/60 and 0/100) are applicable in BSIMSOI. The $Q_{subs}$ formulation is modified to account for dynamic depletion and provide better accuracy in capacitive coupling. The formulation of $Q_{inv}$ and $Q_{acc}$ are recalled below.

First, the bulk charge constant $A_{bulkCV}$ is defined as:

$$A_{bulkCV} = A_{bulk0}\left(1+\frac{CLC}{L_{active}}\right)^{CLE} \tag{6.9}$$

where
$$A_{bulk0} = 1+\left(\frac{K_1}{2\sqrt{\phi_s}}\left(\frac{A_0 L_{eff}}{L_{eff}+2\sqrt{T_{si}X_{dep}}}+\frac{B_0}{W_{eff}+B_1}\right)\right)\frac{1}{1+Keta\cdot V_{bseff}} \tag{6.10}$$

This is done in order to empirically fit $V_{dsatCV}$ to channel length. Experimentally,

$$V_{dsatIV} < V_{dsatCV} < V_{dsatIV}\big|_{L\to\infty} = \frac{V_{gsteffCV}}{A_{bulk}} \tag{6.11}$$

The effective CV $V_{gst}$ is defined as:

$$V_{gsteffCV} = nv_t \ln\left(1+\exp\left[\frac{V_{gs}-V_{th}}{nv_t}\right]\right) \tag{6.12}$$

Then we can calculate the CV saturation drain voltage:

$$V_{dsatCV} = V_{gsteffCV} / A_{bulkCV}\,. \tag{6.13}$$

Define effective CV $V_{ds}$ as:

$$V_{dsCV} = V_{dsatCV} - \frac{1}{2}(V_{dsatCV}-V_{ds}-\delta_4+\sqrt{(V_{dsatCV}-V_{ds}-\delta_4)^2+4\delta_4 V_{dsatCV}}) \tag{6.14}$$

Then the inversion charge can be expressed similarly to BSIM3v3.1 as:

$$Q_{inv} = -W_{active} L_{active} C_{ox} \left( \left( V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right) + \frac{A_{bulkCV}^2 V_{cveff}^2}{12 \left( V_{gsteffCV} - \frac{A_{bulkCV}^2}{2} V_{cveff} \right)} \right) \quad (6.15)$$

The channel partition can be set by *Xpart* parameter. The exact evaluation of source and drain charges for each partition option are presented in Appendix C.

A parameter $V_{FBeff}$ is used to smooth the transition between accumulation and depletion regions. The expression for $V_{FBeff}$ is:

$$V_{FBeff} = V_{fb} - 0.5 \left( (V_{fb} - V_{gb} - \delta) + \sqrt{(V_{fb} - V_{gb} - \delta)^2 + \delta^2} \right) \quad (6.16)$$

where $V_{gb} = V_{gs} - V_{bseff}$ , $V_{fb} = V_{th} - \phi_s - K_1 \sqrt{\phi_s - V_{bseff}}$ .

The physical meaning of the function is the following: it is equal to $V_{gb}$ for $V_{gb}<V_{FB}$, and equal to $V_{FB}$ for $V_{gb}>V_{FB}$. Using $V_{FBeff}$, the accumulation charge can be calculated as:

$$Q_{acc} = -W_{active} L_{active} C_{ox} (V_{FBeff} - V_{fb}) \quad (6.17)$$

The gate-induced depletion charge is equal to:

$$Q_{sub0} = -W_{active} L_{active} C_{ox} \frac{K_1^2}{2} \left( -1 + \sqrt{1 + \frac{4(V_{gs} - V_{FBeff} - V_{gsteffcv} - V_{bseff})}{K_1^2}} \right) \quad (6.18)$$

The use of $V_{bseff}$, rather than $V_{bs}$, ensures that the body charge is constant in full depletion.

### *6.3.2 Discussion of Body-to-Gate/Drain Coupling*

Due to a floating body node, body-to-gate/drain capacitive coupling factors are important in determining the transient value of $V_{bs}$ [6-2]. A series of plots of front gate charge $Q_{subs}$, the charge components $Q_{subs1}$ and $Q_{subs2}$, as well as body capacitances and body capacitive coupling ratios, unique to SOI, are presented below. The option capmod=3 was used, although analogous characteristics can be plotted for capmod=2. The corresponding .dc SPICE line is included under the plot. The Si film thickness of a device simulated is 1500Å, so that the device operates in PD

mode, and there is full depletion at the drain and partial depletion at the source.

As $V_{ds}$ increases, the total charge $Q_{subs}$ increases, until $V_{ds}$ reaches $V_{dsat}$. $Q_{subs2}$ increases starting from the point when the drain gets fully depleted. Until that point, $Q_{subs1}$ increases as well, but after that point it might decrease because $X_c$ decreases. However, the total charge $Q_{subs}$ exhibits monotonic behavior, as can be seen from both Fig. 6-2 and Fig. 6-3.

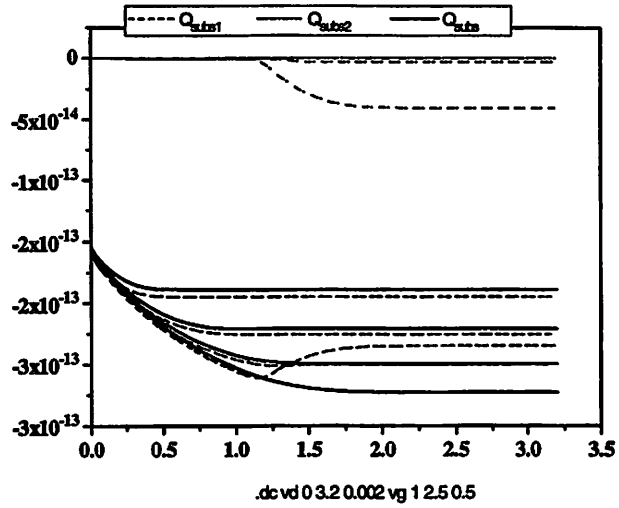



Fig. 6-2 Body charge components for the $V_{ds}$ sweep.

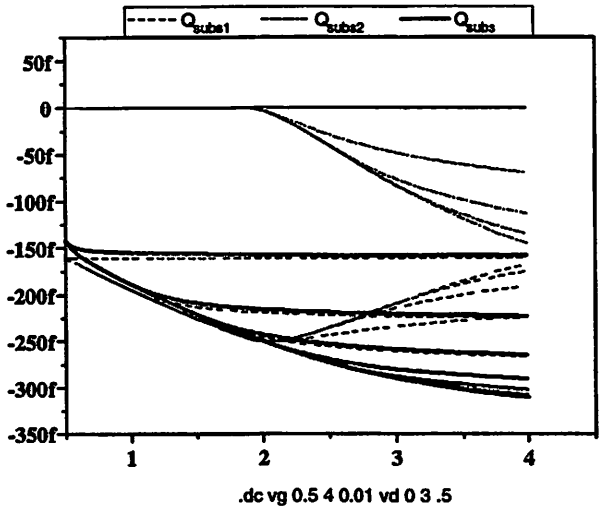



Fig. 6-3 Body charge components for the $V_{gs}$ sweep.

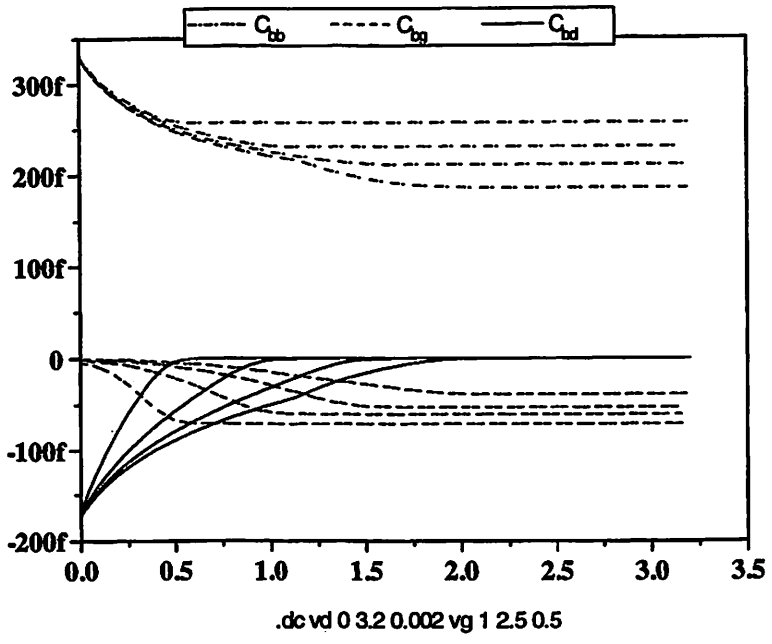



Fig. 6-4 Body capacitances for a $V_{ds}$ sweep.

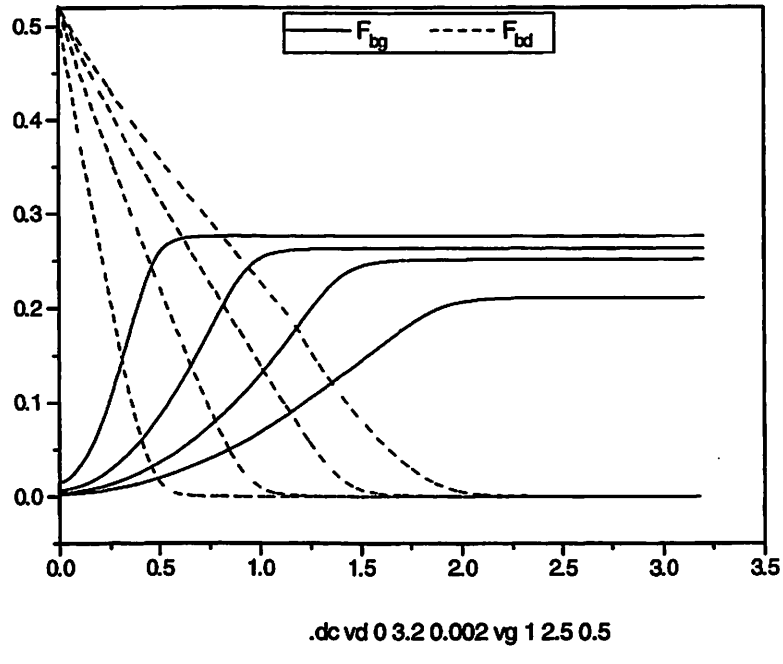



Fig. 6-5 Capacitive coupling factors as a function of a $V_{ds}$ sweep.

Body capacitance vs. $V_{ds}$ is plotted in Fig. 6-4. At $V_{ds} > V_{dsat}$, the body-to-drain capacitance ($C_{bd}$) reduces to zero because the depletion charge becomes constant at saturation. At the same time, body-to-gate capacitance ($C_{bg}$) and body-to-body capacitance ($C_{bb}$) become constant. The body capacitive coupling factors $F_{bd}(\equiv \frac{C_{bd}}{C_{bb}})$ and $F_{bg}(\equiv \frac{C_{bg}}{C_{bb}})$ are plotted in Fig. 6-5. From source-drain symmetry at $V_{ds}$=0, $F_{bd}$=0.5.

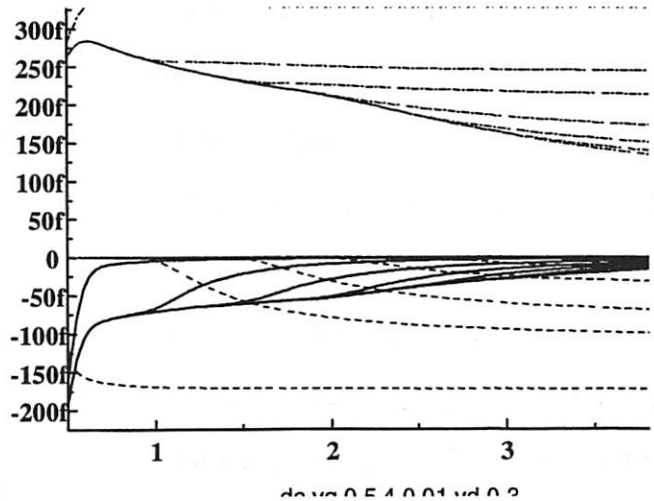



Fig. 6-6 Body capacitances as a function of a $V_{gs}$ sweep.

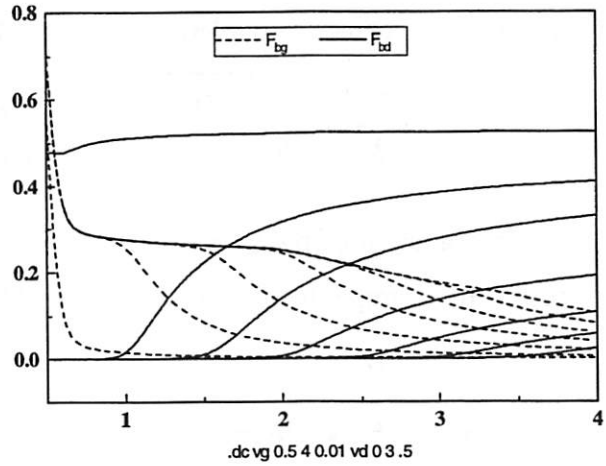



Fig. 6-7 Capacitive coupling factors as a function of a $V_{gs}$ sweep.

As $V_{gs}$ is increased, $C_{bd}$ and $C_{bb}$ follow the corresponding enveloping curves (Fig. 6-6). $V_{gs}$ increases, the $F_{bd}$ increases. It is because for higher $V_{gs}$, the device goes into triode regime and $Q_{subs}$ becomes very sensitive to $V_{ds}$. At the same time, the gate gets decoupled from the body by the inversion layer and hence $C_{bg}$ and $F_{bg}$ drop.

### *6.3.3 Backgate Charges*

Typical SOI technology usually has buried oxide thickness ranging from 100nm to 400nm. Since the buried oxide is so thick, the backgate charge along the channel is normally negligible as compared to channel inversion and depletion charge. However, proper backgate charge model is still important in achieving a proper backgate coupling factor and the continuity of the gate charge.

As shown in Fig. 6-1, the backgate charge is divided into two parts: $Q_{e1}$ is coupled to the body and $Q_{e2}$ is coupled to gate directly. Let first look at the case of $V_{ds} = 0$. The total body charge $Q_{sicv}$ at full depletion using $Q_{sub0}$ equation is

$$Q_{sicv} = C_{ox}WL\frac{K_1^{\,2}}{2}\left[1-\sqrt{1+\frac{4\left(\phi_s + K_1\sqrt{\phi_s - V_{bs0t}} - V_{bs0t}\right)}{K_1^{\,2}}}\right] \tag{6.19}$$

Meanwhile, the channel depletion charge coupled to the front gate $Q_{bf0}$ is equal to

$$Q_{bf0} = C_{ox}WL\frac{K_1^{\,2}}{2}\left(1-\sqrt{1+\frac{4(\phi_s + K_1\sqrt{\phi_s - V_{bs0mos}} - V_{bs0mos})}{K_1^{\,2}}}\right) \tag{6.20}$$

Then $Q_{sicv}$ - $Q_{bf0}$ will be the amount of body charge coupled to the backgate, i.e. $Q_{e1}$. In general when $V_{ds}$ is greater than zero, a simple formula is derived for $Q_{e1}$

$$Q_{e1} = Q_{bf0} - Q_{sicv} - WLC_{box}X_cV_{cs} \tag{6.21}$$

The last term accounts for excess backgate charge when $V_{bs}$ is larger than $V_{bs0eff}$ in the undepleted region. The second part of backgate charge $Q_{e2}$ is derived by assuming a linear channel potential profile from $V_{cs}$ to $V_{ds}$ (see Fig. 6-2) and the expression is

$$Q_{e2} = -WLC_{boxt}\frac{1-X_c}{2}(V_{dsCV} - V_{csCV}) \tag{6.22}$$

where $C_{cboxt} = \dfrac{C_{si}C_{box}}{C_{si}+C_{box}}$ is the coupling ratio from channel to substrate. Backgate charges are plotted in Fig. 6.8 for an NFD device. The corresponding .dc SPICE input line is included in the picture. For the $V_{ds}$ sweep, the backgate charge is nonzero when the drain side of the device becomes depleted for a high enough drain bias. Since $V_{gst}$ modulates $V_{dsat}$, the same thing happens in case of a $V_{gs}$ sweep.

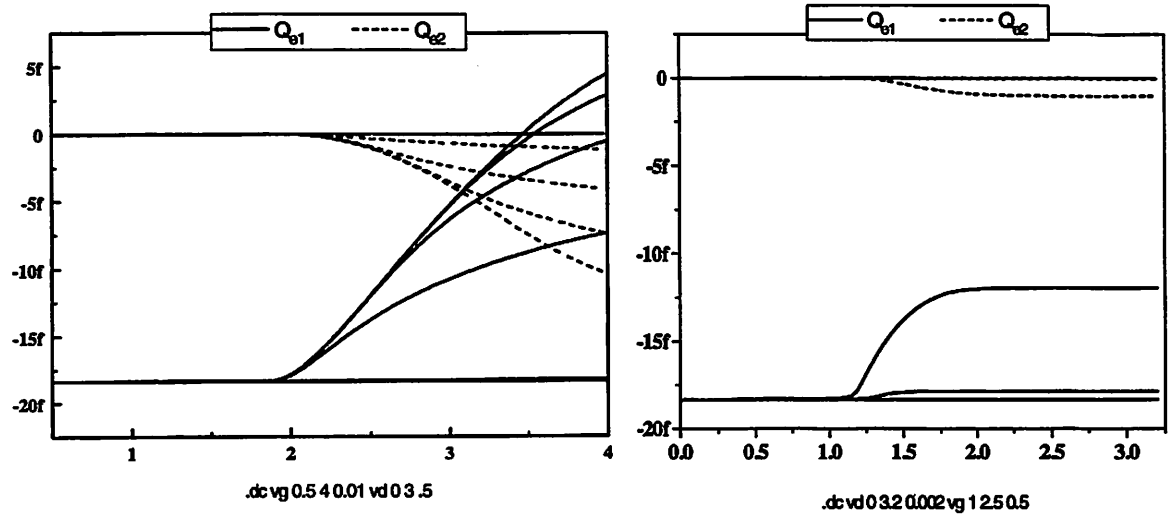



Fig. 6.8 Backgate charges for a $V_{gs}$ and a $V_{ds}$ sweep.

## 6.4. Junction Charges

Expressions for junction charges are similar to BSIM3v3.1. A diffusion capacitance term, which is important in forward $V_{bs}/V_{bd}$ operation regime, is added. The parameter $T_t$ represents the time of charge to transit across the junction. The appropriate depletion capacitance is multiplied by a factor $G_1$. This factor keeps track of full depletion and the variable neutral region thickness: in full depletion, since front gate-to-back gate coupling controls the channel potential, there is no coupling of the fully depleted node to the body (usually, this node is the drain). So the corresponding junction capacitance reduces to zero. The $G_1$ formulation is dropped for the purely NFD case of ddMod=0. The expression for source-body junction charge is:

For $V_{bs} < 0$,

$$Q_{jswg} = C_{jswg}\frac{T_{si}}{10^{-7}}G_{1s}\frac{P_{bswg}}{1-Mj_{swg}}\left[1-\left(1-\frac{V_{bs}}{P_{bswg}}\right)^{1-M_{jswg}}\right]+T_t\cdot I_{bs1}$$

else

$$Q_{jswg} = C_{jswg}\frac{T_{si}}{10^{-7}}G_{1s}V_{bs}\left(1+\frac{0.5M_{jswg}V_{bs}}{P_{bswg}}\right)+T_t\cdot I_{bs1} \tag{6.23}$$

Here

$$G_{1s} = \sqrt{\phi_s - V_{bs0}} - \sqrt{\phi_s - V_{bs}} \tag{6.24}$$

Similarly, the drain side junction charge expression is derived by multiplying the body-drain depletion capacitance by the same factor as in (6.23), but with $V_{bs}$ replaced by $V_{bd}$. The $G_{1,2}$ term is necessary to achieve stability in full depletion, making sure that the appropriate body capacitive couplings reduce to zero due to constant body charge.

## 6.5. Extrinsic Capacitances

Expressions for extrinsic (parasitic) capacitances that are common in bulk and SOI MOSFETs were taken directly from BSIM3v3.1. They are source/drain-to-gate overlap capacitance and source/drain-to-gate fringing capacitance. Additional SOI-specific parasitics added are substrate-to-source sidewall capacitance $C_{essw}$, and substrate-to-drain sidewall capacitance $C_{edsw}$, substrate-to-source bottom capacitance ($C_{esb}$) and substrate-to-drain bottom capacitance ($C_{edb}$) (Fig. 6-9).

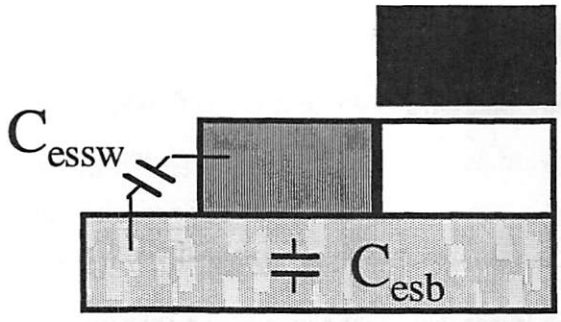



Fig. 6-9 SOI MOSFET extrinsic charge components. $C_{essw}$ is the substrate-to-source sidewall capacitance. $C_{esb}$ is the substrate-to-source bottom capacitance.

In SOI, there is a parasitic source/drain-buried oxide-Si substrate parasitic MOS structure with a bias dependent capacitance. If $V_{s,d}$=0, this MOS structure might be in accumulation. However, if $V_{s,d}=V_{dd}$, the MOS structure is in depletion with a much smaller capacitance, because the Si substrate is lightly doped. The bias dependence of this capacitance is similar to high frequency MOS depletion capacitance (Fig. 6.10). It might be substantial in devices with large source/drain diffusion areas. BSIMSOI models it by piece-wise expressions, with accurately chosen parameters to achieve smoothness of capacitance and continuity to the second derivative of charge. The substrate-to-source bottom capacitance $C_{esb}$ is:

$$C_{esb}=\begin{cases} C_{box} & if \quad V_{se}<V_{sdfb} \\ C_{box}-\dfrac{1}{A_{sd}}\left(C_{box}-C_{\min}\right)\left(\dfrac{V_{se}-V_{sdfb}}{V_{sdth}-V_{sdfb}}\right)^2 & elseif \quad V_{se}<V_{sdfb}+A_{sd}\left(V_{sdth}-V_{sdfb}\right) \\ C_{\min}+\dfrac{1}{1-A_{sd}}\left(C_{box}-C_{\min}\right)\left(\dfrac{V_{se}-V_{sdth}}{V_{sdth}-V_{sdfb}}\right)^2 & elseif \quad V_{se}<V_{sdth} \\ C_{\min} & else \end{cases} \tag{6.25}$$

Physical parameters $V_{sdfb}$ (flat-band voltage of the MOS structure) and $V_{sdth}$ (threshold voltage of the MOS structure) can be easily extracted from measurement. $C_{min}$ should also be extracted from measurement, and it can account for deep depletion as well. The expression for $C_{edb}$ is similar to $C_{esb}$. Fig. 6.10 shows the comparison of the model and measured $C_{esb}$.

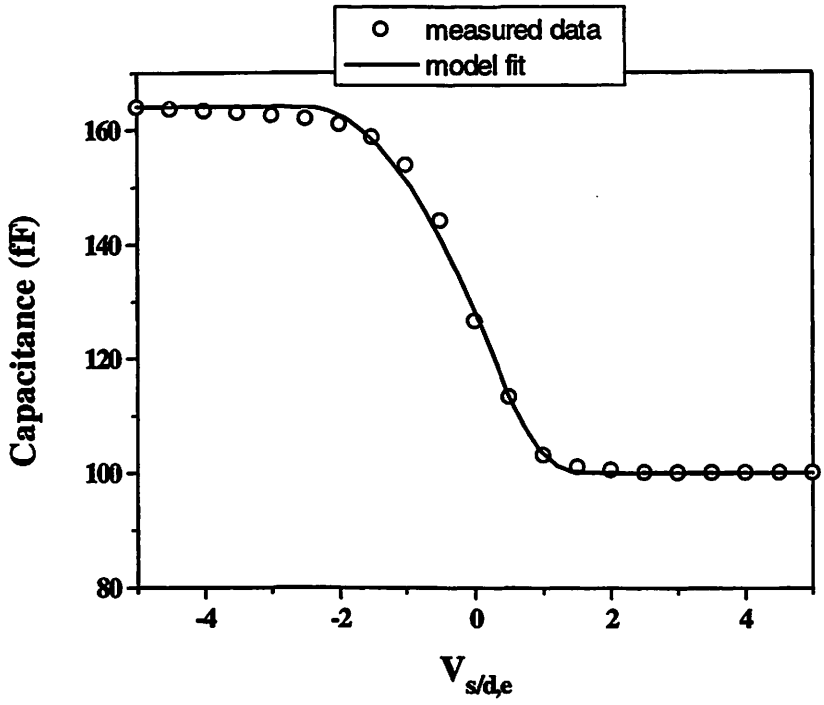



Fig. 6.10 Bottom source/drain to substrate capacitance for a PD SOI MOSFET.

# Chapter 7: Diode and BJT Model

## 7.1. General Information

Diodes and parasitic BJT currents in SOI are extremely important in both DC and transient simulation. The current components included are body-to-source/drain injection, recombination in body-to-source/drain junction depletion region, source/drain-to-body injection, recombination in neutral body and tunneling current . Conventional p-n junction diode model is only applicable if there is presence of a neutral region. In full depletion, the minimum body potential is bound to $V_{bs0eff}$. As $V_{bs}$ approaches $V_{bs0eff}$ from above, diode can sink less and less current with a very small $V_{bs}$ decrement. The physical explanation is that the amount of majority carriers available for diffusion or recombination becomes very small. When $V_{bs}=V_{bs0eff}$, diode current reduces to zero. The general equations used are

$$V_{bs0\_dio} = 0.5\left[V_{bs0eff} - \delta_1 + \sqrt{\left[V_{bs0eff} - \delta_1\right]^2 + 4\delta_1}\right] \tag{7.1}$$

$$I_{bs1} = W_{eff} T_{si} j_{sdif} \left( e^{\frac{V_{bs}}{n \cdot V_t}} - e^{\frac{V_{bs0\_dio}}{n \cdot V_t}} \right) \tag{7.2}$$

Equation (7.1) is a smoothing function that makes $V_{bs0\_dio}$ equal to $V_{bs0eff}$ if $V_{bs0eff}$ is positive. Otherwise, $V_{bs0\_dio}$ is equal to zero and the diode equation returns to the conventional diode model. The diode model shows good agreement with MEDICI simulation as shown in Fig. 7.1. The simulated structure is a gated-diode with the gate voltage biased at turn-on.

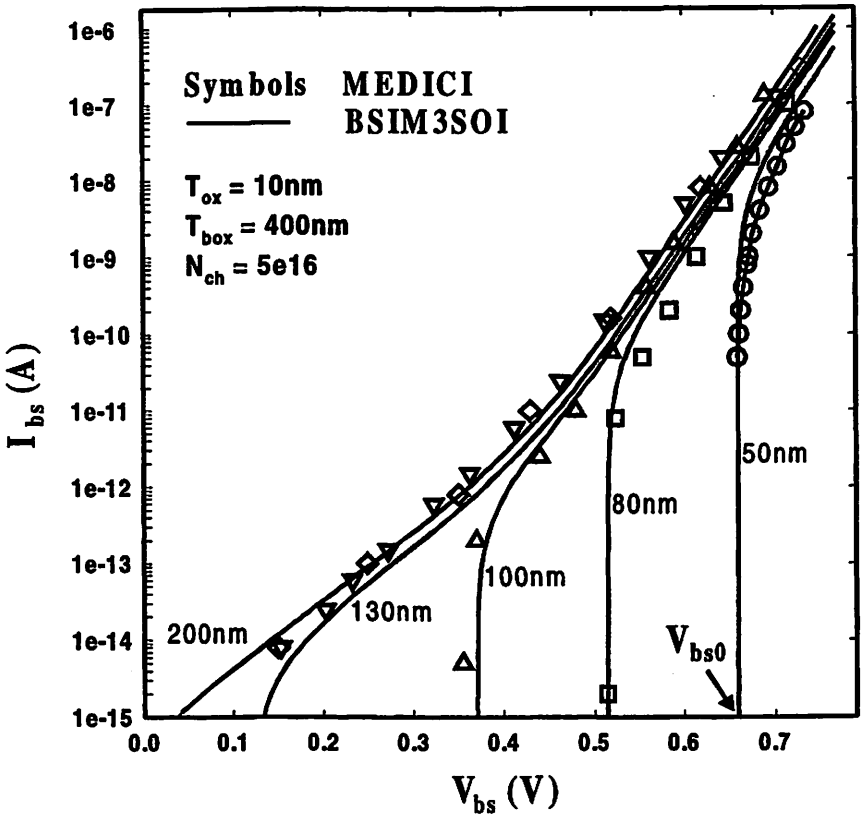



Figure 7-1 Body-source diode characteristic for different silicon film thickness from MEDICI simulation and model. The general equation used is $I_{bs} = W \cdot T_{si} \cdot J_s\left(\exp(V_{bs}/nV_T) - \exp(V_{bs0}/nV_T)\right)$.

## 7.2. Notes on "Kink" in Fully Depleted Devices

BSIMSOI relies on this diode model to tie $V_{bs}$ to $V_{bs0eff}$ in FD condition. When $V_{bs}$ is close to $V_{bs0eff}$, the B-S diode can sink a large range of impact ionization or leakage with a small change of body potential. Hence $V_{bs}$ will stay close to $V_{bs0eff}$ until the level of body current is high. For this reason, the "kink" in $I_d$-$V_d$ curve has strong dependence on $V_{bs0eff}$ as illustrated in Fig. 7.2. If a negative backgate bias is applied, $V_{bs0eff}$ is reduced. Hence the onset of kink occurs at smaller $V_{ds}$ and the magnitude of kink becomes larger.

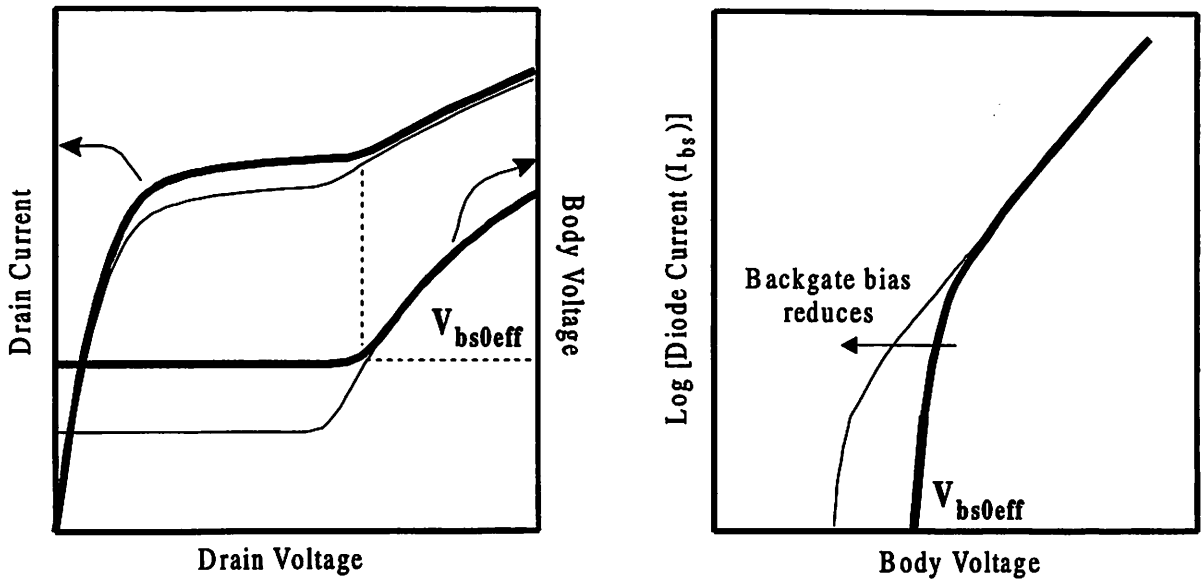



Figure 7-2 Relationship between the onset of kink in FD device and the diode current characteristics. The thinner lines have a reduced backgate bias compared to the thicker lines.

## 7.3. Diode I-V Formulation

The formula for backward injection current in Body-Source diode is:

$$I_{bs1} = W_{eff} T_{si} j_{sdif} \left( e^{\frac{V_{bs}}{n_{dio} \cdot V_t}} - e^{\frac{V_{bs0\_dio}}{n_{dio} \cdot V_t}} \right) \tag{7.3}$$

Here $n_{dio}$ is the diode non-ideality factor, $j_{sbjt}$ and $j_{sdif}$ are the saturation currents. The carrier recombination in the space-charge region is modeled in a similar fashion, with $n_{dio}$ replaced by $2n_{dio}$:

$$I_{bs2} = W_{eff} T_{si} j_{srec} \left( e^{\frac{V_{bs}}{2n_{dio} \cdot V_t}} - e^{\frac{V_{bs0\_dio}}{2n_{dio} \cdot V_t}} \right) \tag{7.4}$$

The expression for the recombination current in the neutral body is assigned to $I_{bs}$ as well, and is equal to:

$$I_{bs3} = \left(1 - \alpha_{bjt}\right) I_{bjt} \tag{7.5}$$

where $I_{bjt}$ is the forward injection current in B-S diode and $\alpha_{bjt}$ is the transport factor in the base (neutral body). The expression for $I_{bjt}$ is described later.

Finally, reverse bias exponential current $I_{bs4}$ is added to the body-to-source diode current. This current can be significant in junctions with high doping concentration (reverse bias tunneling). It can also model reverse bias avalanche junction breakdown for high negative $V_{bs}$. The expression is:

$$I_{bs4} = W_{eff} T_{si} j_{stun} \left( 1 - e^{-\frac{V_{bs}}{n_t \cdot V_t}} \right) \tag{7.6}$$

Since this current component supplies holes into the body, this current does not have a $V_{bs0\_dio}$ term. Finally, drain diode leakage has the same components as source, except for the body recombination component (see Appendix C).

The parasitic bipolar transistor current is very important in transient body discharge, especially in pass-gate floating body SOI designs. The BJT emitter current is modeled as

$$I_{bjt} = W_{eff} T_{si} j_{bjt} \left( e^{\frac{V_{bs}}{n \cdot V_t}} - e^{\frac{V_{bs0\_dio}}{n \cdot V_t}} \right) \left( 1 - e^{-\frac{V_{ds}}{2n \cdot V_t}} \right) \tag{7.7}$$

This formulation is different from the conventional BJT equations, in which the BJT current from emitter and collector are included. Inside the BSIMSOI model, $V_{ds}$ is always positive and therefore BJT current is always flowing from source to drain and there is no need to implement the backward BJT current. This formulation gives less truncation error than the complementary implementation. The collector current becomes

$$I_c = I_{bjt} - I_{bs3} = \alpha_{bjt} I_{bjt}, \text{ where } \alpha_{bjt} = 1 - 0.5 \left( \frac{W_b}{Edl} \right)^2 \tag{7.8}$$

Here $W_b$ is the basewidth including $V_{ds}$-dependent base shortening (see Appendix C).

The total diode leakage current is equal to $I_{bs1}+I_{bs2}+I_{bs3}+I_{bs4}+I_{bd1}+I_{bd2}+I_{bd4}$. The total drain current is $I_{drain,total} = I_{ds,MOSFET} + I_c$.

# Chapter 8: Parameter Extraction

## 8.1. Extraction Strategy

The complicated physics in SOI MOSFETs makes parameter extraction quite involved. It is always preferable to have more measurements so that the parameters extracted can have more valid physical meaning. Similar to conventional bulk devices, two basic extraction strategies can be used: single device extraction, and group device extraction. The group device extraction is more popular because of several reasons. In analog circuit, channel length and width scalability is very important. In digital circuit, statistical modeling is often used to predict the circuit performance due to process variation. Hence channel length scalability is also important. Besides, model parameters extracted from group device extraction have better physical meaning than that from single device extraction. In this work, we shall emphasize on group device extraction.

Parameter extraction using body contact devices is highly recommended because parameters related to body effect, impact ionization and leakage currents can be directly extracted. This yields less ambiguity in extracting technology parameters for I-V fitting purposes.

## 8.2. I-V Measurement

Measurement set B is used to extract PD/FD transition and backgate effect parameters. For each body-contacted device :

(B1) $I_{ds}$ vs. $V_{gs}$ @ small $V_{ds}$ with different $V_{bs}$ and different $V_{es}$.

$V_{th}$ at different $V_{es}$ can be plotted against $V_{bs}$ to extract $N_{ch}$, $K_1$, $V_{bsa}$ and $K_{b1}$. Subthreshold $V_{bs0eff}$ parameters ($K_{b3}$) can be extracted from the subthreshold characteristic with different $V_{es}$'s. Length dependence parameters of $V_{bs0}$ can be extracted by plotting $V_{th}$ versus $L_{eff}$.

Measurement set D is used to extract MOS temperature dependent parameter. For a long channel body-contacted device:

(D1) $I_{ds}$ vs. $V_{gs}$ @ small $V_{ds}$, $V_{bs}$=0V, $V_{es}$=0V, repeat with several temperatures.

(D2) $I_{ds}$ vs. $V_{ds}$ @ different $V_{gs}$, $V_{bs}$=0V, $V_{es}$=0V, repeat with several temperatures.

Notice that the self-heating parameters have to be extracted from set A.

Measurement set E is used to extract diode parameters. For a long channel body-contacted device or gated diode :

(E1) $I_{diode}$ vs. $V_{bs}$ @ $V_{gs}$=-1V, $V_{es}$=0V, repeat with several temperature

Measurement set F is used to extract BJT parameters. For each body-contacted device:

(F1) $I_{ds}$ vs. $I_b$ @ $V_{gs}$=-1V, $V_{es}$=0V, $V_{ds}$=1V.

Measurement set G is used to verify the floating body device data. For each floating-body device :

(G1) $I_{ds}$ vs. $V_{gs}$ @ small $V_{ds}$ with different $V_{es}$.

(G2) $I_{ds}$ vs. $V_{gs}$ @ $V_{ds}$=$V_{dd}$ with different $V_{es}$.

(G3) $I_{ds}$ vs. $V_{ds}$ @ different $V_{gs}$ and $V_{es}$.

For FD technology, measurement with body contact is still recommended because diode, body effect and impact ionization parameters can be directly extracted. It may be difficult to measure the body current in FD device. But the impact ionization parameters can still be extracted from measurement set G because the diode parameters have been extracted. The impact ionization can also be measured by applying a negative backgate bias together with a positive body bias. However, the low efficiency of body current collection in short channel devices may affect the accuracy of extraction.

## 8.3. I-V Extraction Procedure

Before any model parameters can be extracted, some process parameters have to be provided. They are listed below in Table 8.1:

| *Input parameter names* | *Physical meaning* |
|---|---|
| $T_{ox}$ | Front gate oxide thickness |
| $T_{box}$ | Back gate oxide thickness |
| $N_{ch}$ | Channel doping concentration |
| $T_{nom}$ | Temperature at which data is taken |
| $T_{si}$ | Si film thickness |
| $L_{drawn}$ | Mask level channel length |
| $W_{drawn}$ | Mask level channel width |
| $R_{bsh}$ | Body contact external diffusion resistance |

Table 8-1 Prerequisite input parameters prior to extraction process

The procedure for parameter extraction is outlined below. These procedures are based on physical understanding of the model and based on local optimization. The availability of a body contact is assumed. The SOI-specific parameters are typed in bold letters. (Note: Fitting Target Data refers to measurement data for model extraction.)

**Step 1**

| Extracted Parameters & Fitted Target Data | Device & Experimental Data |
|---|---|
| **$Kb_1$**<br><br>Fitting Target Exp. Data: $V_{bs0}(V_{bs})$ | Large size device, *B1*<br>$I_{ds}$ vs. $V_{gs}$ @$V_{ds}$=50mV at different $V_{bs}$ and $V_{es}$<br>Extracted $V_{th}(V_{bs})$ |

## Step 2

| Extracted Parameters & Fitted Target Data | Device & Experimental Data |
|---|---|
| $R_{dsw}P_{rwb}$, $W_r$<br><br>Fitting Target Exp. Data: $R_{ds}(R_{dsw}W, V_{bs})$ | $R_{ds}(R_{dsw}W,V_{bs})$ |

## Step 4

| Extracted Parameters & Fitted Target Data | Device & Experimental Data |
|---|---|
| $\mu te$, $K_{t1}$, $K_{t2}$, $U_{a1}$, $U_{b1}$, $U_{c1}$, $A_t$<br><br>Fitting Target Exp. $I_{ds}(V_{gs}, V_{ds})/W$ | Large Size Device, *D1, D2*<br><br>$I_{ds}$ vs. $V_{gs}$ and $I_{ds}$ vs. $V_{ds}$ |

## Step 5

| Extracted Parameters & Fitted Target Data | Device & Experimental Data |
|---|---|
| $j_{sdif}$, $j_{srec}$, $j_{stun}$, $n_{dio}$, $n_t$, $R_{body0}$, $N_{rb}$<br><br>Fitting Target Exp. $I_{sub}(V_{gs}, V_{bs})/W$ | Large Size Device, *E1*<br><br>$V_{ds}=V_{gs}=0$, $I_{sub}$ vs. $V_{bs}$ |

## Step 6

| Extracted Parameters & Fitted Target Data | Device & Experimental Data |
|---|---|
| $X_{sdif}$, $X_{srec}$, $X_{stun}$<br><br>Fitting Target Exp. $I_{sub}(V_{gs}, V_{bs})/W$ | Large Size Device, *E1*<br><br>$V_{ds}=V_{gs}=0$, $I_{sub}$ vs. $V_{bs}$ at different temperatures |

## Step 7

| Extracted Parameters & Fitted Target Data | Device & Experimental Data |
|---|---|
| **$K_{bjt1}$, Edl, $X_{bjt}$**<br><br>Fitting Target Exp. beta | One set of devices (large and fixed W & different L), *F1*<br><br>Gummel plot with a body contact for different temperatures |

If the body contact is not available, body effect parameters, impact ionization and p-n junction diode parameters can be fitted only from $I_d$ curves at different $V_{es}$. The following strategy is recommended for BSIMSOI:

- Body effect parameters $K_1$, $K_2$, $K_{b1}$ can be extracted from $I_d$-$V_g$ plots at different $V_{es}$.
- Channel length modulation parameters can be extracted from $R_{out}$ in the pre-kink region
- DIBL, impact ionization, and diode leakage parameters can be extracted from optimizing $I_d$-$V_d$ curves in the kink region.
- Parasitic BJT parameters can be extracted from optimizing $I_d$-$V_d$ curves in the breakdown region.

# Part III

# Appendix A: Command Line Information

```
Mname <D node> <G node> <S node> <E node> [P node] <model>
      [L=<val>] [W=<val>]
      [AD=<val>] [AS=<val>] [PD=<val>] [PS=<val>]
      [NRS=<val>] [NRD=<val>] [NRB=<val>]
      [OFF] [BJTOFF=<val>]
      [IC=<val>,<val>,<val>,<val>,<val>]
      [RTH0=<val>] [CTH0=<val>]
      [DEBUG=<val>]
```

## A.1. Description

| | |
|---|---|
| <D node> | Drain node |
| <G node> | Gate node |
| <S node> | Source node |
| <E node> | Substrate node |
| [P node] | Optional external body contact<br>■ if not specified, it is a 4-terminal device<br>■ if specified, it is a 5-terminal device. The P node and B node will be connected by a resistance. |
| <model> | Level 9 BSIMSOI model name |
| [L] | Channel length |
| [W] | Channel width |
| [AD] | Drain diffusion area |

[AS] Source diffusion area

[PD] Drain diffusion perimeter length

[PS] Source diffusion perimeter length

[NRS] Number of squares in source series resistance

[NRD] Number of squares in drain series resistance

[NRB] Number of squares in body series resistance

[OFF] Device simulation off

[BJTOFF] Turn off BJT current if equal to 1

[IC] Initial guess in the order of (Vds, Vgs, Vbs, Ves, Vps). (Vps will be ignored in the case of 4-terminal device)

[RTH0] Thermal resistance per unit width

- if not specified, RTH0 is extracted from model card.
- if specified, it will override the one in model card.

[CTH0] Thermal capacitance per unit width

- if not specified, CTH0 is extracted from model card.
- if specified, it will over-ride the one in model card.

[DEBUG] Please see the debugging notes

## A.2. Notes on Debugging

The instance parameter <DEBUG> allows users to turn on debugging information selectively. Internal parameters (e.g. par) for an instance (e.g. m1) can be plotted by this command.

```
plot m1#par
```

By default, <DEBUG> is set to zero and three internal parameters will be available for plotting.

#body $V_b$ value iterated by SPICE

#temp Device temperature with self-heating mode turned on

If <DEBUG> is set to one, more internal parameters are available for plotting. This serves debugging purposes when there is convergence problem. This can also help the user to understand the model more. Here is the list of internal parameters:

| | |
|---|---|
| #Vbs | Real $V_{bs}$ value used by the IV calculation |
| #Ids | MOS current |
| #Ic | BJT current |
| #Ibs | Body to source diode current |
| #Ibd | Body to drain diode current |
| #Iii | Impact ionization current |
| #Igidl | GIDL current at drain side |
| #Itun | Tunneling current at drain side |
| #Ibp | External body contact to internal body current |
| #Abeff | Effective bulk charge factor |
| #Vbs0eff | Minimum body potential for given external bias. |
| #Vbseff | Effective body voltage |

These parameters are only valid if charge computation is required

| | |
|---|---|
| #Xc | Partial depletion factor |
| #Cbb | Body charge derivative wrt Vbs |
| #Cbd | Body charge derivative wrt Vds |
| #Cbe | Body charge derivative wrt Ves |
| #Cbg | Body charge derivative wrt Vgs |
| #Qbody | Total body charge |
| #Qbf | Channel depletion charge |
| #Qjd | Parasitic drain junction charge |
| #Qjs | Parasitic source junction charge |

# Appendix B: Parameter List

All parameters additional to BSIM3v3 will be shown with bold cases.

## B.1. BSIMSOI Model Control Parameters

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Notes (below the table) |
|---|---|---|---|---|---|
| **None** | **level** | **Level 9 for BSIMSOI** | - | **9** | - |
| | | | | | |
| ***shmod*** | **shMod** | **Flag for self-heating**<br>**0 - no self-heating,**<br>**1 - self-heating** | - | **0** | |
| *Mobmod* | mobmod | Mobility model selector | - | 1 | - |
| *Capmod* | capmod | Flag for the short channel capacitance model | - | 2 | **nI-1** |
| *Noimod* | noimod | Flag for Noise model | - | 1 | - |

## B.2. Process Parameters

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Notes (below the table) |
|---|---|---|---|---|---|
| $t_{si}$ | **Tsi** | **Silicon film thickness** | **m** | **$10^{-7}$** | - |
| $t_{box}$ | **Tbox** | **Buried oxide thickness** | **m** | **$3x10^{-7}$** | - |
| $t_{ox}$ | Tox | Gate oxide thickness | m | $1x10^{-8}$ | - |
| $n_{ch}$ | Nch | Channel doping concentration | $1/cm^3$ | $1.7x10^{17}$ | - |
| $n_{sub}$ | Nsub | Substrate doping concentration | $1/cm^3$ | $6x10^{16}$ | **nI-2** |
| *Ngate* | ngate | poly gate doping concentration | $1/cm^3$ | 0 | - |

## B.3. DC Parameters

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Notes (below the table) |
|---|---|---|---|---|---|
| $V_{th0}$ | vth0 | Threshold voltage @$V_{bs}$=0 for long and wide device | - | 0.7 | **nI-3** |
| $K_1$ | k1 | First order body effect coefficient | $V^{1/2}$ | 0.6 | - |
| $K_2$ | k2 | Second order body effect coefficient | - | 0 | - |
| $K_3$ | k3 | Narrow width coefficient | - | 0 | - |
| $K_{3b}$ | k3b | Body effect coefficient of k3 | 1/V | 0 | - |
| $V_{bsa}$ | **Vbsa** | **Transition body voltage offset** | **V** | **0** | - |
| ***Delp*** | **delp** | **Constant for limiting $V_{bseff}$ to $\phi_s$** | **V** | **0.02** | - |
| $K_{b1}$ | **Kb1** | **Coefficient of $V_{bs0}$ dependency on $V_{es}$** | - | **1** | - |
| $K_{b3}$ | **Kb3** | **Coefficient of $V_{bs0}$ dependency on $V_{gs}$ at subthreshold region** | - | **1** | - |
| $D_{vbd0}$ | **Dvbd0** | **First coefficient of $V_{bs0}$ dependency on $L_{eff}$** | **V** | **0** | - |
| $D_{vbd1}$ | **Dvbd1** | **Second coefficient of $V_{bs0}$ dependency on $L_{eff}$** | **V** | **0** | - |

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Notes (below the table) |
|---|---|---|---|---|---|
| $W_0$ | w0 | Narrow width parameter | m | 0 | - |
| $N_{LX}$ | nlx | Lateral non-uniform doping parameter | m | 1.74e-7 | - |
| $D_{vt0}$ | dvt0 | first coefficient of short-channel effect on Vth | - | 2.2 | - |
| $D_{vt1}$ | dvt1 | Second coefficient of short-channel effect on Vth | - | 0.53 | - |
| $D_{vt2}$ | dvt2 | Body-bias coefficient of short-channel effect on Vth | 1/V | -0.032 | - |
| $D_{vt0w}$ | dvt0w | first coefficient of narrow width effect on Vth for small channel length | - | 0 | - |
| $D_{vt1w}$ | dvt1w | Second coefficient of narrow width effect on Vth for small channel length | - | 5.3e6 | - |
| $D_{vt2w}$ | dvt2w | Body-bias coefficient of narrow width effect on Vth for small channel length | 1/V | -0.032 | - |
| $\mu_0$ | u0 | Mobility at Temp = Tnom<br>NMOSFET<br>PMOSFET | $cm^2/(V\text{-}sec)$ | <br>670<br>250 | - |
| $U_a$ | ua | First-order mobility degradation coefficient | m/V | 2.25e-9 | - |
| $U_b$ | ub | Second-order mobility degradation coefficient | $(m/V)^2$ | 5.9e-19 | - |
| $U_c$ | uc | Body-effect of mobility degradation coefficient | 1/V | -.0465 | - |
| $v_{sat}$ | vsat | Saturation velocity at Temp=Tnom | m/sec | 8e4 | - |
| $A0$ | a0 | Bulk charge effect coefficient for channel length | - | 1.0 | - |
| $A_{gs}$ | ags | Gate bias coefficient of $A_{bulk}$ | 1/V | 0.0 | - |
| $B0$ | b0 | Bulk charge effect coefficient for channel width | m | 0.0 | - |
| $B1$ | b1 | Bulk charge effect width offset | m | 0.0 | - |
| $Keta$ | keta | Body-bias coefficient of bulk charge effect | m | -0.6 | - |
| $A_{bp}$ | **Abp** | **Coefficient of $A_{beff}$ dependency on $V_{gst}$** | - | **1.0** | - |

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Notes (below the table) |
|---|---|---|---|---|---|
| $m_{xc}$ | **mxc** | **Fitting parameter for $A_{beff}$ calculation** | - | **-0.9** | - |
| $a_{dice0}$ | **adice0** | **DICE bulk charge factor** | - | **1** | - |
| $A_1$ | A1 | First non-saturation effect parameter | 1/V | 0.0 | - |
| $A_2$ | A2 | Second non-saturation effect parameter | 0 | 1.0 | - |
| $R_{dsw}$ | rdsw | Parasitic resistance per unit width | $\Omega$-$\mu m^{Wr}$ | 100 | - |
| *Prwb* | prwb | Body effect coefficient of Rdsw | 1/V | 0 | - |
| *Prwg* | prwg | Gate bias effect coefficient of Rdsw | $1/V^{1/2}$ | 0 | - |
| *Wr* | wr | Width offset from Weff for Rds calculation | - | 1 | - |
| *Wint* | wint | Width offset fitting parameter from I-V without bias | m | 0.0 | - |
| *Lint* | lint | Length offset fitting parameter from I-V without bias | m | 0.0 | - |
| *dWg* | dwg | Coefficient of $W_{eff}$'s gate dependence | m/V | 0.0 | |
| *dWb* | dwb | Coefficient of $W_{eff}$'s substrate body bias dependence | $m/V^{1/2}$ | 0.0 | |
| $V_{off}$ | voff | Offset voltage in the subthreshold region for large W and L | V | -0.08 | - |
| *Nfactor* | nfactor | Subthreshold swing factor | - | 1 | - |
| *Eta0* | eta0 | DIBL coefficient in subthreshold region | - | 0.08 | - |
| *Etab* | etab | Body-bias coefficient for the subthreshold DIBL effect | 1/V | -0.07 | - |
| $D_{sub}$ | dsub | DIBL coefficient exponent | - | 0.56 | - |
| $C_{it}$ | cit | Interface trap capacitance | $F/m^2$ | 0.0 | - |

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Notes (below the table) |
|---|---|---|---|---|---|
| $C_{dsc}$ | cdsc | Drain/Source to channel coupling capacitance | $F/m^2$ | 2.4e-4 | - |
| $C_{dscb}$ | cdscb | Body-bias sensitivty of $C_{dsc}$ | $F/m^2$ | 0 | - |
| $C_{dscd}$ | cdscd | Drain-bias sensitivty of $C_{dsc}$ | $F/m^2$ | 0 | - |
| $P_{clm}$ | pclm | Channel length modulation parameter | - | 1.3 | - |
| $P_{dibl1}$ | pdibl1 | First output resistance DIBL effect correction parameter | - | .39 | - |
| $P_{dibl2}$ | pdibl2 | Second output resistance DIBL effect correction parameter | - | 0.086 | - |
| $D_{rout}$ | drout | L dependence coefficient of the DIBL correction parameter in Rout | - | 0.56 | - |
| *Pvag* | pvag | Gate dependence of Early voltage | - | 0.0 | - |
| $\delta$ | delta | Effective $V_{ds}$ parameter | - | 0.01 | - |
| $a_{ii}$ | **aii** | **1st $L_{eff}$ dependence $V_{dsatii}$ parameter** | **1/V** | **0.0** | **-** |
| $b_{ii}$ | **bii** | **2nd $L_{eff}$ dependence $V_{dsatii}$ parameter** | **m/V** | **0.0** | **-** |
| $c_{ii}$ | **cii** | **1st $V_{ds}$ dependence $V_{dsatii}$ parameter** | **-** | **0.0** | **-** |
| $d_{ii}$ | **dii** | **2nd dependence $V_{dsatii}$ parameter** | **V** | **-1.0** | **-** |
| $\alpha_0$ | alpha0 | The first parameter of impact ionization current | m/V | 0.0 | - |
| $\alpha_1$ | alpha1 | The second parameter of impact ionization current | 1/V | 1.0 | - |
| $\beta_0$ | beta0 | The third parameter of impact ionization current | V | 30 | - |
| $\alpha_{gidl}$ | **Agidl** | **GIDL constant** | **$\Omega^{-1}$** | **0.0** | **-** |
| $\beta_{gidl}$ | **Bgidl** | **GIDL exponential coefficient** | **V/m** | **0.0** | **-** |
| $\chi$ | **Ngidl** | **GIDL $V_{ds}$ enhancement coefficient** | **V** | **1.2** | **-** |

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Notes (below the table) |
|---|---|---|---|---|---|
| $n_{tun}$ | Ntun | **Reverse tunneling non-ideality factor** | - | 10.0 | - |
| $n_{diode}$ | Ndiode | **Diode non-ideality factor** | - | 1.0 | - |
| $i_{sbjt}$ | Isbjt | **BJT injection saturation current** | $A/m^2$ | 1e-6 | - |
| $i_{sdif}$ | Isdif | **Body to source/drain injection saturation current** | $A/m^2$ | 0.0 | - |
| $i_{srec}$ | Isrec | **Recombination in depletion saturation current** | $A/m^2$ | 1e-5 | - |
| $i_{stun}$ | Istun | **Reverse tunneling saturation current** | $A/m^2$ | 0.0 | - |
| *Edl* | Edl | **Electron diffusion length** | m | 2e-6 | - |
| $k_{bjt1}$ | Kbjt1 | **Parasitic bipolar early effect coefficient** | m/V | 0 | - |
| *rbody* | Rbody | **Intrinsic body contact sheet resistance** | $ohm/m^2$ | 0.0 | - |
| *rbsh* | Rbsh | **Extrinsic body contact sheet resistance** | $ohm/m^2$ | 0.0 | - |
| *Rsh* | rsh | Source drain sheet resistance in ohm per square | Ω/square | 0.0 | - |

## B.4. AC and Capacitance Parameters

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Notes (below the table) |
|---|---|---|---|---|---|
| *Xpart* | xpart | Charge partitioning rate flag | - | 0 | |
| *CGS0* | cgso | Non LDD region source-gate overlap capacitance per channel length | F/m | calculated | **nC-1** |
| *CGD0* | cgdo | Non LDD region drain-gate overlap capacitance per channel length | F/m | calculated | **nC-2** |

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Note |
|---|---|---|---|---|---|
| *CGEO* | cgeo | **Gate substrate overlap capacitance per unit channel length** | F/m | 0.0 | - |
| *Cjswg* | cjswg | Source/Drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm $T_{si}$) | $F/m^2$ | 1e-10 | - |
| *Pbswg* | pbswg | Source/Drain (gate side) sidewall junction capacitance buit in potential | V | .7 | - |
| *Mjswg* | mjswg | Source/Drain (gate side) sidewall junction capacitance grading coefficient | V | 0.5 | - |
| $t_t$ | tt | **Diffusion capacitance transit time coefficient** | second | 1ps | - |
| $V_{sdfb}$ | vsdfb | **Source/drain bottom diffusion capacitance flatband voltage** | V | calcu-lated | nC-3 |
| $V_{sdth}$ | vsdth | **Source/drain bottom diffusion capacitance threshold voltage** | V | calcu-lated | nC-4 |
| $C_{sdmin}$ | csdmin | **Source/drain bottom diffusion minimum capacitance** | V | calcu-lated | nC-5 |
| $A_{sd}$ | asd | **Source/drain bottom diffusion smoothing parameter** | - | 0.3 | - |
| $C_{sdesw}$ | csdesw | **Source/drain sidewall fringing capacitance per unit length** | F/m | 0.0 | - |
| *CGS1* | cgs1 | Light doped source-gate region overlap capacitance | F/m | 0.0 | - |
| *CGD1* | cgd1 | Light doped drain-gate region overlap capacitance | F/m | 0.0 | - |

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Note |
|---|---|---|---|---|---|
| *CKAPPA* | ckappa | Coefficient for lightly doped region overlap capacitance fringing field capacitance | F/m | 0.6 | - |
| *Cf* | cf | Gate to source/drain fringing field capacitance | F/m | calcu-lated | **nC-6** |
| *CLC* | clc | Constant term for the short channel model | m | $0.1x10^{-7}$ | - |
| *CLE* | cle | Exponential term fro the short channel model | none | 0.0 | - |
| *DLC* | dlc | Length offset fitting parameter from C-V | m | lint | - |
| *DWC* | dwc | Width offset fitting parameter from C-V | m | wint | - |

## B.5. Temperature Parameters

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Note |
|---|---|---|---|---|---|
| *Tnom* | tnom | Temperature at which parameters are expected | °C | 27 | - |
| *μte* | ute | Mobility temperature exponent | none | -1.5 | - |
| *Kt1* | kt1 | Temperature coefficient for threshold voltage | V | -0.11 | - |
| *Kt11* | kt11 | Channel length dependence of the temperature coefficient for threshold voltage | V*m | 0.0 | |
| *Kt2* | kt2 | Body-bias coefficient of the Vth temperature effect | none | 0.022 | - |
| *Ua1* | ua1 | Temperature coefficient for $U_a$ | m/V | 4.31e-9 | - |
| *Ub2* | ub1 | Temperature coefficient for $U_b$ | $(m/V)^2$ | -7.61e-18 | - |
| *Uc1* | uc1 | Temperature coefficient for Uc | 1/V | -.056 | **nT-1** |
| *At* | at | Temperature coefficient for saturation velocity | m/sec | 3.3e4 | - |

| Symbol used in equation | Symbol used in SPICE | Description | Unit | Default | Note |
|---|---|---|---|---|---|
| ***Cth0*** | **cth0** | **Normalized thermal capacity** | **m°C/ (W*sec)** | **0** | - |
| *Prt* | prt | Temperature coefficient for Rdsw | Ω-μm | 0 | - |
| ***Rth0*** | **rth0** | **Normalized thermal resistance** | **m°C/W** | **0** | - |
| $X_{bjt}$ | **xbjt** | **Power dependence of $j_{bjt}$ on temperature** | **none** | **2** | - |
| $X_{dif}$ | **xdif** | **Power dependence of $j_{dif}$ on temperature** | **none** | **2** | - |
| $X_{rec}$ | **xrec** | **Power dependence of $j_{rec}$ on temperature** | **none** | **20** | - |
| $X_{tun}$ | **xtun** | **Power dependence of $j_{tun}$ on temperature** | **none** | **0** | - |

## B.6. Model Parameter Notes

**nI-1.** C*apmod* 0 and 1 do not have the dynamic depletion calculation. Therefore ddMod does not work with these *capmod*. Users are recommended to use *capmod* 2 or 3.

**nI-2.** BSIMSOI refers substrate to the silicon below buried oxide, not the well region in BSIM3. It is used to calculate backgate flatband voltage ($V_{fbb}$) and parameters related to source/drain diffusion bottom capacitance ($V_{sdth}$, $V_{sdfb}$, $C_{sdmin}$). Positive $n_{sub}$ means the same type of doping as the body and negative $n_{sub}$ means opposite type of doping.

**nI-3.** For FD device, $V_{th0}$ is **not** equal to the measured long and wide device threshold voltage because $V_{bs0}$ is higher than zero.

**nC-1.** If *cgso* is not given then it is calculated using:

if (*dlc* is given and is greater 0) then,

$cgso = pl = (dlc*cox) - cgsl$

if (the previously calculated *cgso* <0), then

$cgso = 0$

else $cgso = 0.6 * Tsi * cox$

**nC-2.** *Cgdo* is calculated in a way similar to *Csdo*

**nC-3.** If ($n_{sub}$ is positive)

$$V_{sdfb} = -\frac{kT}{q}\log\left(\frac{10^{20}\cdot n_{sub}}{n_i \cdot n_i}\right) - 0.3$$

else

$$V_{sdfb} = -\frac{kT}{q}\log\left(\frac{10^{20}}{n_{sub}}\right) + 0.3$$

**nC-4.** If ($n_{sub}$ is positive)

$$\phi_{sd} = 2\frac{kT}{q}\log\left(\frac{n_{sub}}{n_i}\right),\ \gamma_{sd} = \frac{5.753\times10^{-12}\sqrt{n_{sub}}}{C_{box}}$$

$$V_{sdth} = V_{sdfb} + \phi_{sd} + \gamma_{sd}\sqrt{\phi_{sd}}$$

else

$$\phi_{sd} = 2\frac{kT}{q}\log\left(-\frac{n_{sub}}{n_i}\right),\ \gamma_{sd} = \frac{5.753\times10^{-12}\sqrt{-n_{sub}}}{C_{box}}$$

$$V_{sdth} = V_{sdfb} - \phi_{sd} - \gamma_{sd}\sqrt{\phi_{sd}}$$

**nC-5.** $X_{sddep} = \sqrt{\dfrac{2\varepsilon_{si}\phi_{sd}}{q\left|n_{sub}\cdot 10^{6}\right|}}$, $C_{sddep} = \dfrac{\varepsilon_{si}}{X_{sddep}}$, $C_{sd\,\min} = \dfrac{C_{sddep}C_{box}}{C_{sddep}+C_{box}}$

**nC-6.** If cf is not given then it is calculated using

$$CF = \frac{2\varepsilon_{ox}}{\pi}\ln\left(1+\frac{4\times10^{-7}}{T_{ox}}\right)$$

**nT-1.** For mobmod=1 and 2, the unit is $m/V^2$. Default is -5.6E-11. For mobmod=3, unit is 1/V and default is -0.056.

# Appendix C: Equation List

## C.1. I-V Model

### C.1.1. $V_{bs0}$ - Body potential at full depletion and strong inversion conditions

(assuming no substrate depletion)

$$T_{sieff} = \sqrt{T_{si}^{\ 2} - 2\frac{\varepsilon_{si} V_{bsa}}{qN_a}},\ C_{sieff} = \frac{\varepsilon_{si}}{T_{sieff}},\ Q_{sieff} = qN_a T_{sieff}$$

$$V_{bs0t} = \phi_s - 0.5 \cdot Q_{si}/C_{si} + V_{bsa} + D_{vbd0} \cdot \left[\exp\left(-D_{vbd1}\frac{L_{eff}}{2litl}\right) + 2\exp\left(-D_{vbd1}\frac{L_{eff}}{litl}\right)\right] \cdot (V_{bi} - \phi_s)$$

$$V_{bs0} = V_{bs0t} - K_{b1}\frac{V_{bs0t} - V_{es} + V_{fbb}}{1 + C_{sieff}/C_{box}}$$

### C.1.2. $V_{thfd}$ - Threshold voltage at fully depleted condition ($V_{bs} = V_{bs0}$)

$$V_{thfd} = V_{th}(V_{bs} = V_{bs0})$$

### C.1.3. $V_{bs0eff}$ / $V_{bs0teff}$ - Effective $V_{bs0}$ / $V_{bs0t}$ for all $V_{gs}$

$$T_0 = 0.5\left[\left(V_{thfd} - V_{gs\_eff}\right) - \delta_1 + \sqrt{\left[\left(V_{thfd} - V_{gs\_eff}\right) - \delta_1\right]^2 + \delta_1^2}\right]$$

$$V_{bs0teff} = V_{bs0t} - T_0$$

$$V_{bs0eff} = V_{bs0} - n_{Fb} \cdot T_0$$

$$n_{Fb} = \frac{1}{1 + K_{3b}\frac{C_{box}}{C_{ox}}\sqrt{1 + \frac{4}{K_1^2}\left(\phi_s + K_1\sqrt{\phi_s - V_{bs0mos}} - V_{bs0mos}\right)}}$$

where $V_{bs0mos}$ is the effective $V_{bs}$ when $V_{bs} = V_{bs0}$

It basically make $V_{bs0eff}$ & $V_{bs0teff}$ a function of $V_{gs}$ as the following if $V_{gs} < V_{thfd}$

$$V_{bs0eff} = V_{bs0} + n_{Fb}\left(V_{gs} - V_{thfd}\right)$$

$$V_{bs0teff} = V_{bs0t} + \left(V_{gs} - V_{thfd}\right)$$

### C.1.4. $V_{bseff}$ - Equivalent $V_{bs}$ bias for MOS IV calculation

$$T_1 = 0.5\left[\left(V_{bs0teff} - V_{bs}\right) - \delta_2 + \sqrt{\left[\left(V_{bs0teff} - V_{bs}\right) - \delta_2\right]^2 + \delta_2^2}\right]$$

$$V_{bsmos} = V_{bs} - \frac{C_{sieff} T_1^2}{2 \cdot Q_{sieff}}$$

It basically make $V_{bsmos}$ a function of $V_{bs0teff}$ as the following if $V_{bs} < V_{bs0teff}$

$$V_{bsmos} = V_{bs} - \frac{C_{sieff}\left(V_{bs0teff} - V_{bs}\right)^2}{2 \cdot Q_{sieff}}$$

otherwise

$$V_{bsmos} = V_{bs}$$

(note $V_{bs}$ is properly bounded to $V_{bs0eff}$ because of the diode implementation)

**$V_{bseff} = V_{bsmos}$ is limited to $\phi_s - delp$ by the following conversion :**

$$V_{bseff} = (\phi_s - delp) - 0.5\left[(\phi_s - delp - V_{bsmos}) - \delta_1 + \sqrt{\left[(\phi_s - delp - V_{bsmos}) - \delta_1\right]^2 + 4\delta_1(\phi_s - delp)}\right]$$

## C.1.5. Threshold Voltage

$$V_{th} = V_{tho} + K_1(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}) - K_2 V_{bseff}$$

$$+ K_1\left(\sqrt{1 + \frac{N_{LX}}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + (K_3 + K_{3b}V_{bseff})\frac{T_{ox}}{W_{eff+}W_o}\Phi_s$$

$$- D_{VT0w}\left(\exp\left(-D_{VT1w}\frac{W_{eff}L_{eff}}{2l_{tw}}\right) + 2\exp\left(-D_{VT1w}\frac{W_{eff}L_{eff}}{l_{tw}}\right)\right)(V_{bi} - \Phi_s)$$

$$- D_{VT0}\left(\left(\exp - D_{VT1}\frac{L_{eff}}{2l_t}\right) + 2\exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right)(V_{bi} - \Phi_s)$$

$$- \left(\exp\left(-D_{sub}\frac{L_{eff}}{2l_{to}}\right) + 2\exp\left(-D_{sub}\frac{L_{eff}}{l_{to}}\right)\right)(E_{tao} + E_{tab}V_{bseff})V_{ds}$$

$$l_t = \sqrt{\varepsilon_{si}X_{dep} / C_{ox}}(1 + D_{VT2}V_{bseff})$$

$$l_{tw} = \sqrt{\varepsilon_{si}X_{dep}/C_{ox}}(1 + D_{VT2w}V_{bseff}) \qquad l_{to} = \sqrt{\varepsilon_{si}X_{dep0} / C_{ox}}$$

$$X_{dep} = \sqrt{\frac{2\varepsilon_{si}(\Phi_s - V_{bseff})}{qN_{ch}}} \qquad X_{dep0} = \sqrt{\frac{2\varepsilon_{si}\Phi_s}{qN_{ch}}}$$

$$V_{bi} = v_t \ln\left(\frac{N_{ch}N_{DS}}{n_i^2}\right) \qquad litl = \sqrt{3T_{si}T_{ox}}$$

## C.1.6. Poly depletion effect

$$V_{poly} + \frac{1}{2}X_{poly}E_{poly} = \frac{qN_{gate}X^2_{poly}}{2\varepsilon_{si}}$$

$$\varepsilon_{ox}E_{ox} = \varepsilon_{si}E_{poly} = \sqrt{2q\varepsilon_{si}N_{gate}V_{poly}}$$

$$V_{gs} - V_{FB} - \phi_x = V_{poly} + V_{ox}$$

$$a(V_{gs} - V_{FB} - \phi_s - V_{poly})^2 - V_{poly} = 0$$

$$a = \frac{\varepsilon^2_{ox}}{2q\varepsilon_{si}N_{gate}T^2_{ox}}$$

$$V_{gs\_eff} = V_{FB} + \phi_s + \frac{q\varepsilon_{si}N_{gate}T^2_{ox}}{\varepsilon^2_{ox}}\left(\sqrt{1+\frac{2\varepsilon^2_{ox}(V_{gs}-V_{FB}-\phi_s)}{q\varepsilon_{si}N_{gate}T^2_{ox}}}-1\right)$$

### C.1.7. Effective $V_{gst}$ for all region (with Polysilicon Depletion Effect)

$$V_{gsteff} = \frac{2nv_t \ln\left[1+\exp\left(\frac{V_{gs\_eff}-V_{th}}{2nv_t}\right)\right]}{1+2nC_{ox}\sqrt{\frac{2\Phi_s}{q\varepsilon_{si}N_{ch}}}\exp\left(-\frac{V_{gs\_eff}-V_{th}-2V_{off}}{2nv_t}\right)}$$

$$n = 1+N_{factor}\frac{\varepsilon_{si}/X_{dep}}{C_{ox}}+\frac{(C_{dsc}+C_{dscd}V_{ds}+C_{dscb}V_{bseff})\left(\exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right)+2\exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right)}{C_{ox}}+\frac{C_{it}}{C_{ox}}$$

### C.1.8. Effective Bulk Charge Factor

$$V_{cs} = V_{bs} - V_{bs0eff}$$

$$T_1 = 1 - 0.5\left[\left(1 - \frac{V_{cs}}{A_{bp}V_{gsteff}}\right) - \delta_1 + \sqrt{\left[\left(1 - \frac{V_{cs}}{A_{bp}V_{gsteff}}\right) - \delta_1\right]^2 + \delta_1{}^2}\right]$$

$$X_{csat} = m_{xc}T_1^2 + (1 - m_{xc})T_1$$

$X_{csat}$ is a parameter describing the dynamic depletion effect for a given $V_{gs}$. It varies within (0, 1). The parameter $m_{xc}$ is used to adjust the slope of transition.

$$A_{bulk} = 1 + \left(\frac{K_1}{2\sqrt{\phi_s}}\left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{T_{si}X_{dep}}}\left(1 - A_{gs}V_{gsteff}\left(\frac{L_{eff}}{L_{eff} + 2\sqrt{T_{si}X_{dep}}}\right)^2\right) + \frac{B_0}{W_{eff} + B_1}\right)\right)\frac{1}{1 + Keta \cdot V_{bseff}}$$

$$A_{beff} = X_{csat}A_{bulk} + (1 - X_{csat})A_{dice},\ A_{dice} = \frac{A_{dice0}}{1 + C_{boxt}/C_{ox}},\ C_{cboxt} = \frac{C_{si}C_{box}}{C_{si} + C_{box}}$$

### C.1.9. Mobility and Saturation Velocity

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})(\frac{V_{gsteff}}{T_{ox}}) + U_b(\frac{V_{gsteff}}{T_{ox}})^2}$$

For Mobmod=3

$$\mu_{eff} = \frac{\mu_0}{1 + [U_a(\frac{V_{gstef} + 2V_{th}}{T_{ox}}) + U_b(\frac{V_{gsteff} + 2V_{th}}{T_{ox}})^2](1 + U_c V_{bseff})}$$

### C.1.10. Drain Saturation Voltage

For $R_{ds}>0$ or $\lambda \neq 1$:

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

$$a = A_{beff}{}^2 W_{eff} \nu_{sat} C_{ox} R_{DS} + (\frac{1}{\lambda} - 1) A_{beff}$$

$$b = -((V_{gsteff} + 2\nu_t)(\frac{2}{\lambda} - 1) + A_{beff} E_{sat} L_{eff} + 3A_{beff}(V_{gsteff} + 2\nu_t) W_{eff} \nu_{sat} C_{ox} R_{DS})$$

$$c = (V_{gsteff} + 2\nu_t) E_{sat} L_{eff} + 2(V_{gsteff} + 2\nu_t)^2 W_{eff} \nu_{sat} C_{ox} R_{DS}$$

$$\lambda = A_1 V_{gsteff} + A_2$$

For $R_{ds}$=0, $\lambda$=1:

$$V_{dsat} = \frac{E_{sat} L_{eff} (V_{gsteff} + 2\nu_t)}{A_{beff} E_{sat} L_{eff} + (V_{gsteff} + 2\nu_t)}$$

$$E_{sat} = \frac{2\nu_{sat}}{\mu_{eff}}$$

### C.1.11. $V_{dseff}$

$$V_{dseff} = V_{dsat} - \frac{1}{2}(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}})$$ ($\delta$ is parameter Delta)

### C.1.12. Drain current expression

$$I_{ds,MOSFET} = \frac{I_{ds0}(V_{dseff})}{1 + \frac{R_{ds} I_{dso}(V_{dseff})}{V_{dseff}}} (1 + \frac{V_{ds} - V_{dseff}}{V_A})$$

$$\beta = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}}$$

$$I_{dso} = \frac{\beta V_{gsteff} \left(1 - A_{beff} \frac{V_{dseff}}{2[V_{gsteff} + 2\nu_t]}\right) V_{dseff}}{1 + \frac{V_{dseff}}{E_{sat} L_{eff}}}$$

$$V_A = V_{Asat} + \left(1 + \frac{P_{vag} V_{gsteff}}{E_{sat} L_{eff}}\right)\left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}}\right)^{-1}$$

$$V_{ACLM} = \frac{A_{beff} E_{sat} L_{eff} + V_{gsteff}}{P_{clm} A_{beff} E_{sat} litl}(V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout}(1 + P_{DIBLCB} V_{bseff})}\left(1 - \frac{A_{beff} V_{dsat}}{A_{beff} V_{dsat} + 2v_t}\right)$$

$$\theta_{rout} = P_{DIBLC1}\left[\exp\left(-D_{ROUT}\frac{L_{eff}}{2l_{t0}}\right) + 2\exp\left(-D_{ROUT}\frac{L_{eff}}{l_{t0}}\right)\right] + P_{DIBLC2}$$

$$V_{Asat} = \frac{E_{sat} L_{eff} + V_{dsat} + 2R_{DS} v_{sat} C_{ox} W_{eff} V_{gsteff}\left[1 - \frac{A_{beff} V_{dsat}}{2(V_{gsteff} + 2v_t)}\right]}{2/\lambda - 1 + R_{DS} v_{sat} C_{ox} W_{eff} A_{beff}}$$

$$litl = \sqrt{\frac{\varepsilon_{si} T_{ox} T_{Si}}{\varepsilon_{ox}}}$$

### C.1.13.Drain/Source Resistance

$$R_{ds} = R_{dsw}\frac{1 + P_{rwg} V_{gsteff} + P_{rwb}\left(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s}\right)}{\left(10^6 W_{eff}\right)^{Wr}}$$

### C.1.14. Impact Ionization Current

$$I_{ii} = \frac{\alpha_0 + \alpha_1 L_{eff}}{L_{eff}} \cdot I_d \cdot V_{dseffii} \cdot \exp\left(-\frac{\beta_0}{V_{dseffii}}\right)$$

$$V_{dsatii} = \frac{E_{sat} L_{eff} V_{gst}}{M_1 E_{sat} L_{eff} + M_2 V_{gst}},\quad M_1 = A_{ii} + \frac{B_{ii}}{L_{eff}},\quad M_2 = 1 + \left(\frac{C_{ii}}{V_{ds} - D_{ii}}\right)^2$$

$V_{dseffii}$ is calculated the same way as $V_{dseff}$ with $V_{dsat}$ replaced by $V_{dsatii}$.

### C.1.15. Gate-Induced-Drain-Leakage (GIDL)

**At drain,** $I_{dgidl} = W_{eff}\alpha_{gidl} \cdot E_s \cdot \exp\left(-\frac{\beta_{gidl}}{E_s}\right),\ E_s = \frac{V_{ds} - V_{gs} - \chi}{3 \cdot T_{ox}}$

**At source,** $I_{sgidl} = W_{eff}\alpha_{gidl} \cdot E_s \cdot \exp\left(-\frac{\beta_{gidl}}{E_s}\right),\ E_s = \frac{-V_{gs} - \chi}{3 \cdot T_{ox}}$

default of $\chi$ is 1.2V.

If $E_s$ is negative, $I_{gidl}$ is set to zero for both drain and source.

### C.1.16. Body contact current

$$R_{bp} = R_{body0}\frac{W_{eff}}{L_{eff}},\ R_{bodyext} = R_{bsh}N_{rb}$$

**For 4-T device,** $I_{bp} = 0$

**For 5-T device,**

$$I_{bp} = \frac{V_{bp}}{\frac{R_{bp}}{\sqrt{V_{bs} - V_{bs0eff}}} + R_{bodyext}}$$

### *C.1.17. Diode and BJT currents*

**For source side,**

Bipolar Transport Factor

$$W_b = L_{eff} - k_{bjt1} \cdot V_{ds}, \qquad \alpha_{bjt} = 1 - 0.5\left(\frac{W_b}{Edl}\right)^2$$

$V_{bs0}$ for diode current

$$V_{bs0\_dio} = 0.5\left[V_{bs0eff} - \delta_1 + \sqrt{\left[V_{bs0eff} - \delta_1\right]^2 + 4\delta_1}\right]$$

BJT emitter current

$$I_{bjt} = W_{eff} T_{si} j_{sbjt}\left(e^{\frac{V_{bs}}{n_{dio} \cdot V_t}} - e^{\frac{V_{bs0\_dio}}{n_{dio} \cdot V_t}}\right)\left(1 - e^{-\frac{V_{ds}}{2n_{dio} \cdot V_t}}\right)$$

Body-to-Source diffusion

$$I_{bs1} = W_{eff} T_{si} j_{sdif}\left(e^{\frac{V_{bs}}{n_{dio} \cdot V_t}} - e^{\frac{V_{bs0\_dio}}{n_{dio} \cdot V_t}}\right)$$

Recombination in depletion region

$$I_{bs2} = W_{eff} T_{si} j_{srec}\left(e^{\frac{V_{bs}}{2n_{dio} \cdot V_t}} - e^{\frac{V_{bs0\_dio}}{2n_{dio} \cdot V_t}}\right)$$

Reversed bias tunneling leakage

$$I_{bs4} = W_{eff} T_{si} j_{stun} \left( 1 - e^{-\frac{V_{bs}}{n_{tun} \cdot V_t}} \right)$$

Recombination in neutral body

$$I_{bs3} = \left(1 - \alpha_{bjt}\right) I_{bjt}$$

BJT collector current

$$I_c = I_{bjt} - I_{bs3}$$

Total body-source current

$$I_{bs} = I_{bs1} + I_{bs2} + I_{bs3} + I_{bs4}$$

**For drain side,**

if $V_{bd} > V_{bs0\_dio}$

$$I_{bd1} = W_{eff} T_{si} j_{sdif} \left( e^{\frac{V_{bd}}{n \cdot V_t}} - e^{\frac{V_{bs0\_dio}}{n \cdot V_t}} \right)$$

$$I_{bd2} = W_{eff} T_{si} j_{srec} \left( e^{\frac{V_{bd}}{2n \cdot V_t}} - e^{\frac{V_{bs0\_dio}}{2n \cdot V_t}} \right)$$

else

$$I_{bd1} = W_{eff} T_{si} j_{sdif} \left( e^{\frac{V_{bd} - V_{bs0\_dio}}{n_{dio} \cdot V_t}} - 1 \right)$$

$$I_{bd2} = W_{eff} T_{si} j_{srec} \left( e^{\frac{V_{bd} - V_{bs0}}{2n_{dio} \cdot V_t}} - 1 \right)$$

$$I_{bd4} = W_{eff} T_{si} j_{stun} \left( 1 - e^{-\frac{V_{bd}}{n_{tun} \cdot V_t}} \right)$$

Total body-drain current

$$I_{bd} = I_{bd1} + I_{bd2} + I_{bd4}$$

### C.1.18. Total body current

$$I_{ii} + I_{dgidl} + I_{sgidl} - I_{bs} - I_{bd} - I_{bp} = 0$$

### C.1.19.Temperature effects

$$V_{th(T)} = V_{th(Tnorm)} + (K_{T1} + K_{t1l} / L_{eff} + K_{T2} V_{bseff})(T / T_{norm} - 1)$$

$$\mu_{o(T)} = \mu_{o(Tnorm)} (\frac{T}{T_{norm}})^{\mu te} \quad v_{sat(T)} = v_{sat(Tnorm)} - A_T (T / T_{norm} - 1)$$

,

$$R_{dsw(T)} = R_{dsw(T_{norm})} + P_{rt} (\frac{T}{T_{norm}} - 1)$$

$$U_{a(T)} = U_{a(Tnorm)} + U_{a1} (T / T_{norm} - 1)$$

$$U_{b(T)} = U_{b(Tnorm)} + U_{b1} (T / T_{norm} - 1)$$

$$U_{c(T)} = U_{c(Tnorm)} + U_{c1} (T / T_{norm} - 1)$$

$$R_{th} = R_{th0} \sqrt{\frac{T_{box}}{T_{si}}} / W_{eff} \,, \quad C_{th} = C_{th0} \cdot W_{eff}$$

$$j_{sbjt} = i_{sbjt} \left( \frac{T}{T_{nom}} \right)^{X_{bjt}/n} \exp\left[ -\frac{qE_g(300)}{nkT} \left( 1 - \frac{T}{T_{nom}} \right) \right]$$

$$j_{sdif} = i_{sdif} \left( \frac{T}{T_{nom}} \right)^{X_{sdif}/n} \exp\left[ -\frac{qE_g(300)}{nkT} \left( 1 - \frac{T}{T_{nom}} \right) \right]$$

$$j_{srec} = i_{srec}\left(\frac{T}{T_{nom}}\right)^{X_{srec}/2n} \exp\left[-\frac{qE_g(300)}{2nkT}\left(1-\frac{T}{T_{nom}}\right)\right]$$

$$j_{stun} = i_{stun}\left(\frac{T}{T_{nom}}\right)^{X_{stun}/n_t}$$

$E_g(300)$ is the energy gap energy at 300K.

# C.2. C-V Model

## C.2.1. Dimension Dependence

$$\delta W_{eff} = DWC + \frac{Wl}{L^{Wln}} + \frac{Ww}{W^{Wwn}} + \frac{Wwl}{L^{Wln}W^{Wwn}}$$

$$\delta L_{eff} = DLC + \frac{Ll}{L^{Lln}} + \frac{Lw}{W^{Lwn}} + \frac{Lwl}{L^{Lln}W^{Lwn}}$$

$$L_{active} = L_{drawn} - 2\delta L_{eff}$$

$$W_{active} = W_{drawn} - 2\delta W_{eff}$$

## C.2.2. Charge Conservation

$$Q_{Bf} = Q_{ac0} + Q_{sub0} + Q_{subs}$$

$$Q_{inv} = Q_{inv,s} + Q_{inv,d}$$

$$Q_g = -\left(Q_{inv} + Q_{Bf} + Q_{e2}\right)$$

$$Q_e = Q_{e1} + Q_{e2}$$

$$Q_b = Q_{Bf} - Q_{e1} + Q_{js} + Q_{jd}$$

$$Q_s = Q_{inv,s} - Q_{js}$$

$$Q_d = Q_{inv,d} - Q_{jd}$$

$$Q_g + Q_e + Q_b + Q_s + Q_d = 0$$

### *C.2.3. Front Gate Body Charge*

#### C.2.3.1. Accumulation Charge

$$V_{FBeff} = V_{fb} - 0.5\left[(V_{fb} - V_{gb} - \delta) + \sqrt{(V_{fb} - V_{gb} - \delta)^2 + \delta^2}\right]$$

where $V_{gb} = V_{gs} - V_{bseff}$

$$V_{fb} = V_{th} - \phi_s - K_1\sqrt{\phi_s - V_{bseff}}$$

$$V_{gsteff,cv} = nv_t \ln\left(1 + \exp\left[\frac{V_{gs} - V_{th}}{nv_t}\right]\right)$$

$$Q_{acc} = -W_{active} L_{active} C_{ox} (V_{FBeff} - V_{fb})$$

#### C.2.3.2. Gate Induced Depletion Charge

$$Q_{sub0} = -W_{active} L_{active} C_{ox} \frac{K_1^2}{2}\left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FBeff} - V_{gsteffcv} - V_{bseff})}{K_1^2}}\right)$$

#### C.2.3.3. Drain Induced Depletion Charge

For capMod = 2

$$V_{dsatCV} = V_{gsteffCV} / A_{bulkCV}$$

$$V_{dsCV} = V_{dsatCV} - \frac{1}{2}(V_{dsatCV} - V_{ds} - \delta + \sqrt{(V_{dsatCV} - V_{ds} - \delta)^2 + 4\delta V_{dsatCV}})$$

$$V_{csCV} = V_{cs} + 0.5\left(V_{dsCV} - V_{cs} + \delta - \sqrt{(V_{dsCV} - V_{cs} + \delta)^2 + 4\delta V_{dsCV}}\right)$$

$V_{dsCV}$ is equal to $V_{dsatCV}$ when $V_{dseff}$ is equal to $V_{dsatCV}$.

$$X_c = \frac{[2V_{dsatCV} - V_{csCV}]V_{csCV}}{[2V_{dsatCV} - V_{dsCV}]V_{dsCV}}$$

For capMod = 3

$$V_{dsatCV} = V_{gsteff} + K_1\sqrt{\phi_s} + \frac{K_1^2}{2} - K_1\sqrt{V_{gsteff} + K_1\sqrt{\phi_s} + \phi_s + \frac{K_1^2}{4}}$$

$$V_{dsCV} = V_{dseff} + (V_{dsatCV} - V_{dsat})\left(\frac{V_{dseff}}{V_{dsat}}\right)^2$$

$$V_{csCV} = V_{cs} + 0.5\left(V_{dsCV} - V_{cs} + \delta - \sqrt{(V_{dsCV} - V_{cs} + \delta)^2 + 4\delta V_{dsCV}}\right)$$

$$X_c = \frac{V_{csCV}\left(V_{gsteff} + K_1\sqrt{\phi_s - V_{bs}} - 0.5\cdot V_{csCV}\right) - \frac{2}{3}K_1\left[(\phi_s + V_{csCV} - V_{bs})^{3/2} - (\phi_s - V_{bs})^{3/2}\right]}{V_{dsCV}\left(V_{gsteff} + K_1\sqrt{\phi_s - V_{bs}} - 0.5\cdot V_{dsCV}\right) - \frac{2}{3}K_1\left[(\phi_s + V_{dsCV} - V_{bs})^{3/2} - (\phi_s - V_{bs})^{3/2}\right]}$$

$$Q_{subs1} = W_{eff} L_{eff} C_{ox} K_1 \frac{K_1\left[\frac{2}{3}\left(V_{gsteff} + K_1\sqrt{\phi_s - V_{bs}} + (\phi_s - V_{bs})\right)\left((\phi_s + V_{csCV} - V_{bs})^{1/2} - (\phi_s - V_{bs})^{1/2}\right) - 0.4\left((\phi_s + V_{csCV} - V_{bs})^{3/2} - (\phi_s - V_{bs})^{3/2}\right) - K_1 V_{csCV}\left((\phi_s - V_{bs}) + 0.5\cdot V_{dsCV}\right)\right]}{V_{dsCV}\left(V_{gsteff} + K_1\sqrt{\phi_s - V_{bs}} - 0.5\cdot V_{dsCV}\right) - \frac{2}{3}K_1\left[(\phi_s + V_{dsCV} - V_{bs})^{3/2} - (\phi_s - V_{bs})^{3/2}\right]}$$

$$Q_{subs2} = W_{effCV} L_{effCV} C_{ox} K_1\sqrt{\phi_s - V_{bs0eff}}\cdot(1 - X_c)$$

### C.2.3.4.Back Gate Body Charge

$$Q_{sicv} = C_{ox} WL \frac{K_1^2}{2}\left[1 - \sqrt{1 + \frac{4\left(\phi_s + K_1\sqrt{\phi_s - V_{bs0t}} - V_{bs0t}\right)}{K_1^2}}\right]$$

$$Q_{bf0} = C_{ox}\frac{K_1^2}{2}\left(1 - \sqrt{1 + \frac{4(\phi_s + K_1\sqrt{\phi_s - V_{bs0mos}} - V_{bs0mos})}{K_1^2}}\right)$$

$$Q_{e1} = -Q_{sicv} + Q_{bf0} - WX_c LC_{box}(V_{bs} - V_{bs0})$$

$$Q_{e2} = -WLC_{boxt}\frac{1 - X_c}{2}(V_{dsCV} - V_{csCV})$$

### *C.2.4. Inversion Charge*

$$Q_{inv} = -W_{active} L_{active} C_{ox} \left( \left( V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right) + \frac{A_{bulkCV}^{\ 2} V_{cveff}^{\ 2}}{12 \left( V_{gsteffCV} - \frac{A_{bulkCV}^{\ 2}}{2} V_{cveff} \right)} \right)$$

#### C.2.4.1. 50/50 Charge Partition

$$Q_{inv,s} = Q_{inv,.d} = 0.5 \cdot Q_{inv}$$

#### C.2.4.2. 40/60 Charge Partition

$$Q_{inv,s} = -\frac{W_{active} L_{active} C_{ox}}{2 \left( V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cvefff} \right)^2} \left( V_{gsteffCV}^{\ 3} - \frac{4}{3} V_{gsteffCV}^{\ 2} \left( A_{bulkCV} V_{cveff} \right) + \frac{2}{3} V_{gsteff} \left( A_{bulkCV} V_{cveff} \right)^2 - \frac{2}{15} \left( A_{bulkCV} V_{cveff} \right)^3 \right)$$

$$Q_{inv,d} = -\frac{W_{active} L_{active} C_{ox}}{2 \left( V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cvefff} \right)^2} \left( V_{gsteffCV}^{\ 3} - \frac{5}{3} V_{gsteffCV}^{\ 2} \left( A_{bulkCV} V_{cveff} \right) + V_{gsteff} \left( A_{bulkCV} V_{cveff} \right)^2 - \frac{1}{5} \left( A_{bulkCV} V_{cveff} \right)^3 \right)$$

#### C.2.4.3. 0/100 Charge Partition

$$Q_{inv,s} = -W_{active} L_{active} C_{ox} \left( \frac{V_{gsteffCV}}{2} + \frac{A_{bulkCV} V_{cveff}}{4} - \frac{\left( A_{bulkCV} V_{cveff} \right)^2}{24 \left( V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right)} \right)$$

$$Q_{inv,d} = -W_{active} L_{active} C_{ox} \left( \frac{V_{gsteffCV}}{2} - \frac{3 A_{bulkCV} V_{cveff}}{4} + \frac{\left( A_{bulkCV} V_{cveff} \right)^2}{8 \left( V_{gsteffCV} - \frac{A_{bulkCV}}{2} V_{cveff} \right)} \right)$$

## *C.2.5. Overlap Capacitance*

### C.2.5.1. Source Overlap Capacitance

$$V_{gs\_overlap} = \frac{1}{2}\left\{(V_{gs}+\delta)+\sqrt{(V_{gs}+\delta)^2+4\delta}\right\}$$

$$\frac{Q_{overlap,s}}{W_{active}} = CGS0\cdot V_{gs} + CGS1\left\{V_{gs}-V_{gs\_overlap}+\frac{CKAPPA}{2}\left(-1+\sqrt{1+\frac{4V_{gs\_overlap}}{CKAPPA}}\right)\right\}$$

### C.2.5.2. Drain Overlap Capacitance

$$V_{gd\_overlap} = \frac{1}{2}\left\{(V_{gd}+\delta)+\sqrt{(V_{gd}+\delta)^2+4\delta}\right\}$$

$$\frac{Q_{overlap,d}}{W_{active}} = CGD0\cdot V_{gd} + CGD1\left\{V_{gd}-V_{gd\_overlap}+\frac{CKAPPA}{2}\left(-1+\sqrt{1+\frac{4V_{gd\_overlap}}{CKAPPA}}\right)\right\}$$

### C.2.5.3. Gate Overlap Capacitance

$$Q_{overlap,g} = -\left(Q_{overlap,s}+Q_{overlap,d}\right)$$

### C.2.5.4.Source/Drain Junction Charge

**For $V_{bs} < 0$**

$$Q_{jswg} = C_{jswg}\frac{T_{si}}{10^{-7}}G_1\frac{P_{bswg}}{1-Mj_{swg}}\left[1-\left(1-\frac{V_{bs}}{P_{bswg}}\right)^{1-M_{jswg}}\right]+T_t\cdot I_{bs1}$$

**else**

$$Q_{jswg} = C_{jswg}\frac{T_{si}}{10^{-7}}G_1 V_{bs}\left(1+\frac{0.5M_{jswg}V_{bs}}{P_{bswg}}\right)+T_t\cdot I_{bs1}$$

**For $V_{bd} < 0$**

$$Q_{jdwg} = C_{jswg}\frac{T_{si}}{10^{-7}}G_2\frac{P_{bswg}}{1-Mj_{swg}}\left[1-\left(1-\frac{V_{bd}}{P_{bswg}}\right)^{1-M_{jswg}}\right]+T_t\cdot I_{bd1}$$

**else**

$$Q_{jdwg} = C_{jswg}\frac{T_{si}}{10^{-7}}G_2 V_{bs}\left(1+\frac{0.5M_{jswg}V_{bd}}{P_{bswg}}\right)+T_t\cdot I_{bd1}$$

Source : $G_1 = \sqrt{\phi_s - V_{bs0eff}} - \sqrt{\phi_s - V_{bs}}$

Drain : $G_2 = \sqrt{\phi_s - V_{bs0eff}} - \sqrt{\phi_s + V_{cs}}$

## *C.2.6. Extrinsic Charges*

### C.2.6.1.Bottom S/D to Substrate Charge

$$C_{sld,e} = \begin{cases} C_{box} & if \quad V_{sld,e} < V_{sdfb} \\ C_{box} - \dfrac{1}{A_{sd}}\left(C_{box} - C_{\min}\right)\left(\dfrac{V_{sld,e} - V_{sdfb}}{V_{sdth} - V_{sdfb}}\right)^2 & elseif \quad V_{sld,e} < V_{sdfb} + A_{sd}\left(V_{sdth} - V_{sdfb}\right) \\ C_{\min} + \dfrac{1}{1-A_{sd}}\left(C_{box} - C_{\min}\right)\left(\dfrac{V_{sld,e} - V_{sdth}}{V_{sdth} - V_{sdfb}}\right)^2 & elseif \quad V_{sld,e} < V_{sdth} \\ C_{\min} & else \end{cases}$$

### C.2.6.2.Sidewall S/D to Substrate Charge

$$C_{sdesw} = C_{sdesw}\log\left(1+\frac{T_{si}}{T_{box}}\right)$$

### C.2.6.3.Gate to substrate overlap charge

$$C_{egov} = C_{eg0}\left(V_{gs} - V_{es}\right)$$

# Appendix D: Some Useful Charge Derivations

## D.1. Some derivations for the EBCI-BSIMSOI model

The channel potential can be derived as follow

$$q_i(y) = WC_{ox}\left[V_{gst} - V_y(y) - K_1\left(\sqrt{\phi_s - V_{bs} + V_y(y)} + \sqrt{\phi_s - V_{bs}}\right)\right] \tag{D.7}$$

At any point y along the channel

$$I_{ds}y = W\mu C_{ox}\left[\left(V_{gst} + K_1\sqrt{\phi_s - V_{bs}} - 0.5V_y(y)\right)V_y(y) - \frac{2}{3}K_1\left(\left(\phi_s - V_{bs} + V_y(y)\right)^{3/2} - \left(\phi_s - V_{bs}\right)^{3/2}\right)\right] \tag{D.8}$$

here assume constant mobility

$$I_{ds} = \frac{W\mu C_{ox}}{L}\left[\left(V_{gst} + K_1\sqrt{\phi_s - V_{bs}} - 0.5V_{ds}\right)V_{ds} - \frac{2}{3}K_1\left(\left(\phi_s - V_{bs} + V_{ds}\right)^{3/2} - \left(\phi_s - V_{bs}\right)^{3/2}\right)\right] \tag{D.9}$$

So y can be expressed as a function of channel potential $V_y$

$$\frac{y}{L} = \frac{\left(V_{gst} + K_1\sqrt{\phi_s - V_{bs}} - 0.5V_y(y)\right)V_y(y) - \frac{2}{3}K_1\left(\left(\phi_s - V_{bs} + V_y(y)\right)^{3/2} - \left(\phi_s - V_{bs}\right)^{3/2}\right)}{\left(V_{gst} + K_1\sqrt{\phi_s - V_{bs}} - 0.5V_{ds}\right)V_{ds} - \frac{2}{3}K_1\left(\left(\phi_s - V_{bs} + V_{ds}\right)^{3/2} - \left(\phi_s - V_{bs}\right)^{3/2}\right)} \tag{D.10}$$

At $y = X_cL$, $V_y = V_{cs}$, therefore

$$X_c = \frac{\left(V_{gst} + K_1\sqrt{\phi_s - V_{bs}} - 0.5V_{cs}\right)V_{cs} - \frac{2}{3}K_1\left(\left(\phi_s - V_{bs} + V_{cs}\right)^{3/2} - \left(\phi_s - V_{bs}\right)^{3/2}\right)}{\left(V_{gst} + K_1\sqrt{\phi_s - V_{bs}} - 0.5V_{ds}\right)V_{ds} - \frac{2}{3}K_1\left(\left(\phi_s - V_{bs} + V_{ds}\right)^{3/2} - \left(\phi_s - V_{bs}\right)^{3/2}\right)} \tag{D.11}$$

The depletion charge $Q_{subs1}$ can be calculated by this expression

$$Q_{subs1}(y) = WC_{ox}K_1 \int_0^{X_c} \sqrt{\phi_s - V_{bs} - V_y(y)}\,dy = WC_{ox}K_1 \int_0^{V_{cs}} \sqrt{\phi_s - V_{bs} - V_y}\left(\frac{dy}{dV_y}\right)dV_y \qquad \text{(D.12)}$$

$\frac{dy}{dV_y}$ can be calculated from (D.10). After integrating (D.12), $Q_{subs1}$ can be calculated

$$Q_{subs1} = W_{eff}L_{eff}C_{ox}K_1 \frac{K_1\left[\frac{2}{3}\left(V_{gsteff} + K_1\sqrt{\phi_s - V_{bs}} + (\phi_s - V_{bs})\right)\left((\phi_s + V_{dscv} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}}\right) - 0.4\left((\phi_s + V_{dscv} - V_{bs})^{\frac{5}{2}} - (\phi_s - V_{bs})^{\frac{5}{2}}\right) - K_1V_{dscv}\left((\phi_s - V_{bs}) + 0.5\cdot V_{dscv}\right)\right]}{V_{dscv}\left(V_{gsteff} + K_1\sqrt{\phi_s - V_{bs}} - 0.5\cdot V_{dscv}\right) - \frac{2}{3}K_1\left[(\phi_s + V_{dscv} - V_{bs})^{\frac{3}{2}} - (\phi_s - V_{bs})^{\frac{3}{2}}\right]} \qquad \text{(D.13)}$$

# Appendix E: References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