

Copyright © 1994, by the author(s).  
All rights reserved.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission.

**A PERFORMANCE-DRIVEN ROUTER FOR RF  
AND MICROWAVE ANALOG CIRCUIT DESIGN**

by

Edoardo Charbon, Gary Holmlund,  
Alberto Sangiovanni-Vincentelli, and Bruce Donecker

Memorandum No. UCB/ERL M94/40

25 May 1994

COVER PAGE

**A PERFORMANCE-DRIVEN ROUTER FOR RF  
AND MICROWAVE ANALOG CIRCUIT DESIGN**

by

Edoardo Charbon, Gary Holmlund,  
Alberto Sangiovanni-Vincentelli, and Bruce Donecker

Memorandum No. UCB/ERL M94/40

25 May 1994

**ELECTRONICS RESEARCH LABORATORY**

College of Engineering  
University of California, Berkeley  
94720

# A Performance-Driven Router for RF and Microwave Analog Circuit Design

## Abstract

Techniques are presented for the routing of RF and microwave circuits. In this approach, sensitivities of performance with respect to parasitics are calculated and a set of bounds on critical parasitics is derived. Sensitivities are used to generate weights for a cost function which drives an area router. The routing scheme consists of two distinct phases, detailed routing and refinement. First, connectivity and a subset of all parasitic constraints is implemented by a maze router based on the A\* algorithm. Then an expansion step is applied to all nets simultaneously to enforce all remaining constraints. Finally, a global check on all layout parasitics is performed. If violations are found, a new set of weights based on sensitivities and on the severity of each violation is recalculated and the routing is repeated. Results show the suitability of the approach and its effectiveness on benchmark examples.

## 1 Introduction

Great effort has been devoted over the years to create general purpose CAD tools for schematic design and optimization of RF and microwave circuits, among others [1, 2]. Considerable attention has also been devoted to parasitic extraction and modeling of interconnections in various technologies. In particular, stripline realizations of interconnect have been extensively studied for different technologies [3, 4, 5].

Layout synthesis has not received comparable attention in the literature due to the inherent complexity of the problem and to the lack of designs whose size could justify a CAD based approach. More recently however, the increasing complexity of monolithic RF and microwave integrated circuits (MMIC) suggests that an automated approach to the physical synthesis is preferable for efficiency, reliability and yield considerations. The main difficulty in designing a CAD tool for automated routing of microwave circuits is the distributed nature of the parasitics introduced by the various layout components. Hence, compact models for accurately characterizing parasitic effects on performance are hard to generate, thus making the design of specifications-driven algorithms a difficult task.

LINMIC [6], a knowledge-based interactive layout tool, was aimed at designers with minimum expertise by providing aids for the layout synthesis of MMICs at relatively low frequencies. Later, in [1] a CAD framework was proposed based on explicit 3-D simulation of all geometrical structures as a way of interactively achieve a satisfactory layout. A fundamental limitation of these approaches however, is that no explicit reference to performance is done during the physical design phase. Thus the effectiveness of the tools in obtaining high-performance layouts is strongly limited.

Other semi-automated topology-driven approaches to the routing of MMICs have also been proposed [7, 8]. These systems include template-based routines for the abutment of pre-defined cells implementing devices as well as interconnect. The knowledge of the relative position of all cells provides the starting point of the layout realization, thus strongly limiting the flexibility of the approach and its applicability to complex designs. In addition, due to the inherent requirements of the tools, the synthesis process often results in a large number of time-consuming iterations necessary to obtain a circuit which guarantees performance.

We propose a constraint-based approach to the routing of MMICs. The flow diagram of the approach is shown in Figure 1. Firstly, a constraint generator maps high-frequency performance specifications onto a set of bounds on all classes of distributed parasitic components of interconnections and devices. Using sensitivity analysis in combination with constrained optimization, bounds are calculated on parasitics so as to insure maximum flexibility in the physical realization of the layout [9]. Then, Sensitivities, in combination with performance specifications, are used to calculate a set of weights for the area router. The role of the weights is to control a cost function which penalizes those realizations with highly critical parasitics.

However, not all constraints can be effectively enforced by the area router. Equality constraints

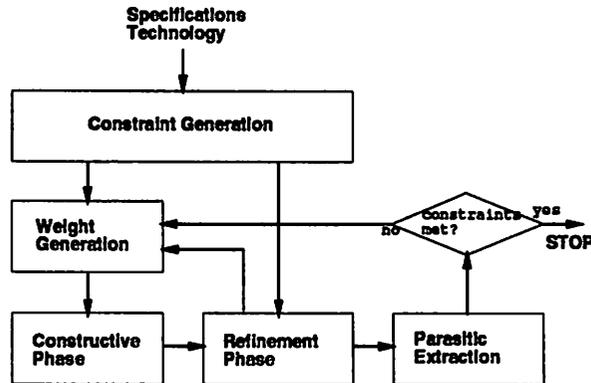


Figure 1: Flow diagram of the tool.

are generally absent at low frequencies, however in microwave circuits they play an essential role. For example the length of interconnection lines often need be enforced to a precise value since the functionality of the circuit is often based on the delay of signals and their reflections. Equality constraints are generally implemented in a cost function as a notch centered at the desired constraint value. However, a notch in the cost function of an area router can result in two major drawbacks. Due to its steepness a notch masks the cost function from other components everywhere except in the neighborhood of the notch center. As a result the quality of the solution chosen by the algorithm can be low since the remaining constraints have not been satisfied. Secondly, due to the local nature of the interconnect length estimator of the router, the algorithm tends to oscillate in the neighborhood of an obstacle. Hence, the router can yield highly convoluted interconnect realizations which often result in severe performance degradations.

A solution to these problems is to follow the routing or *constructive* phase, by a further step or *refinement*. The refinement is based on a progressive expansion of all nets simultaneously. All equality constraints are gradually enforced on all nets while no new violations are created on the remaining constraints. This is accomplished by defining a feasibility area within which the net expansion is allowed. The feasibility area is constantly updated after each expansion to insure that no additional violations are introduced. If infeasibility is detected a new set of weights is generated and the cycle is repeated. At the completion of the layout, the entire circuit is checked against constraint violations so as to verify that all performance specifications are met. Parasitics are directly extracted from all physical geometries and estimated by means of *ad hoc* analytical models based on 2-D and 3-D field analysis. In case a specification violation occurs, the parasitics responsible for the violation are identified and a sensitivity-based scheme is used to create a new set of weights. The cycle is then restarted. The finite step loop ends when all specifications are met.

There are several advantages to our approach. Firstly, the constraint generation phase can be

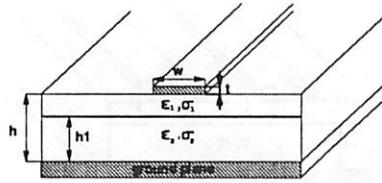


Figure 2: Single microstrip line over lossy substrate.

performed only once for each circuit, given a particular technology. Routing can be performed with a different cost weighting scheme to obtain higher compactness or higher performance. Furthermore, the constructive phase of the routing algorithm insures that a feasible layout is reached before performing a set of adjustments required to meet the final specifications. The model of performance dependence on parasitics, in combination with analytical parasitic modeling, allows efficient performance estimation.

The paper is organized as follows. In Section 2 the models for interconnect used in our layout synthesis approach are presented. In Section 3 the process of generating constraints on layout components for RF and microwave circuits is described. In Section 4 the constructive and the refinement phases of the router are outlined and in Section 5 the practical suitability of the approach is demonstrated through an example.

## 2 RF and Microwave Interconnect Modeling

Accurate interconnect modeling is a fundamental requirement of a constraint-driven approach to the routing of RF and microwave circuits. For reasons of efficiency closed formulae and analytical models for interconnect lines and all relevant parasitics are desirable. Since the area of application of this work is that of MMICs, all interconnect lines are modeled as microstrip transmission lines. Parasitic effects such as inductive and capacitive crosstalk are modeled as coupling capacitances and mutual inductances. Almost all models for interconnect can be represented by the two-dimensional setting of Figure 2. The transmission line is fully described by its characteristic impedance  $Z_o$  and loss  $\alpha$ .

Capacitive and inductive couplings caused by other lines can be easily included in the model as discrete passive components calculated by numerical 2-D field solvers. When coupling is induced by three-dimensional structures, complete 3-D solutions can be used. Using such methods it is possible to obtain correction terms  $\Delta Z_o$  and  $\Delta \alpha$  as a function of the geometries involved.

Discontinuities are modeled using discrete components, while radiation and surface-wave propagation effects have been neglected due to the the relative small circuit size if compared with the signal wavelengths. Substrate-dependent losses have been taken into account in the full model.

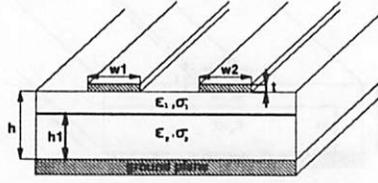


Figure 3: Coupled microstrip lines.

## 2.1 Modeling Single Interconnect Lines

Contrary to simple striplines, microstrip lines are inhomogeneous transmission lines since the field between strip and ground plane is not entirely included in the substrate. Therefore the dominant mode of propagation is not purely transverse electromagnetic (TEM) but quasi-TEM.

As a consequence the effective dielectric constant  $\epsilon_r$  of the transmission medium is lower than the substrate dielectric constants  $\epsilon_1, \epsilon_2$ . Closed forms for characteristic impedance  $Z_o$  and effective dielectric constant  $\epsilon_r$  have been derived using a number of *static* techniques, as reviewed in [10, 11]. Statically derived formulae are quite accurate at frequency below a few gigahertz. High accuracy can be obtained at higher frequencies using adequate frequency-dependent correction factors. Appendix A gives a summary of the formulae used by the router for the initial sizing of all interconnect dimensions.

Power losses in microstrip lines are related to the the following causes: conductor losses, dissipations in the substrate, radiation and surface-wave propagation. At the frequency of interest ( $f < 40$  GHz) and for the materials used in our implementations, radiation and surface-wave propagation effects have been neglected [12]. However surface-wave propagation could be easily be modeled using the closed forms reported in [13]. Closed form expressions for conductor losses  $\alpha_c$  and  $\alpha_d$  substrate losses exist for microstrip lines and are reported by a number of authors [10, 11]. A summary of the formulae used in our approach for estimating the loss of microstrip lines is in Appendix A.

## 2.2 Modeling Coupled Microstrip Lines

Coupled microstrip lines are used in a variety of applications, namely directional couplers, filters and impedance matching networks [14]. From elemental symmetric coupler analysis, it is known that even and odd modes of propagation can be described by the odd and even mode characteristic impedances  $Z_{oo}$  and  $Z_{eo}$ . Even and odd characteristic impedances are obtained from the following equalities

$$Z_{oe} = \sqrt{\frac{L_e}{C_e}} = \frac{\sqrt{\epsilon_{eff-e}}}{c C_e}, \quad Z_{oo} = \sqrt{\frac{L_o}{C_o}} = \frac{\sqrt{\epsilon_{eff-o}}}{c C_o},$$

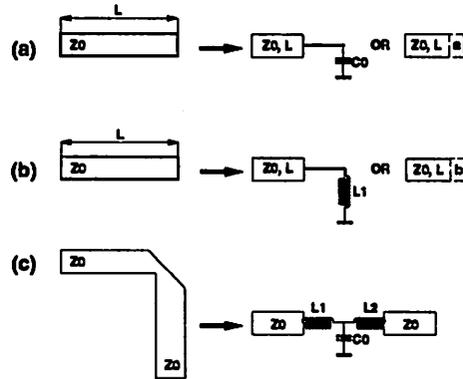


Figure 4: Typical Discontinuities in RF and microwave circuits.

where  $C_e(C_o)$  and  $L_e(L_o)$  are the even (odd) capacitances and self inductances of the lines,  $\epsilon_{eff-e}$  ( $\epsilon_{eff-o}$ ) is the even (odd) permittivity of the substrate and  $c$  is the wave velocity in empty space. Semi-empirical expressions for  $C_e$  and  $C_o$  are given in Appendix A. Alternatively, analytical expressions for crosscoupling and substrate capacitances can also be obtained. In our implementation these expressions have been preferred for their simplicity and relatively high accuracy (See Appendix A).

### 2.3 Modeling Microstrip Discontinuities

The following discontinuities are generally present in microwave circuits: (a) open circuits, (b) short circuits, (c) right-angled jogs or bends, (d) gaps, (e) steps, (f) transverse slits, (g) T-junctions, and (h) cross-junctions. For the purposes of this work we consider open, short circuits and bends, while T-junctions can be easily included in the analysis. The remaining discontinuities are not of concern during the routing phase.

Discontinuities can be modeled with an equivalent circuit of discrete components (Figure 4). These models can be used to generate constraints on the physical dimensions of the discontinuity. Notice that configurations (a) and (b) can be also represented as transmission lines with length augmented by a factor  $(a,b)$ . Appendix B summarizes the parameters as implemented in the cost function of the router.

### 2.4 Modeling 3-D Discontinuities

The presence of 3-D objects in the neighborhood of an interconnect line causes inductive and/or capacitive coupling. The patterns of the field lines are generally very complex, and can be accurately simulated through 3-D numerical analysis. Analytical models have been derived from the simulation data based on the knowledge of the physics underlying the effect as in [15]. A 3-D field solver has been

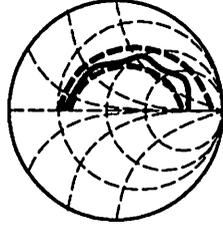


Figure 5: Specification of a RF and microwave circuit.

used to perform extensive simulations of 3-D structures frequently encountered in layout synthesis. Analytical models have been created based on these data by fitting a polynomial function onto them. Appendix C summarizes the models used in our approach.

### 3 Constraint Generation

#### Parasitic Constraints

Due to the distributed nature of parasitics in microwave circuits, the constraint generation techniques outlined in [9] are not applicable directly. Furthermore, because of the more complex nature of performance, a new definition of specification is needed. For a given a performance  $W_i$ , let us define *performance specification* the set of inequalities which determine lower- and upper-bounds for  $W_i$  and the range of frequencies for which they are valid. For example, consider the input reflection coefficient  $S_{11}$  illustrated in Figure 5. The solid line represents the actual value of  $S_{11}$  obtained from the complete layout after extraction and the dotted lines are the frequency dependent specifications to performance  $S_{11}$  explicitly expressed by Equation (1).

$$\begin{aligned}
|L_0| \leq |S_{11}| \leq |U_0|, \quad \angle L_0 \leq \angle S_{11} \leq \angle U_0, \quad \text{for } f_0 - \Delta f_0 \leq f \leq f_0 + \Delta f_0 \\
|L_1| \leq |S_{11}| \leq |U_1|, \quad \angle L_1 \leq \angle S_{11} \leq \angle U_1, \quad \text{for } f_1 - \Delta f_1 \leq f \leq f_1 + \Delta f_1 \\
\vdots \\
|L_n| \leq |S_{11}| \leq |U_n|, \quad \angle L_n \leq \angle S_{11} \leq \angle U_n, \quad \text{for } f_n - \Delta f_n \leq f \leq f_n + \Delta f_n.
\end{aligned} \tag{1}$$

In general, for a set of performances  $\{W_i\}$ ,  $i = 1, \dots, N_w$  and a set of parasitics  $\{p_j\}$ ,  $j = 1, \dots, N_p$ , *parasitic constraint generation* is defined as the process of creating a inequality constraint on a subset of  $\{p_j\}$ :

$$p_j \leq p_j^{(bound)},$$

to guarantee the fulfillment of all performance constraints in the entire frequency range.

$$\Delta W_i(f) \leq \overline{\Delta W_i(f)}, \quad \forall i = 1, \dots, N_w, \forall f \in [f_{min}, f_{max}],$$

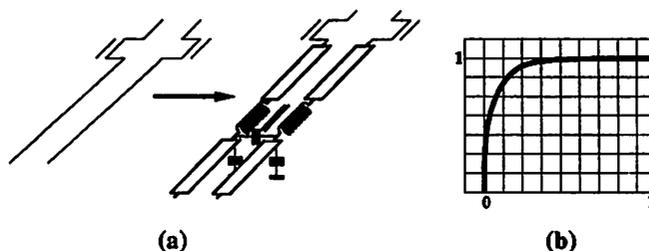


Figure 6: Interconnect model for sensitivity calculation and objective of constrained optimization.

where  $\Delta W_i(f)$  represents the total and  $\overline{\Delta W_i(f)}$  the maximum allowed degradation of performance  $W_i$  with respect to all parasitics within the entire range of operation. Parasitics such as cross-couplings, characteristic impedance deviation, losses and microstrip line length tolerances are constrained in this fashion. Also constraints on parasitics related to short and open microstrip terminations can be derived from the above constraints as described in Section 2.

Assuming that performance is linear near its nominal value at all frequencies, it can be represented as a linear combination of its sensitivity with respect to all distributed parasitics at all frequencies. Since parasitics can contribute constructively as well as destructively to performance, positive and negative sensitivities must be considered separately for constraint computation. Using the notation of [9], positive and negative components of the performance degradation  $\Delta W_i^+$  and  $\Delta W_i^-$  with respect to all parasitics belonging to the set  $\{p_j\}$  is, in first approximation

$$\Delta W_i(f)^+ = \sum_j S_j^i(f)^+ p_j, \quad \Delta W_i(f)^- = \sum_j S_j^i(f)^- p_j \quad (2)$$

Technology-related process variations can be taken into account by simply replacing nominal values of sensitivities with worst-case values as suggested in [9] or by finding bounds on parasitic and device mismatches as proposed in [16].

The bounds on the distributed parasitics are calculated by using constrained optimization, the objective being the maximization of the flexibility of the layout generation process. To insure that all relevant parasitics are considered during the optimization, each interconnect line to be implemented in the circuit is modeled as a microstrip line with inductive and capacitive coupling with all the other nets. Figure 6(a) shows a pair of interconnect lines and devices and the corresponding model. The objective function of the optimizer is a polynomial of second order monotonic in the range from zero to one as shown in Figure 6(b). Bounds on critical parasitics are made as large as possible, while at the same time tightening unnecessarily loose bounds on uncritical parasitics.

The circuit schematic is augmented using this model and the sensitivities of performance with respect to all parasitic components are computed using `SENSCALC-MW` and the simulator `MNS` [7]. Using the knowledge of the range within the parasitic can vary, all parasitics, whose cumula-

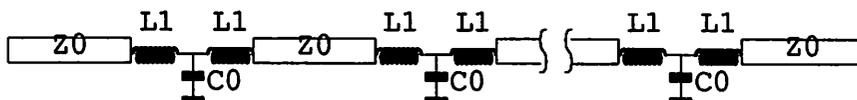


Figure 7: Interconnect model for microstripline with multiple bends.

tive contribution to performance degradation is negligible are discarded. Hence bounds on critical parasitics are computed using the program PARCAR [9].

### Constraints on Interconnect Length

RF and microwave circuits rely for functionality on transmission lines with a specific length. However tolerances from the nominal value of the length are possible. Hence the length  $\ell_j$  of microstrip line  $j$  is constrained by three equations

$$\begin{aligned} \ell_j &= L_j, \\ \Delta \ell_j^+ &\leq \Delta L_j^+, \\ \Delta \ell_j^- &\leq \Delta L_j^-, \end{aligned}$$

where  $L_j$  is the nominal length and  $\Delta L_j^{+/-}$  are maximum allowed positive and negative deviations from nominal. While  $L_j$  is determined by design, constraints  $\Delta L_j^{+/-}$  must be computed numerically. Using MNS the sensitivity of each performance with respect to length variations can be quantified, thus, using constrained optimization, constraints on the tolerances are calculated.

### Constraints on Interconnect Realization

Parasitics involving the detailed realization of interconnect such as bends, gaps and steps need be considered in a somewhat different way. A bended interconnect realization is shown in Figure 7, where the bends have been replaced with the appropriate models of Section 2. Consider the problem of finding a constraint on the number of bends in the microstrip line. Suppose the microstrip line is partitioned into  $N$  segments of length  $L/N$  each, where  $L$  is the nominal length of the microstrip. Let us model  $N - 1$  bends as in Figure 7. Due to the repetitive character of the model, performance sensitivities with respect to the discrete components  $S_{L/C}^W$  of each bend are necessarily equal. Therefore the cumulative effect of  $N$  bends on performance  $W$  is

$$\Delta W = \sum_{i=1}^{N-1} (S_{L_1}^W L_1 + S_{C_0}^W C_0) = (N - 1)(S_{L_1}^W L_1 + S_{C_0}^W C_0)$$

Consequently only one  $(L_1, C_0)$  pair need be considered during the optimization. After the optimization two scenarios are possible:

(a) parasitics are not critical and therefore they have been eliminated. In this case, given the maximum and minimum values for  $C_0$  and  $L_1$ ,  $N^{(bound)}$  can be computed as following

$$N^{(bound)} = 1 + \min\{[C_0^{(max)}/C_0^{(min)}], [L_1^{(max)}/L_1^{(min)}]\}$$

Note that if  $C_0^{(min)} = 0$  and  $L_1^{(min)} = 0$ , the constraint on  $N$  is  $\infty$ , thus it can be neglected.

(b) parasitics are critical and bounded. In this case  $N^{(bound)}$  can be obtained by replacing the maximum value of  $C_0$  and  $L_1$  with its bound.

$$N^{(bound)} = 1 + \min\{\lfloor C_0^{(bound)}/C_0^{(min)} \rfloor, \lfloor L_1^{(bound)}/L_1^{(min)} \rfloor\}$$

Violations to this constraints are included in the cost function of the router and are checked during the refinement phase.

## 4 Routing

Equality constraints cannot be handled efficiently by a maze router via a cost function, due to the instability they induce in the algorithm [17, Chp.3]. Consequently, two phases must be implemented. During the first phase, called *constructive phase*, all inequality constraints, i.e. constraints related to interconnect parasitics, are enforced. The second phase or *refinement*, enforces all equality constraints while no new parasitic violations are introduced. Both phases have been implemented in a tool called CORAL .

### Constructive Phase

The first phase of the routing scheme consists of a maze router based on the A\* algorithm [17, Chp.3], [18] which uses a “depth-first” approach. The A\* algorithm is based on a heuristic estimation of the cost of a path connecting the propagation node on the grid and a terminal target. In CORAL the cost estimate is given by the Manhattan distance between the nodes. Such heuristic is always optimistic with respect to the real path length, therefore the algorithm is *admissible* [17, Ch.3]. An optimal path for a net  $j$  is defined as the path minimizing a cost function  $f(x)$ .

$$f(x) = \ell(x) \left( 1 + K_c(x) + w_j^R \frac{Viol[R_j(x)]}{R^0} + w_j^C \frac{Viol[C_j(x)]}{C^0} + \frac{1}{C^0} \sum_{jk} w_{jk}^C Viol[C_{jk}(x)] + w_j^Z \frac{Viol[Z_j(x)]}{Z^0} \right), \quad (3)$$

where

$\ell(x)$  = estimated interconnect length of net  $j$

$K_c(x)$  = measure for local congestion at  $x$

$R_j(x)$  = integral of the estimated transmission line loss of net  $j$  at  $x$

$C_j(x)$  = integral of the estimated substrate capacitance of net  $j$  at  $x$

$C_{jk}(x)$  = integral of the estimated cross-capacitance between nets  $j$  and  $k$  at  $x$

$Z_j(x)$  = local estimated deviation of characteristic impedance from nominal for net  $j$  at  $x$

$Viol[m]$  =  $m$  if  $m > 0$ , otherwise it is zero

$R^0$ ,  $C^0$  and  $Z^0$  = normalization factors

$w_j^R$ ,  $w_j^C$ ,  $w_{jk}^C$  and  $w_j^Z$  = weights (see description in text)

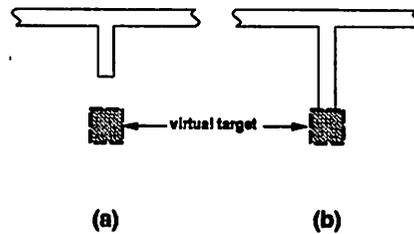


Figure 8: Constructive stub generation.

The algorithm minimizes the estimated interconnect length  $\ell$  at each location  $x$ . At this point the constraint on the length  $\ell$  is not enforced. All Parasitics are estimated using the approximations of section 2.

Weights  $w_j^R$ ,  $w_j^C$ ,  $w_{jk}^C$  and  $w_j^Z$  are calculated based on the relative sensitivity of performance with respect to each parasitic element as

$$w_j = w_0 \sum_{i,j} \left( \frac{S_j^i(f)^-}{\overline{\Delta W_i(f)^-}} + \frac{S_j^i(f)^+}{\overline{\Delta W_i(f)^+}} \right)$$

where  $\overline{\Delta W_i(f)^{+/-}}$  represents the specification of performance  $W_i$  at frequency  $f$  and  $S_j^i(f)^{+/-}$  its sensitivity with respect to parasitic  $j$ .  $w_0$  is a normalization factor, such that if sensitivities are not all zero, at least one weight is set to one and all the others are in the interval from zero to one. With this definition the items in Equation (3) can be seen as an approximation to the actual violation of parasitic constraints. If, at the end of the refinement phase, performance specifications are not met the weights of parasitics responsible for the violations will be modified [19].

Interconnect length  $\ell$ , obtained at the end of the constructive phase cannot be further reduced except; in some cases, by using a reroute/rip-up scheme. Hence, the algorithm stops if loss and substrate capacitance violations occur or if the maximum transmission line length  $L$  is reached. If at the end of the routing all violations vanish, then it is guaranteed that net  $j$  satisfies all inequality constraints. It is the task of the refinement phase to enforce the remaining constraints, including the transmission line length  $L$ .

The synthesis of open circuit stubs requires generation of dummy targets to be used by the algorithm in order to set a propagation direction. The dummy target is placed at a distance smaller than the nominal stub length, in an area where no constraint violations occur (Figure 8 (a)). The algorithm implements the interconnect line so as to minimize length (Figure 8 (b)). The refinement phase will enforce the obtained length to the nominal value. The routing order of the nets is determined automatically giving priority to the wiring of stubs and of nets on which parasitic constraints are tightest. This is done to not compromise the ability of the router to meet all parasitic constraints by routing first non critical nets.

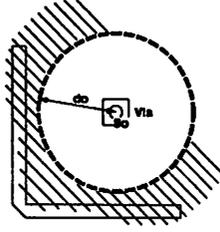


Figure 9: Feasibility polytope around a via.

### Refinement Phase

This phase is responsible for the enforcement of all equality constraints while insuring that no additional violation be introduced in the layout. Refinement is only applied to the set of all nets for which at least a violation exists, call  $C$  such set. Consider the constraint for the transmission line length of net  $j$ ,  $L_j$ . Since previously obtained line length is guaranteed to be smaller than the constraint, the interconnect line needs be expanded. However the expansion must occur inside a space where no constraint violations are possible. We call this space *feasibility polytope* of net  $j$ , or  $\mathcal{F}_j$ .  $\mathcal{F}_j$  is defined as the intersection of all two-dimensional spaces  $\mathcal{B}_j(p_k)$ , for which parasitic  $p_k$  associated with net  $j$  does not exceed its predefined constraint.

Assume that each parasitic can be expressed in form of a  $n^{\text{th}}$  order polynomial  $\mathcal{P}_n(\mathbf{x}, \mathbf{s}, \mathbf{V})$ , where  $\mathbf{x}$  is the location of a point in the interconnect and  $\mathbf{s}$  is the position of any objects responsible for  $p_k$ .  $\mathbf{V}$  is the vector of all known design parameters (interconnect width, via size, etc.). Then, the location of  $\mathcal{B}_j(p_k)$ 's boundaries is the locus of all  $\mathbf{x}$  that solve

$$\mathcal{P}_n(\mathbf{x}, \mathbf{s}_0, \mathbf{V}) - p_k^{(\text{bound})} = 0, \quad (4)$$

for given object position  $\mathbf{s}_0$  and parameter  $\mathbf{V}$ . As illustration consider the effect of a via structure on the characteristic impedance of a microstrip line. Given the width of both objects, the thickness of conductors and substrate, a model for the deviation of microstrip impedance  $\Delta Z_o$  is derived (section 2). The resulting space  $\mathcal{B}(\Delta Z_o)$  is a two-dimensional sphere centered in  $\mathbf{s}_0$  with radius  $d_0$ , where  $d_0$  is computed solving Equation (4) for a given constraint  $\Delta Z_o^{(\text{bound})}$ . Hence any implementations of the microstrip outside this space will satisfy the constraint, as shown in Figure 9.

Given  $P_j$ , the set of all constrained parasitics relevant to net  $j$ ,  $\mathcal{F}_j$  is computed as

$$\mathcal{F}_j = \bigcap_{p_k \in P_j} \mathcal{B}_j(p_k).$$

The boundaries of polytope  $\mathcal{F}_j$  are often a complex function of relative position and size of the surrounding layout objects and by the constraint imposed on each parasitic  $p_k$  as shown in Figure 10 (a) (dotted lines).

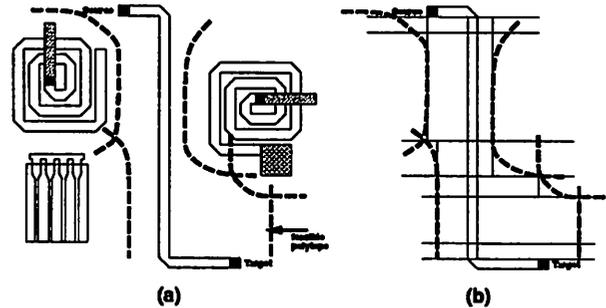


Figure 10: Distributed parasitics acting on the interconnect determine the feasibility polytope.

The task of the refinement algorithm is to find a interconnect implementation which satisfies the following requirements

1. the implementation should be within the feasibility polytope
2. the number of bends should be within constraint  $N^{(bound)}$
3. the length  $\ell$  should be within allowed tolerances from the nominal value

If the initial number of bends  $b$  exceeds the maximum allocated number the refinement phase terminates. If, on the other hand,  $n = N^{(bound)} - b \geq 4$ , then the expansion algorithm is applied. Since only Manhattan expansion is allowed, the polytope of each net is horizontally sliced in correspondence of each vertex as shown in Figure 10 (b). Two additional slices are added at a standard distance from source and target, corresponding to the minimum distance between bends. Between each pair of horizontal cuts a rectangle is built of width equal to the minimum polytope diameter between the cuts. Call  $R$  the set of all the rectangles non-adjacent to source and target obtained in this fashion. Since it is preferable to expand interconnect as uniformly as possible in order to keep it at the center of the polytope, the maximum possible number of rectangles  $r$  is selected for expansion, where  $r = \lfloor \frac{n}{4} \rfloor$ . This ensures that the minimum possible horizontal expansion is performed, thus maintaining the distance between interconnect and polytope boundary highest. The interconnect can be expanded in two opposite directions in two adjacent rectangles to maximize the length increase  $\Delta\ell$ , or in two equal direction to minimize the number of bends.

Hence, there exist a large number of combinations of choices of expansion rectangles to obtain the desired expansion. The problem can be formulated as follows:

*Find  $\bar{R}$ , a subset of  $R$ , such that the total expansion  $\Delta\ell$  is maximized subject to the constraint on number of bends.*

This problem can be solved using exhaustive enumeration techniques or linear programming. Due to the low number of vertices per polytope, in CORAL the former solution has been adopted.

An expansion step  $e = \min_{j \in C} \Delta \ell_j / K$  is selected, where  $K$  is a constant proportional to the worst-case number of expansion steps of the algorithm. For each net  $j$  the set of all expansion rectangles  $\bar{R}_j$  is

```

refinement(layout) {
  set_initial_expansion_step;
  set_initial_expansion_direction;
  set_constrained_nets;
  until (all constraints met OR infeasibility) {
    compute_polytope_boundary;
    identify_expansion_rectangles;
    if (max_expansion < required_expansion) exit;
    expand_segments;
    update_polytopes;
    if (check_feasibility == NOT_OK) exit;
    update_constrained_nets;
    update_expansion_step;
  }
}

```

Figure 11: Refinement algorithm in CORAL .

calculated and each net is expanded by  $e$ . The expansion is continued until either a net  $j$  reaches its nominal length  $L_j$  or a the location of a polytope vertex changes. If the first event occurs, net  $j$  is dropped from  $C$ ,  $e$  is recalculated and the expansion continues. If, on the other hand the second event occurs,  $\bar{R}_j$  is recomputed for all nets in  $C$  and the expansion proceeds. If a wire crosses the polytope associated with its net, then the algorithm exits.

The refinement algorithm is summarized in Figure 11. If the algorithm exits with infeasibility, the partially expanded layout is analyzed for performance violations, a new set of weights is generated and the routing is repeated.

## Performance Verification and Weight Modification

The verification step is the last phase of the routing scheme. Deviations from the nominal value of performance are computed using the linearized performance model of Equation (2) and estimations of layout parasitics from the models of section 2. The effects of vias, FET's and other transmission lines are represented in terms of analytical correction factors of the nominal value of the characteristic impedance of the microstrip. Capacitive/inductive coupling between microstrips are represented in a similar way, where the effects of all relevant structures are accounted for by means of correction factors. Microstrip discontinuities are represented based on the equivalent two-port model proposed for example by [20]. Special discontinuities can be ignored if known design procedures are adopted [14, page 259].

After all relevant parasitic components are identified and quantified, Equations (2) are used

Parasitic	parameter	type of model	generation time (sec)
single models			
substrate cap.	$C_1$	1st ord. polynomial	414.8
cross-over cap.	$C_{12}$	2nd ord. polynomial	6281.7
parallel line cap.	$C_{12}$	2nd ord. polynomial	1888.3
char. impedance	$Z_w$	logarithmic	-
bend	$C, L_1, L_2$	lumped passive	-
via hole	$L_1$	1st ord. polynomial	2401.0 (HP9000/750)
correction factors			
adjacent line	$\Delta C_1$	2nd ord. polynomial	3040.9
adjacent pad/spiral	$\Delta Z_w$	2nd ord. polynomial	2543.7
adjacent via	$\Delta Z_w$	2nd ord. polynomial	36 hrs (HP9000/750)

Table 1: Analytical model for a number of parasitic effects encountered in the circuits.

to verify that all performances be within specifications. If a performance specification has not been satisfied, at least one parasitic constraint violation must exist. All parasitics responsible for the violation can be easily identified, thus the set of weights associated with these parasitics can be modified so as to insure that a new routing attempt with a modified cost function will reach a satisfactory solution. A possible weight modification scheme could be to decrease the weights associated with parasitics within constraints while increasing those of parasitics found to be violating constraints. However this strategy might cause indefinite weight oscillation, thus severely degrading the convergence properties of the algorithm.

An alternative is to allow only an increase in the value of the weights. In addition, only weights associated with violations should be modified. In our approach, weights are increased by an amount  $\Delta w_j$ , inversely proportional to the entity of the violation that the corresponding parasitics induced [19]

$$\Delta w_j = \frac{1 - w_j}{m_0} \sum_{i,f} \left( \frac{S_j^i(f)^-}{\Delta W_i(f)^- - \Delta W_i(f)^-} + \frac{S_j^i(f)^+}{\Delta W_i(f)^+ - \Delta W_i(f)^+} \right)$$

where  $m_0$  is a normalization factor so that the maximum of the increased weights is one and all the others are within zero and one.

## 5 Results

The routing methodology described in this paper has been applied to a number of benchmark circuits. In this section two examples are discussed in detail. First, a number of analytical models for MMIC microstrip lines has been computed for the GaAs technology on which the chips were designed. Table 1 shows a summary of the models, along with the CPU time required for their generation on a DECstation 5000/240. Consider first the traveling wave amplifier (TWA) shown in Figure 12. The specifications are listed in Table 2. The calculation of sensitivities using SENSALC-

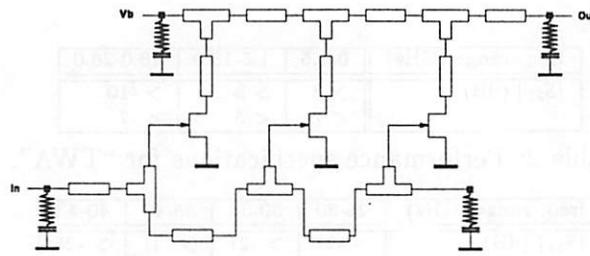


Figure 12: Schematic of "TWA".

MW and of all critical parasitics using PARCAR required 31 seconds and 351 seconds respectively on a DECstation 5000/240. The obtained bounds were used by CORAL to route the circuit in 53 seconds on a DECstation 5000/240. The resulting layout is in Figure 13 and the performance

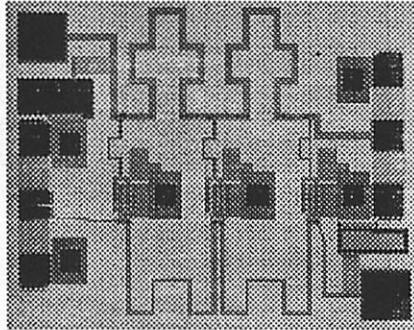


Figure 13: Final layout of "TWA".

evaluation is in Table 4. All performance specifications were met.

Next, consider the three-stage amplifier shown in Figure 14. The specifications are illustrated in

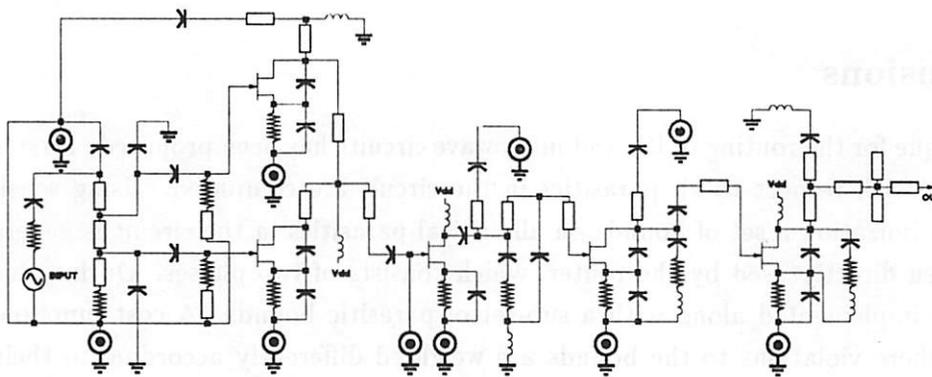


Figure 14: Schematic of "pcn38".

freq. range (GHz)	0-1.5	1.5-18.0	18.0-26.0
$ S_{21} $ (dB)	> 3 < 7	> 3 < 5	> -10 < -7

Table 2: Performance specifications for "TWA".

freq. range (GHz)	25-30	30-35	35-40	40-43
$ S_{11} $ (dB)	> -21 < -12	> -21 < -15	> -21 < -15	> -25 < -16
$ S_{22} $ (dB)	> -15 < -8	> -15 < -8	> -15 < -8	> -15 < -8
$ S_{21} $ (dB)	> 22 < 30	> 22 < 25	> 22 < 25	> 22 < 25

Table 3: Performance specifications for "pcn38".

freq. range (GHz)	1.5	18.0	26.0
$ S_{21} $ (dB)	6.28	4.30	-8.21

Table 4: Estimated performance of circuit "TWA" after layout completion.

freq. range (GHz)	25-30	30-35	35-40	40-43
$ S_{11} $ (dB)	-15.15	-20.03	-15.54	-20.12
$ S_{22} $ (dB)	-8.78	-11.43	-13.41	-8.76
$ S_{21} $ (dB)	22.54	23.21	23.57	22.53

Table 5: Estimated performance of circuit "pcn38" after layout completion.

Table 3. All relevant parasitic constraints were generated in a total CPU time of 2454 sec on a DECstation 5000/240. The computed bounds have then been used by CORAL to route the pre-placed circuit, the resulting layout is shown in Figure 15 and the extracted deviations from nominal performance are listed in Table 5. The CPU time for the routing phase was 348 sec on a DECstation 5000/240. As expected, all performance specifications were met. Figure 16 shows the simulation results of  $|S_{11}|$ ,  $|S_{22}|$  and  $|S_{21}|$  respectively.

## 6 Conclusions

A novel technique for the routing of RF and microwave circuits has been proposed. First, sensitivities of performance with respect to all parasitics in the circuit are computed. Using sensitivities and constrained optimization a set of bounds on all critical parasitics in the circuit is generated. These bounds are then directly used by the router, which consists of two phases. During the first phase connectivity is implemented along with a sub-set of parasitic bounds. A cost function drives this routing step where violations to the bounds are weighted differently according to their criticality. During the second phase a refinement is performed on all nets simultaneously so as to enforce all remaining constraints. A final verification is performed on the layout to insure that all performance

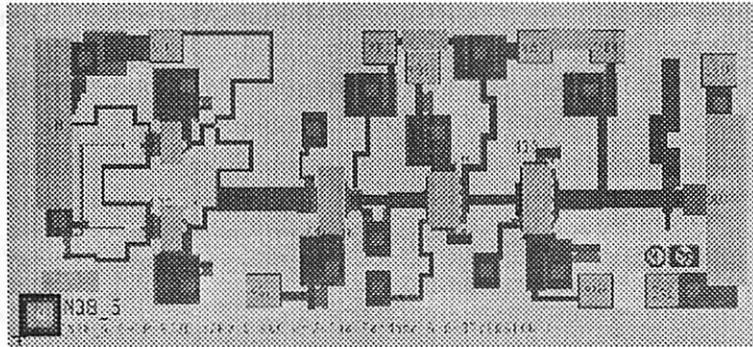


Figure 15: Final layout of "pcn38".

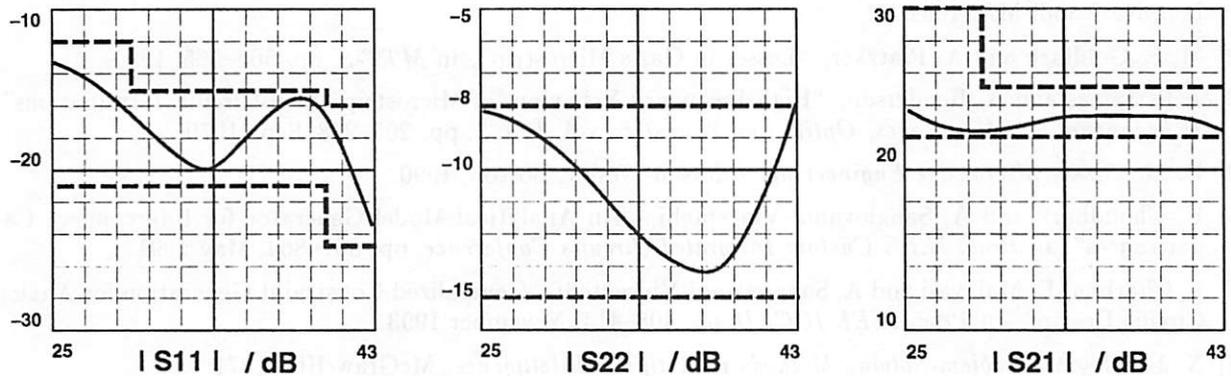


Figure 16: Performance of "pcn38".

specifications be met. In case one or more violations are detected the weighting of violations in the cost is modified based on the severity of the violations and a new routing is performed. The cycle concludes when all violations have been eliminated or when the maximum number of iterations is reached.

## References

- [1] R. H. Jansen, R. G. Aronold and I. G. Eddison, "A Comprehensive CAD Approach to Design of MMICs up to MM-Wave Frequencies", *MTT-T*, vol. 36, n. 2, pp. 208–219, February 1988.
- [2] W. L. Williams R. C. Compton and B. Rutledge, "Puff, an interactive Microwave Computer Aided Design Program for Personal Computers", in *MTT-S*, pp. 707–708, 1987.
- [3] A. E. Ruehli, "Survey of Computer-Aided Electrical Analysis of Integrated Circuit Interconnections", *IBM Journal of Research and Development*, vol. 23, n. 6, pp. 626–639, November 1979.
- [4] K. Nabors and J. White, "A Fast Multipole Algorithm for Capacitance Extraction of Complex 3-D Geometries", in *Proc. IEEE Custom Integrated Circuits Conference*, May 1989.

- [5] M. Kamon, M. T. Tsuk and J. White, "FastHenry: A Multiple-Accelerated 3-D Inductance Extraction Program", in *Proc. Design Automation Conference*, pp. 678-683, June 1993.
- [6] R. H. Jansen, "LINMIC: A CAD Package for the Layout-Oriented Design of Single- and Multi-Layer MICs/MMICs up to mm-Wave Frequencies", *"Microwave Journal"*, pp. 151-161, February 1986.
- [7] Hewlett-Packard Microwave and RF Design System, *Manuals*, Santa Rosa Systems Division, Santa Rosa, CA, December 1992.
- [8] J. F. Zürcher, "MICROS - A CAD/CAM Program for Fast Realization of Microstrip Masks", in *MTT-S*, pp. 481-484, 1985.
- [9] U. Choudhury and A. Sangiovanni-Vincentelli, "Constraint Generation for Routing Analog Circuits", in *Proc. Design Automation Conference*, pp. 561-566, June 1990.
- [10] T. Edwards, *Foundations for Microstrip Circuit Design*, Wiley, West Sussex, UK, 2nd Ed. 1992.
- [11] K. C. Gupta, R. Garg and R. Chadha, *Computer Aided Design of Microwave Circuits*, Artech House Inc., Norwood, MA, 1981.
- [12] M. E. Goldfarb and A. Platzker, "Losses in GaAs Microstrip", in *MTT-S*, pp. 563-565, 1990.
- [13] J. R. James and A. Henderson, "High-Frequency Behaviour of Microstrip Open-Circuit Terminations", *IEE Journal on Microwaves, Optics and Acoustics*, vol. 3, n. 5, pp. 205-218, Sept 1979.
- [14] D. M. Pozar, *Microwave Engineering*, Addison-Wesley, Boston, 1990.
- [15] U. Choudhury and A. Sangiovanni-Vincentelli, "An Analytical-Model Generator for Interconnect Capacitances", in *Proc. IEEE Custom Integrated Circuits Conference*, pp. 861-864, May 1991.
- [16] E. Charbon, E. Malavasi and A. Sangiovanni-Vincentelli, "Generalized Constraint Generation for Analog Circuit Design", in *Proc. IEEE ICCAD*, pp. 408-414, November 1993.
- [17] N. J. Nilsson, *Problem-Solving Methods in Artificial Intelligence*, McGraw-Hill, 1971.
- [18] G. W. Clow, "A Global Routing Algorithm for General Cells", in *Proc. Design Automation Conference*, pp. 45-51, 1984.
- [19] E. Malavasi, U. Choudhury and A. Sangiovanni-Vincentelli, "A Routing Methodology for Analog Integrated Circuits", in *Proc. IEEE ICCAD*, pp. 202-205, November 1990.
- [20] M. Thorburn A. Weisshaar, S. Luo and V. K. Tripathi, "Modeling of Radial Microstrip Bends", in *MTT-S*, pp. 1051-1054, 1990.
- [21] M. V. Schneider, "Microstrip Lines for Microwave Integrated Circuits", *Bell Syst. Tech. Journal*, vol. 48, pp. 1421-1444, May/June 1969.
- [22] M. V. Getsinger, "Microstrip Dispersion Model", *MTT-T*, vol. 21, n. 1, pp. 34-39, Jan 1973.
- [23] S. Ramo, J. R. Whinnery and T. Van Duzer, *Fields and Waves in Communication Electronics*, Prentice-Hall, Englewood Cliffs, N.J., 1984.
- [24] HFSS, *Manuals*, Santa Rosa Systems Division, Santa Rosa, CA, 1990.

## Appendix A: Closed Form Expressions for Microstrip Lines

For a uniform, isotropic, non-magnetic substrate with permittivity  $\epsilon_r$ , the characteristic impedance of the microstrip line of Figure 2, the characteristic impedance  $Z_o$  is computed as follows [21, 22]

$$Z_o = \frac{\eta}{2\pi\sqrt{\epsilon_{re}}} \ln\left(\frac{8h}{w_e} + \frac{w_e}{4h}\right), \quad w/h \leq 1$$

$$Z_o = \frac{\eta}{\sqrt{\epsilon_{re}}} \left[\frac{w_e}{h} + 1.393 + \frac{2}{3} \ln\left(\frac{w_e}{h} + \frac{13}{9}\right)\right]^{-1}, \quad w/h \geq 1$$

where  $\eta = 120\pi$ .  $\epsilon_{re}$  and  $\frac{w_e}{h}$  are computed as follows

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(1 + 10\frac{h}{w}\right)^{-\frac{1}{2}} - \frac{(\epsilon_r - 1)t/h}{4.6\sqrt{w/h}},$$

$$\frac{w_e}{h} = \frac{w}{h} + \frac{5t}{4\pi h} \left(1 + \ln\frac{4\pi w}{t}\right), \quad w/h \geq 1/2\pi$$

$$\frac{w_e}{h} = \frac{w}{h} + \frac{5t}{4\pi h} \left(1 + \ln\frac{2h}{t}\right), \quad w/h \leq 1/2\pi$$

where  $t$  is the conductor thickness. The loss  $\alpha$  is the sum of conductor loss  $\alpha_c$  and dielectric loss  $\alpha_d$ , with

$$\alpha_c = 1.38A \frac{R_s}{hZ_o} \frac{32 - (w_e/h)^2}{32 + (w_e/h)^2} \text{ dB/m}, \quad w/h \leq 1$$

$$\alpha_c = 6.1 \times 10^{-5} A \frac{R_s Z_o \epsilon_{re}}{h} \left(w_e/h + \frac{\frac{2}{3}w_e/h}{w_e/h + 13/9}\right) \text{ dB/m}, \quad w/h \geq 1,$$

where the surface resistance  $R_s$  is the DC conductor resistance at frequencies for which the penetration depth is comparable or greater than the thickness of the conductor [23, Chp.4.4]. This has always been the case in our MMIC benchmarks. Otherwise the formula  $R_s = \sqrt{\pi f \mu_o \rho}$  should be used.  $A$  is computed as follows.

$$A = 1 + \frac{h}{w_e} \left(1 + \frac{1}{\pi} \ln\frac{2h}{t}\right), \quad w/h \geq 1/2\pi,$$

$$A = 1 + \frac{h}{w_e} \left(1 + \frac{1}{\pi} \ln\frac{4\pi}{t}\right), \quad w/h \leq 1/2\pi.$$

The dielectric loss  $\alpha_d$  is computed as

$$\alpha_d = 27.3 \frac{\epsilon_r}{\epsilon_r - 1} \frac{\epsilon_{re} - 1}{\sqrt{\epsilon_{re}}} \frac{\tan\delta}{\lambda_0} \text{ dB/m},$$

where  $\tan\delta$  is the loss tangent of the dielectric and  $\lambda_0$  is the wavelength of the signal.

These models can be extended to higher frequencies by replacing the effective permittivity  $\epsilon_{re}$  by its frequency-dependent value

$$\epsilon_{re}(f) = \epsilon_r - \frac{\epsilon_r - \epsilon_{re}}{1 + G(f/f_p)^2},$$

where

$$f_p = \frac{Z_o}{2\mu_o h}.$$

An  $G$  is a material dependent linear function of  $Z_o$ .

For the coupled lines shown in Figure 3 the even and odd capacitances of Section 2 are estimated as follows [10]

$$C_e = C_p + C_f + C'_f, \quad C_o = C_p + C_f + C_{ga} + C_{gd},$$

where for  $0.2 \leq w/h \leq 2$ ,  $0.05 \leq s/h \leq 2$  and  $\epsilon_r \geq 1$

$$C_p = \epsilon_o \epsilon_r \frac{w}{h}, \quad 2C_f = \frac{\sqrt{\epsilon_{re}}}{c Z_o} - C_p,$$

[10] gives empirical expressions for  $C_f$ ,  $C_{ga}$  and  $C_{gd}$ .

Simpler analytical models can be found by using the solution of Laplace's equation in two dimensions to fit a simple function in the widths  $w_1$ ,  $w_2$  of the conductors and their spacing  $s$  [15]. Hence, substrate capacitance  $C_{0i}$ ,  $i = 1, 2$  and coupling capacitance  $C_{12}$  are computed as follows

$$C_{0i} = k_0 + k_1 w_i, \quad i = 1, 2, \quad C_{12} = \mathcal{P}(1/s) + \mathcal{P}(1/(s + w_1)) + \mathcal{P}(1/(s + w_2)),$$

where  $\mathcal{P}$  is a polynomial of second order and has been reported in [15]. The models account for the parallel plate and fringing component of the capacitance. Since some of the field is diverted from ground to the other plate, the substrate capacitances  $C_{0i}$ ,  $i = 1, 2$  need be corrected by the terms

$$C_{1c} = \mathcal{P}(1/(s + s_0)) + \mathcal{P}(1/(s + s_0 + w_2)), \quad C_{2c} = \mathcal{P}(1/(s + s_0)) + \mathcal{P}(1/(s + s_0 + w_1)),$$

where  $s_0$  is a constant and  $\mathcal{P}$  corresponds to the usual polynomial. These formulae have been used to obtain relatively accurate estimates of parasitic capacitances in CORAL.

## Appendix B: Microstrip Line Discontinuities

The discrete component realization of circuits depicted in Figure 4 are computed as follows [10].

(a)

$$C_0 = w \exp(2.2036 \sum_{i=1}^5 K_\epsilon \log(\frac{w}{h})^{i-1}) \text{ pF},$$

where the coefficients  $K_\epsilon$  are a monotonic function of  $\epsilon_r$ . The stripline augmentation  $L$  is approximated by the expression  $\frac{c Z_0 C_0}{\sqrt{\epsilon_r c}}$ ,  $c$  being the wave velocity in empty space.

(b)  $L_0$  is generally computed with *ad hoc* simulations of the via used in the layout. In our implementation results from simulations performed with the package HFSS [24] have been used.

(c)

$$\begin{aligned} C_0 &= w \frac{(14 \epsilon_r + 12.5)w/h - (1.83 \epsilon_r + 2.25)}{\sqrt{w/h}}, \quad w/h < 1 \text{ pF}, \\ C_0 &= w [(9.5 \epsilon_r + 1.25)w/h - (5.2 \epsilon_r + 7.0)] \text{ pF}, \\ L_1 &= 100 h [4\sqrt{w/h} - 4.21] \text{ nH}. \end{aligned}$$

## Appendix C: 3-D Discontinuities

Consider a microstrip line of width  $w$  in presence of a via structure located at a distance  $s$  and size  $w_2$ . The analytical model for the deviation  $\Delta Z_o$  from the nominal characteristic impedance  $Z_o$  is

$$\Delta Z_o = \frac{k_3}{s} + \frac{k_4}{s^2} + \frac{k_5}{s + w_2} + \frac{k_6}{(s + w_2)^2}.$$

The coefficients are obtained by fitting the model to the data from numerical simulations obtained through the package HFSS on a large number of geometries.

Models based on the same formula have been obtained for pairs of a transmission line and spiral interconnection and short circuit trough a via of the same type.