THE DESIGN OF A GaAs MESFET TEMPERATURE INDEPENDENT VOLTAGE REFERENCE CIRCUIT AND THE EVALUATION OF GaAs LARGE SIGNAL MESFET MODELS

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ABSTRACT

A number of large signal computer models for GaAs MESFETs have been implemented in the simulation program SPICE. The accuracy of these models has not been thoroughly investigated previously, and therefore an evaluation of these models was undertaken. A second study examined the effects of temperature on GaAs MESFETs. The effects are shown by plotting extracted SPICE parameters for two of the models over the test temperature range. The data provides new information for a proposed temperature independent voltage reference circuit that is designed and simulated using SPICE.

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I. INTRODUCTION

The development of GaAs MESFET technology has led to very high speed GaAs digital integrated circuits as well as GaAs monolithic microwave integrated circuits. To aid in the design of GaAs integrated circuits, high speed computers have been used for circuit simulation. At present, one such program is U. C. Berkeley's SPICE2[1]. SPICE2 was originally released to the public without a GaAs large signal MESFET model. In 1983, a GaAs MESFET model was introduced into SPICE2[2] and more recently two other models have been implemented. [3], [4]

In the first part of this report, the large signal SPICE models are evaluated and compared. In the course of the evaluation, some attention is given to the material properties of GaAs as well as to the GaAs MESFET device characteristics. It is shown that present models lack the sophistication necessary to model the GaAs MESFET with sufficient accuracy. Therefore, the circuit designer must be aware of these shortcomings for effective circuit simulation.

In the second part of this report, the results of a study to determine the temperature effects on GaAs MESFET devices are presented. Extensive measurements were made with MESFETs from several different manufacturers. The devices were measured at various temperatures, and the current-voltage data was recorded.

The SPICE large signal GaAs MESFET device parameters were extracted from

the recorded data for the Curtice and Statz models. The results are presented in plots showing SPICE parameters versus temperature. These temperature-dependent paramenters were then used in the design of a proposed temperature independent voltage reference circuit. The circuit has not been fabricated to date. Experimental results will be presented elsewhere when available.

II. BASIC MESFET PRINCIPLES

The development of a suitable MESFET model depends greatly upon the MESFET's physical structure, the electrical operation of the device, and on a knowledge of GaAs material properties. In this section, the material properties which make GaAs theoretically appealing are presented. The parasitic effects which hinder the MESFET's performance in practical designs will be discussed, and the MESFET's structure will be covered.

A. GaAs Material Properties

One of the most important and desirable characteristic of GaAs is that it has a higher electron transport mobility factor than silicon. With a doping level of $Nd=10^{17}cm^{-3}$, GaAs has a low field mobility of $4500cm^2/V\text{-}sec.$ and a peak electron saturation drift velocity of $2X10^7cm/sec.$ For comparison, silicon with a doping level of $Nd=10^{17}cm^{-3}$ has an electron mobility of $800cm^2/V\text{-}sec.$ and a peak drift velocity of $1X10^7cm/sec.$ (Figure 1).[5] The extremely high electron mobility and electron velocity permit GaAs devices to have wider bandwidth and faster switching capabilities than those of silicon.

Insight into the physics responsible for the greater speed in GaAs is gained by studying the energy momentum diagrams (Figure 2).[5] GaAs is a direct bandgap material while Si is an indirect bandgap material. Thus from the figure, GaAs requires 1.4eV of energy while silicon requires 1.1eV to promote an electron from

the valence band to the conduction band. However, GaAs requires no change in momentum for the promotion, whereas silicon has a 2.3eV gap at the zero momentum point. Promotion of electrons to a higher momentum state translates to a higher effective mass. The effective mass of electrons traveling through GaAs is $0.068M_o$, where M_o equals the free electron rest mass. This compares with an effective mass of $0.92M_o$ for silicon.

A second important distinction between silicon and GaAs is the unique semi-insulating GaAs substrate. GaAs substrates are made insulating by a complex compensation scheme. Generally, shallow donors in GaAs are compensated by deep acceptors, and shallow acceptors are compensated by deep donors. As an example of this compensation method, Si ions a shallow donors introduced during the cystal growth are compensated with intentionally added Cr deep acceptors. The semi-insulating GaAs is typically manufactured with an intrinsic resistivity of 10^8ohm-cm. The high resistivity results in the depletion of carriers in the substrate which reduces the interconnection capacitance to ground. Furthermore, advanced metallization schemes such as air-bridge metal are also commonly used to further reduce interconnect capacitance. The reduced capacitance is essential for high speed digital or high frequency analog integrated circuit applications.

B. MESFET Structure

Cross sections of two GaAs MESFETs are shown in Figures (3) and (4). The

first figure shows an ion implanted MESFET made with a fully planar process. Planar processed MESFETs are currently being investigated by many research laboratories, and it is anticipated that planar processed MESFETs will become the main device for GaAs digital ICs. A primany motivation for using planar processing is that no etching of the active layer is required, thus allowing the most dense packing of active devices. The second figure shows a mesa etched GaAs MESFET. This type of GaAs MESFET is presently the most widely used.

One unpleasant aspect of GaAs MESFETs in contrast to MOSFETs is that the gate is not insulated from the channel. Rather, the gate metal makes direct contact to the semiconductor over the channel region to form a Schottky diode. Attempts at finding a native oxide to insulate the gate of GaAs MESFETs have been unsuccessful. In silicon MOSFETs, a similar problem was overcome by using the native oxide SiO_2[6]. As will be discussed later, the Schottky diode at the MESFET's gate provides major new challenges for circuit designers to overcome since the gate conducts significant current when it is forward biased.

C. MESFET Parasitic Effects

Although GaAs material properties are potentially superior to silicon, the GaAs MESFET as manufactured with present techniques exhibits more device parasitic effects than the silicon MOSFET device. These effects make modeling and designing with MESFETs very difficult. Some important parasitic effects of the

MESFET are considered briefly in this section.

The most problematic and frequently noted parasitics[9] are the looping, kinking, and backgating effects. Although these effects are not well understood, the commonly cited causes of these problems are bad surface passivation and deep level traps in the semi-insulating substrate. Some of these problems will disappear as GaAs MESFET technology matures.

The looping effect shown in Figure (5) is generally observed in low frequency current-voltage characteristics. This effect exists in gated as well as in ungated MESFETs[7],[8]. For this reason, some researchers believe that deep level donors in the substrate below the channel are the cause of this problem. According to published reports, it appears that the looping effect is removed or suppressed greatly by adding a compensating buffer layer[7],[8]. The time constant associated with the looping effect ranges from 0.1Hz to 1KHz (Figure 6).[9]

The kink effect corresponds to the extra flow of source drain current above a certain kink threshold voltage (Figure 7). As of this writing, the cause of the kink is appearently still a mystery to device engineers developing gallium arsenide MESFETs.

Backgating and sidegating are parasitic effects that have received a considerable amount of attention. There are two types of backgating and sidegating. The first is a DC backgating due to the voltage potential of one node effecting another node. The depleted semi-insulating substrate acts as a very high

impedence, connecting one circuit node to another. In order to minimize the DC backgating effect, circuit designers place MESFET transistors far apart (~50 microns) in the circuit layout. The large distance between transistors eliminates the backgating effect, but at the same time significantly increases the interconnection capacitance, thus reducing the main benefit of having a semi-insulating GaAs substrate. The second type of backgating is an AC backgating effect due to electron traps in the substrate under the channel. The electron traps act as small capacitors which tend to cause coupling between transistors (Figure 33).

In digital GaAs ICs, backgating and sidegating effects will cause gates to switch state improperly resulting in logic error in the circuit. In analog applications, the backgating and sidegating problem will make commonly used differential circuit configurations used in silicon ICs difficult to achieve in GaAs ICs. Further investigation is necessary to determine how well the semi-insulating substrate isolates one device from another in a closely packed environment.

III. SPICE GaAs LARGE SIGNAL MESFET MODELS

A. Introduction to GaAs MESFET models

In 1974, Van Tuyl and Liechti[10] approximated the current voltage relationship of a MESFET by the equation:

$$Ids = \beta(Vgs + Vto)^2 (1 + \Omega Vds) \tanh(\phi Vds) \qquad (1.1)$$

This equation was incorporated into a large signal GaAs MESFET model developed at RCA laboratories by Curtice (Figure 8).[11] In 1984, Sussman-Fort[2] implemented this model in SPICE2. Note that this model is obviously assymmetric with respect to the source and drain which is a major limitation.

More recently U. C. Berkeley has developed SPICE3.[12] In this version of SPICE, a new MESFET model developed by Statz at Raytheon Labs (Figure 9)[3] was included. In this new model, the current voltage relationship is approximated by the equation:

$$Ids = \frac{\beta(Vgs + Vto)^2 (1 + \Omega Vds)}{1 + b(Vgs + Vto)} [1 - (1 - \phi Vds/3)^3] \qquad (1.2)$$

$$\text{for } 0 < Vds < 3/\phi$$

$$Ids = \frac{\beta(Vgs + Vto)^2 \ (1 + \Omega Vds)}{1 + b(Vgs + Vto)} \qquad \text{for } 0 > 3/\varnothing$$

In addition to the new voltage-controlled current equation, a capacitance model that also provides source-drain symmetry was introduced. This capacitance model is discussed later in the report.

During the evaluation of the Curtice and Statz GaAs large signal MESFET models mentioned in the previous paragraphs, a publication appeared[4] presenting a new GaAs large signal MESFET model for SPICE. This model has a current voltage relationship:

$$Ids = \beta(Vgs + Vto)^2 \ (1 + \Omega Vds) \ \tanh(\varnothing Vds) + Vds/Rsh \qquad (1.3)$$

$$\varnothing = \varnothing_o \ \beta(VBI + Vto)^2 \ \frac{1 - [(VBI - Vgs) / (VBI + Vto)]^{1/2}}{\beta(Vgs + Vto)^2}$$

$$Rsh = Rsho \ / \ 2[\exp(-Vto - Vgs/STF \ \frac{KT}{q}) + 1]$$

STF = empirical parameter similar to ideality factor

Although the McKinley MESFET model[4] was not investigated in this report as thoroughly as the Curtice or the Statz model, the McKinley model presents certain characteristics that the other two models have not incorporated. Some of the

differences in the McKinley voltage-controlled current equations appear to be a possible improvement to problems existing in the other two models. Reference will be made to the McKinley model when appropriate because of the possible improvement over the other two models.

B. SPICE Parameter Extraction Methods

The extraction of SPICE parameters from measured MESFET data is often a very difficult task. In this study only DC parameters were extracted from the device, as the proposed circuit is a DC voltage reference. The extraction methods utilized are explained more thoroughly in references [13] and [14].

The source resistance Rs was obtained by forcing current into the gate and out of the source node while measuring the voltage at the drain (Figures 10 and 11). An assumption is made that the voltage drop across the drain resistance is zero. Therfore, the relationship $Rs = Is/VD$ is valid. The drain resistance was measured by a similar method shown in Figures (12) and (13). Gate resistance Rg was measured by driving the gate node with a voltage source and concurrently measuring the current flowing in the drain and souce nodes (Figures 14 and 15).

The value of the gate Schottky diode saturation current parameter (Is) was measured by conventional means of extrapolating from $\ln(Ig)$ versus Vg with both source and drain nodes grounded. Finally, the parameters for the voltage-controlled current source, Equations (1.1) and (1.2), were found by using a fitting program

which minimizes the mean square error between the measured and calculated values from the Curtice and Statz models. The FORTRAN source code for the fitting program is provided in Appendix (1).

C. SPICE Parameters Extraction Results

The results show that the SPICE MESFET models are accurate only in a certain region of operation. The region is defined by a lower boundary of approximately 0.3 volts greater than the threshold voltage (V_{to}), and an upper boundary defined by a (V_{gs}) voltage that will maintain a low gate forward bias current. At the threshold of conduction and immediately after conduction begins, the current increases faster than the calculted current (Figure 18 and 19). This problem is more apparent in the enhancement MESFET because the device has a much higher leakage and subthreshold conduction current relative to the magnitude of Idss.

Secondly, the MESFET models fail to model the region where the current kinking effect occurs. In this region, the kink causes enormous error when trying to fit the measured curves to Equations (1.1) and (1.2). For this reason, the fitting was possible only up to V_{ds} = 3.0 volts where the kinking effect was not observed. The results of the curve fitting are shown in the Appendix (2).

The SPICE parameters were extracted from the recorded data in the region where the SPICE models were found to be consistent with measured devices (V_{ds} < 3.0V). Parameters were extracted over the temperature range of 25° to 100°C for

both the Statz model (Eq. 1.2) and for the Curtice model (Eq. 1.1). The extraction shows that the tranconductance term (ß) decreases with temperature. For a first order approximation, the transconductance term (ß) appears to obey the following equation:

$$\beta(T) = \beta_o(T_o / T)^n \quad \text{where } n \approx 1 \qquad (1.4)$$

The threshold voltage (V_{to}) of the device also decreases with temperature. A first order approximation of the threshold voltage (V_{to}) can be represented by a linearly decreasing voltage. The degradation rate for the enhancement MESFET devices was found to be -0.94mV/^{o}C. For the depletion MESFET devices, the degradation rate was found to be -0.83mV/^{o}C. The high Vgs degradation term (b) in the denominator of Eq. (1.2) was shown to be very small and of no significance in the region of fitting (Figures 20-23). Since the term (b) did not effect the region of the curve fit, it was found that the Statz model voltage-controlled current source degenerated to the form of the Curtice model. Furthermore, the Statz model voltage-controlled current source parameters converged to the Curtice model parameters.

D. SPICE Model Comparisions

The Curtice model shown in Figure (8) is not a symmetric MESFET model. In normal MESFETs, there exists a Schottky diode on the gate-to-drain side as well. Secondly, the Curtice model treats the gate source capacitance as a nonlinear

capacitance represented by the diode junction capacitance. This equation takes the form of:

$$C_{gs} = C_{gso} / (1 - V_{gs}/V_{BI})^{1/2} \qquad (1.5)$$

$$C_{gs} = C_{gso} \qquad \text{when } V_{gs} = 0$$

This model has been reported to be inaccurate[16] for modeling the MESFET capacitance. The actual Cgs capacitance has been shown to give the characteristic shown in Figure (24). The gate drain capacitance in the Curtice model is constant. This is incorrect since the gate drain capacitance is in reality a function of gate to drain voltage.

Equation (1.1) which represents the voltage-controlled current source in the Curtice model does not represent the current-voltage characteristic accurately in the region near turn-on, or in the subthreshold region. Figures (18) and (19) show the plots of the square root of Ids versus Vgs with a condition Vds = 1.2 volts applied to the drain. The curve generated by the MESFET model is straight and intersects at Vgs = Vto when Ids = 0mA. From measurements, the drain current does not follow the straight curve but begins to flatten out and eventually plateaus at the leakage current level. Another aspect of the equation which does not match measured results well is the small signal output conductance term. In Equation (1.1), the output conductance is obtained by differentiating the large signal

equations. The model assumes that tha output conductance value is the same for any frequency value. However, from measured results[15] this appears to be a bad approximation to the MESFET's actual output conductance (Figure 25). In the figure, output conductance was shown to decrease with frequency.

The more recently released GaAs MESFET model in SPICE3 is unfortunately similar to the Curtice model in many ways. The output conductance term in the Statz model (Eq. 1.2) is obtained by using exactly the same method as that used in the Curtice model. Therefore the Statz model has exactly the same problem as the Curtice model. Secondly, the problems with modeling the regions near turn-on and subthreshold exist in the Statz model exactly as explained in the Curtice model case.

There are new additions to the Statz model which address some of the problems of the Curtice model. The first improvement introduced by Statz was replacing the hypertangent function in the Curtice model by a hypertangent polynomial approximation function. This facilitate convergence in the SPICE algorithm. The second new tem which is apparent in the Statz model is the new denominator term $[1 + b (V_{gs} + V_{to})]$. This term was added to model the Ids current under high gate to source voltage. However, measurements have shown that the square law equations model the MESFET behavior very well. Only under the condition when the gate to source voltage approaches the Schottky diode turn-on voltage does the Ids current no longer obey the square law. Only then does the newly added denominator term appears to model the current degradation. In other regions of transistor operation, the (b) term is very small and does not effect the current (Ids).

In the Statz model, the symmetry problem observed in the Curtice model was removed by providing a second diode located at the gate to drain. In addition, the new symmetric capacitance model equations are:

1) when $V_{ds} > 0$, then

$$Q_g = 2C_{gso} V_{BI}[1 - (1 + V_{gs}/V_{BI})^{1/2}] + C_{gdo} V_{gd} \qquad (1.6)$$

$$C_{gs} = dQ_g/dV_{gs} = C_{gso} / (1 + V_{gs}/V_{BI})^{1/2}$$

$$C_{gd} = dQ_g/dV_{gd} = C_{gdo}$$

2) when $V_{ds} < 0$, then

$$Q_g = 2C_{gso} V_{BI}[1 - (1 + V_{gd}/V_{BI})^{1/2}] + C_{gdo} V_{gs}$$

$$C_{gs} = dQ_g/dV_{gs} = C_{gdo}$$

$$C_{gd} = dQ_g/dV_{gd} = C_{gso} / (1 + V_{gs}/V_{BI})^{1/2}$$

This capacitance model automatically takes into account the symmetry of the MESFET when used as a pass gate or as a transistor switch.

One of the more critical problem in the Statz and Curtice models exists in the region of subthreshold conduction. Only the McKinley model[4] has attempted to

address this problem by introducing a subthreshold conduction term. This term exponentially decays as the MESFET device goes into full conduction., The McKinley model has also made the saturation voltage parameter (ø) a function of V_{gs}.

In ending this section on SPICE large signal MESFET models, a few words should be said about the difficulties encountered in SPICE2 with the Curtice's, Equation (1.1). Users of SPICE2 have reported that there are major convergence problems with this equation. It appears that the hypertangent function causes a variety of convergence problems in the SPICE2 algorithms.

IV. TEMPERATURE INDEPENDENCE VOLTAGE REFERENCE CIRCUIT

In the previous sections, the temperature dependence of SPICE large signal MESFET parameters were examined. The results were plotted in Figures (20-23). The information obtained from temperature measurements will be used in the design of a temperature stable voltage reference circuit.

A. The Basic Reference

The first step in realizing a voltage reference is to find a temperature stable unit of voltage. In GaAs MESFET technology, the threshold voltage is a candidate for such a unit of voltage. However, the independent terms that make up the threshold voltage are temperature dependent as well as process dependent as seen below:

$$V_p = \varnothing_i + V_T = qN_qA^2/2 \qquad (1.7)$$

$$\varnothing_i = \varnothing_m - X_i - (1/q)[E_c - E_i]$$

$$\varnothing_i = \varnothing_m - X_i + (1/q)[kT \ln(N_d/N_c)]$$

$$V_T = \varnothing_m - X_i + (kT/q) \ln(N_d/N_c) - qN_dA^2/2$$

The threshold voltage if used alone will not make a suitable voltage reference. However, if one considers the last term in Equation (1.7), it is possible to change

the threshold voltage by either changing the process doping level or by changing the channel thickness. Two devices made with different threshold voltages can be used as a standard reference. Subtracting the two threshold voltages, we obtain:

$$V_{T1} - V_{T2} = kT/q \ln(N_{d1}/N_{d2}) + (q/2)[N_{d1}A_1^2 - N_{d2}A_2^2] \qquad (1.8)$$

Notice that in Equation (1.8) many of the temperature dependent terms are cancelled. We can use this to design a circuit where the gate-source is used to sense the threshold voltage.

A circuit that produces a reference voltage is shown conceptually in Figure (27). In this figure, transistor B1 and B2 exhibit different threshold voltages. By using an operational amplifier in a negative feedback configuration, the output voltage is forced to a level that causes the reference devices to operate at an equal drain voltage.

The temperature sensitivity of VREF can be analyzed by considering the equations:

$$V_{GS} = V_T + [I_d/\beta\ (1 + \Omega V_{ds})]^{1/2} \qquad (1.9)$$

$$V_{REF} = V_{GS1} - V_{GS2} = V_{T1} - V_{T2} + \{[I_d/\beta_1\ (1 + \Omega_1 V_{ds1})]^{1/2} - [I_d/\beta_2\ (1 + \Omega_2 V_{ds2})]^{1/2}\}$$

Taking the derivative of Equation (1.9), the following equation is obtained:

$$
\begin{aligned}
VREF/dT = {} & d(VT1 - VT2)/dT \; [1/2](Id)^{-1/2} \\
& \{[Id/\beta 1 \; (1 + \Omega Vds)]^{1/2} - 1/[\beta 2(1 + \Omega Vds)]^{1/2}\} dI/dT \\
& + [(Id)^{1/2}]/2 \; \{d\beta 2/dT) \; \{1/[\beta 2^3 \; (1 + \Omega 2Vds2)]^{1/2} \} \\
& - [(Id)^{1/2}]/2 \; \{d\beta 1/dT) \; \{1/[\beta 1^3 \; (1 + \Omega 1Vds1)]^{1/2} \}
\end{aligned}
$$

B. Threshold Voltage Considerations

The first term in Equation (2.0) is the temperature dependence of the threshold voltage difference. From Equation (1.8), the derivative is taken to obtain the equation:

$$d(VT1 - VT2)/dT = k/q \; \ln(Nd1/Nd2)$$

In the situation when Nd1 = Nd2, the threshold difference will theoretically not vary with temperature. In general, this is impossible to obtain due to process variations. Usually the threshold voltage difference will vary linearly with temperature. From Curtice model simulations with SPICE, the threshold voltage difference was found to vary with a slope of approximately -0.104mV/^{o}C.

C. Bias Current Considerations

The second term in Equation (2.0) can be made insensitive to drain current variations by equating:

$$\beta 1\ (1 + \Omega 1 Vds1) = \beta 2\ (1 + \Omega 2 Vds2)$$

To further reduce the effects of the second term, the drain current can be biased at a point where $dIds/dT = 0$. This occurs because the MESFET's current tends to increase with temperature due to its dependence on threshold voltage, and decrease with temperature due to mobility degradation. These tendencies are nearly in balance at a bias level that is itself only slightly temperature dependent. The bias level effect measured from experimental devices are shown in Figures (28) and (29).

The third term is temperature dependent due to the mobility decreasing at the higher temperatures. This term is not compensated for in the reference circuit. However, it appears that the voltage recference is not effected greatly by this third term and the errors it contributes are relatively small.

D. Reference Circuit

Figure (30) shows a schematic of a GaAs MESFET voltage reference. Transistors B1 and B2 are the differential threshold voltage pair. They are loaded

by depletion current sources B3 and B4. Transistor B3 and B4 are matched transistors. Any mismatch in B3 and B4 will degrade the output voltage temperature coefficient. Transistor BBIAS is the tail current source used to bias the differential pair.

E. Differential Amplifier

In order for the voltage reference to work properly, a high gain differential amplifier is required in the negative feedback path of the circuit. In 1984, one such circuit was proposed by Fiedler[15]. However, the circuit proposed in the report was not fabricated and information concerning its actual performance is unknown. More recently, Larson[19] proposed and fabricated a differential amplifier using a common mode feedback for double-to-single end conversion scheme (Figure 31). In our present work, the design of a differential amplifier has not been addressed; therefore, the circuit will require an off chip amplifier.

F. Voltage Reference Simulation Results

Simulation of the voltage reference circuit was done with the simulation program SPICE using the Curtice model. The transistor parameters for the Curtice model were set to the values obtained from our measurements. The results of the simulation are presented in Appendix (3). They show that the circuit has a temperature dependence of -0.08mV/^{o}C (Figure 32). This translates to a

temperature coefficient of -107ppm/^{o}C which is comparable to low-voltage Si designs. The nominal voltage reference obtained from the measured devices was 0.750 volts.

V. CONCLUSION

The Curtice and Statz GaAs large signal models implemented in SPICE were evaluated. Their abilities to model typical devices were found to be ineffective in certain regions of transistor operation. It appears that further work on MESFET modeling is still required. At present, simulation with SPICE using the Curtice and Statz models will require understanding the model's weaknesses. Simulations should be done only in the regions where the models have been found to be consistent with measurements.

From the temperature study, the SPICE parameters for GaAs MESFETs were extracted over a temperature range of interest. The extracted parameters over temperature were plotted in Figures (20-23). Simple linear temperature relationships were developed to approximate the threshold voltage and the output conductance parameters in SPICE. The beta parameter was modeled by a power function as noted in Equation (1.4).

The temperature measurements led to a proposed temperature independent voltage reference circuit. This circuit was designed and simulated using SPICE. From our SPICE simulations, the voltage reference has a predicted temperature coefficient of -107ppm/^{o}C with a nominal voltage reference of 0.750 volts.

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FIGURE LISTING

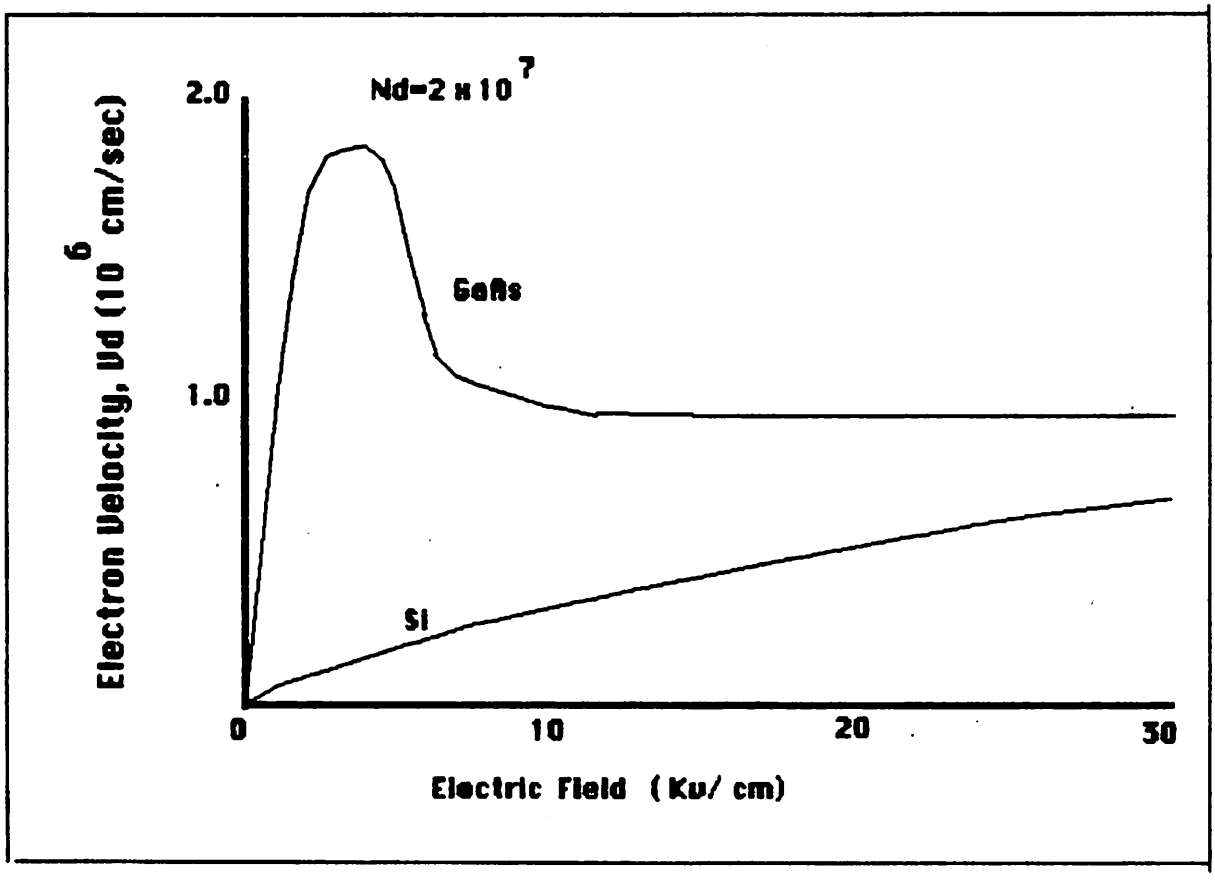
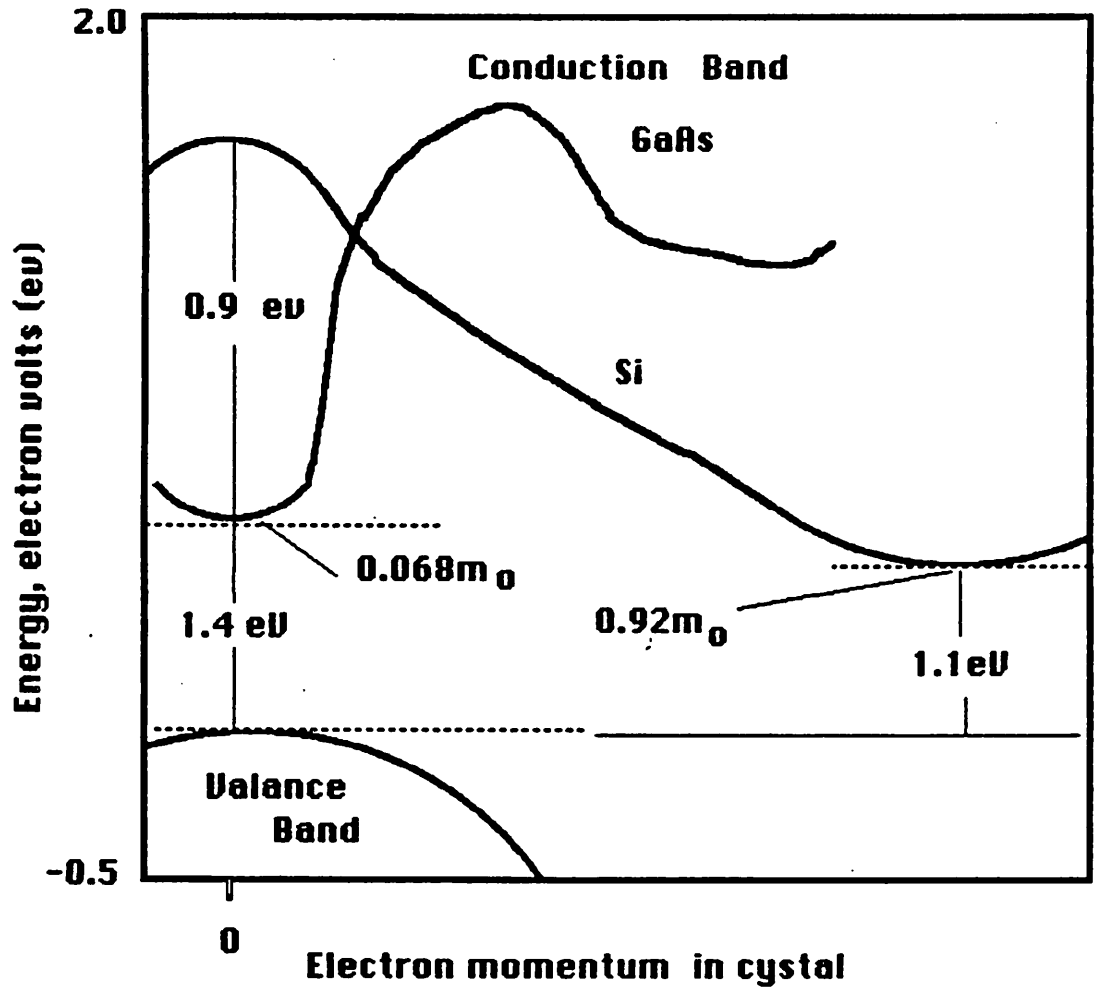
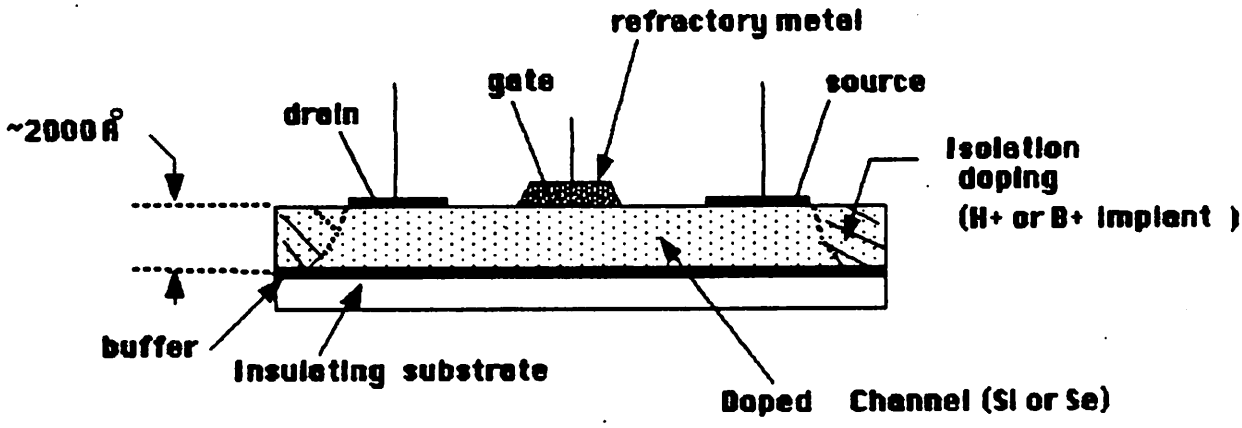

Nd=2 x 10^7
2.0
1.0
GaAs
Si
0
10
20
30
Electric Field (Kv/ cm)
Electron Velocity, Vd (10^6 cm/sec)

Figure 1



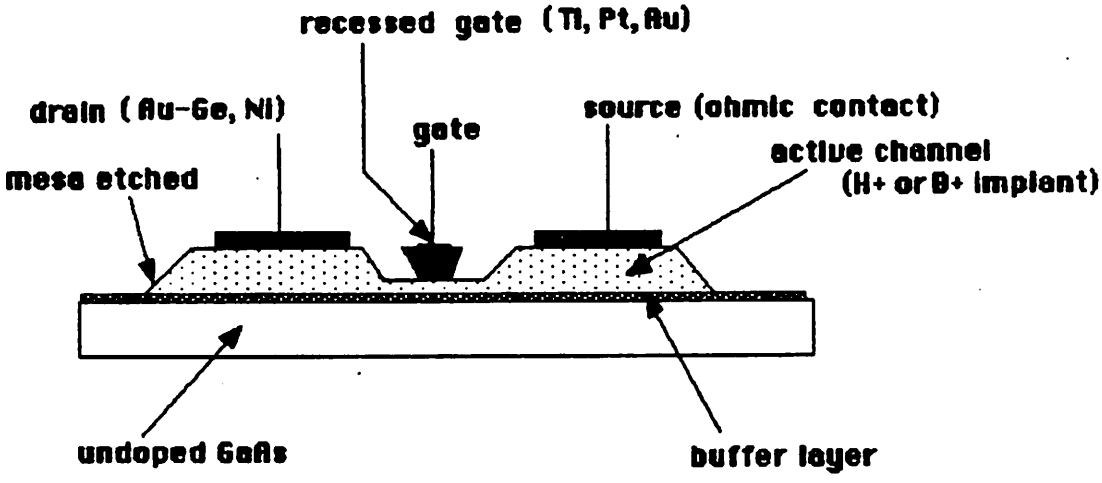
[Johnson, G., " Gallium Arsenide Chips Emerge", High Technology, July 1984]

Figure 2



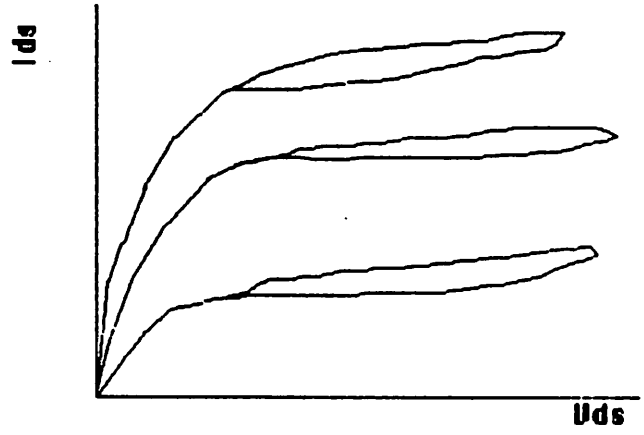
A) Planar Process GaAs MESFET technology (ion implantation)

Figure 3



B) Mesa Etched GaAs MESFET with recessed gate

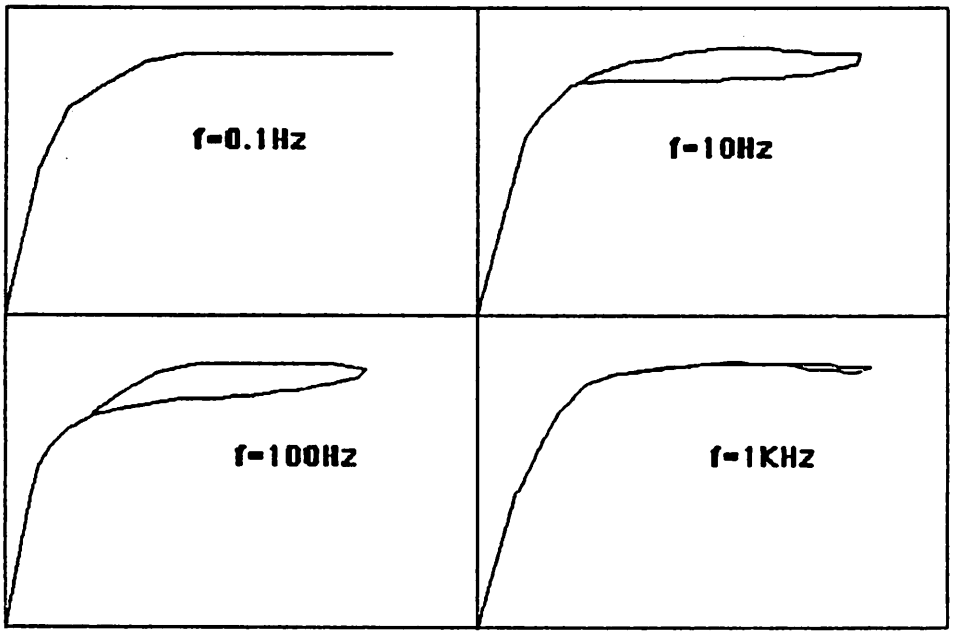
Figure 4



current-voltage characteristic with looping

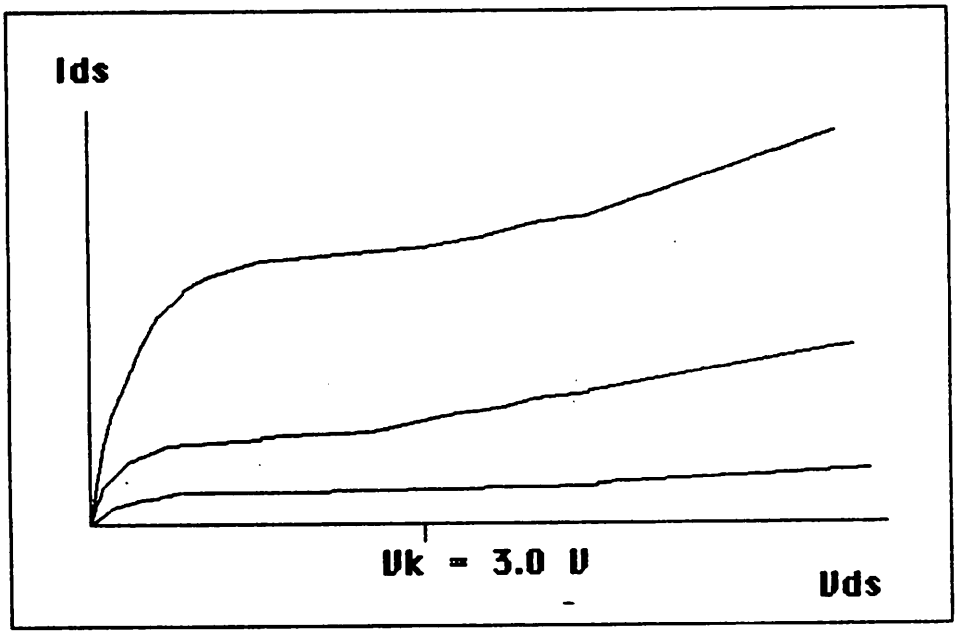
[Rocchi, M. "Statue of Parasitic Effects in GaAs IC", Physica 129B 1985]

Figure 5



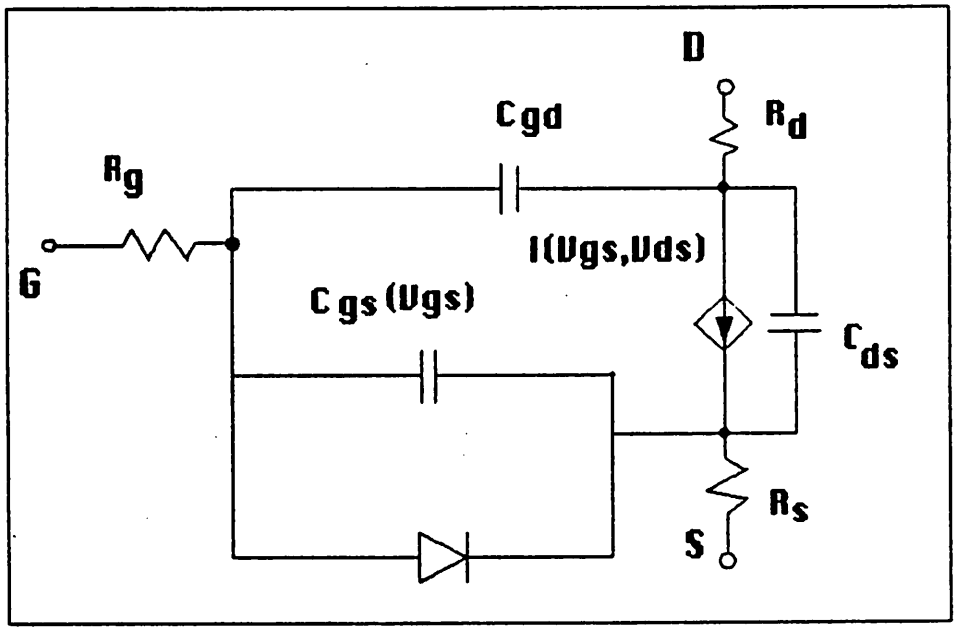
Looping verse frequency for Vgs =0.0
[Rocchi, M. "Surface and Bulk Parasitic Effects in GaAs IC's", Physica 129B, 1985]

Figure 6



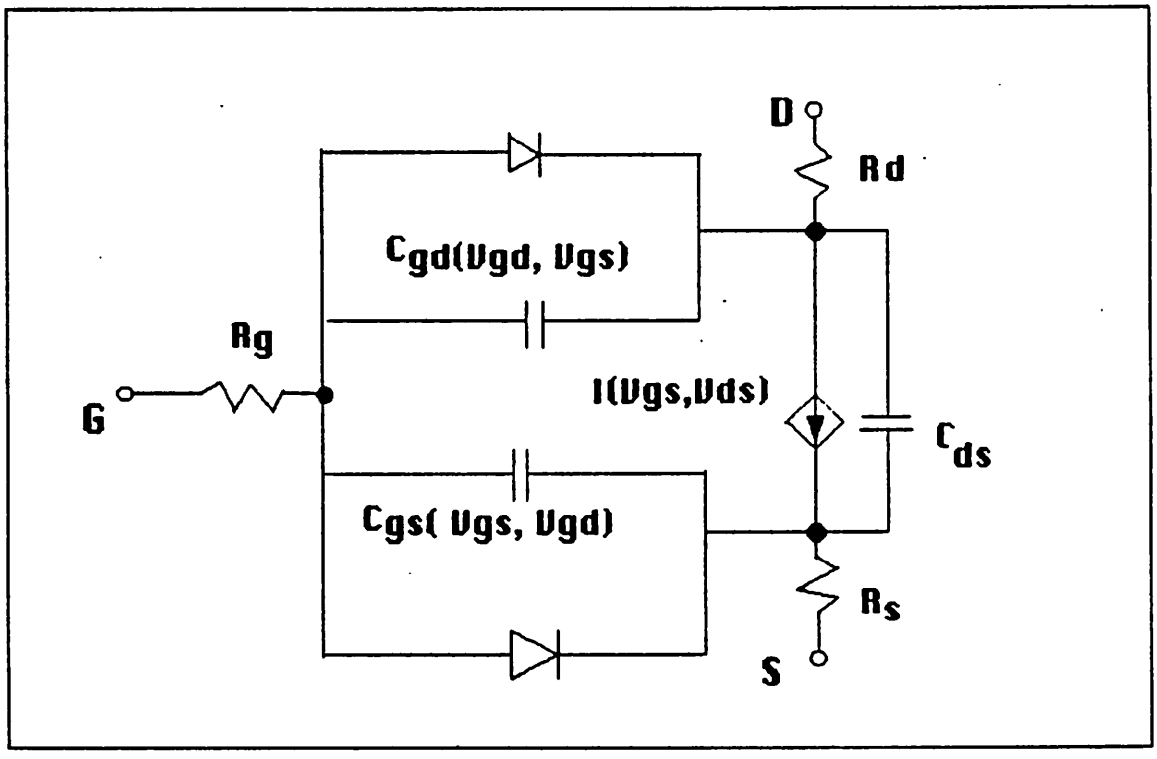
The Kink Effect
[Rocchi, M., "Surface and Bulk Parasitic Effects in GaAs ICs", Physica 129B 1985]

Figure 7



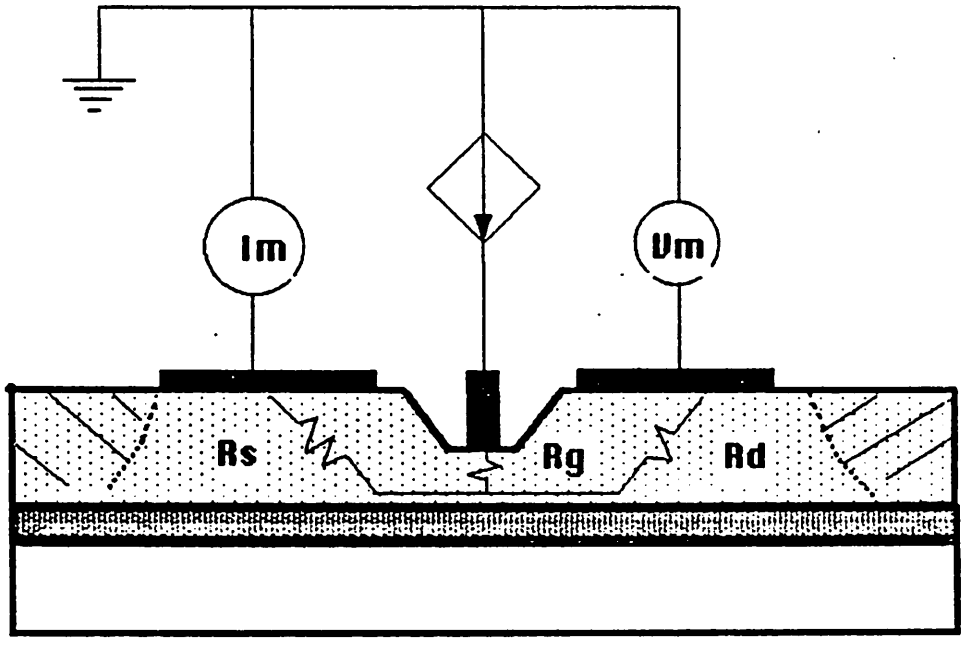
Curtice's GaAs MESFET model

figure 8



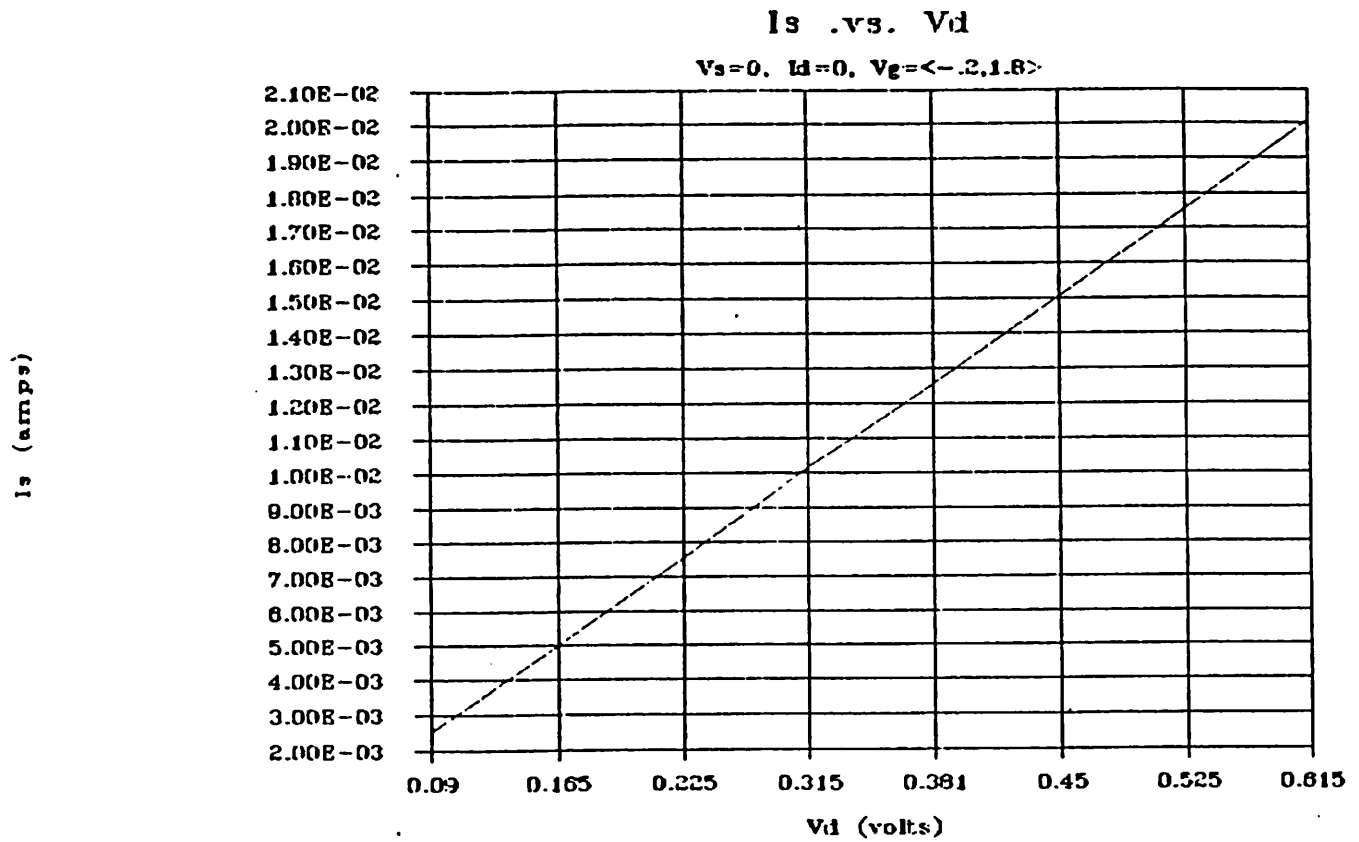
Statz's GaAs MESFET model

Figure 9



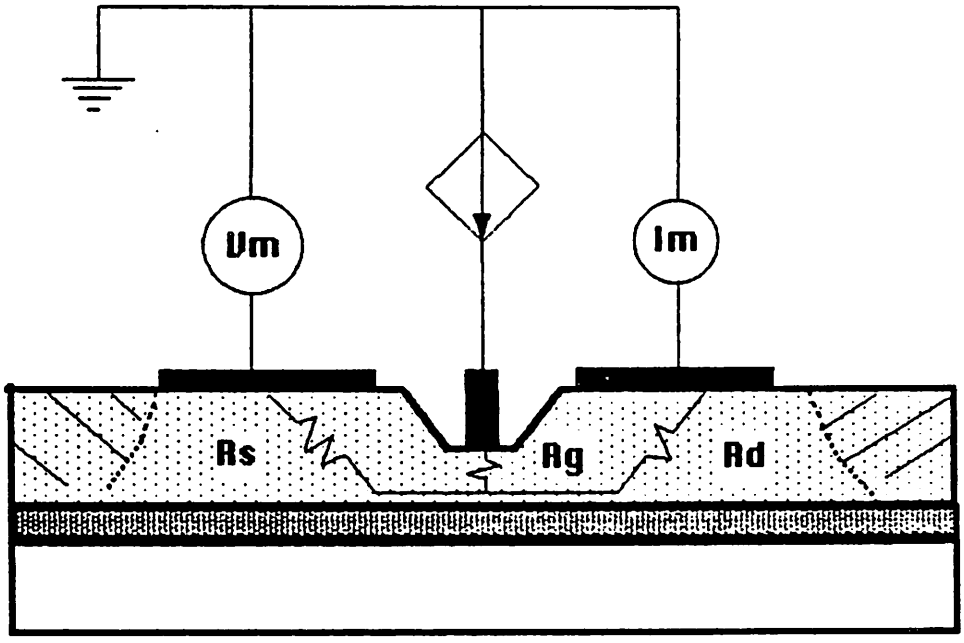
Rs Measurement

Figure 10



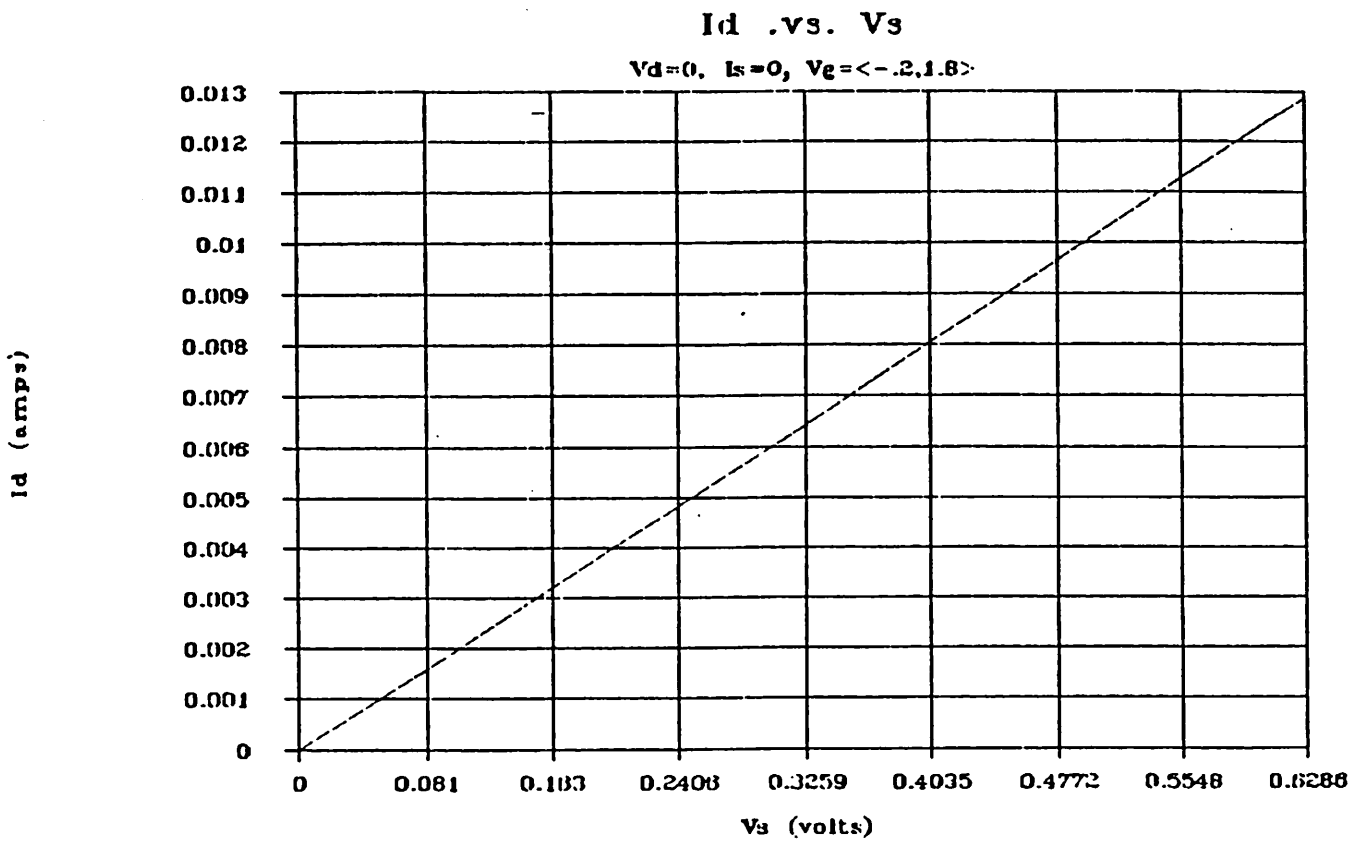
I - V characteristics of measured source resistance

Figure 11



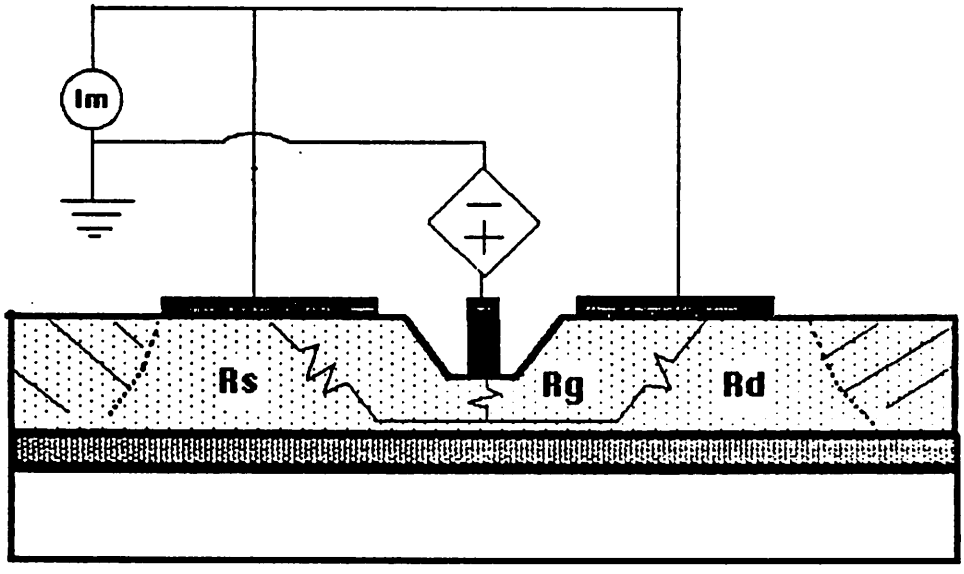
Rd Measurement

Figure 12



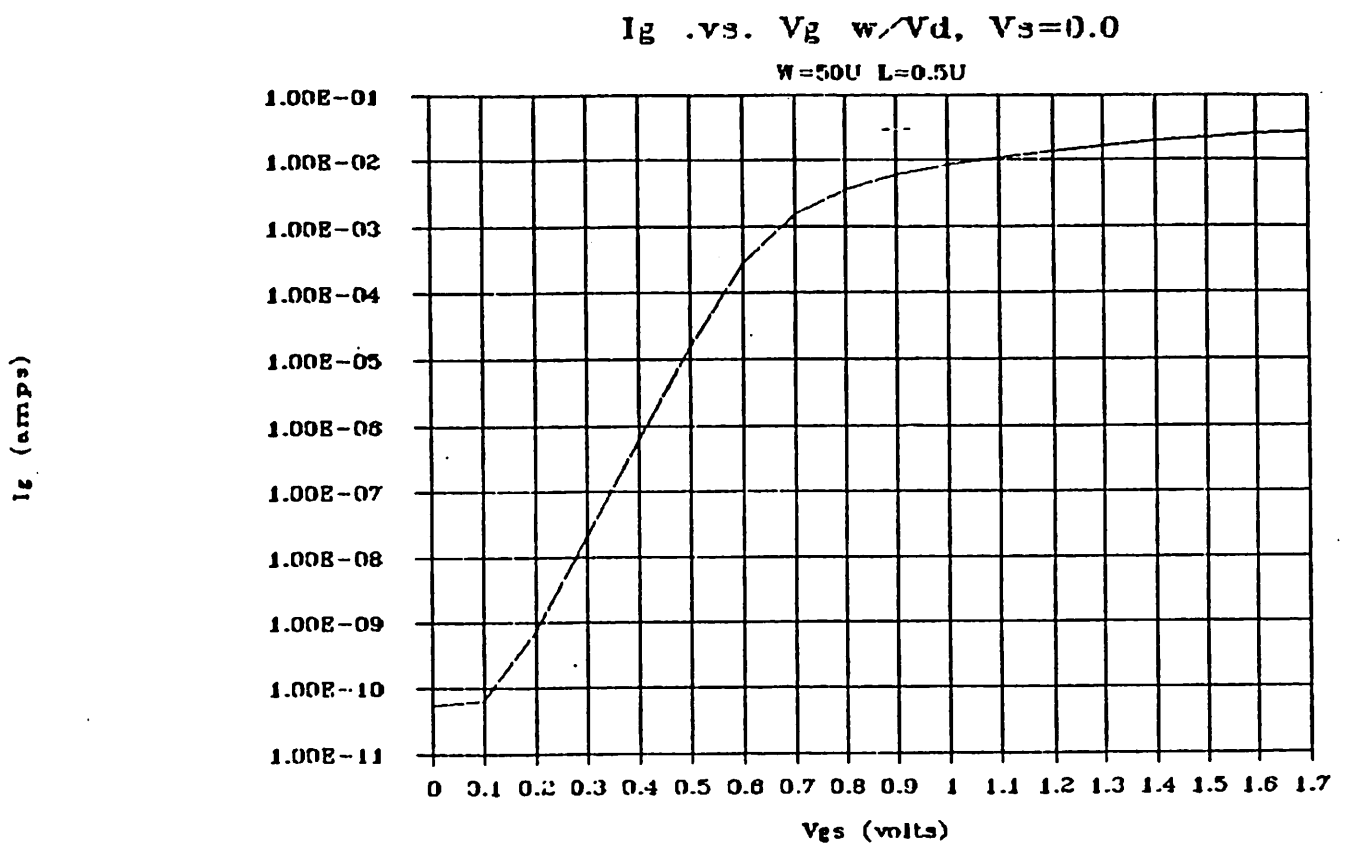
I - V characteristics of measured of drain resistance

Figure 13



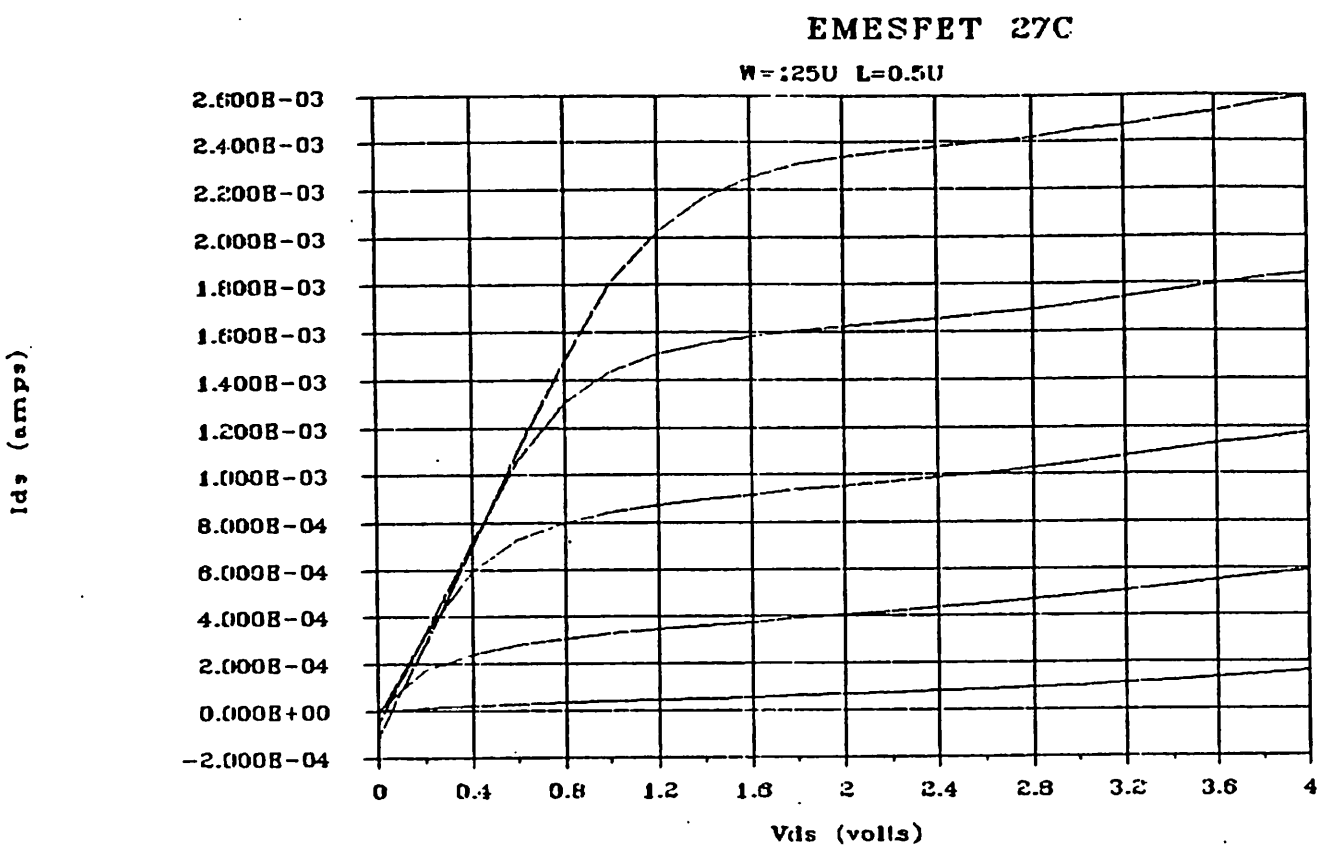
Rg Measured

Figure 14



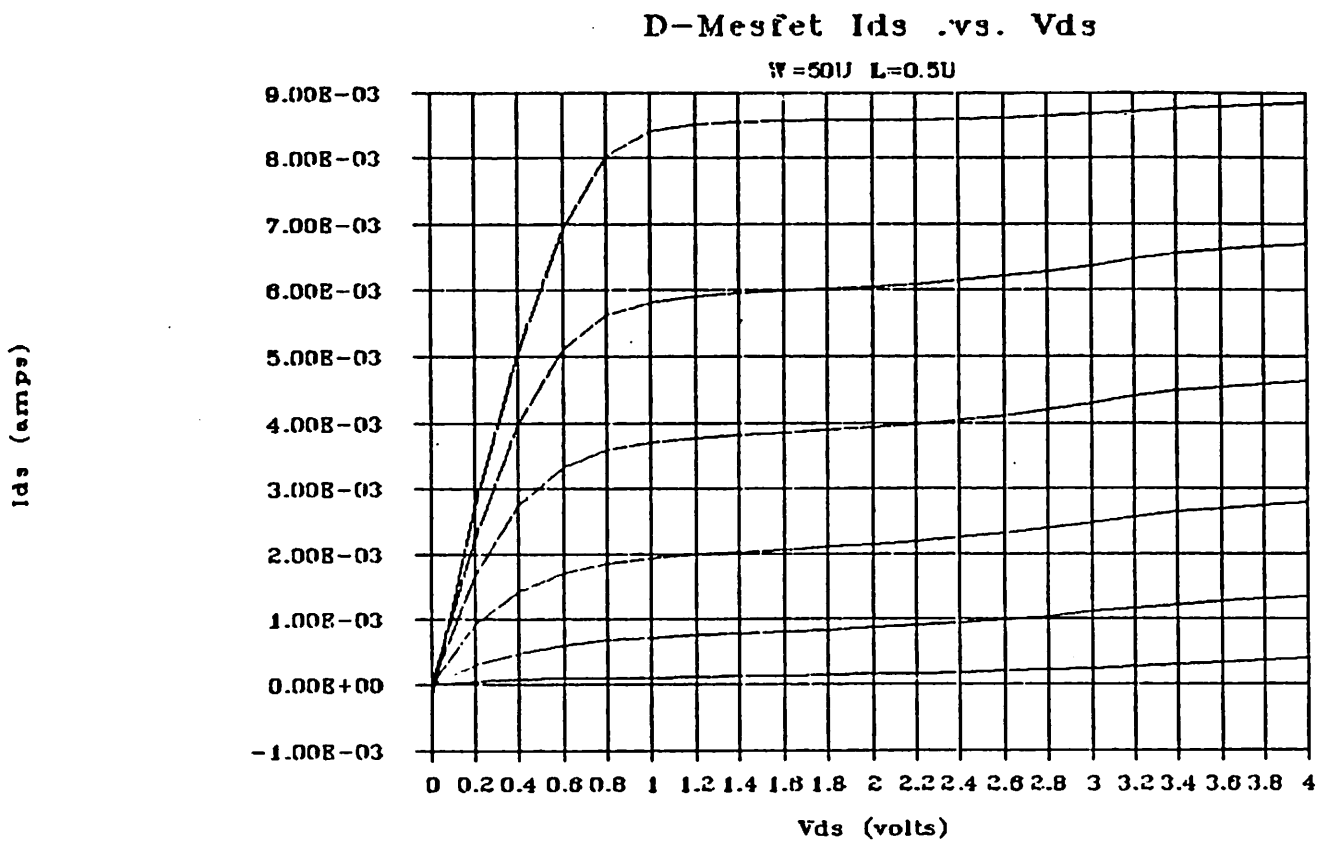
Log (I) versus Vg Characteristics

Figure 15



GaAs Enhancement mode device I - V characteristics

Figure 16

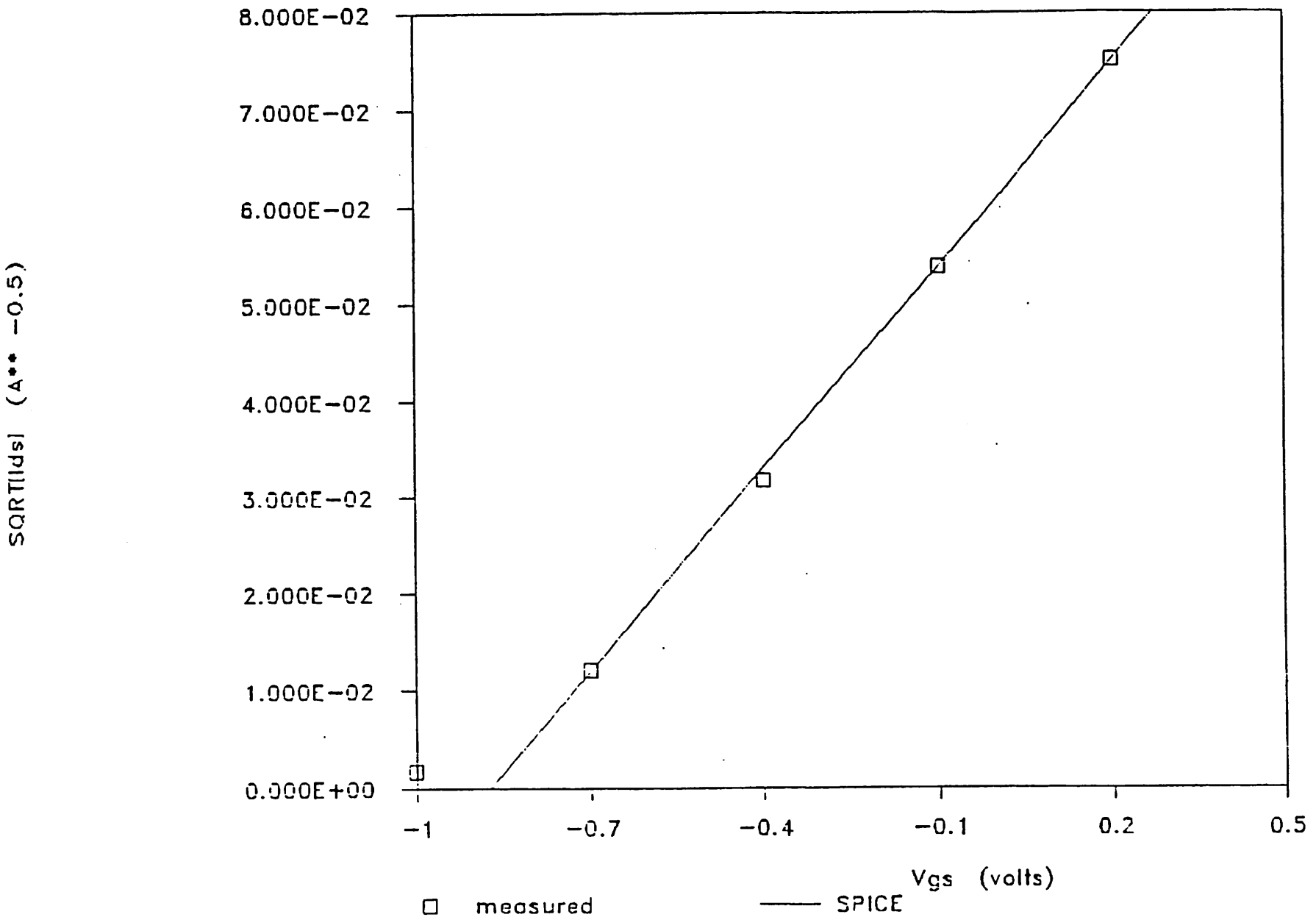


GaAs Depletion mode device I - V characteristics

Figure 17

DMESFET: sqrt(Ids) .vs. Vgs

Figure 18



EMESFET: sqrt(Ids) .vs. Vgs

Figure 19

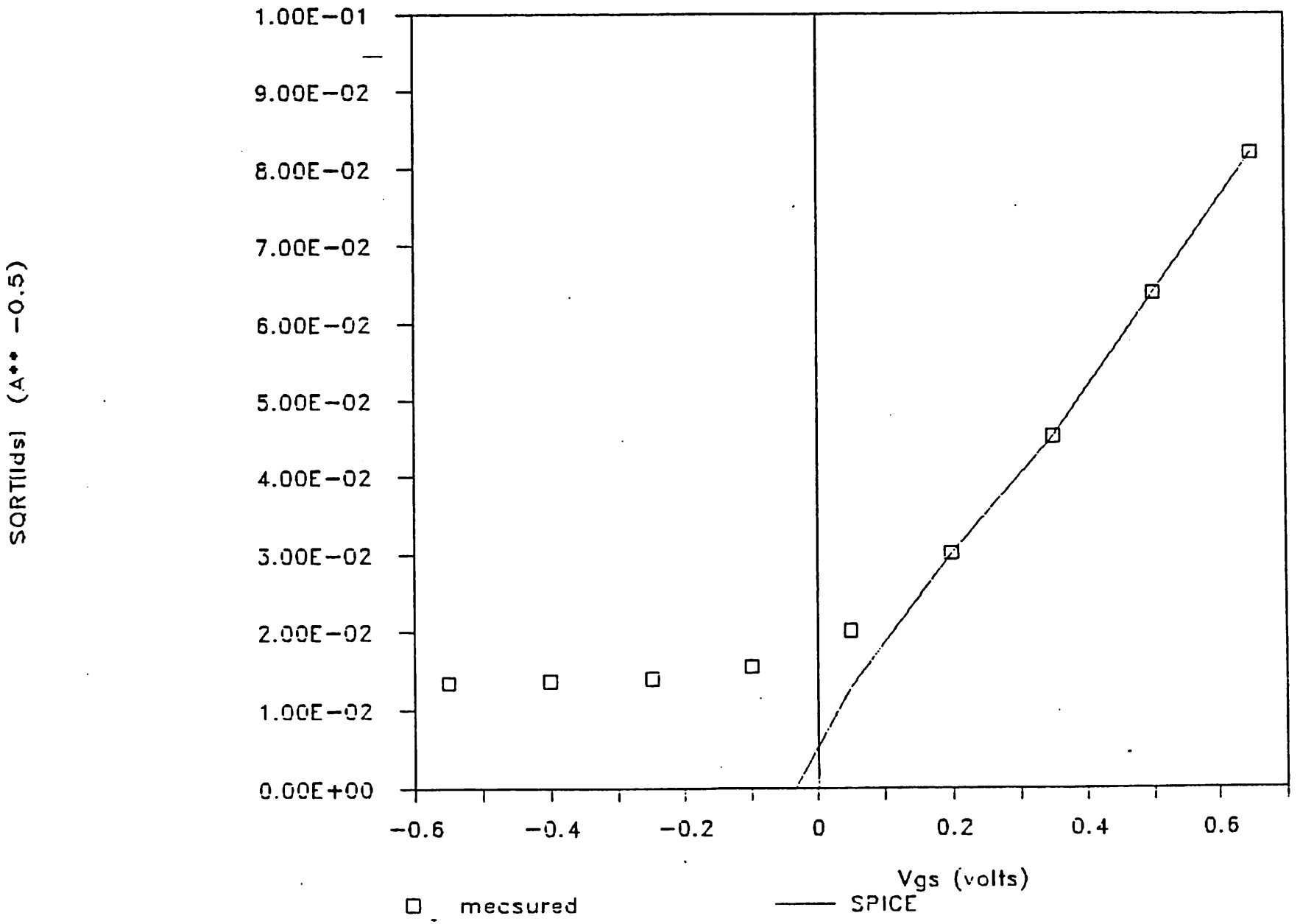
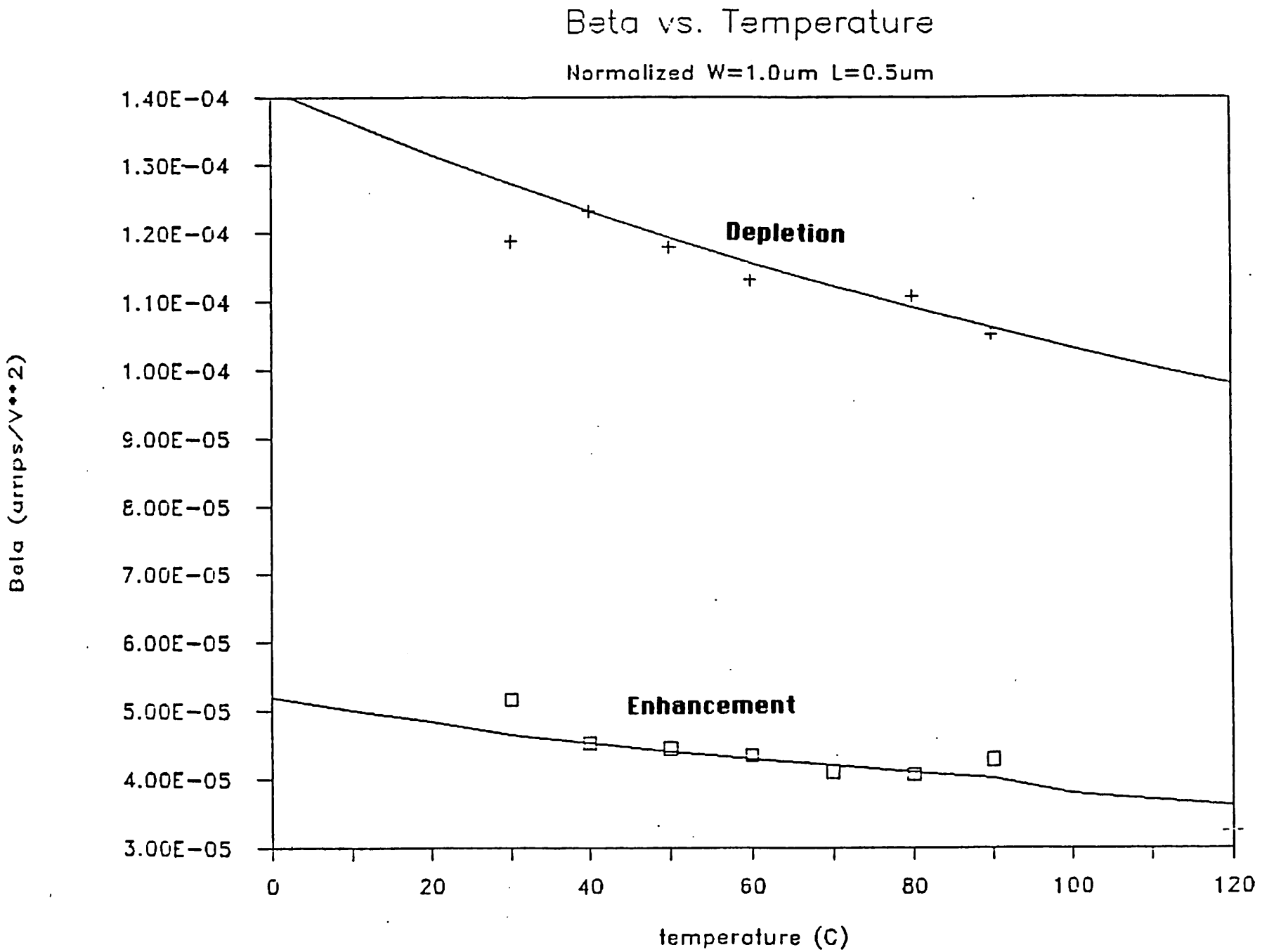
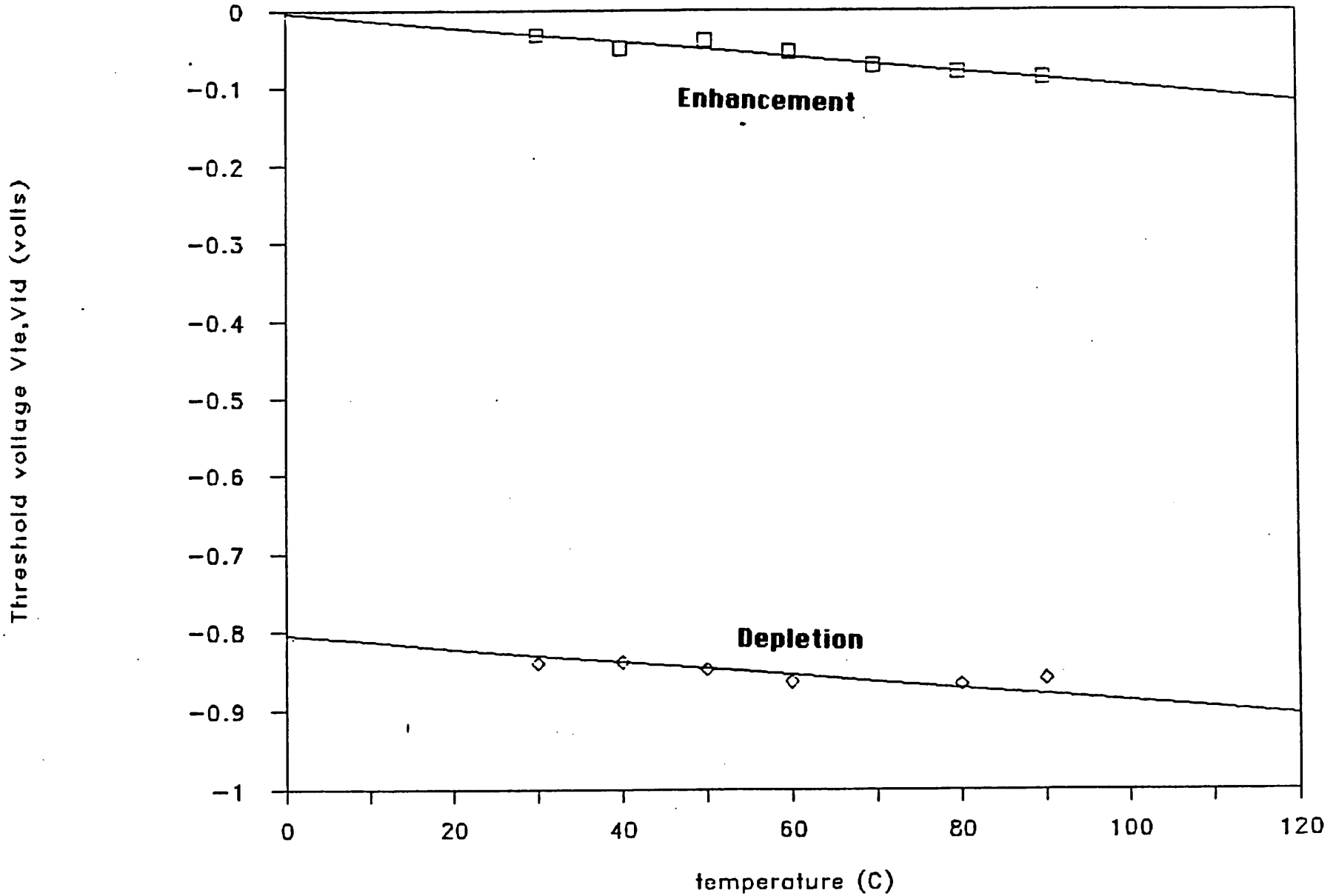


Figure 20


Beta vs. Temperature
Normalized W=1.0um L=0.5um
1.40E-04
1.30E-04
1.20E-04
1.10E-04
1.00E-04
9.00E-05
8.00E-05
7.00E-05
6.00E-05
5.00E-05
4.00E-05
3.00E-05
Beta (amps/V**2)
Depletion
Enhancement
0
20
40
60
80
100
120
temperature (C)

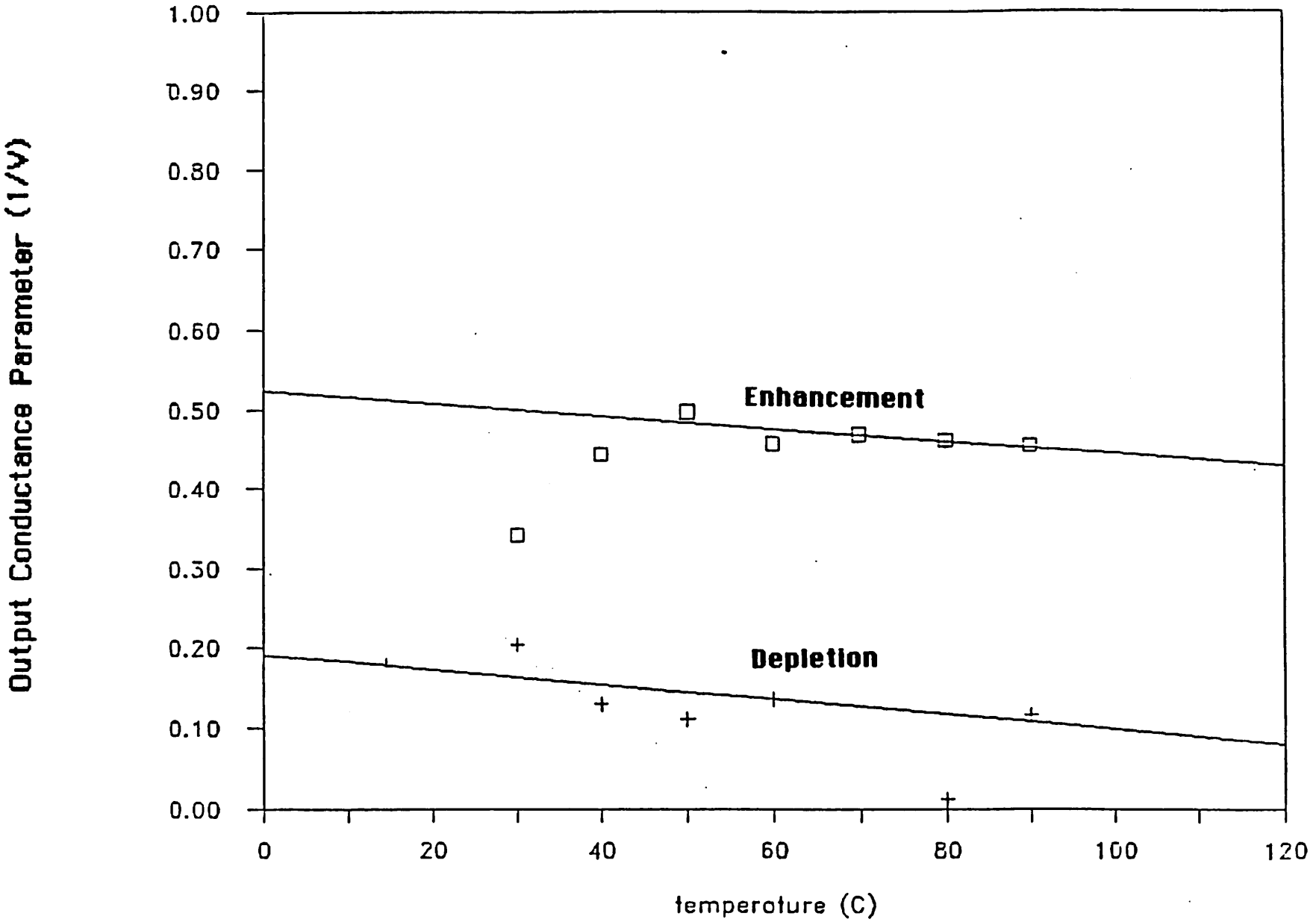
Threshold Voltage .vs. Temperature

Figure 21



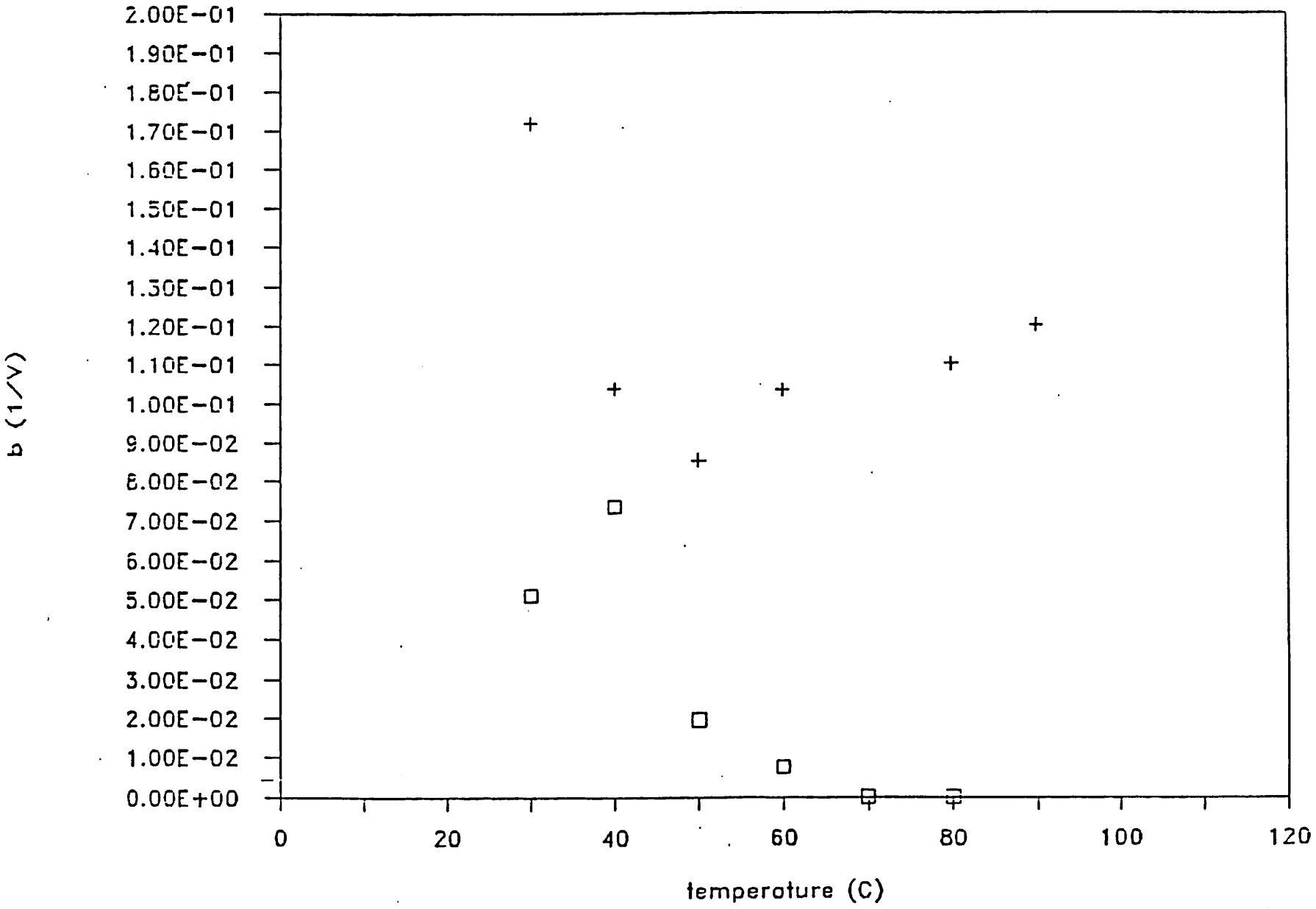
Output Conductance Parameter vs. Temperature

Figure 22



b vs. temperature

Figure 23



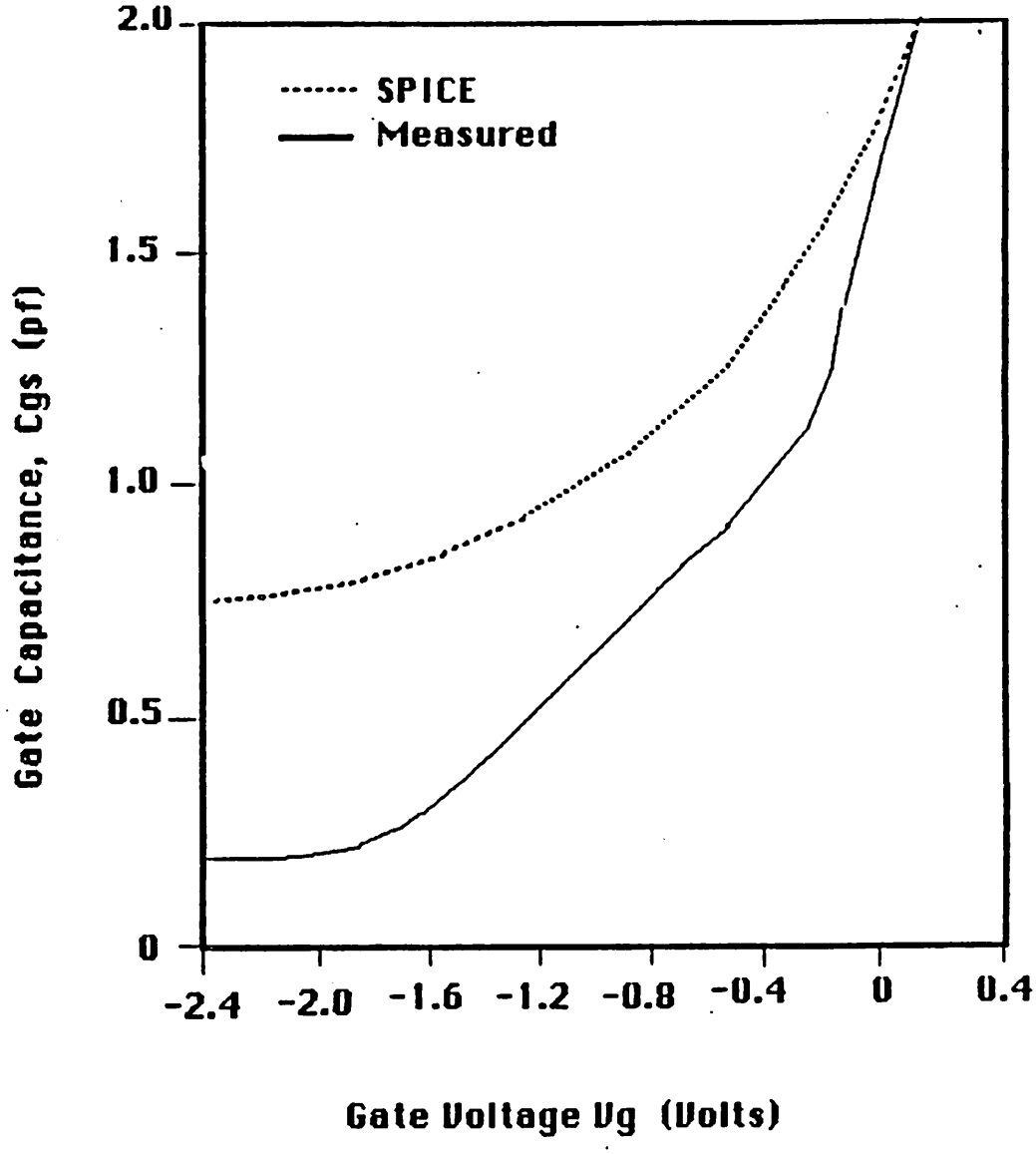

2.0
1.5
1.0
0.5
0
SPICE
Measured
Gate Capacitance, Cgs (pf)
-2.4
-2.0
-1.6
-1.2
-0.8
-0.4
0
0.4
Gate Voltage Vg (Volts)

Figure 24

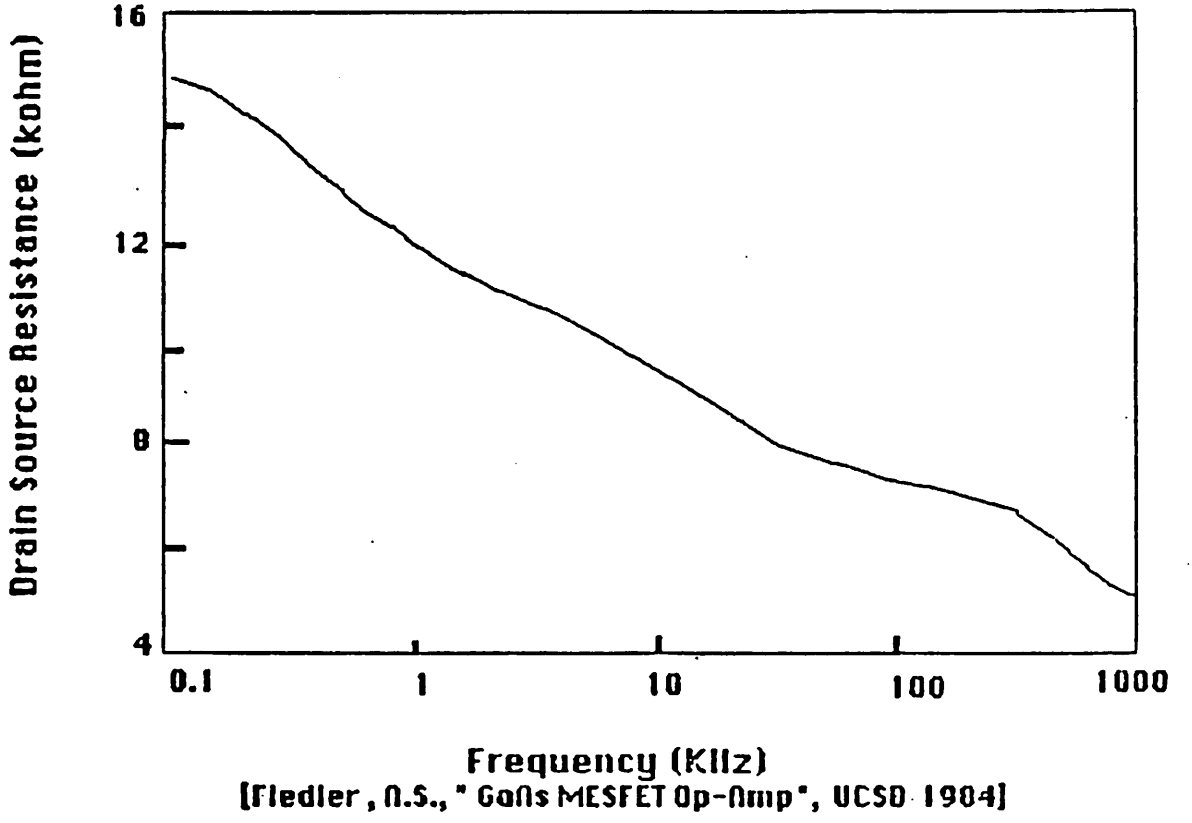
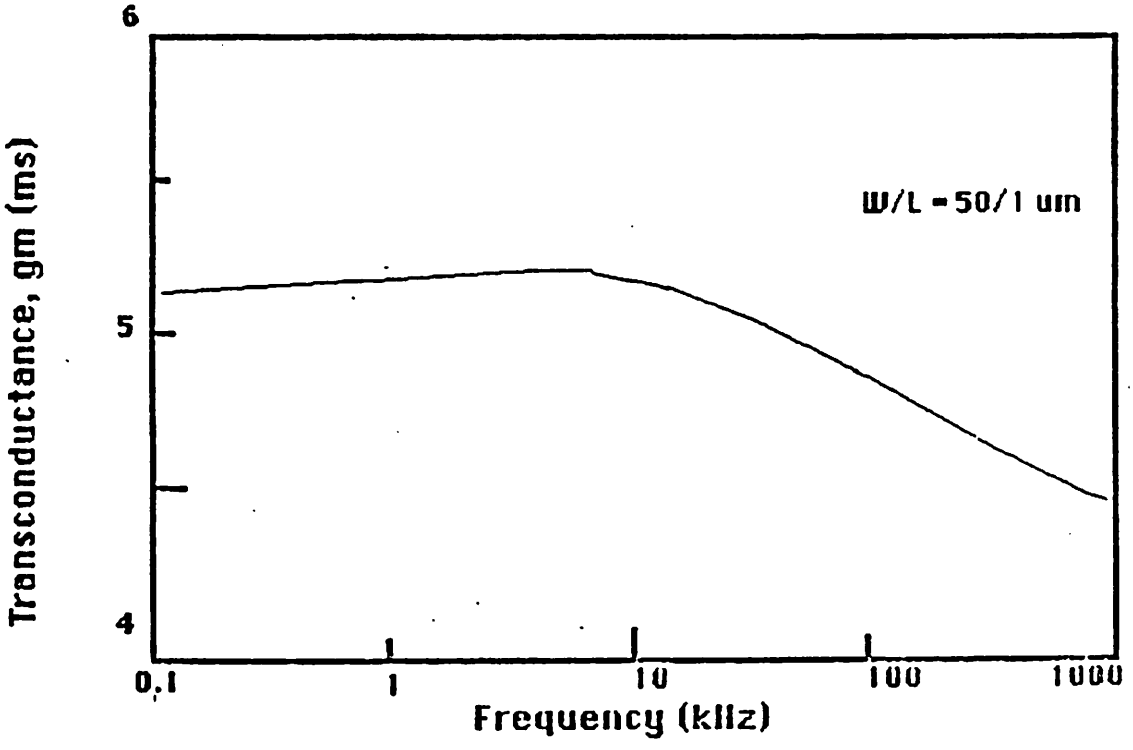

Drain Source Resistance (kohm)
16
12
8
4
0.1
1
10
100
1000
Frequency (KHz)
[Fiedler, A.S., " GaAs MESFET Op-Amp", UCSD 1984]

Figure 25



[A.S. Fedler, " GaAs MESFET Op-Amp", 1984]

Figure 26

Voltage Reference Schematic

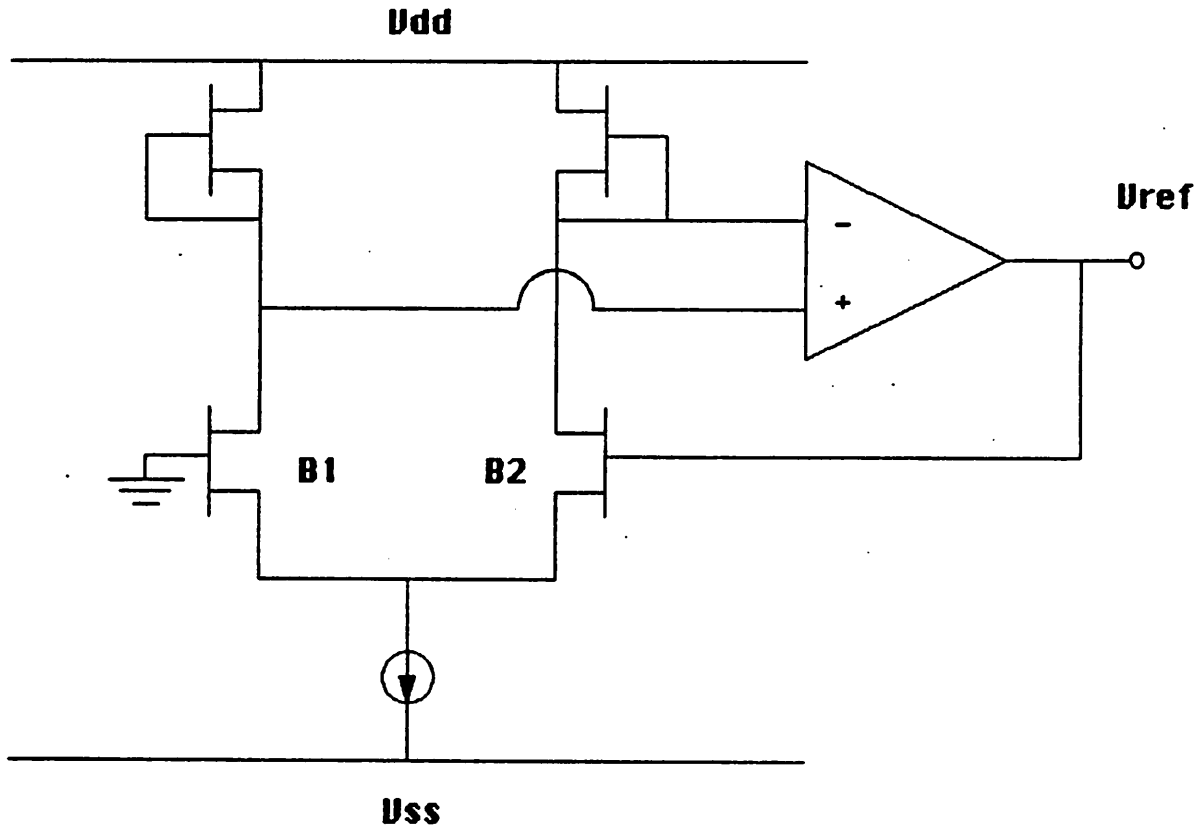
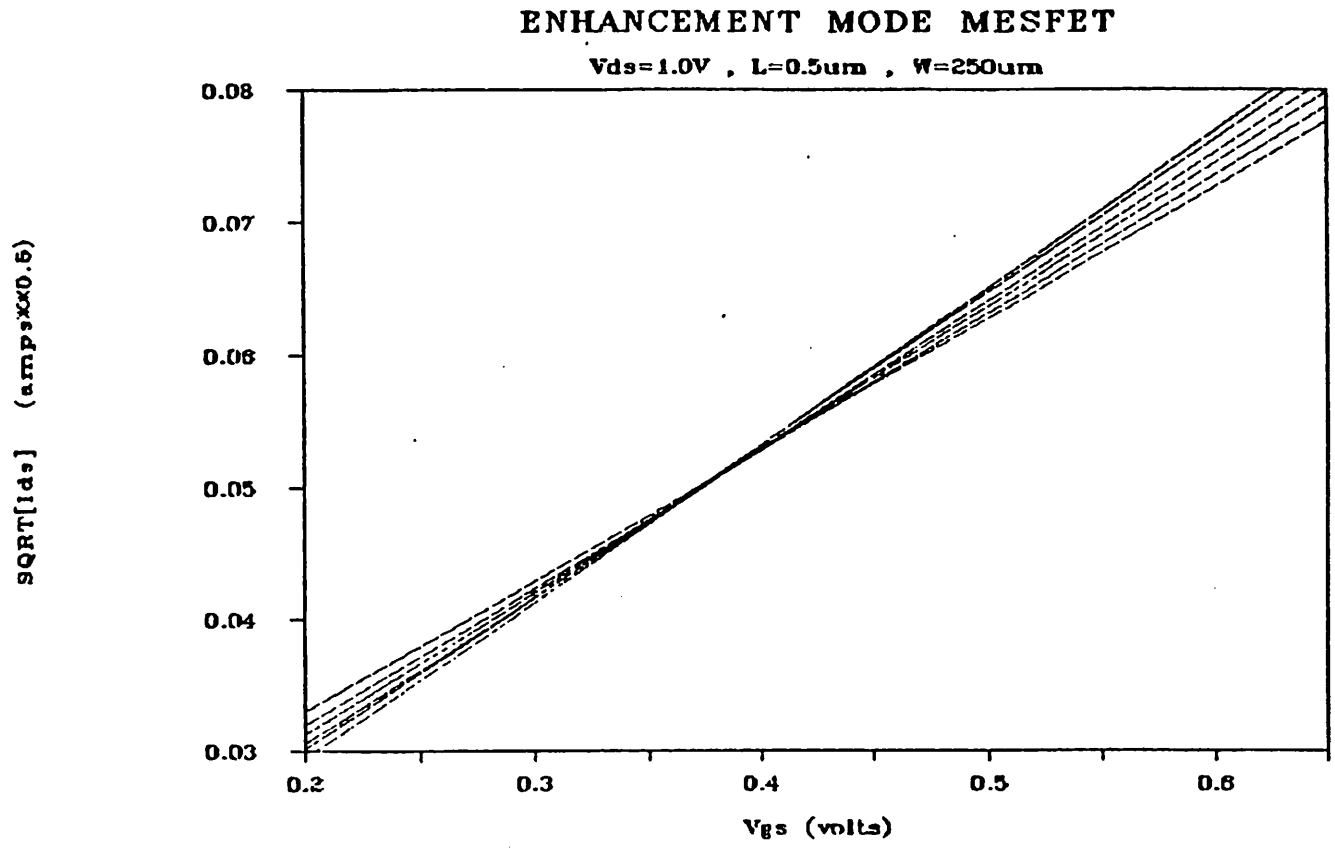
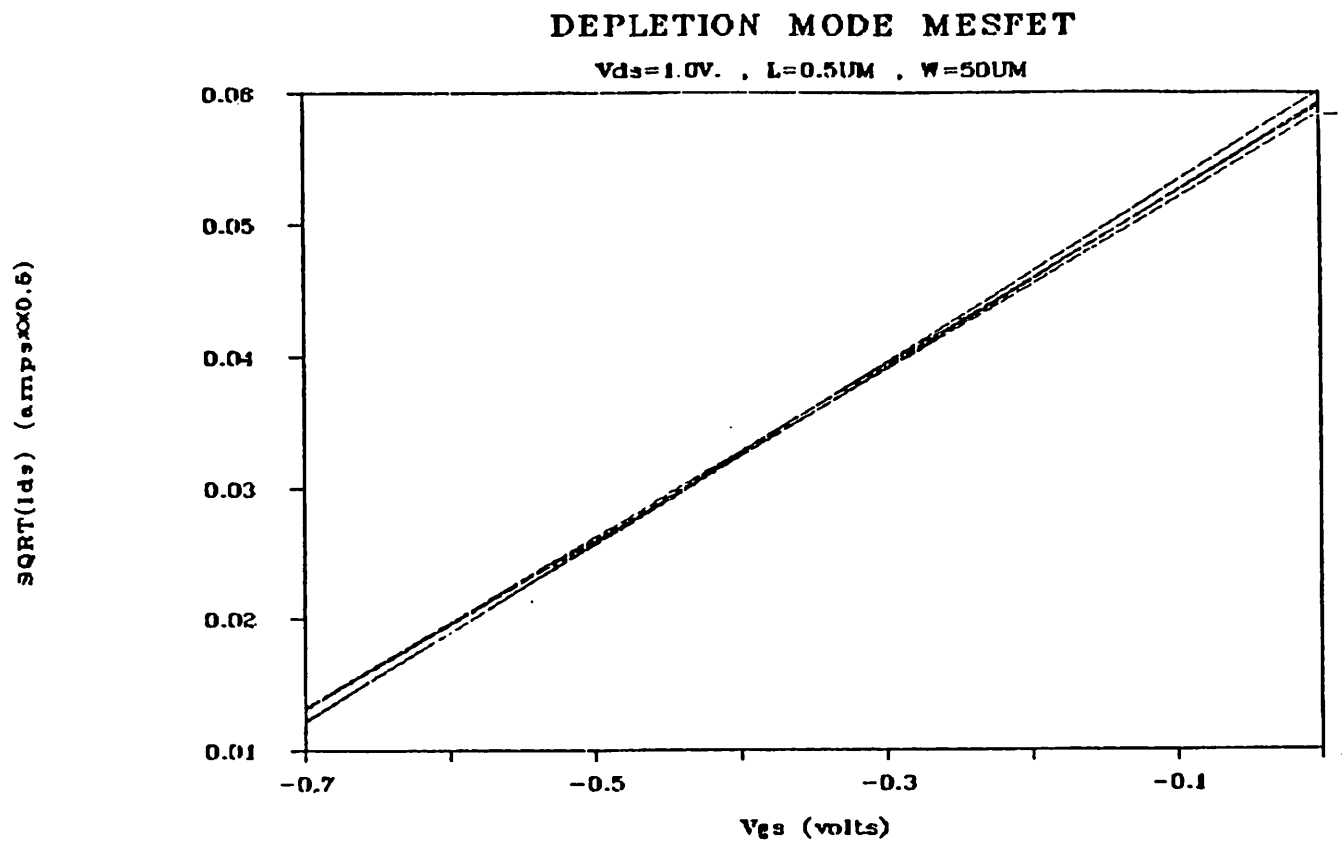


Figure 27



Square root (Ids) versus Vgs plotted over temperature

Figure 28



Square root (Ids) versus Vgs plotted over temperature

Figure 29

Voltage Reference Schematic

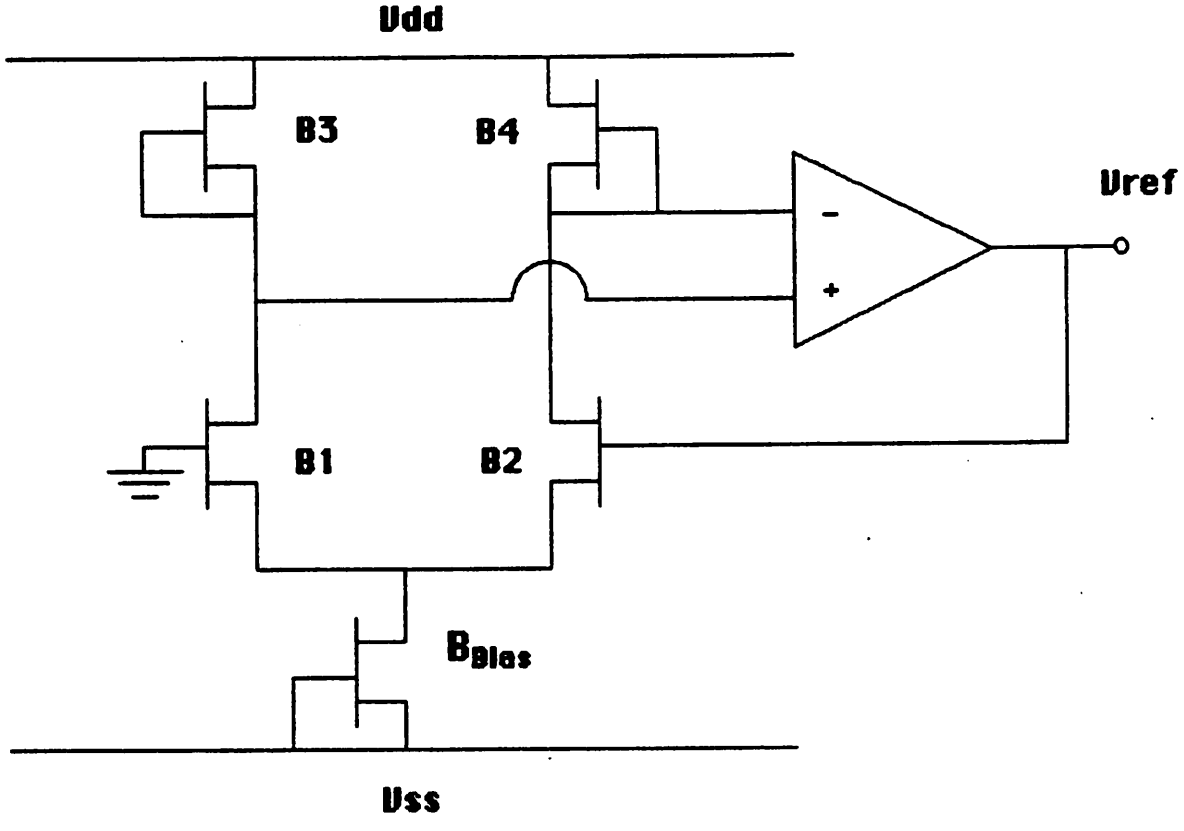


Figure 30

Differential Amplifier with Commom Mode Feedback

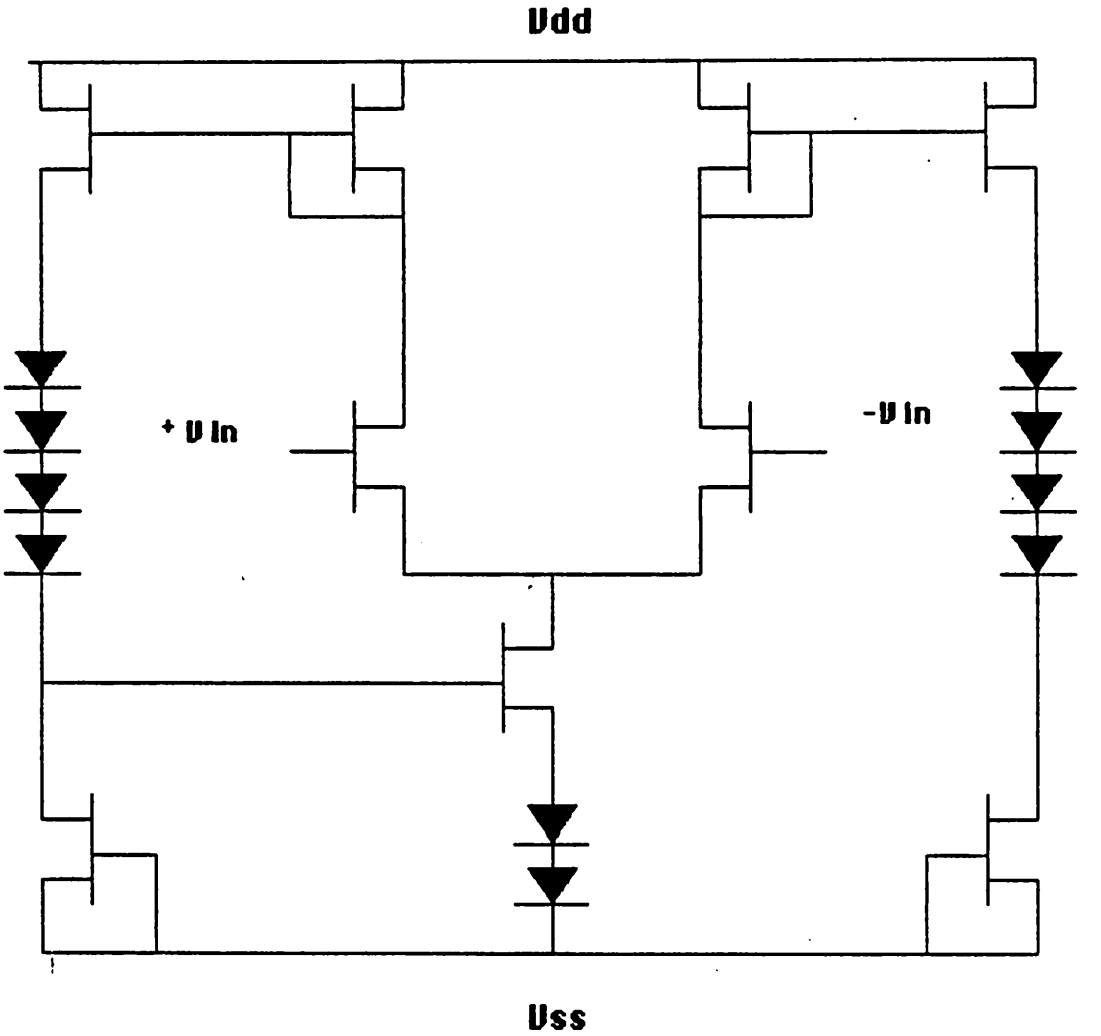
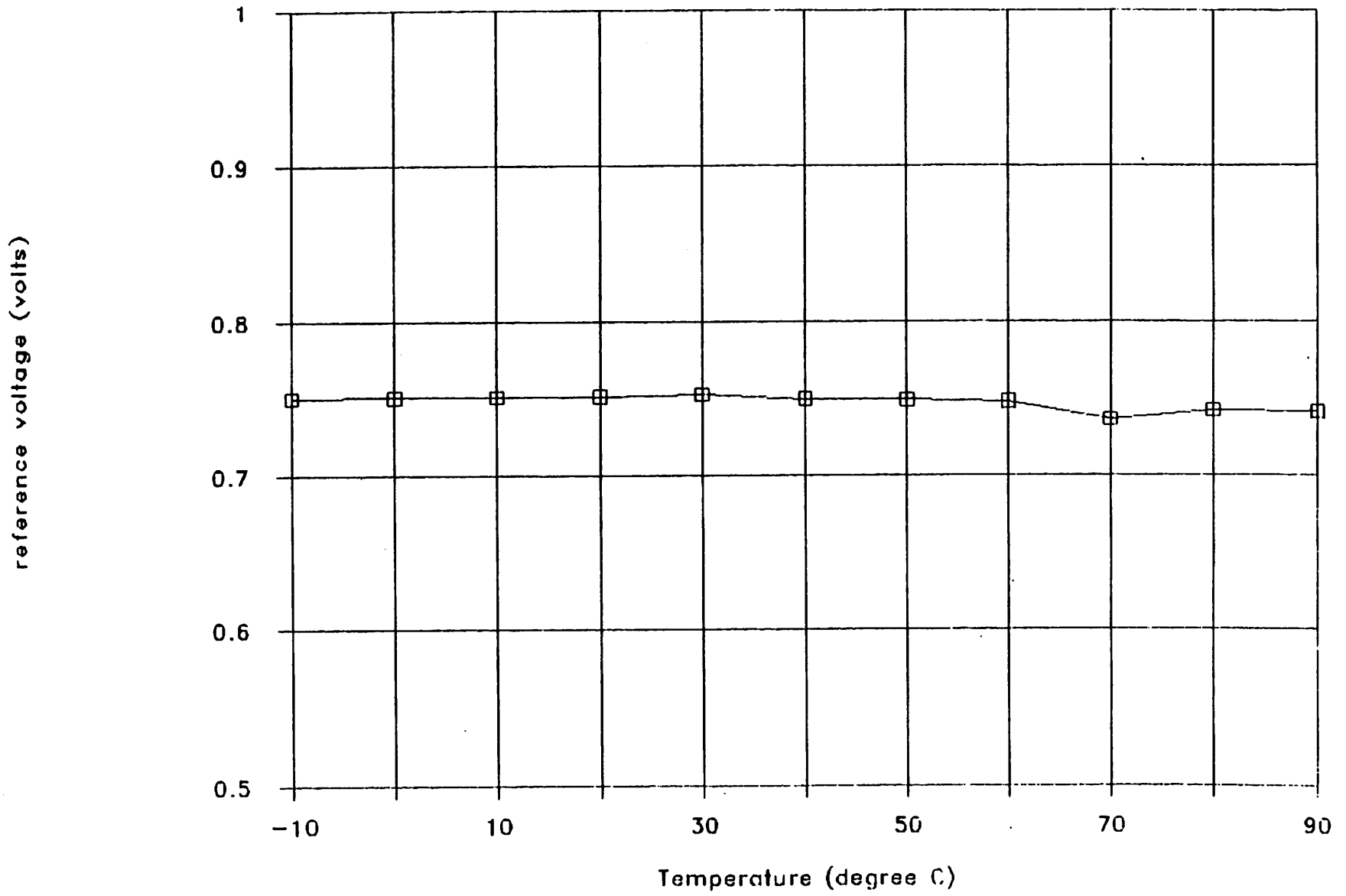


Figure 31

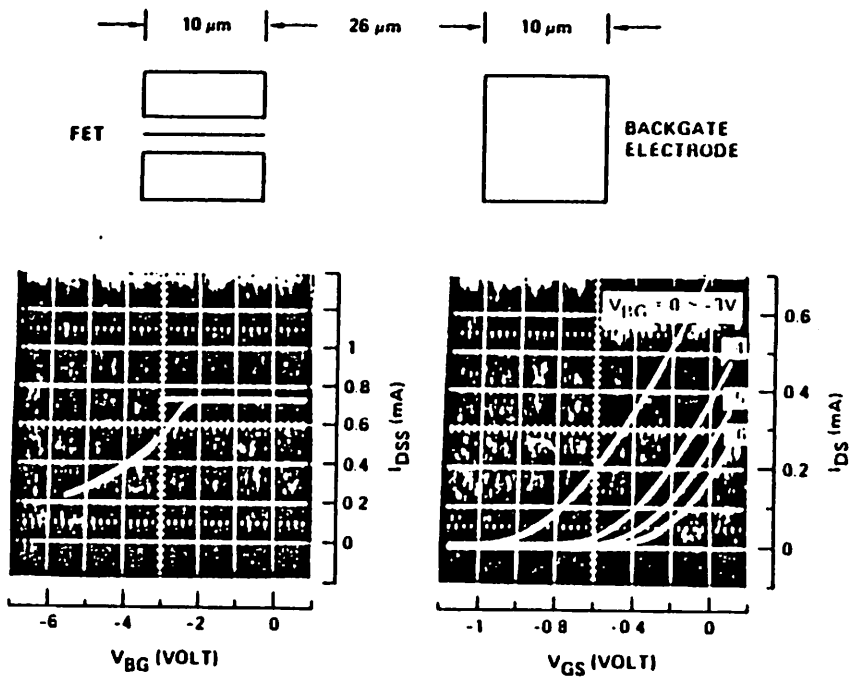
VREF vs. TEMP.

Figure 32

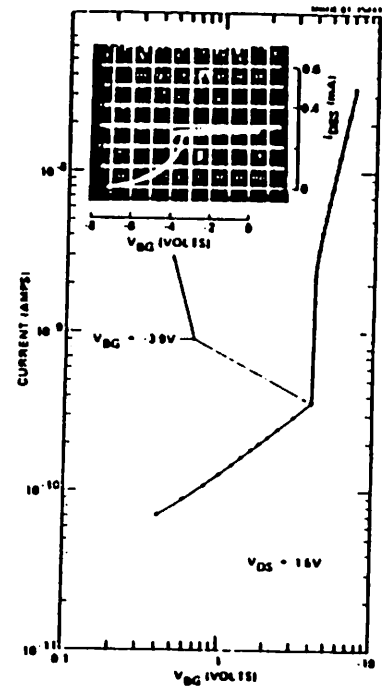


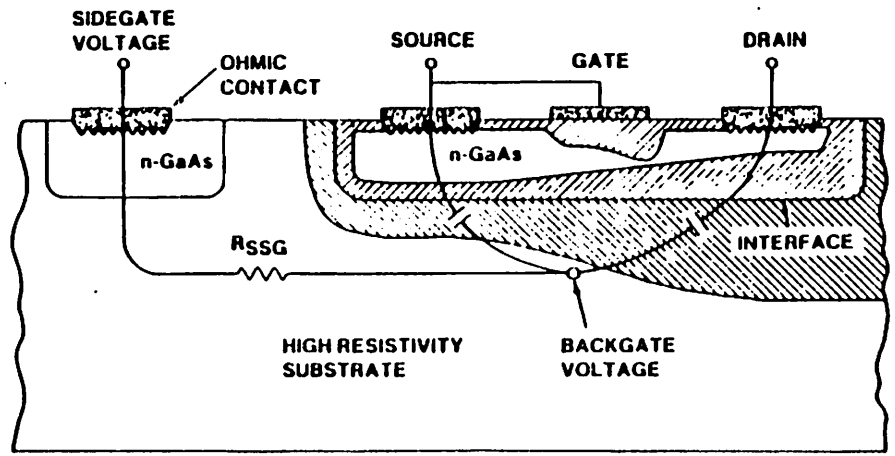
BACKGATING / SIDEGATING

Figure 33



After C.P. Lee et al.





After Goronkin

Appendix 1: FORTRAN source code for fitting program.

Appendix 2: Curve fitting results.

Appendix 3: SPICE simulation results.

```
      PROGRAM INOUT
C #1000

      INTEGER NCUR,NPT,TEMP
      DIMENSION EID(15,50),IID(15,50),ISTART(15)
      DIMENSION VG(15), VD(50), VDI(15,50),TEMP(5)
      REAL*8 VGMAX, VGMIN, VDMAX, VDMIN, VGSTEP, VDSTEP
      REAL*8 VG, VD, VDI, EID, IID, RG, RD, RS
      REAL*8 VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
      CHARACTER*20 fname
      COMMON /RECORD/ EID,IID,VD,VDI,VG
      COMMON /STAT/ ISTART,NCUR,NPT,RG,RD,RS
      COMMON /PARAS/ VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
      DATA fname/' '/
C-----------------------------------------

C PROMPT USER FOR FILENAME.
C FILENAME REQUESTED AT RUNTIME.

C OPEN A FILE TO READ    OPEN(7,FILE=' ')

C READ INPUT INFOMATION.
      READ(7,*,END=1010,ERR=1020)RG,RD,RS
      READ(7,*,END=1010,ERR=1020)VGMAX,VGMIN,VGSTEP
      READ(7,*,END=1010,ERR=1020)VDMAX,VDMIN,VDSTEP

C SET THE BIAS VALUES OF VGS
      I=1
      VG(1)=VGMIN
      NCUR=1
1030  I=I+1
      IF(VGMAX-(VG(I-1)+VGSTEP))1040,1050,1050
1050  VG(I)=VG(I-1)+VGSTEP
      NCUR=NCUR+1
      GO TO 1030
1040  IF(DABS(VGMAX-VG(I-1)-VGSTEP).LT.0.01)GO TO 1050

C  SET THE BIAS VALUES OF VDS
      I=1
      VD(1)=VDMIN
      NPT=1
1060  I=I+1
      IF(VDMAX-(VD(I-1)+VDSTEP))1070,1080,1080
1080  VD(I)=VD(I-1)+VDSTEP
      NPT=NPT+1
      GO TO 1060
1070  IF(DABS(VDMAX-VD(I-1)-VDSTEP).LT.0.01)GO TO 1080

      DO 1090 J=1,NCUR
C READ BACK THE VGS BIAS VALUES
      WRITE(8,1100)VG(J)
1100  FORMAT(6X,'VG= ',G10.4)
```

```
      READ(7,*,END=1010,ERR=1020)(EID(J,I),I=1,NPT)
C READ BACK THE Ids CURRENT VALUES.
      WRITE(8,'(A)')'       Vds (V)      MEASURE Ids (A)   '
      WRITE(8,'(A)')'      ---------    ----------------- '
      WRITE(8,1110)(VD(I),EID(J,I),I=1,NPT)
1110  FORMAT(6X,G10.4,5X,G10.4)
1090  continue


C    CALL THE SUBROUTINE TO ADJUST THE DATA
      CALL COMP(NCUR)
      CALL OPTI(NCUR)
      CALL MEASII(NCUR)
      CALL OPTII(NCUR)
      CALL MEASII(NCUR)
      STOP

1010  WRITE(*,'(A)')' ** END OF FILE ** '
      STOP
1020  WRITE(*,'(A)')'** EEROR I/O ** '
      STOP
      END
```

```
      SUBROUTINE COMP(K)
C THE VALUE OF ' NCUR ' IS THE CURVE NUMBER.
C #2000

      DIMENSION EID(15,50),IID(15,50)
      DIMENSION VG(15),VD(50), VDI(15,50),ISTART(15)
      INTEGER NCUR, NPT, BPT,ISTART,J
      REAL*8 EID,IID,VG,VD,VG2,VDI
      REAL*8 GM,RG,RD,RS
      COMMON /RECORD/ EID,IID,VD,VDI,VG
      COMMON /STAT/ ISTART,NCUR,NPT,RG,RD,RS

C ----------------------------------------
C THE CURVE NUMBER IS ' J '.
C AS LONG AS THE GATE NOT FORWARD BIAS
C ' VGS-VDS<0.4 AND VGS<0.6  ' DO THE
C ADJUSTMENT ON VGS.
      DO 2000 J=1,NCUR
      DO 2010 I=1,NPT
        IF(VG(J)-VD(I).GT.0.4)GO TO 2020
        IF(VG(J).GT.0.6)GO TO 2020
C TEMPORARY STORAGE OF VGS'
        VG2=VG(J)-(EID(J,I)*RS)
        VDI(J,I)=VD(I)-(EID(J,I)*RS+EID(J,I)*RD)
C FIND THE ' GM ' OF BIAS POINT.
C AVERAGE OF THE CHANGE IN ' IDS ' DIVIDED BY
C THE CHANGE IN ' VGS '.

        IF(J.EQ.1)GO TO 2030
        IF(J.EQ.NCUR)GO TO 2040
        GM=(EID(J+1,I)-EID(J-1,I))/(VG(J+1)-VG(J-1))
        IID(J,I)=(1+GM*RS)*EID(J,I)
        GO TO 2010
2030    GM=(EID(J+1,I)-EID(J,I))/(VG(J+1)-VG(J))
        IID(J,I)=(1+GM*RS)*EID(J,I)
        GO TO 2010
2040    GM=(EID(J,I)-EID(J-1,I))/(VG(J)-VG(J-1))
        IID(J,I)=(1+GM*RS)*EID(J,I)
        GO TO 2010
2020    BPT=I
2010    CONTINUE

      ISTART(J)=BPT+1
C ----------------------------------------------------
2000  CONTINUE
      RETURN
      END
```

```
      SUBROUTINE OPTI(K)
C THE VALUE OF ' NCUR ' IS THE CURVE NUMBER.
C #3000

      DIMENSION EID(15,50),IID(15,50)
      DIMENSION VG(15),VD(50), VDI(15,50),ISTART(15)
      DIMENSION REGI(15),REGII(15)
      DIMENSION ERROR(3,3,3,3),ERROR2(3,3,3,3),ERROR3(3,3,3,3)
      INTEGER NCUR, NPT,ISTART,ITER
      INTEGER I,II,J,K,K1,K2,K3,K4
      INTEGER CNT,PCNT,IB,JB,KB,LB
      INTEGER REGI,REGII,IMOVE,CLICK
      REAL*8 EID,IID,VG,VD,VG2,VDI
      REAL*8 GM,RG,RD,RS,MINERR,MERR,ERRSUM
      REAL*8 VT,BETA,LAMBDA,ALPHA,B,DEV,TEMDEV,KVOLT
     1REAL*8 VTSTP,BESTP,LAMSTP,ALSTP,BSTP
      REAL*8 TEMB,TEMBE,TEMLAB,TEMVT,TEMAL
      REAL*8 ICAL,ERROR,ERROR2,ERROR3
      COMMON /RECORD/ EID,IID,VD,VDI,VG
      COMMON /STAT/ ISTART,NCUR,NPT,RG,RD,RS
      COMMON /PARAS/ VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
      COMMON /STAT2/ REGI,REGII,MINERR
C ------------------------------------------------------

      READ(7,*)VT,BETA,LAMBDA,ALPHA,B
      WRITE(8,'(A)')' ----------------------------------------- '
      WRITE(8,'(A)')' INITIAL VALUES FOR VT,BEAT,LAMBDA,ALPHA,B: '
      WRITE(8,3000)VT,BETA,LAMBDA,ALPHA,B
3000  FORMAT(2X,'VT=',G10.4,2X,'BETA=',G10.4,2X,'LAMBDA=',
      1G10.4,2X,'ALPHA=',G10.4,8X,'      B=',G10.4)
      WRITE(8,'(A)')' ----------------------------------------- '

      READ(7,*)DEV
      READ(7,*)KVOLT
      WRITE(*,'(A)')' **** PLEASE WAIT **** '

C ----------------------------------------------
C  DIVIDE THE I-V CURVE INTO THEIR TWO REGIONS
C  OF OPERATION. REGION I=[Vds <= Vgs + Vt]
C  REGION II=[Vds => Vgs + Vt].

      DO 3010 J=1,NCUR
      CNT=0
      DO 3020 I=ISTART(J),NPT
      IF(VDI(J,I).LE.(3.0/ALPHA))CNT=CNT+1
3020  CONTINUE
      REGI(J)=CNT-1
      REGII(J)=CNT+1
3010  CONTINUE

C ------------------------------------------
C  DEFINE THE STEP SIZE OF THE VARIABLES.
C  MAXIMUM INCREMENT OF <+,-> 10 STEPS.
C
```

```
      ITER=0
      MINERR=1.0E30
      TEMDEV=DEV
C  ----------------------------------------
C   THIS IS WERE REITERATION RETURNS TO.
C

3190  ITER=ITER+1
      VTSTP=TEMDEV*VT/2000.0
      BESTP=TEMDEV*BETA/2000.0
      LAMSTP=TEMDEV*LAMBDA/100.0
      ALSTP=TEMDEV*ALPHA/100.0
      BSTP=TEMDEV*B/100.0

C ------------------------------------------------
C  DO A FIT IN REGION II ONLY UP TO KINK VOLTAGE.
C  ASSUME A FIX Vt VOLTATGE.
C  REGION II DOES NOT HAVE ALPHA EXPRESSION.
C

C7  ---------------------------------
      DO 3090 II=1,100
        TEMB=B-BSTP
        TEMBE=BETA-BESTP
        TEMLAM=LAMBDA-LAMSTP
        TEMVT=VT-VTSTP

C6  ---------------------------------
      DO 3080 K1=1,3
C5  ---------------------------------
      DO 3070 K2=1,3
C4  ---------------------------------
      DO 3060 K3=1,3
C3  ---------------------------------
      DO 3050 K4=1,3
      ERROR(K1,K2,K3,K4)=0
      ERROR2(K1,K2,K3,K4)=0
      ERROR3(K1,K2,K3,K4)=0
      PCNT=0
C2  ---------------------------------
      DO 3040 J=1,NCUR
      IMOVE=(NPT-REGII(J))/4
C1  -----------------------------------
      DO 3030 I=REGII(J),NPT,IMOVE
      IF(ISTART(J).GE.NPT)GO TO 3030
      IF(VDI(J,I).GT.KVOLT)GO TO 3030

        ICAL=TEMBE*((VG(J)-TEMVT)**2)*(1+TEMLAM*VDI(J,I))/
      1     (1+TEMB*(VG(J)-TEMVT))
```

```
ERROR2(K1,K2,K3,K4)=ERROR2(K1,K2,K3,K4)+DABS((IID(J,I)-ICAL)/
     1  IID(J,I))

     ERROR(K1,K2,K3,K4)=ERROR(K1,K2,K3,K4)+
     1 DSQRT((IID(J,I)-ICAL)**2)

     ERROR3(K1,K2,K3,K4)=ERROR3(K1,K2,K3,K4)+
     1 (IID(J,I)-ICAL)

     PCNT=PCNT+1
3030 CONTINUE
C1  ----------------------------------
3040 CONTINUE
C2  ----------------------------------

     TEMLAM=TEMLAM+LAMSTP
3050 CONTINUE
C3  ----------------------------------
     TEMBE=TEMBE+BESTP
3060 CONTINUE
C4  ----------------------------------
     TEMB=TEMB+BSTP
3070 CONTINUE
C5  ----------------------------------
     TEMVT=TEMVT+VTSTP
3080 CONTINUE

C
C   FIND THE BEST MOVE.
C
      IB=1
      JB=1
      KB=1
      LB=1
      CLICK=0
      DO 3130 IB=1,3
      DO 3120 JB=1,3
      DO 3110 KB=1,3
      DO 3100 LB=1,3

      ERRSUM=(ERROR2(IB,JB,KB,LB)/(0.25*PCNT))+
      1          (ERROR(IB,JB,KB,LB)/(0.05E-3*PCNT))+
      1          DABS(ERROR3(IB,JB,KB,LB))/(0.10E-3*PCNT)


      IF(ERRSUM.GT.MINERR)GO TO 3100
      IF(ERRSUM.EQ.MINERR)GO TO 3100
      MINERR=ERRSUM
      K4=LB
      K3=KB
      K2=JB
      K1=IB
```

```
      CLICK=1
3100  CONTINUE
3110  CONTINUE
3120  CONTINUE
3130  CONTINUE

      IF(CLICK.EQ.0)GO TO 3140
      GO TO 3250
3140  WRITE(8,3200)MINERR,PCNT
3200  FORMAT(2X,'MIMIMUM SUM OF ERROR=',G10.4,5X,I5)

C     MERR=(MINERR)/DBLE(PCNT)
C     WRITE(8,3210)MERR,PCNT
C3210      FORMAT(2X,'THE MEAN ERROR PER A POINT=',G10.4,2X,I5)
      GO TO 3240
C
C-----------------------------------------
C CHANGE THE PARAMETER ACCORDINGLY.
C
3250  IF(K1.EQ.1)THEN
       VT=VT-VTSTP
      ELSEIF(K1.EQ.3)THEN
       VT=VT+VTSTP
      ELSE
       VT=1.0*VT
      ENDIF

      IF(K2.EQ.1)THEN
       B=B-BSTP
      ELSEIF(K2.EQ.3)THEN
       B=B+BSTP
      ELSE
       B=1.0*B
      ENDIF

      IF(K3.EQ.1)THEN
       BETA=BETA-BESTP
      ELSEIF(K3.EQ.3)THEN
       BETA=BETA+BESTP
      ELSE
       BETA=1.0*BETA
      ENDIF

      IF(K4.EQ.1)THEN
       LAMBDA=LAMBDA-LAMSTP
      ELSEIF(K4.EQ.3)THEN
       LAMBDA=LAMBDA+LAMSTP
      ELSE
       LAMBDA=1.0*LAMBDA
      ENDIF
3090  CONTINUE
C7   ----------------------------------
```

```
C  ------------------------------------
C  A OPTIMUM HAS BEEN FOUND
C
      WRITE(*,'(A)')' *** MAXIMUM ITERATION *** '
      WRITE(8,3200)MINERR,PCNT
C     MERR=(MINERR)/DBLE(PCNT)
C     WRITE(8,3210)MERR,PCNT
      GOTO 3150
3240  WRITE(*,'(A)')' *** SUCCESS! A OPTIMUM HAS BEEN FOUND *** '
      TEMDEV=(TEMDEV/50.0)

3150  WRITE(8,3160)VT,BETA,LAMBDA
3160  FORMAT(2X,' VT=',G10.4,'   BETA=',G10.4,'   LAMBDA=',G10.4)
      WRITE(8,3170)ALPHA,B
3170  FORMAT(2X,' ALPHA=',G10.4,'     B= ',G10.4)
      IF(MINERR.LE.(2.0))GO TO 3180
      WRITE(*,'(A)')' **** ERROR > 5% ITERATE AGAIN **** '
      IF(ITER.GE.10)GO TO 3180
      GO TO 3190

C #3200-MAXIMUM
3180  RETURN
      END
```

```
      SUBROUTINE OPTII(K)
C THE VALUE OF ' NCUR ' IS THE CURVE NUMBER.
C #4000

      DIMENSION EID(15,50),IID(15,50)
      DIMENSION VG(15),VD(50), VDI(15,50),ISTART(15)
      DIMENSION REGI(15),REGII(15)
      DIMENSION ERROR(3,3,3,3),ERROR2(3,3,3,3),ERROR3(3,3,3,3)
      INTEGER NCUR, NPT,ISTART,ITER
      INTEGER I,II,J,K,K1,K2,K3,K4
      INTEGER CNT,PCNT,IB,JB,KB,LB
      INTEGER REGI,REGII,IMOVE,CLICK
      REAL*8 EID,IID,VG,VD,VG2,VDI
      REAL*8 GM,RG,RD,RS,MINERR,MERR,ERRSUM
      REAL*8 VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
      REAL*8 VTSTP,BESTP,LAMSTP,ALSTP,BSTP
      REAL*8 TEMB,TEMBE,TEMLAB,TEMVT,TEMAL
      REAL*8 ICAL,ERROR,ERROR2,ERROR3
      COMMON /RECORD/ EID,IID,VD,VDI,VG
      COMMON /STAT/ ISTART,NCUR,NPT,RG,RD,RS
      COMMON /PARAS/ VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
      COMMON /STAT2/ REGI,REGII,MINERR
C ------------------------------------------------------


C
C  DEFINE THE STEP SIZE OF THE VARIABLES.
C  MAXIMUM INCREMENT OF <+,-> 10 STEPS.
C


      WRITE(*,'(A)')' ***** OPTIMIZATION II IN PROGRESS ***** '
      WRITE(*,'(A)')' **** PLEASE WAIT **** '
      ITER=0
      MINERR=1.0E30
C  ---------------------------------------
C   THIS IS WERE REITERATION RETURNS TO.
C

4260  ITER=ITER+1
      VTSTP=DEV*VT/1000.0
      BESTP=DEV*BETA/1000.0
      LAMSTP=DEV*LAMBDA/1000.0
      ALSTP=DEV*ALPHA/100.0
      BSTP=DEV*B/1000.0

C ----------------------------------------------
C  DO A FIT IN REGION I,II ONLY UP TO KINK VOLTAGE.
C  ASSUME A FIX VALUE FOR BETA,LAMBDA,B.
C  FIND THE LINEAR REGION FINAL POINT.
C
```

```
      DO 4000 J=1,NCUR
        CNT=0
        DO 4010 I=1,NPT


          IF(VDI(J,I).GT.(3.0/ALPHA))GO TO 4010
          CNT=CNT+1
4010    CONTINUE
        REGI(J)=CNT
4000  CONTINUE

C  ---------------------------------------------
C  FIND THE POINT WERE KINK VOLTAGE COME INTO PLAY
C
      DO 4020 J=1,NCUR
       CNT=0
       DO 4030 I=1,NPT
        IF(VDI(J,I).GT.KVOLT)GO TO 4030
        CNT=CNT+1
4030   CONTINUE
       REGII(J)=CNT
4020  CONTINUE

C7  --------------------------
      DO 4100 II=1,100
        TEMAL=ALPHA-ALSTP

C6  --------K1=ALPHA-------------
      DO 4090 K1=1,3
C5  --------K2=BETA--------------
      DO 4080 K2=1,3


C4  --------K3=LAMBDA------------
      DO 4070 K3=1,3
C3  --------K4=B-----------------
      DO 4060 K4=1,3

      ERROR(K1,K2,K3,K4)=0.0
      ERROR2(K1,K2,K3,K4)=0.0
      ERROR3(K1,K2,K3,K4)=0.0
      PCNT=0
C2  --------------------------
      DO 4050 J=1,NCUR
      IMOVE=(REGII(J)-ISTART(J))/8
C1  ---------------------------
      DO 4040 I=ISTART(J),REGII(J),IMOVE
      IF(ISTART(J).GE.NPT)GO TO 4040
      IF(I.GT.REGI(J))GO TO 4110

C       **** LINEAR REGION ****
        ICAL=(BETA*((VG(J)-VT)**2)*(1+LAMBDA*VDI(J,I))
     1     *(1-(1-(TEMAL*VDI(J,I)/3))**3))/(1+B*(VG(J)-VT))
```

```
ERROR2(K1,K2,K3,K4)=ERROR2(K1,K2,K3,K4)+DABS((IID(J,I)-ICAL)/
     1     IID(J,I))


        ERROR(K1,K2,K3,K4)=ERROR(K1,K2,K3,K4)+DABS(IID(J,I)-ICAL)

        ERROR3(K1,K2,K3,K4)=ERROR3(K1,K2,K3,K4)+(IID(J,I)-ICAL)

        PCNT=PCNT+1
        GO TO 4040


C       **** SATURATION REGION ****
4110    ICAL=BETA*((VG(J)-VT)**2)*(1+LAMBDA*VDI(J,I))/
     1     (1+B*(VG(J)-VT))


ERROR2(K1,K2,K3,K4)=ERROR2(K1,K2,K3,K4)+DABS((IID(J,I)-ICAL)/
     1     IID(J,I))


        ERROR(K1,K2,K3,K4)=ERROR(K1,K2,K3,K4)+DABS(IID(J,I)-ICAL)

        ERROR3(K1,K2,K3,K4)=ERROR3(K1,K2,K3,K4)+(IID(J,I)-ICAL)

        PCNT=PCNT+1
4040 CONTINUE
4050 CONTINUE

C1  ------------------------------------
C2  ------------------------------------
     TEMB=TEMB+BSTP
4060 CONTINUE
C3  -------------------------------------
     TEMLAM=TEMLAM+LAMSTP
4070 CONTINUE
C4  --------------------------------
     TEMAL=TEMAL+ALSTP
4080 CONTINUE
C5  --------------------------------
     TEMBE=TEMBE+BESTP
4090 CONTINUE
C6  --------------------------------


C
C   FIND THE BEST MOVE.
C
```

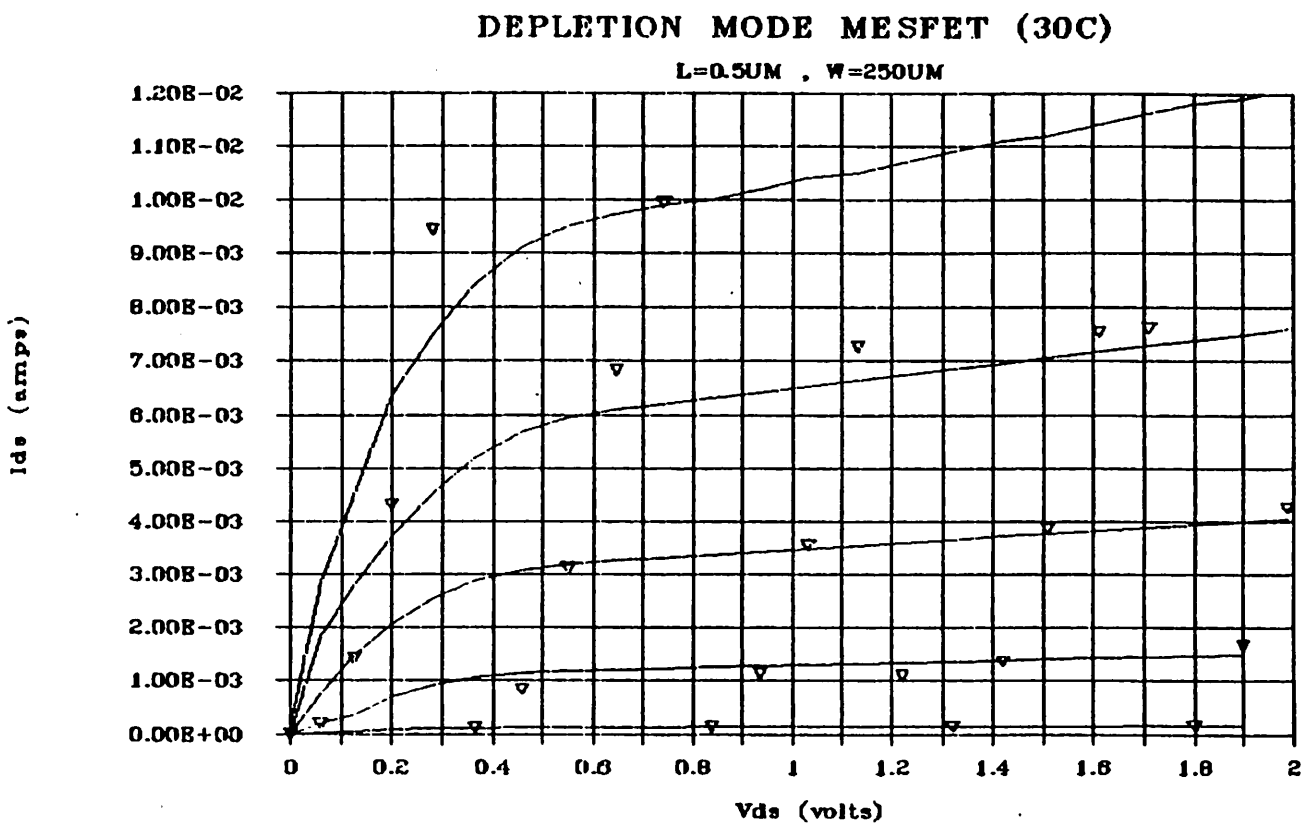
```
      IB=1
      JB=1
      KB=1
      LB=1
      CLICK=0
      DO 4150 IB=1,3
      DO 4140 JB=1,3
      DO 4130 KB=1,3
      DO 4120 LB=1,3

      ERRSUM=(ERROR2(IB,JB,KB,LB)/(1.50*PCNT))+
      1          (ERROR(IB,JB,KB,LB)/(0.1E-3*PCNT))+
      1          DABS(ERROR3(IB,JB,KB,LB))/(0.10E-3*PCNT)


        IF(ERRSUM.GT.MINERR)GO TO 4120
        IF(ERRSUM.EQ.MINERR)GO TO 4120
        MINERR=ERRSUM
        K4=LB
        K3=KB
        K2=JB
        K1=IB
        CLICK=1

4120  CONTINUE
4130  CONTINUE
4140  CONTINUE
4150  CONTINUE

      IF(CLICK.EQ.0)GO TO 4160
      GO TO 4170
4160  WRITE(8,4200)MINERR,PCNT
4200  FORMAT(2X,'MIMIMUM SUM OF SQUARE ERROR=',G10.4,5X,I5)


C     MERR=(MINERR)/DBLE(PCNT)
C     WRITE(8,4210)MERR,PCNT
C4210     FORMAT(2X,'THE      MEAN      DEVIATION      PER      A
POINT=',G10.4,2X,I5)
      GO TO 4250

C-----------------------------------
C CHANGE THE PARAMETER ACCORDINGLY.
C
4170  IF(K4.EQ.1)THEN
        B=1.0*B
C       B=B-BSTP
      ELSEIF(K4.EQ.3)THEN
        B=1.0*B
C       B=B+BSTP
      ELSE
```

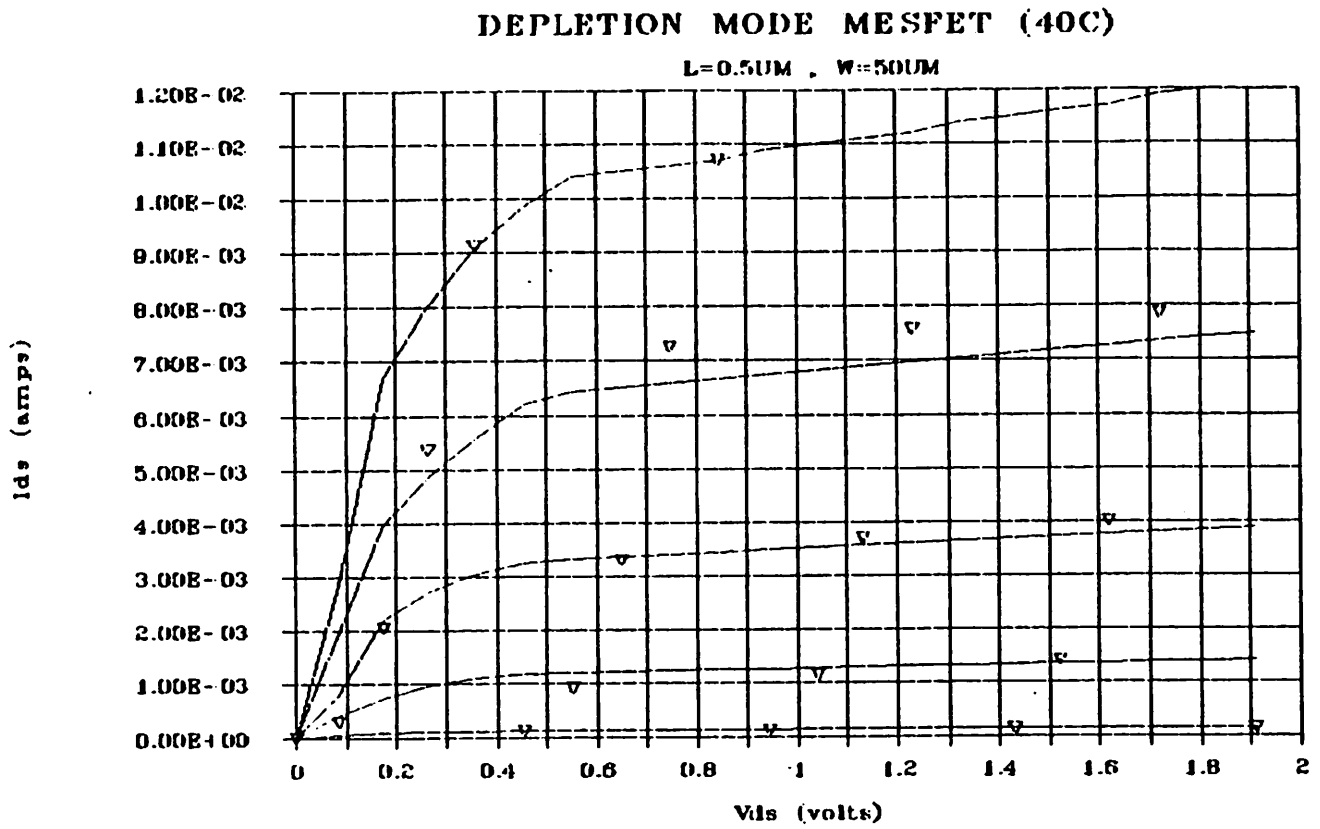
```
      B=1.0*B
     ENDIF

     IF(K3.EQ.1)THEN
      LAMBDA=1.0*LAMBDA
C     LAMBDA=LAMBDA-LAMSTP
     ELSEIF(K3.EQ.3)THEN
      LAMBDA=1.0*LAMBDA
C     LAMBDA=LAMBDA+LAMSTP
     ELSE
      LAMBDA=1.0*LAMBDA
     ENDIF



     IF(K2.EQ.1)THEN
      BETA=1.0*BETA
C     BETA=BETA-BESTP
     ELSEIF(K2.EQ.3)THEN
      BETA=1.0*BETA
C     BETA=BETA+BESTP
     ELSE
      BETA=1.0*BETA
     ENDIF

     IF(K1.EQ.1)THEN
      ALPHA=ALPHA-ALSTP
     ELSEIF(K1.EQ.3)THEN
      ALPHA=ALPHA+ALSTP
     ELSE
      ALPHA=1.0*ALPHA
     ENDIF
4100 CONTINUE
C5  ------------------------------------

C  A OPTIMUM HAS BEEN FOUND
C
     WRITE(*,'(A)')' *** MAXIMUM ITERATION *** '
     WRITE(8,4200)MINERR,PCNT
C    MERR=(MINERR)/DBLE(PCNT)
C    WRITE(8,4210)MERR,PCNT
     GOTO 4270
4250 WRITE(*,'(A)')' *** SUCCESS! A OPTIMUM HAS BEEN FOUND *** '
     DEV=(DEV/100.0)

4270 WRITE(8,4280)VT,BETA,LAMBDA
4280 FORMAT(2X,' VT=',G10.4,'   BETA=',G10.4,'   LAMBDA=',G10.4)
     WRITE(8,4180)ALPHA,B
4180 FORMAT(2X,' ALPHA=',G10.4,'     B= ',G10.4)
     IF(MINERR.LE.(2.00))GO TO 4190
     WRITE(*,'(A)')' **** ERROR > 5% ITERATE AGAIN **** '
     IF(ITER.GE.10)GO TO 4190
     GO TO 4260
```

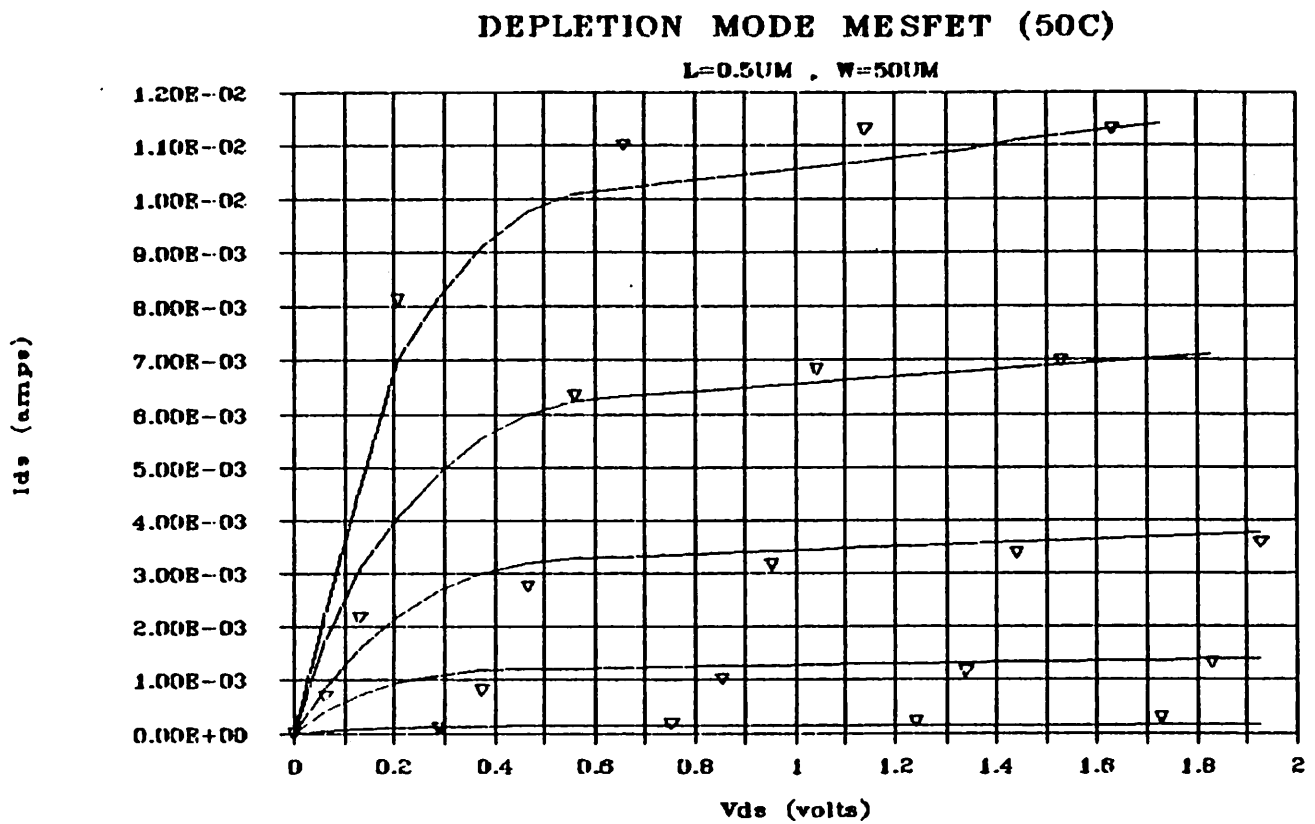
```
C #4300-MAXIMUM
4190 RETURN
     END
```

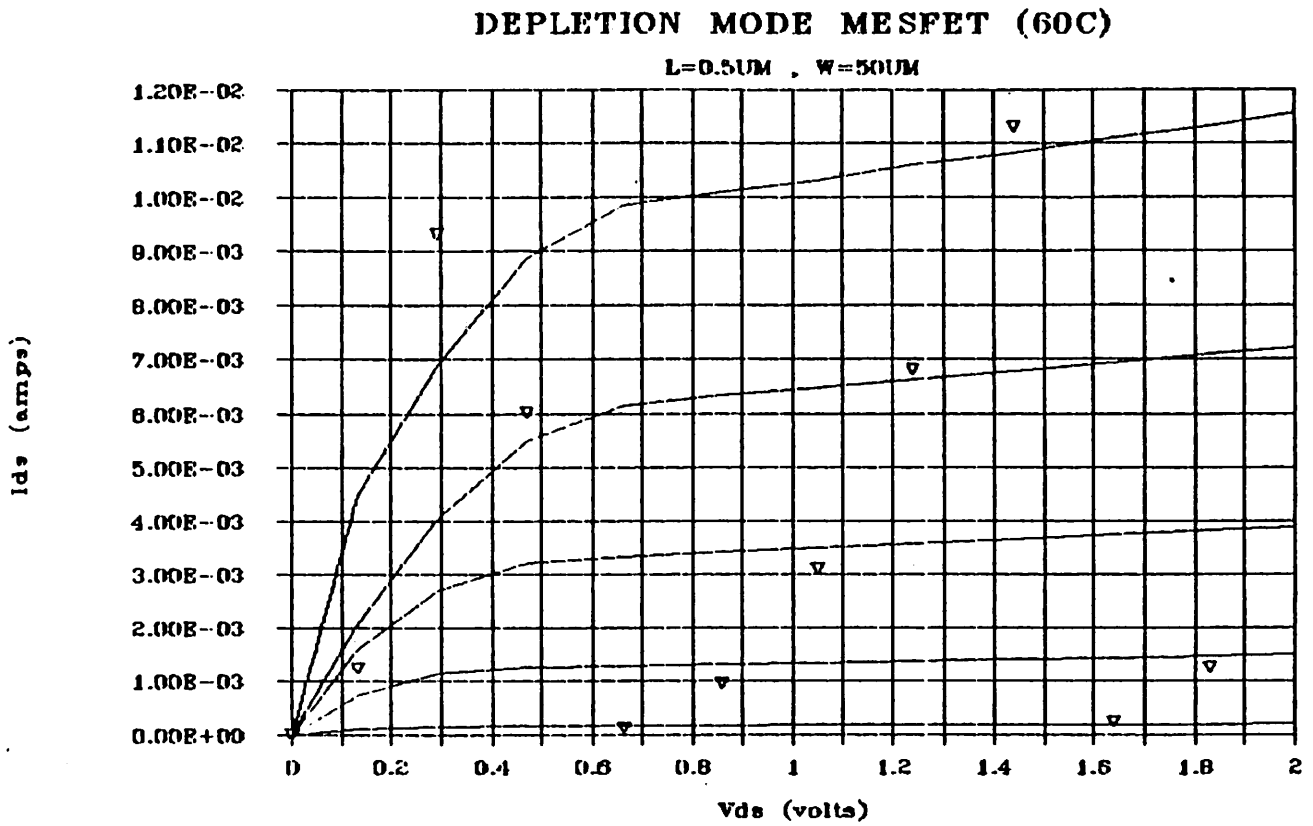
```
      SUBROUTINE MEASII(K)
C THE VALUE OF ' NCUR ' IS THE CURVE NUMBER.
C #4000

      DIMENSION EID(15,50),IID(15,50),ICAL(15,50)
      DIMENSION VG(15),VD(50), VDI(15,50),ISTART(15)
      DIMENSION REGI(15),REGII(15),ERROR(15,50)
      INTEGER NCUR, NPT,ISTART
      INTEGER I,J,CNT,PCNT,REGI,REGII
      REAL*8 EID,IID,VG,VD,VDI
      REAL*8 GM,RG,RD,RS,MINERR,MERR
      REAL*8 VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
      REAL*8 ICAL,ERROR
      COMMON /RECORD/ EID,IID,VD,VDI,VG
      COMMON /STAT/ ISTART,NCUR,NPT,RG,RD,RS
      COMMON /PARAS/ VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
      COMMON /STAT2/ REGI,REGII,MINERR
C ---------------------------------------------------


C
C  DEFINE THE STEP SIZE OF THE VARIABLES.
C  MAXIMUM INCREMENT OF <+,-> 10 STEPS.
C
      WRITE(*,'(A)')' **** PLEASE WAIT **** '

C
C
      DO 4000 J=1,NCUR
        CNT=0
        DO 4010 I=1,NPT
          IF(VDI(J,I).GT.(3.0/ALPHA))GO TO 4010
          CNT=CNT+1
4010    CONTINUE
        REGI(J)=CNT
4000  CONTINUE


C  ------------------------------------------------
C  FIND THE POINT WERE KINK VOLTAGE COME INTO PLAY
C
      DO 4020 J=1,NCUR
       CNT=0
       DO 4030 I=1,NPT
        IF(VDI(J,I).GT.KVOLT)GO TO 4030
        CNT=CNT+1
4030   CONTINUE
       REGII(J)=CNT
4020  CONTINUE
```

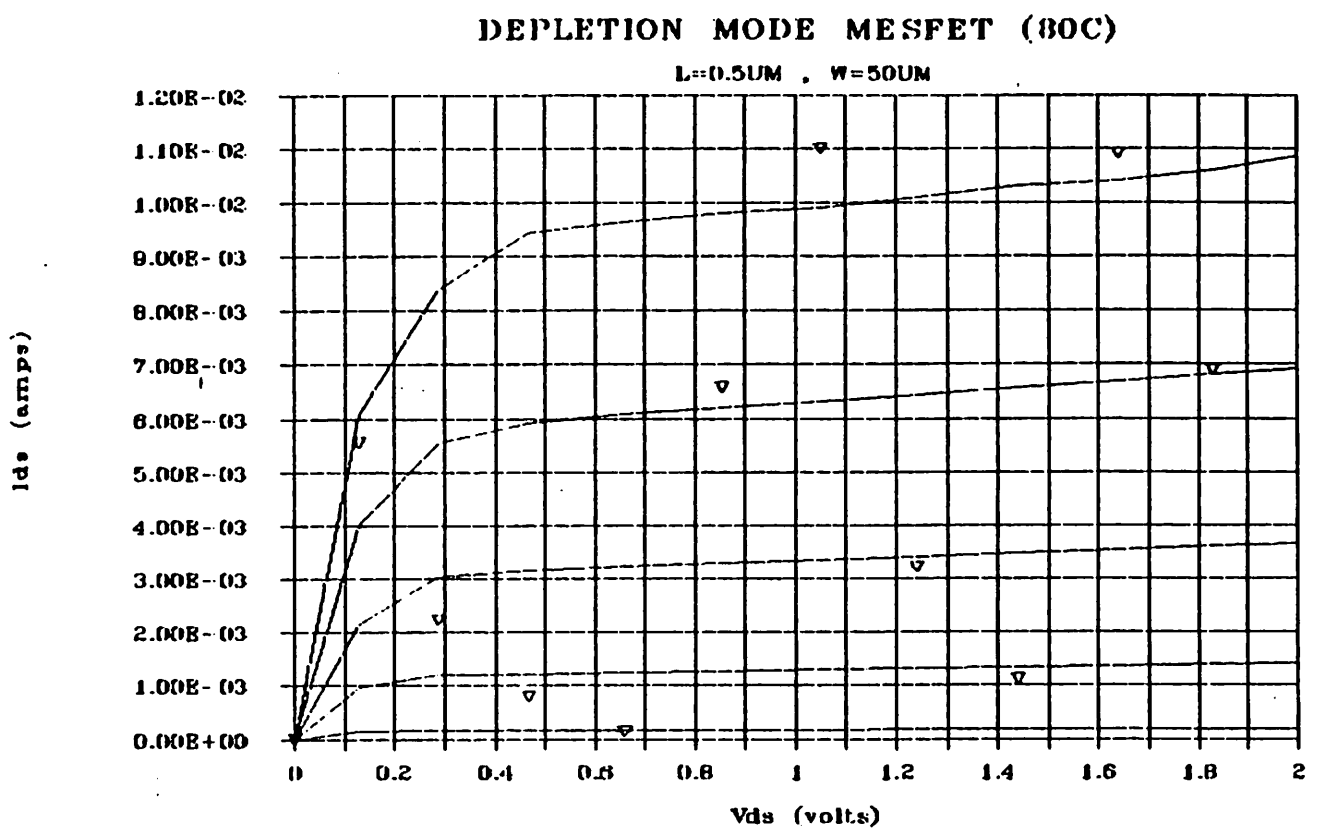
```
C  ----------------------------------------
C CALCULATE THE I-V CURRENTS AND DETERMINE
C ERROR.

C2  --------------------------
     DO 4050 J=1,NCUR
C1  ---------------------------
     DO 4040 I=ISTART(J),REGII(J)
     IF(ISTART(J).GE.NPT)GO TO 4040
     IF(I.GT.REGI(J))GO TO 4090


C       **** LINEAR REGION ****
        ICAL(J,I)=(BETA*((VG(J)-VT)**2)*(1+LAMBDA*VDI(J,I))
     1     *(1-(1-(ALPHA*VDI(J,I)/3))**3))/(1+B*(VG(J)-VT))
        ERROR(J,I)=DABS((IID(J,I)-ICAL(J,I))/
     1     IID(J,I))
        GO TO 4040
C       **** SATURATION REGION ****
4090    ICAL(J,I)=BETA*((VG(J)-VT)**2)*(1+LAMBDA*VDI(J,I))/
     1     (1+B*(VG(J)-VT))
        ERROR(J,I)=DABS((IID(J,I)-ICAL(J,I))/
     1     IID(J,I))
4040 CONTINUE
4050 CONTINUE
C1  -----------------------------------
C2  -----------------------------------

C  ---------------------------------------
C  WRITE OUT THE EXTERNAL, INTERNAL, AND
C  CALCULATED CURRENT.

     WRITE(8,'(A)')' ------------------------------------------ '
     DO 4100 J=1,NCUR
        IF(ISTART(J).GE.REGII(J))GO TO 4100
        WRITE(8,4110)VG(J),ISTART(J)
4110    FORMAT(5X,'VG= ',G10.4,3X,'ISTART= ',I7)

     WRITE(8,'(A)')'        Vds  (V)         COMPENSATED  Ids(A)
CALCULATED Ids
     1(A)    PERCENT ERROR '
     WRITE(8,'(A)')'          ---------      -------------------
--------------
     1---    -------------- '
        WRITE(8,4120)(VDI(J,I),IID(J,I),ICAL(J,I),
     1 ERROR(J,I),I=ISTART(J),REGII(J))

4120    FORMAT(3X,G10.4,6X,G10.4,12X,G10.4,9X,G10.4)

4100 CONTINUE
C #4200
     RETURN
     END
```

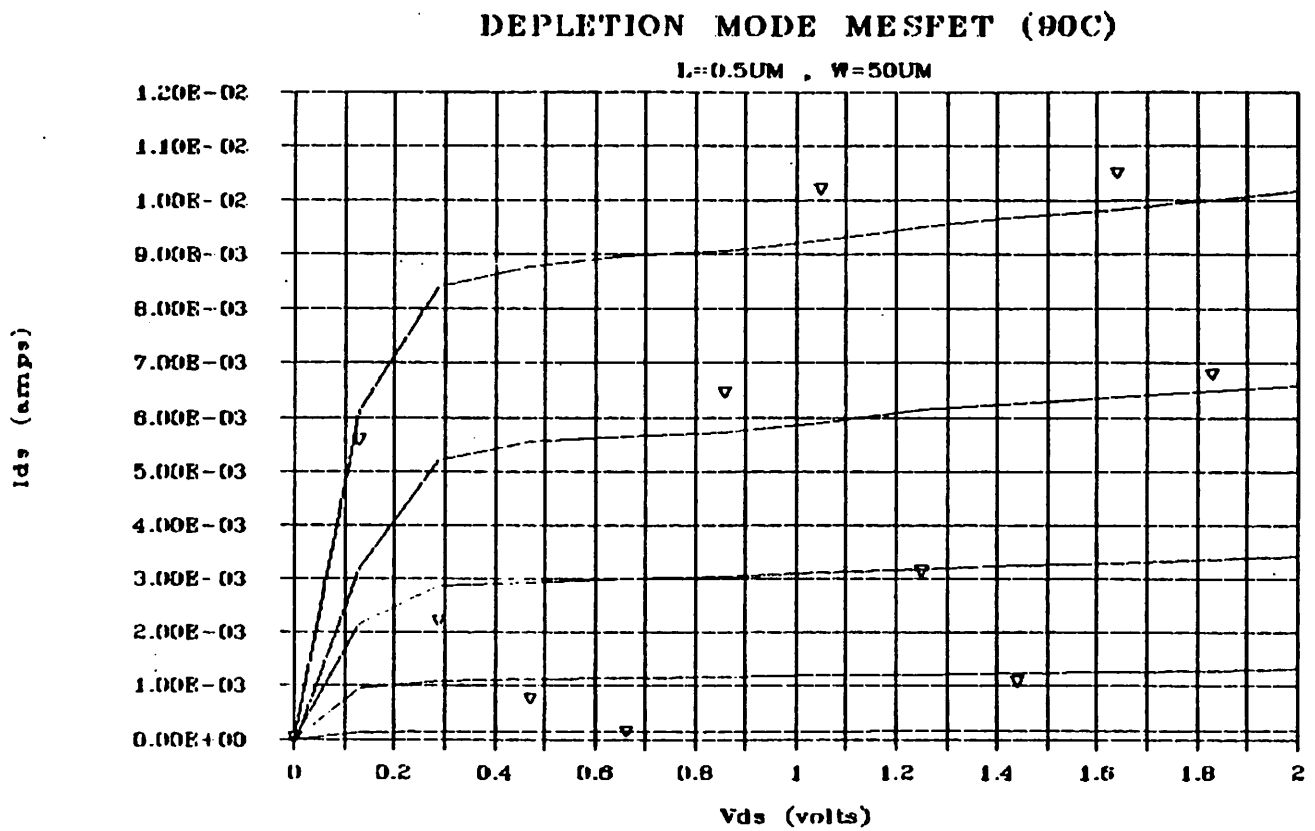

DEPLETION MODE MESFET (30C)
L=0.5UM , W=250UM
Ids (amps)
1.20E-02
1.10E-02
1.00E-02
9.00E-03
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)

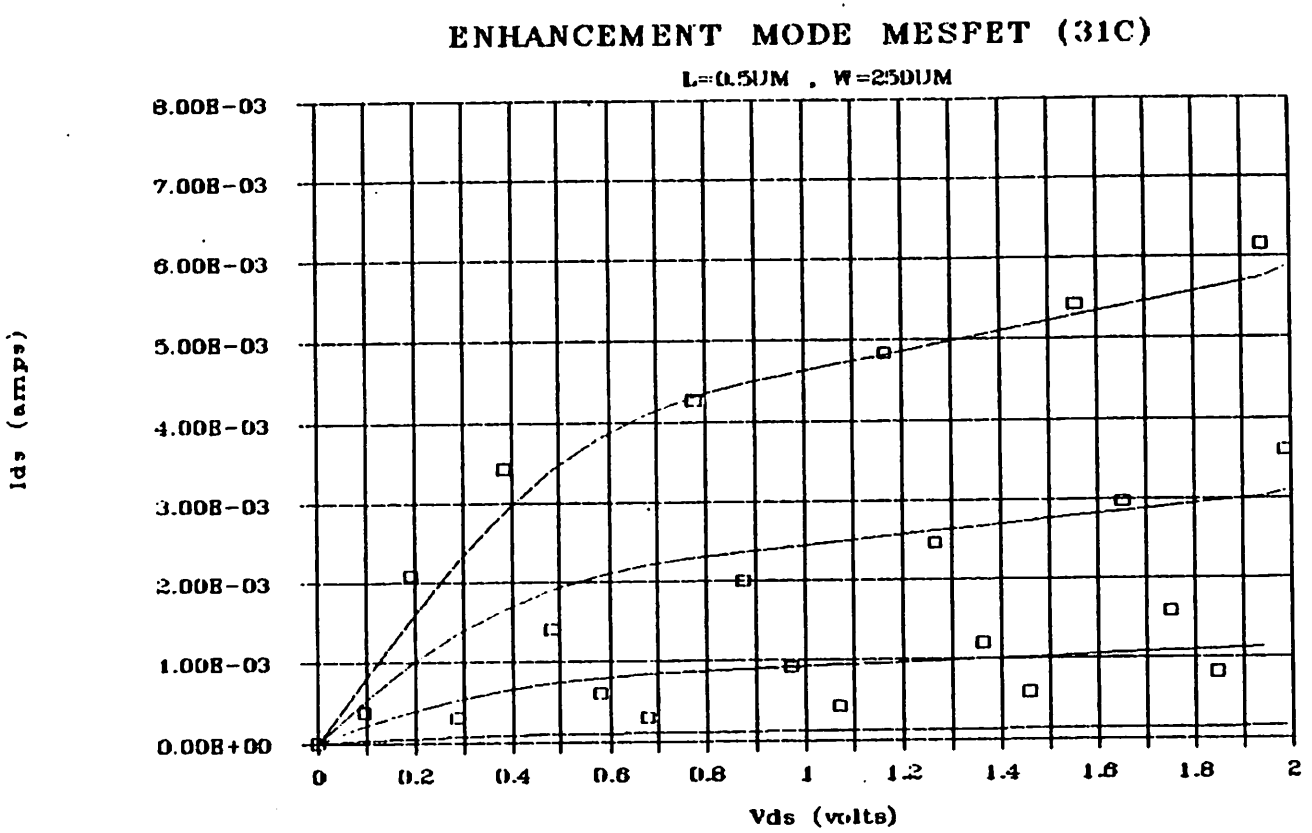

DEPLETION MODE MESFET (40C)
L=0.5UM , W=50UM
1.20E-02
1.10E-02
1.00E-02
9.00E-03
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)

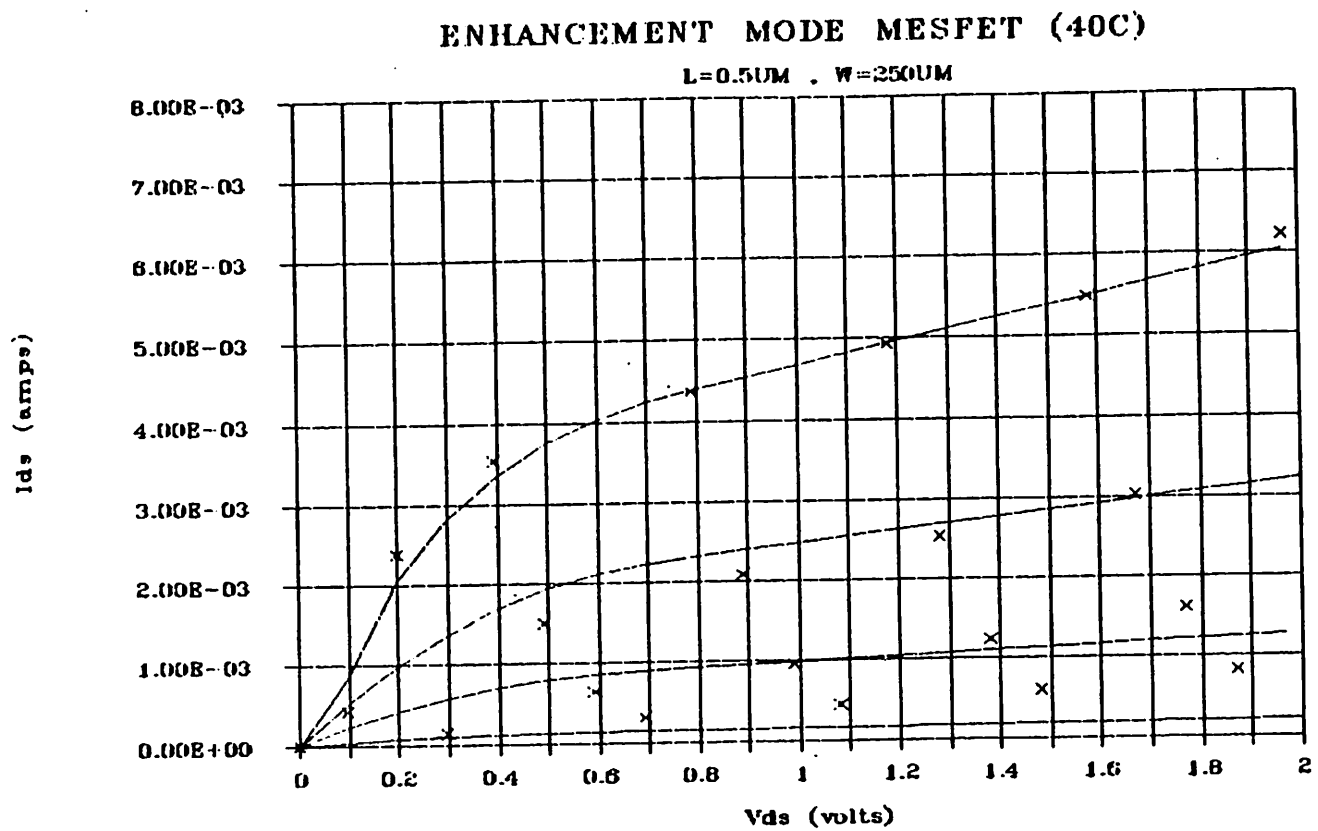

DEPLETION MODE MESFET (50C)
L=0.5UM , W=50UM
1.20E-02
1.10E-02
1.00E-02
9.00E-03
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)

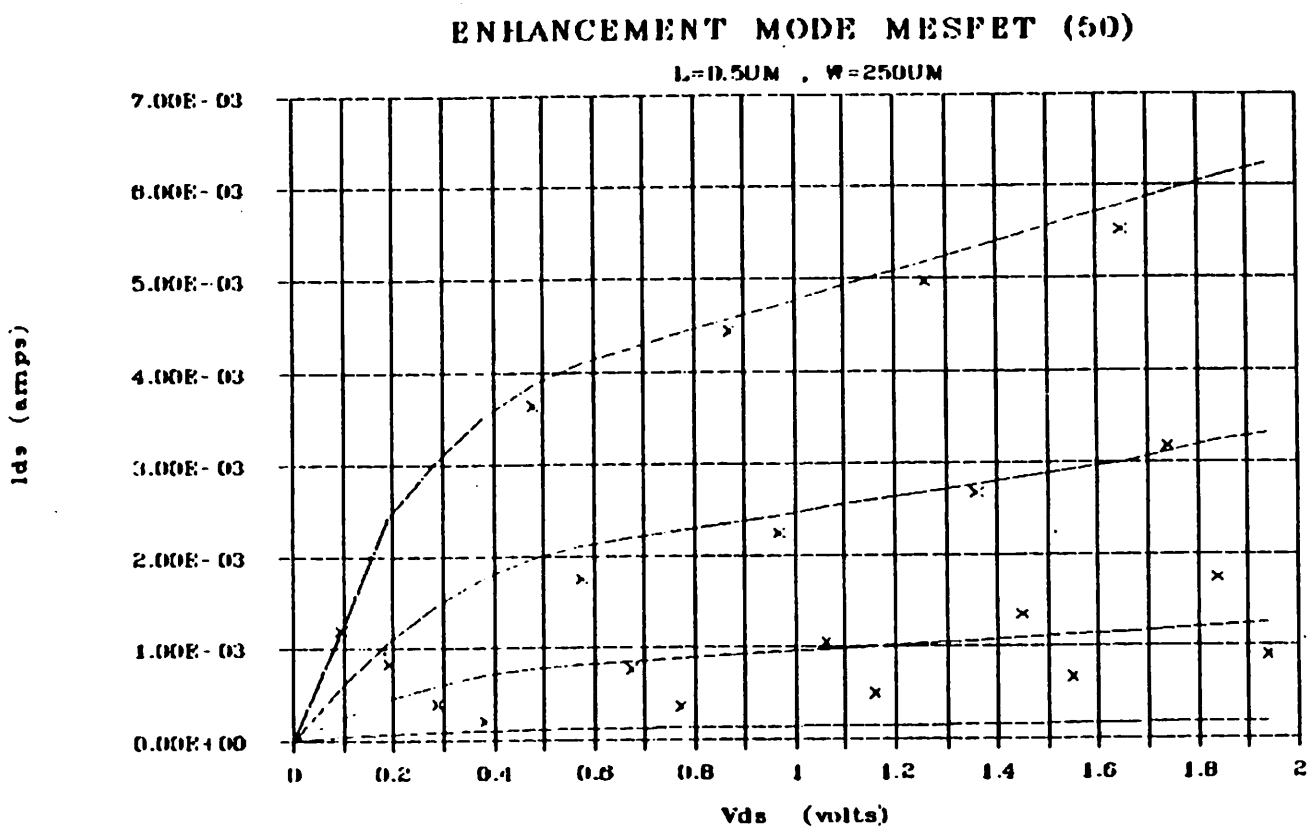

DEPLETION MODE MESFET (60C)
L=0.5UM , W=50UM
1.20E-02
1.10E-02
1.00E-02
9.00E-03
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)

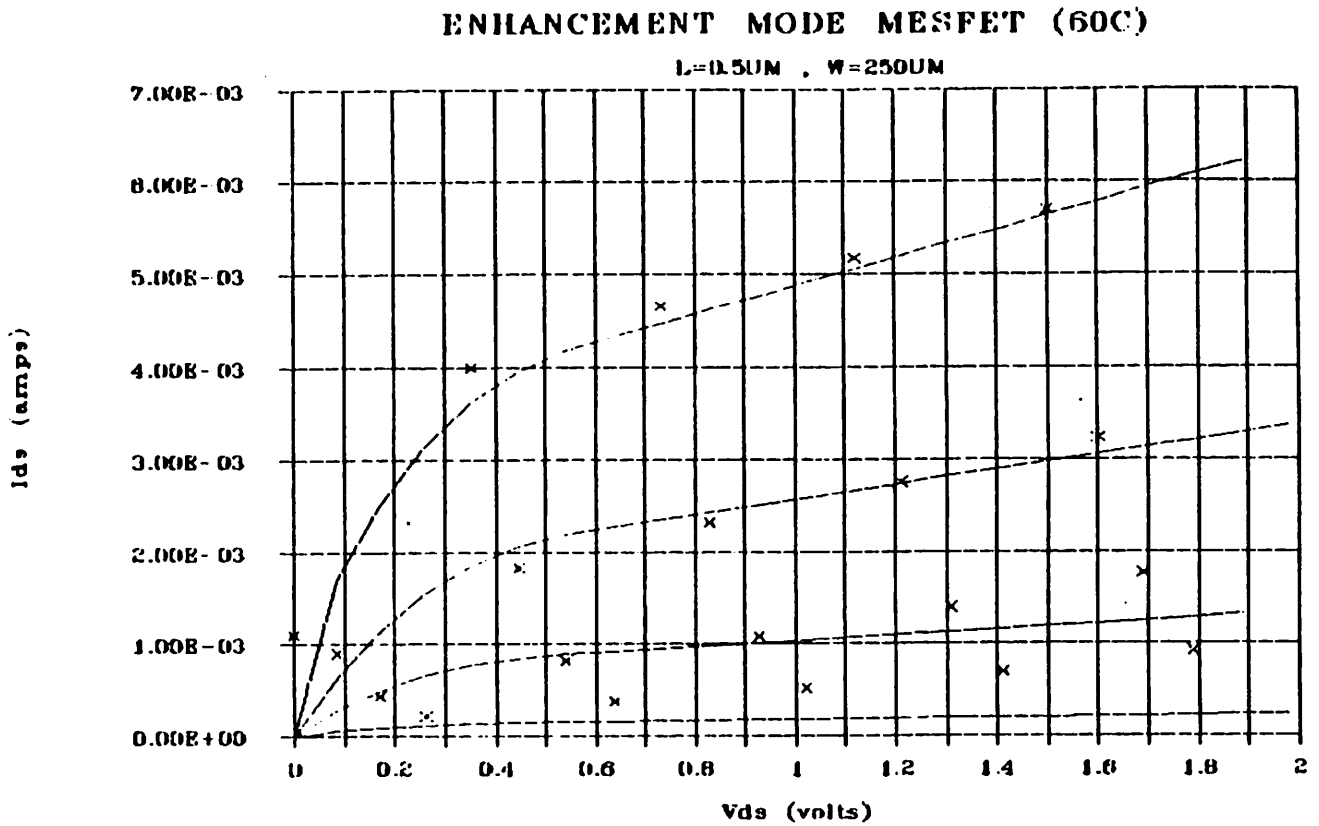

DEPLETION MODE MESFET (80C)
L=0.5UM , W=50UM
1.20E-02
1.10E-02
1.00E-02
9.00E-03
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)

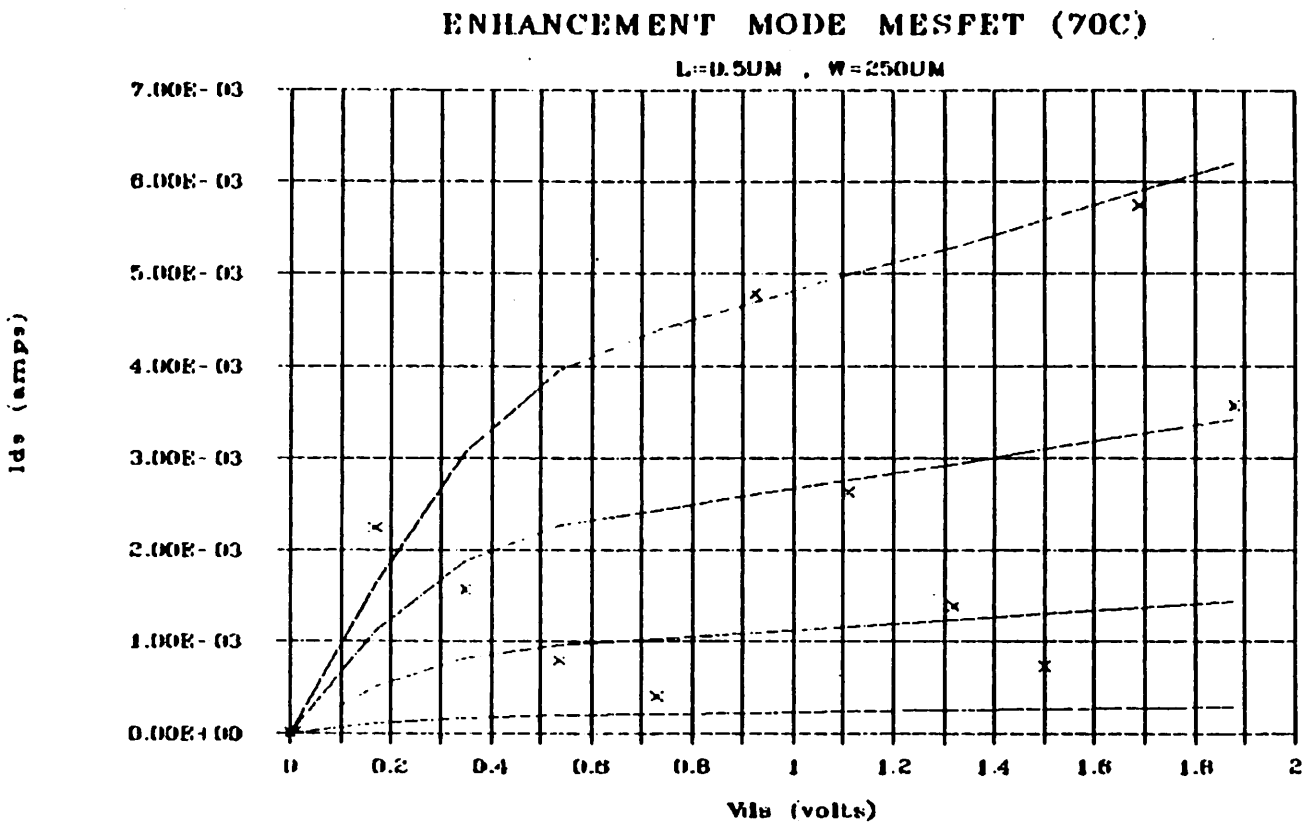

DEPLETION MODE MESFET (90C)
L=0.5UM , W=50UM
1.20E-02
1.10E-02
1.00E-02
9.00E-03
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)

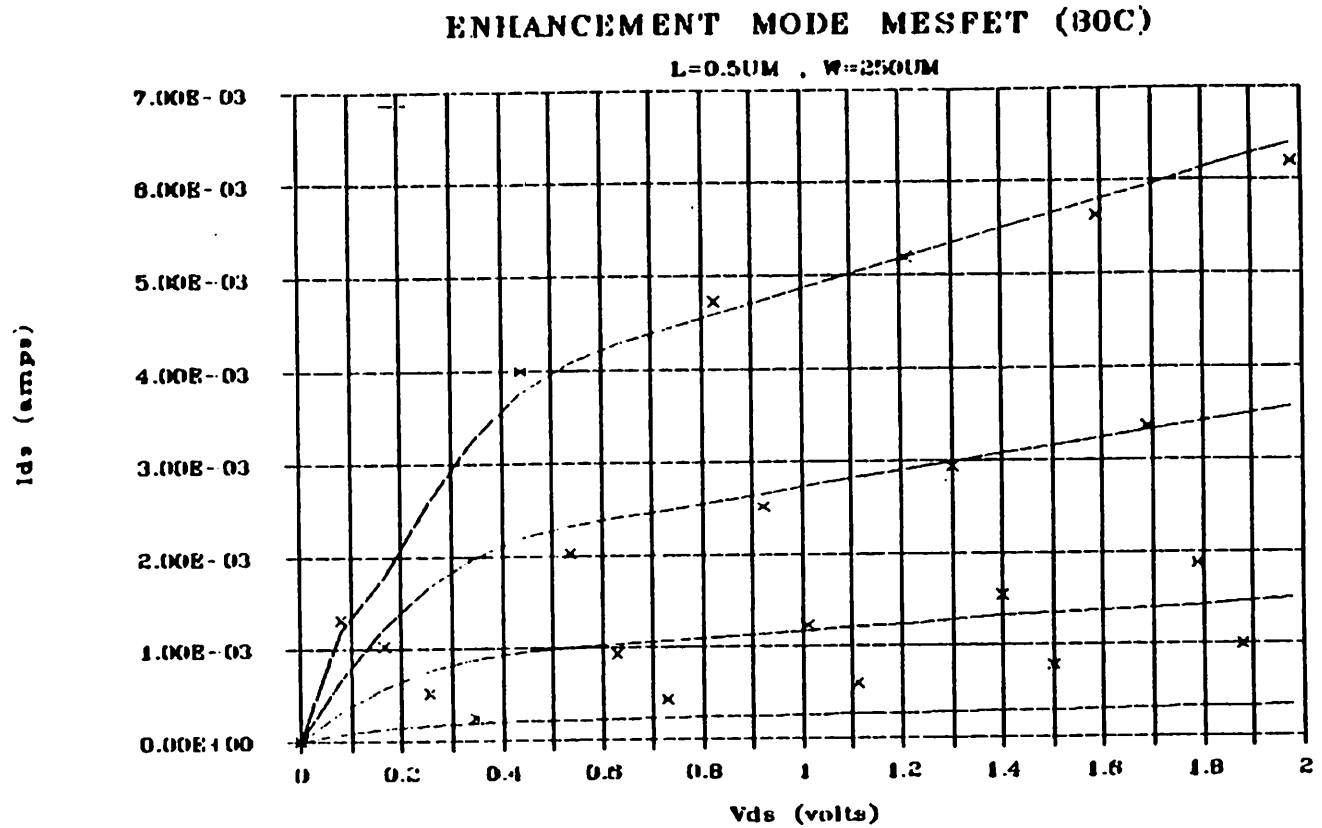

ENHANCEMENT MODE MESFET (31C)
L=0.5UM , W=250UM
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)

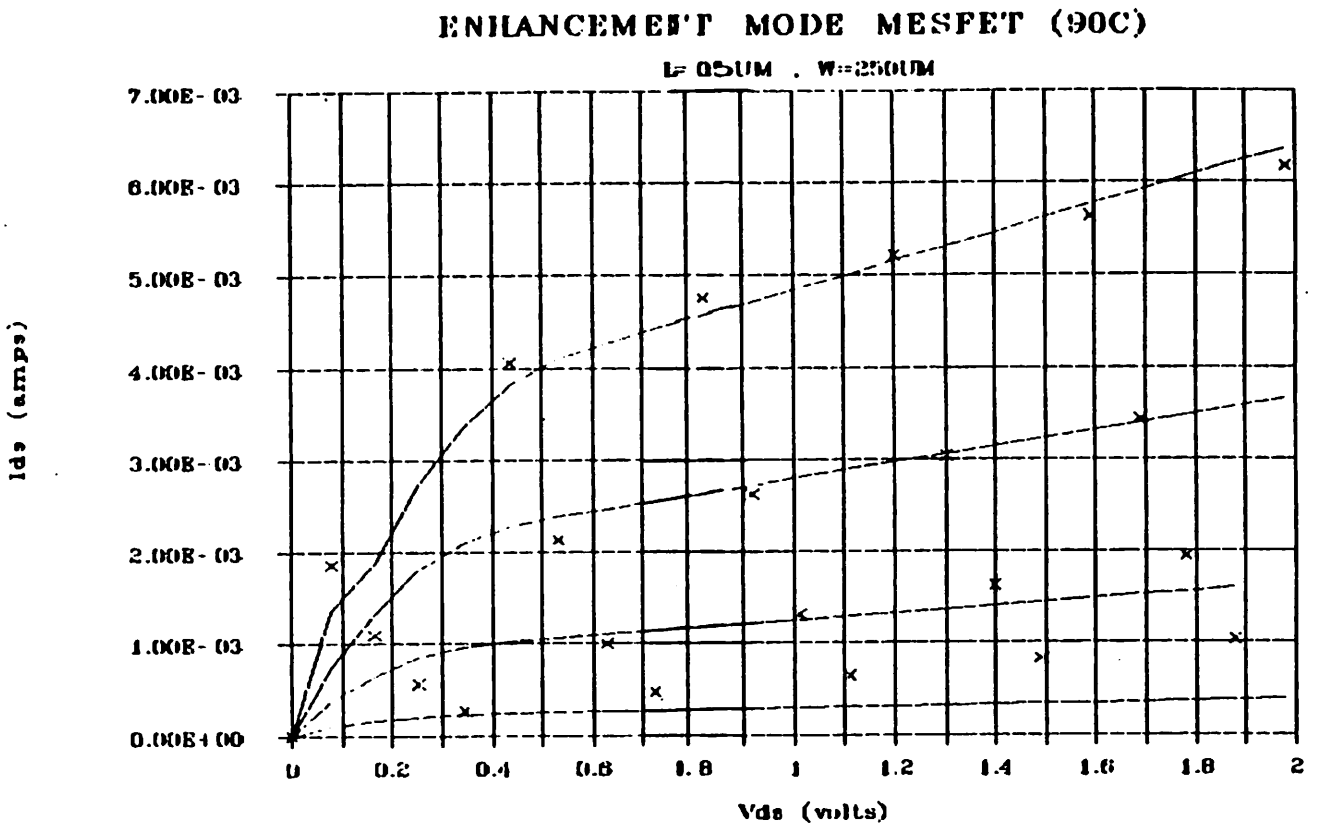

ENHANCEMENT MODE MESFET (40C)
L=0.5UM . W=250UM
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)


ENHANCEMENT MODE MESFET (50)
L=0.5UM , W=250UM
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)


ENHANCEMENT MODE MESFET (60C)
L=0.5UM , W=250UM
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)


ENHANCEMENT MODE MESFET (70C)
L=0.5UM , W=250UM
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)


ENHANCEMENT MODE MESFET (80C)
L=0.5UM , W=250UM
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)


ENHANCEMENT MODE MESFET (90C)
L= 05UM , W=250UM
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Ids (amps)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Vds (volts)

```
******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE -10C

****     CIRCUIT DESCRIPTION

*****************************************************************************


*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.78V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMES-10 250.0
BDEP1 4 6 7 DMES-10 125.0
BDL1 0 1 1 DMES-10 31.0
BDL2 0 2 2 DMES-10 31.0
BBIAS2 7 8 8 DMES-10 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMES-10 8
BB2 15 16 16 DMES-10 8
BB3 16 17 17 DMES-10 8
BB4 17  8 8  DMES-10 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP -10
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.36V V(2)=-1.36V V(4)=-1.99V V(6)=-4.52V V(7)=-4.0V
+ V(9)=-4.52V V(15)=-1.25V V(16)=-2.51V V(17)=-3.77V

.MODEL EMES-10 GASFET VTO=-0.02816 VBI=0.65 ALPHA=3.465 BETA=5.379E-5
+ LAMBDA=0.5024  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES-10 GASFET VTO=-0.8262 VBI=0.65 ALPHA=4.875 BETA=14.66E-5
+ LAMBDA=0.1676 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE -10C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = -10.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.3946	(2)	-1.3950	(4)	-2.0241	(6)	-4.5007
(7)	-4.0379	(8)	-5.0000	(9)	-4.5007	(15)	-1.2500
(16)	-2.5000	(17)	-3.7500				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS	6.111D-03

TOTAL POWER DISSIPATION 3.06D-02 WATTS

```
******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE OC

****     CIRCUIT DESCRIPTION

******************************************************************************


*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.78V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMESO 250.0
BDEP1 4 6 7 DMESO 125.0
BDL1 0 1 1 DMESO 31.0
BDL2 0 2 2 DMESO 31.0
BBIAS2 7 8 8 DMESO 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMESO 8
BB2 15 16 16 DMESO 8
BB3 16 17 17 DMESO 8
BB4 17 8 8   DMESO 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 0
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.36V V(2)=-1.36V V(4)=-1.97V V(6)=-4.52V V(7)=-4.0V
+ V(9)=-4.52V V(15)=-1.25V V(16)=-2.51V V(17)=-3.77V

.MODEL EMESO GASFET VTO=-0.02909 VBI=0.65 ALPHA=3.465 BETA=5.182E-5
+ LAMBDA=0.5016  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMESO GASFET VTO=-0.8271 VBI=0.65 ALPHA=4.875 BETA=14.12E-5
+ LAMBDA=0.1666 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 0C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.3939	(2)	-1.3943	(4)	-2.0018	(6)	-4.5011
(7)	-4.0382	(8)	-5.0000	(9)	-4.5011	(15)	-1.2500
(16)	-2.5000	(17)	-3.7500				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS	5.952D-03

TOTAL POWER DISSIPATION 2.98D-02 WATTS

```
******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 10C

****     CIRCUIT DESCRIPTION

*****************************************************************************


*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.60V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMES10 250.0
BDEP1 4 6 7 DMES10 125.0
BDL1 0 1 1 DMES10 31.0
BDL2 0 2 2 DMES10 31.0
BBIAS2 7 8 8 DMES10 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMES10 8
BB2 15 16 16 DMES10 8
BB3 16 17 17 DMES10 8
BB4 17 8 8   DMES10 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 10
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.36V V(2)=-1.36V V(4)=-1.95V V(6)=-4.52V V(7)=-4.06V
+ V(9)=-4.52V V(15)=-1.25V V(16)=-2.51V V(17)=-3.77V

.MODEL EMES10 GASFET VTO=-0.03003 VBI=0.65 ALPHA=3.465 BETA=4.99E-5
+ LAMBDA=0.5008  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES10 GASFET VTO=-0.8279 VBI=0.65 ALPHA=4.875 BETA=13.62E-5
+ LAMBDA=0.1657 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 10C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 10.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.3928	(2)	-1.3932	(4)	-1.9791	(6)	-4.5016
(7)	-4.0386	(8)	-5.0000	(9)	-4.5016	(15)	-1.2500
(16)	-2.5001	(17)	-3.7501				

VOLTAGE SOURCE CURRENTS

NAME CURRENT

VSS 5.801D-03

TOTAL POWER DISSIPATION 2.90D-02 WATTS

```
******** 1/ 1/80******** FSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 20C

****     CIRCUIT DESCRIPTION

*****************************************************************************


*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.78V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMES20 250.0
BDEP1 4 6 7 DMES20 125.0
BDL1 0 1 1 DMES20 31.0
BDL2 0 2 2 DMES20 31.0
BBIAS2 7 8 8 DMES20 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMES20 8
BB2 15 16 16 DMES20 8
BB3 16 17 17 DMES20 8
BB4 17 8 8   DMES20 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 20
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.37V V(2)=-1.37V V(4)=-1.93V V(6)=-4.52V V(7)=-4.05V
+ V(9)=-4.52V V(15)=-1.25V V(16)=-2.51V V(17)=-3.77V

.MODEL EMES20 GASFET VTO=-0.03097 VBI=0.65 ALPHA=3.465 BETA=4.828E-5
+ LAMBDA=0.5000  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES20 GASFET VTO=-0.8287 VBI=0.65 ALPHA=4.875 BETA=13.16E-5
+ LAMBDA=0.1648 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 20C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 20.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.3922	(2)	-1.3927	(4)	-1.9567	(6)	-4.5019
(7)	-4.0388	(8)	-5.0000	(9)	-4.5019	(15)	-1.2501
(16)	-2.5002	(17)	-3.7503				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS	5.660D-03

TOTAL POWER DISSIPATION 2.83D-02 WATTS

```
******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 30C

****     CIRCUIT DESCRIPTION

*****************************************************************************


*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.60V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMES30 250.0
BDEP1 4 6 7 DMES30 125.0
BDL1 0 1 1 DMES30 31.0
BDL2 0 2 2 DMES30 31.0
BBIAS2 7 8 8 DMES30 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMES30 8
BB2 15 16 16 DMES30 8
BB3 16 17 17 DMES30 8
BB4 17 8 8   DMES30 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 30
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.38V V(2)=-1.38V V(4)=-1.92 V(6)=-4.51V V(7)=-4.04V
+ V(9)=-4.52V V(15)=-1.25V V(16)=-2.50V V(17)=-3.75V

.MODEL EMES30 GASFET VTO=-0.03191 VBI=0.65 ALPHA=3.465 BETA=4.638E-5
+ LAMBDA=0.4993  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES30 GASFET VTO=-0.8296 VBI=0.65 ALPHA=4.875 BETA=12.72E-5
+ LAMBDA=0.1639 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 30C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 30.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.3898	(2)	-1.3903	(4)	-1.9324	(6)	-4.5038
(7)	-4.0404	(8)	-5.0000	(9)	-4.5038	(15)	-1.2503
(16)	-2.5006	(17)	-3.7510				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS	5.523D-03

TOTAL POWER DISSIPATION 2.76D-02 WATTS

```
******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 40C

****     CIRCUIT DESCRIPTION

******************************************************************************


*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.60V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMES40 250.0
BDEP1 4 6 7 DMES40 125.0
BDL1 0 1 1 DMES40 31.0
BDL2 0 2 2 DMES40 31.0
BBIAS2 7 8 8 DMES40 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMES40 8
BB2 15 16 16 DMES40 8
BB3 16 17 17 DMES40 8
BB4 17 8 8   DMES40 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 40
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.40V V(2)=-1.40V V(4)=-1.92V V(6)=-4.50V V(7)=-4.04V
+ V(9)=-4.5V V(15)=-1.25V V(16)=-2.5V V(17)=-3.75V

.MODEL EMES40 GASFET VTO=-0.04129 VBI=0.65 ALPHA=3.465 BETA=4.52E-5
+ LAMBDA=0.4915  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES40 GASFET VTO=-0.8380 VBI=0.65 ALPHA=4.875 BETA=10.32E-5
+ LAMBDA=0.1563 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 40C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 40.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.4098	(2)	-1.4102	(4)	-1.9307	(6)	-4.5032
(7)	-4.0368	(8)	-5.0000	(9)	-4.5032	(15)	-1.2508
(16)	-2.5015	(17)	-3.7523				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS	5.465D-03

TOTAL POWER DISSIPATION 2.73D-02 WATTS

```
******** 1/ 1/80******** FSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 50C

****     CIRCUIT DESCRIPTION

*****************************************************************************



*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.60V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMES50 250.0
BDEP1 4 6 7 DMES50 125.0
BDL1 0 1 1 DMES50 31.0
BDL2 0 2 2 DMES50 31.0
BBIAS2 7 8 8 DMES50 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMES50 8
BB2 15 16 16 DMES50 8
BB3 16 17 17 DMES50 8
BB4 17 8 8   DMES50 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 50
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.44V V(2)=-1.44V V(4)=-1.94 V(6)=-4.49V V(7)=-4.02V
+ V(9)=-4.49V V(15)=-1.24V V(16)=-2.49V V(17)=-3.74V

.MODEL EMES50 GASFET VTO=-0.05066 VBI=0.65 ALPHA=3.465 BETA=4.40E-5
+ LAMBDA=0.4836  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES50 GASFET VTO=-0.8463 VBI=0.65 ALPHA=4.875 BETA=11.93E-5
+ LAMBDA=0.1453 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 50C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 50.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.4382	(2)	-1.4386	(4)	-1.9373	(6)	-4.5038
(7)	-4.0352	(8)	-5.0000	(9)	-4.5038	(15)	-1.2518
(16)	-2.5037	(17)	-3.7555				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS	5.393D-03

TOTAL POWER DISSIPATION 2.70D-02 WATTS

```
******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 60C

****     CIRCUIT DESCRIPTION

*****************************************************************************


*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.60V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMES60 250.0
BDEP1 4 6 7 DMES60 125.0
BDL1 0 1 1 DMES60 31.0
BDL2 0 2 2 DMES60 31.0
BBIAS2 7 8 8 DMES60 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMES60 8
BB2 15 16 16 DMES60 8
BB3 16 17 17 DMES60 8
BB4 17 8 8   DMES60 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 60
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.49V V(2)=-1.49V V(4)=-1.94 V(6)=-4.49V V(7)=-4.02V
+ V(9)=-4.49V V(15)=-1.249V V(16)=-2.48V V(17)=-3.72V

.MODEL EMES60 GASFET VTO=-0.06002 VBI=0.65 ALPHA=3.465 BETA=4.30E-5
+ LAMBDA=0.4758  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES60 GASFET VTO=-0.8546 VBI=0.65 ALPHA=4.875 BETA=11.58E-5
+ LAMBDA=0.1360 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 60C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 60.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.4614	(2)	-1.4618	(4)	-1.9386	(6)	-4.5081
(7)	-4.0369	(8)	-5.0000	(9)	-4.5081	(15)	-1.2540
(16)	-2.5080	(17)	-3.7621				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS	5.333D-03

TOTAL POWER DISSIPATION 2.67D-02 WATTS

```
******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 70C

****     CIRCUIT DESCRIPTION

*****************************************************************************



*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.60V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMES70 250.0
BDEP1 4 6 7 DMES70 125.0
BDL1 0 1 1 DMES70 31.0
BDL2 0 2 2 DMES70 31.0
BBIAS2 7 8 8 DMES70 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMES70 8
BB2 15 16 16 DMES70 8
BB3 16 17 17 DMES70 8
BB4 17 8 8   DMES70 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 70
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.53V V(2)=-1.53V V(4)=-1.99 V(6)=-4.46V V(7)=-3.99V
+ V(9)=-4.46V V(15)=-1.24V V(16)=-2.48V V(17)=-3.72V

.MODEL EMES70 GASFET VTO=-0.06941 VBI=0.65 ALPHA=3.465 BETA=4.20E-5
+ LAMBDA=0.4680  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES70 GASFET VTO=-0.8554 VBI=0.65 ALPHA=4.875 BETA=11.24E-5
+ LAMBDA=0.1266 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 70C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 70.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.4844	(2)	-1.4848	(4)	-1.9392	(6)	-4.5107
(7)	-4.0411	(8)	-5.0000	(9)	-4.5107	(15)	-1.2579
(16)	-2.5159	(17)	-3.7738				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS	5.189D-03

TOTAL POWER DISSIPATION 2.59D-02 WATTS

```
******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 80C

****     CIRCUIT DESCRIPTION

*****************************************************************************


*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.60V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMES80 250.0
BDEP1 4 6 7 DMES80 125.0
BDL1 0 1 1 DMES80 31.0
BDL2 0 2 2 DMES80 31.0
BBIAS2 7 8 8 DMES80 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMES80 8
BB2 15 16 16 DMES80 8
BB3 16 17 17 DMES80 8
BB4 17 8 8   DMES80 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 80
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.60V V(2)=-1.60V V(4)=-2.03V V(6)=-4.42V V(7)=-3.95V
+ V(9)=-4.41V V(15)=-1.22V V(16)=-2.44V V(17)=-3.67V

.MODEL EMES80 GASFET VTO=-0.07879 VBI=0.65 ALPHA=3.465 BETA=4.10E-5
+ LAMBDA=0.4601  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES80 GASFET VTO=-0.8713 VBI=0.65 ALPHA=4.875 BETA=10.92E-5
+ LAMBDA=0.1173 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 80C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 80.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.4871	(2)	-1.4875	(4)	-1.9202	(6)	-4.5425
(7)	-4.0647	(8)	-5.0000	(9)	-4.5425	(15)	-1.2666
(16)	-2.5332	(17)	-3.7998				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS	5.202D-03

TOTAL POWER DISSIPATION 2.60D-02 WATTS

```
******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 90C

****     CIRCUIT DESCRIPTION

*****************************************************************************


*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.60V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMES90 250.0
BDEP1 4 6 7 DMES90 125.0
BDL1 0 1 1 DMES90 31.0
BDL2 0 2 2 DMES90 31.0
BBIAS2 7 8 8 DMES90 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMES90 8
BB2 15 16 16 DMES90 8
BB3 16 17 17 DMES90 8
BB4 17 8 8   DMES90 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 90
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.69V V(2)=-1.69V V(4)=-2.10 V(6)=-4.37V V(7)=-3.90V
+ V(9)=-4.37V V(15)=-1.20V V(16)=-2.44V V(17)=-3.67V

.MODEL EMES90 GASFET VTO=-0.08816 VBI=0.65 ALPHA=3.465 BETA=4.01E-5
+ LAMBDA=0.4523  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES90 GASFET VTO=-0.8796 VBI=0.65 ALPHA=4.875 BETA=10.62E-5
+ LAMBDA=0.1080 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:49********

VOLTAGE REFEREANCE 90C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 90.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.4768	(2)	-1.4772	(4)	-1.8876	(6)	-4.5821
(7)	-4.1001	(8)	-5.0000	(9)	-4.5821	(15)	-1.2802
(16)	-2.5604	(17)	-3.8406				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS	5.132D-03

TOTAL POWER DISSIPATION 2.57D-02 WATTS

```
******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 100C

****     CIRCUIT DESCRIPTION

*****************************************************************************


*
*  ALL THE SUPPLY VOLTAGES.
*
VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.60V
*
*  CIRCUIT
*  ACTIVE DEVICES
*
BENH1 1 17 7 EMES100 250.0
BDEP1 4 6 7 DMES100 125.0
BDL1 0 1 1 DMES100 31.0
BDL2 0 2 2 DMES100 31.0
BBIAS2 7 8 8 DMES100 65.0
*
* LEVEL SHIFT DIODE
D1 2 4  DIMOD 300
*
*  IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*  BIAS CIRCUIT *
BB1 0 15 15  DMES100 8
BB2 15 16 16 DMES100 8
BB3 16 17 17 DMES100 8
BB4 17 8 8   DMES100 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 100
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.75V V(2)=-1.75V V(4)=-2.15V V(6)=-4.30V V(7)=-3.85V
+ V(9)=-4.33V V(15)=-1.18V V(16)=-2.38V V(17)=-3.58V

.MODEL EMES100 GASFET VTO=-0.08909 VBI=0.65 ALPHA=3.465 BETA=3.90E-5
+ LAMBDA=0.4515  RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES100 GASFET VTO=-0.8804 VBI=0.65 ALPHA=4.875 BETA=10.33E-5
+ LAMBDA=0.1070 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15  RS=28.0 VJ=0.65
.END
```

******** 1/ 1/80******** PSpice 2.03 (May 1985) ******* 0:34:48********

VOLTAGE REFEREANCE 100C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 100.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-1.3765	(2)	-1.3770	(4)	-1.7646	(6)	-4.6534
(7)	-4.1670	(8)	-5.0000	(9)	-4.6534	(15)	-1.7032
(16)	-2.6063	(17)	-3.9095				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS	4.993D-03

TOTAL POWER DISSIPATION 2.50D-02 WATTS