THE DESIGN OF A GaAs MESFET TEMPERATURE INDEPENDENT VOLTAGE REFERENCE CIRCUIT AND THE EVALUATION OF GaAs LARGE SIGNAL MESFET MODELS

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ABSTRACT

A number of large signal computer models for GaAs MESFETs have been implemented in the simulation program SPICE. The accuracy of these models has not been thoroughly investigated previously, and therefore an evaluation of these models was undertaken. A second study examined the effects of temperature on GaAs MESFETs. The effects are shown by plotting extracted SPICE parameters for two of the models over the test temperature range. The data provides new information for a proposed temperature independent voltage reference circuit that is designed and simulated using SPICE.

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I. INTRODUCTION

The development of GaAs MESFET technology has led to very high speed GaAs digital integrated circuits as well as GaAs monolithic microwave integrated circuits. To aid in the design of GaAs integrated circuits, high speed computers have been used for circuit simulation. At present, one such program is U. C. Berkeley's SPICE2[^1]. SPICE2 was originally released to the public without a GaAs large signal MESFET model. In 1983, a GaAs MESFET model was introduced into SPICE2[^2] and more recently two other models have been implemented.[^3],[^4]

In the first part of this report, the large signal SPICE models are evaluated and compared. In the course of the evaluation, some attention is given to the material properties of GaAs as well as to the GaAs MESFET device characteristics. It is shown that present models lack the sophistication necessary to model the GaAs MESFET with sufficient accuracy. Therefore, the circuit designer must be aware of these shortcomings for effective circuit simulation.

In the second part of this report, the results of a study to determine the temperature effects on GaAs MESFET devices are presented. Extensive measurements were made with MESFETs from several different manufacturers. The devices were measured at various temperatures, and the current-voltage data was recorded.

The SPICE large signal GaAs MESFET device parameters were extracted from
the recorded data for the Curtice and Statz models. The results are presented in plots showing SPICE parameters versus temperature. These temperature-dependent parameters were then used in the design of a proposed temperature independent voltage reference circuit. The circuit has not been fabricated to date. Experimental results will be presented elsewhere when available.
II. BASIC MESFET PRINCIPLES

The development of a suitable MESFET model depends greatly upon the MESFET's physical structure, the electrical operation of the device, and on a knowledge of GaAs material properties. In this section, the material properties which make GaAs theoretically appealing are presented. The parasitic effects which hinder the MESFET's performance in practical designs will be discussed, and the MESFET's structure will be covered.

A. GaAs Material Properties

One of the most important and desirable characteristic of GaAs is that it has a higher electron transport mobility factor than silicon. With a doping level of \( N_d = 10^{17} \text{ cm}^{-3} \), GaAs has a low field mobility of 4500 cm\(^2\)/V-sec. and a peak electron saturation drift velocity of 2\( \times 10^7 \) cm/sec. For comparison, silicon with a doping level of \( N_d = 10^{17} \text{ cm}^{-3} \) has an electron mobility of 800 cm\(^2\)/V-sec. and a peak drift velocity of 1\( \times 10^7 \) cm/sec. (Figure 1).[5] The extremely high electron mobility and electron velocity permit GaAs devices to have wider bandwidth and faster switching capabilities than those of silicon.

Insight into the physics responsible for the greater speed in GaAs is gained by studying the energy momentum diagrams (Figure 2).[5] GaAs is a direct bandgap material while Si is an indirect bandgap material. Thus from the figure, GaAs requires 1.4 eV of energy while silicon requires 1.1 eV to promote an electron from
the valence band to the conduction band. However, GaAs requires no change in momentum for the promotion, whereas silicon has a 2.3eV gap at the zero momentum point. Promotion of electrons to a higher momentum state translates to a higher effective mass. The effective mass of electrons traveling through GaAs is 0.068$M_o$, where $M_o$ equals the free electron rest mass. This compares with an effective mass of 0.92$M_o$ for silicon.

A second important distinction between silicon and GaAs is the unique semi-insulating GaAs substrate. GaAs substrates are made insulating by a complex compensation scheme. Generally, shallow donors in GaAs are compensated by deep acceptors, and shallow acceptors are compensated by deep donors. As an example of this compensation method, Si ions a shallow donors introduced during the crystal growth are compensated with intentionally added Cr deep acceptors. The semi-insulating GaAs is typically manufactured with an intrinsic resistivity of $10^8$ohm-cm. The high resistivity results in the depletion of carriers in the substrate which reduces the interconnection capacitance to ground. Furthermore, advanced metallization schemes such as air-bridge metal are also commonly used to further reduce interconnect capacitance. The reduced capacitance is essential for high speed digital or high frequency analog integrated circuit applications.

B. MESFET Structure

Cross sections of two GaAs MESFETs are shown in Figures (3) and (4). The
first figure shows an ion implanted MESFET made with a fully planar process. Planar processed MESFETs are currently being investigated by many research laboratories, and it is anticipated that planar processed MESFETs will become the main device for GaAs digital ICs. A primary motivation for using planar processing is that no etching of the active layer is required, thus allowing the most dense packing of active devices. The second figure shows a mesa etched GaAs MESFET. This type of GaAs MESFET is presently the most widely used.

One unpleasant aspect of GaAs MESFETs in contrast to MOSFETs is that the gate is not insulated from the channel. Rather, the gate metal makes direct contact to the semiconductor over the channel region to form a Schottky diode. Attempts at finding a native oxide to insulate the gate of GaAs MESFETs have been unsuccessful. In silicon MOSFETs, a similar problem was overcome by using the native oxide SiO$_2$[6]. As will be discussed later, the Schottky diode at the MESFET's gate provides major new challenges for circuit designers to overcome since the gate conducts significant current when it is forward biased.

C. MESFET Parasitic Effects

Although GaAs material properties are potentially superior to silicon, the GaAs MESFET as manufactured with present techniques exhibits more device parasitic effects than the silicon MOSFET device. These effects make modeling and designing with MESFETs very difficult. Some important parasitic effects of the
MESFET are considered briefly in this section.

The most problematic and frequently noted parasitics\textsuperscript{[9]} are the looping, kinking, and backgating effects. Although these effects are not well understood, the commonly cited causes of these problems are bad surface passivation and deep level traps in the semi-insulating substrate. Some of these problems will disappear as GaAs MESFET technology matures.

The looping effect shown in Figure (5) is generally observed in low frequency current-voltage characteristics. This effect exists in gated as well as in ungated MESFETs\textsuperscript{[7],[8]}. For this reason, some researchers believe that deep level donors in the substrate below the channel are the cause of this problem. According to published reports, it appears that the looping effect is removed or suppressed greatly by adding a compensating buffer layer\textsuperscript{[7],[8]}. The time constant associated with the looping effect ranges from $0.1\text{Hz}$ to $1\text{KHz}$ (Figure 6).\textsuperscript{[9]}

The kink effect corresponds to the extra flow of source drain current above a certain kink threshold voltage (Figure 7). As of this writing, the cause of the kink is apparently still a mystery to device engineers developing gallium arsenide MESFETs.

Backgating and sidegating are parasitic effects that have received a considerable amount of attention. There are two types of backgating and sidegating. The first is a DC backgating due to the voltage potential of one node effecting another node. The depleted semi-insulating substrate acts as a very high
impedence, connecting one circuit node to another. In order to minimize the DC backgating effect, circuit designers place MESFET transistors far apart (~50 microns) in the circuit layout. The large distance between transistors eliminates the backgating effect, but at the same time significantly increases the interconnection capacitance, thus reducing the main benefit of having a semi-insulating GaAs substrate. The second type of backgating is an AC backgating effect due to electron traps in the substrate under the channel. The electron traps act as small capacitors which tend to cause coupling between transistors (Figure 33).

In digital GaAs ICs, backgating and sidegating effects will cause gates to switch state improperly resulting in logic error in the circuit. In analog applications, the backgating and sidegating problem will make commonly used differential circuit configurations used in silicon ICs difficult to achieve in GaAs ICs. Further investigation is necessary to determine how well the semi-insulating substrate isolates one device from another in a closely packed environment.
III. SPICE GaAs LARGE SIGNAL MESFET MODELS

A. Introduction to GaAs MESFET models

In 1974, Van Tuyl and Liechti[10] approximated the current voltage relationship of a MESFET by the equation:

\[ I_{ds} = \beta(V_{gs} + V_{to})^2 (1 + \Omega V_{ds}) \tanh(\varphi V_{ds}) \]  

This equation was incorporated into a large signal GaAs MESFET model developed at RCA laboratories by Curtice (Figure 8).[11] In 1984, Sussman-Fort[2] implemented this model in SPICE2. Note that this model is obviously asymmetric with respect to the source and drain which is a major limitation.

More recently U. C. Berkeley has developed SPICE3.[12] In this version of SPICE, a new MESFET model developed by Statz at Raytheon Labs (Figure 9)[3] was included. In this new model, the current voltage relationship is approximated by the equation:

\[ I_{ds} = \frac{\beta(V_{gs} + V_{to})^2 (1 + \Omega V_{ds})}{1 + b(V_{gs} + V_{to})} [1 - (1 - \varphi V_{ds}/3)^3] \]  

for \( 0 < V_{ds} < 3/\varphi \)
\[ I_{ds} = \frac{\beta(V_{gs} + V_{to})^2 (1 + \Omega V_{ds})}{1 + b(V_{gs} + V_{to})} \quad \text{for } 0 > 3/\varnothing \]

In addition to the new voltage-controlled current equation, a capacitance model that also provides source-drain symmetry was introduced. This capacitance model is discussed later in the report.

During the evaluation of the Curtice and Statz GaAs large signal MESFET models mentioned in the previous paragraphs, a publication appeared\(^{[4]}\) presenting a new GaAs large signal MESFET model for SPICE. This model has a current voltage relationship:

\[ I_{ds} = \beta(V_{gs} + V_{to})^2 (1 + \Omega V_{ds}) \tanh(\varnothing V_{ds}) + V_{ds}/R_{sh} \quad (1.3) \]

\[ \varnothing = \varnothing_o \beta(V_{BI} + V_{to})^2 \left( \frac{1 - [(V_{BI} - V_{gs})/2(V_{BI} + V_{to})]^{1/2}}{\beta(V_{gs} + V_{to})} \right) \]

\[ R_{sh} = R_{sho} / 2[\exp(-V_{to} - V_{gs}/STF KT/q) + 1] \]

\[ STF = \text{empirical parameter similar to ideality factor} \]

Although the McKinley MESFET model\(^{[4]}\) was not investigated in this report as thoroughly as the Curtice or the Statz model, the McKinley model presents certain characteristics that the other two models have not incorporated. Some of the
differences in the McKinley voltage-controlled current equations appear to be a possible improvement to problems existing in the other two models. Reference will be made to the McKinley model when appropriate because of the possible improvement over the other two models.

B. SPICE Parameter Extraction Methods

The extraction of SPICE parameters from measured MESFET data is often a very difficult task. In this study only DC parameters were extracted from the device, as the proposed circuit is a DC voltage reference. The extraction methods utilized are explained more thoroughly in references [13] and [14].

The source resistance $R_s$ was obtained by forcing current into the gate and out of the source node while measuring the voltage at the drain (Figures 10 and 11). An assumption is made that the voltage drop across the drain resistance is zero. Therefore, the relationship $R_s = I_s/V_D$ is valid. The drain resistance was measured by a similar method shown in Figures (12) and (13). Gate resistance $R_g$ was measured by driving the gate node with a voltage source and concurrently measuring the current flowing in the drain and source nodes (Figures 14 and 15).

The value of the gate Schottky diode saturation current parameter ($I_s$) was measured by conventional means of extrapolating from $\ln(I_g)$ versus $V_g$ with both source and drain nodes grounded. Finally, the parameters for the voltage-controlled current source, Equations (1.1) and (1.2), were found by using a fitting program.
which minimizes the mean square error between the measured and calculated values from the Curtice and Statz models. The FORTRAN source code for the fitting program is provided in Appendix (1).

C. SPICE Parameters Extraction Results

The results show that the SPICE MESFET models are accurate only in a certain region of operation. The region is defined by a lower boundary of approximately 0.3 volts greater than the threshold voltage ($V_{th}$), and an upper boundary defined by a ($V_{gs}$) voltage that will maintain a low gate forward bias current. At the threshold of conduction and immediately after conduction begins, the current increases faster than the calculated current (Figure 18 and 19). This problem is more apparent in the enhancement MESFET because the device has a much higher leakage and subthreshold conduction current relative to the magnitude of $I_{dss}$.

Secondly, the MESFET models fail to model the region where the current kinking effect occurs. In this region, the kink causes enormous error when trying to fit the measured curves to Equations (1.1) and (1.2). For this reason, the fitting was possible only up to $V_{ds} = 3.0$ volts where the kinking effect was not observed. The results of the curve fitting are shown in the Appendix (2).

The SPICE parameters were extracted from the recorded data in the region where the SPICE models were found to be consistent with measured devices ($V_{ds} < 3.0V$). Parameters were extracted over the temperature range of 25° to 100°C for
both the Statz model (Eq. 1.2) and for the Curtice model (Eq. 1.1). The extraction shows that the transitconductance term ($\beta$) decreases with temperature. For a first order approximation, the transitconductance term ($\beta$) appears to obey the following equation:

$$\beta(T) = \beta_0 \left(\frac{T_0}{T}\right)^n \quad \text{where} \quad n = 1 \quad (1.4)$$

The threshold voltage ($V_{to}$) of the device also decreases with temperature. A first order approximation of the threshold voltage ($V_{to}$) can be represented by a linearly decreasing voltage. The degradation rate for the enhancement MESFET devices was found to be $-0.94\text{mV/}^\circ\text{C}$. For the depletion MESFET devices, the degradation rate was found to be $-0.83\text{mV/}^\circ\text{C}$. The high $V_{gs}$ degradation term ($b$) in the denominator of Eq. (1.2) was shown to be very small and of no significance in the region of fitting (Figures 20-23). Since the term ($b$) did not effect the region of the curve fit, it was found that the Statz model voltage-controlled current source degenerated to the form of the Curtice model. Furthermore, the Statz model voltage-controlled current source parameters converged to the Curtice model parameters.

D. SPICE Model Comparisons

The Curtice model shown in Figure (8) is not a symmetric MESFET model. In normal MESFETs, there exists a Schottky diode on the gate-to-drain side as well. Secondly, the Curtice model treats the gate source capacitance as a nonlinear
capacitance represented by the diode junction capacitance. This equation takes the form of:

\[
C_{gs} = C_{gso} / \left(1 - \frac{V_{gs}}{V_{BI}}\right)^{1/2}
\]  
(1.5)

\[
C_{gs} = C_{gso} \quad \text{when } V_{gs} = 0
\]

This model has been reported to be inaccurate\textsuperscript{[16]} for modeling the MESFET capacitance. The actual \( C_{gs} \) capacitance has been shown to give the characteristic shown in Figure (24). The gate drain capacitance in the Curtice model is constant. This is incorrect since the gate drain capacitance is in reality a function of gate to drain voltage.

Equation (1.1) which represents the voltage-controlled current source in the Curtice model does not represent the current-voltage characteristic accurately in the region near turn-on, or in the subthreshold region. Figures (18) and (19) show the plots of the square root of \( I_d \) versus \( V_{gs} \) with a condition \( V_{ds} = 1.2 \) volts applied to the drain. The curve generated by the MESFET model is straight and intersects at \( V_{gs} = V_{to} \) when \( I_d = 0 \) mA. From measurements, the drain current does not follow the straight curve but begins to flatten out and eventually plateaus at the leakage current level. Another aspect of the equation which does not match measured results well is the small signal output conductance term. In Equation (1.1), the output conductance is obtained by differentiating the large signal
equations. The model assumes that the output conductance value is the same for any frequency value. However, from measured results\cite{15} this appears to be a bad approximation to the MESFET's actual output conductance (Figure 25). In the figure, output conductance was shown to decrease with frequency.

The more recently released GaAs MESFET model in SPICE3 is unfortunately similar to the Curtice model in many ways. The output conductance term in the Statz model (Eq. 1.2) is obtained by using exactly the same method as that used in the Curtice model. Therefore the Statz model has exactly the same problem as the Curtice model. Secondly, the problems with modeling the regions near turn-on and subthreshold exist in the Statz model exactly as explained in the Curtice model case.

There are new additions to the Statz model which address some of the problems of the Curtice model. The first improvement introduced by Statz was replacing the hypertangent function in the Curtice model by a hypertangent polynomial approximation function. This facilitate convergence in the SPICE algorithm. The second new term which is apparent in the Statz model is the new denominator term \[1 + b(Vgs + Vto)\]. This term was added to model the \(I_{ds}\) current under high gate to source voltage. However, measurements have shown that the square law equations model the MESFET behavior very well. Only under the condition when the gate to source voltage approaches the Schottky diode turn-on voltage does the \(I_{ds}\) current no longer obey the square law. Only then does the newly added denominator term appears to model the current degradation. In other regions of transistor operation, the \(b\) term is very small and does not effect the current (\(I_{ds}\)).
In the Statz model, the symmetry problem observed in the Curtice model was removed by providing a second diode located at the gate to drain. In addition, the new symmetric capacitance model equations are:

1) when $V_{ds} > 0$, then

$$Q_g = 2C_{gso} V_{BI}[1 - (1 + V_{gs}/V_{BI})^{1/2}] + C_{gdo} V_{gd} \quad (1.6)$$

$$C_{gs} = \frac{dQ_g}{dV_{gs}} = C_{gso} / (1 + V_{gs}/V_{BI})^{1/2}$$

$$C_{gd} = \frac{dQ_g}{dV_{gd}} = C_{gdo}$$

2) when $V_{ds} < 0$, then

$$Q_g = 2C_{gso} V_{BI}[1 - (1 + V_{gd}/V_{BI})^{1/2}] + C_{gdo} V_{gs}$$

$$C_{gs} = \frac{dQ_g}{dV_{gs}} = C_{gdo}$$

$$C_{gd} = \frac{dQ_g}{dV_{gd}} = C_{gso} / (1 + V_{gs}/V_{BI})^{1/2}$$

This capacitance model automatically takes into account the symmetry of the MESFET when used as a pass gate or as a transistor switch.

One of the more critical problem in the Statz and Curtice models exists in the region of subthreshold conduction. Only the McKinley model$^4$ has attempted to
address this problem by introducing a subthreshold conduction term. This term exponentially decays as the MESFET device goes into full conduction. The McKinley model has also made the saturation voltage parameter ($\phi$) a function of $V_{gs}$.

In ending this section on SPICE large signal MESFET models, a few words should be said about the difficulties encountered in SPICE2 with the Curtice's, Equation (1.1). Users of SPICE2 have reported that there are major convergence problems with this equation. It appears that the hypertangent function causes a variety of convergence problems in the SPICE2 algorithms.
IV. TEMPERATURE INDEPENDENCE VOLTAGE REFERENCE CIRCUIT

In the previous sections, the temperature dependence of SPICE large signal MESFET parameters were examined. The results were plotted in Figures (20-23). The information obtained from temperature measurements will be used in the design of a temperature stable voltage reference circuit.

A. The Basic Reference

The first step in realizing a voltage reference is to find a temperature stable unit of voltage. In GaAs MESFET technology, the threshold voltage is a candidate for such a unit of voltage. However, the independent terms that make up the threshold voltage are temperature dependent as well as process dependent as seen below:

\[
V_p = \phi_i + \phi_T = qNqA^2/2
\]

\[
\phi_i = \phi_m - X_i - (1/q)[E_c - E_i]
\]

\[
\phi_i = \phi_m - X_i + (1/q)[kT \ln(N_d/N_c)]
\]

\[
\phi_T = \phi_m - X_i + (kT/q) \ln(N_d/N_c) - qNdA^2/2
\]

The threshold voltage if used alone will not make a suitable voltage reference. However, if one considers the last term in Equation (1.7), it is possible to change
the threshold voltage by either changing the process doping level or by changing the channel thickness. Two devices made with different threshold voltages can be used as a standard reference. Subtracting the two threshold voltages, we obtain:

\[ \text{VT}_1 - \text{VT}_2 = \frac{kT}{q} \ln(\text{Nd}_1/\text{Nd}_2) + \left(\frac{q}{2}\right)[\text{Nd}_1 A_1^2 - \text{Nd}_2 A_2^2] \]  

(1.8)

Notice that in Equation (1.8) many of the temperature dependent terms are cancelled. We can use this to design a circuit where the gate-source is used to sense the threshold voltage.

A circuit that produces a reference voltage is shown conceptually in Figure (27). In this figure, transistor B1 and B2 exhibit different threshold voltages. By using an operational amplifier in a negative feedback configuration, the output voltage is forced to a level that causes the reference devices to operate at an equal drain voltage.

The temperature sensitivity of VREF can be analyzed by considering the equations:

\[ \text{VGS} = \text{VT} + \left[\frac{\text{Id}}{\beta} (1 + \Omega \text{Vds})\right]^{1/2} \]  

(1.9)

\[ \text{VREF} = \text{VGS}_1 - \text{VGS}_2 = \text{VT}_1 - \text{VT}_2 + \left[\frac{\text{Id}_1}{\beta_1} (1 + \Omega_1 \text{Vds}_1)\right]^{1/2} \]

\[ - \left[\frac{\text{Id}_2}{\beta_2} (1 + \Omega_2 \text{Vds}_2)\right]^{1/2} \]
Taking the derivative of Equation (1.9), the following equation is obtained:

\[
\frac{V_{REF}}{dT} = \frac{d(V_{T1} - V_{T2})}{dT} \left[ \frac{1}{2} \right] (ld)^{-1/2} \\
= \left\{ \left[ \frac{ld}{\beta_1 (1 + \Omega V_{ds})} \right]^{1/2} - \frac{1}{\beta_2 (1 + \Omega V_{ds})} \right\} \frac{dI}{dT} \\
+ \frac{1}{2} \left[ \frac{d\beta_2}{dT} \right] \left\{ \frac{1}{\beta_2^3 (1 + \Omega_2 V_{ds2})} \right\} \\
- \frac{1}{2} \left[ \frac{d\beta_1}{dT} \right] \left\{ \frac{1}{\beta_1^3 (1 + \Omega_1 V_{ds1})} \right\}
\]

B. Threshold Voltage Considerations

The first term in Equation (2.0) is the temperature dependence of the threshold voltage difference. From Equation (1.8), the derivative is taken to obtain the equation:

\[
\frac{d(V_{T1} - V_{T2})}{dT} = \frac{k}{q} \ln(N_{d1}/N_{d2})
\]

In the situation when \(N_{d1} = N_{d2}\), the threshold difference will theoretically not vary with temperature. In general, this is impossible to obtain due to process variations. Usually the threshold voltage difference will vary linearly with temperature. From Curtice model simulations with SPICE, the threshold voltage difference was found to vary with a slope of approximately \(-0.104\text{mV/°C}\).
C. Bias Current Considerations

The second term in Equation (2.0) can be made insensitive to drain current variations by equating:

\[ \beta_1 (1 + \Omega_1 V_{ds1}) = \beta_2 (1 + \Omega_2 V_{ds2}) \]

To further reduce the effects of the second term, the drain current can be biased at a point where \( \frac{dI_{ds}}{dT} = 0 \). This occurs because the MESFET's current tends to increase with temperature due to its dependence on threshold voltage, and decrease with temperature due to mobility degradation. These tendencies are nearly in balance at a bias level that is itself only slightly temperature dependent. The bias level effect measured from experimental devices are shown in Figures (28) and (29).

The third term is temperature dependent due to the mobility decreasing at the higher temperatures. This term is not compensated for in the reference circuit. However, it appears that the voltage reference is not effected greatly by this third term and the errors it contributes are relatively small.

D. Reference Circuit

Figure (30) shows a schematic of a GaAs MESFET voltage reference. Transistors B1 and B2 are the differential threshold voltage pair. They are loaded
by depletion current sources B3 and B4. Transistor B3 and B4 are matched transistors. Any mismatch in B3 and B4 will degrade the output voltage temperature coefficient. Transistor BBIAS is the tail current source used to bias the differential pair.

E. Differential Amplifier

In order for the voltage reference to work properly, a high gain differential amplifier is required in the negative feedback path of the circuit. In 1984, one such circuit was proposed by Fiedler[15]. However, the circuit proposed in the report was not fabricated and information concerning its actual performance is unknown. More recently, Larson[19] proposed and fabricated a differential amplifier using a common mode feedback for double-to-single end conversion scheme (Figure 31). In our present work, the design of a differential amplifier has not been addressed; therefore, the circuit will require an off chip amplifier.

F. Voltage Reference Simulation Results

Simulation of the voltage reference circuit was done with the simulation program SPICE using the Curtice model. The transistor parameters for the Curtice model were set to the values obtained from our measurements. The results of the simulation are presented in Appendix (3). They show that the circuit has a temperature dependence of -0.08mV/°C (Figure 32). This translates to a
temperature coefficient of -107ppm/°C which is comparable to low-voltage Si designs. The nominal voltage reference obtained from the measured devices was 0.750 volts.
V. CONCLUSION

The Curtice and Statz GaAs large signal models implemented in SPICE were evaluated. Their abilities to model typical devices were found to be ineffective in certain regions of transistor operation. It appears that further work on MESFET modeling is still required. At present, simulation with SPICE using the Curtice and Statz models will require understanding the model's weaknesses. Simulations should be done only in the regions where the models have been found to be consistent with measurements.

From the temperature study, the SPICE parameters for GaAs MESFETs were extracted over a temperature range of interest. The extracted parameters over temperature were plotted in Figures (20-23). Simple linear temperature relationships were developed to approximate the threshold voltage and the output conductance parameters in SPICE. The beta parameter was modeled by a power function as noted in Equation (1.4).

The temperature measurements led to a proposed temperature independent voltage reference circuit. This circuit was designed and simulated using SPICE. From our SPICE simulations, the voltage reference has a predicted temperature coefficient of -107ppm/°C with a nominal voltage reference of 0.750 volts.
REFERENCES


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Figure 1
Electron momentum in crystal

[Johnson, G., "Gallium Arsenide Chips Emerge", High Technology, July 1984]
Figure 3

- Refractory metal
- Gate / Source
- Isolation doping
  - (H⁺ or B⁺ implant)
- Insulating substrate
- Doped Channel (Si or Se)
- Buffer

A) Planar Process GaAs MESFET technology (ion implantation)
B) Mesa Etched GaAs MESFET with recessed gate
current-voltage characteristic with looping

[Rocchi, M. "Statue of Parasitic Effects in GaAs IC", Physica 129B 1985]
Looping verse frequency for $V_{gs} = 0.0$

[ Rocchi, M. "Surface and Bulk Parasitic Effects in GaAs IC's", Physica 129B, 1985]
The Kink Effect
(Rocchi, M., "Surface and Bulk Parasitic Effects in GaAs ICs", Physica 129B 1985)

Figure 7
Curtice's GaAs MESFET model

figure 8
Statz's GaAs MESFET model

Figure 9
Rs Measurement

Figure 10
Figure 11

**I - V characteristics of measured source resistance**
Rd Measurement

Figure 12
I vs. Vd

Vd=0, Is=0, Vg=<-2,1.8>

I - V characteristics of measured drain resistance

Figure 13
Figure 14

Rg Measured
Log(I) versus Vg Characteristics

Figure 15
GaAs Enhancement mode device \( I - V \) characteristics

Figure 16
GaAs Depletion mode device I - V characteristics

Figure 17
DMESFET: $\sqrt{I_{ds}}$ vs. $V_{gs}$

Figure 18

- $V_{gs}$ (volts)
- $\sqrt{I_{ds}}$ (A** -0.5)

- Measured
- SPICE
Figure 20

Beta vs. Temperature

Normalized W=1.0um L=0.5um
Threshold Voltage vs. Temperature

Figure 21

Enhancement

Depletion
Output Conductance Parameter vs. Temperature

Figure 22
Figure 23

b vs. temperature

b (1/V)

temperature (C)
Figure 24
Figure 25

Drain Source Resistance (kohm)

Frequency (KHz)

[Fledler, N.S., "GaAs MESFET Op-Amp", UCSD 1984]
Figure 26

Transconductance, $g_{m}$ (ms)

Frequency (kHz)

$W/L = 50/1 \text{ um}$

[A.S. Fedler, "GaAs MESFET Op-Amp", 1984]
Voltage Reference Schematic

Figure 27
ENHANCEMENT MODE MESFET

$V_{ds} = 1.0\, V$, $L = 0.5\, \mu m$, $W = 250\, \mu m$

Square root ($\sqrt{I_{ds}}$) versus $V_{gs}$ plotted over temperature

Figure 28
DEPLETION MODE MESFET

Vds=1.0V, L=0.5UM, W=50UM

Square root (Ids) versus Ugs plotted over temperature

Figure 29
Voltage Reference Schematic

Figure 30
Differential Amplifier with Common Mode Feedback

![Differential Amplifier with Common Mode Feedback](image)

Figure 31
BACKGATING / SIDEGATING

Figure 33

After C.P. Lee et al.

After Goronkin
Appendix 1: FORTRAN source code for fitting program.
Appendix 2: Curve fitting results.
Appendix 3: SPICE simulation results.
PROGRAM INOUT
C #1000

INTEGER NCUR,NPT,TEMP
DIMENSION EID(15,50),IID(15,50),ISTART(15)
DIMENSION VG(15),VD(50),VDI(15,50),TEMP(5)
REAL*8 VGMAX, VGMIN, VDMAX, VDMIN, VGSTEP, VDSTEP
REAL*8 VG, VD, VDI, EID, IID, RG, RD, RS
REAL*8 VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
CHARACTER*20 fname
COMMON /RECORD/ EID,IID,VD,VDI,VG
COMMON /STAT/ ISTART,NCUR,NPT,RG,RD,RS
COMMON /PARAS/ VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
DATA fname/' '/

C PROMPT USER FOR FILENAME.
C FILENAME REQUESTED AT RUNTIME.
C OPEN A FILE TO READ     OPEN(7,FILE= ' ')
C
C READ INPUT INFORMATION.
READ(7,*,END=1010,ERR=1020)RG,RD,RS
READ(7,*,END=1010,ERR=1020)VGMAX,VGMIN,VGSTEP
READ(7,*,END=1010,ERR=1020)VDMAX, VDMIN, VDSTEP

C SET THE BIAS VALUES OF VGS
I=1
VG(1)=VGMIN
NCUR=1
1030 I=I+1
   IF(VGMAX-(VG(I-1)+VGSTEP))1040,1050,1050
1050 VG(I)=VG(I-1)+VGSTEP
   NCUR=NCUR+1
   GO TO 1030
1040 IF(DABS(VGMAX-VG(I-1)-VGSTEP).LT.0.01) GO TO 1050

C SET THE BIAS VALUES OF VDS
I=1
VD(1)=VDMIN
NPT=1
1060 I=I+1
   IF(VDMAX-(VD(I-1)+VDSTEP))1070,1080,1080
1080 VD(I)=VD(I-1)+VDSTEP
   NPT=NPT+1
   GO TO 1060
1070 IF(DABS(VDMAX-VD(I-1)-VDSTEP).LT.0.01) GO TO 1080

DO 1090 J=1,NCUR
C READ BACK THE VGS BIAS VALUES
WRITE(8,1100) VG(J)
1100 FORMAT(6X,'VG= ',G10.4)
READ(7,*),END=1010,ERR=1020)(EID(J,I),I=1,NPT)
C READ BACK THE Ids CURRENT VALUES.
WRITE(8,'(A)')' Vds (V) MEASURE Ids (A) ';
WRITE(8,'(A)')' --------------
WRITE(8,1110)(VD(I),EID(J,I),I=1,NPT)
1110 FORMAT(6X,G10.4,5X,G10.4)
1090 continue

C CALL THE SUBROUTINE TO ADJUST THE DATA
CALL COMP(NCUR)
CALL OPTI(NCUR)
CALL MEASII(NCUR)
CALL OPTII(NCUR)
CALL MEASII(NCUR)
STOP

1010 WRITE(*,'(A)')' ** END OF FILE ** ' STOP
1020 WRITE(*,'(A)')'** EEROR I/O ** ' STOP
END
SUBROUTINE COMP(K)
C THE VALUE OF 'NCUR' IS THE CURVE NUMBER.
C #2000

DIMENSION EID(15,50),IID(15,50)
DIMENSION VG(15),VD(50),VDI(15,50),ISTART(15)
INTEGER NCUR, NPT, BPT, ISTART, J
REAL*8 EID, IID, VG, VD, VG2, VDI
REAL*8 GM, RG, RD, RS
COMMON /RECORD/ EID, IID, VG, VD, VDI, VG
COMMON /STAT/ ISTART, NCUR, NPT, RG, RD, RS

C ------------------------
C THE CURVE NUMBER IS 'J'.
C AS LONG AS THE GATE NOT FORWARD BIAS
C 'VGS-VDS<0.4 AND VGS<0.6' DO THE
C ADJUSTMENT ON VGS.
DO 2000 J=1,NCUR
DO 2010 I=1,NPT
    IF(VG(J)-VD(I).GT.0.4)GO TO 2020
    IF(VG(J).GT.0.6)GO TO 2020
C TEMPORARY STORAGE OF VGS'
    VG2=VG(J)-(EID(J,I)*RS)
    VDI(J,I)=VD(I)-(EID(J,I)*RS+EID(J,I)*RD)
C FIND THE 'GM' OF BIAS POINT.
C AVERAGE OF THE CHANGE IN 'IDS' DIVIDED BY
C THE CHANGE IN 'VGS'.
    IF(J.EQ.1)GO TO 2030
    IF(J.EQ.NCUR)GO TO 2040
    GM=(EID(J+1,I)-EID(J-1,I))/(VG(J+1)-VG(J-1))
    II(J,I)=(1+GM*RS)*EID(J,I)
    GO TO 2010
  2030 GM=(EID(J+1,I)-EID(J,I))/(VG(J+1)-VG(J))
    II(J,I)=(1+GM*RS)*EID(J,I)
    GO TO 2010
  2040 GM=(EID(J,I)-EID(J-1,I))/(VG(J)-VG(J-1))
    II(J,I)=(1+GM*RS)*EID(J,I)
    GO TO 2010
  2020 BPT=I
  2010 CONTINUE
    ISTART(J)=BPT+1
C ------------------------
2000 CONTINUE
RETURN
END
SUBROUTINE OPTI(K)
C THE VALUE OF 'NCUR' IS THE CURVE NUMBER.
C #3000

DIMENSION EID(15,50),IID(15,50)
DIMENSION VG(15),VD(50),VDI(15,50),ISTART(15)
DIMENSION REGI(15),REGII(15)
DIMENSION ERROR(3,3,3,3),ERROR2(3,3,3,3),ERROR3(3,3,3,3)
INTEGER NCUR, NPT,ISTART,ITER
INTEGER I,II,J,K,K1,K2,K3,K4
INTEGER CNT,PCNT,IB,JB,KB,LB
INTEGER REGI,REGII,IMOVE,CLICK
REAL*8 EID,IID,VD,VDI,GV,VD,VD2,VDI
REAL*8 GM,RG,RD,RS,MINERR,MERR,ERRSUM
REAL*8 VT,BETA,LAMBDALPHA,B,DEV,TEMDV,KVOLT
REAL*8 VG2,BSTP,BESTP,LAMSTP,ALSTP,BSTP
REAL*8 TEMTB,TEMBE,TEMLAB,TEMVT,TEMA
REAL*8 ICAL,ERROR,ERROR2,ERROR3
COMMON /RECORD/ EID,IID,VD,VDI,VG
COMMON /STAT/ ISTART,NCUR,NPT,RG,RD,RS
COMMON /PARAS/ VT,BETA,LAMBDALPHA,B,DEV,KVOLT
COMMON /STAT2/ REGI,REGII,MINERR
C
READ(7,*)VT,BETA,LAMBDALPHA,B
WRITE(8,'(A)')' INITIAL VALUES FOR VT,BETA,LAMBDALPHA,B:
WRITE(8,3000)VT,BETA,LAMBDALPHA,B
3000 FORMAT(2X,'VT=',G10.4,2X,'BETA=',G10.4,2X,'LAMBDA=',G10.4,2X,'ALPHA=',G10.4,8X,'B=',G10.4)
WRITE(8,'(A)')'
READ(7,*)DEV
READ(7,*)KVOLT
WRITE(*,'(A)')' **** PLEASE WAIT **** '
C -------------------------------
C DIVIDE THE I-V CURVE INTO THEIR TWO REGIONS
C OF OPERATION. REGION I=[Vds <= Vgs + Vt]
C REGION II=[Vds => Vgs + Vt].
DO 3010 J=1,NCUR
CNT=0
DO 3020 I=ISTART(J),NPT
IF(VDI(J,I).LE.(3.0/ALPHA))CNT=CNT+1
3020 CONTINUE
REGI(J)=CNT-1
REGII(J)=CNT+1
3010 CONTINUE
C -------------------------------
C DEFINE THE STEP SIZE OF THE VARIABLES.
C MAXIMUM INCREMENT OF <+,-> 10 STEPS.
ITER=0
MINERR=1.0E30
TEMDEV=DEV

C THIS IS WHERE REITERATION RETURNS TO.

3190 ITER=ITER+1
VTSTP=TEMDEV*VT/2000.0
BESTP=TEMDEV*BETA/2000.0
LAMSTP=TEMDEV*LAMBDA/100.0
ALSTP=TEMDEV*ALPHA/100.0
BSTP=TEMDEV*B/100.0

C DO A FIT IN REGION II ONLY UP TO KINK VOLTAGE.
C ASSUME A FIX VT VOLTAGE.
C REGION II DOES NOT HAVE ALPHA EXPRESSION.
C

C7 DO 3090 II=1,100
    TEMB=B-BSTP
    TEMBE=BETA-BESTP
    TEMLAM=LAMBDA-LAMSTP
    TEMVT=VT-VTSTP

C6 DO 3080 K1=1,3
C5 DO 3070 K2=1,3
C4 DO 3060 K3=1,3
C3 DO 3050 K4=1,3
ERROR(K1,K2,K3,K4)=0
ERROR2(K1,K2,K3,K4)=0
ERROR3(K1,K2,K3,K4)=0
PCNT=0

C2 DO 3040 J=1,NCUR
    IMOVE=(NPT-REGII(J))/4
C1 DO 3030 I=REGII(J),NPT,IMOVE
    IF(ISTART(J).GE.NPT)GO TO 3030
    IF(VDI(J,I).GT.KVOLT)GO TO 3030
    ICAL=TEMBE*(((VG(J)-TEMVT)**2)*(1+TEMLAM*VDI(J,I)))/
          (1+TEMB*(VG(J)-TEMVT))
\[ \text{ERROR2}(K_1, K_2, K_3, K_4) = \text{ERROR2}(K_1, K_2, K_3, K_4) + \text{DABS}(\frac{\text{IID}(J, I) - \text{ICAL}}{1}) + 1 \]

\[ \text{ERROR}(K_1, K_2, K_3, K_4) = \text{ERROR}(K_1, K_2, K_3, K_4) + \\sqrt{\left(\frac{\text{IID}(J, I) - \text{ICAL}}{1}\right)^2} \]

\[ \text{ERROR3}(K_1, K_2, K_3, K_4) = \text{ERROR3}(K_1, K_2, K_3, K_4) + (\text{IID}(J, I) - \text{ICAL}) \]

\[ \text{PCNT} = \text{PCNT} + 1 \]

\[ \text{CONTINUE} \]

\[ \text{TEMlam} = \text{TEMlam} + \text{Lamstp} \]

\[ \text{CONTINUE} \]

\[ \text{TEMB} = \text{TEMB} + \text{BSTP} \]

\[ \text{CONTINUE} \]

\[ \text{TEMV} = \text{TEMV} + \text{VTSP} \]

\[ \text{CONTINUE} \]

\[ \text{FIND THE BEST MOVE.} \]

\[ \text{IB} = 1 \]
\[ \text{JB} = 1 \]
\[ \text{KB} = 1 \]
\[ \text{LB} = 1 \]
\[ \text{CLICK} = 0 \]
\[ \text{DO 3130 IB} = 1, 3 \]
\[ \text{DO 3120 JB} = 1, 3 \]
\[ \text{DO 3110 KB} = 1, 3 \]
\[ \text{DO 3100 LB} = 1, 3 \]

\[ \text{ERRSUM} = (\text{ERRSUM} + (\text{ERROR}(\text{IB}, \text{JB}, \text{KB}, \text{LB})/(0.25*\text{PCNT})) + 1 \]
\[ \text{ERRSUM} = \text{ERRSUM} + (\text{ERROR}(\text{IB}, \text{JB}, \text{KB}, \text{LB})/(0.05*\text{PCNT})) + 1 \]
\[ \text{ERRSUM} = \text{ERRSUM} + (\text{DABS}(\text{ERROR3}(\text{IB}, \text{JB}, \text{KB}, \text{LB})/(0.1*\text{PCNT})) + 1 \]

\[ \text{IF} (\text{ERRSUM} \gt \text{MINERR}) \text{GO TO 3100} \]
\[ \text{IF} (\text{ERRSUM} = \text{MINERR}) \text{GO TO 3100} \]
\[ \text{MINERR} = \text{ERRSUM} \]
\[ \text{K4} = \text{LB} \]
\[ \text{K3} = \text{KB} \]
\[ \text{K2} = \text{JB} \]
\[ \text{K1} = \text{IB} \]
CLICK=1
3100 CONTINUE
3110 CONTINUE
3120 CONTINUE
3130 CONTINUE

IF(CLIK.EQ.0) GO TO 3140
GO TO 3250
3140 WRITE(8,3200)MINERR,PCNT
3200 FORMAT(2X,'MIMUM SUM OF ERROR=',G10.4,5X,15)
C    MERR=(MINERR)/DBLE(PCNT)
C WRITE(8,3210)MERR,PCNT
C3210 FORMAT(2X,'THE MEAN ERROR PER A POINT=',G10.4,2X,15)
     GO TO 3240
C
C CHANGE THE PARAMETER ACCORDINGLY.
C
3250 IF(K1.EQ.1) THEN
    VT = VT - VTSTP
ELSEIF(K1.EQ.3) THEN
    VT = VT + VTSTP
ELSE
    VT = 1.0*VT
ENDIF

IF(K2.EQ.1) THEN
    B = B - BSTP
ELSEIF(K2.EQ.3) THEN
    B = B + BSTP
ELSE
    B = 1.0*B
ENDIF

IF(K3.EQ.1) THEN
    BETA = BETA - BESTP
ELSEIF(K3.EQ.3) THEN
    BETA = BETA + BESTP
ELSE
    BETA = 1.0*BETA
ENDIF

IF(K4.EQ.1) THEN
    LAMBDA = LAMBDA - LAMSTP
ELSEIF(K4.EQ.3) THEN
    LAMBDA = LAMBDA + LAMSTP
ELSE
    LAMBDA = 1.0*LAMBDA
ENDIF
3090 CONTINUE
C7 --------------
C
C A OPTIMUM HAS BEEN FOUND
C
WRITE(*,'(A)')' *** MAXIMUM ITERATION *** '
WRITE(8,3200)MINERR,PCNT
C MERR=(MINERR)/DBLE(PCNT)
C WRITE(8,3210)MERR,PCNT
GOTO 3150
3240 WRITE(*,'(A)')' *** SUCCESS! A OPTIMUM HAS BEEN FOUND *** '
TEMDEV=(TEMDEV/50.0)
3150 WRITE(8,3160)VT,BETA,LAMBDA
3160 FORMAT(2X,' VT=',G10.4,' BETA=',G10.4,' LAMBDA=',G10.4)
WRITE(8,3170)ALPHA,B
3170 FORMAT(2X,' ALPHA=',G10.4,' B=',G10.4)
IF(MINERR.LE.(2.0))GO TO 3180
WRITE(*,'(A)')' **** ERROR > 5% ITERATE AGAIN **** '
IF(ITER.GE.10)GO TO 3180
GO TO 3190
C #3200-MAXIMUM
3180 RETURN
END
SUBROUTINE OPTII(K)
C THE VALUE OF ' NCUR ' IS THE CURVE NUMBER.
C #4000

DIMENSION EID(15,50),IID(15,50)
DIMENSION VG(15),VD(50),VDI(15,50),ISTART(15)
DIMENSION REGI(15),REGII(15)
DIMENSION ERROR(3,3,3,3),ERROR2(3,3,3,3),ERROR3(3,3,3,3)
INTEGER NCUR, NPT,ISTART,ITER
INTEGER I,II,J,K,K1,K2,K3,K4
INTEGER CNT,PCNT,IB,JB,KB,LB
INTEGER REGI,REGII,IMOVE,CLICK
REAL*8 EID,IID,VG,VD,VDI
REAL*8 GM,RG,RD,RS,MINERR,MERR,ERRSUM
REAL*8 VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
REAL*8 VTSTP,BESTP,LAMSTP,ALSTP,BSTP
REAL*8 TEMB,TEMBE,TEMLAB,TEMVT,TEMAL
REAL*8 ICAL,ERROR,ERROR2,ERROR3
COMMON /RECORD/ EID,IID,VD,VDI,VG
COMMON /STAT/ ISTART,NCUR,NPT,RG,RD,RS
COMMON /PARAS/ VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
COMMON /STAT2/ REGI,REGII,MINERR

C DEFINE THE STEP SIZE OF THE VARIABLES.
C MAXIMUM INCREMENT OF <+,-> 10 STEPS.
C
WRITE(*,'(A)')' ***** OPTIMIZATION II IN PROGRESS ***** ',
WRITE(*,'(A)')' ***** PLEASE WAIT **** ',
ITER=0
MINERR=1.0E30

C THIS IS WHERE REITERATION RETURNS TO.
C
4260 ITER=ITER+1
VTSTP=DEV*VT/1000.0
BESTP=DEV*BETA/1000.0
LAMSTP=DEV*LAMBDA/1000.0
ALSTP=DEV*ALPHA/100.0
BSTP=DEV*B/1000.0

C DO A FIT IN REGION I,II ONLY UP TO KINK VOLTAGE.
C ASSUME A FIX VALUE FOR BETA,LAMBDA,B.
C FIND THE LINEAR REGION FINAL POINT.
DO 4000 J=1,NCUR
   CNT=0
   DO 4010 I=1,NPT
      IF(VDI(J,I).GT.(3.0/ALPHA))GO TO 4010
      CNT=CNT+1
   4010 CONTINUE
   REGI(J)=CNT
4000 CONTINUE

C FIND THE POINT WHERE KINK VOLTAGE COME INTO PLAY

DO 4020 J=1,NCUR
   CNT=0
   DO 4030 I=1,NPT
      IF(VDI(J,I).GT.KVOLT)GO TO 4030
      CNT=CNT+1
   4030 CONTINUE
   REGII(J)=CNT
4020 CONTINUE

C7 DO 4100 11=1,100
   TEMAL=ALPHA-ALSTP
C6 K1=ALPHA-
   DO 4090 Kl=l,3
C5 K2=BETA--
   DO 4080 K2=l,3
C4 K3=LAMBDA
   DO 4070 K3=l,3
C3 K4=B :
   DO 4060 K4=l,3
   ERRORC Kl,K2,K3,K4)=0.0
   ERROR2(Kl,K2,K3,K4)=0.0
   ERROR3(Kl,K2,K3,K4)=0.0
   PCNT=0
C2 DO 4050 J=1,NCUR
   IMOVE=(REGII(J)-ISTART(J))/8
   DO 4040 I=ISTART(J),REGII(J),IMOVE
      IF(ISTART(J).GE.NPT)GO TO 4040
      IF(I.GT.REGI(J))GO TO 4110
      **** LINEAR REGION ****
      ICAL=(BETA*(((VG(J)-VT)**2)*(1+LAMBDA*VDI(J,I))
      *((1-(1-(TEMAL*VDI(J,I)/3)**3)/(1+B*(VG(J)-VT)))

C1 -----------------
ERROR2(K1,K2,K3,K4) = ERROR2(K1,K2,K3,K4) + DABS((IID(J,I) - ICA)/
   IID(J,I))

ERROR(K1,K2,K3,K4) = ERROR(K1,K2,K3,K4) + DABS(IID(J,I) - ICA)
ERROR3(K1,K2,K3,K4) = ERROR3(K1,K2,K3,K4) + (IID(J,I) - ICA)
PCNT = PCNT + 1
GO TO 4040

C ***** SATURATION REGION *****
4110 ICAL = BETA*((VG(J) - VT)**2)*(1+LAMBDA*VDI(J,I))/
   (1+B*(VG(J) - VT))

ERROR2(K1,K2,K3,K4) = ERROR2(K1,K2,K3,K4) + DABS((IID(J,I) - ICA)/
   IID(J,I))

ERROR(K1,K2,K3,K4) = ERROR(K1,K2,K3,K4) + DABS(IID(J,I) - ICA)
ERROR3(K1,K2,K3,K4) = ERROR3(K1,K2,K3,K4) + (IID(J,I) - ICA)
PCNT = PCNT + 1
4040 CONTINUE
4050 CONTINUE
C
C FIND THE BEST MOVE.
C
IB=1
JB=1
KB=1
LB=1
CLICK=0
DO 4150 IB=1, 3
    DO 4140 JB=1: ,3
        DO 4130 KB=1, ,3
            DO 4120 LB=1 ,3
                ERRSUM=(ERROR2(IB,JB,KB,LB)/(1.50*PCNT))+
                    1 (ERROR(IB,JB,KB,LB)/(0.1E-3*PCNT))+
                    1 DABS(ERROR3(IB,JB,KB,LB))/(0.10E-3*PCNT)
                IF(ERRSUM.GT.MINERR)GO TO 4120
                IF(ERRSUM.EQ.MINERR)GO TO 4120
                MINERR=ERRSUM
                K4=LB
                K3=KB
                K2=JB
                K1 = IB
                CLICK=1
        CONTINUE
    CONTINUE
4130 CONTINUE
4140 CONTINUE
4150 CONTINUE

4120 CONTINUE
4130 CONTINUE
4140 CONTINUE
4150 CONTINUE

IF(CLICK.EQ.0)GO TO 4160
GO TO 4170
4160 WRITEC8,4200)MINERR,PCNT
4200 FORMATC2X,'MINIMUM SUM OF SQUARE ERROR=',GIO.4,5X,15)+
        C MERR=(MINERR)/DBLE(PCNT)
        C WRITEC8,4210)MERR,PCNT
4210 FORMATC2X,'THE MEAN DEVIATION PER POINT=',GIO.4,2X,2I5)
        GO TO 4250

C----------------------------------------------
C CHANGE THE PARAMETER ACCORDINGLY.
C
4170 IF(K4.EQ.1)THEN
    B=1.0*B
    C
    ELSEIF(K4.EQ.3)THEN
    B=1.0*B
    C
    ELSE
B=1.0*B
ENDIF

IF(K3.EQ.1)THEN
  LAMBDA=1.0*LAMBDA
ELSEIF(K3.EQ.3)THEN
  LAMBDA=1.0*LAMBDA
ELSE
  LAMBDA=1.0*LAMBDA
ENDIF

IF(K2.EQ.1)THEN
  BETA=1.0*BETA
ELSEIF(K2.EQ.3)THEN
  BETA=1.0*BETA
ELSE
  BETA=1.0*BETA
ENDIF

IF(K1.EQ.1)THEN
  ALPHA=ALPHA-ALSTP
ELSEIF(K1.EQ.3)THEN
  ALPHA=ALPHA+ALSTP
ELSE
  ALPHA=1.0*ALPHA
ENDIF

4100 CONTINUE
C5  -----------------------------

C A OPTIMUM HAS BEEN FOUND
C
WRITE(*,'(A)')' *** MAXIMUM ITERATION *** '
WRITE(8,4200)MINERR,PCNT
C MERR=(MINERR)/DBLE(PCNT)
C WRITE(8,4210)MERR,PCNT
GOTO 4270
4250 WRITE(*,'(A)')' *** SUCCESS! A OPTIMUM HAS BEEN FOUND *** '
    DEV=(DEV/100.0)
4270 WRITE(8,4280)VT,BETA,LAMBDA
4280 FORMAT(2X,' VT=',G10.4,' BETA=',G10.4,' LAMBDA=',G10.4)
WRITE(8,4180)ALPHA,B
4180 FORMAT(2X,' ALPHA=',G10.4,' B= ',G10.4)
IF(MINERR.LE.(2.00))GO TO 4190
WRITE(*,'(A)')' **** ERROR > 5% ITERATE AGAIN **** '
IF(ITER.GE.10)GO TO 4190
GO TO 4260
C #4300-MAXIMUM
4190 RETURN
END
SUBROUTINE MEASII(K)
C THE VALUE OF ' NCUR ' IS THE CURVE NUMBER.
C #4000

DIMENSION EID(15,50),IID(15,50),ICAL(15,50)
DIMENSION VG(15),VD(50),VDI(15,50),ISTART(15)
DIMENSION REGI(15),REGII(15),ERROR(15,50)
INTEGER NCUR,NPT,ISTART
INTEGER I,J,CNT,PCNT,REGI,REGII
REAL*8 EID,IID,VG,VD,VDI
REAL*8 GM,RG,RD,RS,MINERR,MERR
REAL*8 VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
REAL*8 ICAL,ERROR
COMMON /RECORD/ EID,IID,VD,VDI,VG
COMMON /STAT/ ISTART,NCUR,NPT,RG,RD,RS
COMMON /PARAS/ VT,BETA,LAMBDA,ALPHA,B,DEV,KVOLT
COMMON /STAT2/ REGI,REGII,MINERR

C DEFINE THE STEP SIZE OF THE VARIABLES.
C MAXIMUM INCREMENT OF <+,-> 10 STEPS.
C
WRITE(*,'(A)')' **** PLEASE WAIT ****'

C
DO 4000 J=1,NCUR
  CNT=0
  DO 4010 I=1,NPT
    IF(VDI(J,I).GT.(3.0/ALPHA))GO TO 4010
    CNT=CNT+1
  4010 CONTINUE
  REGI(J)=CNT
4000 CONTINUE

C FIND THE POINT WERE KINK VOLTAGE COME INTO PLAY
C
DO 4020 J=1,NCUR
  CNT=0
  DO 4030 I=1,NPT
    IF(VDI(J,I).GT.KVOLT)GO TO 4030
    CNT=CNT+1
  4030 CONTINUE
  REGII(J)=CNT
4020 CONTINUE
C ------------------------------------------
C CALCULATE THE I-V CURRENTS AND DETERMINE
C ERROR.
C ------------------------------------------

C2 DO 4050 J=1,NCUR
C1 DO 4040 I=ISTART(J),REGII(J)
         IF(ISTART(J).GE.NPT)GO TO 4040
         IF(I.GT.REGI(J))GO TO 4090

C **** LINEAR REGION ****
ICAL(J,I)=(BETA*((VG(J)-VT)**2)*(1+LAMBDA*VDI(J,I))
          *(1-(1-(ALPHA*VDI(J,I)/3)**3))/(1+B*(VG(J)-VT))
         ERROR(J,I)=DABS((IID(J,I)-ICAL(J,I))/
          IID(J,I))
         GO TO 4040

C **** SATURATION REGION ****
4090 ICAL(J,I)=BETA*((VG(J)-VT)**2)*(1+LAMBDA*VDI(J,I))/
          (1+B*(VG(J)-VT))
         ERROR(J,I)=DABS((IID(J,I)-ICAL(J,I))/
          IID(J,I))
4040 CONTINUE
4050 CONTINUE
C1 ------------------------------------------
C2 ------------------------------------------

C ------------------------------------------
C WRITE OUT THE EXTERNAL, INTERNAL, AND
C CALCULATED CURRENT.
C ------------------------------------------

WRITE(8,'(A)')
DO 4100 J=1,NCUR
         IF(ISTART(J).GE.REGII(J))GO TO 4100
         WRITE(8,4110)VG(J),ISTART(J)
4110 FORMAT(5X,'VG=',G10.4,3X,'ISTART=',I7)

WRITE(8,'(A)')' Vds (V) COMPENSATED Ids (A)
CALCULATED Ids
1(A) PERCENT ERROR '
WRITE(8,'(A)')

*------------------------------------------*
1---
*------------------------------------------*

WRITE(8,4120)(VDI(J,I),IID(J,I),ICAL(J,I),
         ERROR(J,I),I=ISTART(J),REGII(J))

4120 FORMAT(3X,G10.4,6X,G10.4,12X,G10.4,9X,G10.4)
4100 CONTINUE
C #4200
RETURN
END
DEPLETION MODE MESFET (30C)

L=0.5UM, W=250UM
DEPLETION MODE MESFET (40C)

L=0.5 µM, W=50 µM
DEPLETION MODE MESFET (50C)

$L=0.5\text{UM}, W=50\text{UM}$
DEPLETION MODE MESFET (60C)

L=0.50UM, W=500UM

Vds (volts)

Vds (volts)

Ids (amps)
DEPLETION MODE MESFET (80C)

L=0.5UM, W=50UM

Id (amps) vs Vds (volts)

0.00E+00 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0

0.00E+00 0.10E-02 0.20E-02 0.30E-02 0.40E-02 0.50E-02 0.60E-02 0.70E-02 0.80E-02 0.90E-02 1.00E-02 1.10E-02 1.20E-02
ENHANCEMENT MODE MESFET (31C)

L=0.5UM, W=250UM

Graph showing the relationship between Vds (volts) and Ids (amps) for an enhancement mode MESFET.
ENHANCEMENT MODE MESFET (40C)

L=0.50UM, W=250UM
ENHANCEMENT MODE MESFET (60C)

$V_{ds}$ (volts)

$I_{ds}$ (amps)

$L = 0.5 \mu m$, $W = 250 \mu m$
ENHANCEMENT MODE MESFET (70C)

$V_{DS}$ (volts) vs $I_{DS}$ (amps) for $L=0.5\mu m$, $W=250\mu m$
ENHANCEMENT MODE MESFET (30C)

L=0.5UM, W=250UM

ids (amps)

Vds (volts)
ENHANCEMENT MODE MESFET (90°C)

Lp 0.5um, W = 250um

Vds (volts)

Id (amps)
VOLTAGE REFERENCE -10C

**** CIRCUIT DESCRIPTION

* ALL THE SUPPLY VOLTAGES.

VSS 8 0 DC -5.0V
VB1 5 0 DC -3.78V

* CIRCUIT
* ACTIVE DEVICES

BENH1 1 17 7 EMES-10 250.0
BDNP1 4 6 7 DMES-10 125.0
BDL1 0 1 1 DMES-10 31.0
BDL2 0 2 2 DMES-10 31.0
BBIAS2 7 8 8 DMES-10 65.0

* LEVEL SHIFT DIODE
D1 2 4 DIMOD 300

* IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10

* BIAS CIRCUIT
BB1 0 15 15 DMES-10 8
BB2 15 16 16 DMES-10 8
BB3 16 17 17 DMES-10 8
BB4 17 8 8 DMES-10 8
VON 18 0 DC -4.52

* CONTROL CARDS
.WIDTH OUT=80
.TEMP -10
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.36V V(2)=-1.36V V(4)=-1.99V V(6)=-4.52V V(7)=-4.0V
  + V(9)=-4.52V V(15)=-1.25V V(16)=-2.51V V(17)=-3.77V

.MODEL EMES-10 GASFET VTO=-0.02816 VBI=0.65 ALPHA=3.465 BETA=5.379E-5
  + LAMBDA=0.5024 RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
  + TAU=0.0 KF=0.0 AF=1
.MODEL DMES-10 GASFET VTO=-0.0262 VBI=0.65 ALPHA=4.875 BETA=14.66E-5
  + LAMBDA=0.1676 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
  + TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15 RS=28.0 VJ=0.65
.END
VOLTAGE REFEREANCE -10C

**** SMALL SIGNAL BIAS SOLUTION  TEMPERATURE = -10.000 DEG C

*********************************************************************************************************************************************************************************************************

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 1)</td>
<td>-1.3946</td>
<td>( 2)</td>
<td>-1.3950</td>
<td>( 4)</td>
<td>-2.0241</td>
<td>( 6)</td>
<td>-4.5007</td>
</tr>
<tr>
<td>( 7)</td>
<td>-4.0379</td>
<td>( 8)</td>
<td>-5.0000</td>
<td>( 9)</td>
<td>-4.5007</td>
<td>(15)</td>
<td>-1.2500</td>
</tr>
<tr>
<td>(16)</td>
<td>-2.5000</td>
<td>(17)</td>
<td>-3.7500</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VOLTAGE SOURCE CURRENTS

NAME     CURRENT

VSS      6.111D-03

TOTAL POWER DISSIPATION 3.06D-02 WATTS
VOLTAGE REFERENCE 0C

**** CIRCUIT DESCRIPTION

***********************************************************************
* ALL THE SUPPLY VOLTAGES.
* VSS 8 0 DC -5.0V
* VBI 5 0 DC -3.78V
* CIRCUIT
* ACTIVE DEVICES
* BENG1 1 17 7 EMESO 250.0
BDEP1 4 6 7 DMESO 125.0
BDL1 0 1 1 DMESO 31.0
BDL2 0 2 2 DMESO 31.0
BBIAS2 7 8 8 DMESO 65.0
* LEVEL SHIFT DIODE
D1 2 4 DIMOD 300
* IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
* BIAS CIRCUIT *
BB1 0 15 15 DMESO 8
BB2 15 16 16 DMESO 8
BB3 16 17 17 DMESO 8
BB4 17 8 8 DMESO 8
VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 0
.OP
 OPTIONS TNOM=30
.NODESET V(1)=-1.36V V(2)=-1.36V V(4)=-1.97V V(6)=-4.52V V(7)=-4.0V
+ V(9)=-4.52V V(15)=-1.25V V(16)=-2.51V V(17)=-3.77V

.MODEL EMESO GASFET VTO=-0.02909 VBI=0.65 ALPHA=3.465 BETA=5.182E-5
+ LAMBDA=0.5016 RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMESO GASFET VTO=-0.8271 VBI=0.65 ALPHA=4.875 BETA=14.12E-5
+ LAMBDA=0.1666 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15 RS=28.0 VJ=0.65
.END
VOLTAGE REFERENCE : Vc

**** SMALL SIGNAL BIAS SOLUTION  TEMPERATURE = 000 DEG C

**************************************************************************************************************************

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 1)</td>
<td>-1.3939</td>
<td>( 2)</td>
<td>-1.3943</td>
<td>( 4)</td>
<td>-2.0018</td>
<td>( 6)</td>
<td>-4.5011</td>
</tr>
<tr>
<td>( 7)</td>
<td>-4.0382</td>
<td>( 8)</td>
<td>-5.0000</td>
<td>( 9)</td>
<td>-4.5011</td>
<td>(15)</td>
<td>-1.2500</td>
</tr>
<tr>
<td>(16)</td>
<td>-2.5000</td>
<td>(17)</td>
<td>-3.7500</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VOLTAGE SOURCE CURRENTS

NAME   CURRENT

VSS   5.952D-03

TOTAL POWER DISSIPATION  2.98D-02 WATTS
VOLTAGE REFERENCE 10C

**** CIRCUIT DESCRIPTION

**************************************************
*
* ALL THE SUPPLY VOLTAGES.
* VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.60V
*
* CIRCUIT
* ACTIVE DEVICES
*
BENH1 1 17 7 EMES10 250.0
BDEP1 4 6 7 DMES10 125.0
BDL1 0 1 1 DMES10 31.0
BDL2 0 2 2 DMES10 31.0
BBIAS2 7 8 8 DMES10 65.0
*
* LEVEL SHIFT DIODE
D1 2 4 DIMOD 300
*
* IDEAL OPAMP
RINF 2 1 1.0E15
EDUT 9 0 2 1 1E4
RBK 9 6 10
*
* BIAS CIRCUIT *
BB1 0 15 15 DMES10 8
BB2 15 16 16 DMES10 8
BB3 16 17 17 DMES10 8
BB4 17 8 8 DMES10 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 10
.OF
.OPTIONS TNUM=30
.NODESET V(1)=-1.36V V(2)=-1.36V V(4)=-1.95V V(6)=-4.52V V(7)=-4.06V
+ V(9)=-4.52V V(15)=-1.25V V(16)=-2.51V V(17)=-3.77V

.MODEL EMES10 GASFET VTO=-0.03003 VBI=0.65 ALPHA=3.465 BETA=4.99E-5
+ LAMBDA=0.50008 RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES10 GASFET VTO=-0.8279 VBI=0.65 ALPHA=4.875 BETA=13.62E-5
+ LAMBDA=0.1657 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15 RS=28.0 VJ=0.65
.END
VOLTAGE REFERENCE 10C

**** SMALL SIGNAL BIAS SOLUTION  TEMPERATURE =  10.000 DEG C

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1)</td>
<td>-1.3928</td>
<td>(2)</td>
<td>-1.3932</td>
<td>(4)</td>
<td>-1.9791</td>
<td>(6)</td>
<td>-4.5016</td>
</tr>
<tr>
<td>(7)</td>
<td>-4.0386</td>
<td>(8)</td>
<td>-5.0000</td>
<td>(9)</td>
<td>-4.5016</td>
<td>(15)</td>
<td>-1.2500</td>
</tr>
<tr>
<td>(16)</td>
<td>-2.5001</td>
<td>(17)</td>
<td>-3.7501</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VOLTAGE SOURCE CURRENTS

<table>
<thead>
<tr>
<th>NAME</th>
<th>CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>5.801D-03</td>
</tr>
</tbody>
</table>

TOTAL POWER DISSIPATION  2.90D-02 WATTS
VOLTAGE REFERENCE 20C

**** CIRCUIT DESCRIPTION

************************************************************

* ALL THE SUPPLY VOLTAGES.
* VSS 8 0 DC -5.0V
* VB1 5 0 DC -3.78V
*
* CIRCUIT
* ACTIVE DEVICES
*
Benh1 1 17 7 EMES20 250.0
Bdep1 4 6 7 DMES20 125.0
BDL1 0 1 1 DMES20 31.0
BDL2 0 2 2 DMES20 31.0
BBias2 7 8 8 DMES20 65.0
*
* LEVEL SHIFT DIODE
D1 2 4 DMOD 300
*
* IDEAL OPAMP
RInf 2 1 1.0E15
EOut 9 0 2 1 1E4
RBK 9 6 10
*
* BIAS CIRCUIT *
BB1 0 15 15 DMES20 8
BB2 15 16 16 DMES20 8
BB3 16 17 17 DMES20 8
BB4 17 8 8 DMES20 8
*Von 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 20
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.37V V(2)=-1.37V V(4)=-1.93V V(6)=-4.52V V(7)=-4.05V
+ V(9)=-4.52V V(15)=-1.25V V(16)=-2.51V V(17)=-3.77V

.MODEL EMES20 GASFET VTO=-0.03097 VBI=0.65 ALPHA=3.465 BETA=4.8*10E-5
+ LAMBDA=0.5000 RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES20 GASFET VTO=-0.8287 VBI=0.65 ALPHA=4.875 BETA=13.16*10E-5
+ LAMBDA=0.1648 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMOD D IS=8E-15 RS=28.0 VJ=0.65
.END
VOLTAGE REFERENCE 20C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 20.000 DEG C

VOLTAGE SOURCE CURRENTS

<table>
<thead>
<tr>
<th>NAME</th>
<th>CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>5.660D-03</td>
</tr>
</tbody>
</table>

TOTAL POWER DISSIPATION 2.83D-02 WATTS
VOLTAGE REFERENCE 30C

**** CIRCUIT DESCRIPTION

* ALL THE SUPPLY VOLTAGES.
* VSS 8 0 DC -5.0V
* VB1 5 0 DC -3.60V
* CIRCUIT
* ACTIVE DEVICES
* BENH1 1 17 7 EMES30 250.0
  BDEP1 4 6 7 DMES30 125.0
  BDL1 0 1 1 DMES30 31.0
  BDL2 0 2 2 DMES30 31.0
  BBIAS2 7 8 8 DMES30 65.0
* LEVEL SHIFT DIODE
  D1 2 4 DIMOD 300
* IDEAL OPAMP
  RINF 2 1 1.0E15
  EOUT 9 0 2 1 1E4
  RBK 9 6 10
* BIAS CIRCUIT *
  BB1 0 15 15 DMES30 8
  BB2 15 16 16 DMES30 8
  BB3 16 17 17 DMES30 8
  BB4 17 8 8 DMES30 8
  VON 18 0 DC -4.52
* CONTROL CARDS
  .WIDTH OUT=80
  .TEMP 30
  .OP
  .OPTIONS TNOm=30
  .NODESET V(1)=-1.38V V(2)=-1.38V V(4)=-1.92 V(6)=-4.51V V(7)=-1.04V
  + V(9)=-4.52V V(15)=-1.25V V(16)=-2.50V V(17)=-3.75V
  .MODEL EMES30 GASFET VTO=-0.03191 VBI=0.65 ALPHA=3.465 BETA=4.638E-5
  + LAMBDA=0.4993 RG=129 RG=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
  + TAU=0.0 KF=0.0 AF=1
  .MODEL DMES30 GASFET VTO=-0.0296 VBI=0.65 ALPHA=4.8T5 BETA=12.7E-5
  + LAMBDA=0.1639 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
  + TAU=0.0 KF=0.0 AF=1
  .MODEL DIMOD D IS=8E-15 RS=28.0 VJ=0.65
.END
VOLTAGE REFERENCE 30°C

**** SMALL SIGNAL BIAS SOLUTION  TEMPERATURE = 30.000 DEG C

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-1.3898</td>
<td>2</td>
<td>-1.3903</td>
<td>4</td>
<td>-1.9324</td>
<td>6</td>
<td>-4.5038</td>
</tr>
<tr>
<td>7</td>
<td>-4.0404</td>
<td>8</td>
<td>-5.0000</td>
<td>9</td>
<td>-4.5038</td>
<td>15</td>
<td>-1.2503</td>
</tr>
<tr>
<td>16</td>
<td>-2.5006</td>
<td>17</td>
<td>-3.7510</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VOLTAGE SOURCE CURRENTS

<table>
<thead>
<tr>
<th>NAME</th>
<th>CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>5.523D-03</td>
</tr>
</tbody>
</table>

TOTAL POWER DISSIPATION  2.76D-02 WATTS
VOLTAGE REFERENCE 40C

CIRCUIT DESCRIPTION

************************************************************

* ALL THE SUPPLY VOLTAGES.

* VSS 8 0 DC -5.0V
* VB1 5 0 DC -3.60V
* CIRCUIT
* ACTIVE DEVICES

* BENH1 1 17 7 EMES40 250.0
* BDEP1 4 6 7 DMES40 125.0
* BDL1 0 1 1 DMES40 31.0
* BDL2 0 2 2 DMES40 31.0
* BBIAS2 7 8 8 DMES40 65.0

* LEVEL SHIFT DIODE
D1 2 4 DIMOD 300

* IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10

* BIAS CIRCUIT *
BB1 0 15 15 DMES40 8
BB2 15 16 16 DMES40 8
BB3 16 17 17 DMES40 8
BB4 17 8 8 DMES40 8
VON 18 0 DC -4.52

* CONTROL CARDS
.WIDTH OUT=80
.TEMP 40
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.40V V(2)=-1.40V V(4)=-1.92V V(6)=-4.50V V(7)=-4.04V
+ V(9)=-4.5V V(15)=-1.25V V(16)=-2.5V V(17)=-3.75V

.MODEL EMES40 GASFET VTO=-0.04129 VBI=0.65 ALPHA=3.465 BETA=4.52E-5
+ LAMBDA=0.4915 RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES40 GASFET VTO=-0.0380 VBI=0.65 ALPHA=4.875 BETA=17.32E-5
+ LAMBDA=0.1563 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15 RS=28.0 VJ=0.65
.END
VOLTAGE REFERENCE 40°C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 40.000 DEG C

***************************************************************************

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 1)</td>
<td>-1.4098</td>
<td>( 2)</td>
<td>-1.4102</td>
<td>( 4)</td>
<td>-1.9307</td>
<td>( 6)</td>
<td>-4.5032</td>
</tr>
<tr>
<td>( 7)</td>
<td>-4.0368</td>
<td>( 8)</td>
<td>-5.0000</td>
<td>( 9)</td>
<td>-4.5032</td>
<td>(15)</td>
<td>-1.2508</td>
</tr>
<tr>
<td>(16)</td>
<td>-2.5015</td>
<td>(17)</td>
<td>-3.7523</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VOLTAGE SOURCE CURRENTS

NAME CURRENT

VSS 5.465D-03

TOTAL POWER DISSIPATION 2.73D-02 WATTS
VOLTAGE REFERENCE 50C

CIRCUIT DESCRIPTION

* ALL THE SUPPLY VOLTAGES.

VSS 8 0 DC -5.0V
*VB1 5 0 DC -3.69V

CIRCUIT

ACTIVE DEVICES

BENH1 1 17 7 EMES50 250.0
BDEP1 4 6 7 DMES50 125.0
BDL1 0 1 1 DMES50 31.0
BDL2 0 2 2 DMES50 31.0
BBIAS2 7 8 8 DMES50 65.0

LEVEL SHIFT DIODE

D1 2 4 DIMOD 300

IDEAL OPAMP

RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10

BIAS CIRCUIT

BB1 0 15 15 DMES50 8
BB2 15 16 16 DMES50 8
BB3 16 17 17 DMES50 8
BB4 17 8 8 DMES50 8

VON 18 0 DC -4.52

CONTROL CARDS

.WIDTH OUT=80
.TEMP 50
.OPTIONS TNOM=30
.NODESET V(1)=-1.44V V(2)=-1.44V V(4)=-1.94V V(6)=-4.49V V(7)=-4.02V + V(9)=-4.49V V(15)=-1.24V V(16)=-2.49V V(17)=-3.74V

.MODEL EMES50 GASFET VTO=-0.05066 VBI=0.65 ALPHA=3.465 BETA=4.40E-5 + LAMBDA=0.4836 RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0 + TAU=0.0 KF=0.0 AF=1

.MODEL DMES50 GASFET VTO=-0.8463 VBI=0.65 ALPHA=4.875 BETA=11.93E-5 + LAMBDA=0.1453 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0 + TAU=0.0 KF=0.0 AF=1

.MODEL DIMOD D IS=8E-15 RS=28.0 VJ=0.65
.END
VOLTAGE REFERENCE 50°C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 50.000 DEG C

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-1.4382</td>
<td>2</td>
<td>-1.4386</td>
<td>4</td>
<td>-1.9373</td>
<td>6</td>
<td>-4.5038</td>
</tr>
<tr>
<td>7</td>
<td>-4.0352</td>
<td>8</td>
<td>-5.0000</td>
<td>9</td>
<td>-4.5038</td>
<td>15</td>
<td>-1.2518</td>
</tr>
<tr>
<td>16</td>
<td>-2.5037</td>
<td>17</td>
<td>-3.7555</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VOLTAGE SOURCE CURRENTS

NAME    CURRENT

VSS      5.393D-03

TOTAL POWER DISSIPATION 2.70D-02 WATTS
VOLTAGE REFERENCE 60C

**** CIRCUIT DESCRIPTION

* ALL THE SUPPLY VOLTAGES.
* VSS 8 0 DC -5.0V
* VB1 5 0 DC -3.60V
* CIRCUIT
* ACTIVE DEVICES
* BENH1 1 17 7 EMES60 250.0
BDEP1 4 6.7 DMES60 125.0
BDL1 0 1 1 DMES60 31.0
BDL2 0 2 2 DMES60 31.0
BBIAS2 7 8 8 DMES60 65.0
* LEVEL SHIFT DIODE
D1 2 4 DIMOD 300
* IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
* BIAS CIRCUIT *
BB1 0 15 15 DMES60 8
BB2 15 16 16 DMES60 8
BB3 16 17 17 DMES60 8
BB4 17 8 8 DMES60 8
*VON 18 0 DC -4.52
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 60
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.49V V(2)=-1.49V V(4)=-1.94 V(6)=-4.49V V(7)=-4.02V
+ V(9)=-4.49V V(15)=-1.249V V(16)=-2.48V V(17)=-3.72V

.MODEL EMES60 GASFET VTO=-0.06002 VBI=0.65 ALPHA=3.465 BETA=4.50E-5
+ LAMBDA=0.4758 RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES60 GASFET VTO=-0.8546 VBI=0.65 ALPHA=4.875 BETA=11.58E-5
+ LAMBDA=0.1360 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15 RS=28.0 VJ=0.65
.END
**VOLTAGE REFERENCE 60°C**

**** SMALL SIGNAL BIAS SOLUTION  

TEMPERATURE = 60.000 DEG C

---------------------------------------------------------------------------------------------------------------

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1)</td>
<td>-1.4614</td>
<td>(2)</td>
<td>-1.4618</td>
<td>(4)</td>
<td>-1.9386</td>
<td>(6)</td>
<td>-4.5081</td>
</tr>
<tr>
<td>(7)</td>
<td>-4.0369</td>
<td>(8)</td>
<td>-5.0000</td>
<td>(9)</td>
<td>-4.5081</td>
<td>(15)</td>
<td>-1.540</td>
</tr>
<tr>
<td>(16)</td>
<td>-2.5080</td>
<td>(17)</td>
<td>-3.7621</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VOLTAGE SOURCE CURRENTS**

<table>
<thead>
<tr>
<th>NAME</th>
<th>CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>5.333D-03</td>
</tr>
</tbody>
</table>

**TOTAL POWER DISSIPATION** 2.67D-02 WATTS
VOLTAGE REFERENCE 70C

**** CIRCUIT DESCRIPTION

**********************************************************************
* ALL THE SUPPLY VOLTAGES.
* VSS 8 0 DC -5.0V
* VB1 5 0 DC -3.60V
*
* CIRCUIT
* ACTIVE DEVICES
*
BENH1 1 17 7 EMES70 250.0
BDEP1 4 6 7 DMES70 125.0
BDL1 0 1 1 DMES70 31.0
BDL2 0 2 2 DMES70 31.0
BBIAS2 7 8 8 DMES70 65.0
*
* LEVEL SHIFT DIODE
D1 2 4 DIMOD 300
*
* IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*
* BIAS CIRCUIT *
BB1 0 15 15 DMES70 8
BB2 15 16 16 DMES70 8
BB3 16 17 17 DMES70 8
BB4 17 8 8 DMES70 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 70
.OPTIONS TNOM=30
.NODESET V(1)=-1.53V V(2)=-1.53V V(4)=-1.99 V(6)=-4.46V V(7)=-3.99V
+ V(9)=-4.46V V(15)=-1.24V V(16)=-2.48V V(17)=-3.72V

.MODEL EMES70 GASFET VTO=-0.06941 VBI=0.65 ALPHA=3.465 BETA=4.20E-5
+ LAMBDA=0.4680 RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES70 GASFET VTO=-0.8554 VBI=0.65 ALPHA=4.875 BETA=11.24E-5
+ LAMBDA=0.1266 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15 RS=28.0 VJ=0.65
.END
VOLTAGE REFERENCE 70°C

**** SMALL SIGNAL BIAS SOLUTION

TEMPERATURE = 70.000 DEG C

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-1.4844</td>
<td>2</td>
<td>-1.4848</td>
<td>4</td>
<td>-1.9392</td>
<td>6</td>
<td>-4.5107</td>
</tr>
<tr>
<td>7</td>
<td>-4.0411</td>
<td>8</td>
<td>-5.0000</td>
<td>9</td>
<td>-4.5107</td>
<td>15</td>
<td>-1.2579</td>
</tr>
<tr>
<td>16</td>
<td>-2.5159</td>
<td>17</td>
<td>-3.7738</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VOLTAGE SOURCE CURRENTS

<table>
<thead>
<tr>
<th>NAME</th>
<th>CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>5.189D-03</td>
</tr>
</tbody>
</table>

TOTAL POWER DISSIPATION 2.59D-02 WATTS
VOLTAGE REFEREANCE 80C

**** CIRCUIT DESCRIPTION

******************************************************************************
* AL!E THE SUPPLY VOLTAGES.
* VSS 8 0 DC -5.0V
* VBI 5 0 DC -3.60V
* CIRCUIT
* ACTIVE DEVICES
* BENH1 1 17 7 EMESBO 250.0
BDEP1 4 6 7 DMESBO 125.0
BDL1 0 1 1 DMESBO 31.0
BDL2 0 2 2 DMESBO 31.0
BBIAS2 7 8 8 DMESBO 65.0
* LEVEL SHIFT DIODE
Dl 2 4 DIMOD 300
* IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
* BIAS CIRCUIT *
BB1 0 15 15 DMESBO B
BB2 15 16 16 DMESBO B
BB3 16 17 17 DMESBO B
BB4 17 8 8 DMESBO B
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 80
.OP
.OPTIONS TNOM=30
.NOSET V(1)=-1.60V V(2)=-1.60V V(4)=-2.03V V(6)=-4.42V V(7)=-3.95V
+ V(9)=-4.41V V(15)=-1.22V V(16)=-2.44V V(17)=-3.67V

.MODEL EMESBO GASFET VTO=-0.07879 VBI=0.65 ALPHA=3.465 BETA=4.10E-5
+ LAMBDA=0.4601 RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMESBO GASFET VTO=-0.8713 VBI=0.65 ALPHA=4.875 BETA=10.92E-5
+ LAMBDA=0.1173 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15 RS=28.0 VJ=0.65
.END
VOLTAGE REFEREANCE 80C

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 80.000 DEG C

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1)</td>
<td>-1.4871</td>
<td>(2)</td>
<td>-1.4875</td>
<td>(4)</td>
<td>-1.9202</td>
<td>(6)</td>
<td>-4.5425</td>
</tr>
<tr>
<td>(7)</td>
<td>-4.0647</td>
<td>(8)</td>
<td>-5.0000</td>
<td>(9)</td>
<td>-4.5425</td>
<td>(15)</td>
<td>-1.2666</td>
</tr>
<tr>
<td>(16)</td>
<td>-2.5332</td>
<td>(17)</td>
<td>-3.7998</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VOLTAGE SOURCE CURRENTS

<table>
<thead>
<tr>
<th>NAME</th>
<th>CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>5.202D-03</td>
</tr>
</tbody>
</table>

TOTAL POWER DISSIPATION 2.60D-02 WATTS
VOLTAGE REFERENCE 90C

**** CIRCUIT DESCRIPTION

*******************************************************************************

* ALL THE SUPPLY VOLTAGES.
* VSS 8 0 DC -5.0V
* VB1 5 0 DC -3.60V
* CIRCUIT
* ACTIVE DEVICES
* BENH1 1 17 7 EMES90 250.0
BDEF1 4 6 7 DMES90 125.0
BBD1 0 1 1 DMES90 31.0
BBD2 0 2 2 DMES90 31.0
BBIAS2 7 8 8 DMES90 65.0
* LEVEL SHIFT DIODE
D1 2 4 DIMOD 300
* IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
* BIAS CIRCUIT *
BB1 0 15 15 DMES90 8
BB2 15 16 16 DMES90 8
BB3 16 17 17 DMES90 8
BB4 17 8 8 DMES90 8
*VON 18 0 DC -4.52
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 90
.OP
.NODESET V(1)=-1.69V V(2)=-1.69V V(4)=-2.10 V(6)=-4.37V V(7)=-3.90V
+ V(9)=-4.37V V(15)=-1.20V V(16)=-2.44V V(17)=-3.67V
.MODEL EMES90 GASFET VTO=-0.08816 VBI=0.65 ALPHA=3.465 BETA=4.01E-5
+ LAMBDA=0.4523 RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES90 GASFET VTO=-0.8796 VBI=0.65 ALPHA=4.875 BETA=10.62E-5
+ LAMBDA=0.1080 RS=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD DI=8E-15 RS=28.0 VJ=0.65
.END
VOLTAGE REFERENCE 90°C

**** SMALL SIGNAL BIAS SOLUTION  TEMPERATURE =  90.000 DEG C

******************************************************************************

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 1)</td>
<td>-1.4768</td>
<td>( 2)</td>
<td>-1.4772</td>
<td>( 4)</td>
<td>-1.8876</td>
<td>( 6)</td>
<td>-4.5821</td>
</tr>
<tr>
<td>( 7)</td>
<td>-4.1001</td>
<td>( 8)</td>
<td>-5.0000</td>
<td>( 9)</td>
<td>-4.5821</td>
<td>(15)</td>
<td>-1.2002</td>
</tr>
<tr>
<td>(16)</td>
<td>-2.5604</td>
<td>(17)</td>
<td>-3.8406</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VOLTAGE SOURCE CURRENTS

NAME  CURRENT

VSS    5.132D-03

TOTAL POWER DISSIPATION  2.57D-02 WATTS
VOLTAGE REFERENCE 100C

**** CIRCUIT DESCRIPTION

******************************************************************************

* ALL THE SUPPLY VOLTAGES.
* VSS 8 0 DC -5.0V
* VB1 5 0 DC -3.60V
*
* CIRCUIT
* ACTIVE DEVICES
*
BENH1 1 17 7 EMES100 250.0
BD1P1 4 6 7 DMES100 125.0
BDL1 0 1 1 DMES100 31.0
BDL2 0 2 2 DMES100 31.0
BBIAS2 7 8 8 DMES100 65.0
*
* LEVEL SHIFT DIODE
D1 2 4 DIMOD 300
*
* IDEAL OPAMP
RINF 2 1 1.0E15
EOUT 9 0 2 1 1E4
RBK 9 6 10
*
* BIAS CIRCUIT *
BB1 0 15 15 DMES100 8
BB2 15 16 16 DMES100 8
BB3 16 17 17 DMES100 8
BB4 17 8 8 DMES100 8
*VON 18 0 DC -4.52
*
* CONTROL CARDS
.WIDTH OUT=80
.TEMP 100
.OP
.OPTIONS TNOM=30
.NODESET V(1)=-1.75V V(2)=-1.75V V(4)=-2.15V V(6)=-4.30V V(7)=-3.85V
+ V(9)=-4.33V V(15)=-1.18V V(16)=-2.38V V(17)=-3.58V

.MODEL EMES100 GASFET VTO=-0.08909 VBI=0.65 ALPHA=3.465 BETA=3.90E-5
+ LAMBDA=0.4515 RG=1289 RD=6705 RS=1734 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DMES100 GASFET VTO=-0.8804 VBI=0.65 ALPHA=4.875 BETA=10.33E-5
+ LAMBDA=0.1070 RG=423 RD=1469 RS=1359 CGD=0.0 CGS=0.0 CDS=0.0
+ TAU=0.0 KF=0.0 AF=1
.MODEL DIMOD D IS=8E-15 RS=28.0 VJ=0.65
.END
**VOLTAGE REFERENCE 100C**

**** SMALL SIGNAL BIAS SOLUTION  

**TEMPERATURE = 100.000 DEG C**

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 1)</td>
<td>-1.3765</td>
<td>( 2)</td>
<td>-1.3770</td>
<td>( 4)</td>
<td>-1.7646</td>
<td>( 6)</td>
<td>-4.6534</td>
</tr>
<tr>
<td>( 7)</td>
<td>-4.1670</td>
<td>( 8)</td>
<td>-5.0000</td>
<td>( 9)</td>
<td>-4.6534</td>
<td>(15)</td>
<td>-1.3032</td>
</tr>
<tr>
<td>(16)</td>
<td>-2.6063</td>
<td>(17)</td>
<td>-3.9095</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VOLTAGE SOURCE CURRENTS**

NAME       CURRENT

VSS        4.993D-03

**TOTAL POWER DISSIPATION** 2.50D-02 WATTS