BSIM4.0.0 TECHNICAL NOTES

by

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Introduction

BSIM4.0.0 model is developed to explicitly address many issues in modeling sub-0.13 micron CMOS technology and RF high-speed CMOS circuit simulation. The plans and progress of the development were presented and discussed at several Compact Model Council (CMC) meetings in 1998 and 1999 period. Many inputs and several requests from those meetings were incorporated into the model. BSIM4 beta version was tested by CMC member companies and their feedback was incorporated into BSIM4.0.0.

BSIM4.0.0 has the following major improvements and additions over BSIM3v3:

- an accurate new model of the intrinsic input resistance (Rii) for both RF, high-frequency analog and high-speed digital applications;
- flexible substrate resistance network for RF modeling;
- a new accurate channel thermal noise model and a noise partition model for the induced gate noise;
- a non-quasi-static (NQS) model that is consistent with the Rii-based RF model and a consistent AC model that accounts for the NQS effect in both transconductances and capacitances;
- an accurate gate direct tunneling model;
- a comprehensive and versatile geometry-dependent parasitics model for various source/drain connections and multi-finger devices;
- improved model for steep vertical retrograde doping profiles;
- better model for pocket-implanted devices in Vth, bulk charge effect model, and Rout;
- asymmetrical and bias-dependent source/drain resistance, either internal or external to the intrinsic MOSFET at the user's discretion;
- acceptance of either the electrical or physical gate oxide thickness as the model input at the user's choice in a physically accurate manner;
- the quantum mechanical charge-layer-thickness model for both IV and CV;
- a more accurate mobility model for predictive modeling;
- a gate-induced drain leakage (GIDL) current model, available in BSIM for the first time;
- an improved unified flicker (1/f) noise model, which is smooth over all bias regions and considers the bulk charge effect;
- different diode IV and CV characteristics for source and drain junctions;
Threshold Voltage Model

- **General description**

In addition to all the features of the BSIM3v3 model [1], the BSIM4 $V_{th}$ model can more accurately model devices with non-uniform doping profile in both vertical and lateral directions. It also removes a phantom second $V_{th}$ roll-up when $L<L_{min}$ in BSIM3v3. A new long channel DIBL model [2] for pocket devices is also implemented.

- **Vertical non-uniform doping effects**

When the channel doping is not uniform in the vertical direction, there is no single "$N_{ch}$" available. To clarify its meaning, we define it to be the doping concentration at the depletion edge when $V_{bs}=0$. We also rename the "$N_{ch}$" in the IV formulation as $N_{dep}$.

It can be shown [3] that, if we define the zero-th and 1st moment of the vertical doping profile as

\[ D_0 = \int_0^{X_{dep}} (N(x) - N_{dep}) \, dx \]
\[ D_1 = \int_0^{X_{dep}} (N(x) - N_{dep}) \, x \, dx \]

where $X_{dep}$ is the depletion depth and $N(x)$ is the vertical doping profile, then the threshold voltage is

\[ V_{th} = V_{th,N_{dep}} + \frac{qD_0}{C_{ox}} + K_{1,N_{dep}} \left( \sqrt{\phi_s - V_{bs}} - \frac{qD_1}{\varepsilon_{Si}} - \sqrt{\phi_s - V_{bs}} \right) \]

where $V_{th,N_{dep}}$, $K_{1,N_{dep}}$ and $\phi_s = 0.4 + kT \ln \left( N_{dep} / N_i \right) / q$ can be calculated from conventional models. Since the doping profile is unknown, we split $D_0$ and $D_1$ into two parts

\[ D_0 = D_{00} + D_{01} = \int_0^{X_{dep0}} (N(x) - N_{dep}) \, dx + \int_{X_{dep0}}^{X_{dep}} (N(x) - N_{dep}) \, dx \]
\[ D_1 = D_{10} + D_{11} = \int_0^{X_{dep0}} (N(x) - N_{dep}) \, x \, dx + \int_{X_{dep0}}^{X_{dep}} (N(x) - N_{dep}) \, x \, dx \]

where $X_{dep0}$ is the depletion depth when $V_{bs}=0$. $D_{00}$ and $D_{10}$ are constants and $D_{00}$ can be merged into $V_{th0}$ in the model. Assuming there is a steep retrograde well below $X_{dep0}$, it can be shown that $D_{01}$ dominates $D_{11}$ and $D_{01} = C_{01} V_{bs}$. $C_{01}$ depends on the steepness and the depth of the retrograde well. Thus the model for vertical non-uniform doping effect is

\[ V_{th} = V_{th0} + K_1 \left( \phi_s - V_{bs} - \sqrt{\phi_s} \right) - K_2 V_{bs} \]

where $\phi_s = \phi_s + \phi_n$, $\phi_s = 0.4 + kT \ln \left( N_{dep} / N_i \right) / q$, $\phi_n = -qD_{10} / \varepsilon_{Si}$ and $K_2 = qC_{01} / C_{ox}$.

- **Lateral non-uniform doping effects**

Reference [2] shows that for long channel devices with pocket implantation, there can be significant drain-induced threshold voltage shift. It can be modeled as
• junction diode breakdown with or without current limiting; and

• dielectric constant of the gate dielectric as a model parameter.

We have been helped by the input from many users, especially the CMC member companies and their representatives. We would particularly like to thank the CMC members for proposing the geometry-dependent parasitics model, which was drafted by Josef Watts and further enhanced by Jon Sanders.

BSIM4.0.0 beta received intensive evaluation by the TI Mixed Signal Products group. Their testing materially and substantially improved the quality of the present production release. We would particularly like to thank Keith Green, Karthik Vasanth, William Liu, Britt Brooks, Doug Weiser, Brian Mounce, Jon Krick, Jim Hellums, Vinod Gupta, and Tom Vrotsos for their invaluable test effort. We would also like to thank Wenliang Zhang and Bob Daniels of Avant!, and John O'Donovan and Kristin Beggs of Cadence for bug reports.

We appreciate these companies providing us with device data during the BSIM4 development: TI, Hitachi, AMD, IBM, and Conexant.

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The BSIM4 model was developed by Professor Chenming Hu, Research Engineer Weidong Liu, and graduate students Xiaodong Jin, Kanyu M. Cao and Jeff Ou.

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BSIM4 Web Site:
http://www-device.eecs.berkeley.edu/~bsim3-bsim4.html
\[ \Delta V_{th} = -n \cdot V_t \cdot \ln \left( \frac{1 - e^{-V_t V_d}}{L_{eff} + dV_{p} 0 \cdot \left( 1 + e^{-dV_{p} V_d} \right)} \right) \]

For \( V_{th} \) of interest, this equation can be simplified as

\[ \Delta V_{th} = -n \cdot V_t \cdot \ln \left( \frac{L_{eff}}{L_{eff} + dV_{p} 0 \cdot \left( 1 + e^{-dV_{p} V_d} \right)} \right) \]

For short channel devices, the lateral non-uniform doping profile changes the body bias effect and makes \( V_{th} \) roll-up as well. This is modeled by

\[ \Delta V_{th} = \sqrt{1 + \frac{L_{peb}}{L_{eff}} \cdot \left( K_{lox} \cdot \sqrt{\phi_s - V_{heff}} - K_3 \cdot \sqrt{\phi_s} \right) + K_{lox} \cdot \left( \sqrt{1 + \frac{L_{peb}}{L_{eff}}} - 1 \right) \cdot \sqrt{\phi_s}} \]

- **Improved formulation for Short-Channel Effects (SCE)**
  The SCE term used in BSIM3v3 is in the form of \( e^{-L/2I} + 2e^{-L/I} \) , which is a finite value at \( L=0 \) while the \( V_{th} \) roll-up term \( \sqrt{1 + N_{lx}/L - 1} \) goes to infinity. So for devices with \( L<L_{min} \), modeled \( V_{th} \) may have a second roll-up. To eliminate this phantom behavior, we eliminated the approximation used to derive the term \( e^{-L/2I} + 2e^{-L/I} \) and model SCE with the more accurate form

\[ \frac{0.5}{\cosh \left( \frac{L_{peb}}{L_{eff}} \right) - 1} \]

When \( L \) is small, the function \( \approx 1/L^2 \) increases faster than \( \sqrt{1 + N_{lx}/L - 1} \). We also expect it to be more accurate even at \( L > L_{min} \).

- **Model parameters for \( V_{th} \)**

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>( VTH0 )</td>
<td>Long-channel threshold Voltage at ( V_{bs}=0 )</td>
<td>0.7V(nmos) -0.7V(pmos)</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>( VFB )</td>
<td>Flat-band Voltage</td>
<td>-1.0V</td>
<td>Yes</td>
<td>If not given, calculated from ( VTH0 )</td>
</tr>
<tr>
<td>( PHIN )</td>
<td>Non-uniform vertical doping effect</td>
<td>0.0V</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>( K1 )</td>
<td>First body bias coefficient</td>
<td>0.5V</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>( K2 )</td>
<td>Second body bias coefficient</td>
<td>0.0</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>( K3 )</td>
<td>Narrow width coefficient</td>
<td>80.0</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>( K3B )</td>
<td>Body effect coefficient of ( K3 )</td>
<td>0.01V</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>( W0 )</td>
<td>Narrow width parameter</td>
<td>2.5e-6m</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>( LPE0 )</td>
<td>Non-uniform lateral doping parameter at ( V_{bs}=0 )</td>
<td>1.74e-7m</td>
<td>Yes</td>
<td></td>
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<tr>
<td>( LPEB )</td>
<td>Non-uniform lateral doping effect on ( K1 )</td>
<td>0.0m</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>( VBM )</td>
<td>Maximum applied body bias in ( V_{th} ) calculation</td>
<td>-3.0V</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>( DVT0 )</td>
<td>First coefficient of short channel effect on ( V_{th} )</td>
<td>1.0*</td>
<td>Yes</td>
<td></td>
</tr>
</tbody>
</table>
BSIM4.0.0 Technical Notes – Basic IV Model

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Value</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>$DVT1$</td>
<td>Second coefficient of short channel effect on $V_{th}$</td>
<td>1.0*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$DVT2$</td>
<td>Body-bias coefficient of short channel effect on $V_{th}$</td>
<td>-0.0321/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$DVTOW$</td>
<td>First coefficient of narrow width effect on $V_{th}$ for small channel length</td>
<td>0.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$DVTIW$</td>
<td>Second coefficient of narrow width effect on $V_{th}$ for small channel length</td>
<td>5.3e6m'/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$DVT2W$</td>
<td>Body-bias coefficient of narrow width effect on $V_{th}$ for small channel length</td>
<td>-0.032V'/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$DVTP0$</td>
<td>First coefficient of pocket implant effect on $V_{th}$ for long channel length</td>
<td>0.0m</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$DVTP1$</td>
<td>Second coefficient of pocket implant effect on $V_{th}$ for long channel length</td>
<td>0.0V'/V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Guidelines for parameter extraction**

  The parameter extraction procedure is the same as BSIM3v3 except $DVTP0$ and $DVTP1$. There are two ways to extract these two parameters.

  1. Measure $V_{th}$ vs. $V_{ds}$ at $V_{bs}$=0 for long and wide channel devices using the constant current method. Fit the $V_{th}$ model to this curve and extract $VTH0$, $DVTP0$ and $DVTP1$. In the constant current method $V_{th}$ can be defined as $V_{gs}$ at which $I_{ds}$=$I_{crit}W/L$, where $I_{crit}$ can be 1e-7A for NMOS and 5e-8A for PMOS.

  2. Extract $VTH0$, $DVTP0$ and $DVTP1$ directly by fitting $V_{th}$ vs. $L$ at $V_{ds}$=0 and $V_{ds}$=$V_{dd}$ using long devices (eg: devices with $L$>1um).

- **Improved $V_{gsteff}$**

  - **General description**

    In BSim3V3, there is no parameter dedicated to the moderate inversion region. To improve the model accuracy in this region, two parameters, $VOFFL$ and $MINV$, are introduced.

  - **$VOFFL$ parameter**

    For non-uniform channel doping profiles, $VOFF$ parameter varies with $L$. We propose the following length dependence

    $$V_{eff}^{\cdot} = V_{eff} + \frac{V_{off}}{L_{eff}}.$$

  - **$MINV$ parameter**
MINV is incorporated to improve the accuracy of \( g_m \), \( g_m^2/\!\!I_d \), and \( g_m^2/I_d \) in the moderate inversion region. The expressions are:

\[
m^* = 0.5 + \frac{\arctan(\text{minv})}{\pi}
\]

\[
V_{\text{sgst}} = \frac{n \cdot v_i \cdot \ln \left[ 1 + e^{\frac{m^* V_{\text{gs}}}{n}} \right]}{m^* + n \cdot \text{Cox} \sqrt{\frac{2 \Phi_s}{q e_N N_{ch}}} e^{\frac{-V_{\text{eff}} - V_d}{n}}}
\]

An \arctan function is used to limit \( m^* \) between 0 and 1 to improve parameter optimization process.

**Parameters for \( V_{\text{gstoff}} \)**

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOFF</td>
<td>Offset voltage in moderate inversion region for large ( W ) and ( L )</td>
<td>-0.08V</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>VOFFL</td>
<td>Coefficient for gate length dependence of VOFF</td>
<td>0.0m-V</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td>MINV</td>
<td>Coefficient of moderate inversion</td>
<td>0.0</td>
<td>Yes</td>
<td>-</td>
</tr>
</tbody>
</table>

**Guideline for parameter extraction**

In general, the threshold voltage extracted by “linear extrapolation” (peak \( gm \)) method based on the strong inversion IV equations may be considered the threshold voltage for moderate-to-strong inversion. \( V_{th} \) extracted by “constant current” method that extracts \( V_{\text{th}} \) from sub-threshold IV can be considered the threshold voltage for weak-to-moderate inversion. The difference of these two voltages is \( VOFF \). \( VOFFL \) can be extracted from the gate length dependence of the difference. We suggest \( VOFF \), \( VOFFL \), and \( MINV \) to minimize the fitting errors of the target curves such as \( g_m/I_d \) and \( g_m^2/I_d \).

**Improved Bulk Charge Model**

Bulk charge effect has a strong dependence on the channel doping profile. The equation for \( A_{\text{bulk}} \) is:

\[
F_{\text{doping}} = \sqrt{1 + \frac{L_{\text{eff}}}{2} \frac{K_{\lambda x} L_{\text{eff}}}{K_{\lambda x} - K_3} \frac{T_{\text{eff}}}{W_{\text{eff}} + W_0} \phi_s}
\]

\[
A_{\text{bulk}} = \left( 1 + F_{\text{doping}} \left( \frac{A_{\text{L}} L_{\text{eff}}}{L_{\text{eff}} + 2 \sqrt{X_j X_{\text{dep}}} \left( 1 - A_{\text{V}} V_{\text{sgst}} \left( \frac{L_{\text{eff}}}{L_{\text{eff}} + 2 \sqrt{X_j X_{\text{dep}}}} \right) ^2 \right) \right) + \frac{B_0}{W_{\text{eff}} + B_1} \right) ^{1 + \text{Keta} V_{\text{th}}}
\]
BSIM4 provides three different mobility models. The mobMod=0 and 1 models are from BSIM3v3.2.2; the new mobMod=2, a universal mobility model, is more accurate and suitable for predictive modeling.

- **Parameter set for the mobility models**

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable?</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>(U_0)</td>
<td>Low-field mobility</td>
<td>NMOS: 0.067(m^2/Vs); PMOS: 0.025(m^2/Vs)</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>(U_A)</td>
<td>Coefficient of first-order mobility degradation due to vertical field</td>
<td>1.0e-9(m^2/V) for (\text{mobMod}=0) and (1); 1.0e-15(m^2/V) for (\text{mobMod}=2)</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>(U_B)</td>
<td>Coefficient of second-order mobility degradation due to vertical field</td>
<td>1.0e-19(m^2/V^4)</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>(U_C)</td>
<td>Coefficient of mobility degradation due to body-bias effect</td>
<td>-0.0465(V^{-1}) for (\text{mobMod}=1); -0.0465e-9(mA/V^2) for (\text{mobMod}=0) and (2)</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>(E_U)</td>
<td>Exponent for mobility degradation of (\text{mobMod}=2)</td>
<td>NMOS: 1.67; PMOS: 1.0</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
</tbody>
</table>

Note-1: if \(E_U\) is negative, \(E_U\) is set to zero.

- **Model equations**

MobMod=0:

\[
\mu_{\text{eff}} = \frac{\mu_0}{1 + (U_A + U_C V_{\text{eff}}) \left(\frac{V_{s\text{eff}} + 2V_s}{T_{ax}}\right) + U_B \left(\frac{V_{s\text{eff}} + 2V_s}{T_{ax}}\right)^2}
\]

MobMod=1:

\[
\mu_{\text{eff}} = \frac{\mu_0}{1 + U_A \left(\frac{V_{s\text{eff}} + 2V_s}{T_{ax}}\right) + U_B \left(\frac{V_{s\text{eff}} + 2V_s}{T_{ax}}\right)^2 \left(1 + U_C V_{\text{eff}}\right)}
\]

MobMod=2:

\[
\mu_{\text{eff}} = \frac{\mu_0}{1 + \left(U_A + U_C V_{\text{eff}}\right) \left[\frac{V_{s\text{eff}} + C_0 \cdot (V_{th0} - V_{fb} - \varphi_s)}{T_{ax}}\right]^{E_U}}
\]

where the constant \(C_0 = 2\) for NMOS and 2.5 for PMOS.
Output Resistance Model

- **General description**

The output resistance model of BSIM4 has significant improvements over that of BSIM3v3 especially for long-channel devices and pocket-implanted devices. The channel length modulation (CLM) model has been improved over L. Four new parameters $F_{\text{POUT}}$, $P_{\text{DITS}}$, $P_{\text{DITSL}}$, and $P_{\text{DITSD}}$ to model the output resistance of long-channel devices and pocket-implanted devices. For non-pocket devices, use of these parameters are also encouraged because these devices may have non-uniform lateral doping profile due to defect-enhanced diffusion even without pocket implant.

- **Degradation factor**

It can be shown [2] that a long channel device with a drain pocket-implant has lower output resistance than that without it. The degradation ratio can be modeled as

$$F = \frac{1}{1 + f_{\text{pro}} \cdot \frac{\sqrt{L}}{V_{\text{sat}} + 2V_i}}$$

- **Channel-Length-Modulation model**

It has been shown [4] that the CLM model of BSIM3v3 does not scale accurately with L correctly because $V_{ACL\text{M}}$ is assumed to be constant with respect to $V_d$ when deriving $I_d$. We correct this by removing this approximation and derive the $I_d$ formula from integration. Let

$$C_{\text{clm}} = \frac{1}{P_{\text{clm}}} \cdot F \left( 1 + P_{\text{vag}} \frac{V_{\text{gseff}}}{E_{\text{sat}}L_{\text{eff}}} \right) \left( 1 + \frac{R_{ds } \cdot I_{\text{dso}}}{V_{\text{dseff}}} \right) \left( L + \frac{V_{\text{deat}}}{E_{\text{sat}}} \right) \frac{1}{l_{\text{itl}}}$$

$$V_{\text{ACL\text{M}}} = C_{\text{clm}} \cdot (V_d - V_{\text{dseff}})$$

$$V_A = V_{\text{asat}} + V_{\text{ACL\text{M}}}$$

Then omitting other effects gives

$$I_d = I_{\text{dso}} \left( 1 + \int_{V_{\text{dso}}}^{V_A} \frac{1}{V_d} dV_d \right) = I_{\text{dso}} \left( 1 + \frac{1}{C_{\text{clm}}} \ln \left( \frac{V_A}{V_{\text{asat}}} \right) \right)$$

- **Effect of drain induced threshold voltage shift on the output resistance**

Pocket implants introduce a potential barrier at the drain end of the channel. This barrier can be lowered by the drain voltage even in long-channel devices. The output resistance of this effect can be modeled as [2]

$$V_{\text{ADITS}} = \frac{1}{P_{\text{dits}}} \cdot F \cdot \left[ 1 + (1 + P_{\text{dits}} L_{\text{eff}}) e^{P_{\text{dits}} V_d} \right]$$
• **Change in \( V_{ADIBL} \)**

\( V_{ADIBL} \) is separated from \( V_{ACLIM} \), and changed to

\[
V_{ADIBL} = V_{ADIBL,BSIM3} \left( 1 + P_{VAG} \frac{V_{gsteff}}{E_{sat}L_{eff}} \right)
\]

Note that the degradation factor, \( F \), is not applied to \( V_{ADIBL} \). The reason is that \( F \) is derived for long-channel device while DIBL is a short channel effect.

• **Drain current equation**

\( I_{ds} \) is formulated as

\[
I_{ds} = I_{ds0} \cdot \frac{N_f}{1 + \frac{R_{sdeff}}{V_{ds}}} \left[ 1 + \frac{1}{C_{clm} \left( \frac{V_A}{V_{Wasf}} \right)} \left( 1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}} \right) \left( 1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}} \right) \left( 1 + \frac{V_{ds} - V_{dseff}}{V_{ADITS}} \right) \right]
\]

where \( I_{ds0}, V_{Wasf}, V_{ASCBE}, \) and other terms have the same definitions as in BSIM3v3. \( N_f \) is the number of device fingers.

• **Parameters for the Rout model**

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCLM</td>
<td>Channel length modulation parameter</td>
<td>1.0</td>
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<tr>
<td>PDIBLC1</td>
<td>First output resistance DIBL effect correction parameter</td>
<td>0.39</td>
<td>Yes</td>
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<td>PDIBLC2</td>
<td>Second output resistance DIBL effect correction parameter</td>
<td>0.0001</td>
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<td>PDIBLCB</td>
<td>Body effect coefficient of DIBL correction parameter</td>
<td>0.0V^{-1}</td>
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<tr>
<td>DROUT</td>
<td>L dependence coefficient of the DIBL correction parameter in Rout</td>
<td>1.0</td>
<td>Yes</td>
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<td>PSCBE1</td>
<td>First substrate current body-effect parameter</td>
<td>4.24e8V/m</td>
<td>Yes</td>
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<tr>
<td>PSCBE2</td>
<td>Second substrate current body-effect parameter</td>
<td>1.0e-5m/V</td>
<td>Yes</td>
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<tr>
<td>PVAG</td>
<td>Gate dependence of early voltage</td>
<td>0.0</td>
<td>Yes</td>
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<tr>
<td>DELTA</td>
<td>Effective ( V_{ds} ) parameter</td>
<td>0.01V</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>FPROUTE</td>
<td>Pocket degradation parameter in Rout</td>
<td>0.0V/m^{0.5}</td>
<td>Yes</td>
<td>Typical (-500)</td>
</tr>
<tr>
<td>PDITS</td>
<td>Magnitude of DITS on Rout</td>
<td>0.0V^{-1}</td>
<td>Yes</td>
<td>Typical (-0.5)</td>
</tr>
<tr>
<td>PDITSL</td>
<td>L dependence of DITS on Rout</td>
<td>0.0m^{-1}</td>
<td>No</td>
<td>Typical (-1e6)</td>
</tr>
<tr>
<td>PDITSD</td>
<td>( V_{ds} ) dependence of DITS on Rout</td>
<td>0.0V^{-1}</td>
<td>Yes</td>
<td>Typical (-0.3)</td>
</tr>
</tbody>
</table>

• **Guidelines for parameter extraction**

7
Parameters for long channel device fitting: \textit{FPOUT, PDITS, PDITSL,} and \textit{PDITSD}.
Parameters for short channel device fitting: Other parameters.

References

Asymmetric and Bias-Dependent $R_{ds}$ Model

- General
Accurate modeling of the bias-dependent LDD source/drain resistance $R_{ds}(V)$ is very important for deep-submicron CMOS technologies. In BSIM3, $R_{ds}(V)$ is modeled internally through the $I_{ds}$ equation and $R_{ds}(V)=R_{ds}(V)$ is assumed. BSIM4 keeps this option for the sake of simulation efficiency. In addition, BSIM4 allows $R_{ds}(V)$ to be external and asymmetrical (i.e. like the source/drain diffusion resistance, the LDD resistances $R_{ds}(V)$ and $R_{s}(V)$ are connected between the external and internal source (drain) nodes. This feature makes accurate RF CMOS simulation possible. The internal $R_{ds}(V)$ option can be invoked by setting the model selector $rdsMod = 0$ (internal) and the external one by setting $rdsMod =1$ (external).

- Model parameters

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$rdsMod$</td>
<td>Bias-dependent S/D resistance model selector</td>
<td>0</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td>$RDSW$</td>
<td>Zero bias LDD resistance per unit width for $rdsMod=0$</td>
<td>200.0ohm-($\mu$m)$^{WR}$</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
<tr>
<td>$RDSWMIN$</td>
<td>LDD resistance per unit width at high $Vgs$ and zero $Vbs$ for $rdsMod=0$</td>
<td>0.0ohm-($\mu$m)$^{WR}$</td>
<td>No</td>
<td>Note-1</td>
</tr>
<tr>
<td>$RDW$</td>
<td>Zero bias lightly-doped drain resistance $R_{d}(V)$ per unit width for $rdsMod=1$</td>
<td>100.0ohm-($\mu$m)$^{WR}$</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
<tr>
<td>$RDWMIN$</td>
<td>Lightly-doped drain resistance per unit width at high $Vgs$ and zero $Vbs$ for $rdsMod=1$</td>
<td>0.0ohm-($\mu$m)$^{WR}$</td>
<td>No</td>
<td>Note-1</td>
</tr>
<tr>
<td>$RSW$</td>
<td>Zero bias lightly-doped source resistance $R_{s}(V)$ per unit width for $rdsMod=1$</td>
<td>100.0ohm-($\mu$m)$^{WR}$</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
<tr>
<td>$RSWMIN$</td>
<td>Lightly-doped source resistance per unit width at high $Vgs$ and zero $Vbs$ for $rdsMod=1$</td>
<td>0.0ohm-($\mu$m)$^{WR}$</td>
<td>No</td>
<td>Note-1</td>
</tr>
<tr>
<td>$PRWG$</td>
<td>Gate bias dependence of LDD resistance</td>
<td>1.0$V^{-1}$</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
<tr>
<td>$PRWB$</td>
<td>Body bias dependence of LDD resistance</td>
<td>0.0$V^{-0.5}$</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>$WR$</td>
<td>Width dependence parameter of LDD resistance</td>
<td>1.0</td>
<td>Yes</td>
<td>-</td>
</tr>
</tbody>
</table>

Note-1: if negative, a warning message will be issued and the parameter is set to 0.0.
Model equations

\( rdsMod=0 \) (internal \( R_{ds}(V) \)):

\[
R_{ds}(V) = \frac{RDSW_{MIN} + RDSW \cdot \left( PRWB \cdot \left( \sqrt{\Phi_g - V_{sd} - \Phi_s} + \frac{1}{1 + PRWG \cdot V_{sd}} \right) \right)}{\left( 1e6 \cdot Weff CJ \right)^{WR}}.
\]

\( rdsMod=1 \) (External \( R_d(V) \) and \( R_s(V) \)):

\( R_d(V) \) is expressed as

\[
R_d(V) = \frac{RDSW_{MIN} + RDW \cdot \left( -PRWB \cdot V_{sd} + \frac{1}{1 + PRWG \cdot (V_g - V_{fbd})} \right)}{\left( 1e6 \cdot Weff CJ \right)^{WR} \cdot N_f}.
\]

\( R_s(V) \) is expressed as

\[
R_s(V) = \frac{RDSW_{MIN} + RSW \cdot \left( -PRWB \cdot V_{sd} + \frac{1}{1 + PRWG \cdot (V_g - V_{fbd})} \right)}{\left( 1e6 \cdot Weff CJ \right)^{WR} \cdot N_f}.
\]

In the above equations, \( Weff CJ \) is the effective width of the source/drain diffusion regions, \( NF \) is the number of finger, and \( V_{fbd} \) is the flat-band voltage between the gate and the source/drain. \( V_{fbd} \) is given by

If \( NGATE > 0.0 \),

\[
V_{fbd} = \frac{kT}{q} \log \left( \frac{N_{gate}}{N_{sd}} \right)
\]

Else

\( V_{fbd} = 0.0 \)

where \( NGATE \) and \( NSD \) are the doping concentrations in the poly-silicon gate and the source/drain regions, respectively. \( NSD \) defaults to 1.0e20cm\(^{-3}\) and can be binned.

The following figure shows the schematic for \( rdsMod=1 \).
Modeling Quantum-Mechanical Inversion-Layer Thickness and High-\(k\) Gate Dielectrics

- **General**

As the gate oxide thickness is vigorously scaled down, the finite charge-layer thickness cannot be ignored [1]. BSIM4 models this effect in both IV and CV. For this purpose, BSIM4 accepts the electrical gate oxide thickness \(T_{OXE}\) and/or the physical gate oxide thickness \(T_{OXP}\), or their difference \(D_{TOX} = T_{OXE} - T_{OXP}\), as the model inputs, based on which the effect of effective gate oxide capacitance \(C_{oxef}\) on IV and CV is modeled [2].

High-\(k\) gate dielectric can be modeled as an “equivalent oxide” with thickness adjusted for Si\(_2\)O\(_2\) (3.9). For example, 3nm gate dielectric with a dielectric constant of 7.8 would have an equivalent oxide thickness of 1.5nm.

BSIM4 also allows to specify a gate dielectric constant \((E_{PSROX})\) different from 3.9 (Si\(_2\)O\(_2\)) as an alternative approach to modeling high-\(k\) dielectrics.

- **Model parameters**

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>(E_{PSROX})</td>
<td>Gate dielectric constant relative to vacuum</td>
<td>3.9 (Si(_2)O(_2))</td>
<td>No</td>
<td>(E_{PSROX}) typically should be (\geq 3.9)</td>
</tr>
<tr>
<td>(T_{OXE})</td>
<td>Electrical gate equivalent oxide thickness</td>
<td>3.0e-9m</td>
<td>No</td>
<td>Note-1</td>
</tr>
<tr>
<td>(T_{OXP})</td>
<td>Physical gate equivalent oxide thickness</td>
<td>(T_{OXE})</td>
<td>No</td>
<td>Note-1</td>
</tr>
<tr>
<td>(T_{OMX})</td>
<td>(T_{OXE}) at which the other BSIM4 parameters are extracted</td>
<td>(T_{OXE})</td>
<td>No</td>
<td>Note-1</td>
</tr>
<tr>
<td>(D_{TOX})</td>
<td>Defined as ((T_{OXE} - T_{OXP}))</td>
<td>0.0m</td>
<td>No</td>
<td>-</td>
</tr>
</tbody>
</table>

Note-1: if value \(\leq 0.0\), fatal errors will be issued.

- **References:**


**Algorithm and model equations**

- **TOXE** and **TOXP** both given?
  - Yes
    - **TOXE** = **TOXE**
    - **TOXP** = **TOXP**
  - No
    - **TOXE** given?
      - Yes
        - **TOXE** = **TOXE**
        - **TOXP** = **TOXE** - **DTOX**
      - No
        - **TOXP** given?
          - Yes
            - **TOXE** = **TOXP** + **DTOX**
            - **TOXP** = **TOXP**
          - No
            - Default case

- **TOXE** is used to compute: \( V_{th} \), subthreshold swing, \( V_{gs\text{eff}} \), \( A_{bulk} \), mobility, \( V_{dsat} \), \( K_{1ox} = K_1 \cdot \frac{\text{TOXE}}{\text{TOXM}} \), \( K_{2ox} = K_2 \cdot \frac{\text{TOXE}}{\text{TOXM}} \), capMod=0 and 1, and so on; and

- **TOXP** is used to compute \( C_{\text{surf}} \) for drain current and capMod=2 through \( X_{dc} \)

\[
X_{dc} = \frac{1.9 \times 10^{-9}}{1 + \left( \frac{V_{gs\text{eff}} + 4(V_{TH0} - V_{FB} - \Phi)}{2\text{TOXP}} \right)^{0.7}}
\]
Model of Gate-Induced Drain Leakage (GIDL) Current

- General
The gate-induced-drain leakage (GIDL) current [1-2] and its body bias effect are modeled in BSIM4.

- New model parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$AGIDL$</td>
<td>Pre-exponential coefficient for GIDL</td>
<td>0.0mho</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
<tr>
<td>$BGIDL$</td>
<td>Exponential coefficient for GIDL</td>
<td>$2.3 \times 10^9$ V/m</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
<tr>
<td>$CGIDL$</td>
<td>Parameter for the body bias effect on GIDL</td>
<td>$0.5 V^3$</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>$EGIDL$</td>
<td>Fitting parameter for band bending</td>
<td>0.8 V</td>
<td>Yes</td>
<td>-</td>
</tr>
</tbody>
</table>

Note-1: if the binned value is less than or equal to zero, $I_{gild}$ will be zero.

- GIDL equations

$$I_{gild} = AGIDL \cdot W_{eff/J} \cdot N_f \cdot \frac{V_{ds} - (V_{st,eff} - EGIDL)}{3 \cdot T_{aur}} \cdot \exp \left( \frac{3 \cdot T_{aur} \cdot BGIDL}{V_{ds} - (V_{st,eff} - EGIDL)} \right) \cdot \frac{V_{ds}^3}{CGIDL + V_{ds}^3}$$

where $W_{eff/J}$ is the width of the drain diffusion region.

- References


Gate Direct Tunneling Current Model

- **General description**

As the gate oxide thickness is scaled down to 3 nm and below, gate leakage current due to carrier direct tunneling becomes important. This tunneling happens between the (polysilicon) gate and the silicon beneath the gate oxide. The tunneling carriers can be either electrons or holes, or both, either from the conduction band or valence band, depending on (the type of the polysilicon gate and) the bias regime.

In BSIM4, the gate tunneling current of n^+-poly NMOS and p^+-poly PMOS are modeled. Its components include the tunneling current between gate and substrate/body (Igb), and the current between gate and channel region (Igc), which is partitioned between the source and drain terminals by Igc = Igcs + Igcd. Yet another type of tunneling component is the tunneling current between gate and source/drain diffusion regions (Igs and Igd). As an example, Fig. 1 shows schematically the modeled current flows for an NMOST in the inversion region.

![Diagram](image)

Fig. 1. Schematic gate current components flowing between NMOST terminals in inversion.

- **Model selectors**

Two global selectors are provided to turn on/off the tunneling components. igcmod=1 turns on Igcs, Igs and Igd; igbmod=1 turns on Igb. When both are set to 0, no gate tunneling current components are modeled.

- **Equation for V_{ox}**

The gate tunneling current is a strong function of the voltage drop across the gate oxide (V_{ox}). V_{ox} is derived as

\[ V_{ox} = V_{fzb} - V_{fseff} + k_{ox} \sqrt{\varphi_s} + V_{gseff} \]

where V_{fzb} is calculated from V_{ih} under zero bias conditions, V_{gseff} is the effective (V_{gseff} - V_{ih}) with poly-depletion effects considered by V_{gseff}. V_{fseff} is expressed by

\[ V_{fseff} = V_{fzb} - \frac{1}{2} \left[ (V_{fzb} - V_{gb} - \delta) + \sqrt{(V_{fzb} - V_{gb} - \delta)^2 + 4 V_{fzb} \delta} \right]; \delta = 0.02 \]
\( \sqrt{\phi_s} \) is given by
\[
\sqrt{\phi_s} = \frac{k_{tot}}{2} \left[ 1 + \frac{4}{k_{tot}} \left( V_{gs,eff} - V_{f,eff} - V_{g,eff} - V_{b,eff} \right) \right]
\]

As will be shown later on, it is convenient to transform \( V_{ax} \) into
\[
V_{ax} = V_{ax,acc} + V_{ax,depinv}
\]

where \( V_{ax,acc} = V_{f,acc} - V_{f,eff} \) for the accumulation region and \( V_{ax,depinv} = k_{tot} \sqrt{\phi_s} + V_{g,eff} \) for the depletion and inversion regions. Note that \( V_{ax} \) and its derivatives are continuous over all bias regions.

**Equations for the tunneling currents**

1. **Gate-to-substrate/body current** (\( I_{gb} = I_{gb,acc} + I_{gb,inv} \))
   - \( I_{gb,acc} \) -- determined by ECB (Electron tunneling from Conduction Band):
     \[
     I_{gb,acc} = W_{eff} L_{eff} \cdot A \cdot T_{ox,Ratio} \cdot V_{gb} \cdot V_{aux} \cdot \exp\left[ -B \cdot T_{ox} \left( a_{gb,acc} - b_{gb,acc} \cdot V_{ox,acc} \right) \cdot \left( 1 + c_{gb,acc} \cdot V_{ox,acc} \right) \right]
     \]
     where the physical constant \( A = 4.97232 \times 10^{-7} \) A/V², \( B = 7.45669 \times 10^{-1} \) (g/F·s³) is another physical constant, \( T_{ox,Ratio} = \frac{T_{ox,ref}}{T_{ox}} \cdot \frac{1}{T_{ox}^2} \), and
     \[
     V_{aux} = n_{gb,acc} \cdot V_{m} \cdot \log\left( 1 + \exp\left( -\frac{V_{gb} - V_{f,gb}}{n_{gb,acc} \cdot V_{m}} \right) \right).
     \]
   - \( I_{gb,inv} \) -- determined by EVB (Electron tunneling from Valence Band):
     \[
     I_{gb,inv} = W_{eff} L_{eff} \cdot A \cdot T_{ox,Ratio} \cdot V_{gb} \cdot V_{aux} \cdot \exp\left[ -B \cdot T_{ox} \left( a_{gb,inv} - b_{gb,inv} \cdot V_{ox,inv} \right) \cdot \left( 1 + c_{gb,inv} \cdot V_{ox,inv} \right) \right]
     \]
     where \( A = 3.75956 \times 10^{-7} \) A/V², \( B = 9.82222 \times 10^{-1} \) (g/F·s³) is another physical constant, \( T_{ox,Ratio} = \frac{T_{ox,ref}}{T_{ox}} \cdot \frac{1}{T_{ox}^2} \), and
     \[
     V_{aux} = n_{gb,inv} \cdot V_{m} \cdot \log\left( 1 + \exp\left( -\frac{V_{ox,inv} - e_{gb,inv}}{n_{gb,inv} \cdot V_{m}} \right) \right).
     \]

2. **Gate-to-channel current** (\( I_{gc} \)) and gate-to-S/D current (\( I_{gs} \) and \( I_{gd} \))
   - \( I_{gc} \) -- determined by ECB for NMOS and HVB for PMOS (Hole tunneling from Valence Band), respectively.
BSIM4.0.0 Technical Notes – Gate Tunneling Current Model

\[ I_{gc} = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gs_{eff}} \cdot V_{aux} \cdot \exp[-B \cdot T_{ox} (a_{igc} - b_{igc} \cdot V_{oxdepinv}) \cdot (1+c_{igc} \cdot V_{oxdepinv})] \]

where \( A = 4.97232 \times 10^{-7} \) \( A/V^{2} \) for NMOS and \( 3.42537 \times 10^{-7} \) \( A/V^{2} \) for PMOS, \( B = 7.45669 \times 10^{1} \) \( (g/F-s)^{0.5} \) for NMOS and \( 1.16645 \times 10^{1} \) \( (g/F-s)^{0.5} \) for PMOS, and

\[ V_{aux} = n_{igc} \cdot V_{tm} \cdot \log \left( 1 + \exp \left( \frac{V_{gs_{eff}} - V_{th0}}{n_{igc} \cdot V_{tm}} \right) \right). \]

\( I_{gs} \) and \( I_{gd} \) -- \( I_{gs} \) represents the gate tunneling current between the gate and the source diffusion region, while \( I_{gd} \) represents the gate tunneling current between the gate and the drain diffusion region. \( I_{gs} \) and \( I_{gd} \) are determined by ECB for NMOS and by HVB for PMOS, respectively.

\[ I_{gs} = W_{eff} L_{dcig} \cdot A \cdot T_{oxRatioEdg} \cdot V_{gs} \cdot V_{gs} \cdot \exp[-B \cdot T_{ox} \cdot Poxedge \left( a_{igsd} - b_{igsd} \cdot V_{gs} \right) \cdot (1+c_{igsd} \cdot V_{gs})] \]

and

\[ I_{gd} = W_{eff} L_{dcig} \cdot A \cdot T_{oxRatioEdg} \cdot V_{gd} \cdot V_{gd} \cdot \exp[-B \cdot T_{ox} \cdot Poxedge \left( a_{igsd} - b_{igsd} \cdot V_{gd} \right) \cdot (1+c_{igsd} \cdot V_{gd})] \]

where \( A = 4.97232 \times 10^{-7} \) \( A/V^{2} \) for NMOS and \( 3.42537 \times 10^{-7} \) \( A/V^{2} \) for PMOS, \( B = 7.45669 \times 10^{1} \) \( (g/F-s)^{0.5} \) for NMOS and \( 1.16645 \times 10^{1} \) \( (g/F-s)^{0.5} \) for PMOS,

\[ T_{oxRatioEdg} = \left( \frac{T_{oxref}}{T_{ox \cdot Poxedge}} \right)^{max} \cdot \frac{1}{(T_{ox \cdot Poxedge})^{2}}, \quad V_{gs} = \sqrt{(V_{gs} - V_{fbsd})^2 + 1.0e-4}, \quad V_{gd} = \sqrt{(V_{gd} - V_{fbsd})^2 + 1.0e-4}. \]

• Partition of \( I_{gc} \)

To consider the drain bias effects, \( I_{gc} \) is split into two components, \( I_{gcs} \) and \( I_{gcd} \), that is \( I_{gc} = I_{gcs} + I_{gcd} \).

\[ I_{gcs} = I_{gc} \cdot \frac{pigcd \cdot V_{ds} + \exp(-pigcd \cdot V_{ds}) - 1 + 1.0e-4}{pigcd^2 \cdot V_{ds}^2 + 2.0e-4} \]

and

\[ I_{gcd} = I_{gc} \cdot \frac{1 - (pigcd \cdot V_{ds} + 1) \cdot \exp(-pigcd \cdot V_{ds}) + 1.0e-4}{pigcd^2 \cdot V_{ds}^2 + 2.0e-4}. \]
### Table of parameters for the gate tunneling current model

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable?</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>igcmod</td>
<td>Global model selector for Igs, Igd, Igcs and Igcd current components</td>
<td>0</td>
<td>N/A</td>
<td>igcmod==1 turns on Igs, Igd, Igcs and Igcd.</td>
</tr>
<tr>
<td>igbmod</td>
<td>Global model selector for Ig current</td>
<td>0</td>
<td>N/A</td>
<td>igbmod==1 turns on Ig.</td>
</tr>
<tr>
<td>aigbacc</td>
<td>Parameter for Ig in accumulation</td>
<td>0.43 ( \left( \frac{F_s}{g} \right)^{0.5} ) m(^{-1})</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>bigbacc</td>
<td>Parameter for Ig in accumulation</td>
<td>0.054 ( \left( \frac{F_s}{g} \right)^{0.5} ) (mV)(^{-1})</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>cigbacc</td>
<td>Parameter for Ig in accumulation</td>
<td>0.075 V(^{-1})</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>nigbacc</td>
<td>Parameter for Ig in accumulation</td>
<td>1.0</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
<tr>
<td>aigbinv</td>
<td>Parameter for Ig in inversion</td>
<td>0.35 ( \left( \frac{F_s}{g} \right)^{0.5} ) m(^{-1})</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>bigbinv</td>
<td>Parameter for Ig in inversion</td>
<td>0.03 ( \left( \frac{F_s}{g} \right)^{0.5} ) (mV)(^{-1})</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>cigbinv</td>
<td>Parameter for Ig in inversion</td>
<td>0.006 V(^{-1})</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>eigbinv</td>
<td>Parameter for Ig in inversion</td>
<td>1.1V</td>
<td>Yes</td>
<td>-</td>
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<tr>
<td>nigbinv</td>
<td>Parameter for Ig in inversion</td>
<td>3.0</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
<tr>
<td>aigc</td>
<td>Parameter for Igcs and Igcd</td>
<td>NMOS: 0.43 PMOS: 0.31 ( \left( \frac{F_s}{g} \right)^{0.5} ) m(^{-1})</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>bigc</td>
<td>Parameter for Igcs and Igcd</td>
<td>NMOS: 0.054 PMOS: 0.024 ( \left( \frac{F_s}{g} \right)^{0.5} ) (mV)(^{-1})</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>cigc</td>
<td>Parameter for Igcs and Igcd</td>
<td>NMOS: 0.075 V(^{-1}) PMOS: 0.03 V(^{-1})</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>aigsd</td>
<td>Parameter for Igs and Igd</td>
<td>NMOS: 0.43 PMOS: 0.31 ( \left( \frac{F_s}{g} \right)^{0.5} ) m(^{-1})</td>
<td>Yes</td>
<td>-</td>
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<tr>
<td>bigsd</td>
<td>Parameter for Igs and Igd</td>
<td>NMOS: 0.054 PMOS: 0.024 ( \left( \frac{F_s}{g} \right)^{0.5} ) (mV)(^{-1})</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>cigsd</td>
<td>Parameter for Igs and Igd</td>
<td>NMOS: 0.075 V(^{-1}) PMOS: 0.03 V(^{-1})</td>
<td>Yes</td>
<td>-</td>
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<tr>
<td>Parameter</td>
<td>Description</td>
<td>Value</td>
<td>Default</td>
<td>Note</td>
</tr>
<tr>
<td>-----------</td>
<td>-------------</td>
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<tr>
<td>dlcig</td>
<td>S/D overlap length for Igs/Igd</td>
<td>Lint</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>nigc</td>
<td>Parameter for Igs, Igd, Igcs, and Igcd</td>
<td>1.0</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
<tr>
<td>poxedge</td>
<td>Factor for the gate oxide thickness in the S/D overlap regions</td>
<td>1.0</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
<tr>
<td>pigcd</td>
<td>Vds dependence of Igcs and Igcd</td>
<td>1.0</td>
<td>Yes</td>
<td>Note-1</td>
</tr>
<tr>
<td>ntox</td>
<td>Exponent for the tox ratio</td>
<td>1.0</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>toxref</td>
<td>Nominal gate oxide thickness</td>
<td>30.0A</td>
<td>No</td>
<td>Note-1</td>
</tr>
</tbody>
</table>

Note-1: if the value is less than or equal to zero, fatal errors are issued.
Charge-Voltage (CV) Model

• General

BSIM4 provides three options for selecting intrinsic and overlap/fringing capacitance models. Those three capacitance models come from BSIM3v3.2.2, and the BSIM3v3.2.2 CV model parameters are used without change in BSIM4 except that separate CKAPPA parameters, CKAPPAS (binnable, defaulting to 0.6) and CKAPPAD (binnable, defaulting to CKAPPAS), are introduced for the source-side and drain-side diodes, respectively. The following table maps the BSIM4 capacitance models to those in BSIM3v3.2.2.

• BSIM4 capacitance model options

<table>
<thead>
<tr>
<th>BSIM4 capacitance models</th>
<th>Matched capMod in BSIM3v3.2.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>capMod=0</td>
<td>Intrinsic capMod=0 + Overlap/fringing capMod=0</td>
</tr>
<tr>
<td>capMod=1</td>
<td>Intrinsic capMod=2 + Overlap/fringing capMod=2</td>
</tr>
<tr>
<td>capMod=2 (default model)</td>
<td>Intrinsic capMod=3 + Overlap/fringing capMod=2</td>
</tr>
</tbody>
</table>

The BSIM3v3.2.2 capMod=1 is no longer supported in BSIM4.
Electrode Gate and Intrinsic-Input Resistance Model

- General

BSIM4 provides four options for modeling electrode gate (bias-independent) and bias-dependent gate (intrinsic input) resistances. This model also works with multi-finger devices.

- Model parameters

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
<th>Default</th>
<th>Binnable ?</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{gateMod}$ (instance and global)</td>
<td>Gate-resistance model selector</td>
<td>0 - no gate resistance</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td>$R_{SHG}$</td>
<td>Gate-electrode sheet resistance</td>
<td>0.1 ohm/square</td>
<td>No</td>
<td>Warning message if $R_{SHG} \leq 0.0$</td>
</tr>
<tr>
<td>$X_{GW}$</td>
<td>Distance from the gate contact to the channel edge</td>
<td>0.0m</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td>$X_{GL}$</td>
<td>Difference between $L_{drawn}$ and physical gate length</td>
<td>0.0m</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td>$N_{GCON}$</td>
<td>Number of gate contacts for each finger, 1 or 2</td>
<td>1.0</td>
<td>No</td>
<td>Fatal error if &lt;1.0</td>
</tr>
<tr>
<td>$X_{RCRG1}$</td>
<td>Parameter for distributed channel-resistance effect</td>
<td>12.0</td>
<td>Yes</td>
<td>Warning message if $X_{RCRG1} \leq 0.0$</td>
</tr>
<tr>
<td>$X_{RCRG2}$</td>
<td>Parameter to account for the excess channel diffusion resistance</td>
<td>1.0</td>
<td>Yes</td>
<td>-</td>
</tr>
</tbody>
</table>

- Options and schematic

$r_{gateMod} = 0$ (zero-resistance):
No gate resistance is generated.

$R_{geltd}$

$r_{gateMod} = 1$ (constant-resistance):
Only the electrode gate resistance (bias-independent) is generated by adding an internal gate node.
**BSIM4.0.0 Technical Notes – Electrode Gate and Intrinsic-Input Resistance Model**

**rgateMod = 2 (variable-resistance):**
The gate resistance is the sum of the electrode gate resistance and the intrinsic-input resistance \( R_{ii} \) (bias-dependent) [1]. An internal gate node is introduced.

\[
rgateMod = 2(\text{variable-resistance})
\]

The gate resistance is the sum of the electrode gate resistance and the intrinsic-input resistance \( R_{ii} \) (bias-dependent) [1]. An internal gate node is introduced.

\[
R_{geltd} + R_{ii}
\]

**rgateMod = 3 (two-node):**
The electrode gate resistance is in series with the intrinsic-input resistance through two internal gate nodes, so that the overlap capacitance current will not pass through the intrinsic-input resistance.

\[
rgateMod = 3(\text{two-node})
\]

The electrode gate resistance is in series with the intrinsic-input resistance through two internal gate nodes, so that the overlap capacitance current will not pass through the intrinsic-input resistance.

\[
R_{geltd}
\]

\[
R_{ii} \quad \text{and} \quad C_{gso} \quad \text{and} \quad C_{gdo}
\]

**Equations**

**Electrode gate resistance:**

\[
R_{geltd} = \frac{r_{shg} \cdot \left( x_{gw} + \frac{W_{eff} c_{j}}{3 n_{gcon}} \right)}{n_{gcon} \cdot (L_{drawn} - x_{gl}) \cdot NF}
\]

Please refer to “Modeling Series/Parallel Devices” for the layout parameters in the above equation.

**Intrinsic-input resistance:**

\[
\frac{1}{R_{ii}} = x_{rcrg} \cdot \left( \frac{1}{R_{drif}} + \frac{1}{R_{diff}} \right) = x_{rcrg} \cdot \left( \frac{I_{ds}}{V_{ds}} + x_{rcrg} \cdot \frac{W_{eff} H_{off} C_{aoff}}{q L_{eff}} \right)
\]

**References**

Substrate Resistance Network

• General

For CMOS RF circuit simulation, it is essential to consider the high frequency coupling through the substrate. BSIM4 offers a flexible built-in substrate resistance network. This network is constructed such that little simulation efficiency penalty will result. Note that the substrate resistance parameters listed below should be extracted for the total device, not on a per-finger basis.

• Model selector and parameters

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>rbodyMod (instance and global parameter)</td>
<td>Model selector for distributed substrate resistance network</td>
<td>0 – network is turned off</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td>GBMIN (instance and global parameter)</td>
<td>Minimum conductance in parallel with each of the five substrate resistances</td>
<td>1.0e-12mho</td>
<td>No</td>
<td>Note-1</td>
</tr>
<tr>
<td>RBPB (instance and global parameter)</td>
<td>Resistance connected between bNodePrime and bNode</td>
<td>50.0ohm</td>
<td>No</td>
<td>Note-2</td>
</tr>
<tr>
<td>RBPD (instance and global parameter)</td>
<td>Resistance connected between bNodePrime and dbNode</td>
<td>50.0ohm</td>
<td>No</td>
<td>Note-2</td>
</tr>
<tr>
<td>RBPS (instance and global parameter)</td>
<td>Resistance connected between bNodePrime and sbNode</td>
<td>50.0ohm</td>
<td>No</td>
<td>Note-2</td>
</tr>
<tr>
<td>RBDB (instance and global parameter)</td>
<td>Resistance connected between dbNode and bNode</td>
<td>50.0ohm</td>
<td>No</td>
<td>Note-2</td>
</tr>
<tr>
<td>RBSB (instance and global parameter)</td>
<td>Resistance connected between sbNode and bNode</td>
<td>50.0ohm</td>
<td>No</td>
<td>Note-2</td>
</tr>
</tbody>
</table>

Note-1: if GBMIN < 1.0e-20, warning message will be issued since it is too small. Each substrate resistance listed above is connected in parallel with GBMIN to prevent too large resistance values, which would otherwise cause poor convergence.

Note-2: if value < 1.0e-3, it is set to 1.0e-3ohm.
• Topology

\textit{rbodyMod} = 0 (Off):

No substrate network is generated at all.

\textit{rbodyMod} = 1 (On):

All five resistances in the substrate network as shown schematically below are present simultaneously. \textit{GBMIN} is in parallel with each resistance in the network. To simplify the representation of the model topology, \textit{GBMIN} is merged into each resistance. Note that the intrinsic model substrate reference point is the internal body node \texttt{bNodePrime}, into which the impact ionization current \textit{I_{SUB}} and the GIDL current \textit{I_{GIDL}} flow.

![Diagram showing the substrate resistance network with \texttt{bNodePrime} as the internal body node, connected to \textit{I_{SUB}} and \textit{I_{GIDL}} through the parallel resistances RBPD, RBPB, RBSB, RBDB, and GBMIN.]

Fig. 1 Topology with the substrate resistance network turned on.
Non-Quasi-Static Model

- General

BSIM4 uses two different NQS model selectors to turn on the charge-deficit NQS model in transient simulation (using tmqsMod=1) and AC simulation (using acnqsMod=1). The AC NQS model does not require the internal NQS charge node that is required by the transient NQS model. Both the transient NQS and AC NQS models are developed from the same fundamental physical basis: the channel/gate charge response to the external signal are relaxation-time ($\tau$) dependent and the transcapacitances and transconductances (such as $g_m$) for AC analysis can therefore be expressed as functions of $j\omega\tau$.

- Model parameters

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>tmqsMod (instance and global)</td>
<td>Transient NQS model selector</td>
<td>0 - off</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td>acnqsMod (instance and global)</td>
<td>AC NQS model selector</td>
<td>0 - off</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td>XRCRG1</td>
<td>Parameter for distributed channel-resistance effect</td>
<td>12.0</td>
<td>Yes</td>
<td>Warning message if XRCRG1 &lt;= 0.0</td>
</tr>
<tr>
<td>XRCRG2</td>
<td>Parameter to account for the excess channel diffusion conductance</td>
<td>1.0</td>
<td>Yes</td>
<td>-</td>
</tr>
</tbody>
</table>

Warning: these models should not be turned on when rgateMod is set to 2 or 3.

- Model equation

In time domain, the charging current at time $t$ due to channel charge $Q_{ch}(t)$ is expressed as

$$\frac{\partial Q_{ch}(t)}{\partial t} = \frac{Q_{def}(t)}{\tau} \quad (1)$$

Therefore the charging current at the gate, source, and drain terminals for the transient NQS model is obtained from

$$\frac{\partial Q_{g,s,d}(t)}{\partial t} = XPART_{G,D,S} \frac{Q_{def}(t)}{\tau} \quad (2)$$
where $\text{XPART}_{G,D,s}$ are the charge partition number, and $Q_{\text{def}}(t)$ is the difference between the channel charge density $Q_{\text{ch,qt}}(t)$ under quasi-static approximation and $Q_{\text{ch}}(t)$. Thus,

$$Q_{\text{def}}(t) = Q_{\text{ch,qt}}(t) - Q_{\text{ch}}(t) \quad (3)$$

By substituting (3) into (1), it can be shown that in the frequency domain $Q_{\text{ch}}(t)$ can be written as

$$\Delta Q_{\text{ch}}(t) = \frac{\Delta Q_{\text{ch,qt}}(t)}{1 + j\omega \tau} \quad (4)$$

where the transit time $\tau$ is equal to the product of $R_{ii}$ and $WLC_{\text{ox}}$, where $R_{ii}$ is given by

$$\frac{1}{R_{ii}} = x\text{rcrg1} \cdot \left( \frac{1}{R_{\text{drif}}} + \frac{1}{R_{\text{diff}}} \right) = x\text{rcrg1} \cdot \left( \frac{I_{ds}}{V_{\text{dref}}} + x\text{rcrg2} \cdot \frac{W_{\text{eff}} \mu_{\text{eff}} C_{\text{aref}} kT}{q_{\text{eff}}} \right)$$

Based on (4), it can be proved that the transcapacitances $C_{g_d}$, $C_{s_b}$ and $C_{d_i}$ (i stands for any of the $d$, $g$, $s$, and $b$ terminals of the device) and the channel transconductances $g_m$, $g_{ds}$, and $g_{mb}$ all become complex quantities. For example, $g_m$ and $C_{ds}$ now become

$$g_m = \frac{g_m}{1 + \omega^2 \tau^2} + j \left( \frac{g_m \cdot \omega \tau}{1 + \omega^2 \tau^2} \right)$$

$$C_{ds} = \frac{C_{ds}}{1 + \omega^2 \tau^2} + j \left( \frac{C_{ds} \cdot \omega \tau}{1 + \omega^2 \tau^2} \right)$$

The quantities in the above two equations with sub "0" are known from the OP analysis.
Flicker Noise Model

- **General**
  BSIM4 provides two flicker noise models. When the model selector `fnoiMod` is set to 0, a simple flicker noise model which is convenient for hand calculations is invoked. A unified physical flicker noise model, which is the default model, will be used if `fnoiMod == 1`. These two flicker noise models come from BSIM3v3, but the unified model has many improvements. For instance, it is now smooth over all bias regions and considers the bulk charge effect.

- **Model parameters**

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>fnoiMod</code></td>
<td>Flicker noise model selector</td>
<td>1</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td><code>AF</code></td>
<td>Flicker noise exponent</td>
<td>1.0</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>EF</code></td>
<td>Flicker noise frequency</td>
<td>1.0</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>KF</code></td>
<td>Flicker noise coefficient</td>
<td>0.0 ( \text{A}^{-\text{AF}} \cdot \text{s}^{1-EF} \cdot \text{F} )</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>NOIA</code></td>
<td>Flicker noise parameter A</td>
<td>NMOS: 6.25e41 ( \text{eV}^{1-\text{EF}} \cdot \text{s}^{1-\text{EF}} \cdot \text{m}^{-3} )</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PMOS: 6.188e40 ( \text{eV}^{1-\text{EF}} \cdot \text{s}^{1-\text{EF}} \cdot \text{m}^{-3} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>NOIB</code></td>
<td>Flicker noise parameter B</td>
<td>NMOS: 3.125e26 ( \text{eV}^{1-\text{EF}} \cdot \text{s}^{1-\text{EF}} \cdot \text{m}^{-1} )</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PMOS: 1.5e25 ( \text{eV}^{1-\text{EF}} \cdot \text{s}^{1-\text{EF}} \cdot \text{m}^{-1} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>NOIC</code></td>
<td>Flicker noise parameter C</td>
<td>8.75e9 ( \text{eV}^{1-\text{EF}} \cdot \text{s}^{1-\text{EF}} \cdot \text{m} )</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>EM</code></td>
<td>Saturation field</td>
<td>4.1e7V/m</td>
<td>No</td>
<td>-</td>
</tr>
</tbody>
</table>

- **Equations**

  **fnoiMod==0 (simple model):**
  Noise density is 
  \[ S_{id}(f) = \frac{K_F \cdot I_{ds}^{AF}}{C_{ox} L_{eff}^2 f^{EF}} \]

  **fnoiMod==1 (unified physical model):**
  In the inversion region, the noise density is expressed as
  \[
  S_{id,inv}(f) = \frac{kT q^2 \mu_{eff} I_d}{C_{ox} L_{eff}^2 A_{bulk} f^{\eta} \cdot 10^9} \left( NOIA \cdot \log \left( \frac{N_0 + N^+}{N_i + N^+} \right) + NOIB \cdot (N_0 - N_i) + \frac{NOIC}{2} \left( N_0^2 - N_i^2 \right) \right) \\
  + \frac{kT q \Delta L_{lin}}{W_{eff} \cdot L_{eff}^2 f^{\eta} \cdot 10^9} \frac{NOIA + NOIB \cdot N_i + NOIC \cdot N_i^2}{(N_i + N^+)^3}
  \]
where $N^*$, $N_0$, $N_1$, and $\Delta L_{cm}$ are given as

$$N^* = kT \cdot \left( C_{ox} + C_d + C_{it} \right) / q^2, \quad (C_{it} \text{ is a model parameter from DC})$$

$$N_0 = C_{ox} \cdot V_{gs eff} / q$$

$$N_1 = C_{ox} \cdot V_{gs eff} \cdot \left( 1 - \frac{A_{bulk} V_{ds eff}}{V_{gs eff} + 2\nu_t} \right) / q, \quad \text{and}$$

$$\Delta L_{cm} = \frac{1}{\mu_{eff}} \cdot \log \left( \frac{V_{ds} - V_{ds eff}}{E_{sat}} + \frac{E_{sat}}{E_{sat}} \right)$$

$$E_{sat} = \frac{2\nu_t}{\mu_{eff}}, \quad \text{and} \quad L_{it} = \sqrt{3X T_{ox}}$$

In the subthreshold region, the noise density is written as

$$S_{id, sub} (f) = \frac{NO1A \cdot kT \cdot I_{ds}^2}{W_{eff} L_{eff} f^{1/2} N^*} \cdot \cdot \cdot 10^{10}$$

The total flicker noise density is expressed by

$$S_{id} (f) = \frac{S_{id, inv} (f) \cdot S_{id, sub} (f)}{S_{id, sub} (f) + S_{id, inv} (f)}$$
(Holistic) Thermal Noise Model

- General

There are two thermal noise models in BSIM4 as shown in the following figures:
(1) \(tnoiMod=0\) (charge-based): thermal noise model used in BSIM3v3.2.2;
(2) \(tnoiMod=1\) (holistic): new holistic thermal noise model.

In the new thermal noise model, all the short-channel effects and velocity saturation effect incorporated in the IV model are automatically included in the thermal noise model, hence the name "holistic thermal noise model". In addition, the amplification of the channel thermal noise through \(gm\) and \(gmbs\) as well as the induced-gate noise with partial correlation to the channel thermal noise are all captured in the new "noise-partition" model.

- Thermal noise equations

\(tnoiMod=0\):

\[
\bar{i_d}^2 = \frac{4kT\Delta f}{R_{ds}(V) + \frac{L_{eff}}{\mu_{eff}|Q_{inv}|}} \cdot ntnoi
\]

\(tnoiMod=1\):

\[
\bar{v_d}^2 = 4kT \cdot \theta^2 \cdot \frac{V_{dreff} \Delta f}{I_{ds}}
\]

\[
\bar{i_d}^2 = 4kT \frac{V_{dreff} \Delta f}{I_{ds}} \left[\left(g_{ds} + beta \left(\frac{g_m + g_{mbs}}{g_m + g_{ds} + g_{mbs}}\right)\right)^2 - \bar{v_d}^2 \left(g_m + g_{ds} + g_{mbs}\right)^2\right]
\]

where
\[
\theta = 0.37 \cdot \left[ 1 + t\text{noi}b \cdot L_{\text{eff}} \cdot \left( \frac{V_{\text{g}}}{E_{\text{sat}} L_{\text{eff}}} \right)^2 \right]
\]

\[
\beta = 0.577 \cdot \left[ 1 + t\text{noi}a \cdot L_{\text{eff}} \cdot \left( \frac{V_{\text{g}}}{E_{\text{sat}} L_{\text{eff}}} \right)^2 \right]
\]

- **Model Parameters**

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>tnoi</em>Mod</td>
<td>Thermal noise model selector</td>
</tr>
<tr>
<td><em>NTNOI</em></td>
<td>Noise factor for short channel devices for <em>tnoi</em>Mod=0</td>
</tr>
<tr>
<td><em>TNOIA</em></td>
<td>L-dependence parameter for channel thermal noise partitioning</td>
</tr>
<tr>
<td><em>TNOIB</em></td>
<td>L-dependence parameter for channel thermal noise partitioning</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Default value with unit</th>
<th>Binnable?</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>tnoi</em>Mod</td>
<td>0</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td><em>NTNOI</em></td>
<td>1.0</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><em>TNOIA</em></td>
<td>1.5</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><em>TNOIB</em></td>
<td>3.5</td>
<td>No</td>
<td>-</td>
</tr>
</tbody>
</table>

- **Other noise sources modeled in BSIM4**

BSIM4 also models the thermal noise contributions from the substrate, electrode gate, and source/drain resistances. Shot noise due to various gate tunneling current components is modeled as well.
Asymmetric Source/Drain Junction Diode Model with Breakdown

- **Diode IV model selector**

  In BSIM4, there are three junction diode IV models. When the model selector `dioMod` is set to 0 ("resistance-free"), the diode IV is modeled as resistance-free with or without breakdown depending on the parameter values of `XJBVS` or `XJBVD`. When `dioMod` is set to 1 ("breakdown-free"), the diode is modeled exactly the same way as in BSIM3v3.2.2 with current-limiting feature in the forward-bias region through the limiting current `IJTHSFWD` or `IJTHDFWD`; diode breakdown is not modeled for `dioMod`=1 and `XJBVS`, `XJBVD`, `BVS`, and `BVD` parameters all have no effect. When `dioMod` is set to 2 ("resistance-and-breakdown"), BSIM4 models the diode breakdown with current limiting in both forward and reverse operations. In general, setting `dioMod` to 1 produces fast convergence.

- **Model parameters (separate IV and CV parameters for the drain-side and source-side junctions)**

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Default with unit</th>
<th>Binnable</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source side</td>
<td>Drain side</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>NJS</code></td>
<td><code>NJD</code></td>
<td>Junction emission</td>
<td><code>NJS=1.0</code>;</td>
<td>No</td>
</tr>
<tr>
<td><code>XTIS</code></td>
<td><code>XTID</code></td>
<td>temperature</td>
<td><code>XTIS=3.0</code>;</td>
<td>No</td>
</tr>
<tr>
<td><code>IJTHSREV</code></td>
<td><code>IJTHDREV</code></td>
<td>Limiting current</td>
<td><code>IJTHSREV=0.1A</code>;</td>
<td>No</td>
</tr>
<tr>
<td><code>IJTHSFWD</code></td>
<td><code>IJTHDFWD</code></td>
<td>Limiting current</td>
<td><code>IJTHSFWD=0.1A</code>;</td>
<td>No</td>
</tr>
<tr>
<td><code>XJBVS</code></td>
<td><code>XJBVD</code></td>
<td>Fitting parameter</td>
<td><code>XJBVS=1.0</code>;</td>
<td>No</td>
</tr>
<tr>
<td><code>BVS</code></td>
<td><code>BVD</code></td>
<td>Breakdown voltage</td>
<td><code>BVS=10.0V</code>;</td>
<td>No</td>
</tr>
<tr>
<td><code>JSS</code></td>
<td><code>JSD</code></td>
<td>Bottom junction</td>
<td><code>JSS=1.0e-4A/m^2</code>;</td>
<td>No</td>
</tr>
<tr>
<td><code>JSWS</code></td>
<td><code>JSWD</code></td>
<td>Isolation-edge</td>
<td><code>JSWS=0.0A/m</code>;</td>
<td>No</td>
</tr>
<tr>
<td><code>JSWGS</code></td>
<td><code>JSWGD</code></td>
<td>Gate-edge sidewall</td>
<td><code>JSWGS=0.0A/m</code>;</td>
<td>No</td>
</tr>
<tr>
<td><code>CJS</code></td>
<td><code>CJD</code></td>
<td>Bottom junction</td>
<td><code>CJS=5.0e-4F/m^2</code>;</td>
<td>No</td>
</tr>
<tr>
<td><code>PBS</code></td>
<td><code>PBD</code></td>
<td>Bottom junction</td>
<td><code>PBS=1.0V</code>;</td>
<td>No</td>
</tr>
<tr>
<td><code>MJS</code></td>
<td><code>MJD</code></td>
<td>Bottom junction</td>
<td><code>MJS=0.5</code>;</td>
<td>No</td>
</tr>
</tbody>
</table>
BSIM4.0.0 Technical Notes - Diode Model

<table>
<thead>
<tr>
<th>CJSWS</th>
<th>CJSWD</th>
<th>Isolation-edge sidewall junction capacitance per unit length</th>
<th>CJSWS=5.0e-10F/m; CJSWD=CJSWS</th>
<th>No</th>
<th>-</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBSWS</td>
<td>PBSWD</td>
<td>Isolation-edge sidewall junction built-in potential</td>
<td>PBSWS=1.0V; PBSWD=PBSWS</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td>MJSWS</td>
<td>MJSWD</td>
<td>Isolation-edge sidewall junction grading coefficient</td>
<td>MJSWS=0.33; MJSWD=MJSWS</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td>CJSWGS</td>
<td>CJSWGD</td>
<td>Gate-edge sidewall junction capacitance per unit length</td>
<td>CJSWGS=CJSWS; CJSWGD=CJSWS</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td>PBSWGS</td>
<td>PBSWGD</td>
<td>Gate-edge sidewall junction built-in potential</td>
<td>PBSWGS=PBSWS; PBSWGD=PBSWS</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td>MJSWGS</td>
<td>MJSWGD</td>
<td>Gate-edge sidewall junction grading coefficient</td>
<td>MJSWGS=MJSWS; MJSWGD=MJSWS</td>
<td>No</td>
<td>-</td>
</tr>
</tbody>
</table>

Note-1: if $IJTHSREV <= 0.0$, $IJTHSREV$ is set to 0.1.
if $IJTHDREV <= 0.0$, $IJTHDREV$ is set to 0.1.

Note-2: if $IJTHSFWD <= 0.0$, $IJTHSFWD$ is set to 0.1.
if $IJTHDFWD <= 0.0$, $IJTHDFWD$ is set to 0.1.

Note-3: For dioMod=0, if $XJBVS < 0.0$, $XJBVS$ is set to 1.0.
For dioMod=2, if $XJBVS <= 0.0$, $XJBVS$ is set to 1.0.
For dioMod=0, if $XJBVD < 0.0$, $XJBVD$ is set to 1.0.
For dioMod=2, if $XJBVD <= 0.0$, $XJBVD$ is set to 1.0.

Note-4: if $BVS <= 0.0$, $BVS$ is set to 10.0.
if $BVD <= 0.0$, $BVD$ is set to 10.0.

- **IV and breakdown equations**

In the following, the equations will be given only for the source-side diode. The drain-side diode has an analogous set of equations.

**diomod == 0 (resistance-free):**

$$I_{bs} = I_{sbs} \left[ \exp \left( \frac{qV_{bs}}{NJS \cdot kT} \right) - 1 \right] \cdot f_{breakdown} + V_{bs} \cdot G_{min}$$

where $I_{sbs}$ is the total saturation current consisting of the components through the gate-edge and isolation-edge sidewalls and the bottom junction, and $f_{breakdown} = 1 + XJBVS \cdot \exp \left( - \frac{q \cdot (BVS + V_{bs})}{NJS \cdot kT} \right)$

In the above equation, when $XJBVS = 0$, no breakdown will be modeled.

**diomod == 1 (breakdown-free):**

The exponential IV term is linearized at $IJTHSFWD$ in the forward-bias mode only.
The exponential term is linearized at both \textit{IJTHSFWD} in the forward-bias mode and \textit{IJTHSREV} in the reverse-bias mode.

\begin{equation}
I_{bs} = I_{sbs} \left[ \exp \left( \frac{qV_{bs}}{NJS \cdot kT} \right) - 1 \right] + V_{bs} \cdot G_{\text{min}}
\end{equation}

\textbf{diomod == 2 (resistance-and-breakdown):}

The exponential term is linearized at both \textit{IJTHSFWD} in the forward-bias mode and \textit{IJTHSREV} in the reverse-bias mode.

\begin{equation}
I_{bs} = I_{sbs} \left[ \exp \left( \frac{qV_{bs}}{NJS \cdot kT} \right) - 1 \right] \left[ 1 + V_{BS} \cdot \exp \left( - \frac{q(BV + V_{bs})}{NJS \cdot kT} \right) \right] + V_{bs} \cdot G_{\text{min}}
\end{equation}

- **Diode CV model**

The BSIM4 junction diode CV models use equations similar to those of BSIM3v3.2.2, but with separate model parameters used (listed above) for S/D junctions.

\textbf{Note:} The impact of device layout/geometry on the diode IV and CV modeling is given in the section on layout-dependent parasitics model.
**Modeling Series/Parallel Devices**

- **General**

BSIM4 provides a comprehensive and versatile geometry (layout)-dependent parasitics model. This model supports series (such as isolated, shared, or merged S/D) and multi-finger device layout, or a combination of these two configurations.

- **Model parameter and selector**

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Specified on</th>
<th>Description</th>
<th>Default value with unit</th>
<th>Binnable</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>perMod</code></td>
<td>Model card</td>
<td>Whether Ps/Pd (when given) includes the gate-edge perimeter</td>
<td>1 - including the gate-edge perimeter</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td><code>geoMod</code></td>
<td>Model card</td>
<td>Specify how the end S/D diffusions are connected</td>
<td>0 (isolated)</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td><code>rgeoMod</code></td>
<td>instance</td>
<td>Specify the end S/D contact type: point, wide or merged, and how S/D parasitic resistance is computed</td>
<td>0 - no S/D diffusion resistance</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td><code>rgateMod</code></td>
<td>Model card</td>
<td>Select different gate resistance models</td>
<td>0 - no gate resistance</td>
<td>NA</td>
<td>-</td>
</tr>
<tr>
<td><code>DMCG</code></td>
<td>Model card</td>
<td>Distance from the contact center to the gate edge</td>
<td>0m</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>DMCI</code></td>
<td>Model card</td>
<td>Distance in the channel length direction from the contact center to the isolation edge</td>
<td><code>DMCG</code></td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>DMDG</code></td>
<td>Model card</td>
<td>Same as <code>DMCG</code> but for merged devices only</td>
<td>0m</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>DMCGT</code></td>
<td>Model card</td>
<td><code>DMCG</code> in test structures</td>
<td>0m</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>NF</code></td>
<td>instance</td>
<td>Number of device fingers</td>
<td>1</td>
<td>No</td>
<td>Note-1</td>
</tr>
<tr>
<td><code>DWJ</code></td>
<td>Model card</td>
<td>Offset of the S/D junction width due to variations</td>
<td><code>DWC</code> - used in CV model</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>MIN</code></td>
<td>instance</td>
<td>Whether to minimize the number of drain or source diffusions for even-number finger only</td>
<td>0 - minimize the drain diffusion numbers</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>RSHG</code></td>
<td>Model card</td>
<td>Gate electrode sheet resistance per square</td>
<td>0 ohm/square</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>XGW</code></td>
<td>Model card</td>
<td>Distance from the gate contact to the channel edge</td>
<td>0m</td>
<td>No</td>
<td>-</td>
</tr>
<tr>
<td><code>XGL</code></td>
<td>Model card</td>
<td>Offset of the gate length due to variations in patterning</td>
<td>0m</td>
<td>no</td>
<td>-</td>
</tr>
<tr>
<td><code>NGCON</code></td>
<td>Model card</td>
<td>Number of gate contacts</td>
<td>1</td>
<td>no</td>
<td>Note-2</td>
</tr>
</tbody>
</table>

33
Note-1: if less than 1, fatal error;
   if greater than 500, a warning message is given and reset to 20.
Note-2: if less than 1, fatal error;
   if not equal to 1 or 2, a warning message is given and reset to 1.

Details

In the following, only the source-side case is illustrated. The same approach is used for the drain side.

Calculation of Pseff and Aseff
If (Ps is given)
   If (permMod=0)
      Pseff=PS
   Else
      Pseff=PS – Weffcj * NF
   Else
      Pseff computed from NF, DWJ, GEOMOD, DMCG, DMCI, DMDG, DMCGT, and MIN.

If (As is given)
   Aseff=AS
Else
   Aseff computed by NF, DWJ, GEOMOD, DMCG, DMCI, DMDG, DMCGT, and MIN.

NOTE: Pseff and Aseff will be used in junction diode IV and CV evaluations. Pseff itself does not include the gate-edge perimeter. In other words, the total source junction perimeter is equal to (Pseff + Weffcj * NF).

Calculation of S/D resistance
If (rgeoMod = 0)
   The diffusion resistance Rs and internal source node sNodePrime are not generated
Else if (the number of source squares NRS is given)
   Rs=NRS * Rsheet
Else
   Rs computed from NF, DWJ, GEOMOD, DMCG, DMCI, DMDG, DMCGT, and MIM.

Calculation of Weffcj
Weffcj, per-finger device junction width, is used in computation of parasitics, GIDL and bias-dependent Rds(V), not used to compute Ids, intrinsic CV and overlap CV. Weffcj is defined as

$$W_{effc_j} = \frac{W_{drawn}}{NF} - 2 \left( \frac{DWJ + \frac{W_{lc}}{L_{ln}} + \frac{W_{wc}}{W_{wm}} + \frac{W_{wlc}}{L_{ln}W_{wm}}} {L_{ln}W_{wm}} \right)$$

Definition for Wdrawn, PS, PD, AS and AD in the instance line
These instance parameters are defined as the total values for a multi-finger device, not the values for each finger.
• **geoMod option**

<table>
<thead>
<tr>
<th>geoMod</th>
<th>End source</th>
<th>End drain</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>isolated</td>
<td>isolated</td>
<td>NF=Odd</td>
</tr>
<tr>
<td>1</td>
<td>isolated</td>
<td>shared</td>
<td>NF=Odd, Even</td>
</tr>
<tr>
<td>2</td>
<td>shared</td>
<td>isolated</td>
<td>NF=Odd, Even</td>
</tr>
<tr>
<td>3</td>
<td>shared</td>
<td>shared</td>
<td>NF=Odd, Even</td>
</tr>
<tr>
<td>4</td>
<td>isolated</td>
<td>merged</td>
<td>NF=Odd</td>
</tr>
<tr>
<td>5</td>
<td>shared</td>
<td>merged</td>
<td>NF=Odd, Even</td>
</tr>
<tr>
<td>6</td>
<td>merged</td>
<td>isolated</td>
<td>NF=Odd</td>
</tr>
<tr>
<td>7</td>
<td>merged</td>
<td>shared</td>
<td>NF=Odd, Even</td>
</tr>
<tr>
<td>8</td>
<td>merged</td>
<td>merged</td>
<td>NF=Odd</td>
</tr>
<tr>
<td>9</td>
<td>sha/iso</td>
<td>shared</td>
<td>NF=Even</td>
</tr>
<tr>
<td>10</td>
<td>shared</td>
<td>sha/iso</td>
<td>NF=Even</td>
</tr>
</tbody>
</table>

NOTE: All inside S/D are assumed shared. For end S/D, Pseff, Pdeff, Aseff, Adeff are all geoMod dependent.

• **rgeoMod option**

<table>
<thead>
<tr>
<th>rgeoMod</th>
<th>End-source contact</th>
<th>End-drain contact</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No Rs</td>
<td>No Rd</td>
</tr>
<tr>
<td>1</td>
<td>wide</td>
<td>wide</td>
</tr>
<tr>
<td>2</td>
<td>wide</td>
<td>point</td>
</tr>
<tr>
<td>3</td>
<td>point</td>
<td>wide</td>
</tr>
<tr>
<td>4</td>
<td>point</td>
<td>point</td>
</tr>
<tr>
<td>5</td>
<td>wide</td>
<td>merged</td>
</tr>
<tr>
<td>6</td>
<td>point</td>
<td>merged</td>
</tr>
<tr>
<td>7</td>
<td>merged</td>
<td>wide</td>
</tr>
<tr>
<td>8</td>
<td>merged</td>
<td>point</td>
</tr>
</tbody>
</table>

NOTE: Wide contacts are assumed for all inside S/D. The computation of Rs and Rd also depends on the setting of geoMod.

• **Diode saturation current and capacitances**

Saturation current is computed as

\[
\text{Isbs} = \begin{cases} 
1.0e-14; & \text{if } ((Aseff \leq 0.0) \text{ and } (Pseff \leq 0.0)) \\
Aseff \times \text{unitAreaIsbs} + Pseff \times \text{unitLengthSidewallIsbs} + Weffcj \times NF \times \text{unitLengthGateSidewallIsbs}; & \text{Otherwise}
\end{cases}
\]

Zero-bias junction capacitances are calculated by

Bottom junction: \(czbs = \text{unitAreaJctCap} \times Aseff;\)
Isolation-edge sidewall: \(czbssw = \text{unitLengthSidewallJctCap} \times Pseff;\)
Gate-edge sidewall: \(czbdswg = \text{unitLengthGateSidewallJctCap} \times Weffcj \times NF;\)
Total zero-bias Source junction capacitance: \(czbs = czbs + czbssw + czbdswg.\)

• **rgateMod options**

Please refer to the section on “Electrode and intrinsic input resistance model”.
- Definition for layout parameters

DMCI of Point contact

DMCG of Wide contact

DMDG No contact

DMCI of Wide contact

L-XGL
Modeling Temperature Dependence

- General

BSIM4 models the temperature dependencies with the same sets of model equations as those in BSIM3v3.2.2. But separate sets of model parameters are used for source/drain junction diodes to model asymmetry.