0.35 μm CMOS PROCESS ON SIX-INCH WAFERS, Baseline Report V.

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0.35 μm CMOS PPROCESS ON SIX-INCH WAFERS

Baseline Report V.

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February, 2007

Abstract

This report presents details of the third six-inch baseline run, CMOS170, where a moderately complex 0.35 μm twin-well, silicided process was used. This process was based on the first six-inch 0.35 μm run, CMOS161. Different research circuits (IC/MEMS) were placed in the drop-in area, i.e. ring oscillators, a MEMS design, a hyperacuity chip and several different memory circuits. A more complex (triple metal) process flow consisting of 66 steps was introduced by this version of the 0.35 μm process, with the main objective of matching N-channel and P-channel threshold voltages (V_t, absolute values). According to simulations the NMOS threshold voltage was matched to the PMOS values by decreasing the NMOS V_t implantation dose.

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1. INTRODUCTION

This is the third six-inch baseline report we are submitting, describing the latest development in CMOS baseline in the UC Berkeley Microlab. Baseline runs, in conjunction with regular equipment monitoring, play an important role in process control in the Microlab.

CMOS baseline runs had been processed regularly on 4 inch wafers up until 2001; then the first six-inch run (CMOS150) successfully transferred the old 1 µm baseline onto six-inch wafers [1]. CMOS150 was followed by a new and more advanced, 0.35 µm process, which produced the first sub-half micron devices. Run CMOS161 not only established our new 0.35 µm process, but also helped us push out the performance of some of our tools to more advanced processes [2].

The latest baseline run, CMOS170, was initiated with the main goal of further improving device performance as well as introducing a triple metal process into the Microlab. This report includes detailed process flow, parametric test results and motivation behind the latest 0.35 µm six-inch run, CMOS170.

2. PROCESS DEVELOPMENT AND SIMULATION

The first 0.35 µm six-inch run described [2] earlier, yielded well with working NMOS and PMOS devices that had about 0.1 Volt threshold voltage difference ($\Delta Vt \simeq 0.1V$, absolute values of NV_t and PV_t). This prompted us to improve further these electrical parameters, as well as including a triple metal process to satisfy IC requirements on the new test chip. The NMOS threshold implant dose was therefore changed to decrease the NV_t voltages for a better match with the PV_t values. Please note, PV_t values were in the specified range defined by the 0.35 µm process (0.5 V-0.6 V), and satisfied by the previous run (CMOS 161). More simulation and further investigation of the previous run suggested a threshold implant dose reduction, which was applied to a group of 5 wafers in this run. Therefore, wafers 6-10 received implant dose of $3x10^{12}$ cm^{-2}, while the rest of the wafers received $4x10^{12}$ cm^{-2} of BF2 implant (control group). Simulation data in Fig.1 shows a 25% BF2 dose reduction would result in a 0.1 V drop in NMOS transistor threshold voltage (NV_t) and a 50% reduction in dose results in a 0.2 V NV_t drop.

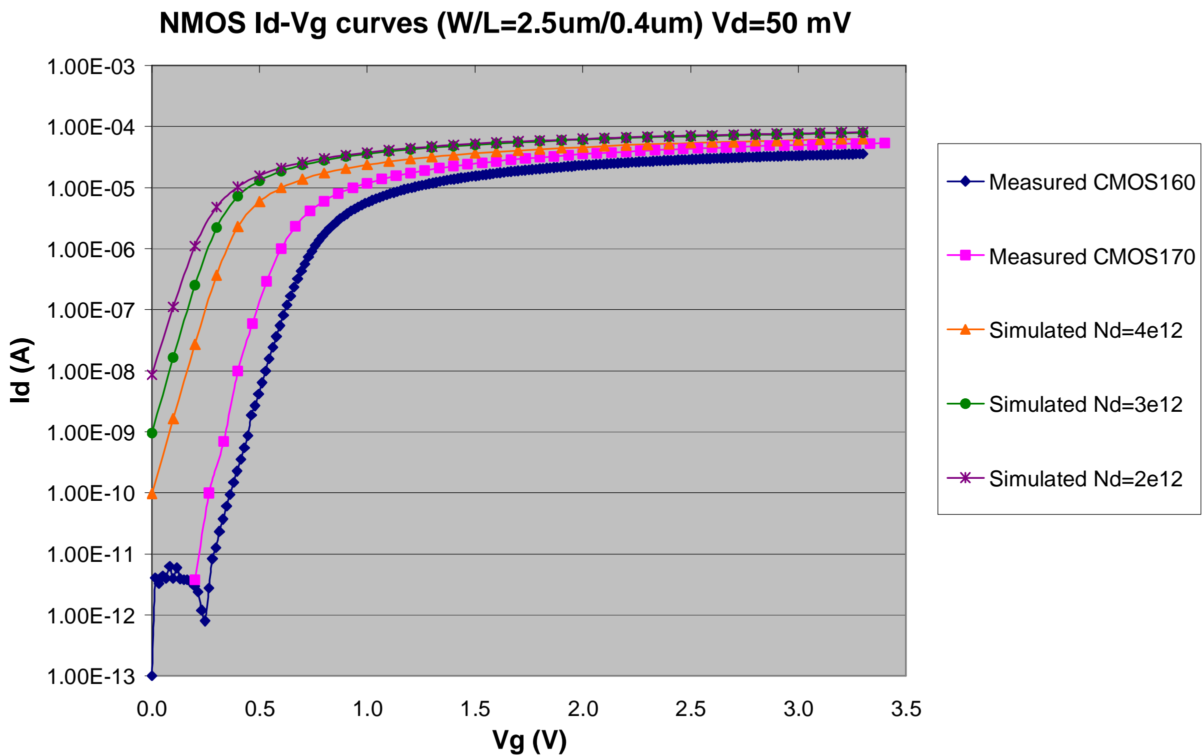


Fig. 1. The simulated effects of NMOS V_t implant dose reduction on NV_t values.

3. CMOS BASELINE FABRICATION PROCESS

A moderately more complex and improved version of the initial 0.35 μm process (CMOS161 run) was used for the new baseline run, which was called CMOS170. This included a triple metal process that utilized chemical-mechanical polishing (CMP) on all of our inter metal dielectric layers, and a new NV_t implant dose to fine tune the electrical parameters. We were also able to push our DUV lithography tool by making 0.3 μm functional transistors on the new run, which was completed in December 2006.

3.1. CMOS170 chip layout

The schematic layout of the CMOS170 chip is shown on Fig. 2. The single transistor section of the old chip was redesigned to address different technologies by arranging the individual transistors into three separate columns. Each column consists of a 5x3 array of PMOS and NMOS transistors, which are varying in channel length (L=0.3, 0.35, 0.4, 0.5, and 1 μm) and channel width (W=2.5, 5, and 7.5 μm). The first column on the left used a more robust design rule, basically followed the old transistor layout, which have already been tested, proven by the CMOS160 run, earlier. These transistors do not follow any specific industrial layout design rule; their gates are reduced while their contacts, active areas, metal lines, etc. are kept within very safe design/processing limit. This report focuses on this group of transistors, which yielded well and achieved our V_t adjustment (NV_t implant split) objective.

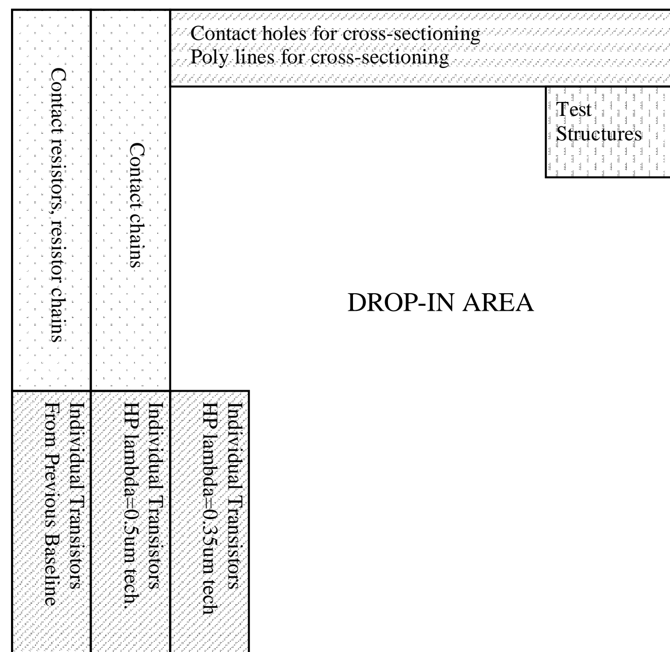


Fig. 2. Schematic layout of the CMOS170 chip

The success of our earlier CMOS161 run, upgrade of Microlab tools and refinement of our 0.35 µm technology prompted us to also try a more aggressive design approach by applying lambda scale design rules to column 2 and 3 transistors. The column 2 transistors in the middle, therefore, received Hewlett Packard's (HP) λ=0.5 µm design rules, while transistors on the third column followed the HP design rules for λ=0.35 µm. These transistors were also successfully fabricated on the baseline chip, more details later. Following industry standards, such as HP design rules, enabled us to push our process boundaries and tool capabilities in the Microlab, also provided an opportunity for a more aggressive future design.

Contact resistors, resistor chains are included in the layout of the baseline chips to monitor the contact resistance value (contact variation) between different process layers [3]. In the latest version of the baseline layout (CMOS161) contact resistance value approached transistor's "on" resistance value, as a result of downscaling the transistors in the layout deign. Contact and via holes sizes of 2, 1.5, 1, and 0.7 µm were included in the new CMOS170 design between the Metal3, Metal2, Metal1, P+ Poly, N+ Poly, P+ Active, and N+ active areas, following transistor contact and via resistance requirements. Complex circuits in the drop-in area require the fabrication of a great number of contacts per die. Therefore, there is a need to monitor the susceptibility of these contacts to random fault and reliability failures, since failure in a single contact or via can be catastrophic to circuit functionality. **Contact chains** are simply long serpentines of contacts connected to each other by two alternating layers of interconnect. Each of the chains consists of 104 contacts between different process layers. These contact chains are expanded version of contact resistors used between the same layers noted earlier. The contact sizes are however larger in this case (1 µm and 2 µm).

The baseline test chip also includes a series of 6 mm long **contact holes and poly lines (chains)** of different sizes located at the upper part of CMOS170 test chip. The contact and poly chains (rows) are offset from each other, just enough, so that any wafer cleaving across the die in the Y direction (perpendicular to wafer flat) will result in engaging one or more contact/poly structures for scanning electron microscopy inspection. Each row contains one contact hole size, all together covering contact sizes of 10, 2, 1, 0.5, 0.35 µm, while the poly lines cover range of 2, 1, 0.5, 0.35, 0.3, 0.25, 0.2 µm provide smaller geometries for litho end etch monitoring/analysis.

The **test structures** section of the baseline chip (top right) also provides necessary structures for in situ monitoring of critical dimension and final analysis of junction depth and early transistor testing on the actual work wafers. These include resolution forks for critical dimension (CD) measurement, several 100 µm x 100 µm boxes for thin film thickness/resistivity measurement of

all deposited grown films, 1μm wide PMOS and NMOS transistors with a large 100 μm x 100 μm S/D and poly area for early characterization of transistors (pre-metal deposition step by making 3 terminal direct contact to S/D/G area of the transistor), as well as 500 μm long pads for spreading resistance analysis (SRP), which can generate junction depth and dopant concentration data in these implanted pads. The **drop-in area** of the baseline chip is open to experimental IC/MEMS test chips provided by internal/external researchers at a cost. Several NOR and NAND gates of different sizes, a few ring oscillators, buffer and inverter circuits of different sizes, an 8 bit adder, a hyperacuity chip, a MEMS design, as well as special test structure for contact plug study were included in the CMOS170 baseline chip.

The **hyperacuity die** included in the CMOS170 baseline chip is a Time-to-Digital Converter (TDC), which performs an Analog to Digital (A/D) Conversion. The continuous-valued input, however, is not expressed by a voltage or current, but by a time delay. The circuit receives rising edge transitions on two input pins, and the timing order and amount of delay between these two signals is coded into a binary number resulting in a much higher resolution (time converted in space) and accuracy in time. A 25 picosecond time resolution can be realized, which in a conventional circuit would be operating in nanosecond range designed for our 0.35 μm process. The design idea was taken from biological models of auditory processing in the Barn Owl. Time is coded in space via arrays of cells receiving the signals. The block diagram of the implanted TDC architecture is shown in Fig.3. The detailed architecture description can be found in Ref. [4].

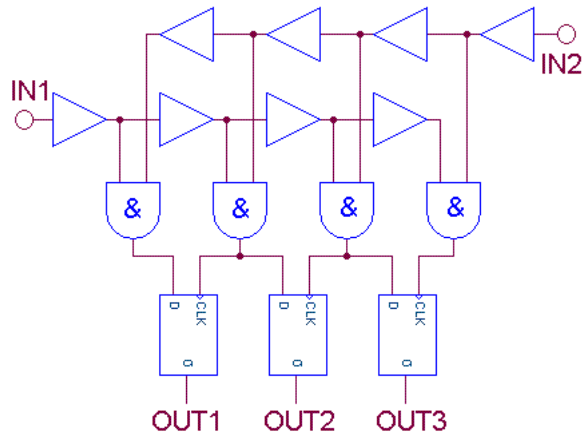


Fig. 3. Block diagram of the implemented Time-to-Digital Converter architecture. Delay chains replace Magnocellular axons, AND gates act like coincidence detector NL neurons, D-latches formulate and store the output thermometer code.

The hyperacuity TDC circuit is functionally divided into two main parts: the delay path and a cellular neural network (CNN). The role of the delay part is to perform the topographic mapping of the input information. The CNN network is responsible for amplification of the stimuli map, and decision-making according to a winner-takes-all strategy. There are of course some additional glue logic, integrated on-chip: A register and a multiplexer were also needed to interface the hyperacuity chip to the outside world. These make the result data readout possible.

The **MEMS** structure included in the CMOS170 layout is an electrostatic mono-directional in-plane displacement microactuator [5]. The device enables a direct evaluation of Young's modulus in a variety of thin film materials (SiC, SiGe, and poly-Si are examples of the materials that may be evaluated). The fabrication steps of the MEMS structure are performed parallel to the CMOS Baseline process flow. The post processing steps, shown in Fig 4, consist of a test-material deposition, pattern, etch, and release.

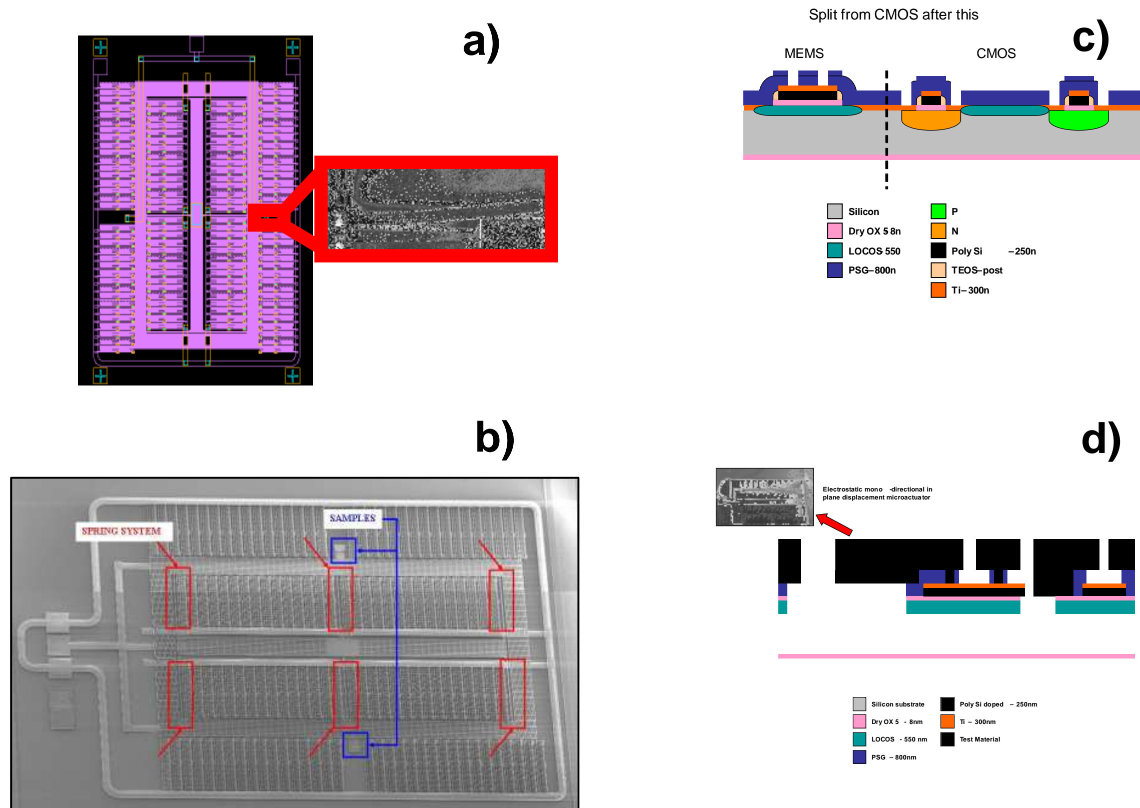


Fig. 4. The electrostatic monodirectional in-place displacement actuator (a) and evaluation (b) of Young's modulus from elastic bending of beam. Fabrication steps of the MEMS structure are performed parallel to the CMOS baseline process flow (c). MEMS post CMOS processing steps follow (d). [6]

3.2. CMOS170 Baseline Fabrication Process

Iterative computer simulation and lessons learnt from previous baseline runs were used to optimize the new 0.35 μm process The final version of the 0.35 μm process consists of 66 steps including the triple metal module needed for the fabrication of more complex circuitry, test dies on the CMOS170 test chip. N-channel and P-channel MOSFET devices, as well as some simple circuits were tested at step 51, post metal1 step, all yielding well with functional devices. This prompted us to continue the run through triple metal process, while testing devices/circuits at metal1, metal2 and metal 3 steps to monitor the health of the run.

Table 1, outlines the process steps used for the triple metal version of the 0.35 μm baseline run. The starting material for this process is P-type wafer with <100> orientation and 36-63 Ohm-cm resistivity. This process utilizes thin gate oxide, lightly doped drain structure, PECVD oxide sidewall spacers, titanium silicide S/D and poly work function engineering. A 0.25 μm thick layer of undoped polysilicon material was deposited, then patterned/etched to form the poly gate electrode structures. These poly gates were then selectively implanted to have their work function adjusted and matched for desired V_t values, based on the computer simulation results obtained earlier. This was achieved by exposing the N- and P- channel transistors' gate electrode during their respective source/drain implant steps (N S/D and P S/D masks were modified to allow for this). CMP and PECVD TEOS inter-metal dielectric was also used for the triple metal version of the 0.35 μm process. This version is fully supported by CMOS170 mask set.

Appendix A shows the test chip layout.
Appendix B contains the detailed process flow.

The CMOS170 process included 21 lithography steps. There were masks used on two layers, which brought the total number of masks down to 15, including the zero layer mask used by the ASML to print alignment marks, also the mask used for opening the pre-alignment marks for easier alignment, after metal depositions and before metal lithography.

Step 0. Starting wafers	Step 33. N-type LDD implant photo
Step 1. Initial oxidation	Step 34. N-type LDD implant
Step 2. Zero layer photo	Step 35. LDD spacer deposition
Step3. Zero layer etch	Step 36. LDD spacer etch
Step 4. Pad oxidation/nitride deposition	Step 37. P+ gate and S/D photo
Step 5. N-well photo	Step 38. P+ gate and S/D implant
Step 6. Nitride etch	Step 39. N+ gate and S/D photo
Step 7. N-well implant	Step 40. N+ gate and S/D implant
Step 8. Nitride removal	Step 41. Backside etch
Step 9. Pad oxidation/nitride deposition	Step 42. Gate and S/D annealing
Step 10. P-well photo	Step 43. Silicidation (Ti)
Step 11. Nitride etch	Step 44. PSG dep. and densification
Step 12. P-well implant	Step 45. Contact photo
Step 13. Nitride removal	Step 46. Contact etch
Step 14. Well drive in	Step 47. Metal 1 deposition
Step 15. Pad oxidation/nitride deposition	Step 48. Metal 1 photo
Step 16. Active area photo	Step 49. Metal 1 aluminum etch
Step 17. Nitride etch	Step 50. Sintering
Step 18. P-well field implant photo	Step 51. Testing
Step 19. P-well field ion implant	Step 52. Dielectric deposition/planarization
Step 20. LOCOS oxidation	Step 53. Via 1 Photo
Step 21. Nitride and pad oxide removal	Step 54. Via 1 Etch
Step 22. Sacrificial oxidation	Step 55. Metal 2 deposition
Step 23. Screen oxidation	Step 56. Metal 2 photo
Step 24. NMOS Vt adjust. implant photo	Step 57. Metal 2 etch
Step 25. NMOS Vt adjustment implant	Step 58. Testing
Step 26. PMOS Vt adjust. implant photo	Step 59. Dielectric deposition/planarization
Step 27. PMOS Vt adjust. implant	Step 60. Via 2 photo
Step 28. Gate oxidation, poly-Si dep.	Step 61. Via 2 etch
Step 29. Gate photo	Step 62. Metal 3 deposition
Step 30. Poly Si etch	Step 63. Metal 3 photo
Step 31. P-type LDD implant photo	Step 64. Metal 3 etch
Step 32. P-type LDD implant	Step 65. Testing

Table 1 – Process steps of CMOS170 baseline run

Table 2 lists all the lithography steps used for the fabrication of CMOS170, as well as the corresponding mask ID and the hard bake methods used for these photolithography steps. All lithography steps were done on a DUV 248 nm ASML stepper. As indicated BARC (Bottom Anti-Reflective Coating) layer was applied at several lithography steps (ARC-600 product type).

Step	Resist	Mask	Hard bake
Zero layer photo	Shipley UV-210-0.6 9000Å	Zero layer mask PM marks	UVBAKE, program J
N-well photo	Shipley UV-210-0.6 9000Å	NWELL mask (Dark field)	Oven bake 120C, 2hrs
P-well photo	Shipley UV-210-0.6 9000Å	PWELL mask (Clear field)	Oven bake 120C, 2hrs
Active area photo	Shipley UV-210-0.6 9000Å	ACTIVE mask (Clear field)	Oven bake 120C, 2hrs
P-well field imp. photo	Shipley UV-210-0.6 9000Å	PFIELD mask (Clear field)	Oven bake 120C, 2hrs
NMOS Vt adj. implant photo	Shipley UV-210-0.6 9000Å	PWELL mask (Clear field)	UVBAKE, program J
PMOS Vt adj. implant photo	Shipley UV-210-0.6 9000Å	NWELL mask (Dark field)	UVBAKE, program J
Poly gate photo	Shipley UV-210-0.6 9000Å + ARC-600	POLY mask (Clear field)	UVBAKE, program U
P-type LDD implant photo	Shipley UV-210-0.6 9000Å	PSELECT mask (Dark filed)	UVBAKE, program J
N-type LDD implant photo	Shipley UV-210-0.6 9000Å	NSELECT mask (Dark field)	UVBAKE, program J
P+ Gate & S/D photo	Shipley UV-210-0.6 9000Å	PSELECT mask (Dark filed)	UVBAKE, program J
N+ Gate & S/D photo	Shipley UV-210-0.6 9000Å	NSELECT mask (Dark field)	UVBAKE, program J
Contact photo	Shipley UV-210-0.6 9000Å + ARC-600	CONTACT mask (Dark field)	Oven bake 120C, 1hr
New PM marks	Shipley UV-210-0.6 9000Å	Zero layer mask PM marks	UVBAKE, Program U
Metal1 photo	Shipley UV-210-0.6 9000Å + ARC-600	METAL1 mask (Clear field)	UVBAKE, program U
Via1 photo	Shipley UV-210-0.6 9000Å	VIA1 mask (dark field)	UVBAKE program U
Opening 4 dies for PM marks	Shipley UV-210-0.6 9000Å	Blank mask	UVBAKE, Program U
Metal2 photo	Shipley UV-210-0.6 9000Å + ARC-600	METAL2 mask (clear field)	UVBAKE program U
Via2 photo	Shipley UV-210-0.6 9000Å	VIA2 mask (dark field)	UVBAKE program U
Opening 4 dies for PM marks	Shipley UV-210-0.6 9000Å	Blank mask	UVBAKE, Program U
Metal3 photo	Shipley UV-210-0.6 9000Å + ARC-600	METAL3 mask (clear field)	UVBAKE program U

Table 2 – Lithography steps and related information

The CMOS170 process required 9 ion implantations, all of which were performed at Core Systems (Sunnyvale, CA). The list of the implantation steps, including implant parameters and blocking materials are shown in Table 3. Implantation split was introduced at NMOS Vt implant, aimed at fine tuning the threshold voltage for NMOS to match to the threshold voltage of PMOS devices. Wafers designated as PCH and NCH were used as in line test monitors.

Step	Species	Dose (cm^{-2})	Energy (KeV)	Wafers	Masking materials
N-well implant	Phosphorus	1E13	150	#1-10, PCH	220nm Si3N4 +PR (Oven bake)
P-well implant	Boron	5E12	60	#1-10, NCH	220nm Si3N4 + PR (Oven bake)
P-well field imp.	Boron	2E13	80	#1-10	PR (Oven bake)
NMOS Vt imp. (Split)	BF2 BF2	4E12 3E12	50 50	#1-5, #6-10, NHC	PR (UVBAKE)
PMOS Vt imp.	Phosphorus	2E12	30	#1-10, PCH	PR (UVBAKE)
P-type LDD imp.	BF2 BF2	5E13 5E13	10, +7 deg. 10, -7 deg.	#1-10, PCH, Tpoly1	PR (UVBAKE)
N-type LDD imp.	Arsenic Arsenic	5E13 5E13	30, +7 deg. 30, -7 deg.	#1-10, NCH, Tpoly2	PR (UVBAKE)
P+ Gate & S/D im.	Boron	3E15	20	#1-10, PCH, Tploy1	PR (UVBAKE)
N+ Gate & S/D im.	Phosphorus	3E15	40	#1-10, NCH, Tpoly2	PR (UVBAKE)

Table 3 – List of implantation steps and parameters

Threshold implant split results are discussed in the parametric test result section, 4.2.
Table 4 contains the list of tools used for the fabrication of the CMOS170 run.

Process module	Tool*	Process step
Lithography	ASML 5500/90 DUV stepper	Listed in Table 2
	SVGCOAT6	
	SVGDEV6	
	UVBAKE	
Plasma etch	AMAT Centura MxP+	Nitride etch
		Oxide etch
		Oxide spacer etch
	Lam 3	Aluminum etch
	Lam 5	Poly-Si etch
High temperature treatment	Tystar 1	Wet/dry oxidation
	Tystar 2	
	Heatpulse 3 (RTP)	Annealing
		Silicidation
CVD	Applied P-5000 (PECVD)	Oxide spacer deposition
	Tystar 9 (LPCVD)	Nitride deposition
	Tystar 10 (LPCVD)	Poly-Si deposition
	Tystar 11 (LPCVD)	PSG deposition
Thin film systems	Novellus	Ti deposition
		Al deposition
	CPA	Al deposition
Wet etch/Cleaning	Sink 6	Pre-furnace piranha clean
		HF dip (10/1, 25/1)
		Rinse (QDR)
	Sink 7	Hot phosphoric etch
		Rinse (QDR)
	Sink 8	Post-lithography piranha clean
		HF dip (5/1)
		Rinse (QDR)

* Detailed tool information at http://microlab.berkeley.edu/labmanual/Labmanualindex.html

Table 4 – Process tool set

4. MEASUREMENT RESULTS OF CMOS170

4.1 Spreading Resistance Analysis (SRA)

Spreading Resistance Analysis was carried out by Solecon Laboratories Inc. (Reno, NV). Graphical presentation of the measurement results, carrier concentration vs. implant depth profile are shown on Fig. 5 and 6.

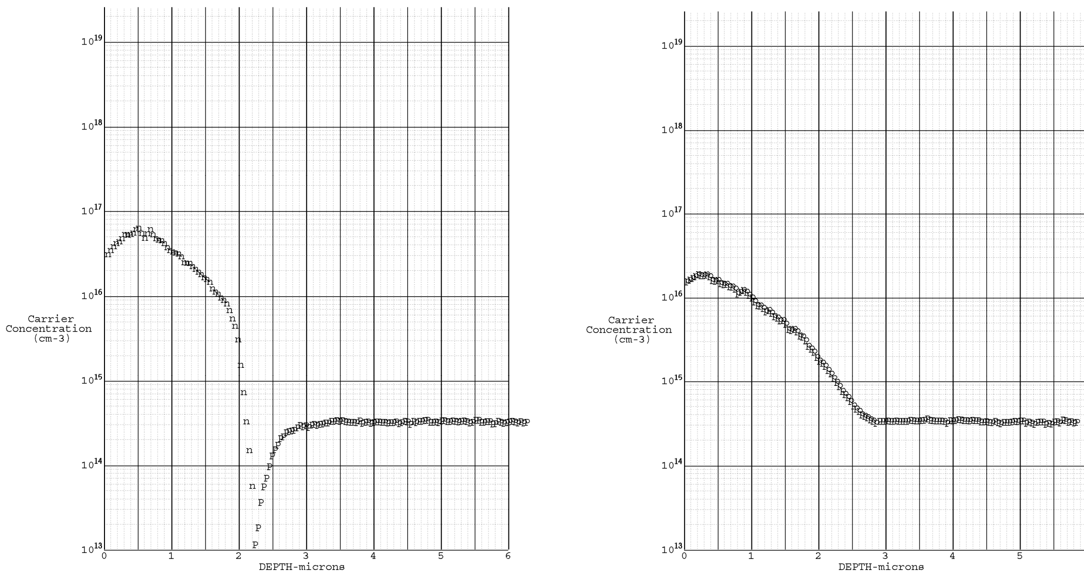


Fig. 5. P-channel (left) and N-channel (right) doping profile under gate oxide

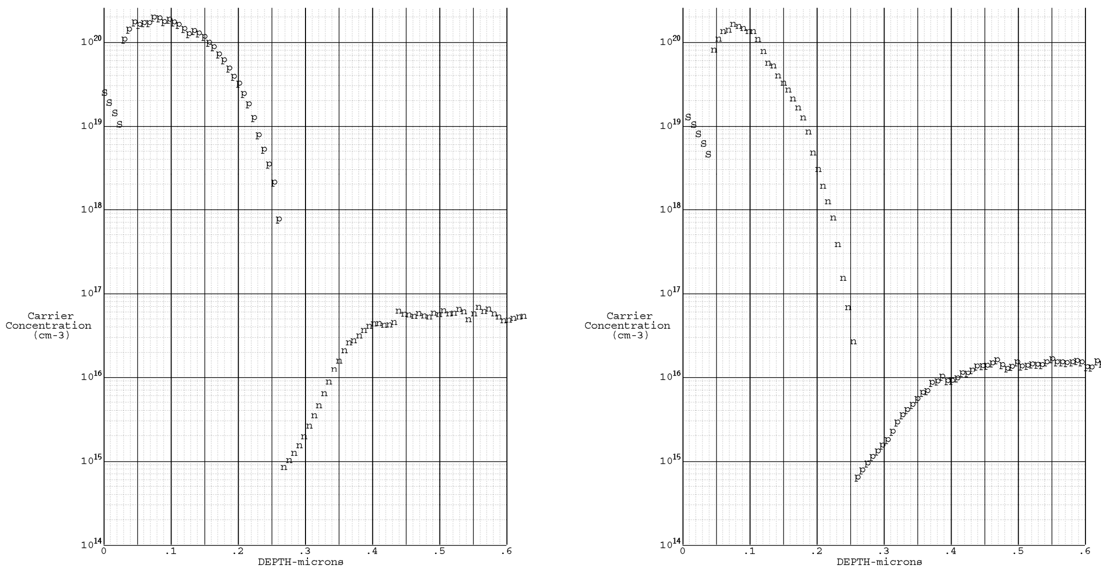


Fig. 6. P+ source-drain (left) and N+ source-drain (right) doping profile

4.2 Electrical measurement results

Electrical measurements were obtained using an automated test system. The HP4062A Semiconductor Parametric Test System utilizes an HP4085A Switching Matrix, an HP4084B Switching Matrix Controller and an Agilent4142B Modular DC Source/Monitor Unit. The system is connected to a Model 2001X Electroglas probe station, which is controlled by a Metrics I/CV software running on a PC workstation. All the test structures and transistors were configured with proper pad array on the chip that would support a 2 x 5 pin probe card (10 tips). Test structure layout was set up this way to allow fast and accurate collection of a large amount of data on device parameters, and other process monitoring related items.

The PC based Metrics software, which includes measurement modules, was used for parametric testing [7]. The following functions have been used to calculate and display transistor characteristics, and to extract transistor and process parameters:

- NIDVD_170 & PIDVD_170 – drain current vs. drain voltage measurement
- NVT_170 & PVT_170 – drain current vs. gate voltage measurement and threshold voltage calculation
- NBODY_170 & PBODY_170 – body bias effect calculation
- DIBL – drain induced barrier lowering effect calculation
- NSATCUR_170 & NSATCUR_170 – saturation current and trans-conductance calculation
- EFFMOB_N*_170 & EFFMOB_P*_170 – effective mobility calculation
  Note: *= 03, 035, 04, 05, 1 indicates the channel width
- M1M2Contactres & M2M3Contactres – contact resistance measurement
- BVds – breakdown voltage of source-drain
- BVox – breakdown voltage of gate oxide

I-V results

The following graphs show typical I-V characteristics of CMOS170 transistors, which were measured on 0.3 μm drawn channel length and 2.5 μm width transistors. Fig. 7 and Fig. 8 demonstrate the Id-Vg, Fig. 9 the Id-Vd curves.

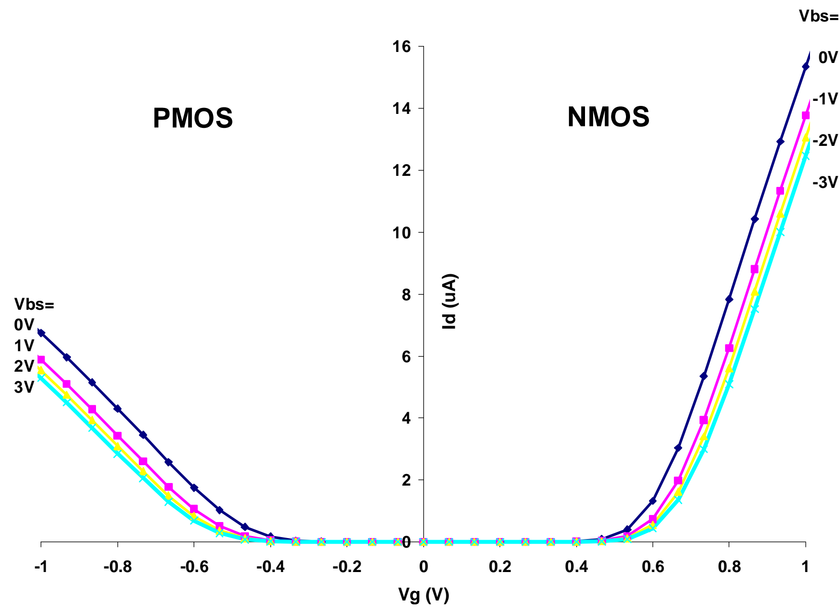


Fig. 7. Drain current vs. gate voltage at varying substrate bias on PMOS and NMOS transistors in the linear region (Vd = 50mV)

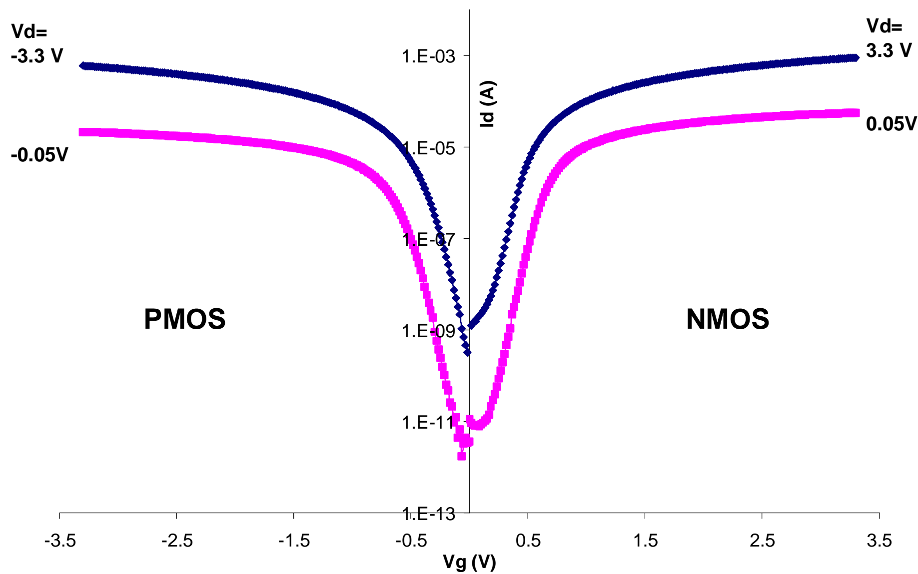


Fig. 8. PMOS and NMOS sub-threshold characteristics

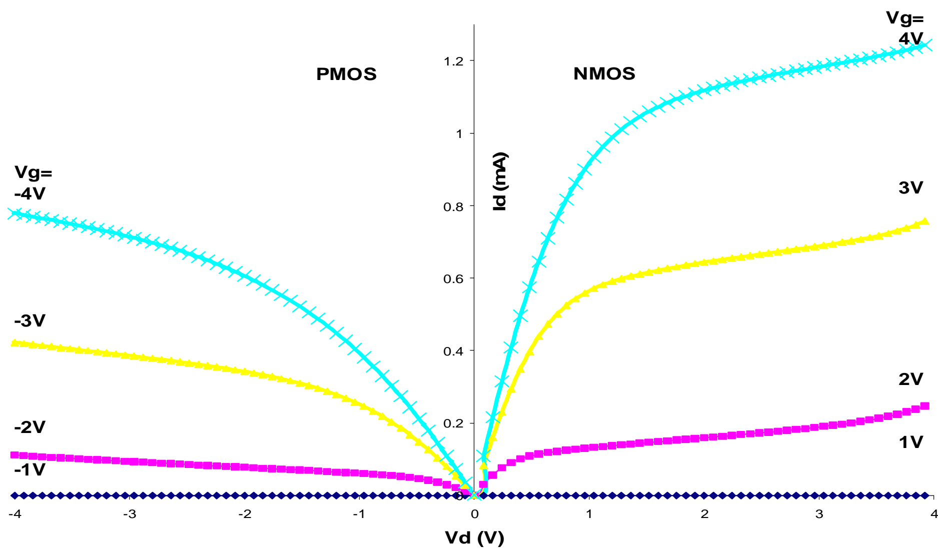
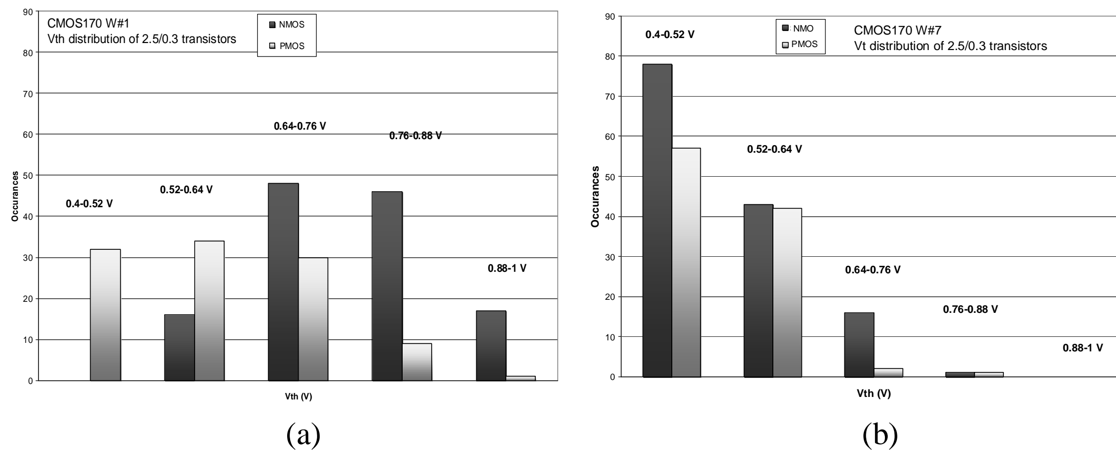


Fig. 9. Drain current vs. drain voltage characteristics of PMOS and NMOS devices

Vt targeting

Threshold voltage adjustment implant splits were applied during the manufacturing process, which was presented previously in Section 2. The following histograms, Fig. 10, show how threshold voltages shifted as a result of these splits.



(a) (b)

Fig. 10. Threshold voltages in NMOS split groups:

(a) NMOS split group #1: Wafers #1, 2, 3, 4, 5 (NVt implant dose 4E12)

(b) NMOS split group #2: Wafers #6, 7, 8, 9, 10 (NVt implant dose 3E12)

Ring oscillators

After the second metal layer deposition ring oscillators were tested. Various types and gate length ring oscillators are available on the test chip; 0.35 µm, 0.5 µm, 1 µm and 2 µm gate length conventional, as well as; 0.6 µm and 1.2 µm gate length voltage controlled ring oscillators. Each device consists of 31 stages. Measurement results for the 1µm gate length oscillator circuitry are presented in Fig. 11, displaying a snap shot of the HP 54503A 500MHz digital oscilloscope screen, frequency curve and measured values. The average oscillation frequency was measured to be 62.2 MHz. The gate delay time using the t_d equation below was calculated to be 0.26 ns.

$$t_d = 1 / 2 * n_s * f_{osc}$$

where n_s is the number of stages (31) and f_{osc} is the oscillation frequency (62.2 MHz).

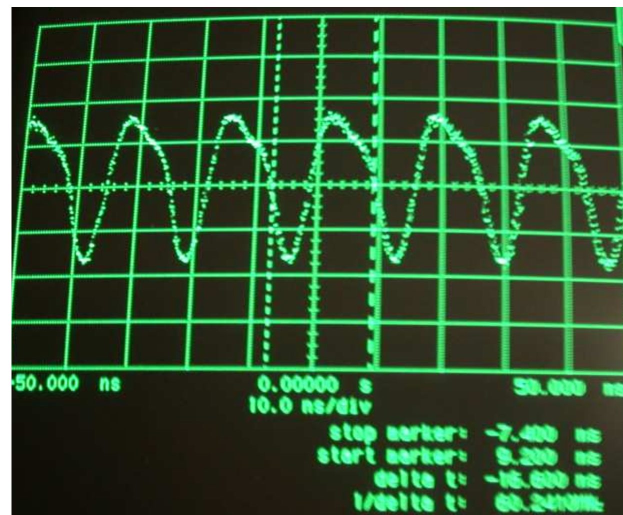


Fig. 11. Snapshot of the oscilloscope screen showing 1µm gate ring oscillator frequency

5. SPICE MODEL PARAMETER EXTRACTION FROM BSIMPro+

Parameters extracted by the MOSFET transistor modeling program (BSIMPro+) provide the foundation for circuit simulation tools (SPICE) to perform simulation on a large group of transistors in an integrated circuit [8]. Here we have provided a transistor model summary, specific to the Microlab's 0.35 μm technology.

I-V measurements were performed on NMOS and PMOS transistors with 6 different channel lengths (0.3, 0.35, 0.4, 0.5, and 1 μm) and 2 different channel widths (2.5 and 5 μm) to obtain a wide overview of device operational characteristics and meet the requirements of BSIMPro+ simulation. Id-Vg measurements were done in both the linear mode (|Vd|=50 mV) and in saturation (Vd=3 V), all under four different back-bias conditions (|Vb|=0, 1, 2, 3V). Id-Vd measurements were performed at four different gate voltages (|Vg|=1, 2, 3 and 4 V) under two back-bias conditions (|Vb|=0 and 2 V). The summary of applied measurement bias conditions is displayed in Table 5, below.

I-V data	Vgs [V]	Vds [V]	Vbs [V]
Ids - Vgs	$0 \leq Vgs \leq 4$ Vgs step = 0.1	Vds = 0.05 (in linear mode) Vds = 3 (in saturation)	$-4 \leq Vbs \leq 0$ Vbs steps = 1
Ids – Vds	$1 \leq Vgs \leq 4$ Vgs step = 1	$0 \leq Vds \leq 4$ Vds step = 0.1	Vbs = 0 Vbs = -2

Table 5 - I-V measurement bias conditions for NMOS devices
(Voltage polarity is reversed for PMOS)

Wafers were measured on an Electroglas 2001 probe station while I-V data curves were generated by an HP4062A semiconductor parametric test system. More detailed description about the measurement setup can be found in section 4.2 of this report. Test results were then converted into BSIMPro+ data format and provided the basis of the MOSFET modeling.

In Appendix C we show parametric measurement results and BSIMPro+ simulation curves for transistors of the sizes described above in this section.

Extracted SPICE parameter sets for NMOS and PMOS are presented in Appendix D.

6. PROCESS AND DEVICE PARAMETERS

Table 6 shows the summary of various measurements and test results of the CMOS170 process. Values shown in this table were extracted from measurements on L=0.3 µm, W=2.5 µm devices.

No.	Parameters	Units	NMOS	PMOS
1	Vt	V	0.53	-0.52
2	Sub Threshold Slope	mV/decade	83	91
3	K (μC_{ox})	$\mu A/V^2$	103	33
4	Delta L	µm	0.03	0.04
5	Delta W	µm	0.37	0.43
6	$\gamma 1$ (|Vsb|=1V)	$V^{1/2}$	0.08	0.09
7	$\gamma 2$ (|Vsb|=3V)	$V^{1/2}$	0.05	0.07
8	Surface dopant concentration	Atom/cm3	2.0E+16	6.0E+16
9	Substrate dopant concentration	Atom/cm3	0.5E+16	4.0E+16
10	Tox (Gate)	nm	7.5	7.5
11	Xj (S-D)	µm	0.26	0.27
12	Xw (Well depth)	µm	2.8	2.3
13	Rdiff (sheet resistance) (S-D)	Ω/square	32	87
14	Rpoly (sheet resistance) (Gate)	Ω/square	300	480
15	Rc M1-diff	Ω	1.1	0.9
16	| S-D breakdown |	V	>4.8	>6
17	S-D leakage (Vds=3.3V, Vgs=0V)	pA/µm	496	130
18	Eff. Mobility (Vbs=0V, Vgs=1V)	cm^2/V-sec	241	91
19	Ring oscillator frequency (31 stages, 1µm gate, 3.3V)	MHz	62.2	

Table 6. – Process and device parameters of CMOS 170 (W/L=2.5 µm /0.3 µm)

Methods, measurement conditions, and explanations for obtaining the parameters in Table 6

1. Threshold voltages were measured by the autoprobe Vt module using the linear extrapolation method [9].

2. Sub-threshold slope values are hand calculated based on the autoprobe DIBLE module (log (Id) vs. Vg). Using the autoprobe's DIBL module a log (I_d) vs. V_g graph was plotted when the device was operating in the linear region: $V_d = |50\text{ mV}|$. By picking a decade of Id change on the y scale the corresponding Vg difference was read from the x scale.

3. K values (gain factor in the linear region) were obtained by hand calculation based on the autoprobe Id-Vg measurements when devices were operating in the linear region. Using the Vt module on the autoprobe, I_d vs. V_g and G_m vs. V_g curves were plotted simultaneously (V_d=|50mV|). The I_d and the corresponding V_g values were picked where Gm maximized. Using the equations

$$K = \mu C_{ox}$$

and

$$I_{ds} = \mu C_{ox}\, W/L\, (V_{gs} - V_{th} - V_{ds}/2)\, V_{ds}$$

values were substituted and K was extracted.

4-5. Effective channel length and width values were obtained from the BSimPro+ simulation program based on the I-V curves measured with the autoprobe Vt and IdVd modules.

6-7. γ_1 and γ_2 (body effect parameters at different body biases) were obtained by hand calculation based on the autoprobe Vt measurements at different body biases. Using the Vt module on the autoprobe, threshold voltage values were defined under different body bias conditions ($|V_{bs}|$=0 V, 1 V, 3 V). Using

$$V_t = V_{to} + \gamma\, ((|2\Phi_B|+|Vsb|)^{1/2} - (|2\Phi_B|)^{1/2})$$

and

$$\Phi_B = kT/q \ln (N_{well}/n_i)$$

γ was extracted for $|V_{bs}|$ = 1 V, 3 V values.

8-9. Surface dopant concentration numbers are based on the SRA results, which matched the values measured on the autoprobe.

10. Gate oxide thickness was measured by the Sopra ellipsometer during processing.

11-12. Well depth and the source-drain depth data arise from the SRA graphs.

13-14. Sheet resistance values were obtained by four-point-probe measurements during processing.

15. Contact resistances were measured on designated test structures by the autoprobe CONTR_SCB module.

16. S-D breakdown measurements were taken using the autoprobe.

17. S-D leakage values were calculated based on the graphs given by autoprobe DIBLE module. Using the [log(Id) vs. Vg] graph, the value of I_d was read at $V_g = 0V$ point on the $V_{ds} = 3.3V$ curve.

18. μ_{eff} (effective mobility) data came from autoprobe measurements using the EFFMOB module. Measurement values were modified to reflect actual C_{ox} value. The originally measured value with the autoprobe's EFFMOB module was multiplied by the factor of 1.23. This ratio was found between the "ideal" C_{ox} value (for t_{ox}=80A) and the lower C_{ox} value that C-V measurement showed in inversion (for "t_{ox}" = t_{ox} + partially depleted poly gate thickness). The factor of 1.23 multiplication was applied because C_{ox} is in the nominator in the μ_{eff} equation

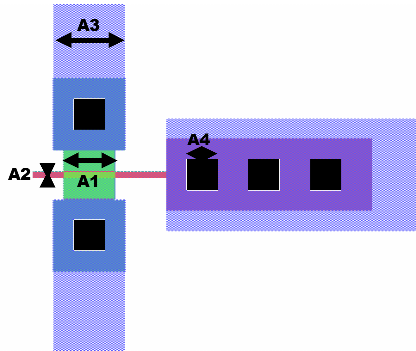
$$\mu_{eff} = g_d / C_{ox} (W/L) (V_g - V_{to})$$

19. Ring oscillator frequency was calculated using the autoprobe RingOsc module.

7. INTRODUCTION OF STANDARD DESIGN RULES IN THE TRANSISTOR DESIGN

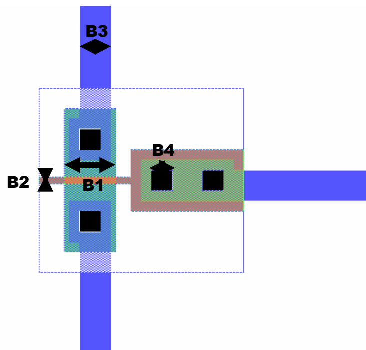
In CMOS170 baseline process we introduced additional transistors with standard, lambda scaled design rules. The comparison in V_t distribution for NMOS and PMOS transistors in column 1-3 is shown in Fig.12-14 a, b respectively.

1st column of transistors with robust design (In house design rules applied)



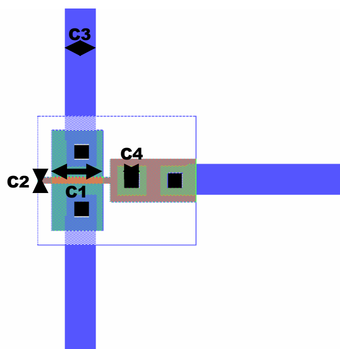
A.1. Gate length: 2.5 µm
A.2. Gate width: 0.3 µm
A.3. Metal line width: 3.5 µm
A.4. Contact hole: 1.5 µm

2nd column of transistors with λ=0.5 µm (HP design rules applied)

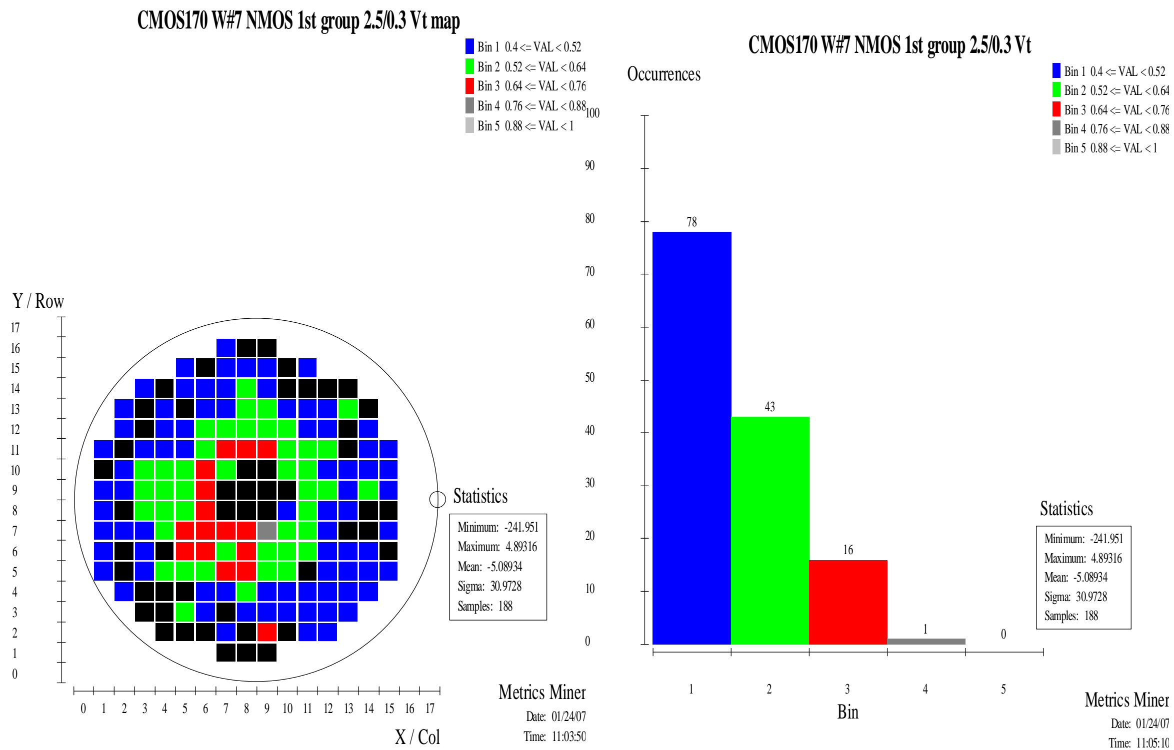


B.1. Gate length: 2.5 µm
B.2. Gate width: 0.3 µm
B.3. Metal line width: 1.5 µm
B.4. Contact hole: 1 µm

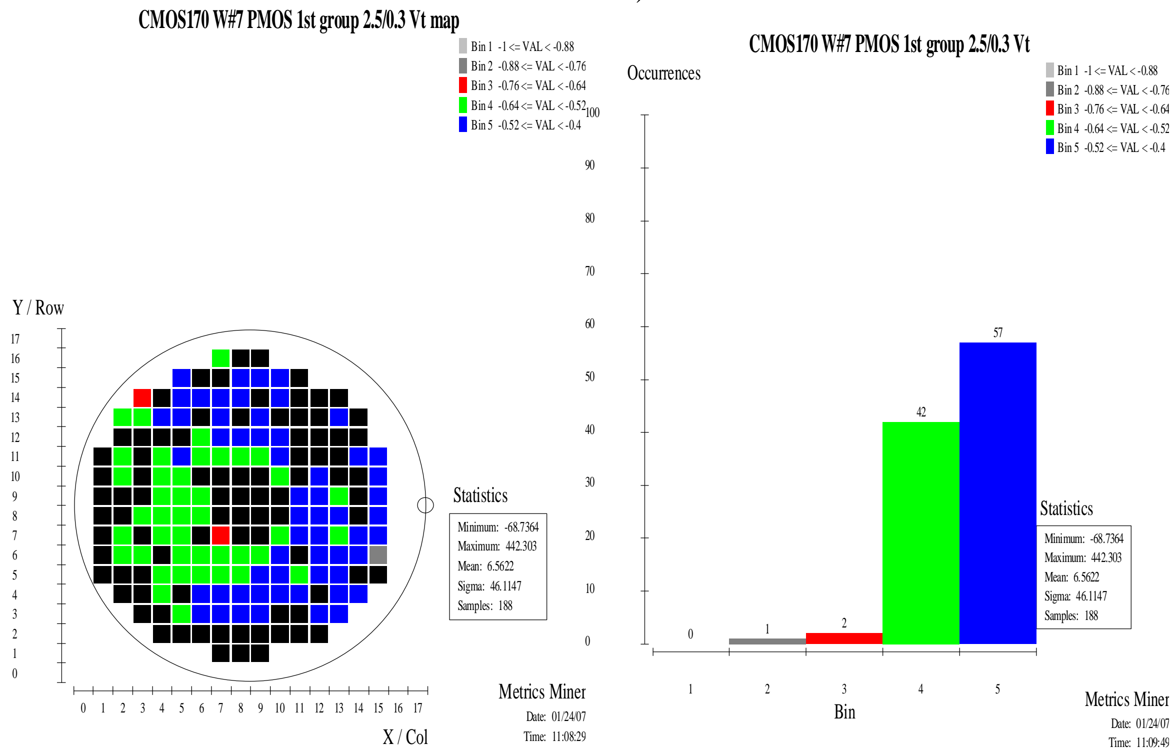
3rd column of transistors with λ=0.35 µm (HP design rules applied)



C.1. Gate length: 2.5 µm
C.2. Gate width: 0.3 µm
C.3. Metal line width: 1.5 µm
C.4. Contact hole: 0.7 µm

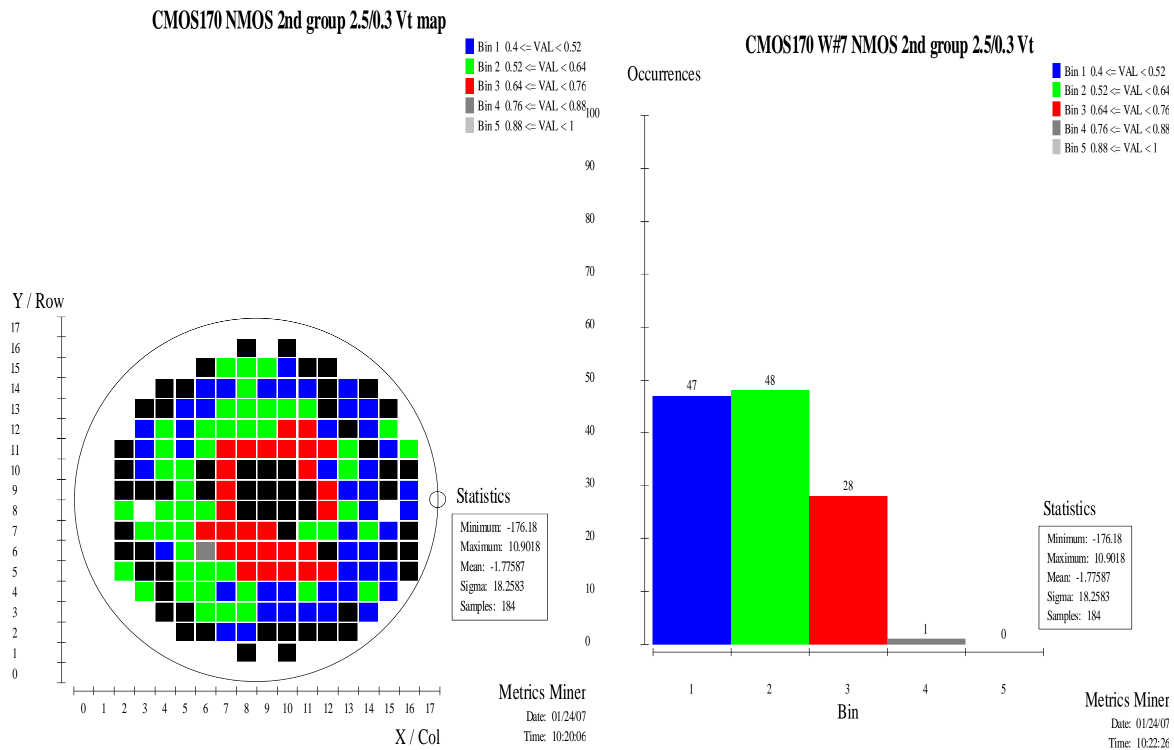


a)

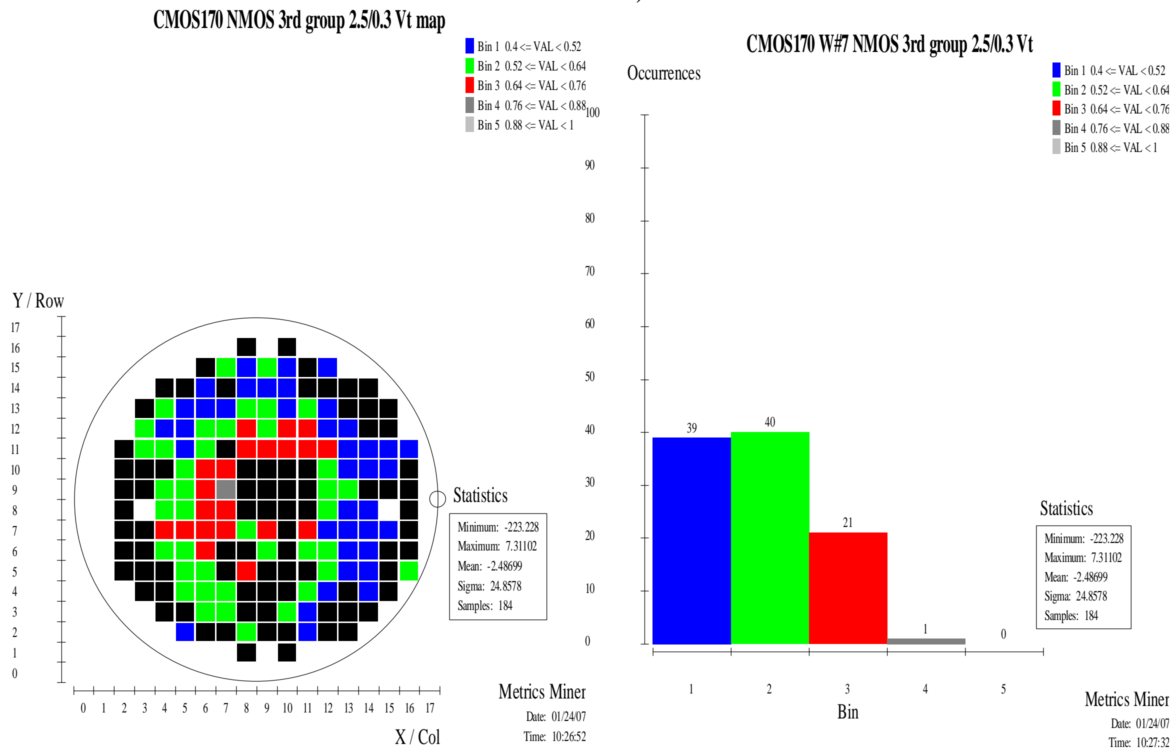


b)

Fig. 12. Vt distribution of NMOS (a) and PMOS (b) transistors with in house design rules

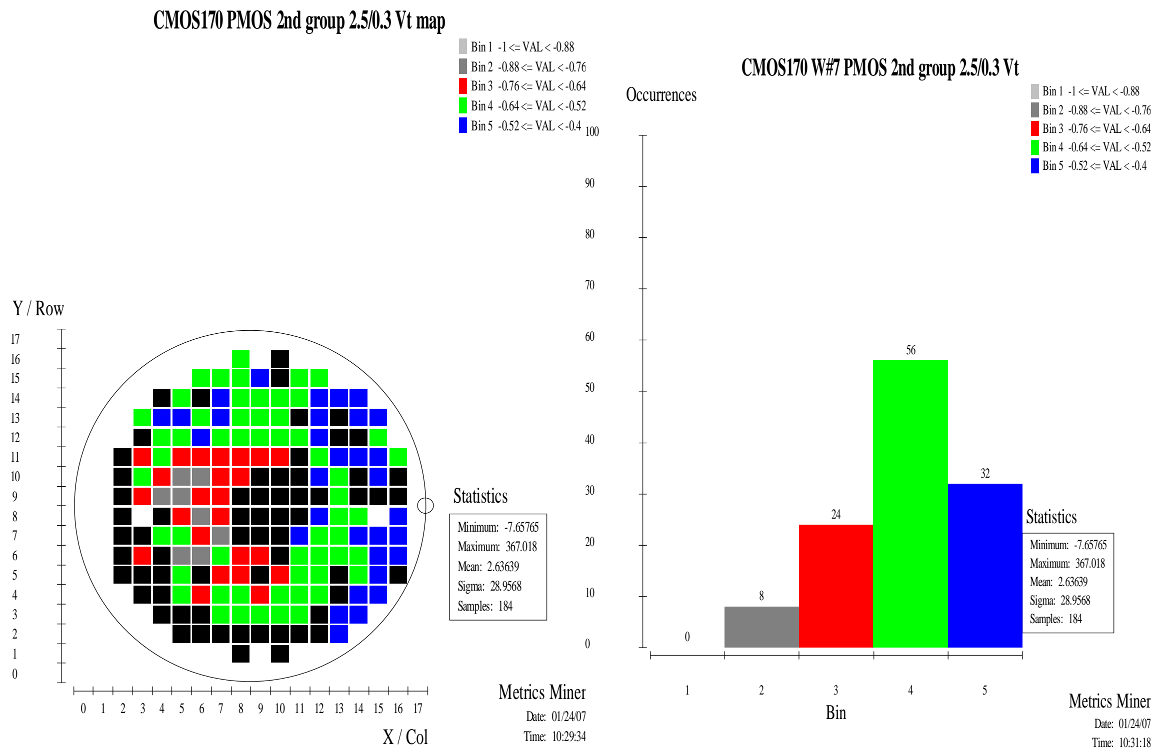


a)

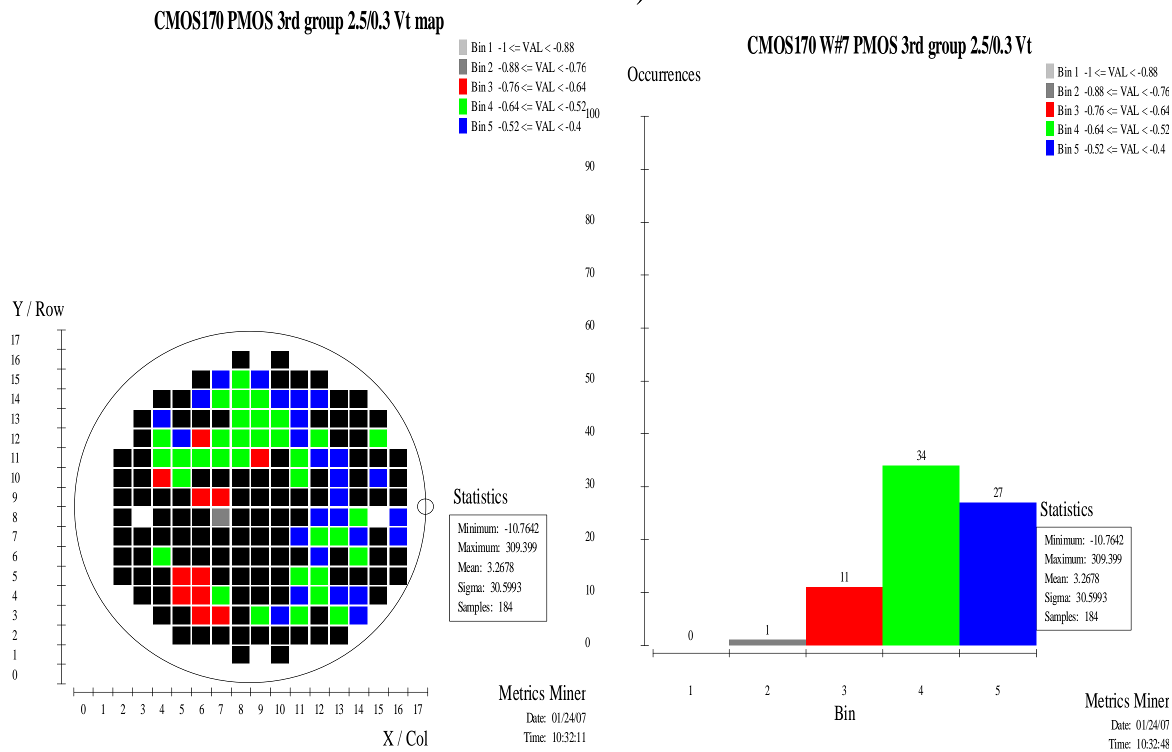


b)

Fig.13. Vt distribution of NMOS (a) and PMOS (b) transistors with λ=0.5 μm



a)



b)

Fig. 14. Vt distribution of NMOS (a) and PMOS (b) transistors with λ=0.35 μm

8. FUTURE WORK

After the release of Mix&Match process on ASML/GCA6 steppers, the baseline team decided to apply Mix&Match scheme as well as shallow trench isolation technology (STI) to the next version of baseline run (CMOS180).

Up until now, local oxidation of silicon (LOCOS) has provided the isolation of NMOS and PMOS transistors for the 0.35 µm process. We are planning on developing the STI module on the new 0.35 µm process.

Also, we would like to improve the back-end process by introducing a multi-stepped metal deposition module. A better metal step coverage will allow the reduction of contact/via hole sizes.

9. REFERENCES

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Biographies

Anita Pongracz earned his M.S. degree in Engineering Physics in 2004 from the Technical University of Budapest, Hungary. Since August 2006 Anita has been working as a baseline process engineer in the UC Berkeley Microfabrication Laboratory. Her main responsibilities are to design, fabricate, test, and evaluate CMOS test devices.

Gyorgy Vida received his M.S. degree in Engineering Physics in 2000 from Technical University of Budapest, Hungary. He was working as a baseline process engineer in the UC Berkeley Microfabrication Laboratory between September 2005 and August 2006.

Appendix A

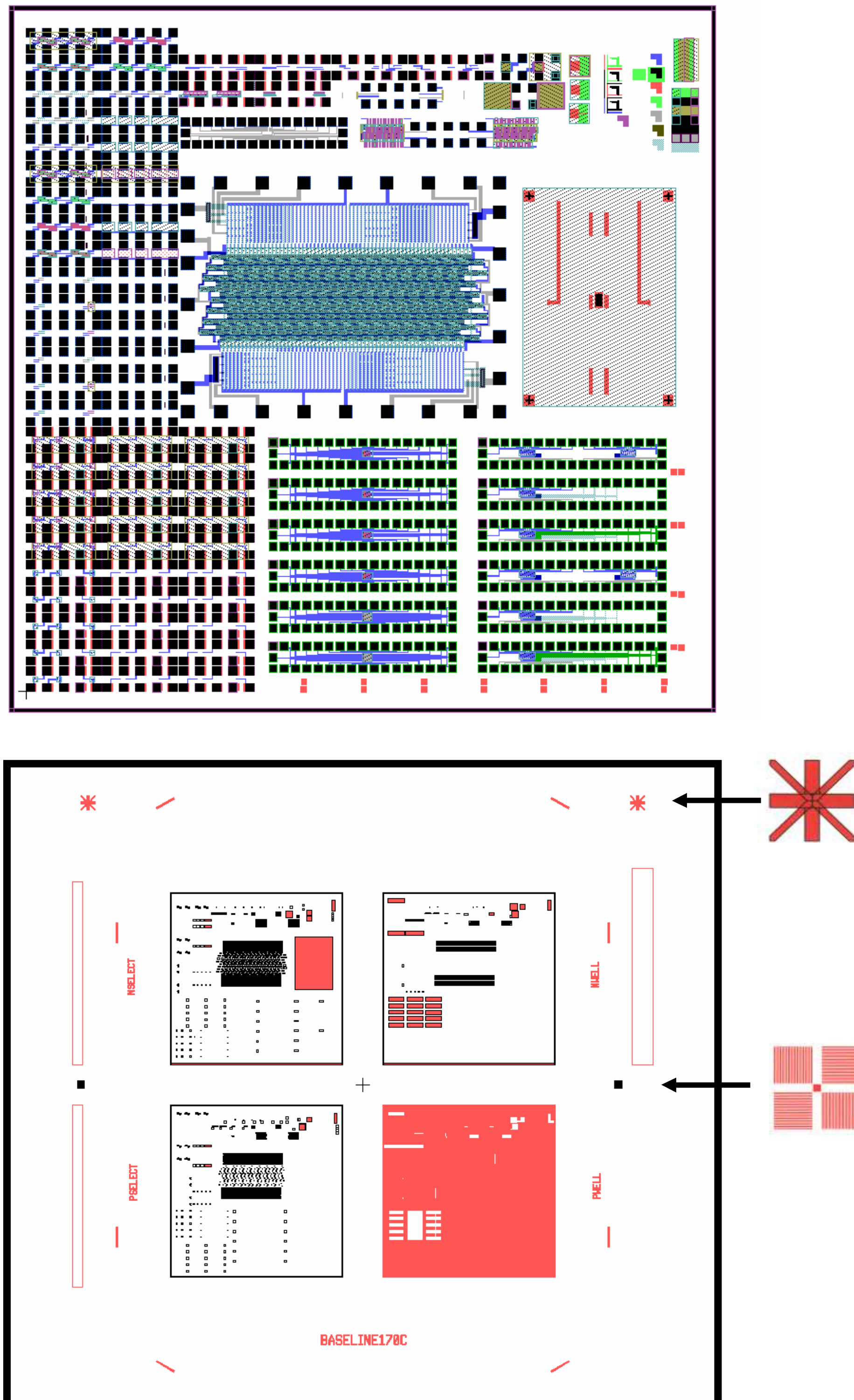

Fig. 15. Baseline chip layout (top) and four mask layers on one ASML reticle, scaled by ¼ (bottom)

Appendix B

Microlab CMOS Process Flow

Version 8.2 (2006)

0.35 µm, twin-well, 150 mm, double poly-Si, metal

(6" process)

Note 1.: This 0.35 µm version of baseline process flow yielded 0.3 µm working transistors

Note 2.: Vt implantation split: 4e12/cm^2 for W#1-5 and 3e12/cm^2 for W#6-10

0.0 Starting Wafers (10): 36-63 ohm-cm, p-type, <100>, 6"

2 monitor wafers (PCH, NCH)

1.0 Initial Oxidation: target = 25 (+/- 5%) nm

Include 2 dummies for PM etch characterization.

1.1 TCA clean furnace tube (tystar1)

Note: Tystar 2, 2TLCA wasn't available

1.2 Standard clean wafers in sink6:

25/1 HF dip until dewet, spin-dry.

1.3 Dry oxidation at 950 C (1GATEOXA):

30 min. dry O2

20 min. dry N2

Measure oxide thickness 19,5 nm

2.0 Zero Layer Photo

Standard DUV lithography process:

HMDS (program 1 on svgcoat6), coat (program 2 on svgcoat6),

RPM=1480, UV210-0.6), soft bake (program 1, 130 C proximity),

Expose (ASML, zero marks mask, 30 mJ/cm2),

Post Exposure Bake (program 1, 130 C on svgdev6) ,

Develop (program 1 on svgdev6).

Hard bake in oven

3.0 Etch zero layer into the substrate: target = 120 nm Si etch

---

3.1. Scribe numbers into the photoresist, numbers will be etched into Si during the following etch

---

3.2. Etch through oxide in Centura MxP+ MXP_OXSP_ETCH

Note: 12s as endpoint detection didn't work

3.3. Etch marks into Si in Centura DPS_SI_ETCH

Check actual etch rate, adjust time.

Note: DPS_SI_ETCH 21 s

Note: Other option lam5 recipe 5003

3.4. Ash photoresist in Matrix

2 min O_2 ash

3.5. Measure the depth of the alignment marks using Asiq.

4.0 Pad Oxidation/Nitride Deposition:

target = 25 nm SiO2 + 220 nm Si3N4

4.1 TCA clean furnace tube (tystar1).

Note: Tystar2 TLC wasn't available

4.2 Standard clean wafers in sink8 + sink6

(NON-MOS and MOS Piranha, dip into HF 25:1 until dewet).

Include NCH, PCH control wafers.

4.3 Dry oxidation at 1000 C (1GATEOXA):

21 min. dry O2

15 minutes dry N2 anneal.

Measure the oxide thickness on PCH and NCH.

4.4 Deposit 220 nm of Si3N4 immediately (9SNITA):

Note: deposition time = 56 min., temp= 800 C., dep. rate = 40A/min

Measure nitride thickness. (Nanospec).

5.0 N-Well Photo:

Standard DUV lithography process.

Mask: N-well (dark field), 25mJ

Standard oven bake (30 min., 120 C)

6.0 Nitride Etch:

Centura MxP+ recipe: MXP_NITRIDE_OE

CH3F=20, Ar=50, O2=7, p=50mT, pw=450W

Monitor endpoint

Note: Measure nitride thickness on every wafer. Make sure to have sufficient blocking for the following implant.

7.0 N-Well Implant: Include PCH.

PCH: phosphorus, 1E13/cm2, 150 KeV.

8.0 Nitride removal:

8.1. Remove PR in Matrix. Clean wafers in sink8 MEMS piranha

8.2. Etch nitride in fresh 160 C phosphoric acid in sink7 (~4 hours)

8.3. Etch pad oxide in 5:1 BHF at sink8 until dewet. Include NCH, PCH.

9.0 Pad Oxidation/Nitride Deposition:

Target = 25 nm SiO2 + 220 nm Si3N4

9.1 TLC clean furnace tube (tystar2).

9.2 Standard clean wafers in sink8 + sink6 (NON-MOS and MOS Piranha, 25:1 HF dip until dewet). Include NCH, PCH.

9.3 Dry oxidation at 1000 C (2DRYOXA):

21 min. dry O2

15 minutes dry N2 anneal.

Measure the oxide thickness on NCH and PCH.

9.4 Deposit 220 nm of Si3N4 immediately (9SNITA):

Approx. time = 55 min., temp = 800 C.

10.0 P-Well Photo:

Standard DUV lithography process. Mask: PWELL (inverse of NWELL), 19 mJ

Oven bake (60 min., 120 C)

11.0 Nitride Etch:

Centura MxP+ recipe: MXP_NITRIDE_OE

CH3F=20, Ar=50, O2=7, p=50mT, pw=450W

Check the etch rate.

Monitor endpoint

Note: Measure nitride thickness on every wafer. Make sure to have sufficient blocking for the following implant.

12.0 P-Well implant:

Boron, 5E12, 60KeV

Include NCH.

13.0 Nitride removal:

13.1. Remove PR in Matrix. Clean wafers in sink8 MEMS piranha

---

13.2. Etch nitride in fresh 160 C phosphoric acid in sink7 (~4 hours)

13.3. Etch pad oxide in 5:1 BHF at sink8 until dewet. Include NCH, PCH.

14.0 Well Drive-In:

14.1 TLC clean furnace tube (tystar2).

14.2 Standard clean wafers in sink8 + sink6 (NON-MOS and MOS).

Include NCH, PCH control wafers.

14.3 Well drive in at 1100 C (2WELLDR):

60 min. temperature ramp from 750 C to 1100 C

150 min. dry O2

15 min. N2

Measure oxide thickness on two wafers.

14.4 Strip oxide in 5:1 BHF at sink8 until dewet.

Note: approx. 2 min

Measure Rs on PCH, NCH

15.0 Pad Oxidation/Nitride Deposition:

Target = 25 nm SiO2 + 220 nm Si3N4

15.1 TLC clean furnace tube (tystar2).

15.2 Standard clean wafers in sink8 + sink6 (NON-MOS, MOS,Piranha + 25:1 HFdip until dewet.) Include NCH, PCH + 2 dummies.

15.3 Dry oxidation at 1000 C (2DRYOXA):

21 min. dry O2

15 minutes dry N2 anneal.

Measure the oxide thickness on NCH.

15.4 Deposit 220 nm of Si3N4 immediately (9SNITA):

Approx. time = 55 min., temp = 800 C.

Only include PCH.

Measure nitride thickness on PCH.

16.0 Active Area Photo:

Std. DUV litho process. Mask ACTIVE, 20 mJ

UVBAKE program U

17.0 Nitride Etch:

Plasma etch nitride in Centura MxP+.   Recipe: MXP_NITRIDE_OE

Monitor endpoint, allow some overetch

Measure Tox on each work wafer (2 points measurement).

18.0 P-Well Field Implant Photo

18.1 Ash the photoresist in Matrix

18.2 Std. clean wafers in sink8 Piranha

18.3 Std. DUV process. Mask PFIELD (inverse of NWELL+ACT)

Oven bake 120 C, 1hrs.

19.0 P-Well Field Ion Implant

Boron, 2E13, 80KeV

20.0 Locos Oxidation: target = 550 nm

20.1 TLC clean furnace tube (tystar2).

20.2 Remove PR in O2 plasma (matrix).

20.3 Standard clean wafers in sink8 MEMS & sink6 MOS piranha,

25:1 HF dip for 5-10 sec.)

Include NCH, PCH.

20.4 Wet oxidation at 1000 C (2WETOXA):

2 hrs. wet O2

20 min. N2 anneal

Measure Tox on 3 work wafers and NCH, PCH.

21.0 Nitride Removal, Pad Oxide Removal.

Include PCH (NCH: no nitride, but LOCOS).

21.1 Dip in 10:1 HF for 60 sec at sink6 to remove thin oxide on top of Si3N4.

21.2 Etch nitride off in fresh phosphoric acid at 160 C. at sink7 ~3-4 hrs.

Measure pad oxide thickness to verify successful nitride etch.

21.3 Etch pad oxide in 5:1 BHF until PCH control wafer dewet at sink6

21.4 LOCOS Oxide wet etch on NCH at sink7 in fresh 5:1 BHF until dewet

---

22.0 Sacrificial oxidation. (Target = 250A)

22.1 TLC clean furnace tube (tystar2).

22.2 Standard clean wafers in sink6 MOS piranha, 25:1 HF dip for 5-10 sec)

Include NCH, PCH.

22.3 Dry oxidation at 900 C (2DRYOXA):

40 min. dry O2

no N2 anneal (set to 1 sec)

Measure the oxide thickness on NCH.

23.0 Screen oxidation. Include NCH, PCH

23.1 TLC clean furnace tube (tystar2).

23.2 Standard clean wafers sink6 MOS piranha, dip in 25:1 HF until NCH, PCH dewet to remove sacr. oxide on active area (Keep in mind you have LOCOS!)

23.3 Sacrificial Oxide: target = 25 (+/- 2) nm

Dry oxidation at 900 C (2DRYOXA):

40 minutes dry O2

15 minutes N2 anneal

Measure Tox on PCH.

24.0 NMOS Vt implant photo

Std. DUV litho. Mask PWELL. UVBAKE (pr. J)

25.0 NMOS Vt implant

Split: BF2, 4E12, 50KeV, w# 1, 2, 3, 4, 5

BF2, 3E12, 50KeV, w# 6, 7, 8, 9, 10, NCH

26.0 PMOS Vt implant photo

26.1 Remove PR in matrix,

26.2 sink8 MEMS piranha clean

26.3 Std. DUV litho. Mask NWELL. UVBAKE (pr. J)

27.0 PMOS Vt implant: phosphorus, , 2E12, 30 KeV w#1-10, PCH

28.0 Gate Oxidation/Poly-Si Deposition:

Target = 8 nm SiO2 + 250 nm undoped poly-Si

28.1 TCA clean furnace tube (tystar1).

Reserve poly-Si deposition tube (tystar10).

28.2 Remove PR in Matrix.

28.3 Standard clean wafers sink8 MEMS, sink6 MOS piranha,

25:1 HF dip until dewet on PCH, NCH approx. 2-3 min.

Include Tox (prime P<100>), Tpoly1, Tpoly2 monitoring wafers.

28.4 Dry oxidation in Tystar1 recipe 1THIN-OX

30 min. dry O2 @ 850C

30 min. N2 anneal @ 900 C

Include PCH, NCH, Tox, Tpoly1, Tpoly2 and 3 test dummies.

Note: ALMACK step 25 in furnace process unless the

pre-oxidation furnace temp. is 450C

28.5 Immediately after oxidation deposit 250 nm of undoped

poly-Si (10suplya).

approx. dep. rate= 85 A/min., temp= 610 C

Note: deposition time was 24 min

Include Tpoly1, Tpoly2 and the 3 test dummies.

28.6 Measurements

a) Measure oxide thickness on Tox. (Rudolph and Sopra ell.)

b) Measure Dit and Qox on Tox. (SCA)

c) Measure poly thickness on Tpoly1. (Nanoduv)

d) Strip oxide from NCH, PCH, measure the sheet resisitance.

29.0 Gate Definition:

Standard DUV lithography process with ARC-600 antireflective coating.

29.1 BARC coating

Pour the room temperature BARC manually on wafer (program 6 on svgcoat6), RPM=0 for 10s, RPM=500 for 3s, RPM=3750 for 30s, yielded 60 nm thick BARC layer

Bake the wafers at 205 C for 60s (program 1 on svgdev6 hard bake plate)

Standard coating without HMDS (program 2 on svgcoat6),

RPM=1480, UV210-0.6), soft bake (program 1, 130 C proximity),

---

29.2 Expose (ASML, POLY mask, 21 mJ/cm2),

Make a matrix measurement, use best energy and focus

29.3 Post Exposure Bake (program 1, 130 C on svgdev6),

Develop (program 1 on svgdev6).

29.4 UVBAKE pr. U

30.0 Plasma etch poly-Si

30.1 Etch poly in Lam5. Recipe: 5003 with modified over etch step:

Pwr:250 W top, 125W bottom; 200sccm HBr, 5sccm O2,

0sccm He. Selectivity ~60:1 poly to oxide.

Apply ~50% over etch after endpoint in main etch.

30.2 Remove PR (matrix),

30.3 Clean wafers at sink8 MEMS piranha.

30.4 Measure channel length with SEM.

31.0 P-type LDD implant photo

Std. DUV lithography. Mask PSELECT, UVBAKE pr. J

32.0 P-type LDD implant. Include PCH, Tpoly1.

BF2, 5e13, 10KeV +7 deg. tilt @ 0 orientation

BF2, 5e13, 10KeV -7 deg. tilt @ 180 orientation

33.0 N-type LDD implant photo

33.1 Remove PR (matrix),

33.2 Clean wafers at sink8 MEMS piranha

33.3 Std. DUV litho. Mask NSELECT. UVBAKE pr. J

34.0 N-type LDD implant. Include NCH, Tpoly2.

As, 5e13, 30KeV +7 deg. tilt @ 0 orientation

As, 5e13, 30KeV -7 deg. tilt @ 180 orientation

35.0 LDD Spacer deposition (spacer width target= 3000 A)

35.1 Remove PR in matrix.

35.2 Standard clean wafers at sink8 MEMS, sink6 MOS Piranha

Include 6 dummies for oxide etch test (3) and SEM test (3).

Reserve and TLC clean tystar2.

35.3 TEOS deposition in P-5000 target=4000 A

Check dep. rate (~ 80 A/min.)

Note: Recipe: A-PE-USG-0.5, deposition time:47 s

35.4 TEOS annealing 900 C, 30 min. (2HIN2ANA)

35.5 Measure TEOS thickness on active area.

36.0 LDD Spacer Formation

36.1 Plasma etch TEOS in Centura MxP+

Verify actual etch rate (~3000 A/min)

Recipe MXP_OXSP_ETCH_EP

Manual endpoint when signal drops

Note: Verify the completion of the etch by measuring 0 A oxide on the ACT measurement area

36.2 Measure spacer with CDSEM.

37.0 P+ Gate & S/D Photo:

37.1. Standard DUV Lithography process.
Mask 2nd modified P+ S/D,

37.2 UVBAKE (pr. J)

38.0 P+ Gate & S/D Implant. Include PCH, Tpoly1.
Boron, 3E15, 20 keV

39.0 N+ Gate & S/D Photo:

39.1 Remove PR in Matrix.

39.2 Std. Clean wafers in sink8 MEMS piranha.

39.3 Standard DUV Lithography process.
Mask 2nd modified N+ S/D,

39.4. UVBAKE (pr. J)

40.0 N+ Gate & S/D Implant. Include NCH and Tpoly2.
Phosphorus, 3E15, 40 KeV

41.0 Back Side Etch:

41.1 Remove PR in O2 plasma (matrix)

41.2 a) Piranha clean wafers in sink8 MEMS side (no dip).
b) dehydrate wafers in oven at 120 C for 30 min.

41.3 a) Coat wafers front side at svgcoat6,
b) UVBAKE

41.4 a) Dip off native oxide in 5:1 BHF in sink8

b) Etch poly-Si in lam5, recipe 5003, no over etch step

Etch to endpoint plus 10 sec.

c) Final dip in 5:1 BHF until dewet (~1min) at sink 8

Incl. NCH, PCH, TPoly1, Tpoly2 to remove

native oxide (~20 sec)

42.0 Gate & S/D annealing. Include all test wafers (NCH, PCH, Tpoly1, Tpoly2).

42.1 PR ashing in Matrix.

42.2 Standard clean wafers in sink8 MEMS and sink6 MOS Pirsanha, no dip

---

42.3 RTA in Heatpulse3, recipe 1050RTA.RCP

450 C 30sec, 900 C 10sec, 1050 C 5 sec in N2

42.4 Check Rs on test wafers with 4-point-probe:

for gate < 250 ohm/sq, for S/D <100.

43.0 Silicidation

43.1 Sputter etch in Novellus (ETCHSTD 1 min) or 25:1 HF dip 30 sec

---

43.2 Ti deposition in Novellus (Ti300STD). Measure Rs.

43.3 RTA annealing in Heatpulse3, Recipe 650RTA6.RCP

450 C 20sec, 650 C 15 sec

Note: Take care of the 80 C scale shift 400-1100 C

43.4 Etch excess Ti and TiN in fresh piranha (120 C, 45 sec.) in Sink7.

Measure field oxide thickness on a LOCOS area to verify the completion of the etch

---

44.0 PSG deposition and densification: target 700 nm

44.1 Clean wafers in sink6 Piranha, NO HF dip!

Include PCH, Si and TiSi test wafers

44.2 Deposit 700 nm PSG in tystar11 (11SDLTOA)

Deposition time is approx.: 47 min., 450 C

44.3 Backside etch PSG.

a) Coat wafers front side at svgcoat6,

b) UVBAKE pr. J

c) Dip off native oxide in 5:1 BHF in sink8

d) Matrix PR removal

e) Clean at Sink8 MEMS & Sink6 MOS Piranha

44.4 Densify PSG in RTA (heatpulse3). Recipe 900RTA6.RCP

450 C, 30 sec, 900 C, 10 sec in N2, silicide chamber.

44.5 Measure PSG thickness on PCH

Note: Measure LOCOS+PSG thickness on a LOCOS measurement area

Remove oxide from PCH and measure Rs

45.0 Contact Photo:

Standard DUV lithography process. Use ARC-600.

CONT mask. Over-expose contact (30-40 mJ/cm2)

Second PM mark should be exposed, before developing

UVBAKE pr. U

46.0 Contact plasma etch in Applied Centura MxP+.

Recipe: MXP_OXSP_ETCH_EP

overetch: 15 sec after endpoint signal drops

Measure R with manual probe on Poly and S/D area on each wafer. R~10-100Ohm Check contact holes structure.

47.0 Metallization: target= 600 nm Al

47.1 Remove PR in O2 plasma (Matrix).

47.2 Standard clean wafers in sink8 MEMS, no HF dip, sink6 MOS piranha or Novellus sputter etch to remove native oxide recipe: ETCHSTD 60s etch

Note: Do not use HF after silicidation

47.3 Sputter Al/2%Si in Novellus:AL7STD,

47.4. Measure Rs at 4-point-probe station

48.0 Metal1 Photo:

Standard DUV litho. process, ARC-600.

Mask METAL1, 21 mJ

UVBAKE pr. U

49.0 Plasma etch metal1 in lam3.

Standard recipe: approx. time: 1min 25 sec, overetch= 50 %

Check R on Fieldox, R=OVLD should be on LOCOS area

50.0 Sintering

50.1 Remove PR in matrix.

50.2 Rinse & spin dry at sink8.

Note:No Piranha or HF

50.3 Sinter in Tystar18 H2SINT4A.018 recipe 20 min @ 400 C

51.0 Testing

Id-Vd, Vt, EffMob, Saturated Current, Body Effect measurements

---

52.0 Dielectric deposition/planarization

52.1. TEOS deposition in P-5000

Target = 2 μm , Recipe: AP-USG2

Measure total oxide thickness before and after deposition; calculate dielectric thickness

---

52.2 Planarization with Chemical Mechanical Polishing, recipe:oxide_st.00

Target = 1 μm removal

Measure oxide thickness

52.3 Rinse wafer at sink8 in DI water

Dehydrate wafer in oven at 120 C for 30 min

53.0 Via 1 Photo

Standard DUV litho. process,

Mask VIA1, 37 mJ

UVBAKE pr. U

54.0 Via 1 Etch in Centura MxP+ recipe:MXP_OXSP_ET_EP

Check resistivity on test area

Note: no endpoint, use patterned test wafer to verify the etch rate

---

55.0 Metal 2 deposition

55.1 Ash the PR in Matrix

55.2 Sputter etch in Novellus, recipe ETCHSTD for 1 min

Al deposition in Novellus, target = 900 nm

Measure Rs of Al film

Note: reserve CPA

56.0 Metal 2 photo

56.1 Opening 4 dies for PM marks

Std. DUV litho. Process

Mask: blank

UVBAKE pr. U

56.2 Etch the metal from the opened areas in Lam3

Note: use pure Al dummies to stabilize the plasma

56.3 Ash the PR in MATRIX

Use SVC-14 at 80 C for 10 min to remove all remained photoresist particles

---

56.4 Standard DUV litho. process, ARC-600.

Mask METAL2, 26 mJ

UVBAKE pr. U

57.0 Plasma etch metal2 in lam3.

57.1 Standard recipe: approx. time: 1min 25 sec, overetch= 50 %

Check R on Fieldox, R=OVLD should be on LOCOS area

Note: Take care of photoresist thickness

57.2 Ash photoresist in Matrix

58.0 Testing with Autoprober

Metal1 and Metal2 contact resistors and chains

Ring Oscillators

59.0 Dielectric deposition/planarization

59.1. TEOS deposition in P-5000

Target = 2 μm , Recipe: AP-USG2

Measure total oxide thickness before and after deposition; calculate dielectric thickness

---

59.2 Planarization with Chemical Mechanical Polishing, recipe:oxide_st.00

Target = 1 μm removal

Measure oxide thickness

59.3 Rinse wafer at sink8 in DI water

Dehydrate wafer in oven at 120 C for 30 min

60.0 Via 2 Photo

Standard DUV litho. process,

Mask VIA1, 37 mJ

UVBAKE pr. U

61.0 Via 2 Etch in Centura MxP+ recipe:MXP_OXSP_ET_EP

Check resistivity on test area

Note: no endpoint, use patterned test wafer to verify the etch rate

---

62.0 Metal 3 deposition

62.1 Ash the PR in Matrix

62.2 Sputter etch in Novellus, recipe ETCHSTD for 1 min

Al deposition in Novellus, target = 900 nm

Measure Rs of Al film

Note: reserve CPA

63.0 Metal 3 photo

63.1 Opening 4 dies for PM marks

Std. DUV litho. Process

Mask: blank

UVBAKE pr. U

63.2 Etch the metal from the opened areas in Lam3

Note: use pure Al dummies to stabilize the plasma

63.3 Ash the PR in MATRIX

Use SVC-14 at 80 C for 10 min to remove all remained photoresist particles

---

63.4 Standard DUV litho. process, ARC-600.

Mask METAL2, 26 mJ

UVBAKE pr. U

64.0 Plasma etch metal3 in lam3.

64.1 Standard recipe: approx. time: 1min 25 sec, overetch= 50 %

Check R on Fieldox, R=OVLD should be on LOCOS area

Note: Take care of photoresist thickness

64.2 Ash photoresist in Matrix

65.0 Testing

Metal 2 and Metal 3 contact resistance and contact chains

Appendix C

BSIMPro+ simulation results

Using the BSIMPro+ MOSFET modeling tool we were able to create a general transistor model based on our measurement results for both NMOS and PMOS devices that provide a very good fit for all the studied transistors with the investigated gate length and width. In the following figures (Fig. 13 – 22), we demonstrate the parametric measurement results and the BSIMPro+ simulation curves displayed on top of each other. Dotted lines represent the measurement data points, while the continuous curves show the simulation results. Six graphs are plotted for each transistor size describing

(a) Id–Vgs at |Vds|=50mV for |Vbs|=0 to 3V
(b) Id-Vds at Vbs=0v for |Vgs|=1 to 4V
(c) Id–Vgs at |Vds|=50mV for |Vbs|=0 to 3V; plotting Id on logarithmic scale
(d) Gds-Vds at Vbs=0V for |Vgs|=1 to 4V
(e) Gm-Vgs at |Vds|=50mV for |Vbs|=0 to 3V
(f) Rout-Vds at Vbs=0V for |Vgs|=1 to 4V.

NMOS measured and simulated data

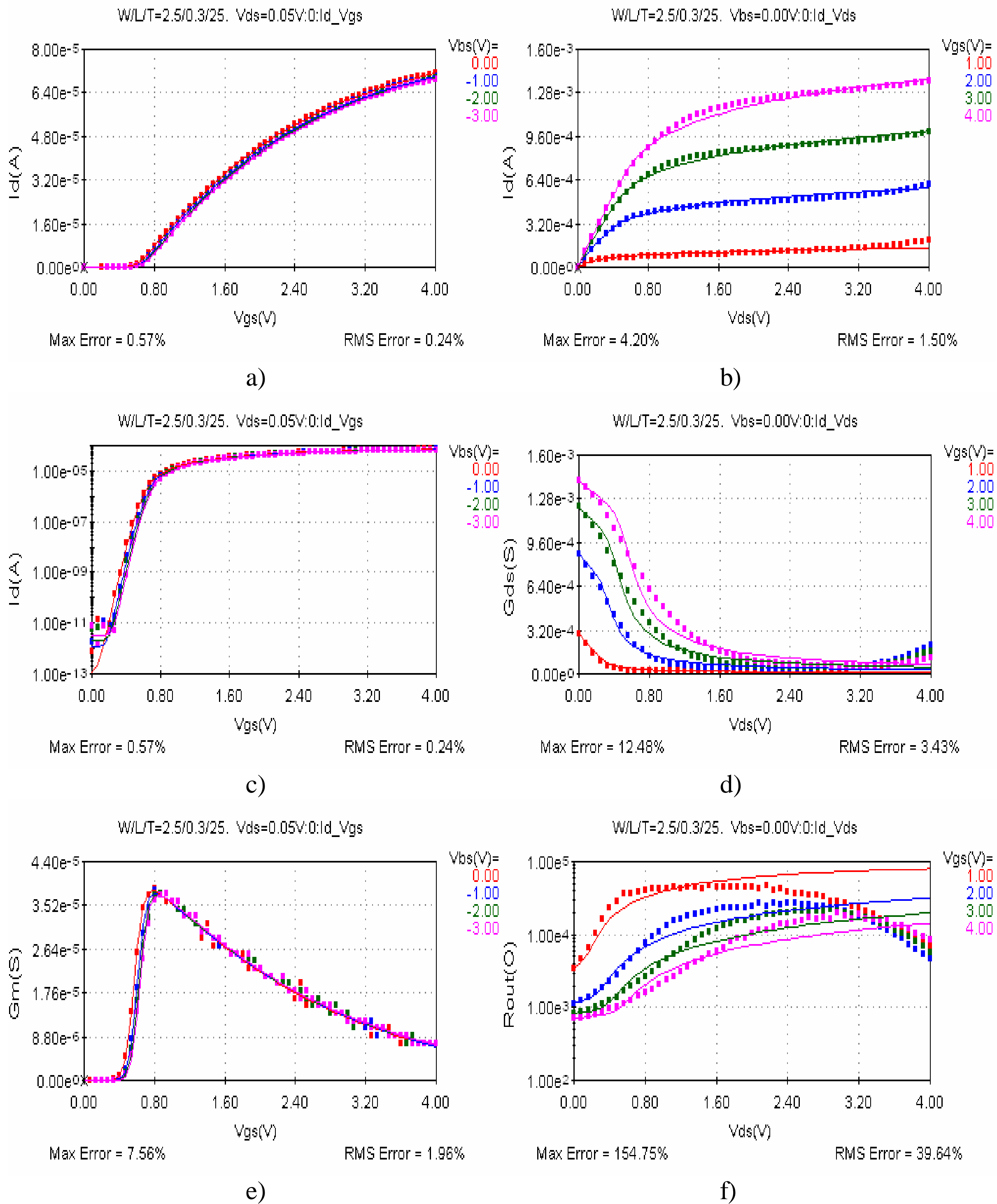

Fig. 16. L=0.3 μm W=2.5 μm NMOS

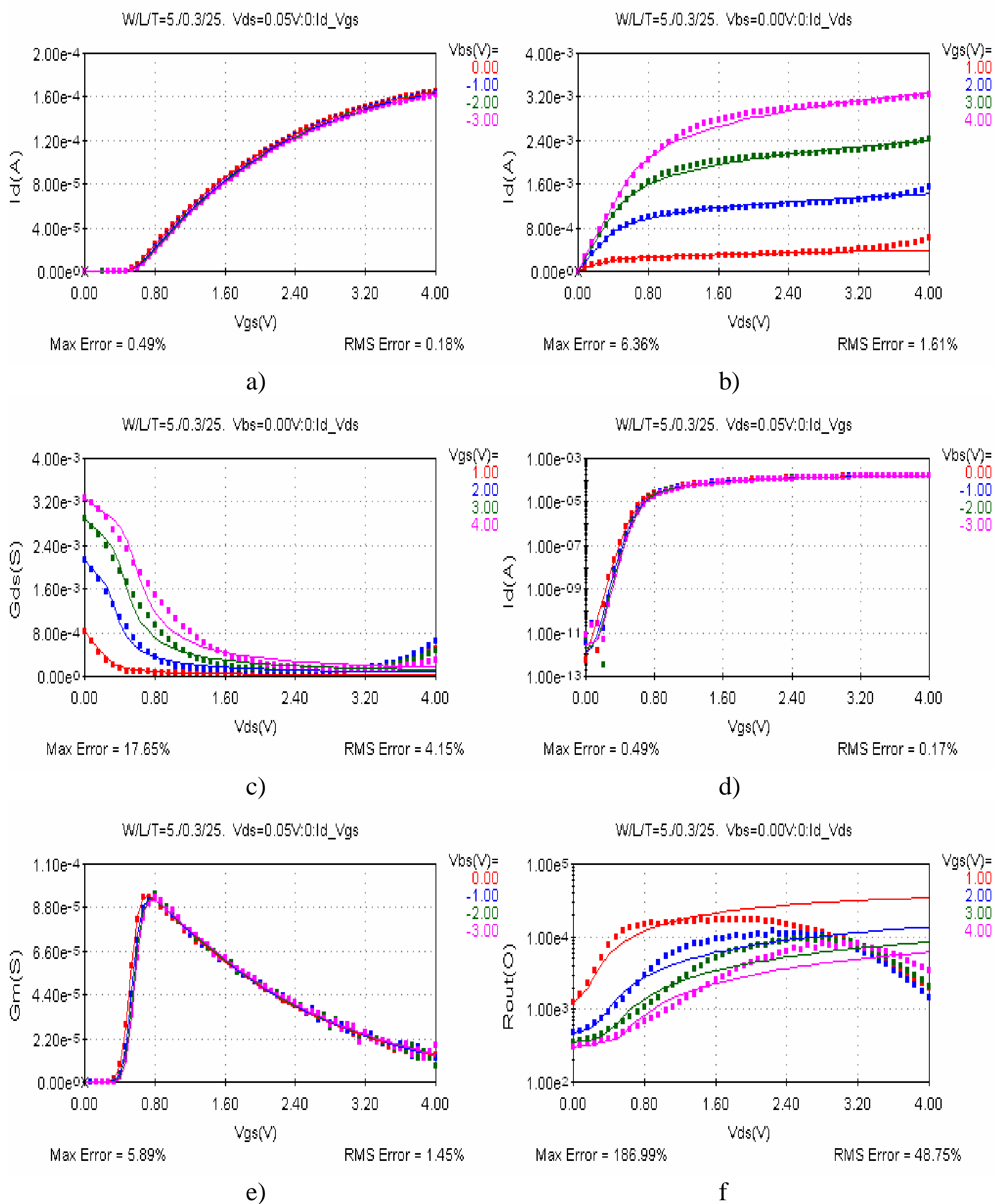

Fig. 17. L=0.3 μm W=5 μm NMOS

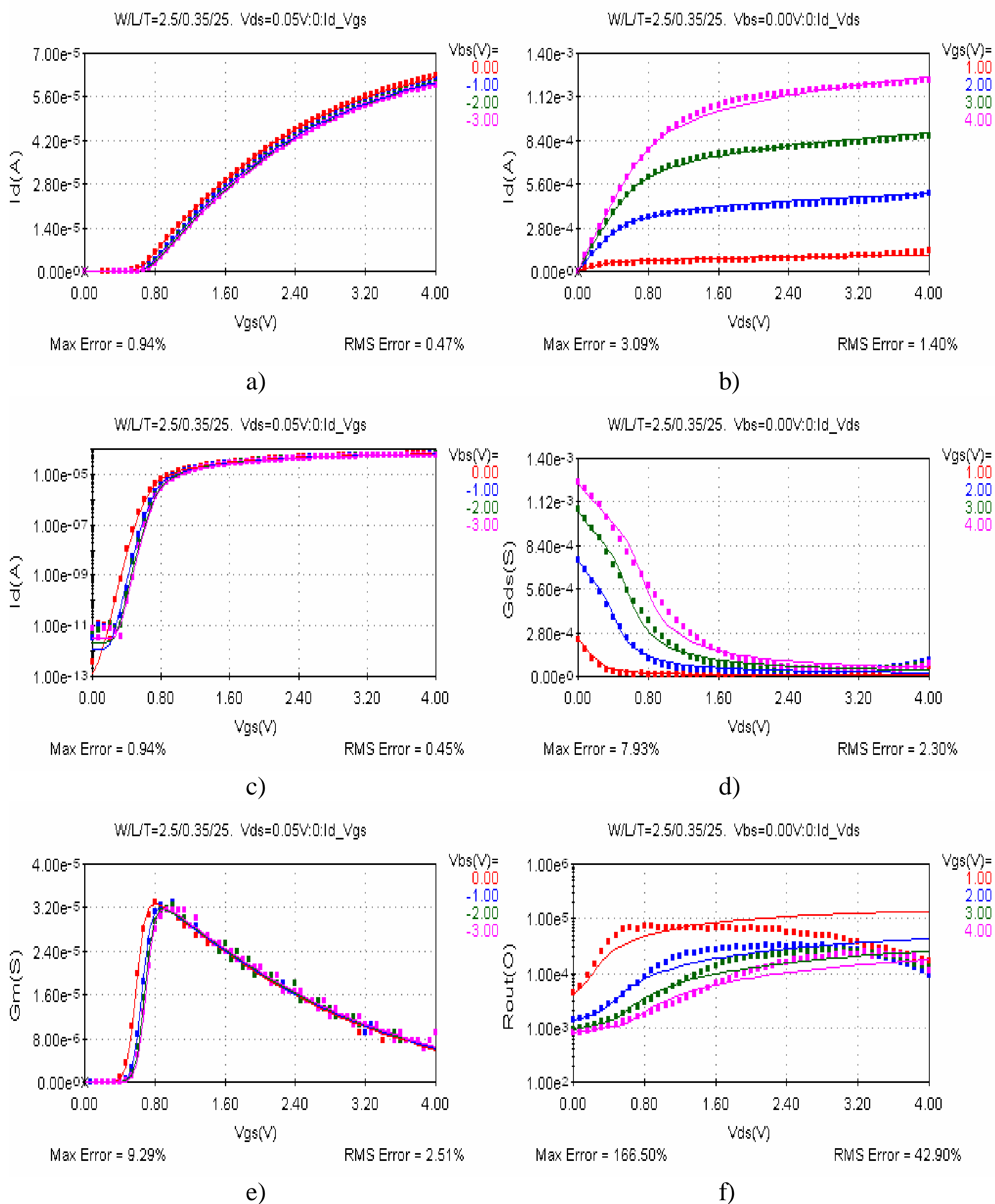

Fig. 18. L=0.35 μm W=2.5 μm NMOS

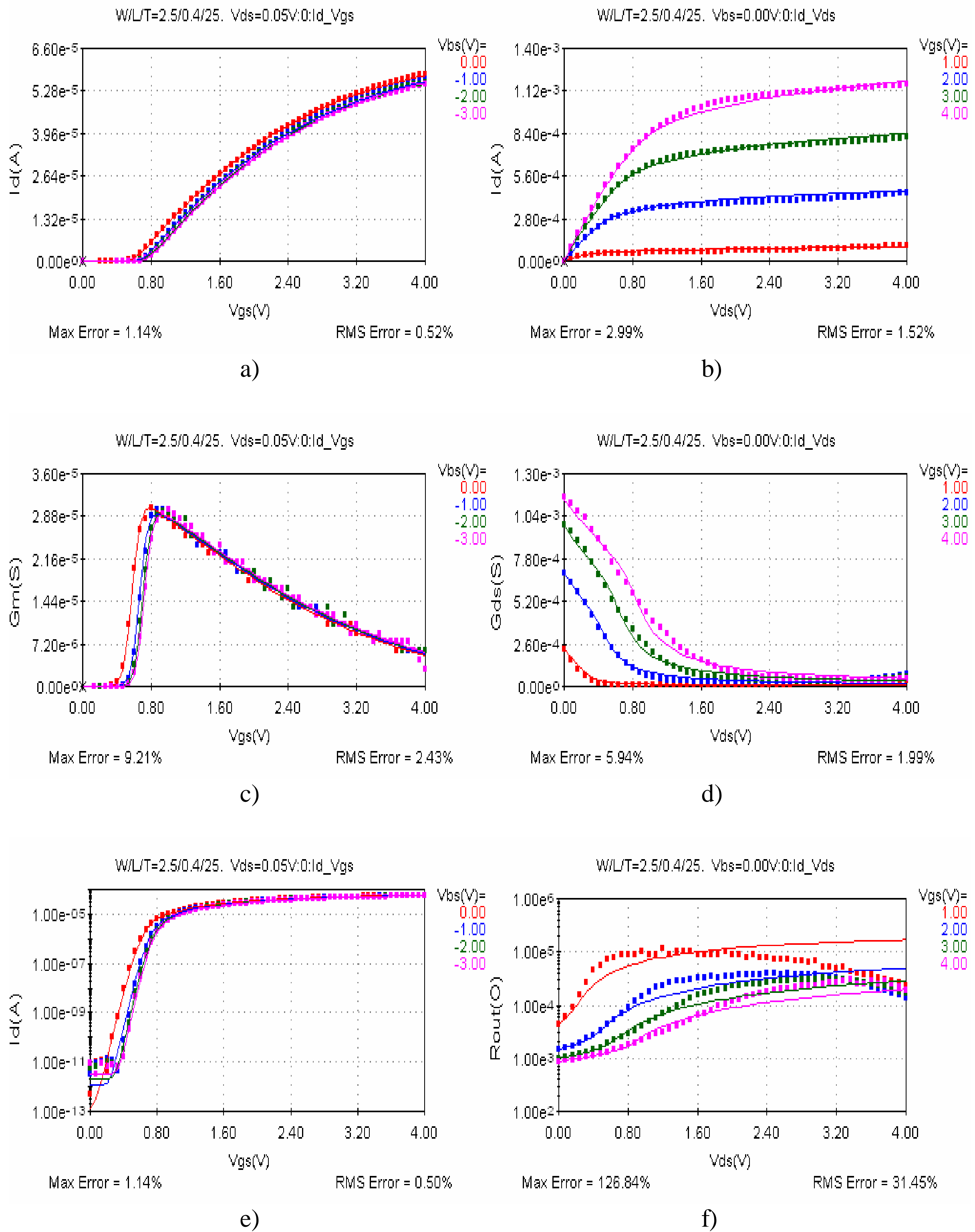

Fig. 19. L=0.4 μm W=2.5 μm NMOS

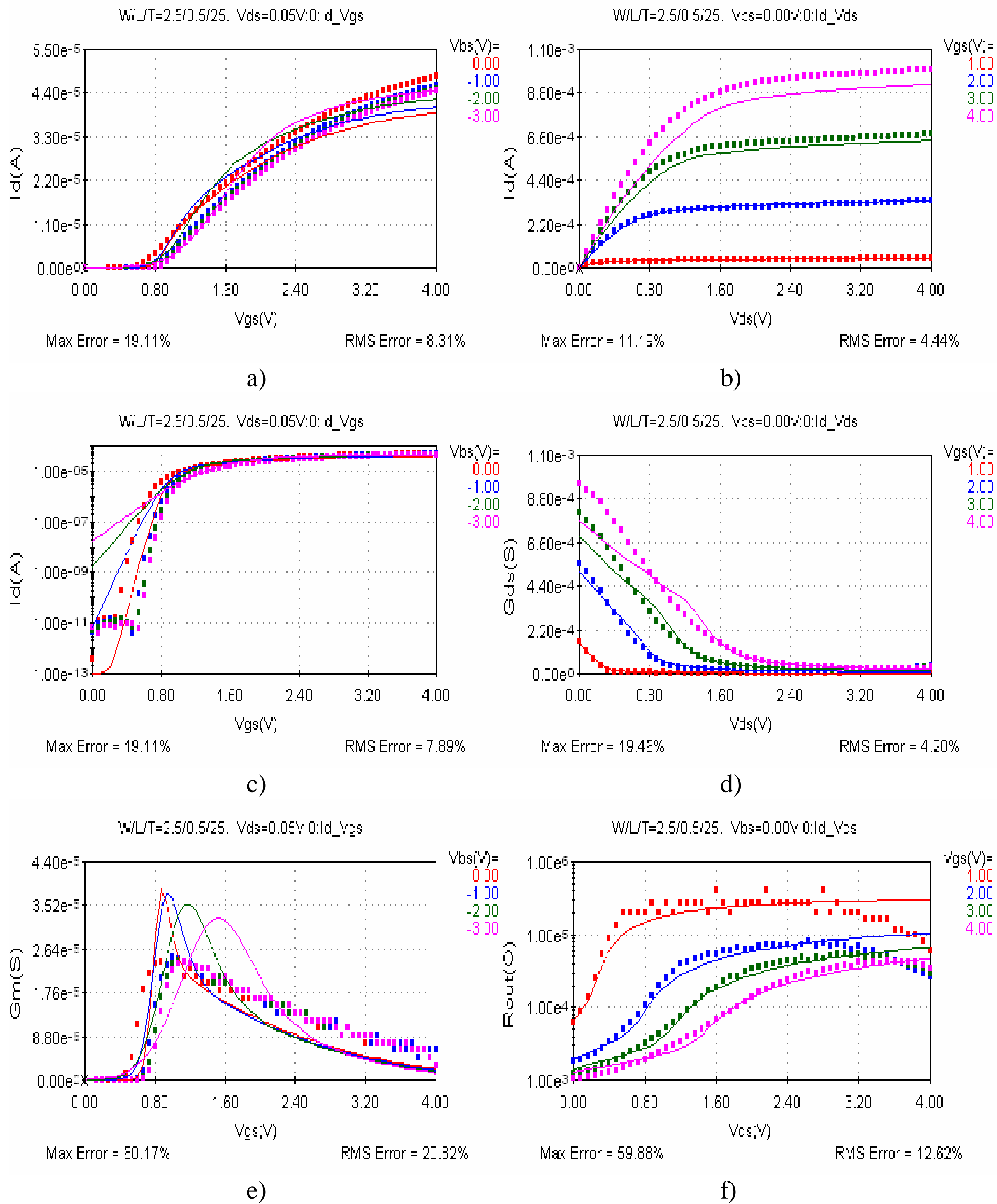

Fig. 20. L=0.5 μm W=2.5 μm NMOS

PMOS measured and simulated data

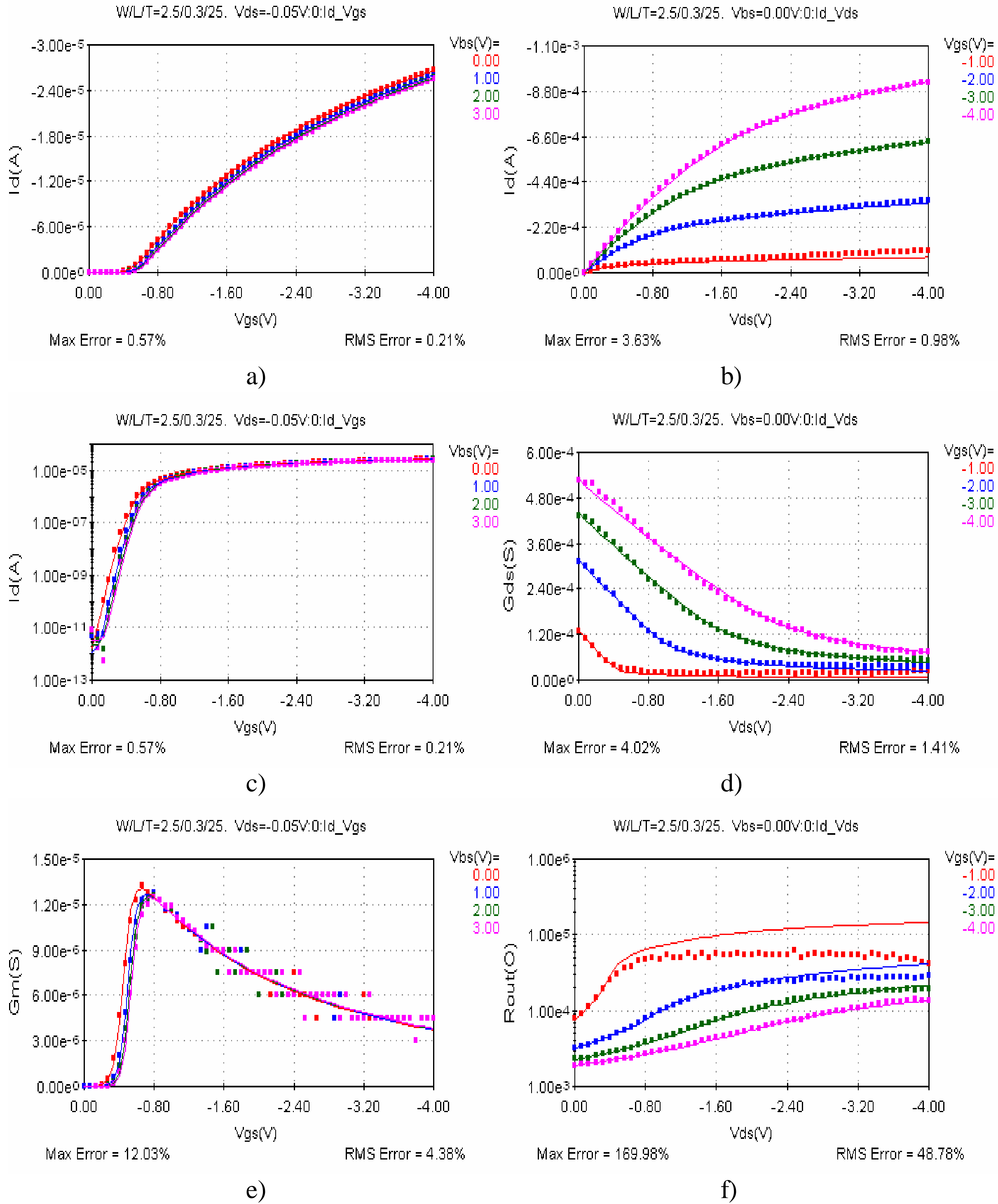

Fig. 21. L=0.3 µm W=2.5 µm PMOS

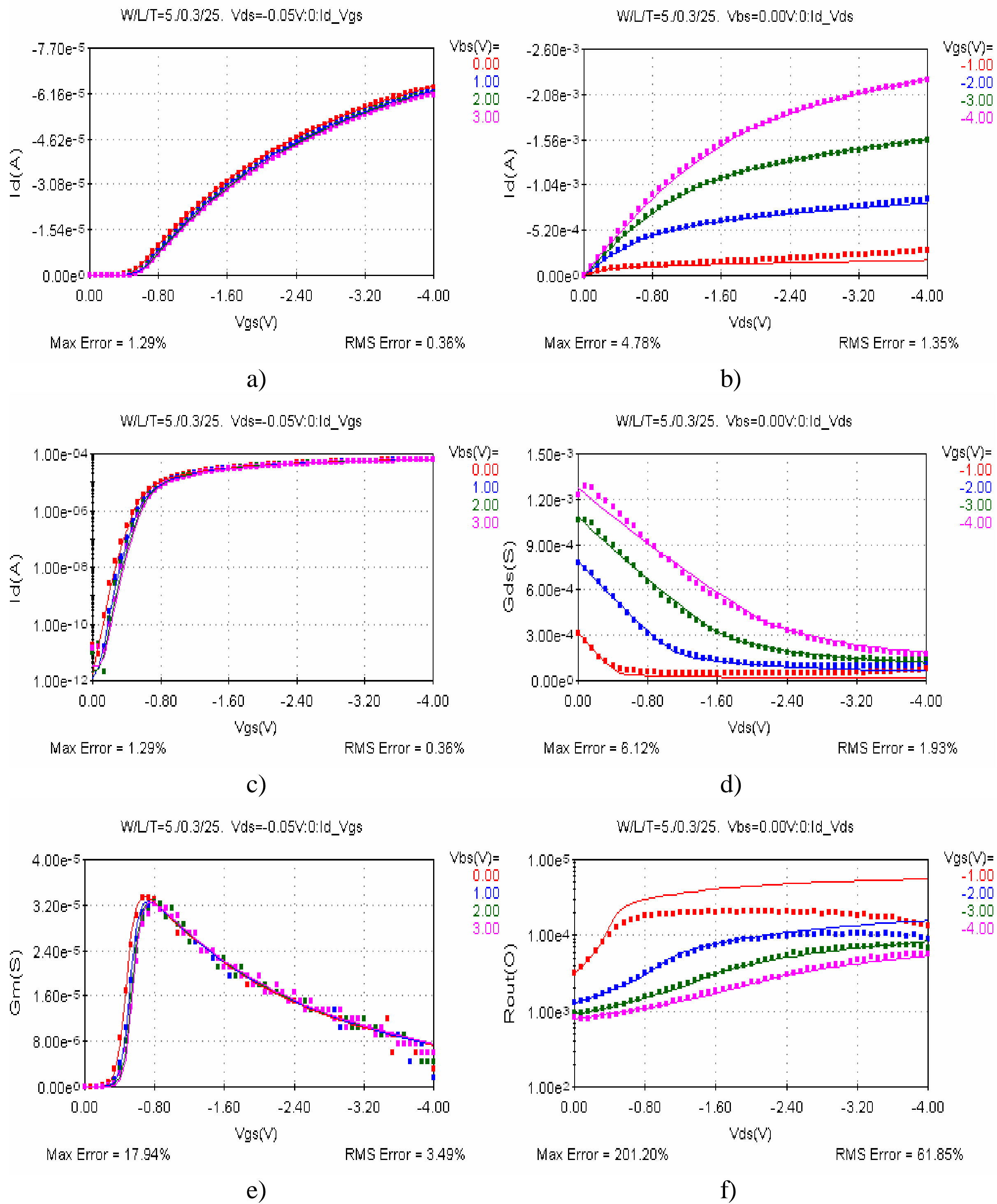

Fig. 22. L=0.3 µm W=5 µm PMOS

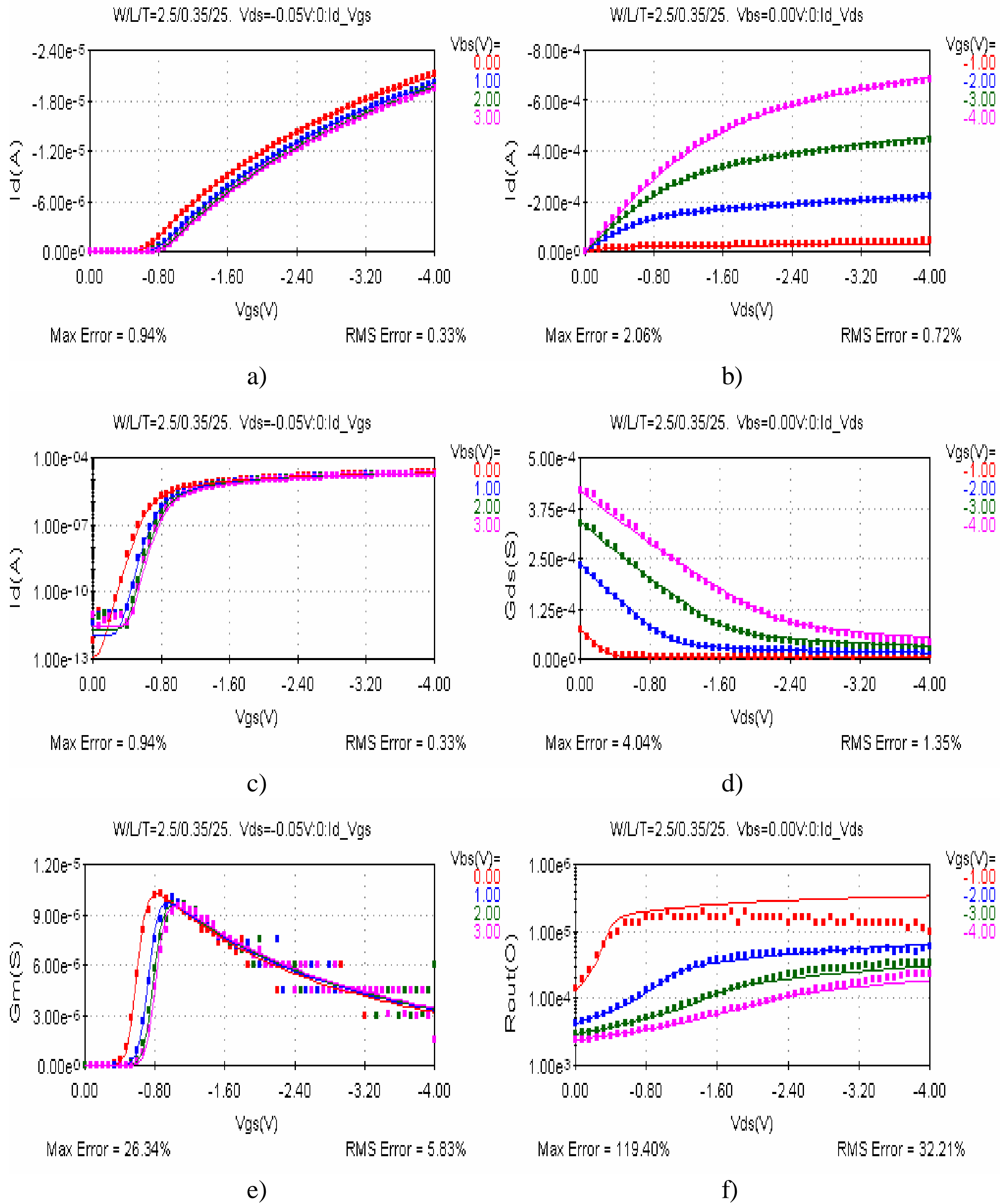

Fig. 23. L=0.35 µm W=2.5 µm PMOS

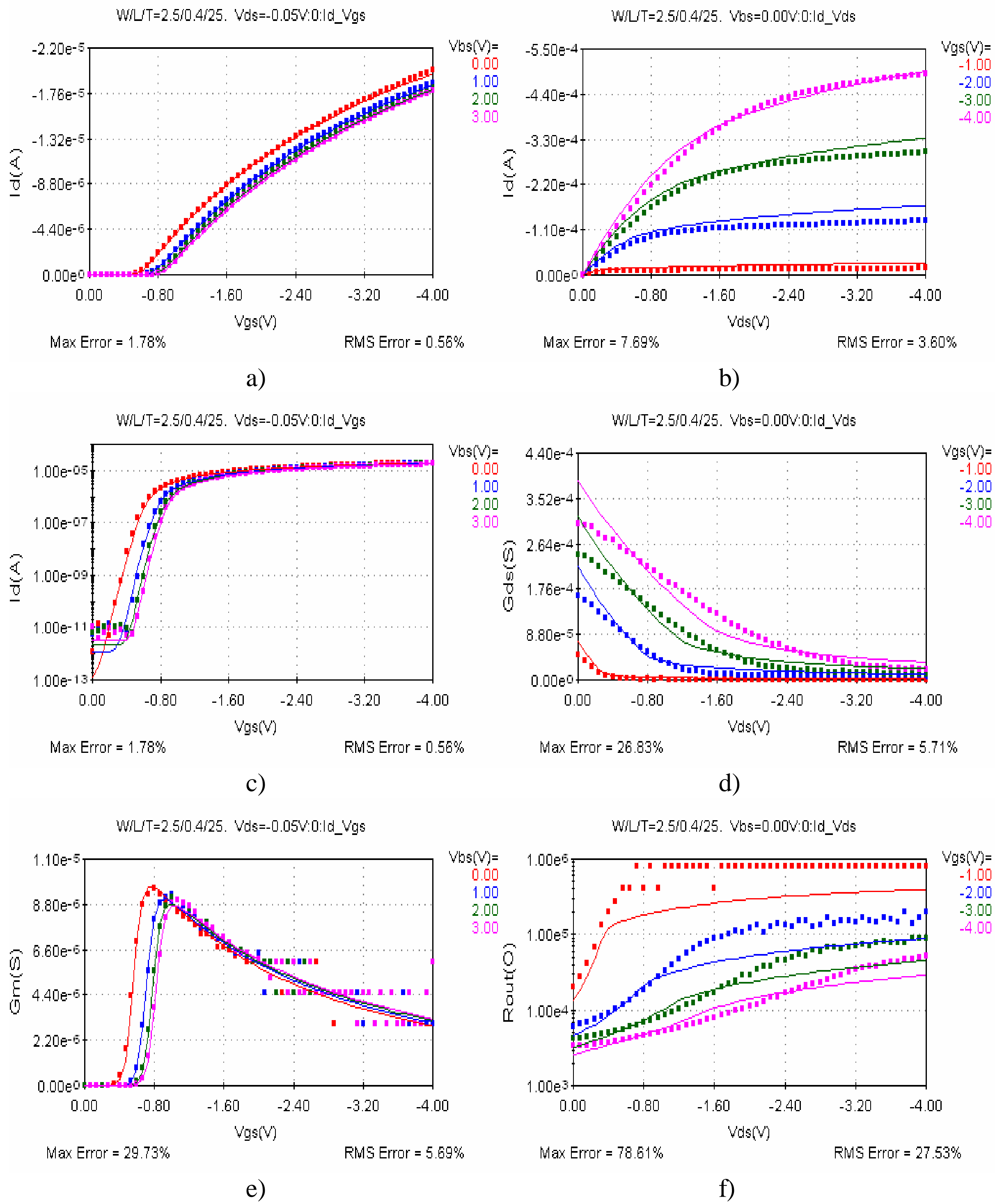

Fig. 24. L=0.4 µm W=2.5 µm PMOS

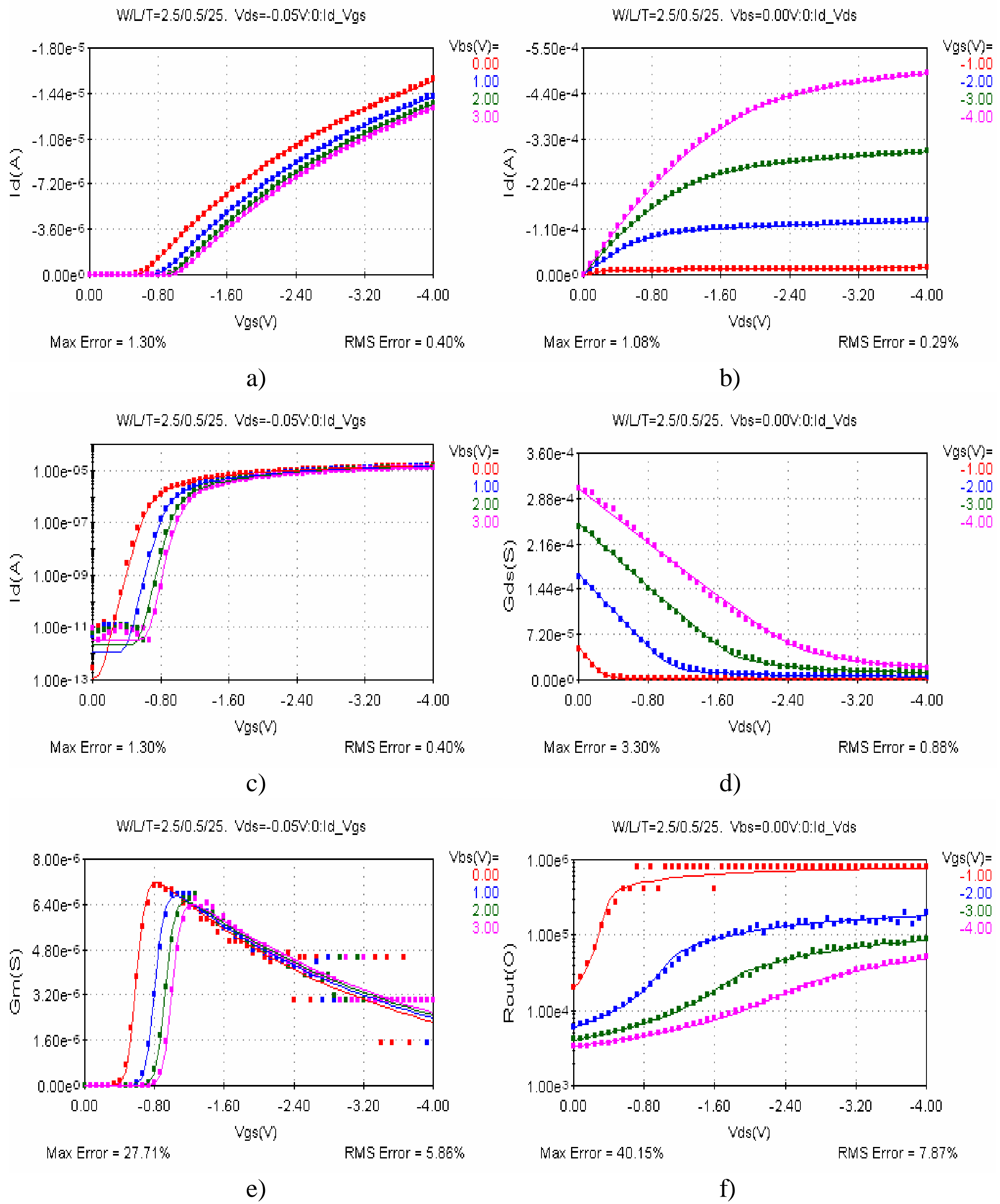

Fig. 25. L=0.5 μm W=2.5 μm PMOS

Appendix D

BSIMPro+ output: Model Cards

NMOS Model Card

```
simulator lang = spice
.model  default  bsim4 type = n
************************************************************
*            MODEL FLAG PARAMETERS
************************************************************
+lmin = 3e-007          lmax = 5e-007          wmin = 2.5e-006           wmax = 5e-006
+version = 4.2          binunit = 1            paramchk= 1               mobmod = 0
+capmod = 2             igcmod = 1             igbmod = 1                geomod  = 0
+diomod = 1             rdsmod = 0             rbodymod = 0              rgeomod = 0
+rgatemod = 0           permod = 1             acnqsmod = 0              trnqsmod = 0
************************************************************
*            GENERAL MODEL PARAMETERS
************************************************************
+tnom = 25              toxe = 8e-009          toxp = 8e-009             toxm = 8e-009
+dtox = 0               epsrox = 3.9           wint = 3.655979e-007      lint = 3.0324491e-008
+ll = 0                 wl = 0                 lln = 1                   wln = 1
+lw = 0                 ww = 6.249625e-013     lwn = 1                   wwn = 1
+lwl = 0                wwl = 0                xl = 0                    xw = 0
+xpart = 0              toxref = 8e-009        dlcig = 0
************************************************************
*            DC PARAMETERS
************************************************************
+vth0 = 0.59882077      k1 = 0.27674332        k2 = -0.064011355         k3 = 0
+k3b = 0                w0 = 0                 dvt0 = 0                  dvt1 = 0.536
+dvt2 = 0.1             dvt0w = 0              dvt1w = 0                 dvt2w = -0.032
+dsub = 0.56            minv = 0               voffl = -3.5248708e-011   dvtp0 = 0
+dvtp1 = 0              lpe0 = 0               lpeb = 0                  vbm = -3
+xj = 2.5e-007          ngate = 0              ndep = 1.7e+017           nsd = 1e+020
+phin = -0.2            cdsc = 2.5e-006        cdscb = 0.0001            cdscd = 0
+ci = 2.5e-006          voff = -0.10422467     nfactor = 0.8             eta0 = 0.08
+etab = 0               u0 = 0.030081558       ua = 1.1411154e-009       ub = 2.2886355e-018
+uc = 3.0968401e-011    eu = 1.67              vsat = 135247.06          a0 = 0.0012288195
+ags = 0.0044010481     a1 = 0                 a2 = 0.17772532           b0 = 0
+b1 = 0                 keta = -0.047          dwg = 0                   dwb = 0
+pclm = 1.2254079       pdiblc1 = 0.39         pdiblc2 = 0.0086          pdiblcb = 0
+drout = 0.56           pvag = 0.000999        delta = 0.01              pscbe1 = 4.24e+009
+pscbe2 = 1e-008        fprout = 0             pdits = 6.9451625e-016    pditsd = 0
+pditsl = 0             rsh = 0                rdsw = 1e-010             rsw = 25
+rdw = 25               rdswmin = 0            rdwmin = 0                rswmin = 0
+prwg = 0               prwb = 0               wr = 1                    alpha0 = 0
+alpha1 = 0             beta0 = 30             agidl = 0                 bgidl = 2.3e+009
+cgidl = 0.5            egidl = 0.8            aigbacc = 1               bigbacc = 0
+cigbacc = 0            nigbacc = 1            aigbinv = 0.35            bigbinv = 0.03
+cigbinv = 0.006        eigbinv = 1.1          nigbinv = 3               aigc = 0.43
+bigc = 0.054           cigc = 0.075           aigsd = 0.43              bigsd = 0.054
+cigsd = 0.075          nigc = 1               poxedge = 1               pigcd = 1
+ntox = 1               xrcrg1 = 12            xrcrg2 = 1
```

```
*          CAPACITANCE PARAMETERS
************************************************************
+cgbo = 0           cgdl = 0            cgsl = 0            clc = 1e-007
+cle = 0.6          ckappas = 0.6       ckappad = 0.6       vfbcv = -1
+acde = 1           moin = 15           noff = 1            voffcv = 0
************************************************************
*          TEMPERATURE PARAMETERS
************************************************************
+kt1 = -0.11        kt1l    = 0         kt2 = 0.022         ute = -1.5
+ua1 = 1e-009       ub1     = -1e-018   uc1 = -5.6e-011     prt = 0
+at = 0
************************************************************
*          NOISE PARAMETERS
************************************************************
+fnoimod = 1        tnoimod = 0         noia = 6.25e+041    noib = 3.125e+026
+noic = 8.75e+009   em = 41000000       af = 1              ef = 1
+kf = 0             tnoia = 1.5         tnoib = 3.5         ntnoi = 1
************************************************************
*          DIODE PARAMETERS
************************************************************
+jss = 0.0001       jsws = 0            jswgs = 0           njs = 1
+ijthsfwd= 0.1      ijthsrev= 0.1       bvs = 10            xjbvs = 1
+xjbvd = 1          pbs = 1             cjs = 0.0005        mjs = 0.5
+pbsws = 1          cjsws = 5e-010      mjsws = 0.33        cjswd = 5e-010
+mjswd = 0.33       pbswgd = 1          cjswgd = 5e-010     mjswgd = 0.33
+tpb = 0            tcj = 0             tpbsw = 0           tcjsw = 0
+tpbswg = 0         tcjswg = 0          xtis = 3
************************************************************
*          LAYOUT RELATED PARAMETERS
************************************************************
+dmcg = 0           dmdg = 0            dmcgt = 0           xgw = 0
+xgl = 0
************************************************************
*          RF PARAMETERS
************************************************************
+rshg = 0.1         gbmin = 1e-012      rbpb = 50           rbpd = 50
+rbps = 50          rbdb = 50           rbsb = 50           ngcon = 1
************************************************************
*          STRESS PARAMETERS
************************************************************
+saref = 1e-006     sbref = 1e-006      wlod = 0            kvth0 = 0
+lkvth0 = 0         wkvth0 = 0          pkvth0 = 0          llodvth = 0
+wlodvth = 0        stk2 = 0            lodk2 = 1           lodeta0 = 1
+ku0 = 0            lku0 = 0            wku0 = 0            pku0 = 0
+llodku0 = 0        wlodku0 = 0         kvsat = 0           steta0 = 0
+tku0 = 0
```

PMOS Model Card

```
simulator lang = spice
.model  default  bsim4 type = p
*****************************************************************
*          MODEL FLAG PARAMETERS
*****************************************************************
+lmin = 3e-007              lmax = 5e-007          wmin = 2.5e-006        wmax = 5e-006
+version = 4.2              binunit = 1            paramchk = 1           mobmod = 0
+capmod = 2                 igcmod  = 1            igbmod = 1             geomod = 0
+diomod = 1                 rdsmod  = 0            rbodymod = 0           rgeomod = 0
+rgatemod= 0                permod = 1             acnqsmod = 0           trnqsmod = 0
*****************************************************************
*          GENERAL MODEL PARAMETERS
*****************************************************************
+tnom = 25                  toxe = 8e-009          toxp = 8e-009          toxm = 8e-009
+dtox = 0                   epsrox = 3.9           wint = 4.3063752e-007 lint = 4.5707824e-008
+ll = 0                     wl = 0                 lln = 1                wln = 1
+lw = 0                     ww = 6.249625e-013     lwn = 1                wwn = 1
+lwl = 0                    wwl = 0                xl = 0                 xw = 0
+xpart = 0                  toxref = 8e-009        dlcig = 0
*****************************************************************
*          DC PARAMETERS
*****************************************************************
+vth0 = -0.62617037         k1 = 1.0075625         k2 = -0.20663782       k3 = 0
+k3b = 0                    w0 = 0                 dvt0 = 0.89352102      dvt1 = 0.18661813
+dvt2 = -0.067456025        dvt0w = 0              dvt1w = 5300000        dvt2w = -0.032
+dsub = 0.56                minv = 0               voffl = 0              dvtp0 = 0
+dvtp1 = 0                  lpe0 = -1.0887256e-014 lpeb = 0               vbm = -3
+xj = 2.4825e-007           ngate = 0              ndep = 1.7e+017        nsd = 1e+020
+phin = -0.0005960161       cdsc = 7.578125e-006   cdscb = -5e-005        cdscd = 1e-006
+cit = 0                    voff = 0               nfactor = 1            eta0 = 0.08
+etab = -8.4171766e-014     u0 = 0                 ua = 0                 ub = 0
+uc = 0                     eu = 1.67              vsat = 300000          a0 = 1.4
+ags = 1.025                a1 = 0                 a2 = 1                 b0 = 0
+b1 = 0                     keta = -0.047          dwg = 0                dwb = 0
+pclm = 0.15                pdiblc1 = 0.39         pdiblc2 = 0.0086       pdiblcb = 0
+drout = 0.56               pvag = 0.00101         delta = 0.01           pscbe1 = 4.24e+009
+pscbe2 = 1e-008            fprout = 0             pdits = 0              pditsd = 0
+pditsl = 0                 rsh = 0                rdsw = 0               rsw = 25
+rdw = 25                   rdswmin = 0            rdwmin = 0             rswmin = 0
+prwg = 0.02                prwb = 0               wr = 1                 alpha0 = 0
+alpha1 = 0                 beta0 = 30             agidl = 0              bgidl = 2.3e+009
+cgidl = 0.5                egidl = 0.8            aigbacc = 1            bigbacc = 0
+cigbacc = 0                nigbacc = 1            aigbinv = 0.35         bigbinv = 0.03
+cigbinv = 0.006            eigbinv = 1.1          nigbinv = 3            aigc = 0.43
+bigc = 0.054               cigc = 0.075           aigsd = 0.43           bigsd = 0.054
+cigsd = 0.075              nigc = 1               poxedge = 1            pigcd = 1
+ntox = 1                   xrcrg1 = 12            xrcrg2 = 1
*****************************************************************
```

```
*           CAPACITANCE PARAMETERS
**************************************************************
+cgbo = 0            cgdl = 0             cgsl = 0             clc = 1e-007
+cle = 0.6           ckappas = 0.6        ckappad = 0.6        vfbcv = -1
+acde = 1            moin = 15            noff = 1             voffcv = 0
**************************************************************
*           TEMPERATURE PARAMETERS
**************************************************************
+kt1 = -0.11         kt1l = 0             kt2 = 0.022          ute = -1.5
+ua1 = 1e-009        ub1 = -1e-018        uc1 = -5.6e-011      prt = 0
+at = 0
**************************************************************
*           NOISE PARAMETERS
**************************************************************
+fnoimod = 1         tnoimod = 0          noia = 6.25e+041     noib = 3.125e+026
+noic = 8.75e+009    em = 41000000        af = 1               ef = 1
+kf = 0              tnoia = 1.5          tnoib = 3.5          ntnoi = 1
**************************************************************
*           DIODE PARAMETERS
**************************************************************
+jss = 0.0001        jsws = 0             jswgs = 0            njs = 1
+ijthsfwd= 0.1       ijthsrev = 0.1       bvs = 10             xjbvs = 1
+xjbvd = 1           pbs = 1              cjs = 0.0005         mjs = 0.5
+pbsws = 1           cjsws = 5e-010       mjsws = 0.33         cjswd = 5e-010
+mjswd = 0.33        pbswgd = 1           cjswgd = 5e-010      mjswgd = 0.33
+tpb = 0             tcj = 0              tpbsw = 0            tcjsw = 0
+tpbswg = 0          tcjswg = 0           xtis = 3
**************************************************************
*           LAYOUT RELATED PARAMETERS
**************************************************************
+dmcg = 0            dmdg = 0             dmcgt = 0            xgw = 0
+xgl = 0
**************************************************************
*           RF PARAMETERS
**************************************************************
+rshg = 0.1          gbmin = 1e-012       rbpb = 50            rbpd = 50
+rbps = 50           rbdb = 50            rbsb = 50            ngcon = 1
**************************************************************
*           STRESS PARAMETERS
**************************************************************
+saref = 1e-006      sbref = 1e-006       wlod = 0             kvth0 = 0
+lkvth0 = 0          wkvth0 = 0           pkvth0 = 0           llodvth = 0
+wlodvth = 0         stk2 = 0             lodk2 = 1            lodeta0 = 1
+ku0 = 0             lku0 = 0             wku0 = 0             pku0 = 0
+llodku0 = 0         wlodku0 = 0          kvsat = 0            steta0 = 0
+tku0 = 0
```